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TECHNICAL MANUAL
AMX702

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Abstract:

This paper contains the drawings and the description of the AMX702 Asynchronous Telemultiplexor.

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FOREWORD

The AMX 702 is a reviced edition of AMX 701. The hardware is the same, but all the IC's have been replaced and renumbered, so the diagrams for AMX 701 or AMX 702 cannot be used for the other controller. The two editions are completely plug compatible and seen from a software point of view they are completely identically.

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MICROPROGRAM FOR THE AMX 702

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DESCRIPTION

The Asynchronous Multiplexer AMX 702 is a controller to the RC 3600 computer, which enables the computer to communicate with up to 8 asynchronous terminals.

Normally the multiplexer is connected to the terminals via the junction panel VJP 703.

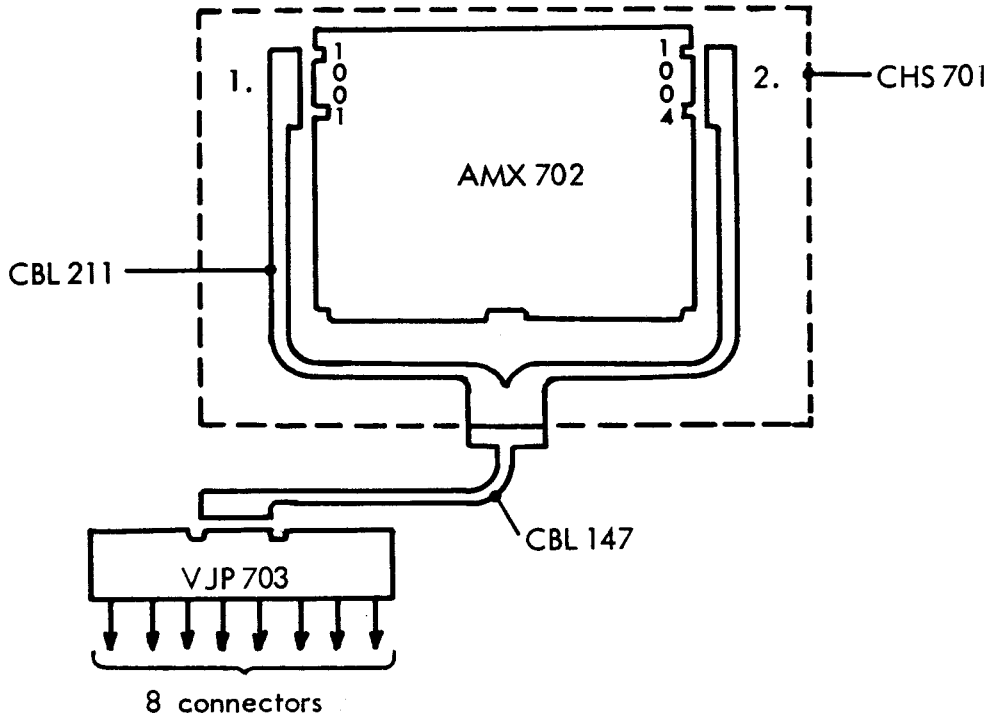

Fig. 1

DATA PATHS in AMX 702

Figure 2 shows the Data Paths in AMX 702, and is also a block diagram for the unit. In each block is written the page number showing where in the logic diagrams, each block is drawn. The function of the controller is described in the Programmers Reference Manual and its contents is supposed to be wellkonwn.

The description follows the diagrams for the Data Paths in AMX 702.

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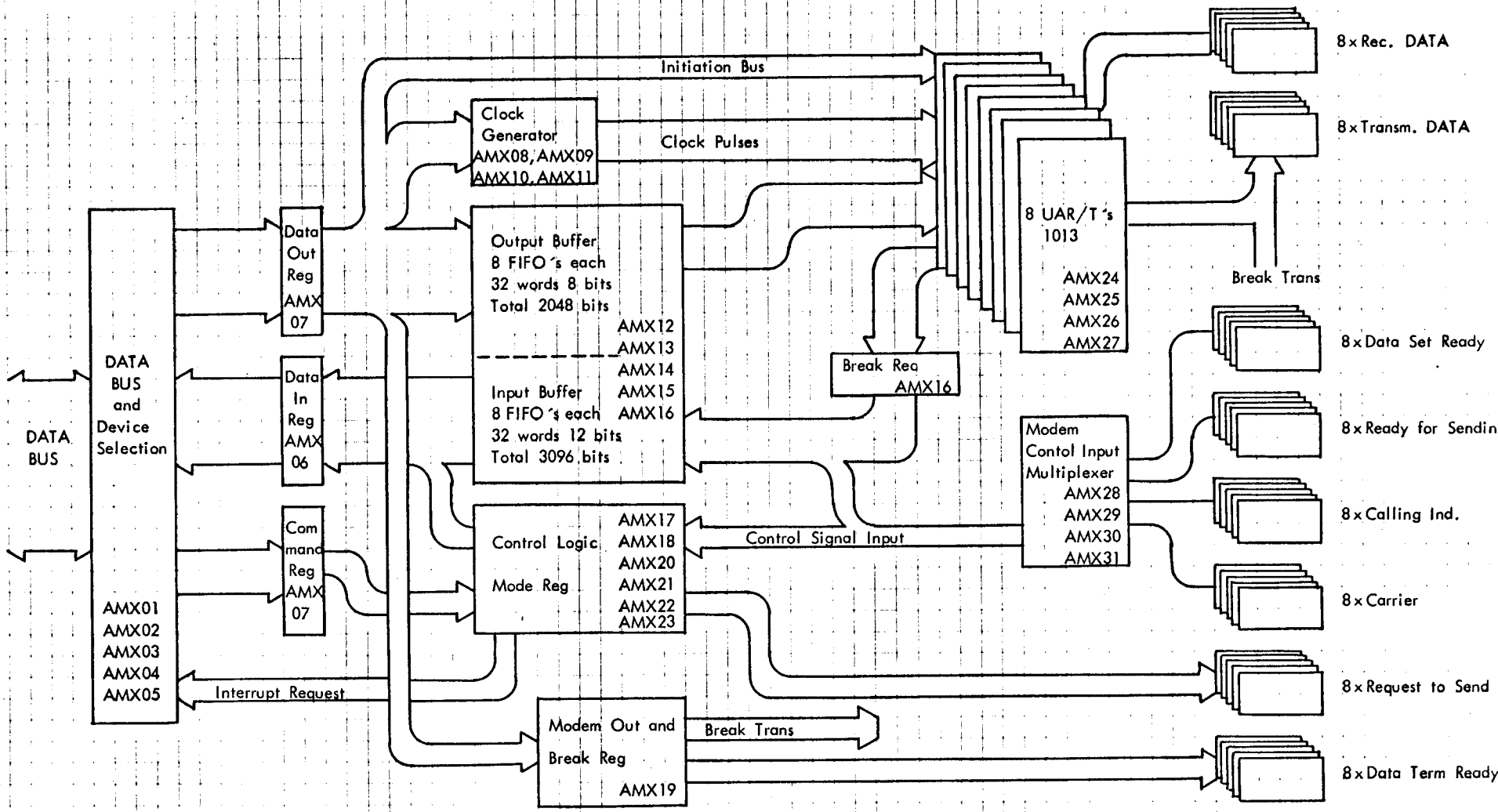


DATA PATH IN AMX 701/702

Figure 2

DATA BUS Connection and Device Selection

The bus connection is made in the normal way.

When a Data Out command with correct device number arrives, then the command is stored in Command Register, and the data is stored in the Data Out Register. The signal DATA OUT command is sent to the Control Logic to say that an event requesting action from Control Logic has occurred in the I/O Bus.

DATA OUT Register

In the DATA OUT Register the following information is stored:

1. After a DOA instruction the command is stored in bit (12:15), and the Channel No. in bit (5:7).
2. After a DOB instruction the character is to be transferred to the Output Buffer stored in bit (8:15) and the Channel No. in bit (5:7).
3. After a DOC instruction the initialization conditions are stored in bit (10:15).

DATA IN Register

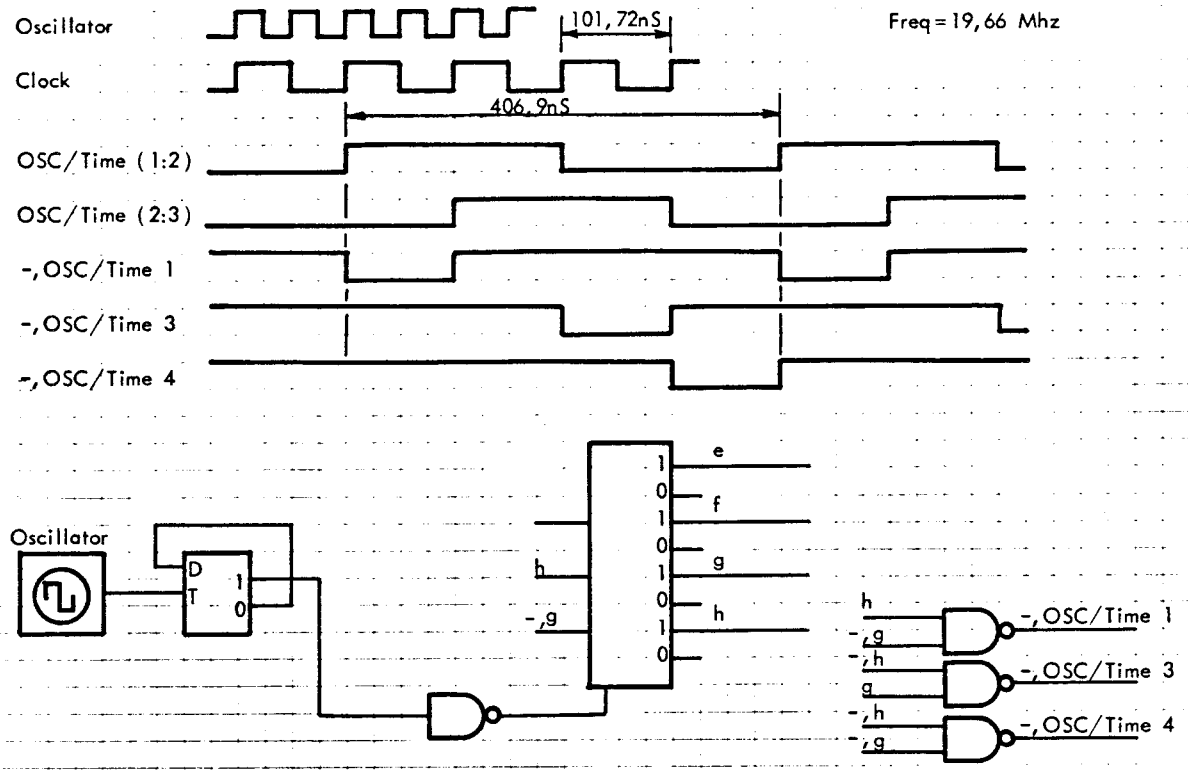
Input characters, their status bits and status information concerning the controller itself are stored in the DATA IN Register.

CLOCK Generator

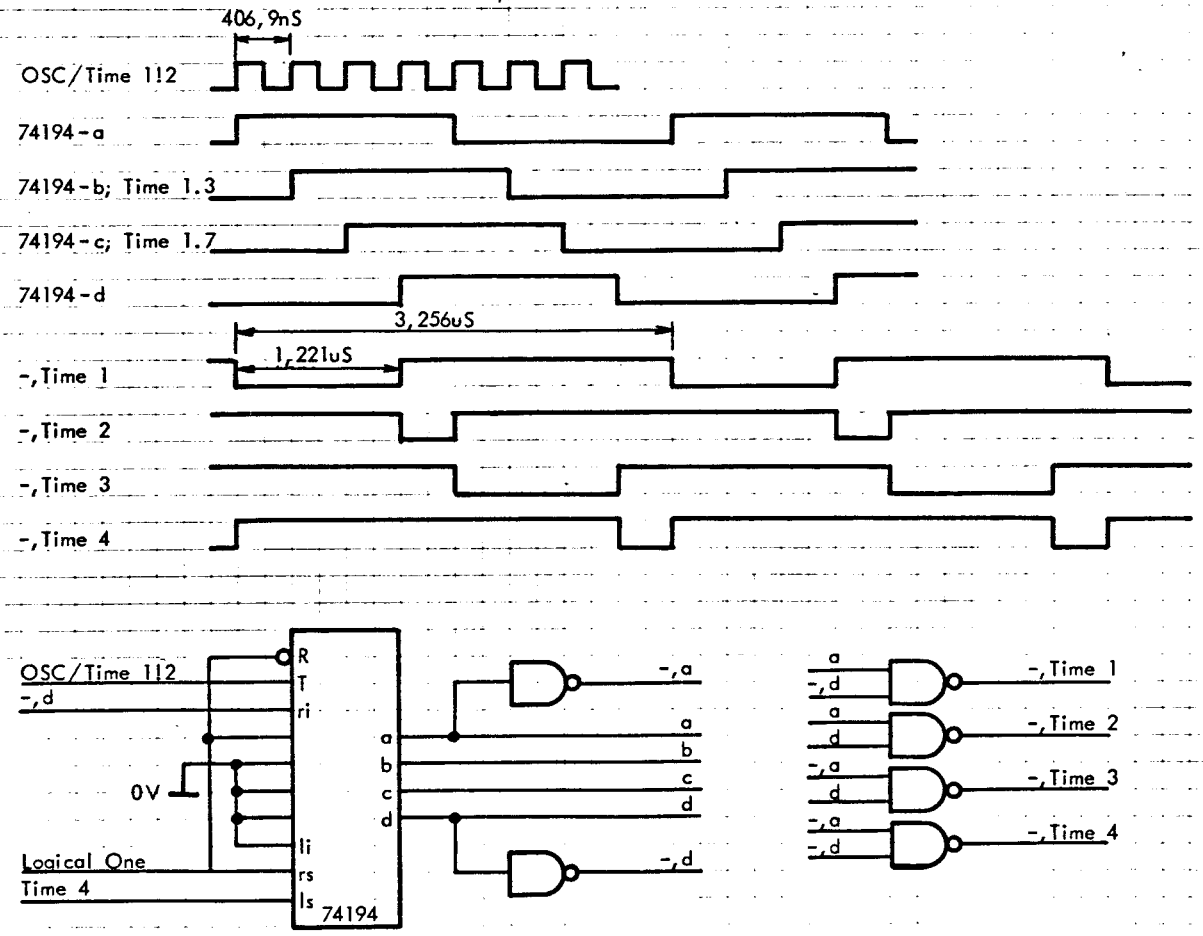
The CLOCK Generator generates clock pulses for:

1. Oscillator Clock System
2. Logic Clock System
3. Clock pulses to the UAR/T's.

TIMING for OSCILLATOR CLOCK SYSTEM



TIMING for LOGIC CLOCK SYSTEM



AMX 701
AMX 702

TIMING DIAGRAM FOR MASTER CLOCK GENERATOR
LOGIC DIAGRAM AMX 08

Figure 3

R 11282

Clock Generator, continued:

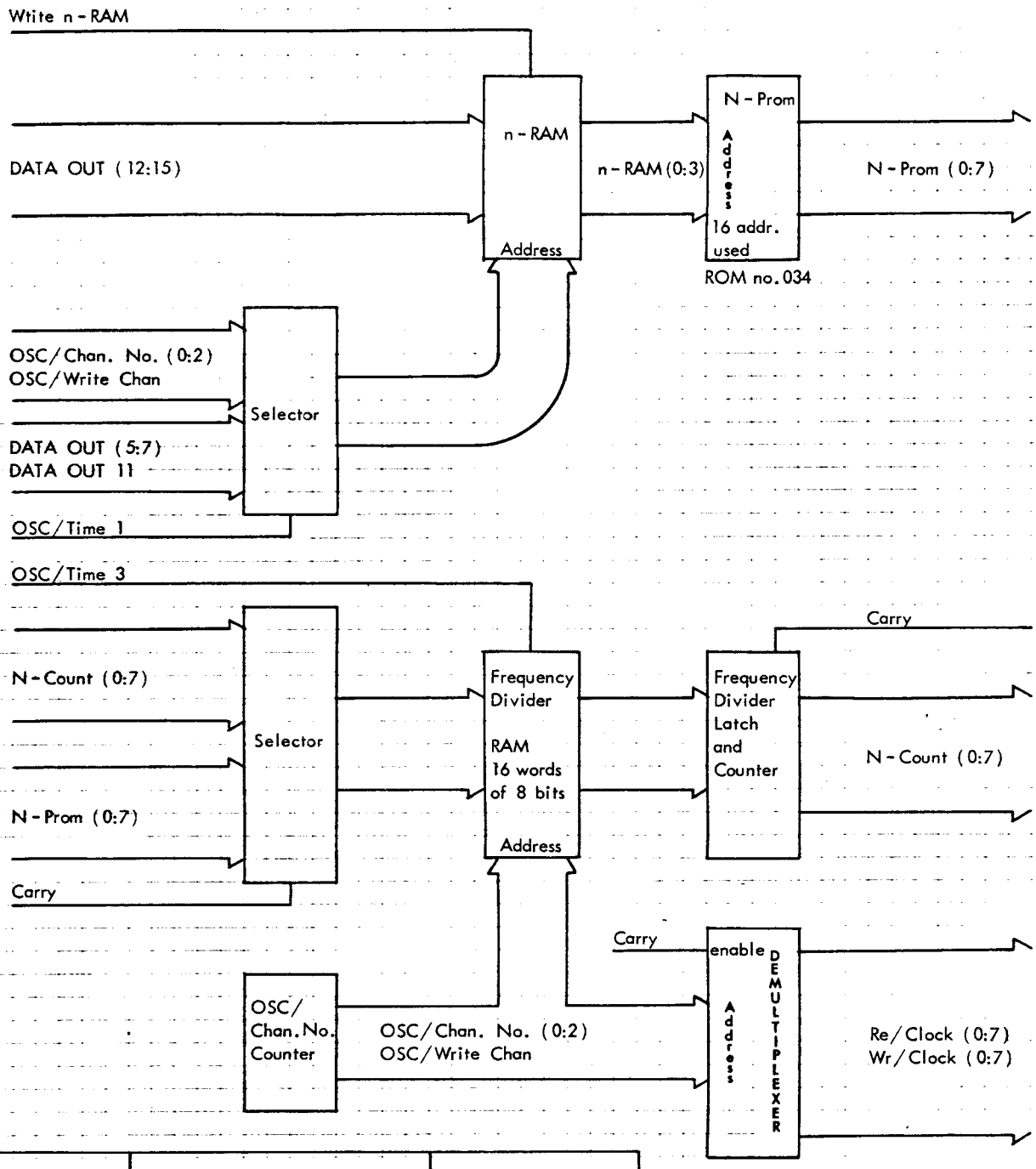
The two first systems are described in the timing diagram on figure 3 and the logic diagram AMX 08.

A block diagram of the clock pulses to the UAR/T's is provided in Figure 4. The UAR/T is a Universal Asynchronous Receiver/Transmitter and is a Large Scale Integrated Circuit. The UAR/T needs clock pulses for both the receiver and the transmitter parts. The clock pulses to the UAR/T must have a frequency 16 times the required bit rate. In AMX 702 the bit rate is controlled by the program, which may use different bit rates for receiver and for transmitter.

The OSC/Chan. No. Counter is a free running counter and its output is used as address for the different RAM's and demultiplexers in the circuit. The circuit is running in four steps and in these four steps the circuits take care of the clock for the receiver or the transmitter part of one channel.

The functions of the circuit in each step are:

1. The OSC/Chan. No. Counter changes and addresses an 8 bit number in the Frequency Divider RAM.
2. The number stored in the RAM is loaded into the Frequency Divider Latch and Counter.
3. The number in the Frequency Divider Latch and Counter is increased by one, and the Carry is one if the new number is 240, else it is zero.
4. If Carry is zero the new number is written back into the same position in the Frequency Divider RAM. If Carry is one the clock is set to one in the right flip-flop in the demultiplexer, and a number is written into the Frequency Divider RAM from N-Prom. The output from the N-Prom is a coding of the contents of the n-RAM.



Time (shifting to)	Action	Action if DOC instruction
1	Change Chan. No.	
2	Load Latch	Write n - RAM
3	Count in Latch	
4	Write back in RAM Set Clock = 1 if Carry	

AMX 701/
AMX 702

BLOCK DIAGRAM FOR GENERATION OF CLOCK
TO UAR/T
Logic Diagram AMX 09, AMX 10, AMX 11

Figure 4

A 11283

CLOCK Generator, continued:

If the addressed n-RAM contains the number 3, it means the channel has to operate at 1200 bps (see section 3.2 in the Reference Manual). The number 3 in the n-RAM is converted to the number 232 by the N-Prom, and after a Carry the number written into the Frequency Divider, RAM is 232 in this case. Next time the channel is addressed by the OSC/Chan. No. Counter, the number 232 is loaded into the Latch, and increased by one, and written back in the RAM again. This is repeated until the number in the Latch is 240, which gives a Carry, sets the clock flip-flop to one again and loads the RAM back to 232. In this way the clock flip-flop is set to one at a rate 8 times lower than the maximum bit rate 240-232=8. The maximum bit rate is 9600 bps, so in this case the bit rate will be 1200 bps.

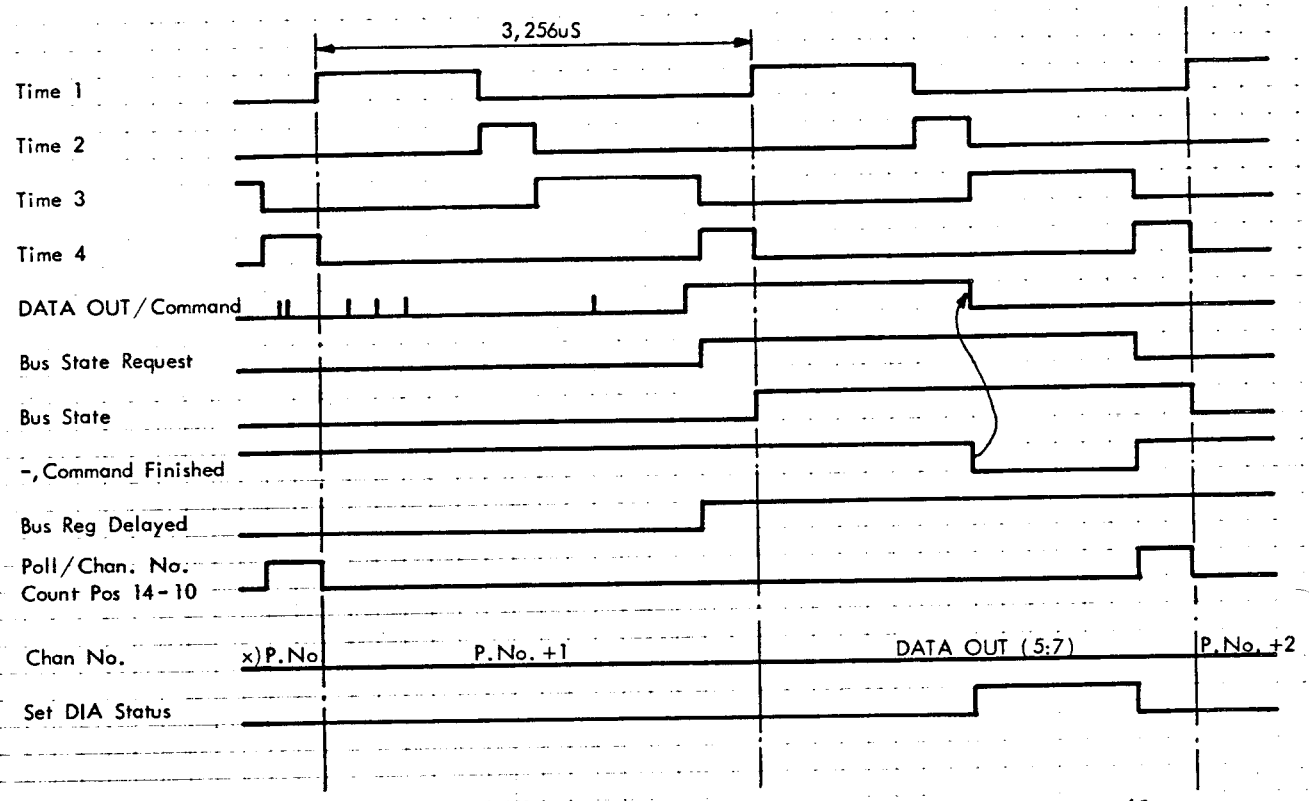
The contents of the n-RAM is changed by a DOC command with DATA OUT 10=1. Figure 5 shows the timing for the DOC command. The new contents of the n-RAM are written into the RAM at OSC/Time 1 and has no unwanted influence on the operation of the Frequency Divider.

OUTPUT BUFFER and INPUT BUFFER

The AMX 702 contains 8 channels and each channel contains an Output Buffer and an Input Buffer. Each Output Buffer has 32 words of 8 bits and each Input Buffer has 32 words of 12 bits. The buffers are "first in first out" buffers (FIFO) and the block diagram on figure 6 shows how these 16 FIFO's are made out of 5 RAMs, each containing 256 words of 4 bits.

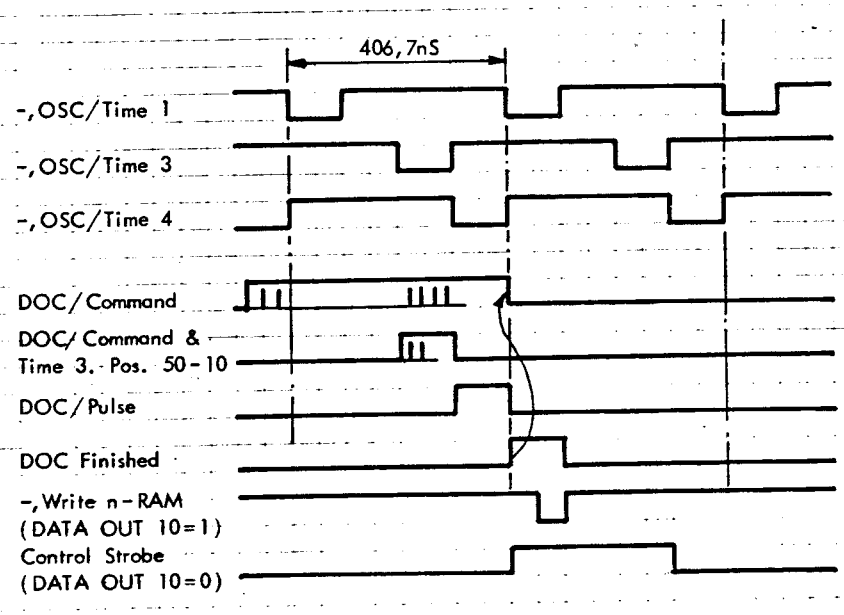
The buffer is addressed by the Write Pointer (used when writing into a buffer) or the Read Pointer (used when reading from a buffer) and by the Chan. No. (0:2). The Chan. No. is used as the three most significant bits in the addressing.

CLOCK for DOA or DOB COMMAND



x) P.No. is the number, which is stored in the Poll Channel Number Counter pos. 63.

CLOCK for DOC COMMAND

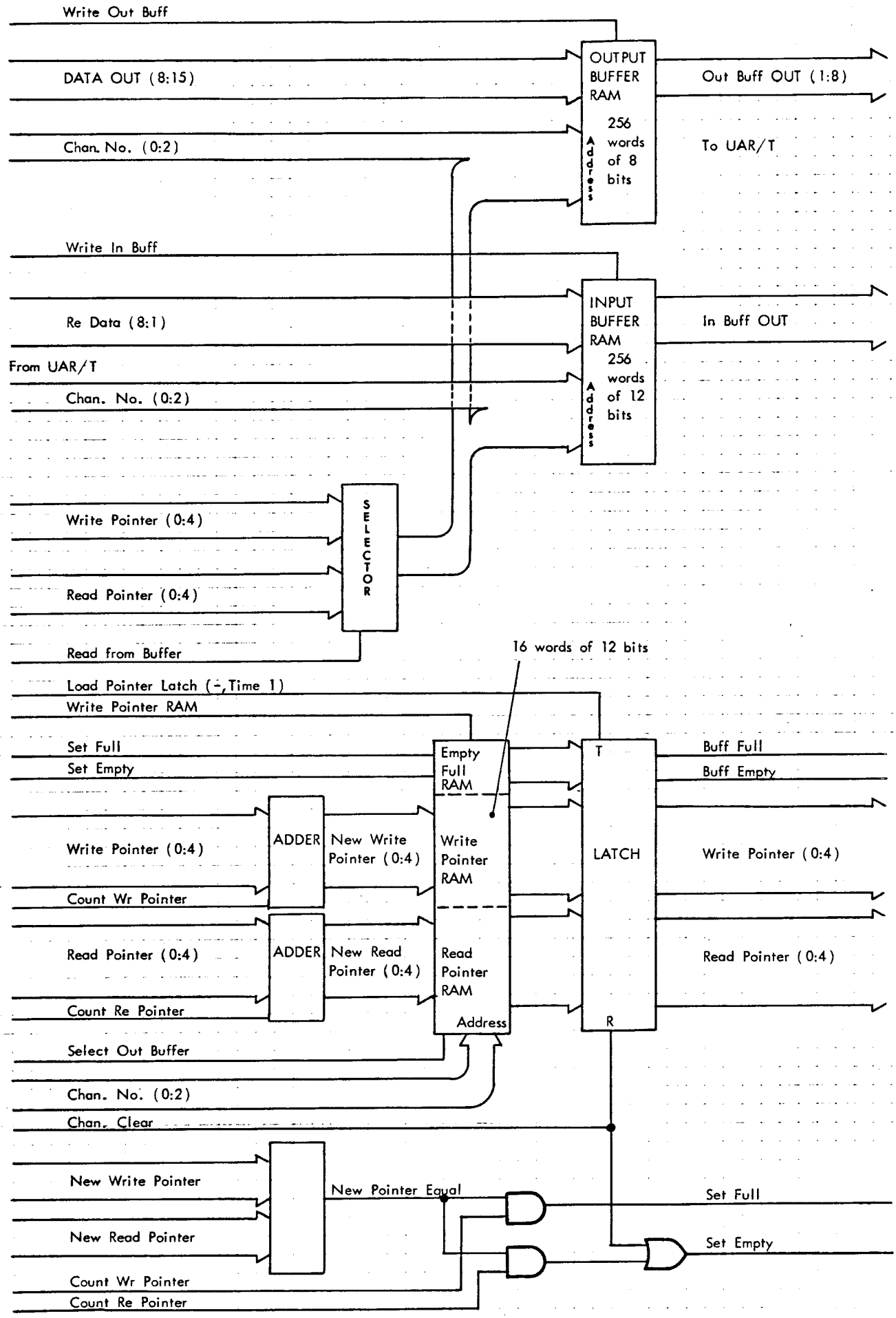


AMX 702

R 12114

TIMING DIAGRAM FOR DOA, DOB AND DOC COMMAND
Logic Diagram AMX 08 and AMX 17

Figure 5



AMX 701
AMX 702

BLOCK DIAGRAM FOR POINTERS AND BUFFERS
Logic Diagram AMX 12, AMX 13, AMX 14 and AMX 15

Figure 6

R 11285

OUTPUT BUFFER and INPUT BUFFER, continued:

When the Control Logic want to read a character from the Input Buffer it is done in the following way:

1. The correct Write Pointer, Read Pointer and Empty Full status is addressed, and loaded into the Latch.
2. The Input Buffer is now addressed and if Buff Empty = 0, then a strobe is sent to the Data In Reg loading the contents of the addressed cell in the Input Buffer into the Data In Reg.
3. If Buff Empty = 0 the Control Logic sets Count Re Pointer = 1 and the new Read Pointer is increased by one. Now the new Read Pointer and the new Write Pointer are compared and if they are equal the set Empty signal goes to one.
4. The new Read Pointer and the new Write Pointer are written into the Pointers RAM again and in case of Buff Empty = 0, the Read Pointer is increased by one. If the new Pointer is equal after a Read, this means that the buffer goes empty and the status is stored in the Empty Full RAM, too. (If they go equal during a write this means that the buffer goes full and this is stored, too).

Writing from a buffer is almost the same. What is different is that the Write Pointer is increased instead of the Read Pointer, and that a strobe is sent to the UARIT instead of the Data In Reg.

Clearing a buffer is done by means of the Control Logic by setting all bits in Read and in Write Pointer to logical one and by setting the Empty bit to one.

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

The Universal Asynchronous Receiver/Transmitter (UAR/T) in the AMX702 is an LSI device constructed on a single monolithic chip utilizing MTNS P-channel enhancement mode transistors. The controller uses 8 UAR/T's, one for each channel. Each UAR/T contains a Receiver part, a Transmitter part and Control part common for both the Receiver part and the Transmitter part.

1. Receiver part.

   When a character is received it is checked for correct parity and for correct stopbit, and the character is stored in the Re Data Reg in the UAR/T. The signal Re Data Available goes to one, telling the Control Logic that a character and its status bits are ready. The output from the UAR/T is tristate logic and the Control Logic is polling the Re Data Registers in the UAR/T's by setting the signal Enable Re Data to one, which transfers the data from the Re Data Reg to the output of the UAR/T. When the Control Logic has transferred a character and its status bits from Re Data Reg to the Input Buffer, it sets the signal Reset Data Available to one, which resets the signal Re Data Available.

2. Transmitter part.

   The Control Logic transfers data from the Output Buffer to the UAR/T by setting the signal Write Strobe to one, which loads the character into Data Holding Register in the UAR/T. The UAR/T starts to transmit the character with a start bit, 5 to 8 data bits, and possibly one parity bit (odd or even), and with one or two stop bits. When the Data Holding Register can accept a new character the signal Trans Buffer Empty goes to one.

3. Control part.

   The Control part of the UAR/T takes care of the following parameter for the Receiving and Transmitting:

   1. Char. length (5,6,7 or 8 bits).
   2. Odd/even parity or no parity.
   3. one or two stop bits (only for transmitting).

   Which parameter a UAR/T has to use is loaded in the Control Bit Holding Register in the UAR/T by a DOC command. The DOC command sets the signal Control Strobe to one , loading the DATA OUT (11:15) into the Control Bit Holding Register as shown on figure 5.

MODEM CONTROL INPUT MULTIPLEXER

The Modem Control Input signal is multiplexed, so that the input from the correct channel is avaiable for the Control Logic.

MODEM OUT and BREAK REGISTER

These two registers are constructed on two addressable Latches. The IORST sets all signals to logical zero.

CONTROL LOGIC

The Control Logic controlling the 8 UAR/T's, the Output Buffer, the Input Buffer, the Data Out Register and the Data In Register. Figure 5 shows a timing diagram for the Control Logic. The unit has two states namely the Bus State and the Poll State.

In Bus State the logic takes care of DOA commands, DOB commands and IORST, and the Chan. No. is DATA OUT (5:7) for the DOA and the DOB command.

In the Poll State the Control Logic senses the Modem Control Input signals, it transfers data from Output Buffer to the UAR/T or it transfers received data from UAR/T to the Input Buffer. The Chan. No. is now the output from the Poll/Chan. No. counter, like it is under a IORST, although an IORST is executed in Bus State.

The timing diagram shows how the signal DATA OUT/command sets the Bus State Request flip-flop, which stops the Poll/Chan. No. counter, and sets the unit in Bus State. In Bus State the signal Command Finished clears the DATA OUT/command signal and ends the Bus State.

CONTROL LOGIC, continued:

The IORST sets the Bus State and the AMX/Reset Reg, and sets the Poll/Chan. No. counter to zero. Poll/Chan. No. is used as Chan. No. during AMX/Reset and Command Finished is not set to one until Poll/Chan. No. 8 is one. Poll/Chan. No. 8 is one when the counter has reached to 8 and All Channel is then cleared by AMX/Reset.

The microprogram run by the Control Logic is explained in details in the 8 pages for Bus State for AMX 702 and in the 3 pages for Poll State for AMX 702. The microprogram used by the Logic in Bus State is determined by the arrived command, and for the Poll State it is determined by priority logic in the controller.

The priority is:

1. Poll/Modem Status
2. Poll/Re Data
3. Poll/Trans Data

INTERRUPT REQUEST

The controller has no BUSY flag and no DONE flag, but it can send an Interrupt Request. It has a flip-flop called Dummy DONE, which operates like a normal DONE flag but it cannot be sensed by the program. Dummy DONE is set by the Control Logic when input arrives to the Input Buffer and when an Output Buffer goes empty. Dummy DONE is only set to one if the controller has sent the command Enable Interrupt and setting Dummy DONE clears the Enable Interrupt flip-flop. If Dummy DONE is one and if Interrupt Disable is zero, the controller sends an Interrupt Request. Interrupt Disable is controlled by Mask bit 2.

BUS STATE for AMX 701/AMX 702

Time (shifting to)	AMX / Reset (IORST)	
1.3	Set Receive-mode and Transmit-mode Register Set Modem signal Register	
1.7		
2	Load Pointer Latch x) Load Buff Full Reg Load Buff Empty Reg	
3	Load DIA Status Reg	Set Select Out Buffer = 0 Set Count Re Pointer = 0 Set Count Wr Pointer = 0 Set Read from Buffer = 0 Set Chan. Clear = 0
4	Set Receive-mode = 0 Set Transmit-mode = 0	

x) Set DATA TERM READY OFF

Set Trans Data to logic one (Stop Break)

Microprogram for AMX 701/AMX 702

AMX / Reset

BUS STATE for AMX 701/AMX 702

Time (shifting to)	DOA/Command Receive, Stop Receive Transmit, Stop Transmit	
1.3	Set Receive-mode and Transmit-mode Register Set Modem signal Register	
1.7		
2	Load Pointer Latch Load Buff Full Reg Load Buff Empty Reg	
3	Load DIA Status Reg	Set Count Re Pointer = 0 Set Count Wr Pointer = 0 Set Read from Buffer = 0 If Transmit = 1 Then Select Out Buffer = 1 If Receive ! Transmit = 1 And DATA OUT 11 = 1 Then Chan. Clear = 1
4	If Chan. Clear = 1 Then Write Pointer RAM x)	

x) If Receive = 1 Then Set Receive-mode = 1
If Stop Receive = 1 Then Set Receive-mode = 0
If Transmit = 1 Then Set Transmit-mode = 1
If Stop Transmit = 1 Then Set Transmit-mode = 0

Microprogram for AMX 701/702

DOA/Command

BUS STATE for AMX 701/AMX 702

Time (shifting to)	DOA/Command Select In Buffer	
1.3	Set Receive-mode and Transmit-mode Register Set Modem signal Register	
1.7		
2	Load Pointer Latch Load Buff Full Reg Load Buff Empty Reg	
3	Load DIA Status Reg If Buff Empty = 1 Then Set Empty Status	Set Select Out Buffer = 0 Set Count Re Pointer = 1 Set Count Wr Pointer = 0 Set Read from Buffer = 1 Set Chan. Clear = 0
4	If Buff Empty = 0 Then Write Pointer RAM	

Microprogram for AMX 701/AMX 702

DOA/Command

BUS STATE for AMX 701/AMX 702

Time (shifting to)	DOA/Command Select Modem Status	
1.3	Set Receive-mode and Transmit-mode Register Set Modem signal Register	
1.7		
2	Load Pointer Latch Load Buff Full Reg Load Buff Empty Reg	
3	Load DIA Status Reg Setting: DIA DATA 0=Calling Ind Reg DIA DATA 1=Carrier Reg DIA DATA 2=Data Set Ready Reg	Set Select Out Buffer = 0 Set Count Re Pointer = 0 Set Count Wr Pointer = 0 Set Read from Buffer = 0 Set Chan. Clear = 0
4		

BUS STATE for AMX 701/AMX 702

<table>
<tr><td>Time
(shifting to)</td><td colspan="2">DOA/ Command
Select In Buff Status
Select Out Buff Status</td></tr>
<tr><td>1.3</td><td colspan="2">Set Receive-mode and Transmit-mode Register
Set Modem signal Register</td></tr>
<tr><td>1.7</td><td colspan="2"></td></tr>
<tr><td>2</td><td colspan="2">Load Pointer Latch
Load Buff Full Reg
Load Buff Empty Reg</td></tr>
<tr><td>3</td><td>Load DIA Status Reg
Setting:
DIA DATA 0 = Not Buff Full
DIA DATA 1 = Buff Empty
DIA DATA 2 = Logical zero</td><td rowspan="2">Set Count Re Pointer = 0
Set Count Wr Pointer = 0
Set Read from Buffer = 0
Set Chan. Clear = 0
If Select Out Buff Status = 1
Then Select Out Buffer = 1</td></tr>
<tr><td>4</td><td></td></tr>
</table>

Microprogram for AMX 701/AMX 702

DOA/ Command

BUS STATE for AMX 701 /AMX 702

Time (shifting to)	DOA/Command Set Data Term. Ready, Clear Data Term. Ready, Start Break, Stop Break	
1.3	Set Receive-mode and Transmit-mode Register Set Modem signal Register	
1.7		
2	Load Pointer Latch x) Load Buff Full Reg Load Buff Empty Reg	
3	Load DIA Status Reg	Set Select Out Buffer = 0 Set Count Re Pointer = 0 Set Count Wr Pointer = 0 Set Read from Buffer = 0 Set Chan. Clear = 0
4		

x) If Set Data Term. Ready = 1 Then Set DATA TERM READY ON
If ClearData Term. Ready = 1 Then Set DATA TERM READY OFF
If Start Break = 1 Then Set Trans Data to logic zero
If Stop Break = 1 Then Set Trans Data to logic one

Microprogram for AMX 701/AMX 702

DOA/Command

BUS STATE for AMX 701 /AMX 702

Time (shifting to)	DOA/ Command Clear One Character	
1.3	Set Receive - mode and Transmit - mode Register Set Modem signal Register	
1.7		
2	Load Pointer Latch Load Buff Full Reg Load Buff Empty Reg	
3	Load DIA Status Reg Setting: DIA DATA 0 = Not Set Empty DIA DATA 1 = 0 DIA DATA 2 = 0	Set Select Out Buffer = 1 Set Count Re Pointer = 1 Set Count Wr Pointer = 0 Set Read from Buffer = 0 Set Chan. Clear = 0
4	If Buff Empty = 0 Then Write Pointers RAM	

Microprogram for AMX 701/AMX 702

DOA/ Command

BUS STATE for AMX 701 /AMX 702

Time (shifting to)	DOB/Command	
1.3	Set Receive-mode and Transmit-mode Register Set Modem signal Register	
1.7		
2	Load Pointer Latch Load Buff Full Reg Load Buff Empty Reg	
3	Load DIA Status Reg	Set Select Out Buffer = 1 Set Count Re Pointer = 0 Set Count Wr Pointer = 1 Set Read from Buffer = 0 Set Chan. Clear = 0
4	If Buff Full=0 Then Write Pointer RAM and Write Out Buffer	

Microprogram for AMX 701 /AMX 702

DOB/Command

POLL STATE for AMX 701/AMX 702

Time (shifting to)	Poll/Modem Status	
1.3	Set Receive-mode and Transmit-mode Register Set Modem signal Register	
1.7	Set Poll Priority	
2	Load Pointer Latch Load Buff Full Reg Load Buff Empty Reg	
3	Load DIA Status Reg Write In Buff x) If Buff Full=0 Then Write Pointer RAM Set Dummy Done	Set Select Out Buffer = 0 Set Count Re Pointer = 0 Set Count Wr Pointer = 1 Set Read from Buffer = 0 Set Chan. Clear = 0
4		

x) If Buff Full = 0 Then Input to In Buff from Modem Reg

If Buff Full = 1 Then Input to In Buff is full Status

Microprogram for AMX 701 /AMX 702

Poll/Modem Status

BUS STATE for AMX 701 /AMX 702

Time (shifting to)	Poll/Re Data	
1.3	Set Receive-mode and Transmit-mode Register Set Modem signal Register	
1.7	Set Poll Priority	
2	Load Pointer Latch Load Buff Full Reg Load Buff Empty Reg	
3	Load DIA Status Reg Write In Buff x) If In Buff Full = 0 Then Write Pointer RAM Reset Data Available Set Dummy Done	Set Select Out Buffer = 0 Set Count Re Pointer = 0 Set Count Wr Pointer = 1 Set Read from Buffer = 0 Set Chan. Clear = 0
4		

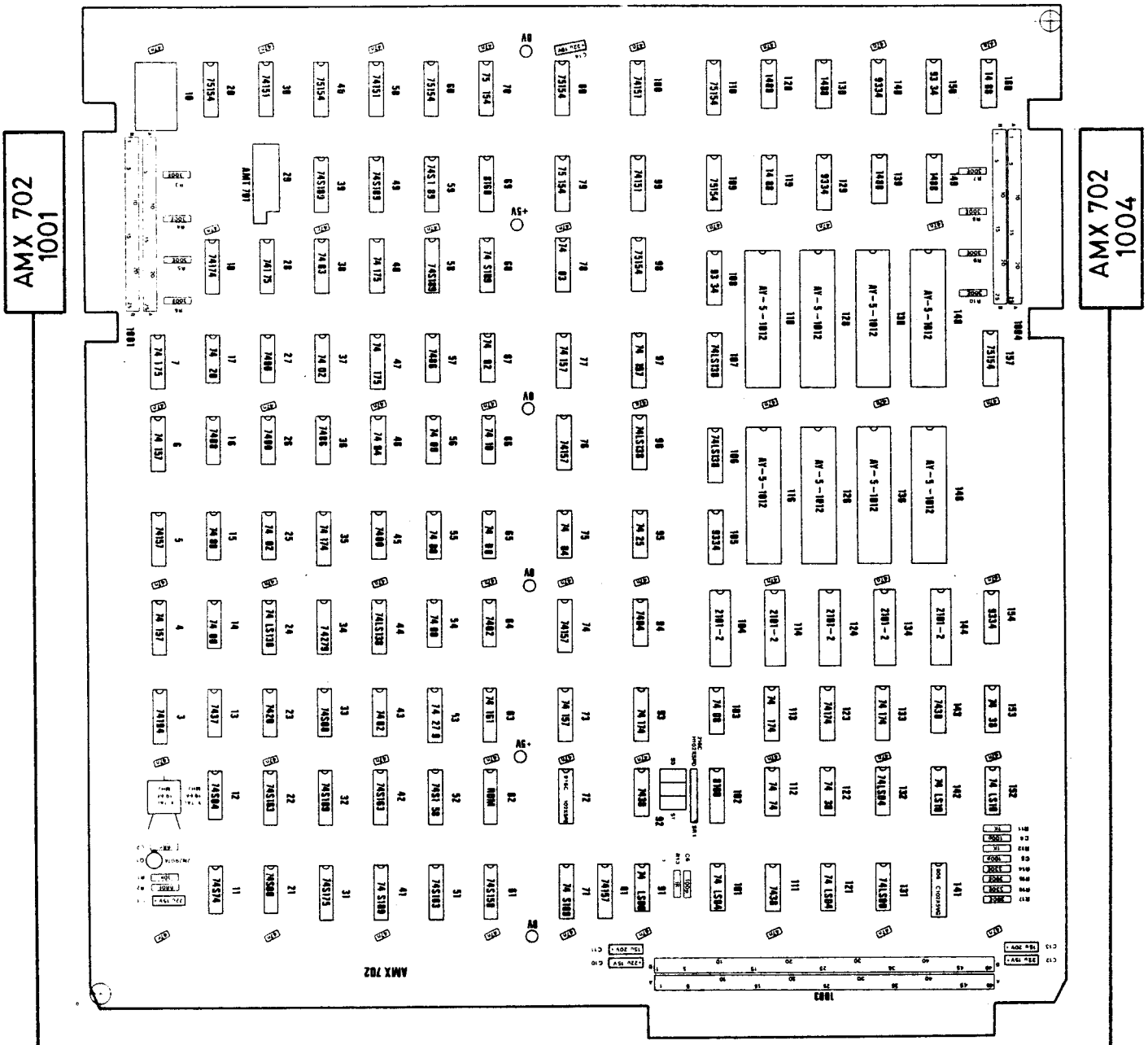
x) If Buff Full = 0 Then Input to In Buffer from UAR/T
If Buff Full = 1 Then Input to In Buffer is full Status

Microprogram for AMX 701/AMX 702

Poll/Re Data

POLL STATE for AMX 701/AMX 702

Time (shifting to)	Poll/Transmitter	
1.3	Set Receive-mode and Transmit-mode Register Set Modem signal Register	
1.7	Set Poll Priority	
2	Load Pointer Latch Load Buff Full Reg Load Buff Empty Reg	
3	Load DIA Status Reg If Buff Empty = 0 Then Write Strobe = 1 and Write Pointer RAM If Pointers Equal = 1 Then Dummy Done = 1	Set Select Out Buffer = 1 Set Count Re Pointer = 1 Set Count Wr Pointer = 0 Set Read from Buffer = 1 Set Chan. Clear = 0
4		


AMX 702
1001
AMX 702
1004
CBL 211
AMX 702-J1

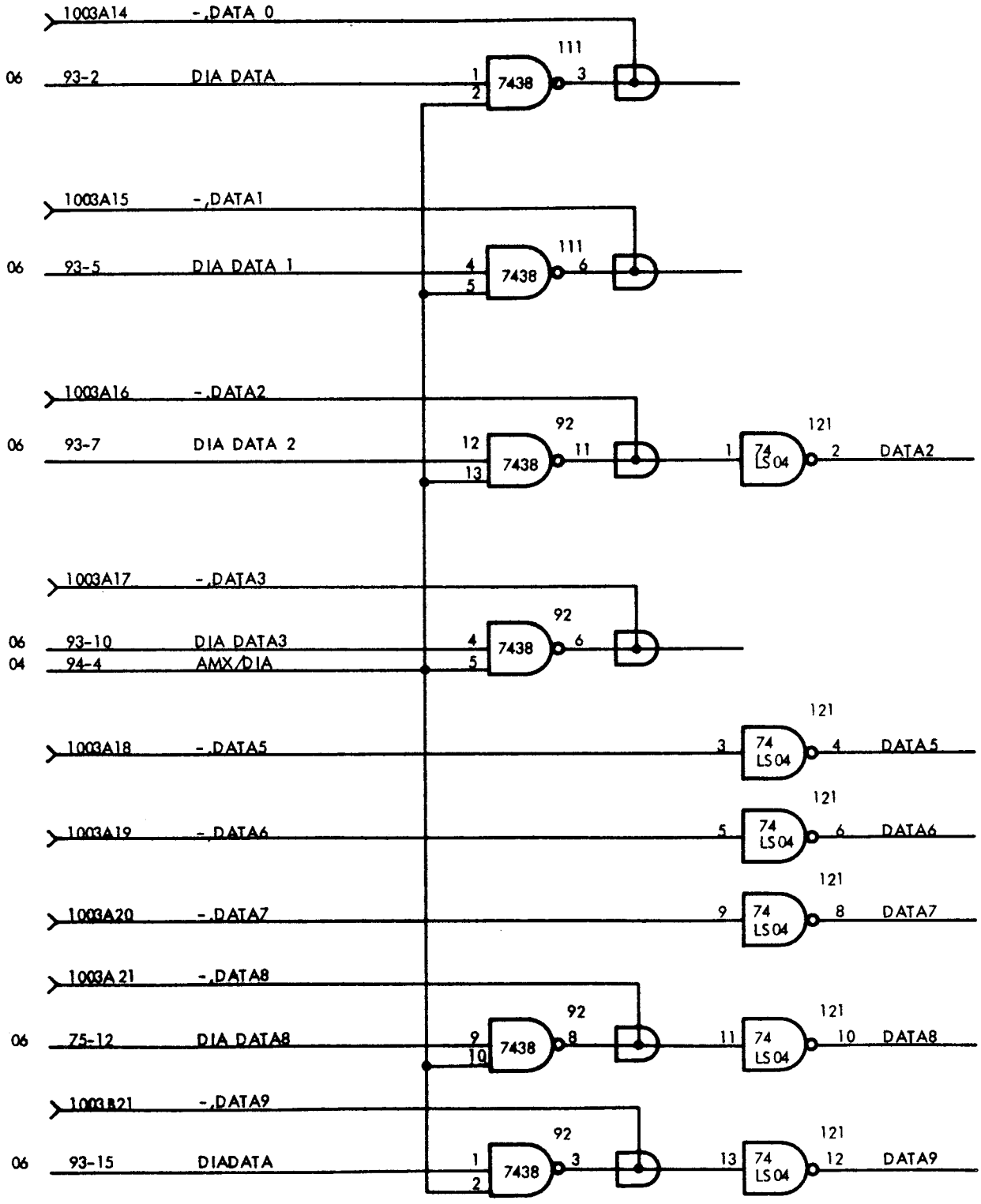
Connector AMX 702 1001	Gen. Addr.	Signal Name	Connector AMX 702 J1
A 1		Trans Data 0	1
B 1		OV	12
A 2		Received Data 0	3
B 2		OV	6
A 3		Req to Send 0	2
B 3		Ready for Sending 0	4
A 4		Data Set Ready 0	9
B 4		Carrier 0	11
A 5		Data Term. Ready 0	5
B 5		Calling Ind. 0	7
A 6		Power On 0	10
B 6		OV	8
A 7		Trans Data 1	13
B 7		OV	24
A 8		Received Data 1	15
B 8		OV	18
A 9		Req to Send 1	14
B 9		Ready for Sending 1	16
A10		Data Set Ready 1	21
B10		Carrier 1	23
A11		Data Term. Ready 1	17
B11		Calling Ind. 1	19
A12		Power On 1	22
B12		OV	20
A13		Trans Data 2	25
B13		OV	42

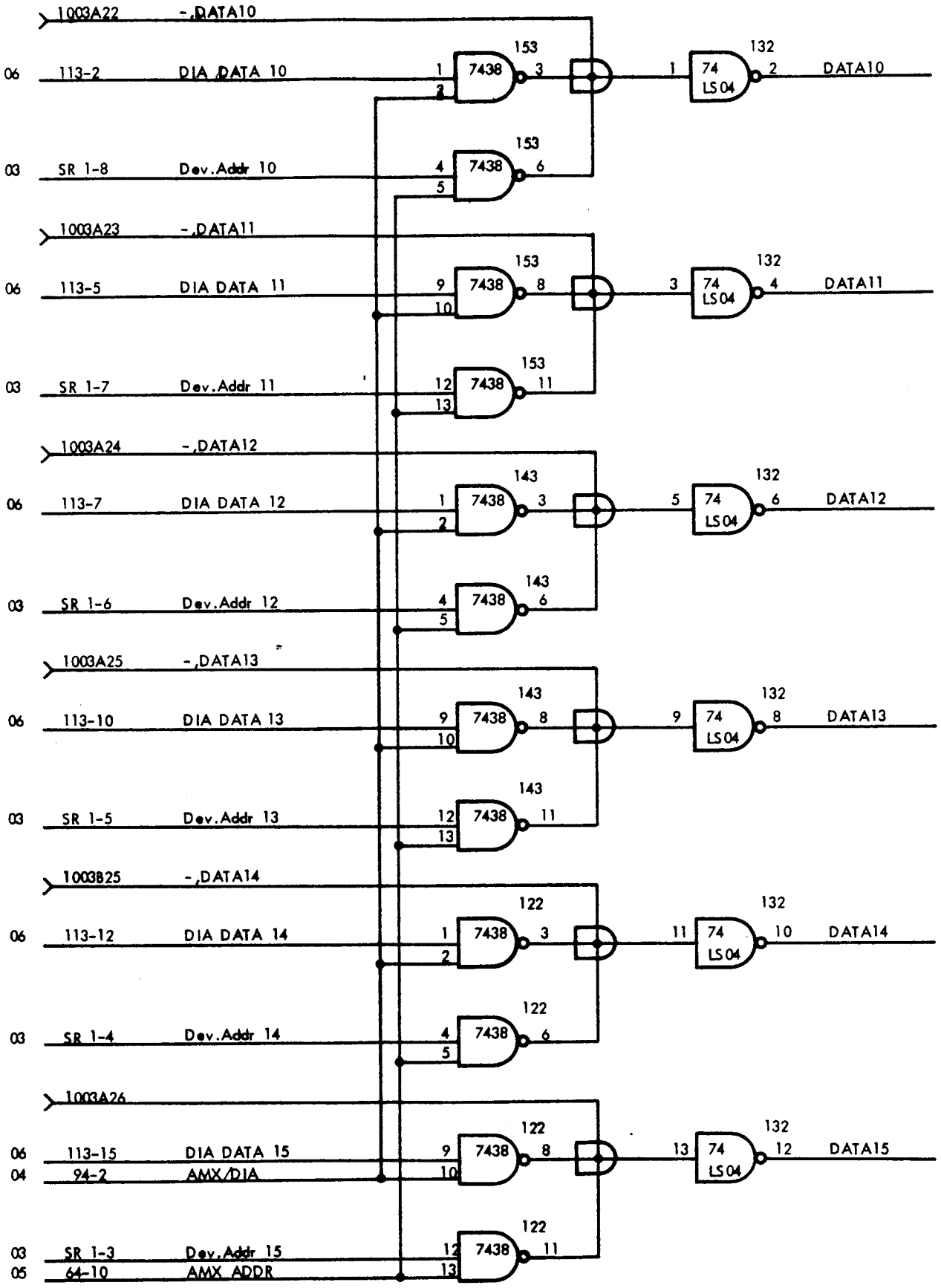
Connector AMX 702 1001	Gen. Addr.	Signal Name	Connector AMX 702 J1
A14		Received Data 2	51
B14		OV	48
A15		Req to Send 2	26
B15		Ready for Sending 2	50
A16		Data Set Ready 2	45
B16		Carrier 2	43
A17		Data Term. Ready 2	49
B17		Calling Ind. 2	47
A18		Power On 2	44
B18		OV	46
A19		Trans Data 3	41
B19		OV	30
A20		Received Data 3	39
B20		OV	36
A21		Req to Send 3	40
B21		Ready for Sending 3	38
A22		Data Set Ready 3	33
B22		Carrier 3	31
A23		Data Term. Ready 3	37
B23		Calling Ind. 3	35
A24		Power On 3	32
B24		OV	34
A25			
B25			

CBL 211

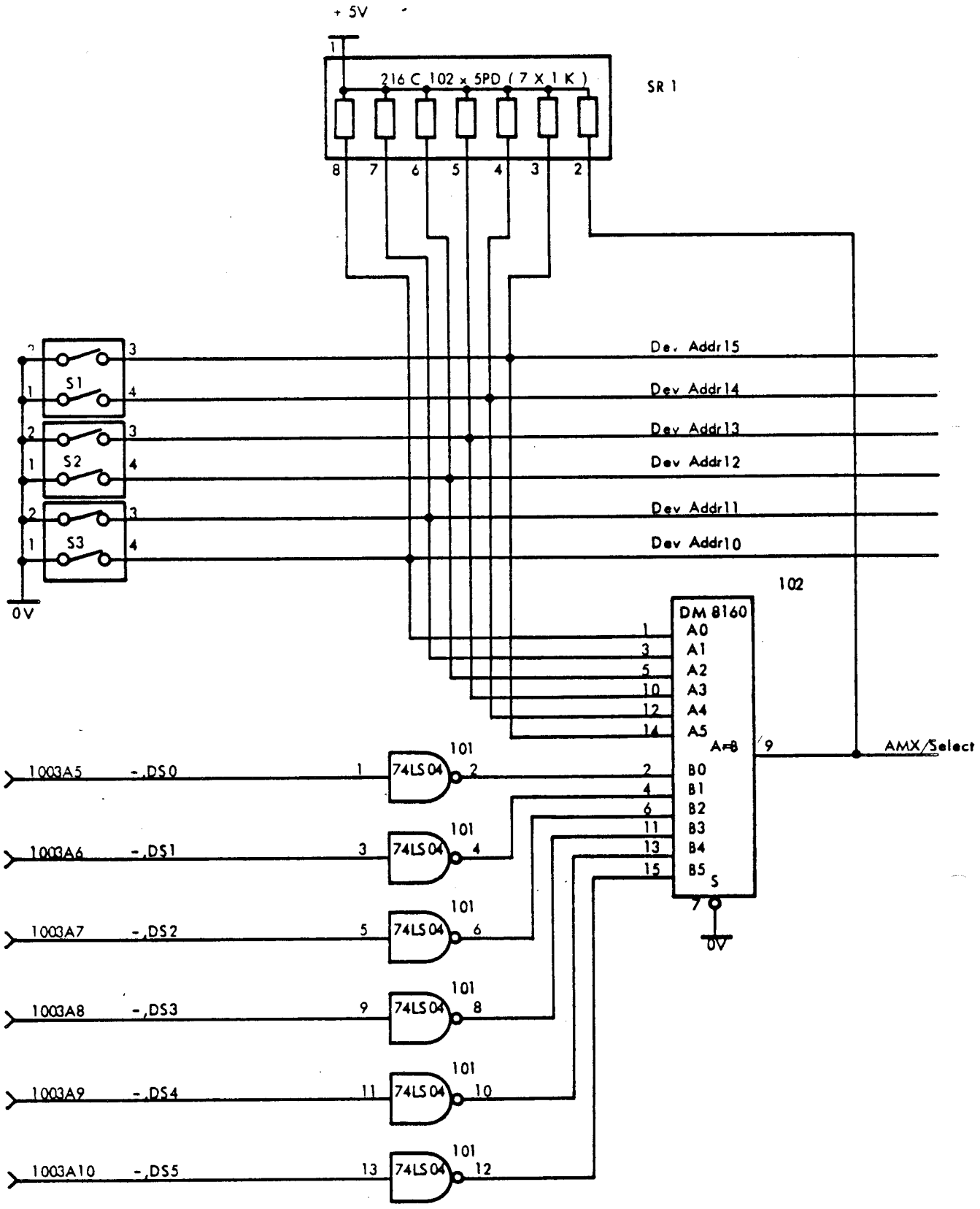
Connector AMX 702 1004	Gen. Addr.	Signal Name	Connector AMX 702 J1	Connector AMX 702 1004	Gen. Addr.	Signal Name	Connector AMX 702 J1
A 1		Trans Data 4	29	A14		Received Data 6	75
B 1		OV	60	B14		OV	98
A 2		Received Data 4	27	A15		Req to Send 6	74
B 2		OV	54	B15		Ready for Sending 6	100
A 3		Req to Send 4	28	A16		Data Set Ready 6	95
B 3		Ready for Sending 4	52	B16		Carrier 6	93
A 4		Data Set Ready 4	57	A17		Data Term. Ready 6	99
B 4		Carrier 4	59	B17		Calling Ind. 6	97
A 5		Data Term. Ready 4	53	A18		Power On 6	94
B 5		Calling Ind. 4	55	B18		OV	96
A 6		Power On 4	58	A19		Trans Data 7	91
B 6		OV	56	B19		OV	80
A 7		Trans Data 5	61	A20		Received Data 7	89
B 7		OV	72	B20		OV	86
A 8		Received Data 5	63	A21		Req to Send 7	90
B 8		OV	66	B21		Ready for Sending 7	88
A 9		Req to Send 5	62	A22		Data Set Ready 7	83
B 9		Ready for Sending 5	64	B22		Carrier 7	81
A10		Data Set Ready 5	69	A23		Data Term. Ready 7	87
B10		Carrier 5	71	B23		Calling Ind. 7	85
A11		Data Term. Ready 5	65	A24		Power On 7	82
B11		Calling Ind. 5	67	B24		OV	84
A12		Power On 5	70	A25			
B12		OV	68	B25			
A13		Trans Data 6	73				
B13		OV	92				

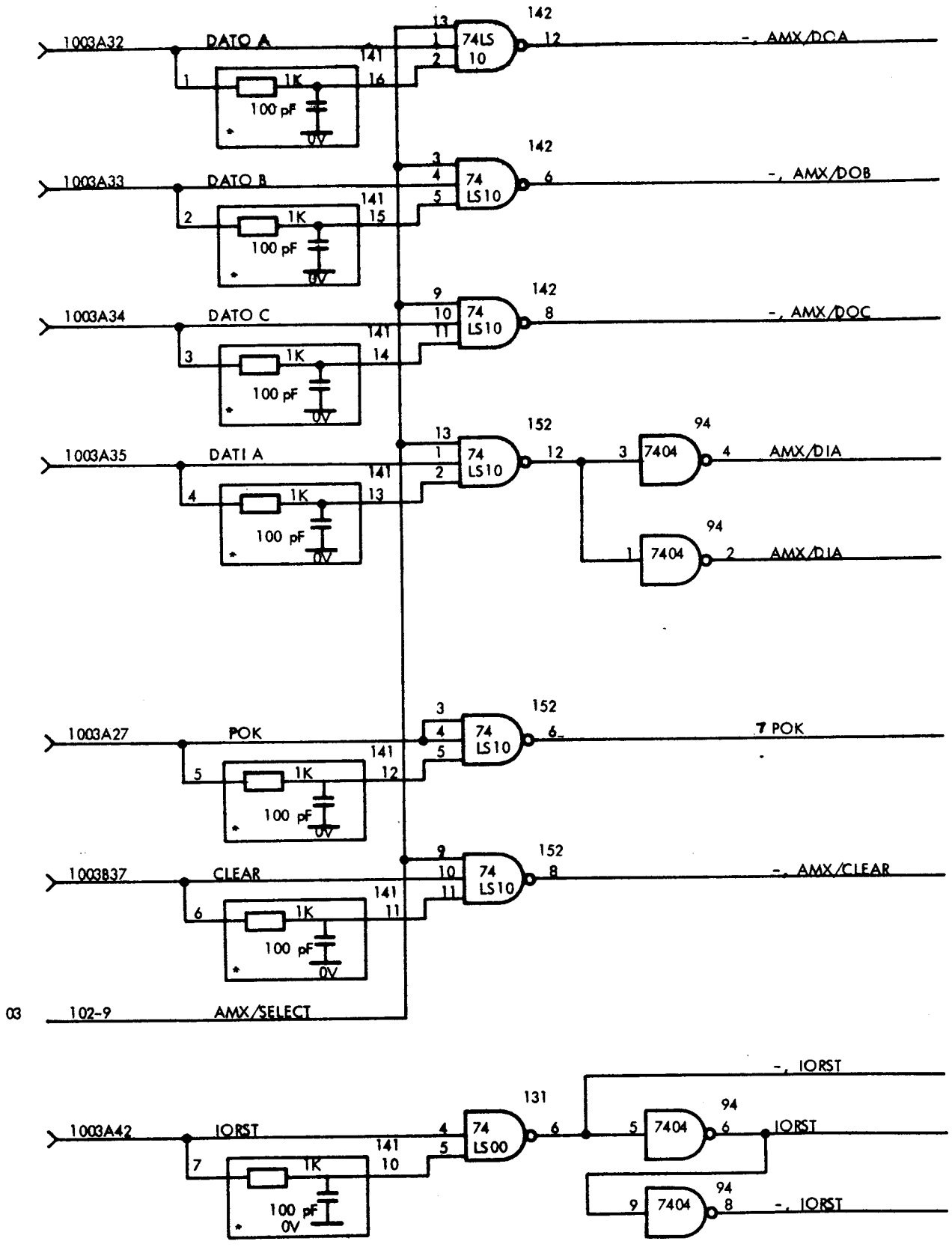
CBL 211

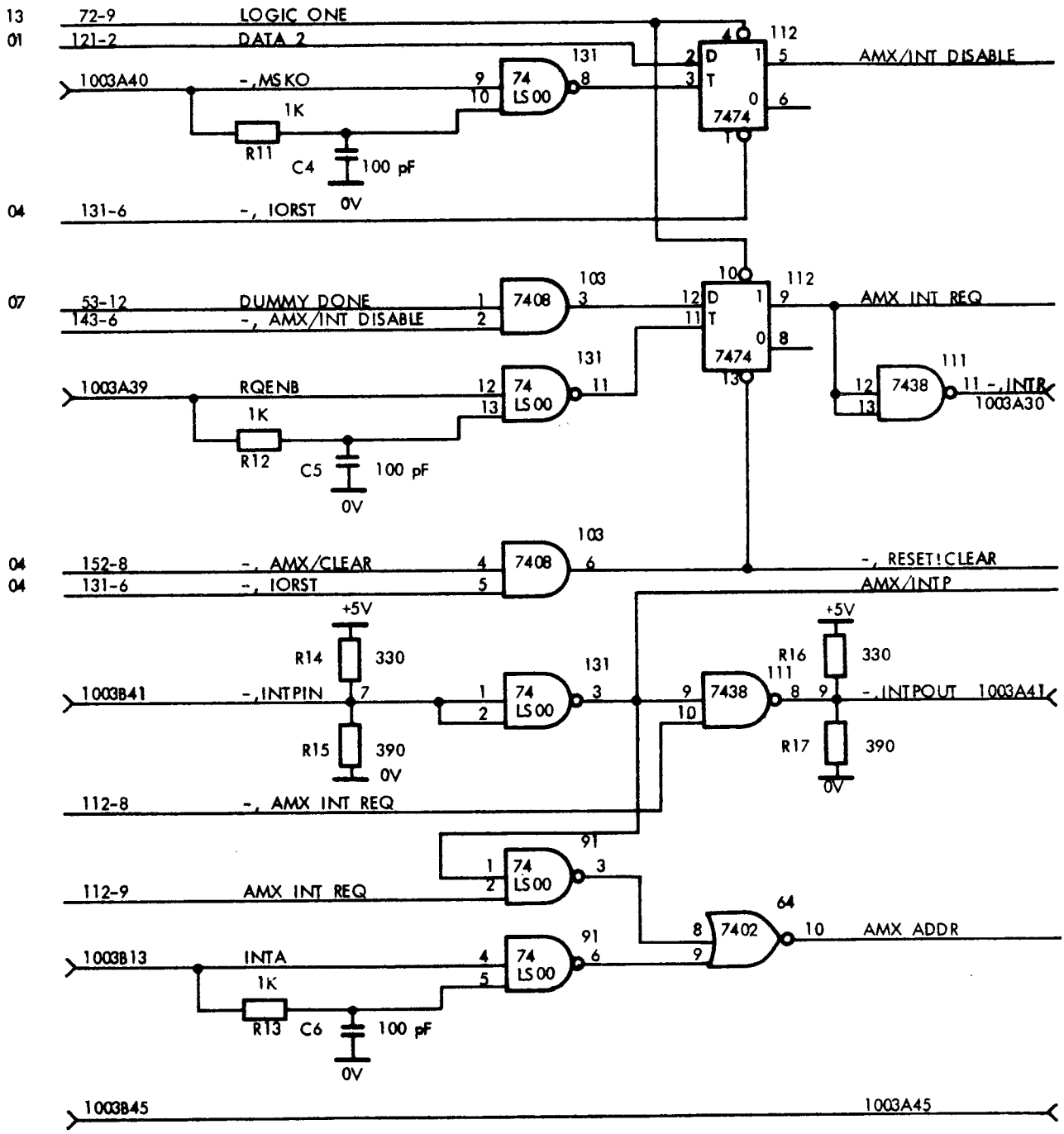

1003A14 -,DATA 0
06 93-2 DIA DATA
111
7438
1003A15 -,DATA1
06 93-5 DIA DATA 1
111
7438
1003A16 -,DATA2
06 93-7 DIA DATA 2
92
7438
121
74 LS04
DATA2
1003A17 -,DATA3
06 93-10 DIA DATA3
04 94-4 AMX/DIA
92
7438
1003A18 -,DATA5
121
74 LS04
DATA5
1003A19 -,DATA6
121
74 LS04
DATA6
1003A20 -,DATA7
121
74 LS04
DATA7
1003A21 -,DATA8
06 Z5-12 DIA DATA8
92
7438
121
74 LS04
DATA8
1003B21 -,DATA9
06 93-15 DIADATA
92
7438
121
74 LS04
DATA9

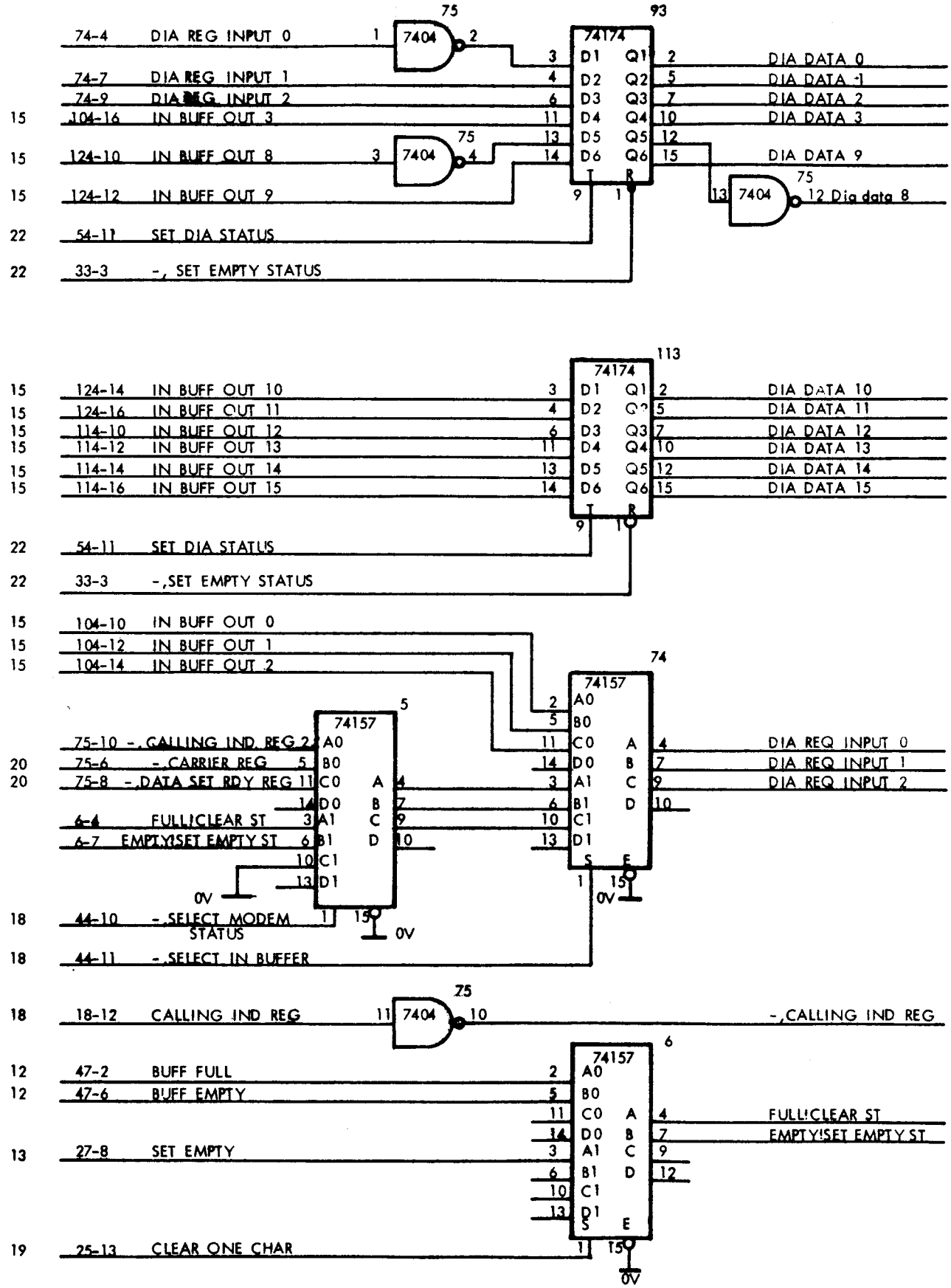


IN-OUT BUS DATA (10 : 15)
Logic diagram


+ 5V
216 C 102 x 5PD (7 X 1 K)
SR 1
8 7 6 5 4 3 2
S1
S2
S3
0V
Dev Addr15
Dev Addr14
Dev Addr13
Dev Addr12
Dev Addr11
Dev Addr10
102
DM 8160
A0
A1
A2
A3
A4
A5
A=B
B0
B1
B2
B3
B4
B5
S
AMX/Select
1003A5 -,DS0
1003A6 -,DS1
1003A7 -,DS2
1003A8 -,DS3
1003A9 -,DS4
1003A10 -,DS5
74LS04
101


1003A32
DATO A
1K
100 pF
0V
74LS 10
142
-, AMX/DOA
1003A33
DATO B
74 LS10
-, AMX/DOB
1003A34
DATO C
-, AMX/DOC
1003A35
DATI A
152
7404
94
AMX/DIA
1003A27
POK
7 POK
1003B37
CLEAR
-, AMX/CLEAR
03
102-9
AMX/SELECT
1003A42
IORST
74 LS00
131
-, IORST
IORST
* IC 906 C 102 X 5VG


13 72-9 LOGIC ONE
01 121-2 DATA 2
1003A40 -,MSKO
1K
R11
C4 100 pF
0V
04 131-6 -, IORST
74 LS00
7474
AMX/INT DISABLE
07 53-12 DUMMY DONE
143-6 -, AMX/INT DISABLE
7408
AMX INT REQ
1003A39 RQENB
R12 C5 100 pF
7438
-,INTR 1003A30
04 152-8 -, AMX/CLEAR
04 131-6 -, IORST
-, RESET!CLEAR
AMX/INTP
+5V
R14 330
R15 390
1003B41 -,INTPIN
R16 330
R17 390
-,INTPOUT 1003A41
112-8 -, AMX INT REQ
112-9 AMX INT REQ
7402
AMX ADDR
1003B13 INTA
R13 C6 100 pF
1003B45
1003A45

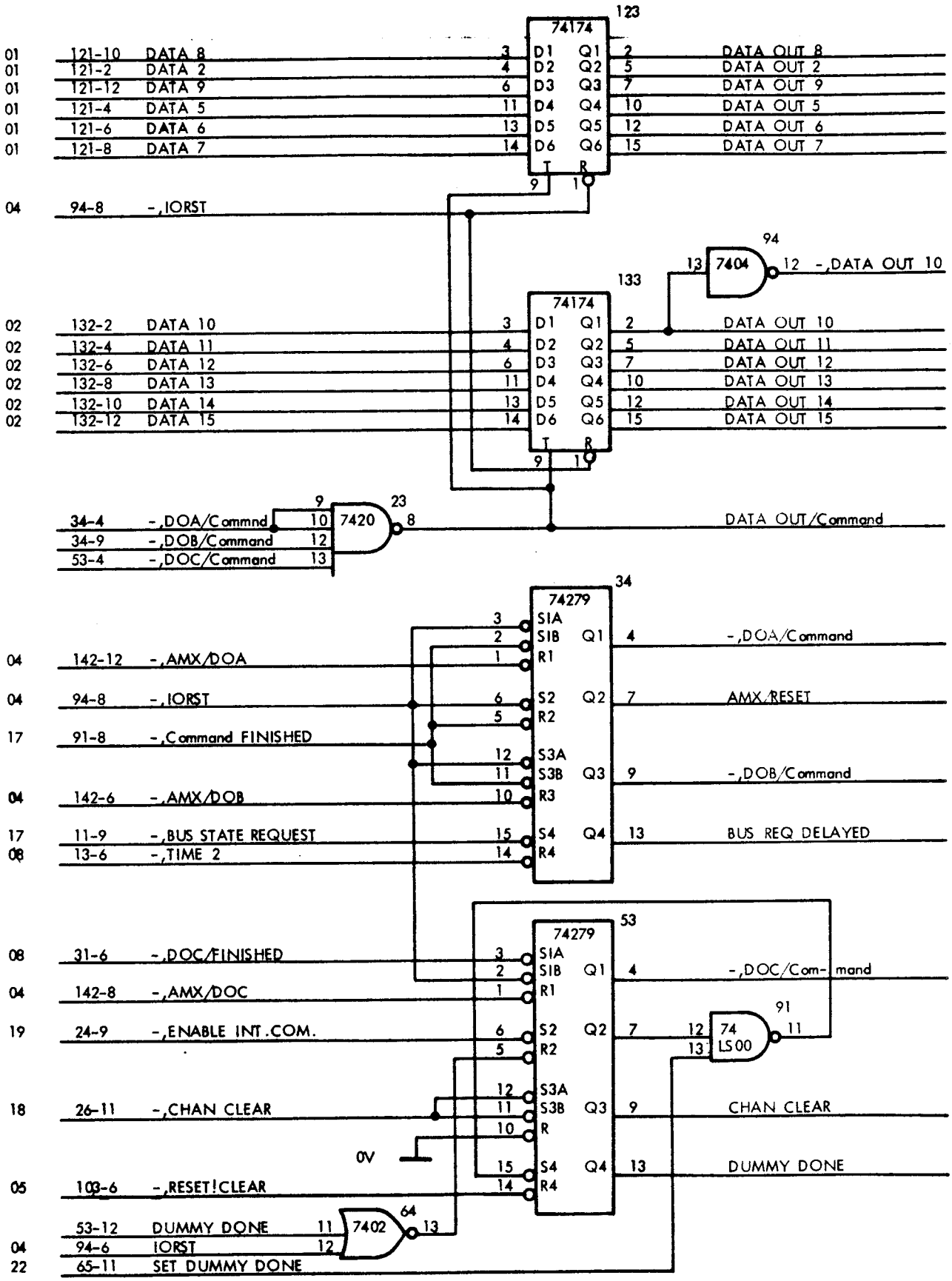


AMX 702 DATA IN REGISTER and SELECTOR

Logic diagram

AMX 06

R 12086

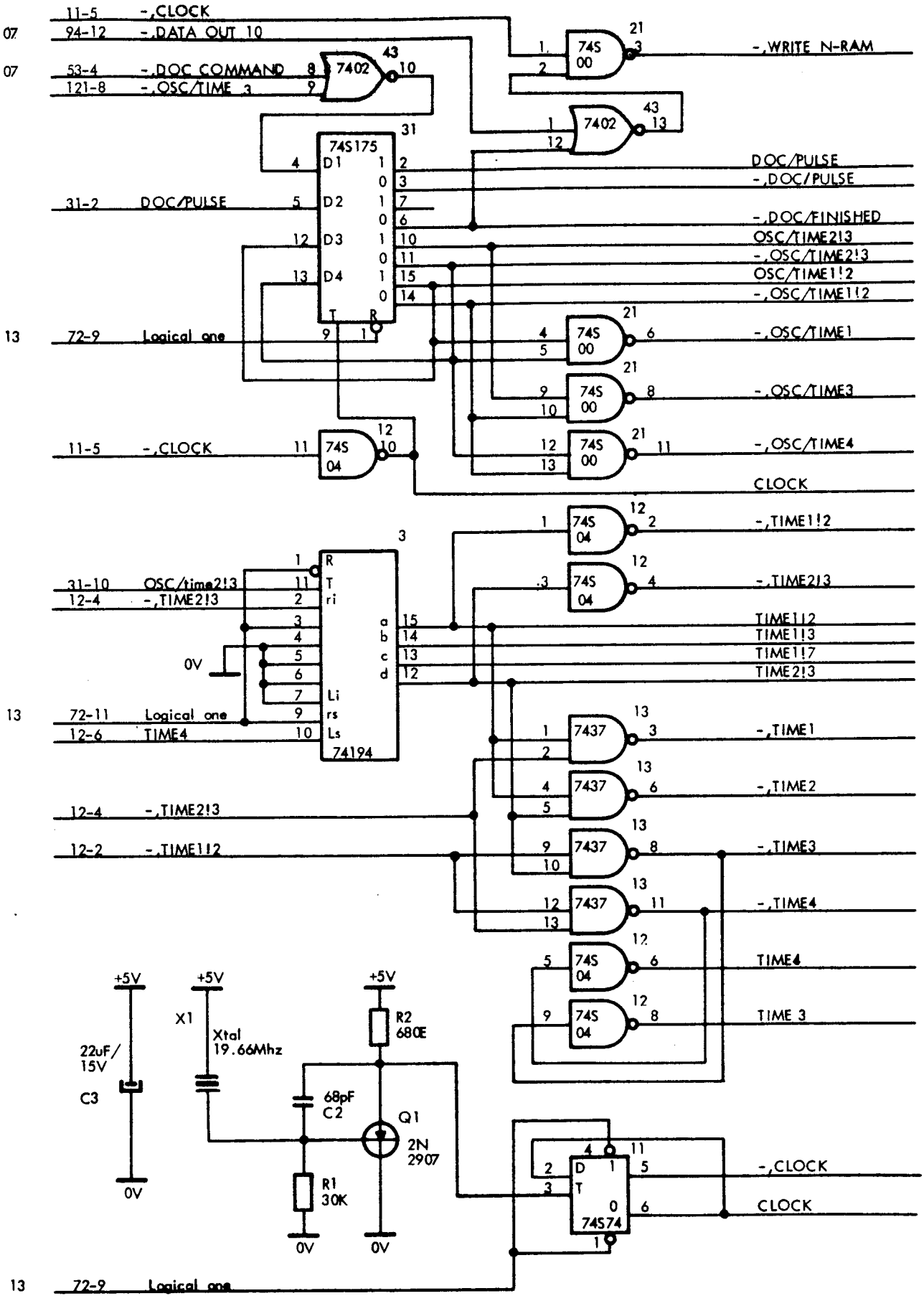


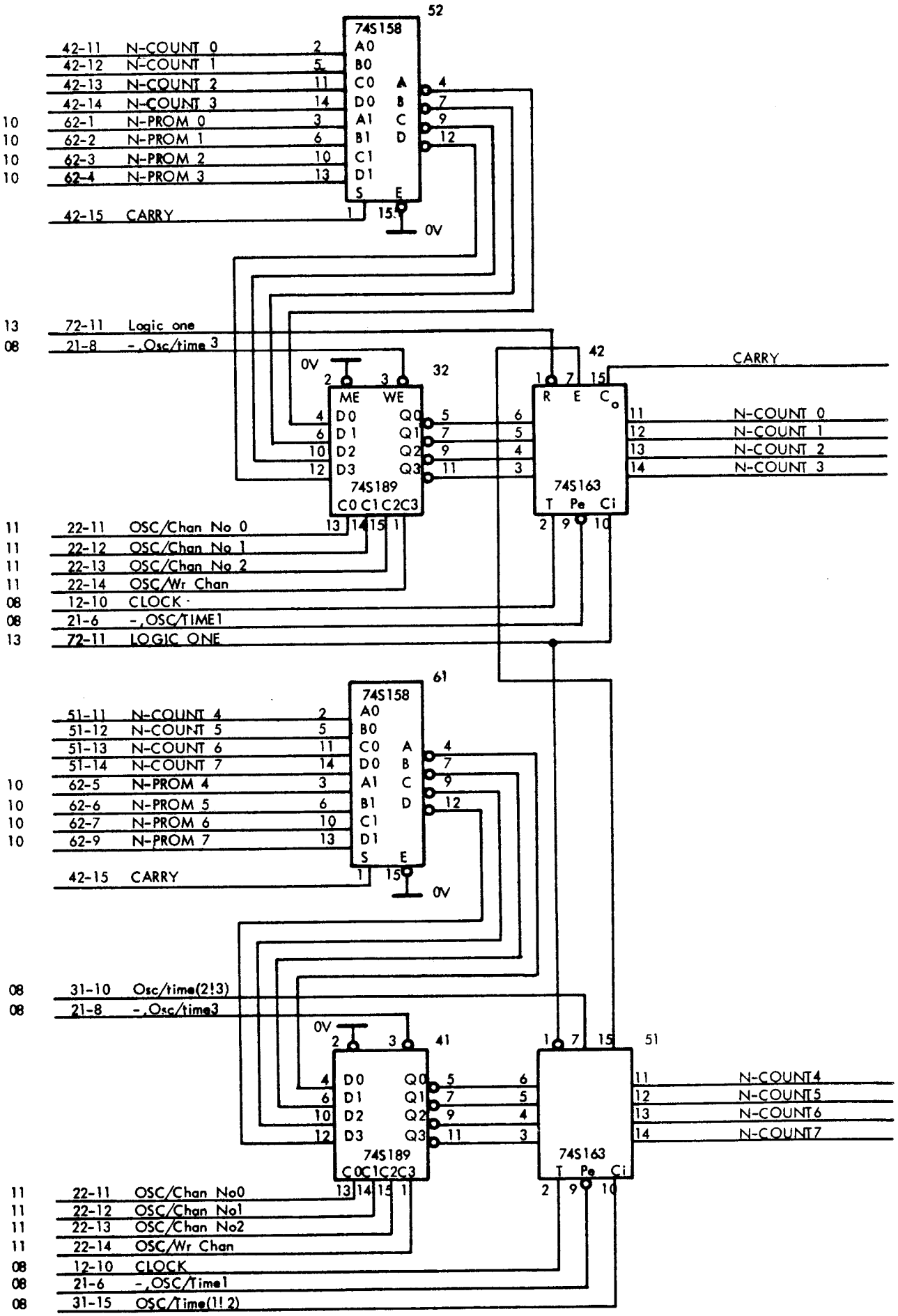
AMX 702

DATA OUT REGISTER and COMMAND REGISTER
Logic diagram

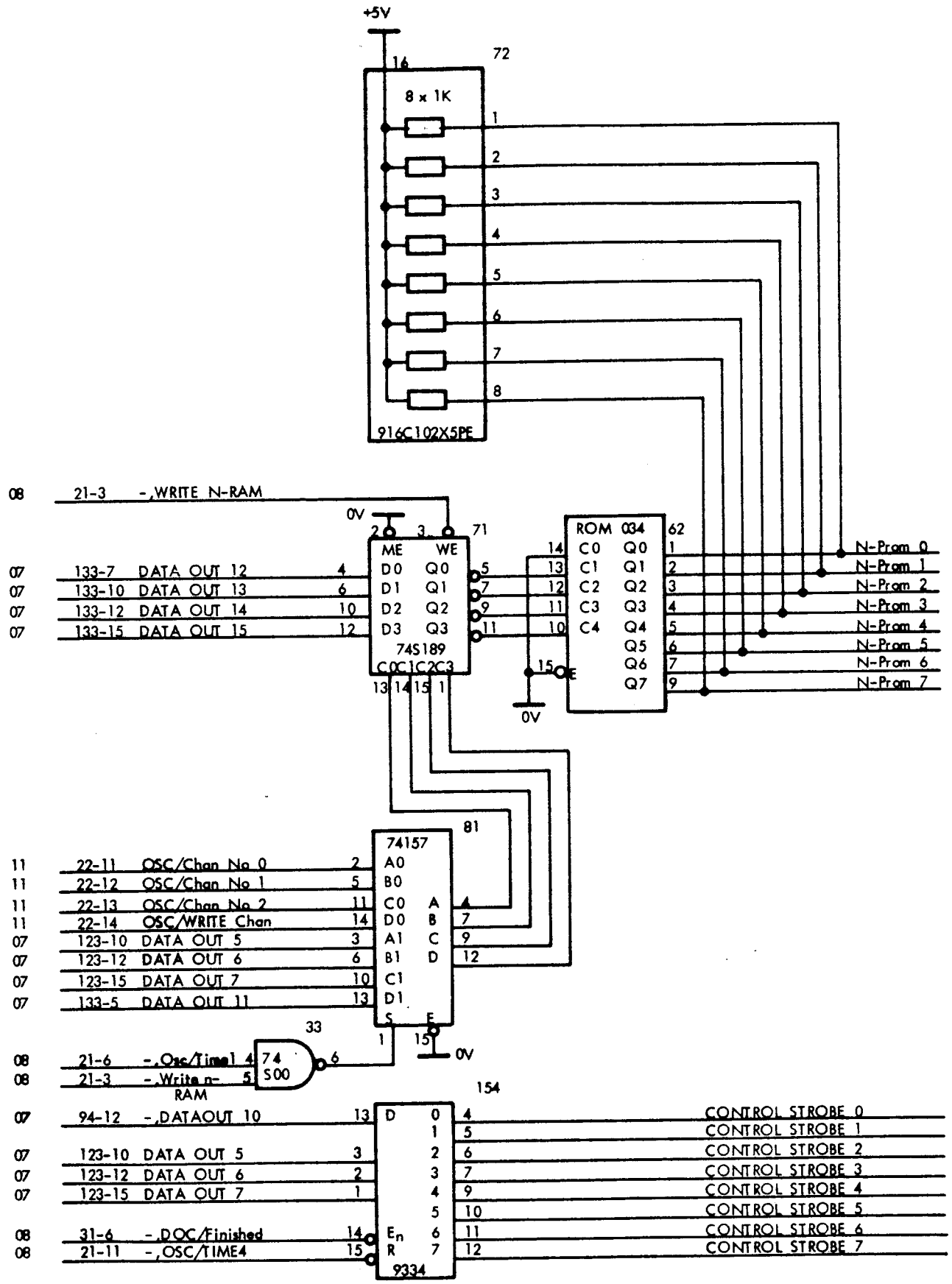
AMX 07

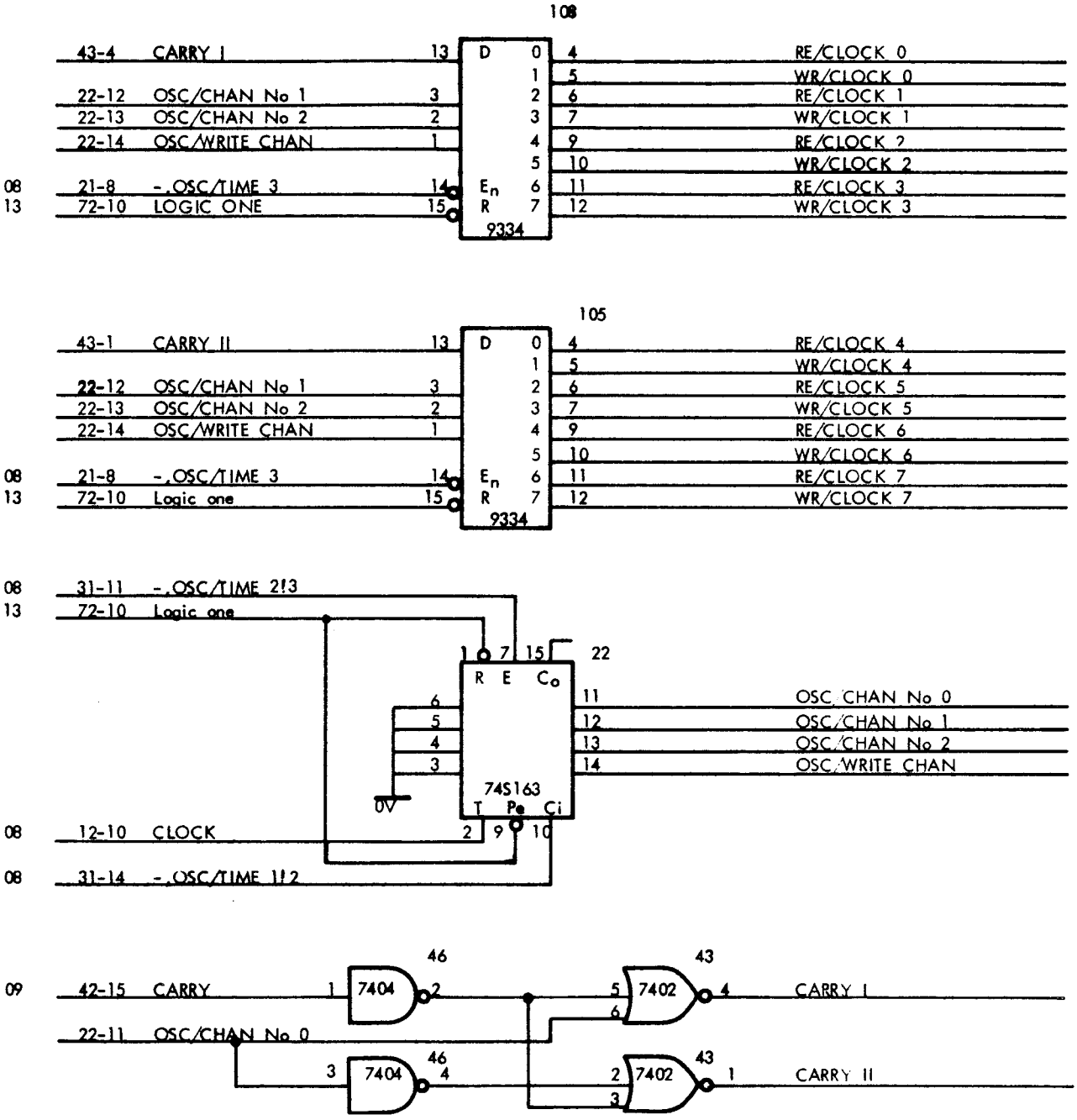
R 12087

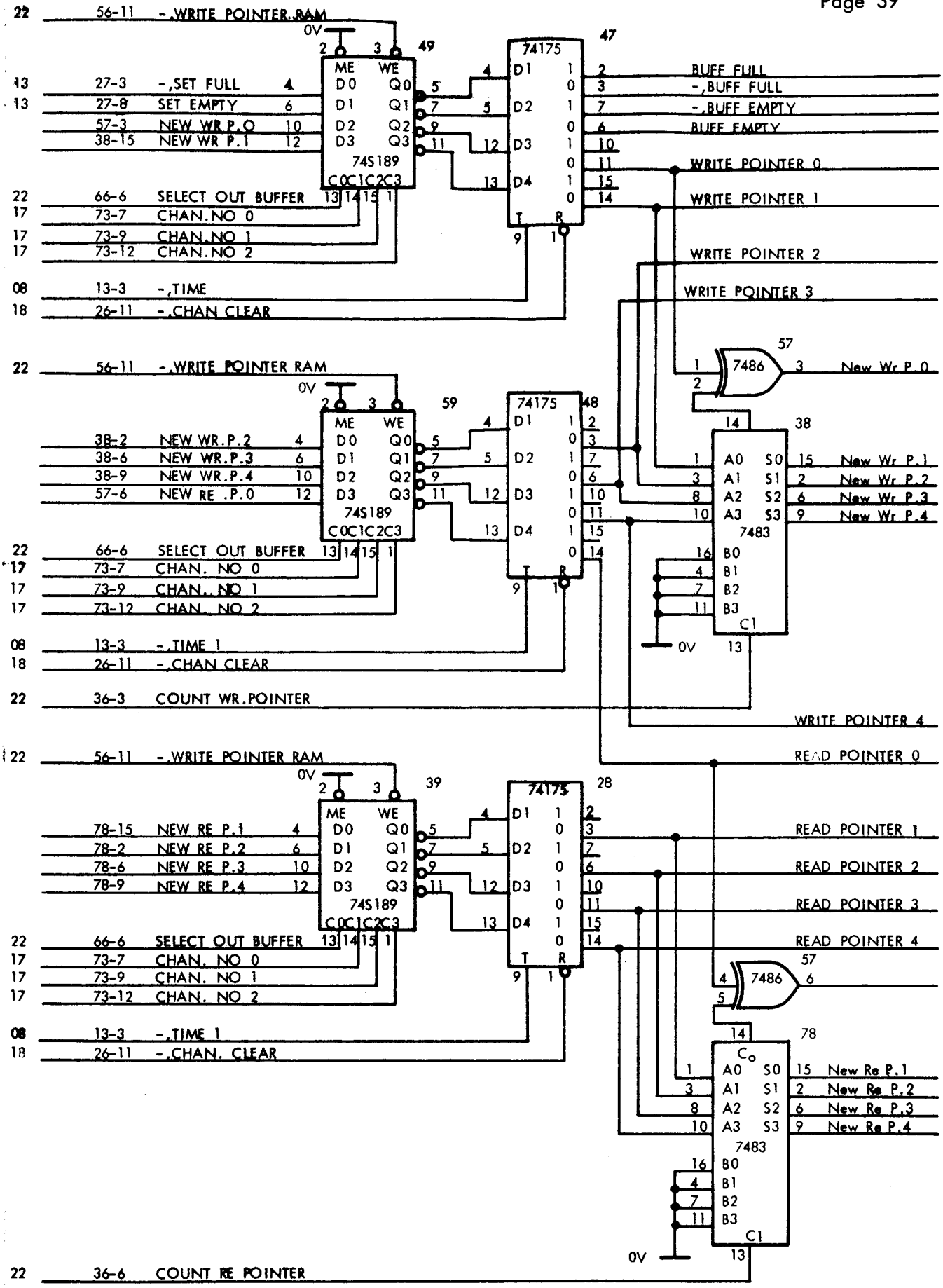

11-5 -,CLOCK
07 94-12 -,DATA OUT 10
07 53-4 -,DOC COMMAND
121-8 -,OSC/TIME 3
7402
74S175
31-2 DOC/PULSE
13 72-9 Logical one
74S 00
74S 04
-,WRITE N-RAM
DOC/PULSE
-,DOC/PULSE
-,DOC/FINISHED
OSC/TIME2!3
-,OSC/TIME2!3
OSC/TIME1!2
-,OSC/TIME1!2
-,OSC/TIME1
-,OSC/TIME3
-,OSC/TIME4
CLOCK
-,TIME1!2
-,TIME2!3
31-10 OSC/time2!3
12-4 -,TIME2!3
0V
13 72-11 Logical one
12-6 TIME4
74194
TIME1!2
TIME1!3
TIME1!7
TIME2!3
7437
-,TIME1
-,TIME2
-,TIME3
-,TIME4
12-4 -,TIME2!3
12-2 -,TIME1!2
TIME4
TIME 3
+5V
22uF/ 15V
C3
X1
Xtal 19.66Mhz
R2 680E
68pF C2
Q1 2N 2907
R1 30K
74S74
-,CLOCK
CLOCK
13 72-9 Logical one



FREQUENCY DIVIDER
Logic diagram


+5V
72
16
8 x 1K
1
2
3
4
5
6
7
8
916C102X5PE
08 21-3 -,WRITE N-RAM
0V
2
3
71
ME
WE
07 133-7 DATA OUT 12 4 D0 Q0 5
07 133-10 DATA OUT 13 6 D1 Q1 7
07 133-12 DATA OUT 14 10 D2 Q2 9
07 133-15 DATA OUT 15 12 D3 Q3 11
74S189
C0C1C2C3
13 14 15 1
ROM 034
62
14 C0 Q0 1
13 C1 Q1 2
12 C2 Q2 3
11 C3 Q3 4
10 C4 Q4 5
Q5 6
Q6 7
Q7 9
15 E
0V
N-Prom 0
N-Prom 1
N-Prom 2
N-Prom 3
N-Prom 4
N-Prom 5
N-Prom 6
N-Prom 7
81
74157
11 22-11 OSC/Chan No 0 2 A0
11 22-12 OSC/Chan No 1 5 B0
11 22-13 OSC/Chan No 2 11 C0 A 4
11 22-14 OSC/WRITE Chan 14 D0 B 7
07 123-10 DATA OUT 5 3 A1 C 9
07 123-12 DATA OUT 6 6 B1 D 12
07 123-15 DATA OUT 7 10 C1
07 133-5 DATA OUT 11 13 D1
S E
1 15 0V
33
08 21-6 -,Osc/Time1 4 74 S00 6
08 21-3 -,Write n- RAM 5
154
07 94-12 -,DATAOUT 10 13 D 0 4
1 5
07 123-10 DATA OUT 5 3 2 6
07 123-12 DATA OUT 6 2 3 7
07 123-15 DATA OUT 7 1 4 9
5 10
08 31-6 -,DOC/Finished 14 En 6 11
08 21-11 -,OSC/TIME4 15 R 7 12
9334
CONTROL STROBE 0
CONTROL STROBE 1
CONTROL STROBE 2
CONTROL STROBE 3
CONTROL STROBE 4
CONTROL STROBE 5
CONTROL STROBE 6
CONTROL STROBE 7

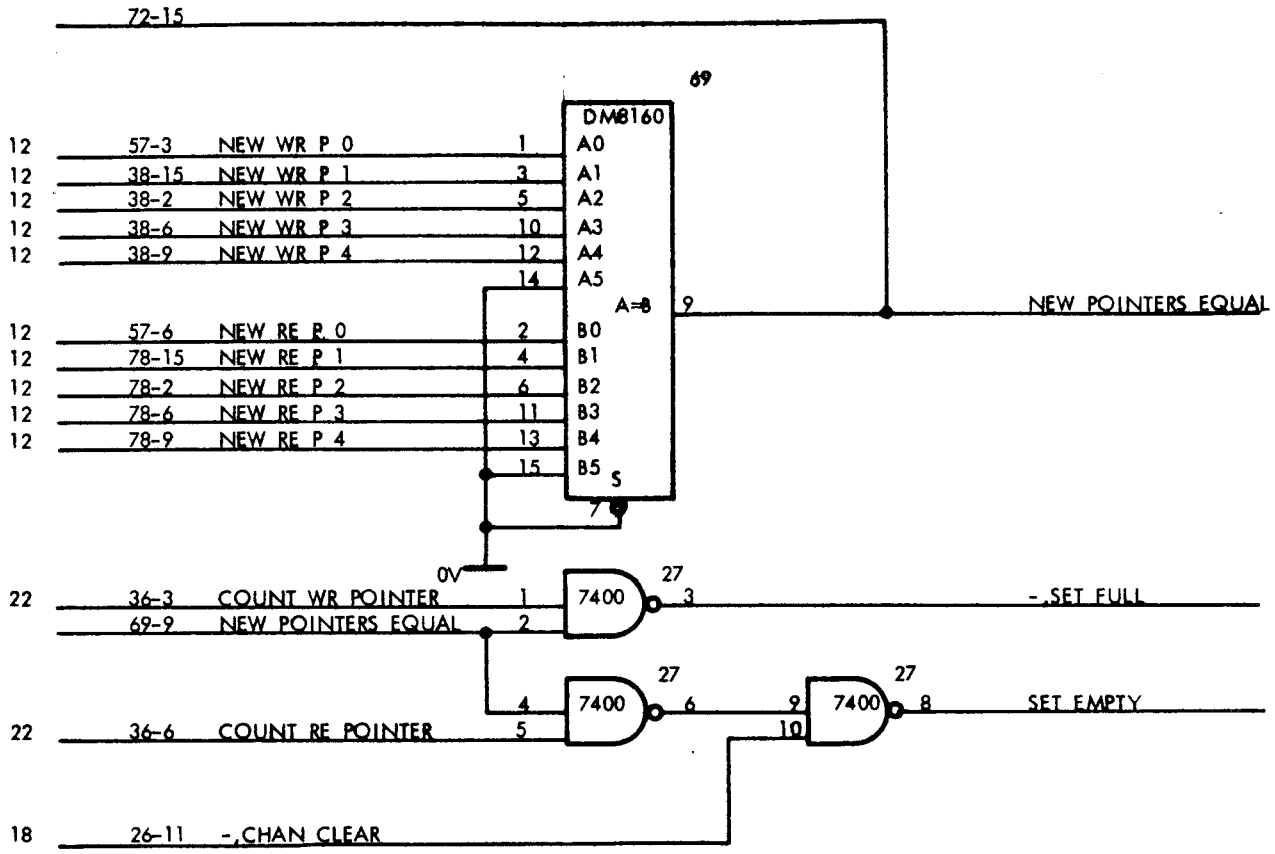

108
43-4 CARRY I
22-12 OSC/CHAN No 1
22-13 OSC/CHAN No 2
22-14 OSC/WRITE CHAN
08 21-8 -.OSC/TIME 3
13 72-10 LOGIC ONE
9334
RE/CLOCK 0
WR/CLOCK 0
RE/CLOCK 1
WR/CLOCK 1
RE/CLOCK 2
WR/CLOCK 2
RE/CLOCK 3
WR/CLOCK 3
105
43-1 CARRY II
22-12 OSC/CHAN No 1
22-13 OSC/CHAN No 2
22-14 OSC/WRITE CHAN
08 21-8 -.OSC/TIME 3
13 72-10 Logic one
9334
RE/CLOCK 4
WR/CLOCK 4
RE/CLOCK 5
WR/CLOCK 5
RE/CLOCK 6
WR/CLOCK 6
RE/CLOCK 7
WR/CLOCK 7
08 31-11 -.OSC/TIME 2!3
13 72-10 Logic one
74S163
0V
08 12-10 CLOCK
08 31-14 -.OSC/TIME 1!2
OSC CHAN No 0
OSC/CHAN No 1
OSC/CHAN No 2
OSC/WRITE CHAN
09 42-15 CARRY
22-11 OSC/CHAN No 0
7404
7402
CARRY I
CARRY II

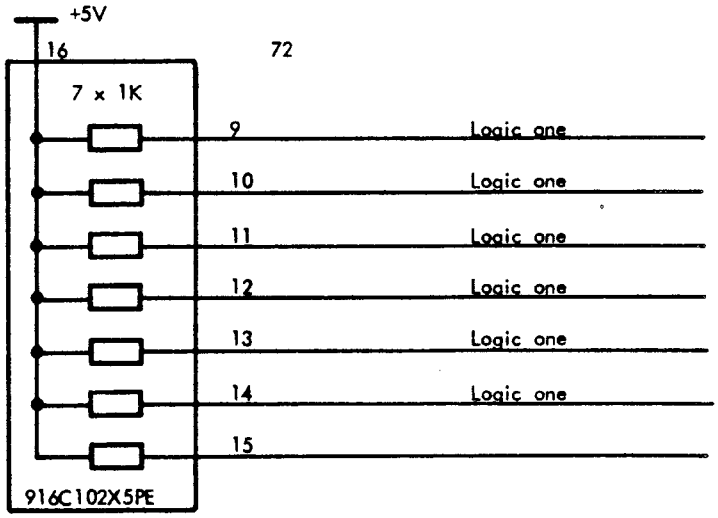


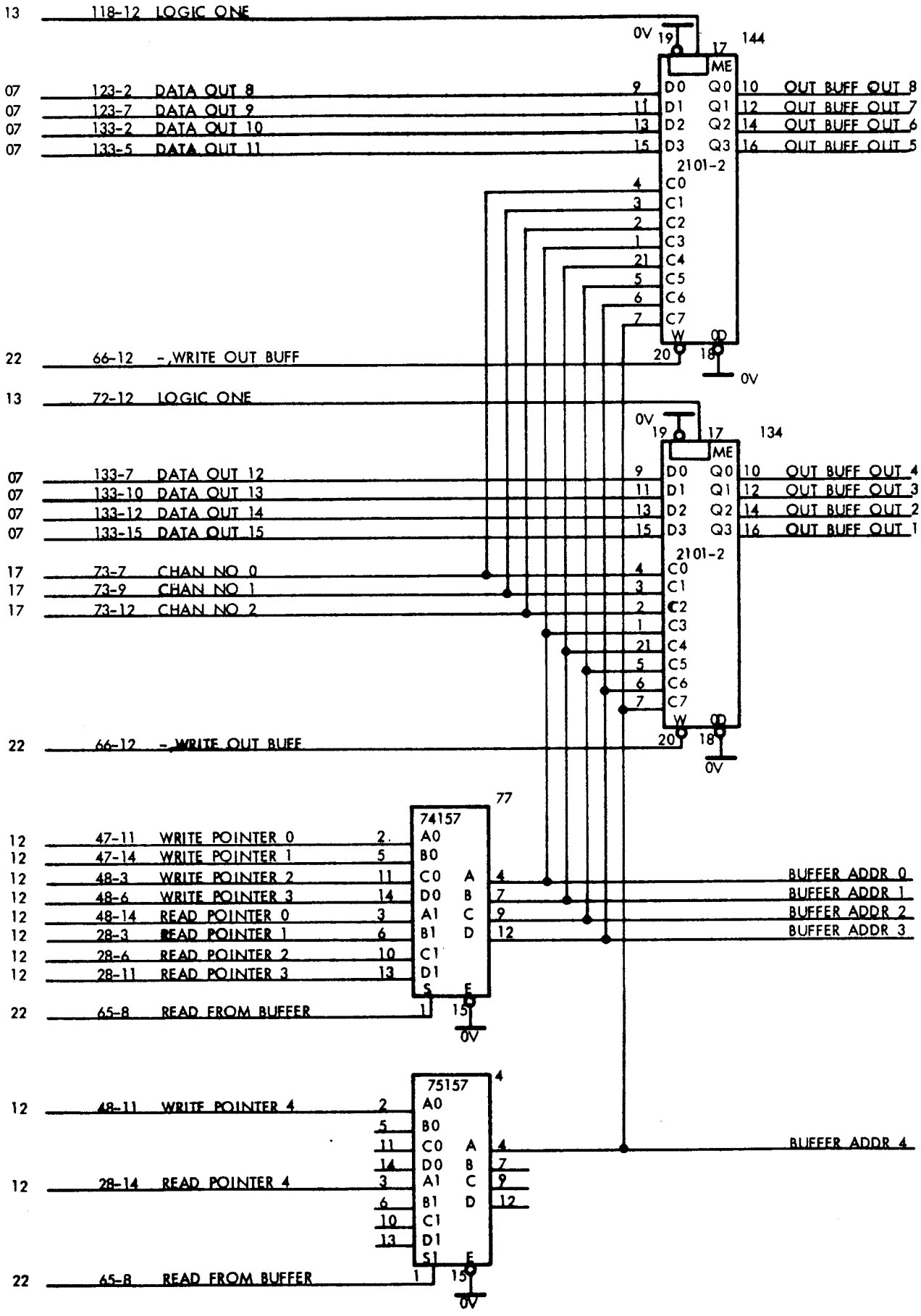
AMX 702
R 12092

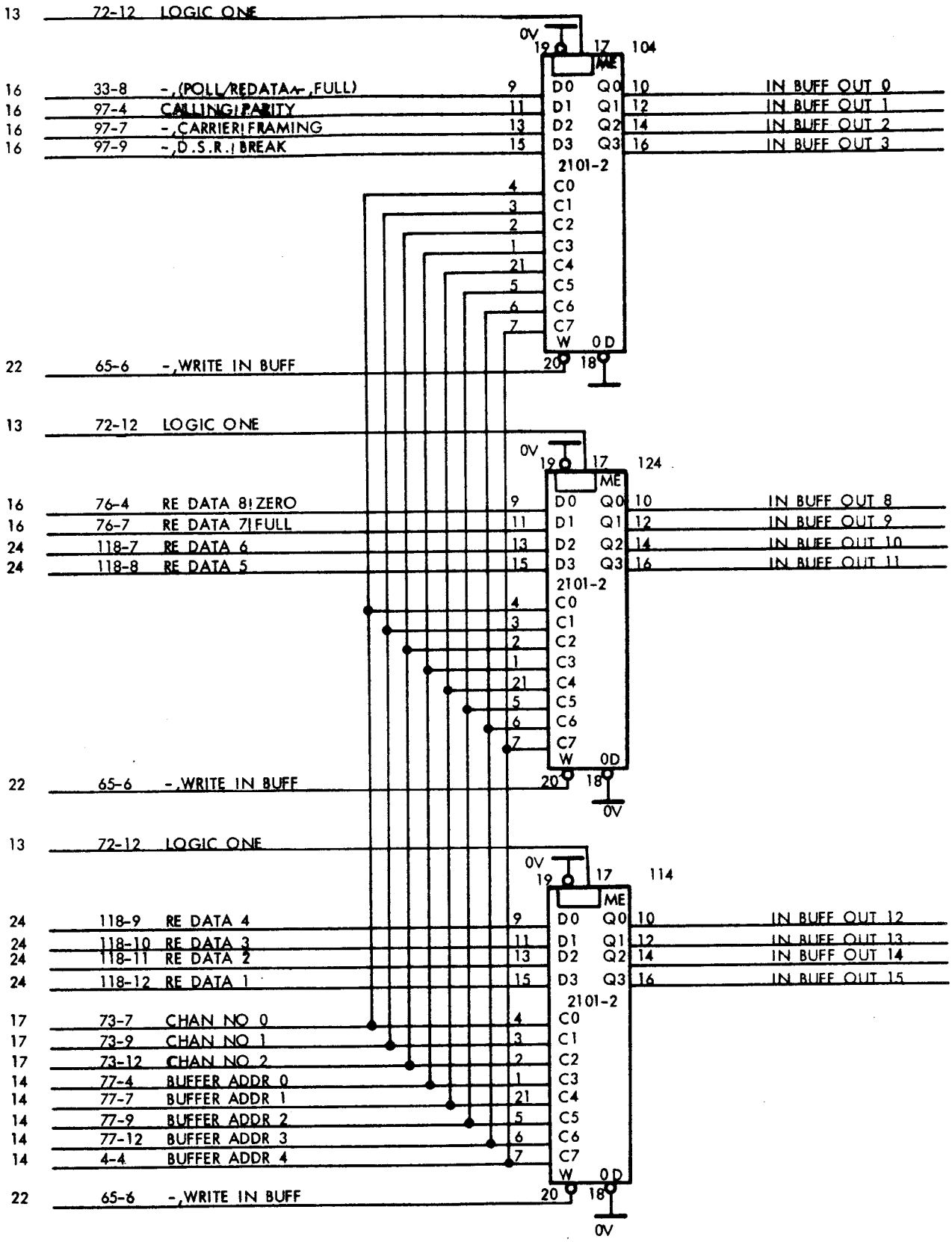
WRITE POINTER and READ POINTER for INPUT BUFFER and OUTPUT BUFFER.
Logic diagram

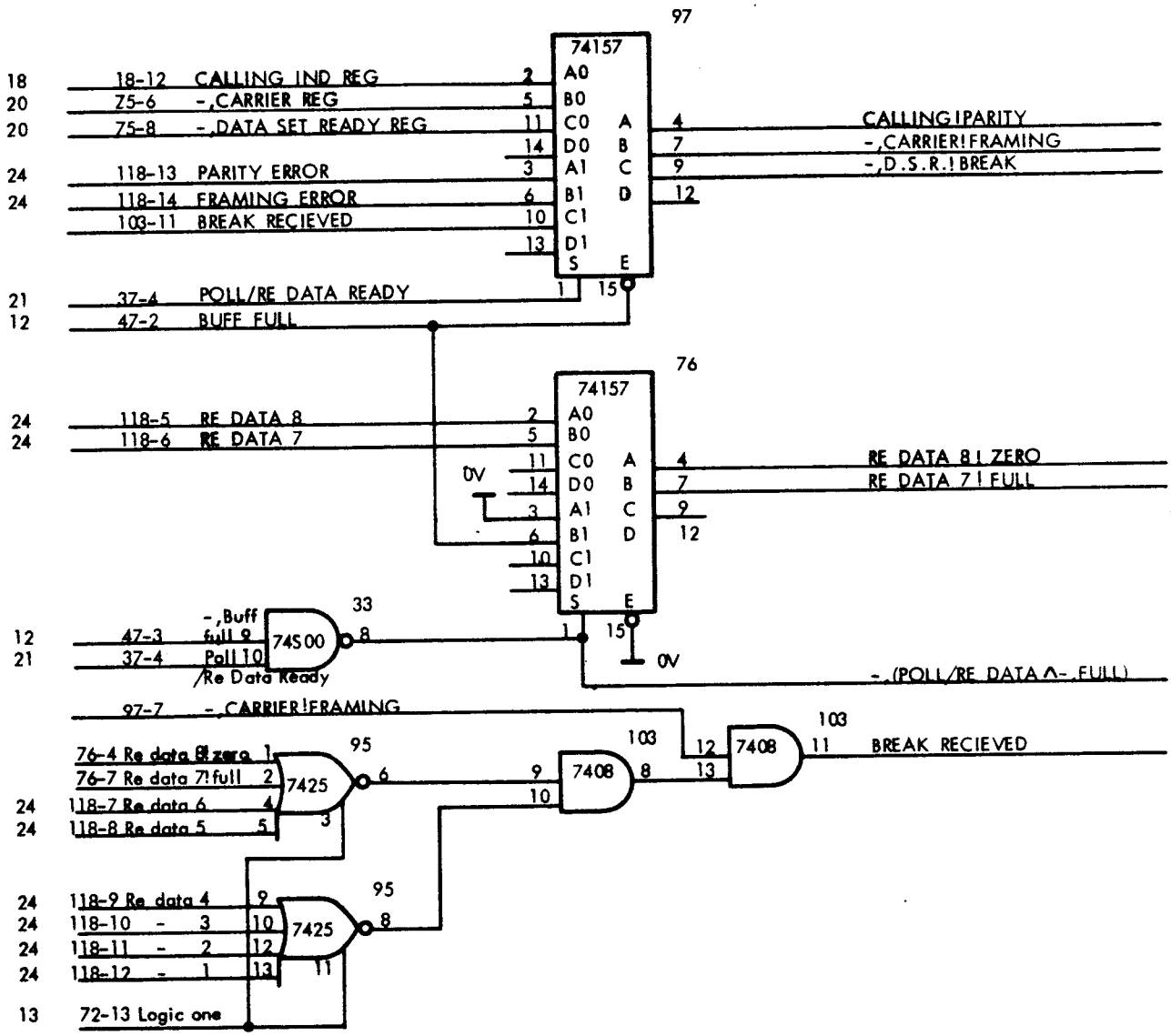
AMX 12

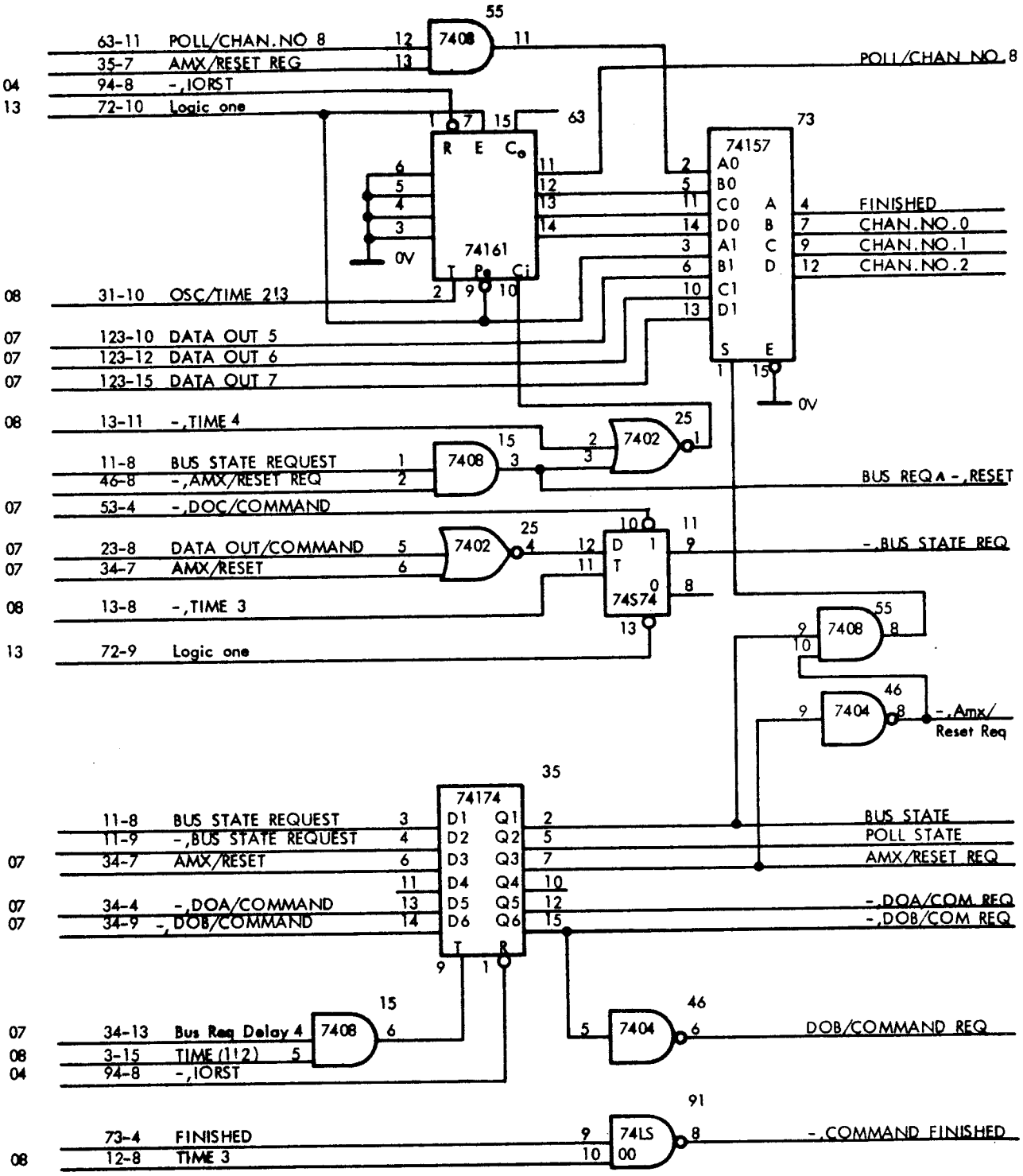

72-15
69
DM8160
12 57-3 NEW WR P 0 1 A0
12 38-15 NEW WR P 1 3 A1
12 38-2 NEW WR P 2 5 A2
12 38-6 NEW WR P 3 10 A3
12 38-9 NEW WR P 4 12 A4
14 A5
A=B 9 NEW POINTERS EQUAL
12 57-6 NEW RE P 0 2 B0
12 78-15 NEW RE P 1 4 B1
12 78-2 NEW RE P 2 6 B2
12 78-6 NEW RE P 3 11 B3
12 78-9 NEW RE P 4 13 B4
15 B5
S
7
0V
27
22 36-3 COUNT WR POINTER 1 7400 3 -,SET FULL
69-9 NEW POINTERS EQUAL 2
27 27
4 7400 6 9 7400 8 SET EMPTY
22 36-6 COUNT RE POINTER 5 10
18 26-11 -,CHAN CLEAR

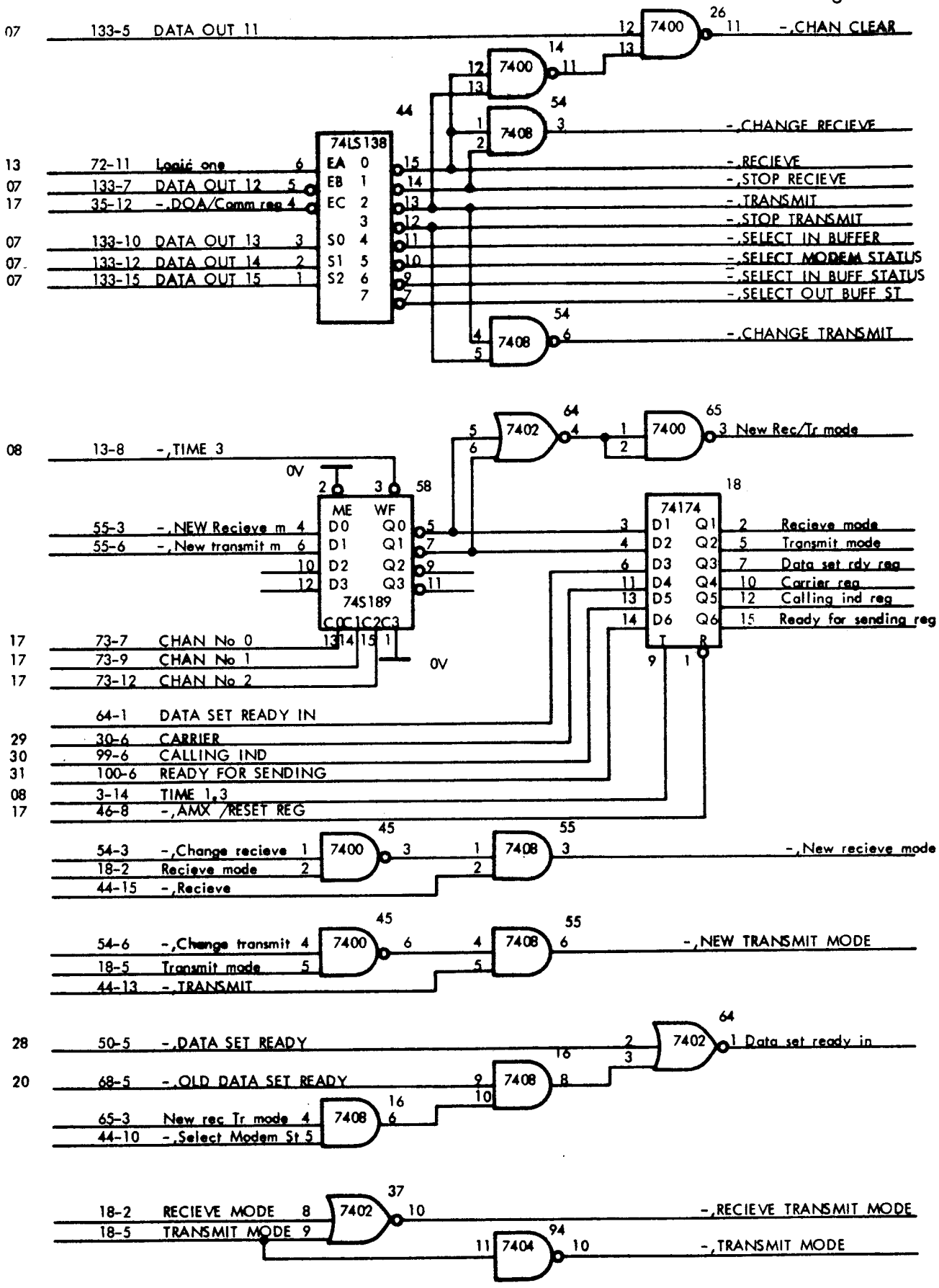

+5V
16
72
7 x 1K
9 Logic one
10 Logic one
11 Logic one
12 Logic one
13 Logic one
14 Logic one
15
916C102X5PE

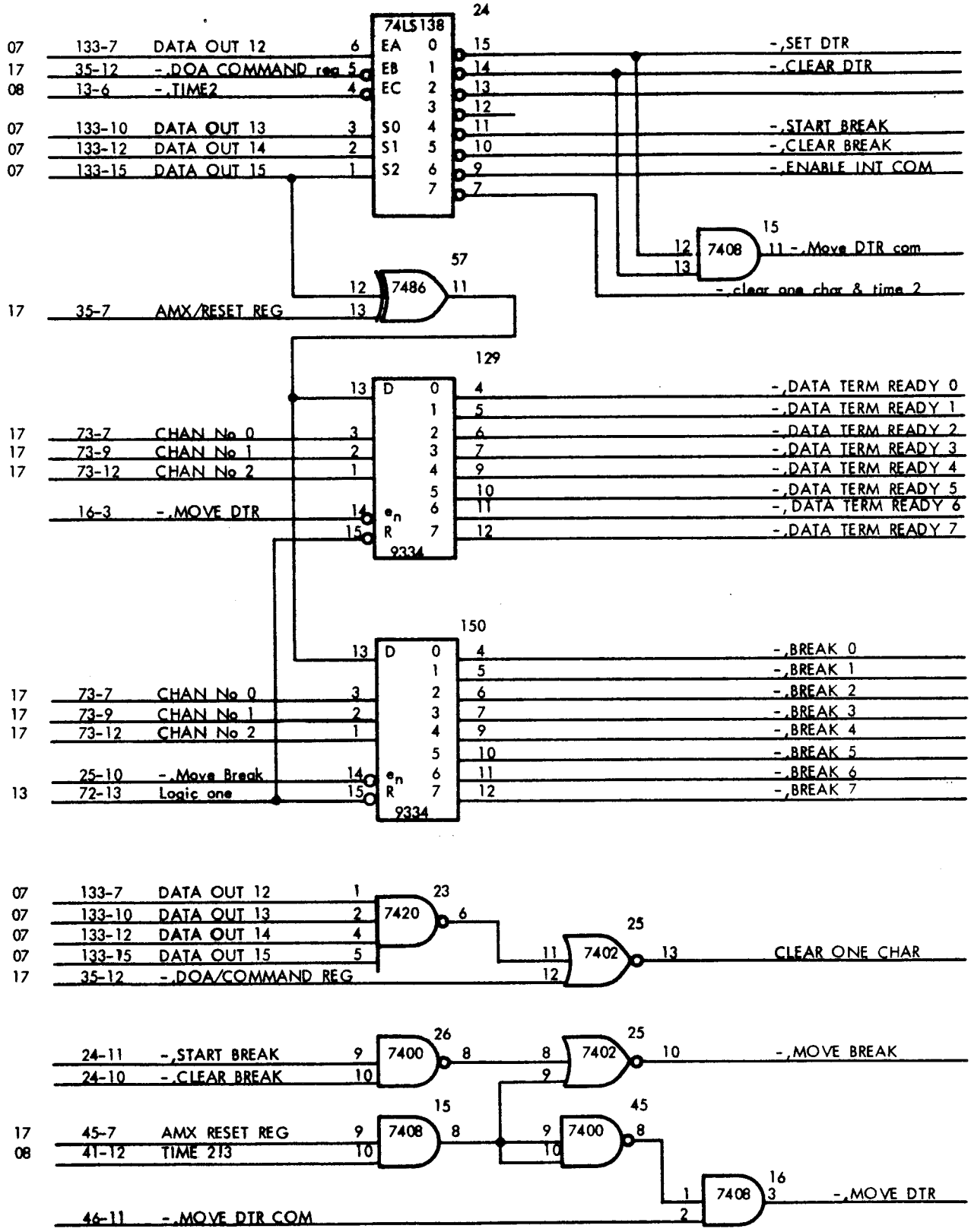

13 118-12 LOGIC ONE
0V 19 17 144
ME
07 123-2 DATA OUT 8
07 123-7 DATA OUT 9
07 133-2 DATA OUT 10
07 133-5 DATA OUT 11
9 D0 Q0 10 OUT BUFF OUT 8
11 D1 Q1 12 OUT BUFF OUT 7
13 D2 Q2 14 OUT BUFF OUT 6
15 D3 Q3 16 OUT BUFF OUT 5
2101-2
4 C0
3 C1
2 C2
1 C3
21 C4
5 C5
6 C6
7 C7
W
20 18
0V
22 66-12 -,WRITE OUT BUFF
13 72-12 LOGIC ONE
0V 19 17 134
ME
07 133-7 DATA OUT 12
07 133-10 DATA OUT 13
07 133-12 DATA OUT 14
07 133-15 DATA OUT 15
9 D0 Q0 10 OUT BUFF OUT 4
11 D1 Q1 12 OUT BUFF OUT 3
13 D2 Q2 14 OUT BUFF OUT 2
15 D3 Q3 16 OUT BUFF OUT 1
2101-2
17 73-7 CHAN NO 0
17 73-9 CHAN NO 1
17 73-12 CHAN NO 2
4 C0
3 C1
2 C2
1 C3
21 C4
5 C5
6 C6
7 C7
W
20 18
0V
22 66-12 -,WRITE OUT BUFF
77
74157
12 47-11 WRITE POINTER 0 2 A0
12 47-14 WRITE POINTER 1 5 B0
12 48-3 WRITE POINTER 2 11 C0 A 4 BUFFER ADDR 0
12 48-6 WRITE POINTER 3 14 D0 B 7 BUFFER ADDR 1
12 48-14 READ POINTER 0 3 A1 C 9 BUFFER ADDR 2
12 28-3 READ POINTER 1 6 B1 D 12 BUFFER ADDR 3
12 28-6 READ POINTER 2 10 C1
12 28-11 READ POINTER 3 13 D1
S E
22 65-8 READ FROM BUFFER 1 15
0V
4
75157
12 48-11 WRITE POINTER 4 2 A0
5 B0
11 C0 A 4 BUFFER ADDR 4
14 D0 B 7
12 28-14 READ POINTER 4 3 A1 C 9
6 B1 D 12
10 C1
13 D1
S1 E
22 65-8 READ FROM BUFFER 1 15
0V

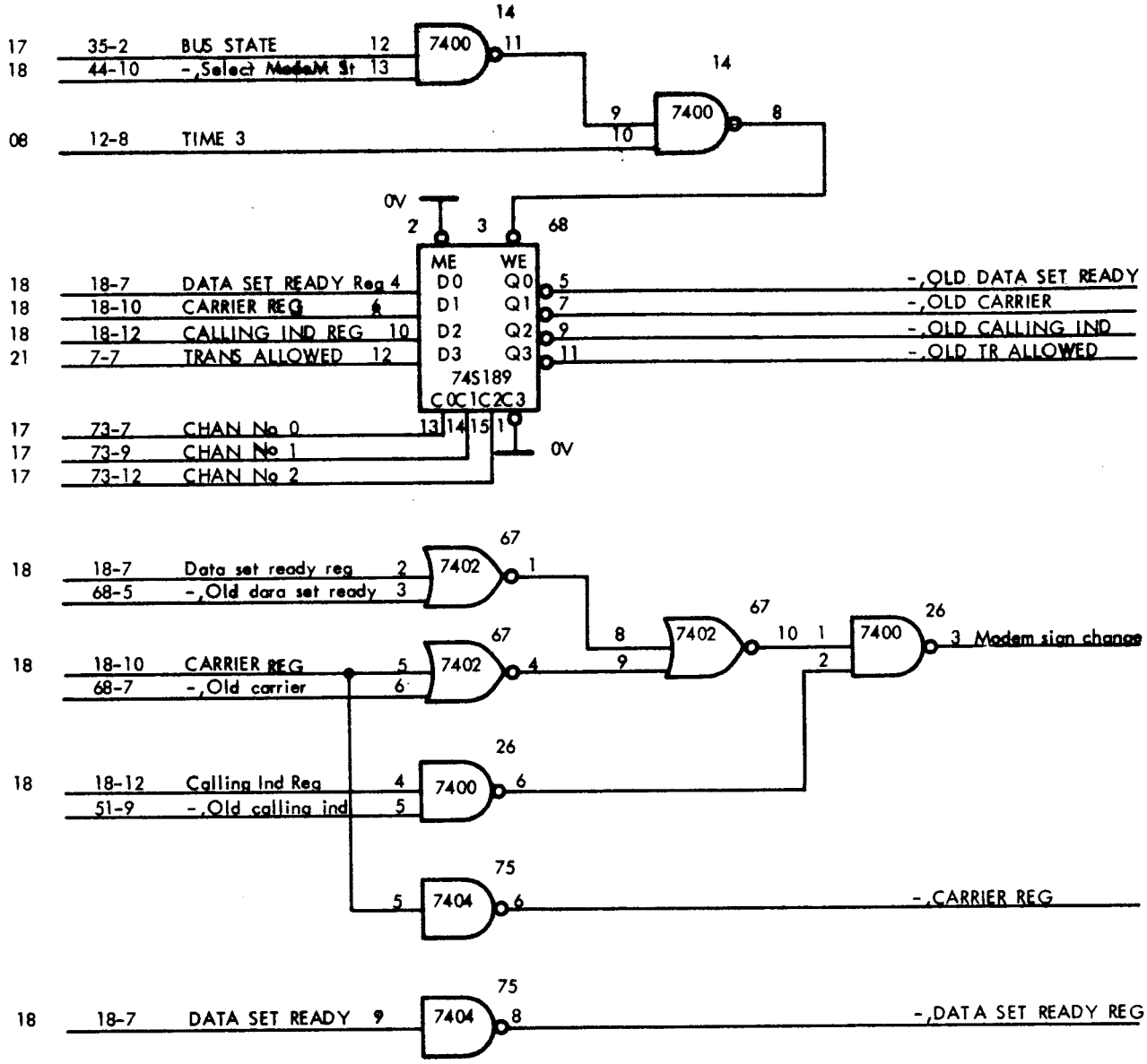

13 72-12 LOGIC ONE
0V
19
17
104
ME
16 33-8 -,(POLL/REDATA+,FULL)
16 97-4 CALLING!PARITY
16 97-7 -,CARRIER!FRAMING
16 97-9 -,D.S.R.!BREAK
9 11 13 15
D0 D1 D2 D3
Q0 Q1 Q2 Q3
10 12 14 16
IN BUFF OUT 0
IN BUFF OUT 1
IN BUFF OUT 2
IN BUFF OUT 3
2101-2
4 3 2 1 21 5 6 7
C0 C1 C2 C3 C4 C5 C6 C7
W
0D
20
18
22 65-6 -,WRITE IN BUFF
13 72-12 LOGIC ONE
0V
19
17
124
ME
16 76-4 RE DATA 8!ZERO
16 76-7 RE DATA 7!FULL
24 118-7 RE DATA 6
24 118-8 RE DATA 5
9 11 13 15
D0 D1 D2 D3
Q0 Q1 Q2 Q3
10 12 14 16
IN BUFF OUT 8
IN BUFF OUT 9
IN BUFF OUT 10
IN BUFF OUT 11
2101-2
4 3 2 1 21 5 6 7
C0 C1 C2 C3 C4 C5 C6 C7
W
0D
20
18
0V
22 65-6 -,WRITE IN BUFF
13 72-12 LOGIC ONE
0V
19
17
114
ME
24 118-9 RE DATA 4
24 118-10 RE DATA 3
24 118-11 RE DATA 2
24 118-12 RE DATA 1
9 11 13 15
D0 D1 D2 D3
Q0 Q1 Q2 Q3
10 12 14 16
IN BUFF OUT 12
IN BUFF OUT 13
IN BUFF OUT 14
IN BUFF OUT 15
2101-2
17 73-7 CHAN NO 0
17 73-9 CHAN NO 1
17 73-12 CHAN NO 2
14 77-4 BUFFER ADDR 0
14 77-7 BUFFER ADDR 1
14 77-9 BUFFER ADDR 2
14 77-12 BUFFER ADDR 3
14 4-4 BUFFER ADDR 4
4 3 2 1 21 5 6 7
C0 C1 C2 C3 C4 C5 C6 C7
W
0D
20
18
22 65-6 -,WRITE IN BUFF
0V

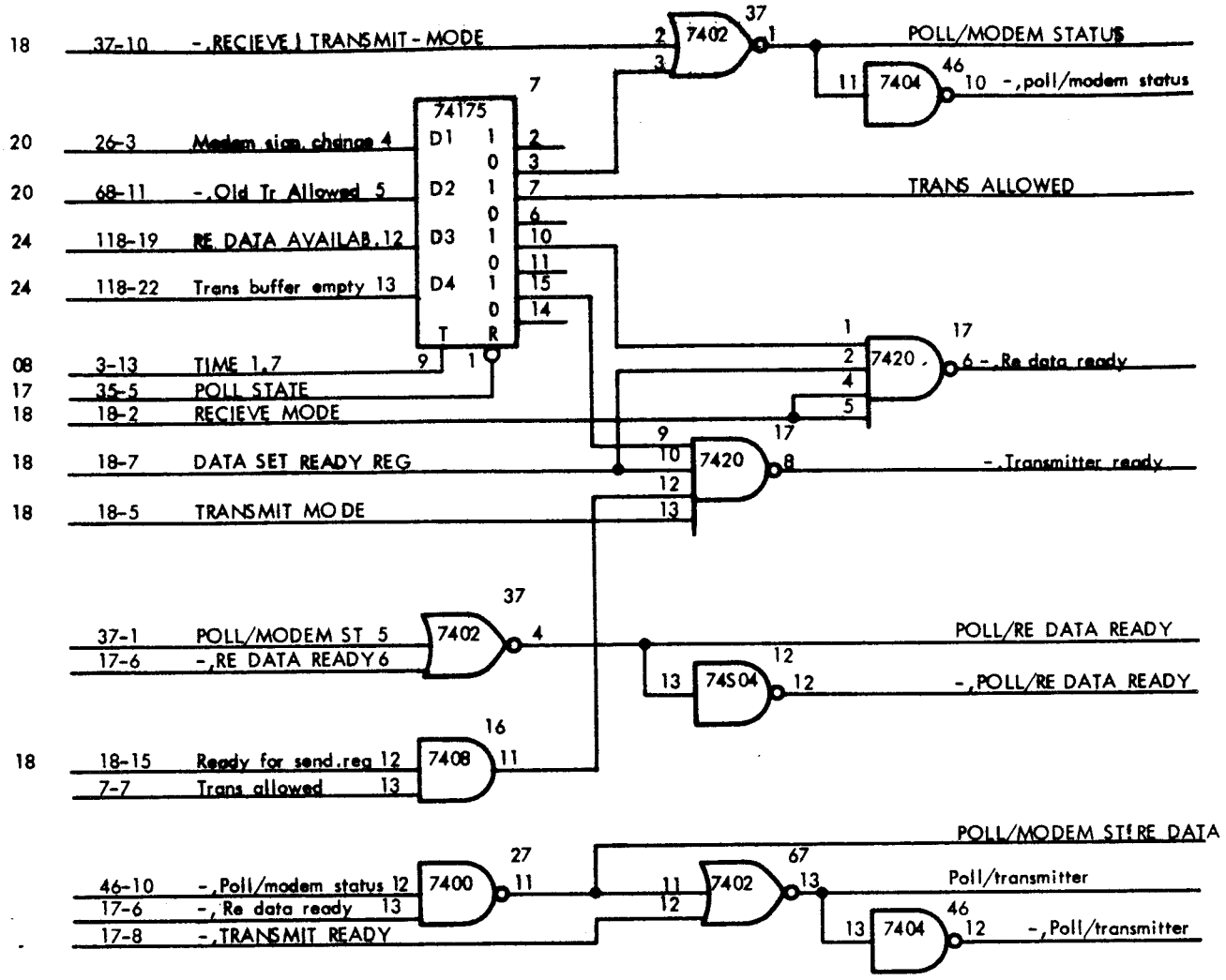

97
74157
18 18-12 CALLING IND REG
20 75-6 -,CARRIER REG
20 75-8 -,DATA SET READY REG
24 118-13 PARITY ERROR
24 118-14 FRAMING ERROR
103-11 BREAK RECIEVED
21 37-4 POLL/RE DATA READY
12 47-2 BUFF FULL
A0 B0 C0 D0 A1 B1 C1 D1 S E
CALLING!PARITY
-,CARRIER!FRAMING
-,D.S.R.!BREAK
76
74157
24 118-5 RE DATA 8
24 118-6 RE DATA 7
0V
RE DATA 8! ZERO
RE DATA 7! FULL
33
12 47-3 -,Buff full 9
21 37-4 Poll 10
/Re Data Ready
74S00
0V
-,(POLL/RE DATA ∧ -,FULL)
97-7 -,CARRIER!FRAMING
76-4 Re data 8! zero
76-7 Re data 7! full
95
7425
24 118-7 Re data 6
24 118-8 Re data 5
103
7408
BREAK RECIEVED
24 118-9 Re data 4
24 118-10 - 3
24 118-11 - 2
24 118-12 - 1
13 72-13 Logic one

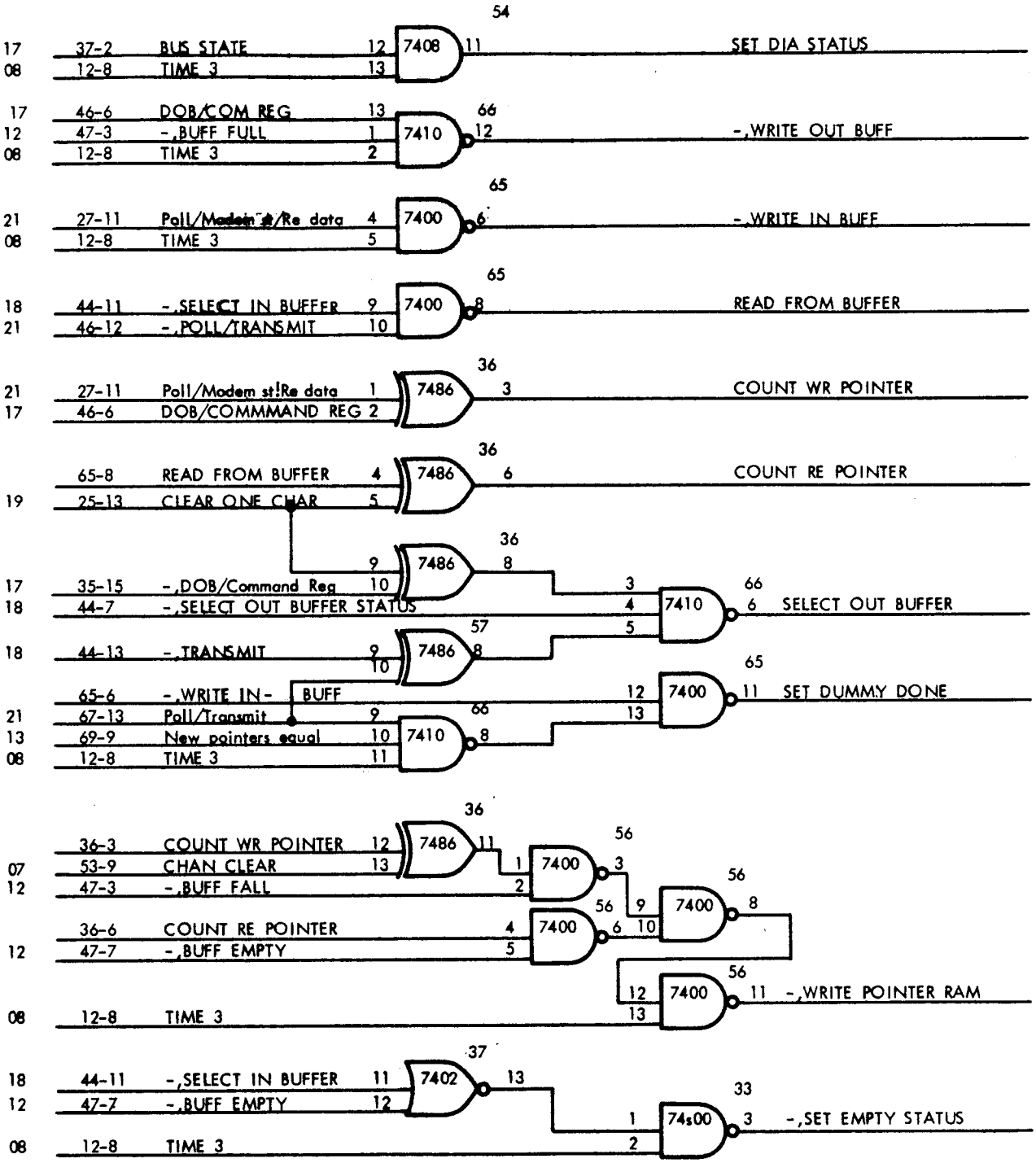

55
63-11 POLL/CHAN.NO 8
35-7 AMX/RESET REG
04 94-8 -,IORST
13 72-10 Logic one
7408
POLL/CHAN NO 8
63
74161
R E Co
T Pe Ci
0V
73
74157
A0 B0 C0 D0 A1 B1 C1 D1
S E
FINISHED
CHAN.NO.0
CHAN.NO.1
CHAN.NO.2
08 31-10 OSC/TIME 2!3
07 123-10 DATA OUT 5
07 123-12 DATA OUT 6
07 123-15 DATA OUT 7
08 13-11 -,TIME 4
7402
11-8 BUS STATE REQUEST
46-8 -,AMX/RESET REQ
BUS REQ A -,RESET
07 53-4 -,DOC/COMMAND
07 23-8 DATA OUT/COMMAND
07 34-7 AMX/RESET
74S74
-,BUS STATE REQ
08 13-8 -,TIME 3
13 72-9 Logic one
7404
-,Amx/ Reset Req
35
74174
D1 D2 D3 D4 D5 D6
Q1 Q2 Q3 Q4 Q5 Q6
11-8 BUS STATE REQUEST
11-9 -,BUS STATE REQUEST
07 34-7 AMX/RESET
07 34-4 -,DOA/COMMAND
07 34-9 -,DOB/COMMAND
BUS STATE
POLL STATE
AMX/RESET REQ
-,DOA/COM REQ
-,DOB/COM REQ
07 34-13 Bus Req Delay 4
08 3-15 TIME (1!2)
04 94-8 -,IORST
DOB/COMMAND REQ
91
73-4 FINISHED
08 12-8 TIME 3
74LS 00
-,COMMAND FINISHED


07 133-5 DATA OUT 11
7400
-,CHAN CLEAR
7400
7408
-,CHANGE RECIEVE
74LS138
13 72-11 Logic one
07 133-7 DATA OUT 12
17 35-12 -,DOA/Comm reg
07 133-10 DATA OUT 13
07 133-12 DATA OUT 14
07 133-15 DATA OUT 15
-,RECIEVE
-,STOP RECIEVE
-,TRANSMIT
-,STOP TRANSMIT
-,SELECT IN BUFFER
-,SELECT MODEM STATUS
-,SELECT IN BUFF STATUS
-,SELECT OUT BUFF ST
7408
-,CHANGE TRANSMIT
08 13-8 -,TIME 3
0V
7402
7400
3 New Rec/Tr mode
74S189
74174
55-3 -,NEW Recieve m
55-6 -,New transmit m
Recieve mode
Transmit mode
Data set rdy reg
Carrier reg
Calling ind reg
Ready for sending reg
17 73-7 CHAN No 0
17 73-9 CHAN No 1
17 73-12 CHAN No 2
64-1 DATA SET READY IN
29 30-6 CARRIER
30 99-6 CALLING IND
31 100-6 READY FOR SENDING
08 3-14 TIME 1,3
17 46-8 -,AMX /RESET REG
54-3 -,Change recieve
18-2 Recieve mode
44-15 -,Recieve
-,New recieve mode
54-6 -,Change transmit
18-5 Transmit mode
44-13 -,TRANSMIT
-,NEW TRANSMIT MODE
28 50-5 -,DATA SET READY
20 68-5 -,OLD DATA SET READY
65-3 New rec Tr mode
44-10 -,Select Modem St
7402
1 Data set ready in
18-2 RECIEVE MODE
18-5 TRANSMIT MODE
-,RECIEVE TRANSMIT MODE
7404
-,TRANSMIT MODE

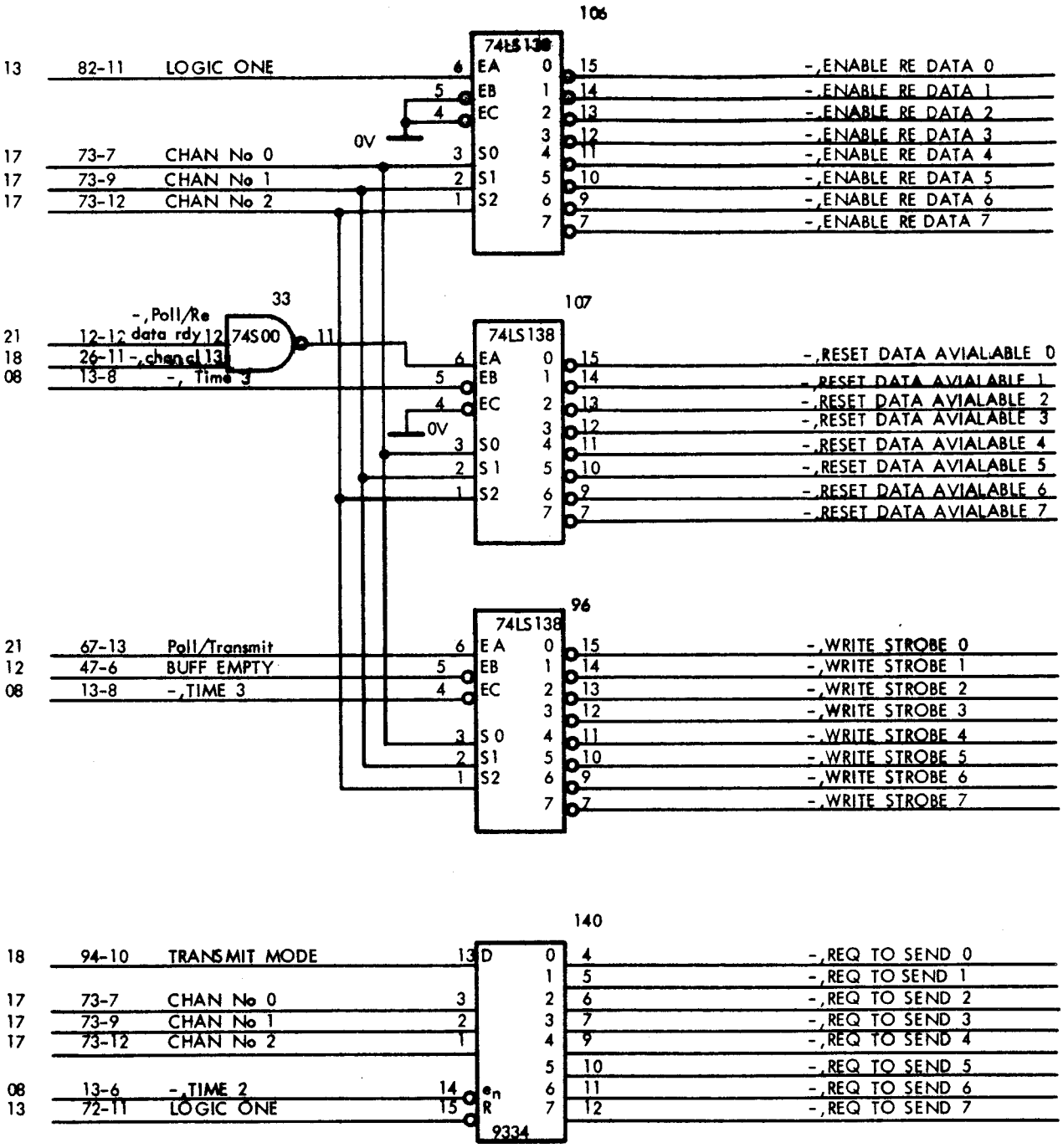

24
74LS138
07 133-7 DATA OUT 12 6 EA 0 15 -,SET DTR
17 35-12 -,DOA COMMAND reg 5 EB 1 14 -,CLEAR DTR
08 13-6 -,TIME2 4 EC 2 13
3 12
07 133-10 DATA OUT 13 3 S0 4 11 -,START BREAK
07 133-12 DATA OUT 14 2 S1 5 10 -,CLEAR BREAK
07 133-15 DATA OUT 15 1 S2 6 9 -,ENABLE INT COM
7 7
15
12 7408 11 -,Move DTR com
13
-,clear one char & time 2
57
12 7486 11
17 35-7 AMX/RESET REG 13
129
13 D 0 4 -,DATA TERM READY 0
1 5 -,DATA TERM READY 1
17 73-7 CHAN No 0 3 2 6 -,DATA TERM READY 2
17 73-9 CHAN No 1 2 3 7 -,DATA TERM READY 3
17 73-12 CHAN No 2 1 4 9 -,DATA TERM READY 4
5 10 -,DATA TERM READY 5
16-3 -,MOVE DTR 14 en 6 11 -,DATA TERM READY 6
15 R 7 12 -,DATA TERM READY 7
9334
150
13 D 0 4 -,BREAK 0
1 5 -,BREAK 1
17 73-7 CHAN No 0 3 2 6 -,BREAK 2
17 73-9 CHAN No 1 2 3 7 -,BREAK 3
17 73-12 CHAN No 2 1 4 9 -,BREAK 4
5 10 -,BREAK 5
25-10 -,Move Break 14 en 6 11 -,BREAK 6
13 72-13 Logic one 15 R 7 12 -,BREAK 7
9334
07 133-7 DATA OUT 12 1
07 133-10 DATA OUT 13 2 7420 23
07 133-12 DATA OUT 14 4 6
07 133-15 DATA OUT 15 5 25
17 35-12 -,DOA/COMMAND REG 11 7402 13 CLEAR ONE CHAR
12
24-11 -,START BREAK 9 7400 26 8 8 7402 25 10 -,MOVE BREAK
24-10 -,CLEAR BREAK 10 9
15 45
17 45-7 AMX RESET REG 9 7408 8 9 7400 8
08 41-12 TIME 213 10 10
16
1 7408 3 -,MOVE DTR
46-11 -,MOVE DTR COM 2

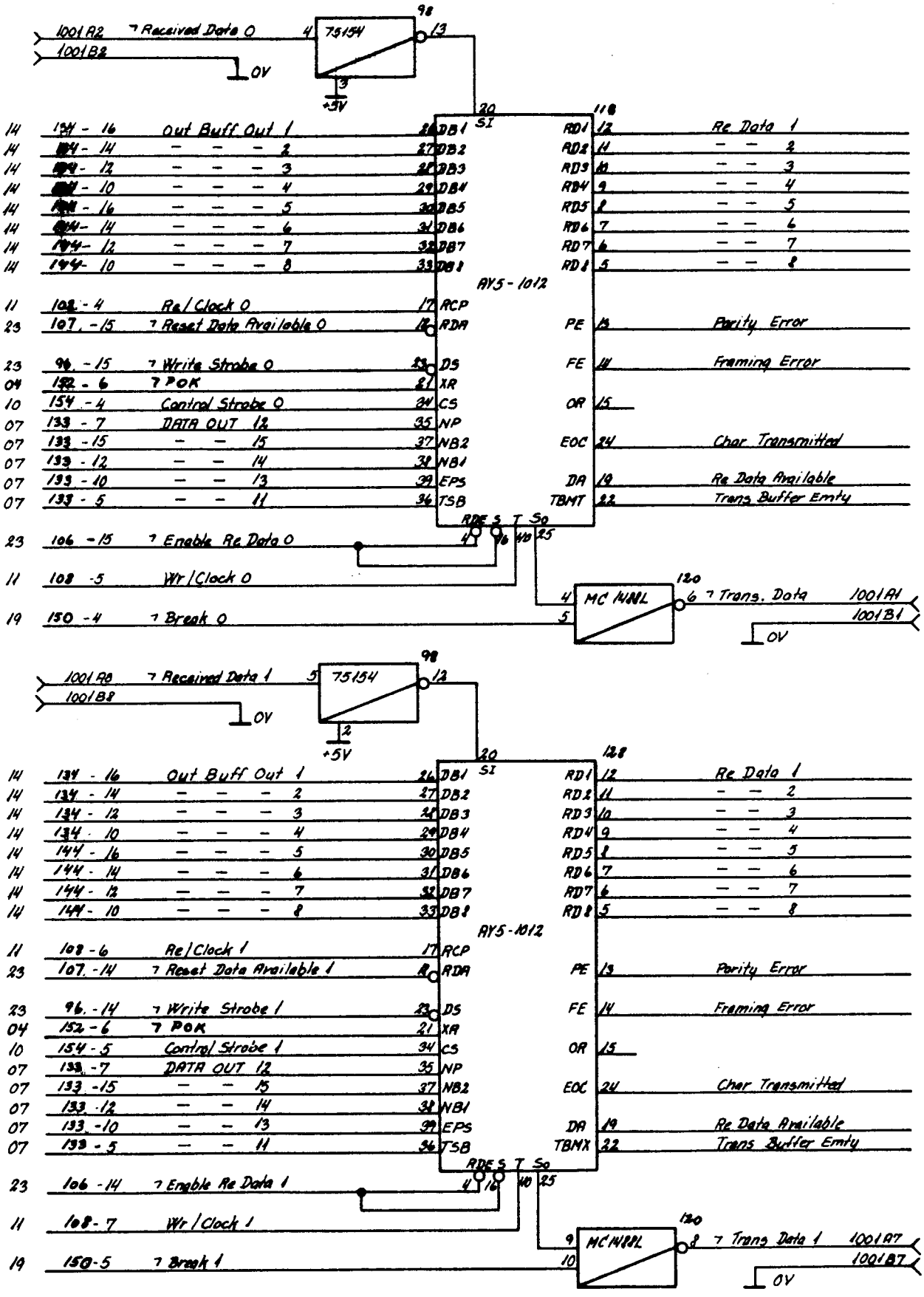

17 35-2 BUS STATE 12
18 44-10 -,Select Modem St 13
7400
14
11
14
9
10
7400
8
08 12-8 TIME 3
0V
2
3
68
ME
WE
18 18-7 DATA SET READY Reg 4
18 18-10 CARRIER REG 6
18 18-12 CALLING IND REG 10
21 7-7 TRANS ALLOWED 12
D0
D1
D2
D3
Q0
Q1
Q2
Q3
5
7
9
11
-,OLD DATA SET READY
-,OLD CARRIER
-,OLD CALLING IND
-,OLD TR ALLOWED
74S189
C0C1C2C3
17 73-7 CHAN No 0
17 73-9 CHAN No 1
17 73-12 CHAN No 2
13
14
15
1
0V
18 18-7 Data set ready reg 2
68-5 -,Old data set ready 3
7402
67
1
18 18-10 CARRIER REG 5
68-7 -,Old carrier 6
7402
67
4
8
9
7402
67
10
1
2
7400
26
3 Modem sign change
18 18-12 Calling Ind Reg 4
51-9 -,Old calling ind 5
7400
26
6
5
7404
75
6
-,CARRIER REG
18 18-7 DATA SET READY 9
7404
75
8
-,DATA SET READY REG


18 37-10 -,RECIEVE/TRANSMIT-MODE
7402
POLL/MODEM STATUS
7404
-,poll/modem status
74175
20 26-3 Modem sign. change 4
20 68-11 -,Old Tr Allowed 5
24 118-19 RE DATA AVAILAB.12
24 118-22 Trans buffer empty 13
D1
D2
D3
D4
TRANS ALLOWED
08 3-13 TIME 1.7
17 35-5 POLL STATE
18 18-2 RECIEVE MODE
7420
-,Re data ready
18 18-7 DATA SET READY REG
18 18-5 TRANSMIT MODE
-,Transmitter ready
37-1 POLL/MODEM ST 5
17-6 -,RE DATA READY 6
POLL/RE DATA READY
74S04
-,POLL/RE DATA READY
18 18-15 Ready for send.reg 12
7-7 Trans allowed 13
7408
POLL/MODEM ST/RE DATA
46-10 -,Poll/modem status 12
17-6 -,Re data ready 13
17-8 -,TRANSMIT READY
7400
Poll/transmitter
-,Poll/transmitter

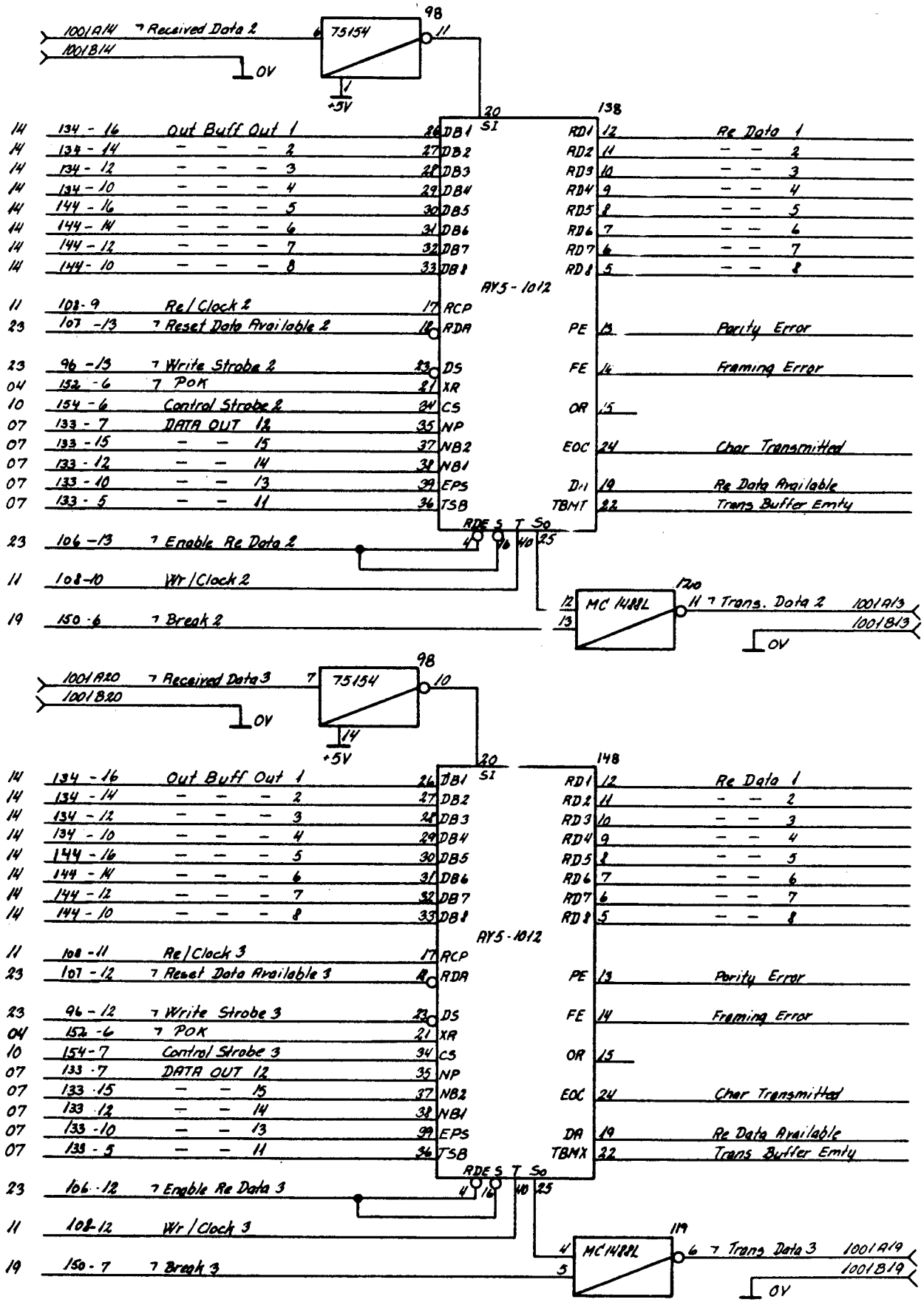


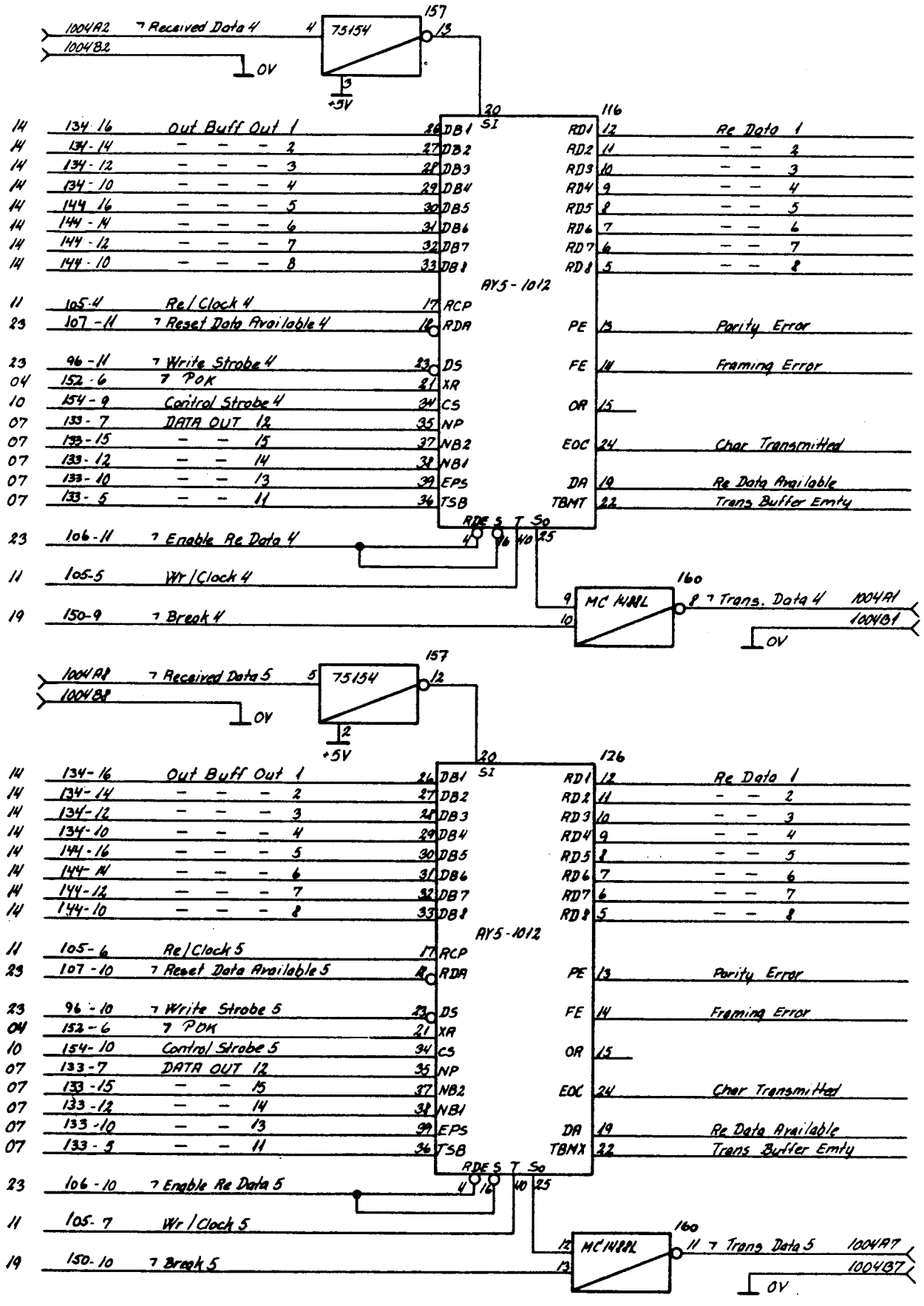
CONTROL LOGIC for INPUT BUFFER and OUTPUT BUFFER
Logic diagram


106
74LS138
13 82-11 LOGIC ONE
0V
17 73-7 CHAN No 0
17 73-9 CHAN No 1
17 73-12 CHAN No 2
EA EB EC S0 S1 S2
-,ENABLE RE DATA 0
-,ENABLE RE DATA 1
-,ENABLE RE DATA 2
-,ENABLE RE DATA 3
-,ENABLE RE DATA 4
-,ENABLE RE DATA 5
-,ENABLE RE DATA 6
-,ENABLE RE DATA 7
33
-,Poll/Re
21 12-12 data rdy 12
18 26-11 -,chan sl 13
08 13-8 -, Time 3
74S00
107
74LS138
-,RESET DATA AVIALABLE 0
-,RESET DATA AVIALABLE 1
-,RESET DATA AVIALABLE 2
-,RESET DATA AVIALABLE 3
-,RESET DATA AVIALABLE 4
-,RESET DATA AVIALABLE 5
-,RESET DATA AVIALABLE 6
-,RESET DATA AVIALABLE 7
96
74LS138
21 67-13 Poll/Transmit
12 47-6 BUFF EMPTY
08 13-8 -,TIME 3
-,WRITE STROBE 0
-,WRITE STROBE 1
-,WRITE STROBE 2
-,WRITE STROBE 3
-,WRITE STROBE 4
-,WRITE STROBE 5
-,WRITE STROBE 6
-,WRITE STROBE 7
140
18 94-10 TRANSMIT MODE
17 73-7 CHAN No 0
17 73-9 CHAN No 1
17 73-12 CHAN No 2
08 13-6 -,TIME 2
13 72-11 LOGIC ONE
D en R
9334
-,REQ TO SEND 0
-,REQ TO SEND 1
-,REQ TO SEND 2
-,REQ TO SEND 3
-,REQ TO SEND 4
-,REQ TO SEND 5
-,REQ TO SEND 6
-,REQ TO SEND 7



UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (0:1)
Logic Diagram

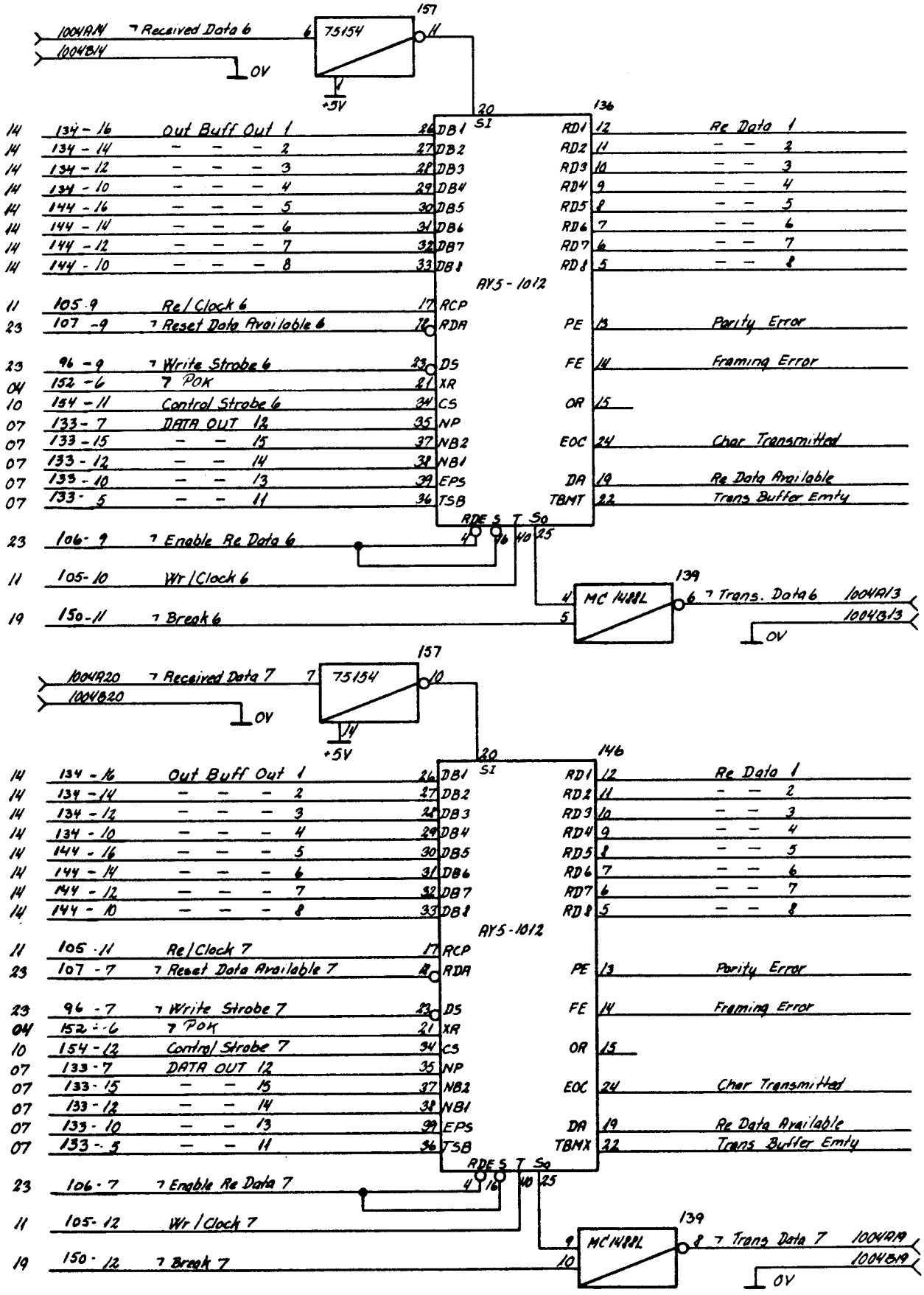

1001A14 ⌐ Received Data 2
1001B14
0V
75154
98
11
+5V
20
SI
138
14 134-16 Out Buff Out 1
14 134-14 — — — 2
14 134-12 — — — 3
14 134-10 — — — 4
14 144-16 — — — 5
14 144-14 — — — 6
14 144-12 — — — 7
14 144-10 — — — 8
11 108-9 Re/Clock 2
23 107-13 ⌐ Reset Data Available 2
23 96-13 ⌐ Write Strobe 2
04 152-6 ⌐ POK
10 154-6 Control Strobe 2
07 133-7 DATA OUT 12
07 133-15 — — 15
07 133-12 — — 14
07 133-10 — — 13
07 133-5 — — 11
23 106-13 ⌐ Enable Re Data 2
11 108-10 Wr/Clock 2
19 150-6 ⌐ Break 2
DB1 DB2 DB3 DB4 DB5 DB6 DB7 DB8
RCP
RDA
DS
XR
CS
NP
NB2
NB1
EPS
TSB
AY5-1012
RD1 RD2 RD3 RD4 RD5 RD6 RD7 RD8
PE
FE
OR
EOC
DAI
TBMT
RDE S T So
Re Data 1
— — 2
— — 3
— — 4
— — 5
— — 6
— — 7
— — 8
Parity Error
Framing Error
Char Transmitted
Re Data Available
Trans Buffer Emty
MC 1488L
120
⌐ Trans. Data 2
1001A13
1001B13
0V
1001A20 ⌐ Received Data 3
1001B20
0V
75154
98
10
+5V
20
SI
148
14 134-16 Out Buff Out 1
14 134-14 — — — 2
14 134-12 — — — 3
14 134-10 — — — 4
14 144-16 — — — 5
14 144-14 — — — 6
14 144-12 — — — 7
14 144-10 — — — 8
11 108-11 Re/Clock 3
23 107-12 ⌐ Reset Data Available 3
23 96-12 ⌐ Write Strobe 3
04 152-6 ⌐ POK
10 154-7 Control Strobe 3
07 133-7 DATA OUT 12
07 133-15 — — 15
07 133-12 — — 14
07 133-10 — — 13
07 133-5 — — 11
23 106-12 ⌐ Enable Re Data 3
11 108-12 Wr/Clock 3
19 150-7 ⌐ Break 3
DB1 DB2 DB3 DB4 DB5 DB6 DB7 DB8
RCP
RDA
DS
XR
CS
NP
NB2
NB1
EPS
TSB
AY5-1012
RD1 RD2 RD3 RD4 RD5 RD6 RD7 RD8
PE
FE
OR
EOC
DA
TBMX
RDE S T So
Re Data 1
— — 2
— — 3
— — 4
— — 5
— — 6
— — 7
— — 8
Parity Error
Framing Error
Char Transmitted
Re Data Available
Trans Buffer Emty
MC1488L
119
⌐ Trans Data 3
1001A19
1001B19
0V

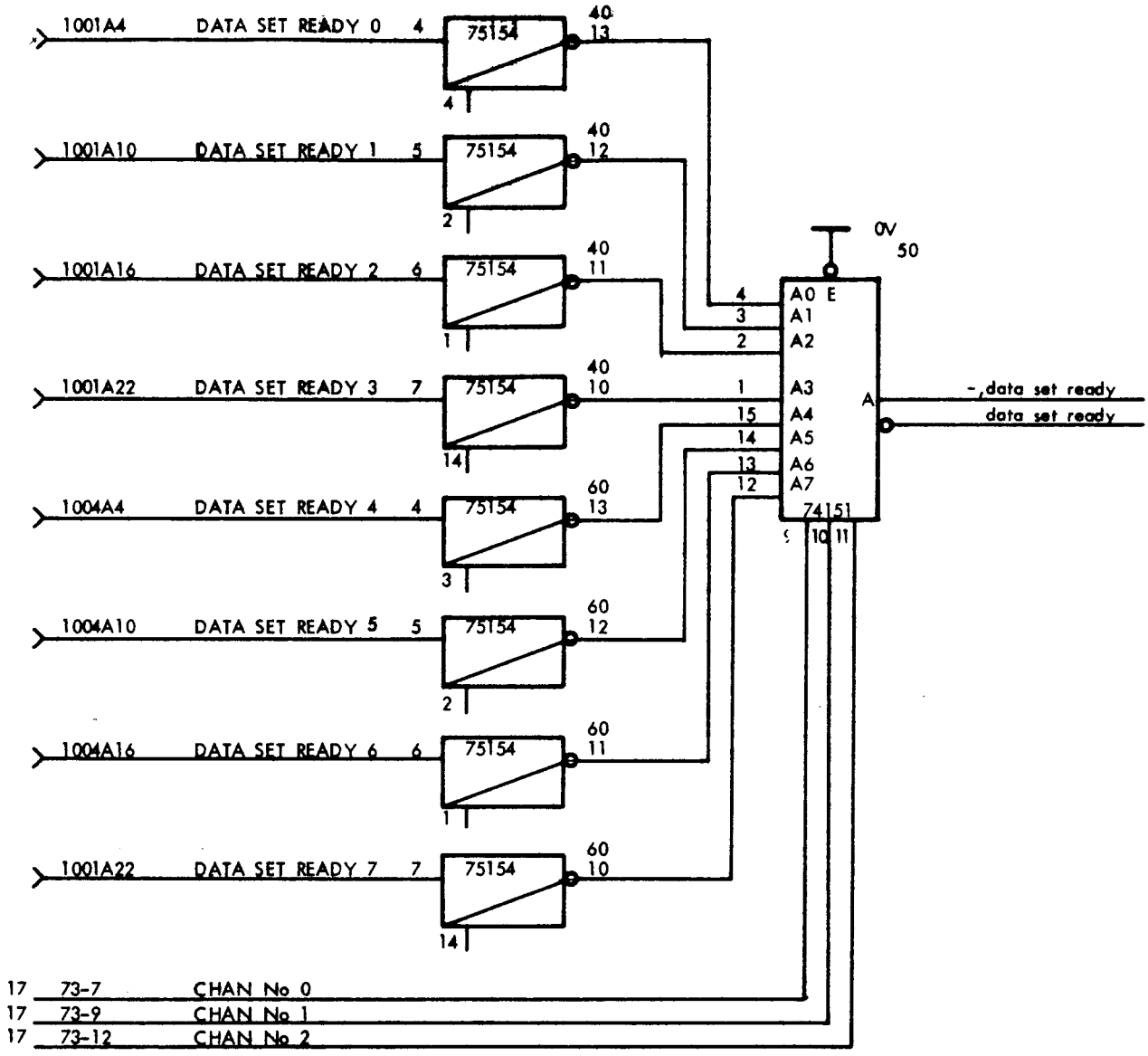


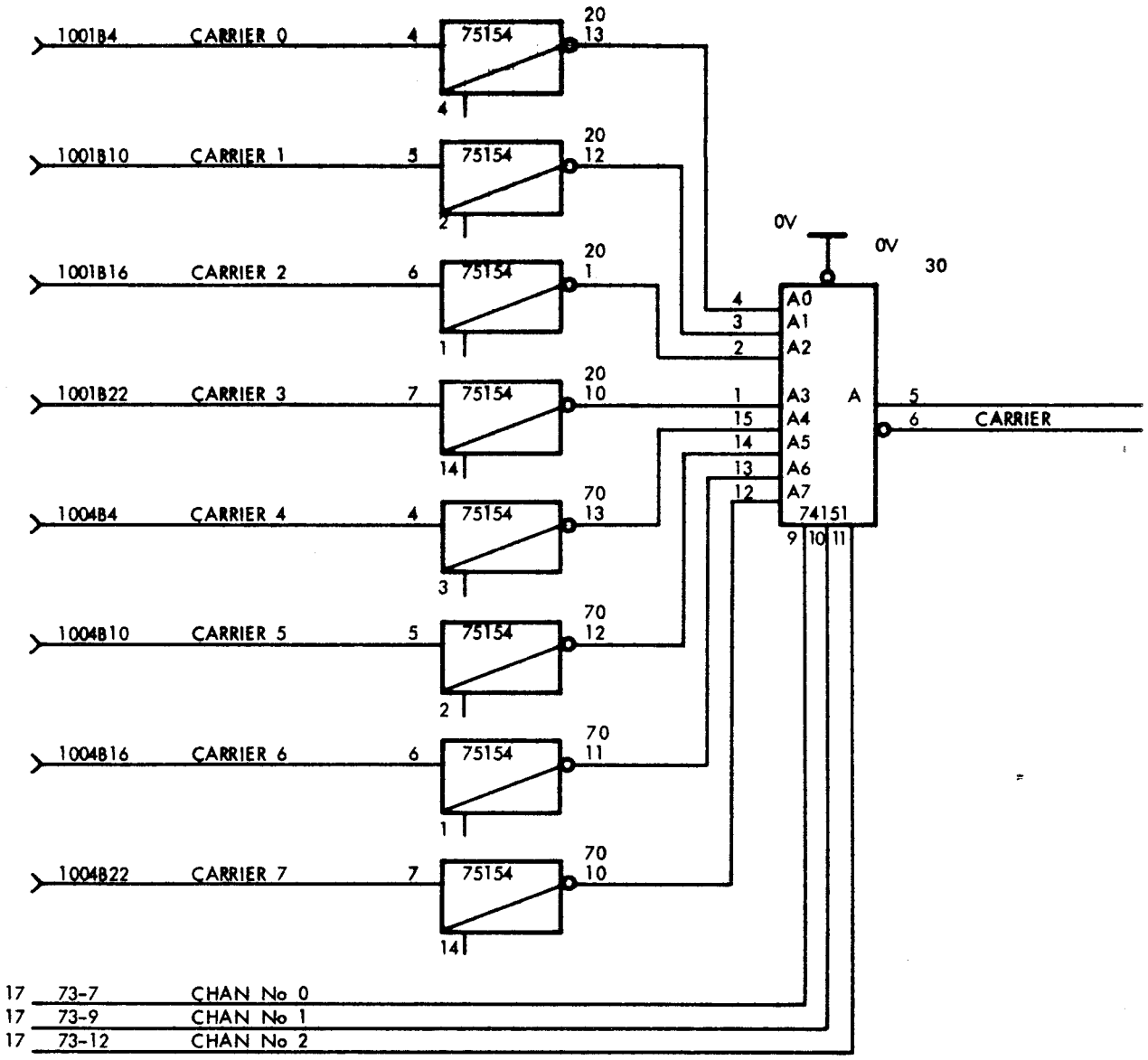
AMX 702
R 12106

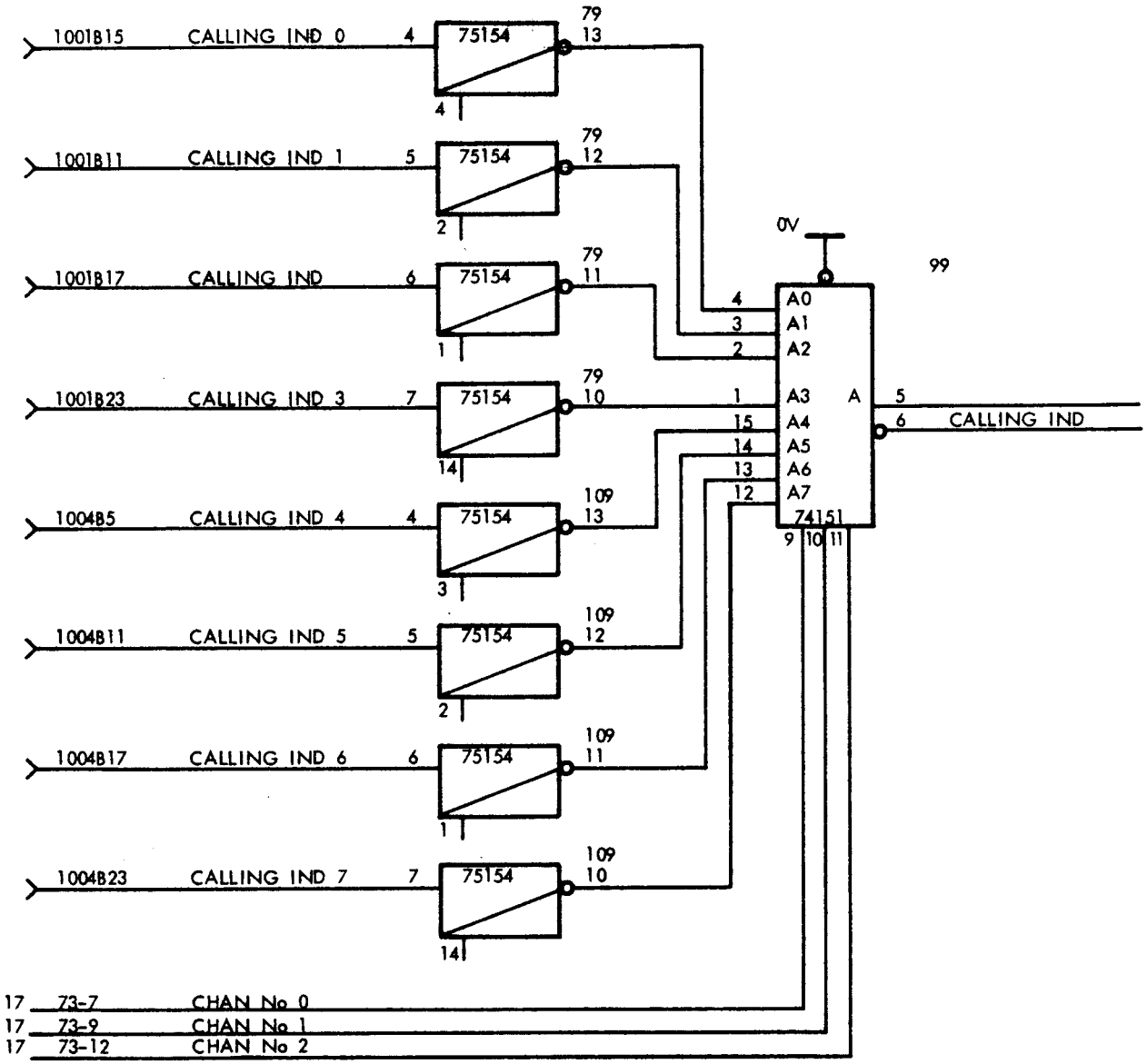
UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (4-5)
Logic Diagram

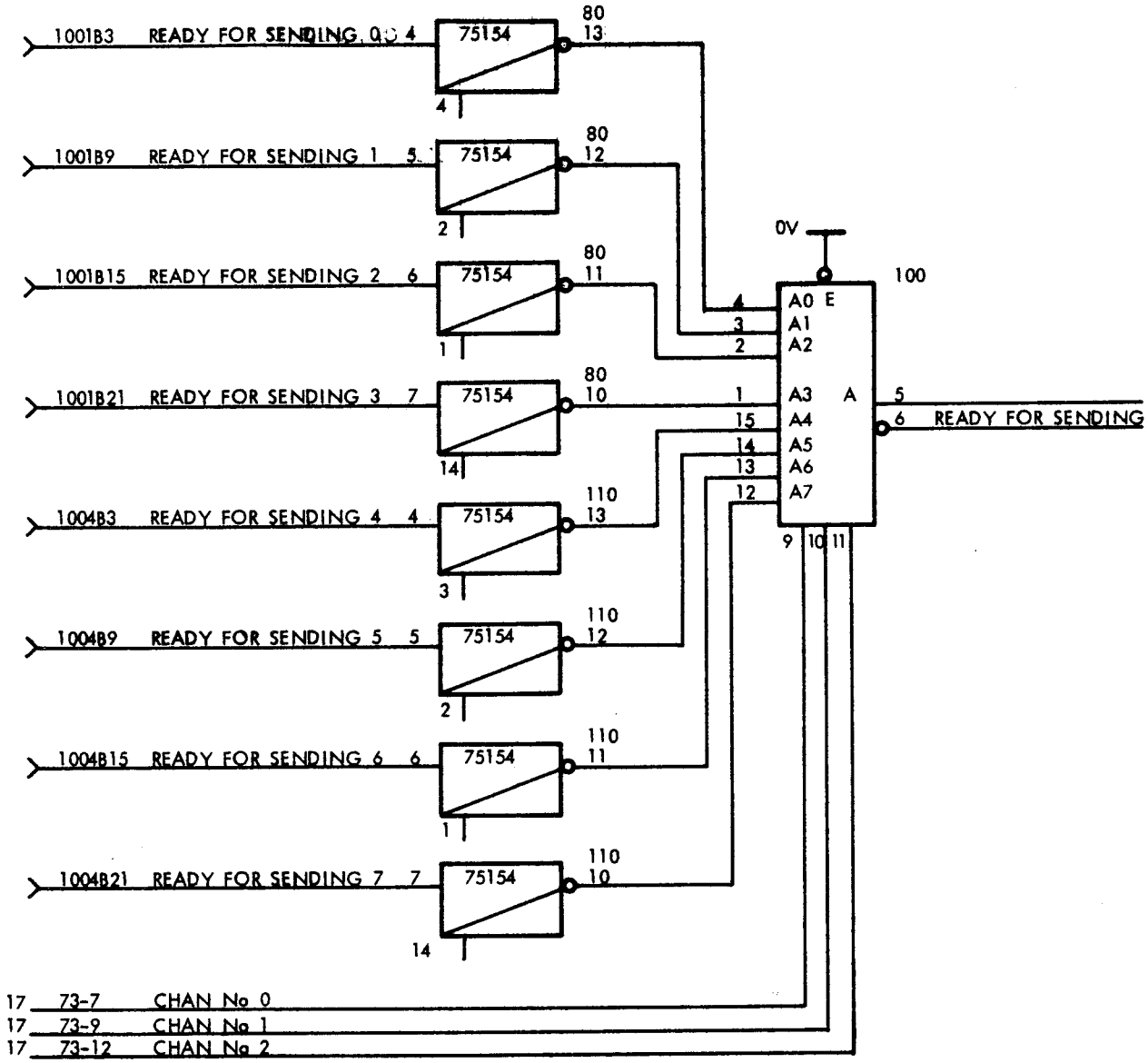
AMX 26

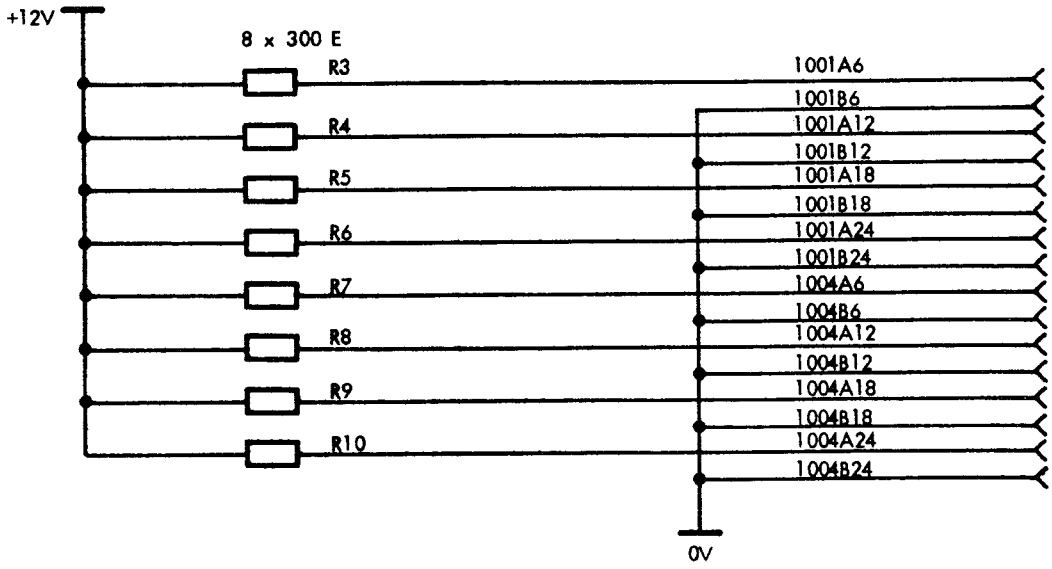

157
1004A/M ¬ Received Data 6
6
75154
11
1004B/4
0V
+5V
20
SI
136
14 134-16 Out Buff Out 1 26 DB1 RD1 12 Re Data 1
14 134-14 - - - 2 27 DB2 RD2 11 - - 2
14 134-12 - - - 3 28 DB3 RD3 10 - - 3
14 134-10 - - - 4 29 DB4 RD4 9 - - 4
14 144-16 - - - 5 30 DB5 RD5 8 - - 5
14 144-14 - - - 6 31 DB6 RD6 7 - - 6
14 144-12 - - - 7 32 DB7 RD7 6 - - 7
14 144-10 - - - 8 33 DB8 RD8 5 - - 8
AY5-1012
11 105-9 Re/Clock 6 17 RCP
23 107-9 ¬ Reset Data Available 6 18 RDA PE 13 Parity Error
23 96-9 ¬ Write Strobe 6 23 DS FE 14 Framing Error
04 152-6 ¬ POK 21 XR
10 154-11 Control Strobe 6 34 CS OR 15
07 133-7 DATA OUT 12 35 NP
07 133-15 - - 15 37 NB2 EOC 24 Char Transmitted
07 133-12 - - 14 38 NB1
07 133-10 - - 13 39 EPS DA 19 Re Data Available
07 133-5 - - 11 36 TSB TBMT 22 Trans Buffer Emty
RDE S T So
23 106-9 ¬ Enable Re Data 6 4 16 40 25
11 105-10 Wr/Clock 6
19 150-11 ¬ Break 6 5
139
4 MC 1488L 6 ¬ Trans. Data 6 1004A/3 1004B/3
0V
157
1004A20 ¬ Received Data 7
7
75154
10
1004B20
0V
14
+5V
20
SI
146
14 134-16 Out Buff Out 1 26 DB1 RD1 12 Re Data 1
14 134-14 - - - 2 27 DB2 RD2 11 - - 2
14 134-12 - - - 3 28 DB3 RD3 10 - - 3
14 134-10 - - - 4 29 DB4 RD4 9 - - 4
14 144-16 - - - 5 30 DB5 RD5 8 - - 5
14 144-14 - - - 6 31 DB6 RD6 7 - - 6
14 144-12 - - - 7 32 DB7 RD7 6 - - 7
14 144-10 - - - 8 33 DB8 RD8 5 - - 8
AY5-1012
11 105-11 Re/Clock 7 17 RCP
23 107-7 ¬ Reset Data Available 7 18 RDA PE 13 Parity Error
23 96-7 ¬ Write Strobe 7 23 DS FE 14 Framing Error
04 152-6 ¬ POK 21 XR
10 154-12 Control Strobe 7 34 CS OR 15
07 133-7 DATA OUT 12 35 NP
07 133-15 - - 15 37 NB2 EOC 24 Char Transmitted
07 133-12 - - 14 38 NB1
07 133-10 - - 13 39 EPS DA 19 Re Data Available
07 133-5 - - 11 36 TSB TBMT 22 Trans Buffer Emty
RDE S T So
23 106-7 ¬ Enable Re Data 7 4 16 40 25
11 105-12 Wr/Clock 7
19 150-12 ¬ Break 7 10
139
9 MC1488L 8 ¬ Trans Data 7 1004A/9 1004B/9
0V


1001A4 DATA SET READY 0 4
1001A10 DATA SET READY 1 5
1001A16 DATA SET READY 2 6
1001A22 DATA SET READY 3 7
1004A4 DATA SET READY 4 4
1004A10 DATA SET READY 5 5
1004A16 DATA SET READY 6 6
1001A22 DATA SET READY 7 7
75154
0V
50
A0 E
A1
A2
A3
A4
A5
A6
A7
74151
data set ready
data set ready
17 73-7 CHAN No 0
17 73-9 CHAN No 1
17 73-12 CHAN No 2


1001B4 CARRIER 0 4 75154 20 13 4
1001B10 CARRIER 1 5 75154 20 12 2
1001B16 CARRIER 2 6 75154 20 1 1
1001B22 CARRIER 3 7 75154 20 10 14
1004B4 CARRIER 4 4 75154 70 13 3
1004B10 CARRIER 5 5 75154 70 12 2
1004B16 CARRIER 6 6 75154 70 11 1
1004B22 CARRIER 7 7 75154 70 10 14
0V
0V
30
A0 4
A1 3
A2 2
A3 1
A4 15
A5 14
A6 13
A7 12
A
74151
9 10 11
5
6 CARRIER
17 73-7 CHAN No 0
17 73-9 CHAN No 1
17 73-12 CHAN No 2


1001B15
CALLING IND 0
4
75154
79
13
4
1001B11
CALLING IND 1
5
75154
79
12
2
1001B17
CALLING IND
6
75154
79
11
1
1001B23
CALLING IND 3
7
75154
79
10
14
1004B5
CALLING IND 4
4
75154
109
13
3
1004B11
CALLING IND 5
5
75154
109
12
2
1004B17
CALLING IND 6
6
75154
109
11
1
1004B23
CALLING IND 7
7
75154
109
10
14
0V
99
4
3
2
1
15
14
13
12
A0
A1
A2
A3
A4
A5
A6
A7
A
74151
9
10
11
5
6
CALLING IND
17
73-7
CHAN No 0
17
73-9
CHAN No 1
17
73-12
CHAN No 2





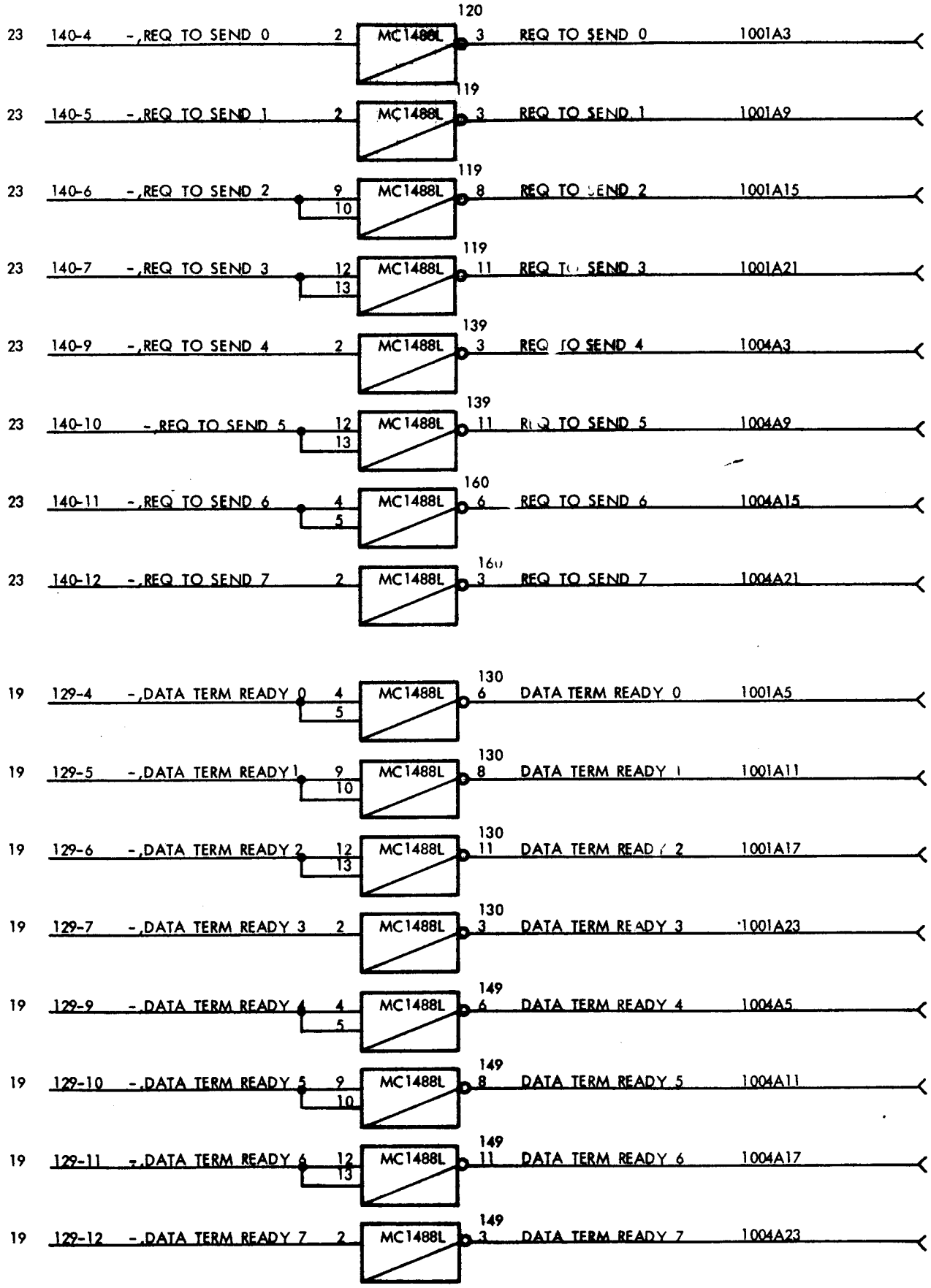
AMX 702

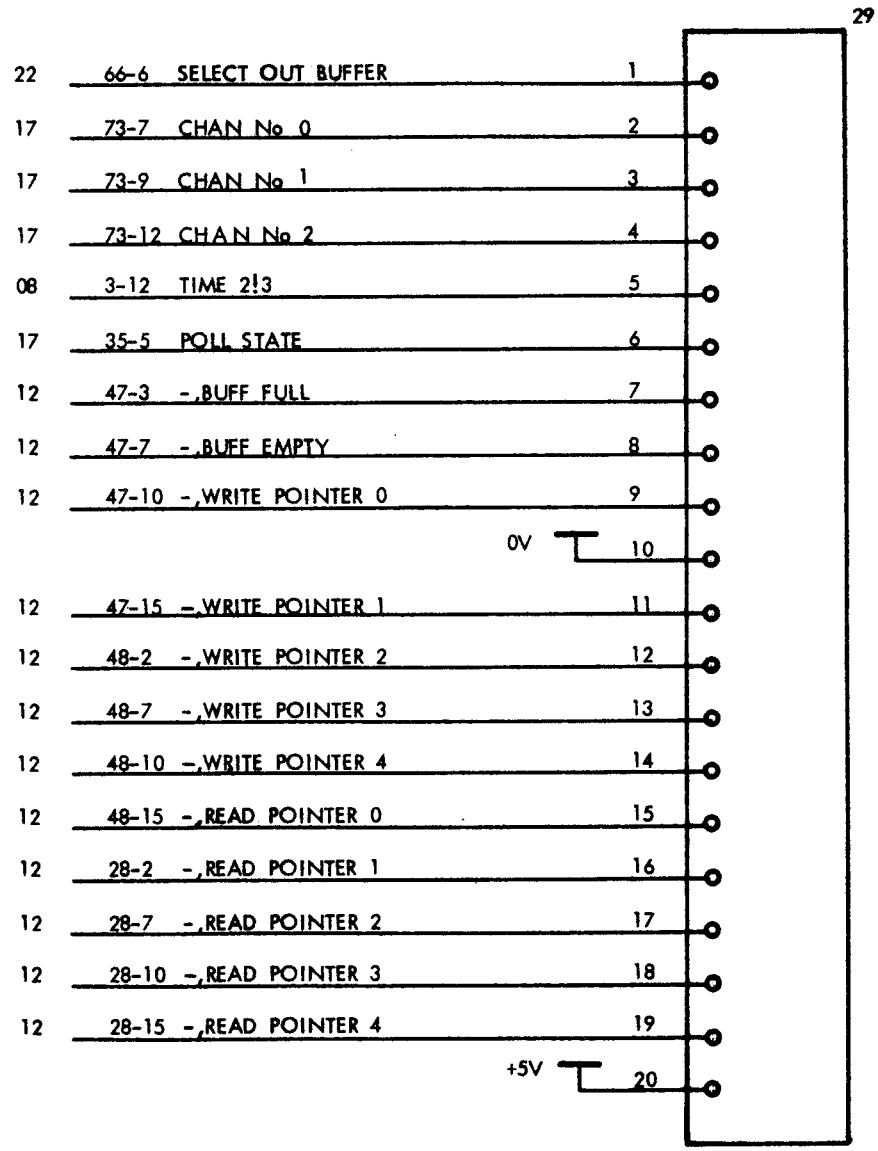
R 12111

MODEM INPUT SIGNAL READY FOR SENDING

Logic diagram

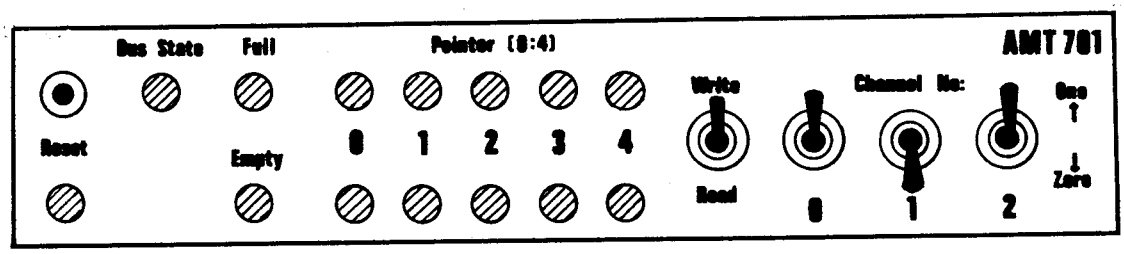
AMX 31


23 140-4 -,REQ TO SEND 0 2 MC1488L 120 3 REQ TO SEND 0 1001A3
23 140-5 -,REQ TO SEND 1 2 MC1488L 119 3 REQ TO SEND 1 1001A9
23 140-6 -,REQ TO SEND 2 9 10 MC1488L 119 8 REQ TO SEND 2 1001A15
23 140-7 -,REQ TO SEND 3 12 13 MC1488L 119 11 REQ TO SEND 3 1001A21
23 140-9 -,REQ TO SEND 4 2 MC1488L 139 3 REQ TO SEND 4 1004A3
23 140-10 -,REQ TO SEND 5 12 13 MC1488L 139 11 REQ TO SEND 5 1004A9
23 140-11 -,REQ TO SEND 6 4 5 MC1488L 160 6 REQ TO SEND 6 1004A15
23 140-12 -,REQ TO SEND 7 2 MC1488L 160 3 REQ TO SEND 7 1004A21
19 129-4 -,DATA TERM READY 0 4 5 MC1488L 130 6 DATA TERM READY 0 1001A5
19 129-5 -,DATA TERM READY 1 9 10 MC1488L 130 8 DATA TERM READY 1 1001A11
19 129-6 -,DATA TERM READY 2 12 13 MC1488L 130 11 DATA TERM READY 2 1001A17
19 129-7 -,DATA TERM READY 3 2 MC1488L 130 3 DATA TERM READY 3 1001A23
19 129-9 -,DATA TERM READY 4 4 5 MC1488L 149 6 DATA TERM READY 4 1004A5
19 129-10 -,DATA TERM READY 5 9 10 MC1488L 149 8 DATA TERM READY 5 1004A11
19 129-11 -,DATA TERM READY 6 12 13 MC1488L 149 11 DATA TERM READY 6 1004A17
19 129-12 -,DATA TERM READY 7 2 MC1488L 149 3 DATA TERM READY 7 1004A23


29
22 66-6 SELECT OUT BUFFER 1
17 73-7 CHAN No 0 2
17 73-9 CHAN No 1 3
17 73-12 CHAN No 2 4
08 3-12 TIME 2!3 5
17 35-5 POLL STATE 6
12 47-3 -,BUFF FULL 7
12 47-7 -,BUFF EMPTY 8
12 47-10 -,WRITE POINTER 0 9
0V 10
12 47-15 -,WRITE POINTER 1 11
12 48-2 -,WRITE POINTER 2 12
12 48-7 -,WRITE POINTER 3 13
12 48-10 -,WRITE POINTER 4 14
12 48-15 -,READ POINTER 0 15
12 28-2 -,READ POINTER 1 16
12 28-7 -,READ POINTER 2 17
12 28-10 -,READ POINTER 3 18
12 28-15 -,READ POINTER 4 19
+5V 20

Description of the AMT 701

The AMT 701 Asynchronous Multiplexor Test Box can be used together with the AMX 701, AMX 702. The AMT 701 must then be connected to the AMX 701 or to the AMX 702 at pos. 29 with a cable which is connected to pos. 40 on the controller board.



Front of Test Box

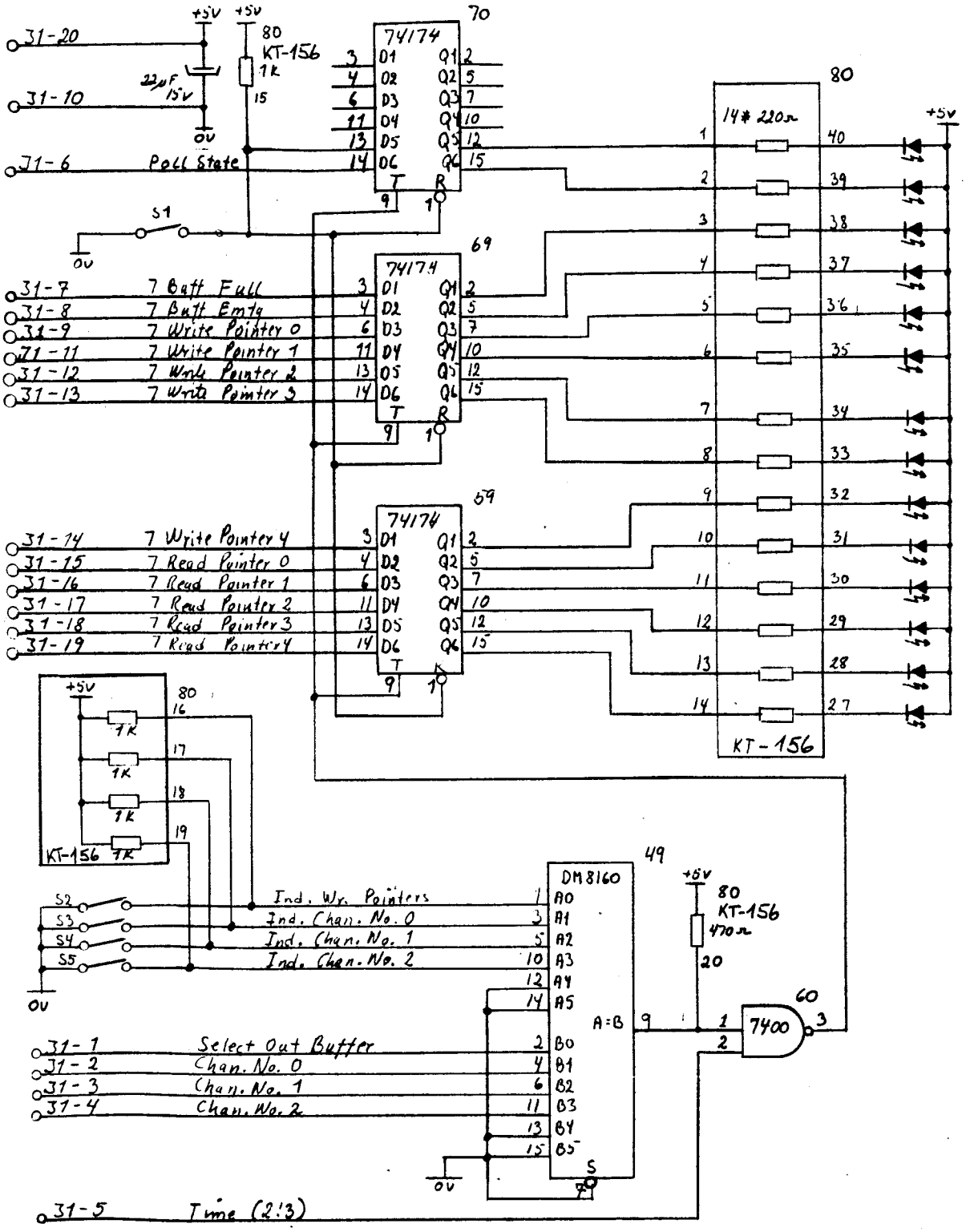
When using the Test Box the operator selects the wanted Channel No. by means of the three switches and with the fourth selects the Output Buffer or the Input Buffer (Write for Output Buffer and Read for Input Buffer). The light panel displays the current value of the Write Pointer and the Read Pointer and the Full/Empty status of the selected buffer.

A press of the Reset button resets the information stored in the Test Box and turns the Reset light on. The next time information is transferred to the Test Box the Reset light is turned off, telling the operator that the Test Box is updated.

On the Test Box the output signal on position 60 pin 3 is very helpful as a trigger signal to the oscilloscope, because the output is only logical zero for the channel selected by the switches on the Test Box.

MVP

28.9.75



AMT 701 A 11319	AMT 701 Asynchronous Multiplexer Testbox	BLAD 5

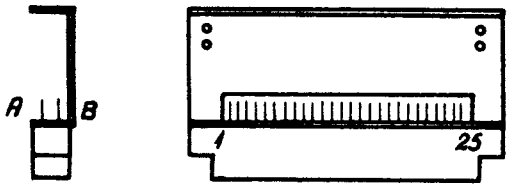
Test Plugs for the AMX 701/AMX 702

Two Test Plugs are delivered with the AMX 701/AMX 702

The Test Plugs are:

1. Test Plug No. 1 or CBL 241
2. Test Plug No. 2 or CBL 242

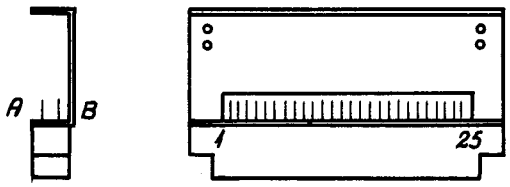
The use of the Test Plugs is described in the Test Program.



1 Edge connector 2 x 25 pol.

TRANS DATA	0	A 1	o	B 1	COMMON	
REC DATA	0	A 2	o	B 2	COMMON	
REQ to S.	0	A 3	o——	B 3	READY f. S.	0
DATA S. R.	0	A 4	o	B 4	CARRIER	0
DATA T. R.	0	A 5	o	B 5	CALL. IND.	0
POWER ON	0	A 6	o	B 6	COMMON	
TRANS DATA	1	A 7	o	B 7	COMMON	
REC DATA	1	A 8	o	B 8	COMMON	
REQ to S.	1	A 9	o——	B 9	READY f. S.	1
DATA S. R.	1	A10	o	B10	CARRIER	1
DATA T. R.	1	A11	o	B11	CALL. IND.	1
POWER ON	1	A12	o	B12	COMMON	
TRANS DATA	2	A13	o	B13	COMMON	
REC DATA	2	A14	o	B14	COMMON	
REQ to S.	2	A15	o——	B15	READY f. S.	2
DATA S. R.	2	A16	o	B16	CARRIER	2
DATA T. R.	2	A17	o	B17	CALL. IND.	2
POWER ON	2	A18	o	B18	COMMON	
TRANS DATA	3	A19	o	B19	COMMON	
REC DATA	3	A20	o	B20	COMMON	
REQ to S.	3	A21	o——	B21	READY f. S.	3
DATA S. R.	3	A22	o	B22	CARRIER	3
DATA T. R.	3	A23	o	B23	CALL. IND.	3
POWER ON	3	A24	o	B24	COMMON	
		A25	o	B25		

Text on the Edge connector:
Testplug No. 1 to AMX 701/AMX 702



1 Edge connector 2 x 25 pol.

TRANS DATA	0	A 1	o	o	B 1	COMMON
REC DATA	0	A 2	o	o	B 2	COMMON
REQ to S.	0	A 3	o	o	B 3	READY f. S. 0
DATA S. R.	0	A 4	o	o	B 4	CARRIER 0
DATA T. R.	0	A 5	o	o	B 5	CALL. IND. 0
POWER ON	0	A 6	o	o	B 6	COMMON
TRANS DATA	1	A 7	o	o	B 7	COMMON
REC DATA	1	A 8	o	o	B 8	COMMON
REQ to S.	1	A 9	o	o	B 9	READY f. S. 1
DATA S. R.	1	A10	o	o	B10	CARRIER 1
DATA T. R.	1	A11	o	o	B11	CALL. IND. 1
POWER ON	1	A12	o	o	B12	COMMON
TRANS DATA	2	A13	o	o	B13	COMMON
REC DATA	2	A14	o	o	B14	COMMON
REQ to S.	2	A15	o	o	B15	READY f. S. 2
DATA S. R.	2	A16	o	o	B16	CARRIER 2
DATA T. R.	2	A17	o	o	B17	CALL. IND. 2
POWER ON	2	A18	o	o	B18	COMMON
TRANS DATA	3	A19	o	o	B19	COMMON
REC DATA	3	A20	o	o	B20	COMMON
REQ to S.	3	A21	o	o	B21	READY f. S. 3
DATA S. R.	3	A22	o	o	B22	CARRIER 3
DATA T. R.	3	A23	o	o	B23	CALL. IND. 3
POWER ON	3	A24	o	o	B24	COMMON
		A25	o	o	B25	

Text on the Edge connector:
Testplug No. 2 to AMX 701/AMX 702

1:2591

MOJ

AMX702:

Pos 62: ROM034

RESISTORS:

R14,R16 (330E) and

R15,R17 (390E) are

2% 0,4W Metalfilm

All other resistors

5% 1/8W Carbonresistors

Switches beside pos 92:

(S1 to S3)

AMX Device Code Selection

(Red Dot = logic Zero)

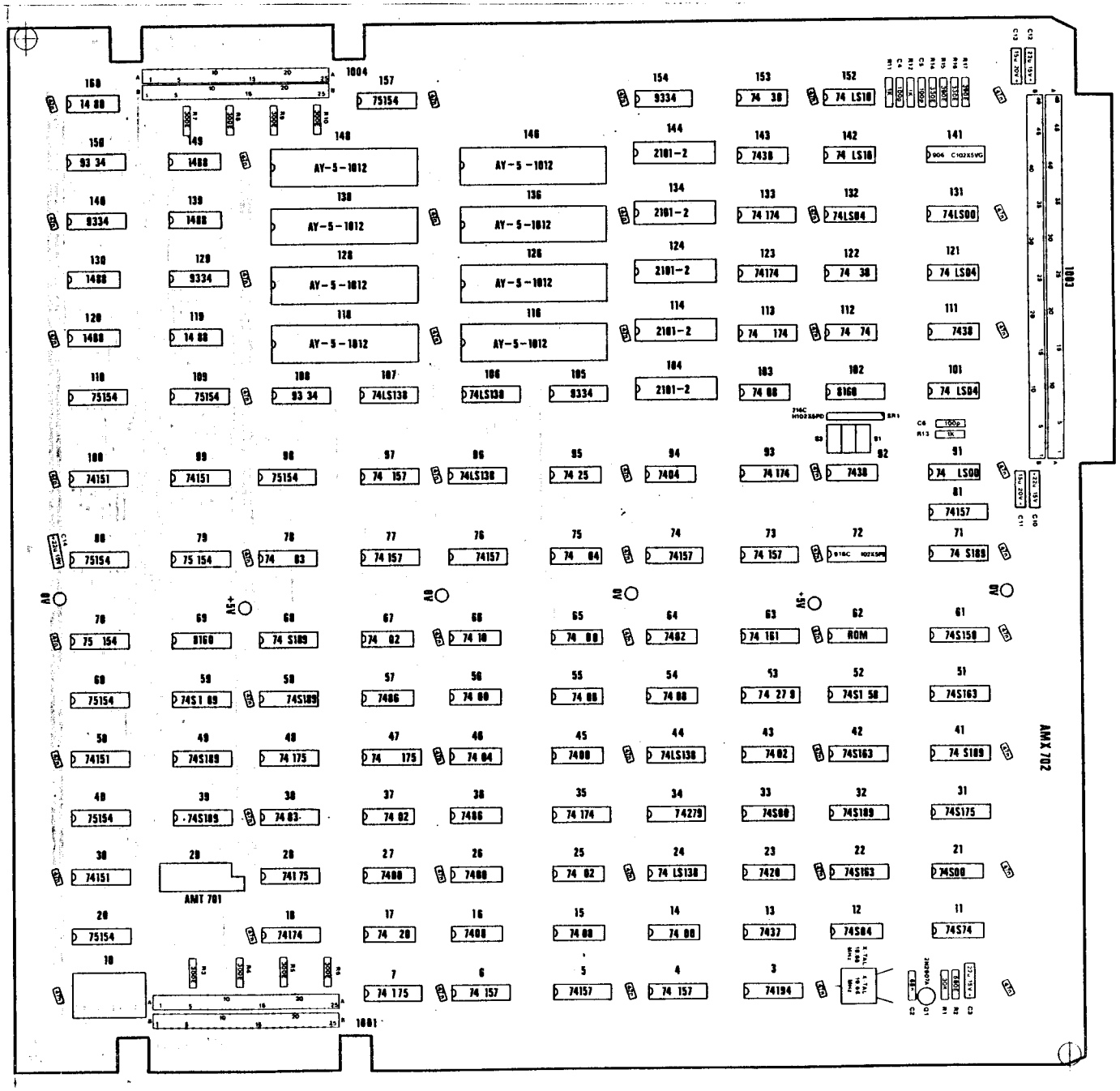
Pos 29:

Plug for Testbox AMT701

Pos 10:

Spare

77.08.16.



PCB ASSEMBLY DRAWING RC 2330

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Do you find errors in this manual? If so, specify by page.

How can this manual be improved?

Other comments?

Name: _____ Title: _____

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Thank you

42-i 1288

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