Title:

FPA 705
Front End Processor Adapter
Reference Manual

A/S REGNECENTRALEN

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Abstract:

This paper describes the logical structure of FPA 705.

(35 pages)

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CONTENTS Section

MAIN CHARACTERISTICS 1

Short Description. 1.1

The FPA 705 is an asynchronous controller intended for use as interconnecting media between the RC 3600 computer and RC 3600, RC 3500, or RC 8000 computers.

FPA 705 contains two subdevices, called the TRANSMITTER and the RECEIVER. Refer to fig. 1.1. Basicly it is two separate controllers each with its own control logic, so transmission can take place in both directions simultaneously.

The two devices are controlled by the normal I/O instructions, but data-transport takes place through the data channel.

The transmission is more than 600K bytes/sec.

Communication with RC 3600. 1.2

Communication with the RC 3600 CPU takes place via the standard I/O bus. Operations are initiated in both the TRANSMITTER and the RECEIVER by using the normal I/O instructions.

Normally, the TRANSMITTER part of FPA 705 is used to transmit a data block to the remote controller, and to receive a single status byte as a response to the transmitted block.

The RECEIVER part of FPA 705 is used to receive a data block from the remote controller, and to transmit a single status byte as a response to the received data block.

Both the TRANSMITTER and the RECEIVER are connected to the Data Channel, so data transfer takes place directly between the FPA 705 and the core memory in RC 3600.

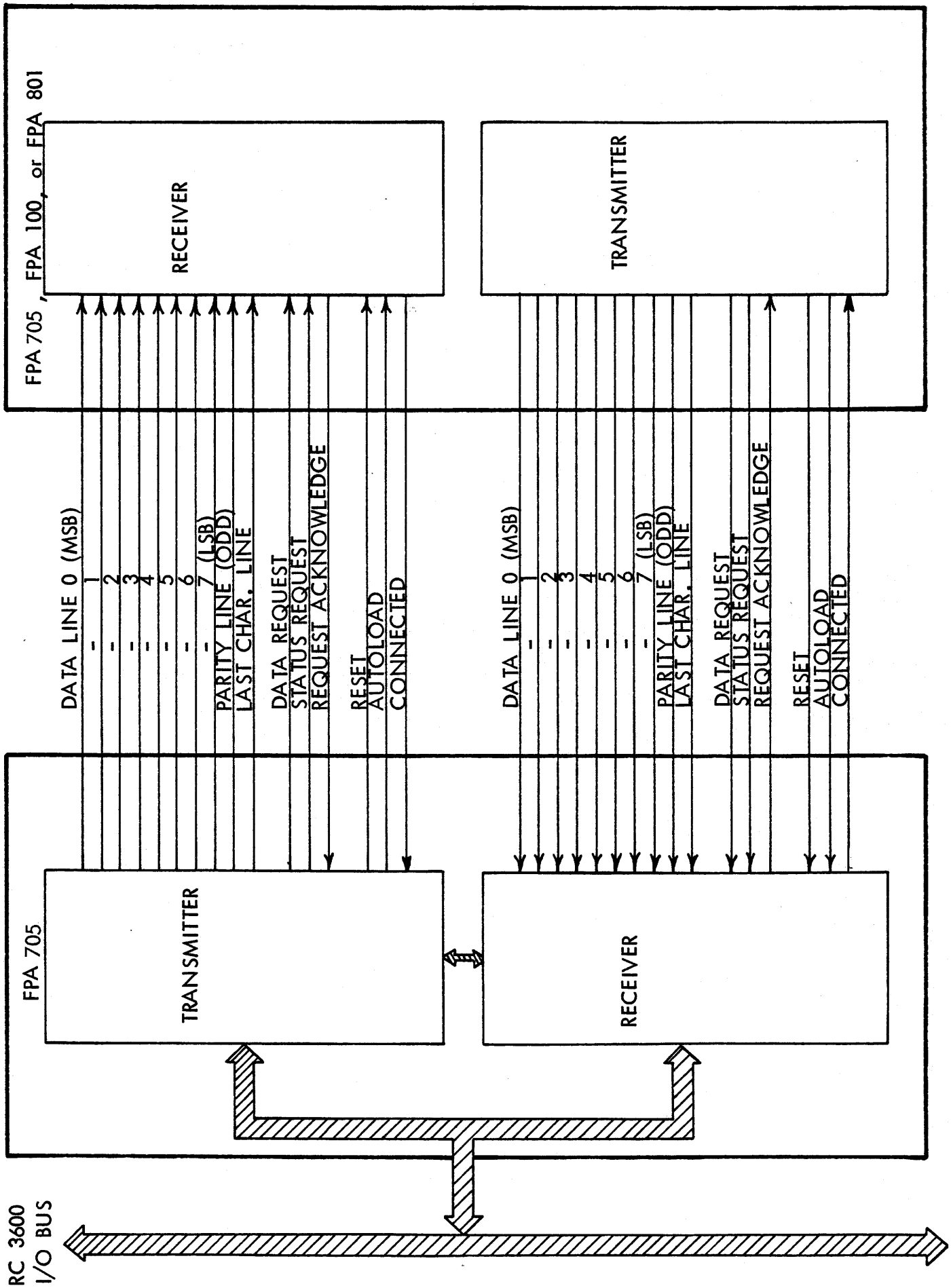


Fig. 1.1. FPA 705 Outline

The communication with the Remote Controller takes place via a set of output and a set of input lines. The output lines and input lines are completely symmetrical, each set consisting of:

9 Data lines, incl. a parity line, and
7 Control lines.

For further specification of the lines refer to section 4.

Included in the control lines is an autoload request line, which is necessary to be able to initiate an autoload procedure.

The communication is asynchronous on a byte by byte manner. Each byte consists of 9 bits: 8 databits + 1 parity bit (ODD parity).

The timing of the byte transfers are under control of two types of request signals and one request acknowledge signal.

The request signals are named:

DATA REQUEST and STATUS REQUEST.

The Data Request is used as a request signal when the Transmitter sends data to the remote controller, and the Status Request is used when the Receiver transmits status to the remote end.

The communication with the remote controller utilizes the asynchronous, fully interlocked technique. Each request signal from FPA 705 must be acknowledged to complete the transfer.

When FPA 705 wants to transmit a byte, the byte is placed on the data lines, and the data request signal is set. When the remote controller has stored the byte, it responds to the request by setting the request acknowledge signal, indicating the reception of the byte. Upon the reception of the acknowledge signal, FPA 705 lowers the request signal, which also causes the remote end to lower the acknowledge signal.

At FPA 705

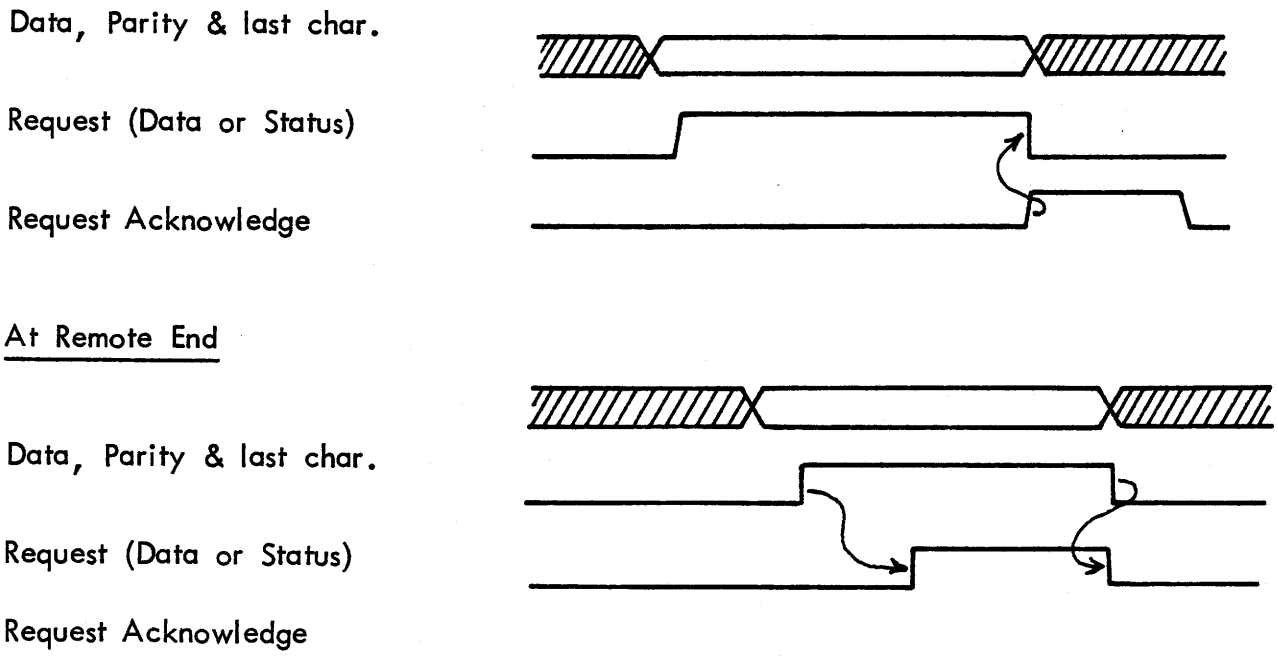


Fig. 1.2. Timing

Simultaneously with transmission of the last byte in a block, the LAST CHAR signal is sent.

Also provided in the control lines is a RESET signal, which notifies the receiver when the transmitter is reset.

The transmission can take place in both directions simultaneously. But if the receiver wants to transmit a STATUS Byte while the transmitter is in progress with transmitting a data block, the STATUS byte is not transmitted, before the transmitter has finished the previous data block, i.e. STATUS bytes are transmitted between data blocks.

Byte Format. 2.1

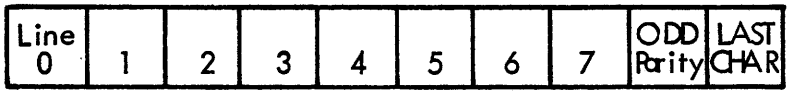


Fig. 2.1. Byte Format

Every byte consists of 10 bits, 8 data bits, one parity bit, and one bit indicating last byte. The parity bit is selected so the 8 databits + the parity bit have ODD parity.

Data Line 7 is the least significant bit of the data byte.

Block Format. 2.2

Fig. 2.2. Block Format

When transmitting, the first byte, the START BYTE, is not taken from the core memory, but from a START BYTE register loaded by I/O instructions.

When receiving, the first byte, the START BYTE, is not stored into core memory but loaded into a status register.

The last data byte differs from the data bytes upon the signal LAST CHAR.

Receiver. 3.1

Program control of the receiver is provided through all I/O transfer instructions. Busy and Done are controlled or sensed in I/O instructions with device code B, changeable by hardware straps in the controller; B is always an even number. Interrupt disable is controlled by interrupt priority mask bit 3.

The clear function (F = 10) clears Busy and Done. Start (F = 01) clears Done, sets Busy, and the operation indicated by the contents of the command register is executed.

The Pulse function (F = 11) is not used.

The receiver terminates all program initiated commands by clearing Busy and setting Done, causing an interrupt if Interrupt Disable is clear.

The IORST instruction clears the BUSY and Done flags together with all registers except the Byte Counter, which is preset to a negative value.

SET ADDRESS COUNTER Instruction. 3.1.1

The DOA AC, REC instruction (see fig. 3.1 and 3.1.1) loads the address counter with the contents of AC - i.e. the 15 bits address for the location in the core memory where the first two received characters are to be stored (except the START BYTE).

DOA Instruction

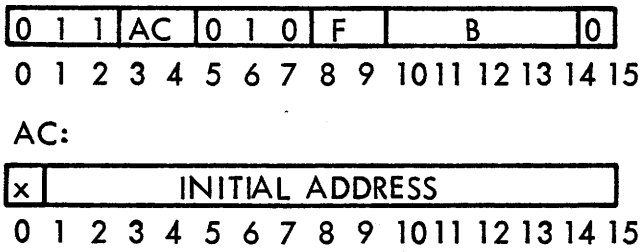


Fig. 3.1.1. DOA-Instruction (x = not used)

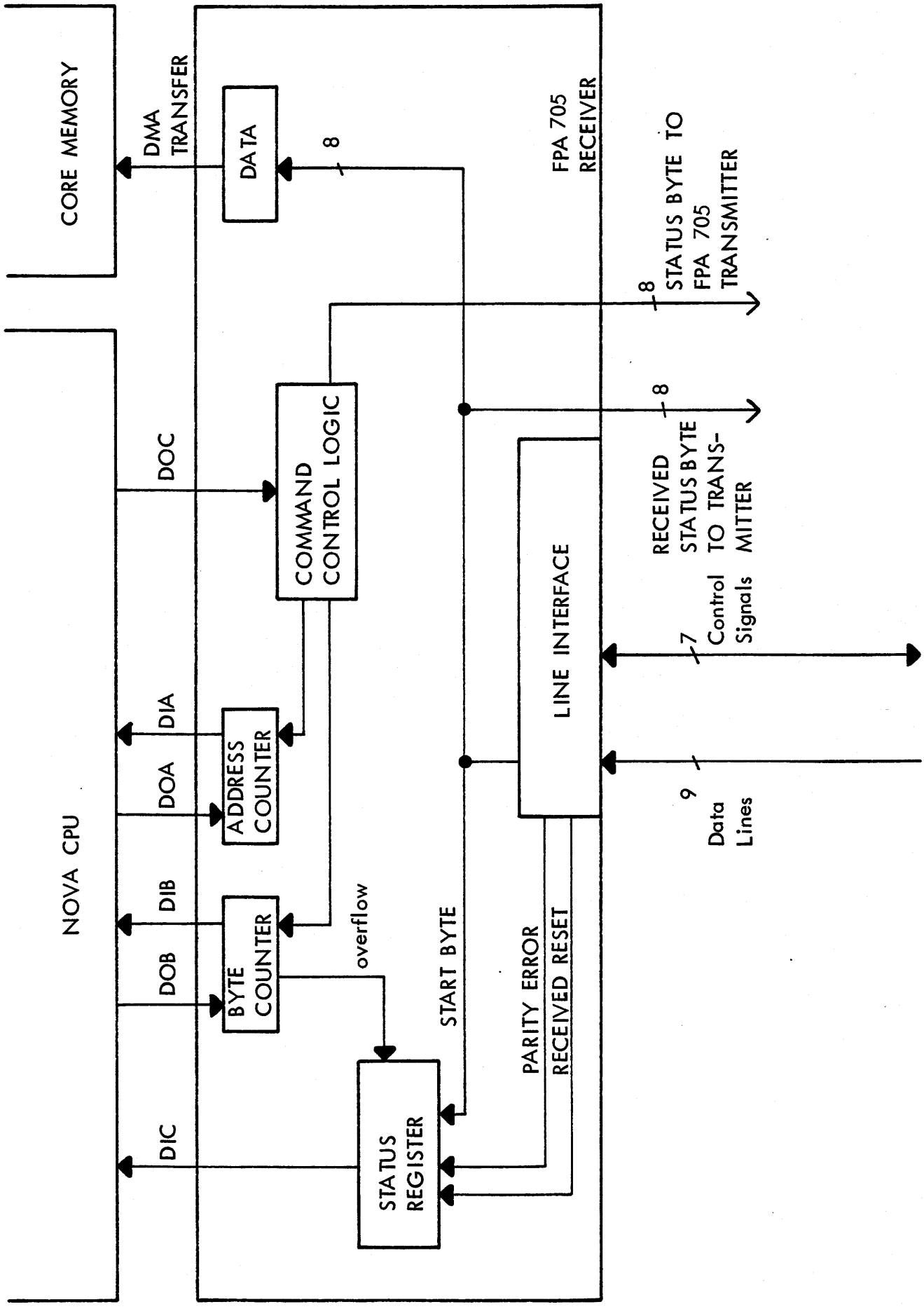


Fig. 3.1. FPA 705 Receiver Survey Diagram

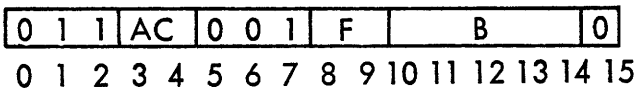
When the reception begins, the address counter is incremented by one every time two characters are stored as a word in the core memory.

In this way the contents of the address counter are one greater than the address of the previous stored word if termination occurs.

READ ADDRESS COUNTER Instruction. 3.1.2

The DIA AC, REC instruction (see fig. 3.1 and 3.1.2) loads the contents of the address counter into the specified AC.

DIA Instruction



AC:

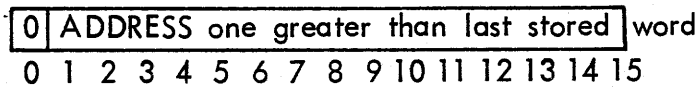


Fig. 3.1.2. DIA Instruction.

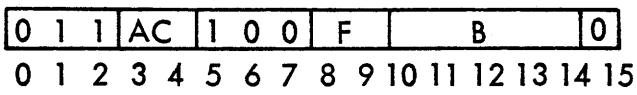
After the instruction has been executed, the selected AC contains the contents of the address counter.

The DIA instruction will not alter the contents of the address counter.

SET BYTE COUNTER Instruction. 3.1.3

The DOB AC, REC instruction (see fig. 3.1 and 3.1.3) loads the byte counter with the contents of AC - i.e. the 16 bit negative byte count (two's complement). The byte count value should be even.

DOB Instruction



AC:

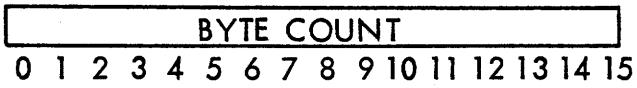
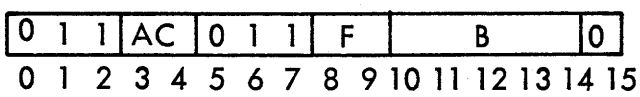


Fig. 3.1.3. DOB Instruction.

READ BYTE COUNTER Instruction. 3.1.4

The DIB AC, REC instruction (see fig. 3.1 and 3.1.4) loads the contents of the Byte Counter into the specified AC.

DIB Instruction



AC:

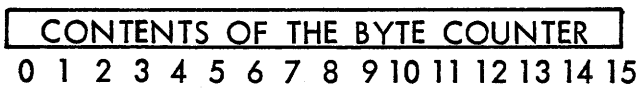
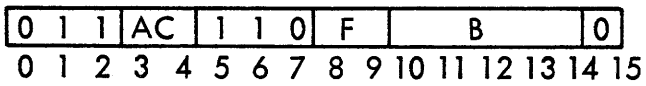


Fig. 3.1.4. DIB Instruction.

SET COMMAND Instruction. 3.1.5

The DOC AC, REC instruction (see fig. 3.1 and 3.1.5) loads the contents of the specified AC into the Command register and the Status Byte register.

DOC Instruction



AC:

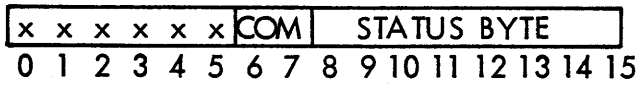


Fig. 3.1.5. DOC Instruction (x = not used).

The command field, bits (6 : 7), specifies the command to be executed.

The possible commands are listed below:

Command Code	Mnemonic
3	NO OPERATION
2	READ BLOCK
1	TRANSMIT STATUS
0	TRANSMIT - RECEIVE

The program starts an operation by executing an I/O instruction with modification S (F = 01, sets Busy and clears Done), and the actual contents of the command register then specifies the type of operation to be executed.

If the start instruction is a DOC S, then the command register is loaded before the operation is executed.

READ BLOCK Command. 3.1.5.1

Receives a datablock and transfers it to the core memory from the address specified by the Set Address Counter and forward.

The datablock is received asynchronously on a byte by byte basis.

The first byte in the datablock is not transferred to the memory, but loaded into a Received START BYTE Register, from which it can be sensed by a Read Status instruction (see section 3.1.6).

Whenever a byte is received a count takes place in the Byte Counter (BYTE COUNT:= BYTE COUNT + 1), except after the first byte in the datablock, the START BYTE.

The received bytes are transferred to the memory on a word by word basis.

The last word will contain one or two bytes depending upon the block length of the received datablock.

The READ BLOCK Command is terminated (by clearing BUSY, setting DONE and causing an interrupt if Interrupt Disable is clear), when the last byte is received and transferred to memory.

If one of the error situations, Parity Error or byte count overflow occurs, the command is not immediately terminated; but the status flags are updated.

If byte count overflow occurs before last byte is received, the status bit OVERFLOW (bit 0) is set, but the command is not terminated before last byte is found.
If a byte is received with parity error, the status bit PARITY ERROR (bit 2) is set, but the command is not terminated before last byte is found.

If a RESET signal is received from the remote transmitter, the command in progress is terminated immediately. This situation is indicated by setting the status bit RECEIVED RESET (bit 3).

TRANSMIT STATUS Command. 3.1.5.2

This command causes the contents of the STATUS BYTE register to be transmitted to the remote computer's Transmitter.

The TRANSMIT STATUS Command is terminated when an acknowledge for the STATUS byte is received from the remote computer, or a RESET occurs as mentioned in section 3.1.5.1.

TRANSMIT - RECEIVE. 3.1.5.3

This command is a combination of the TRANSMIT STATUS Command and the READ BLOCK Command.

First is the contents of the STATUS Byte register transmitted (section 3.1.5.2), then the receiver executes the READ BLOCK Command. There is no termination-interrupt when shifting from Transmit Status to Read Block. The receiver stays busy during the whole operation.

The termination is as described in section 3.1.5.1.

NO OPERATION. 3.1.5.4

The receiver never terminates this command. When initiated by means of the I/O Start function, this command places the receiver in the busy state, and nothing else happens. This command must be terminated by means of the I/O Clear function (or IORST).

READ STATUS Command. 3.1.6

The DIC AC, REC instruction (see fig. 3.1 and 3.1.6) transfers the current state of the receiver into the specified AC. In addition it clears the status register bit 0 : 7.

DIC Instruction

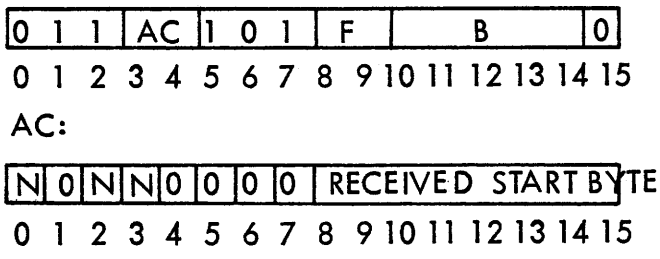


Fig. 3.1.6. DIC Instruction (N = status bit).

The status bits are listed in fig. 3.1.7.

The status bits are flag signals, and the mnemonics refer to the active onestate.

In the following the meaning of each status bit is explained in detail.

Updating of the status register is performed automatically by the receiver.

Bit No.	Mnemonic
0	OVERFLOW
1	0
2	PARITY ERROR
3	RECEIVED RESET
4	0
5	0
6	0
7	0
8	
9	
10	
11	RECEIVED
12	START BYTE
13	
14	
15	

Fig. 3.1.7. Status bit allocation.

OVERFLOW. 3.1.6.1

Indicates Overflow from the Byte Counter.

RECEIVED RESET. 3.1.6.2

Indicates that a RESET signal has been received from the remote transmitter.

PARITY ERROR. 3.1.6.3

Indicates that a character with parity error has been received.

START BYTE. 3.1.6.4

The first character in a received data block is not loaded into core memory, but available to the programmer as status bit 8 : 15.

RECEIVED AUTOLOAD. 3.1.7

This AUTOLOAD signal is a pulse-signal received from the remote transmitter.

This signal is used in the receiver logic to generate an autoload sequence to the CPU, i.e. an RST (Reset) pulse followed by a PL (Program Load) pulse. By a switch on the front panel of FPA 702 this function can be disabled.

Transmitter. 3.2

Program control of the transmitter is provided through all I/O transfer instructions. Busy and Done are controlled or sensed in I/O instructions with device code B + 1, where B is the device code for the receiver (see section 3.1).

Interrupt disable is controlled by interrupt priority mask bit 3.

The clear function (F = 10) clears Busy and Done. Start (F = 01) clears Done, sets Busy, and the operation indicated by the contents of the command register is executed.

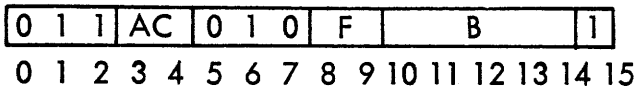
The Transmitter terminates all program initiated commands by clearing Busy and setting Done causing an interrupt, if Interrupt Disable is clear.

The IORST instruction clears the BUSY and DONE flags together with all registers in the Transmitter, and causes a RESET pulse to be sent to the Remote Receiver.

SET ADDRESS COUNTER Instruction. 3.2.1

The DOA AC, XMT instruction (see fig. 3.2 and 3.2.1) loads the address counter with the contents of AC - i.e. the 15 bit address pointing at the location of the first two bytes that are to be transmitted after the START BYTE.

DOA Instruction



AC:

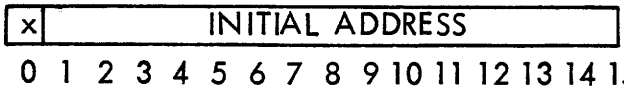


Fig. 3.2.1. DOA Instruction (x = not used).

When the transmission begins, the address counter is incremented by one every time two bytes are transferred from the core memory to the transmitter register.

In this way, the contents of the address counter is one greater than the address of the last transferred byte, if termination occurs.

READ ADDRESS COUNTER Instruction. 3.2.2

The DIA AC, XMT instruction (see fig. 3.2 and 3.2.2) loads the contents of the address counter into the specified AC.

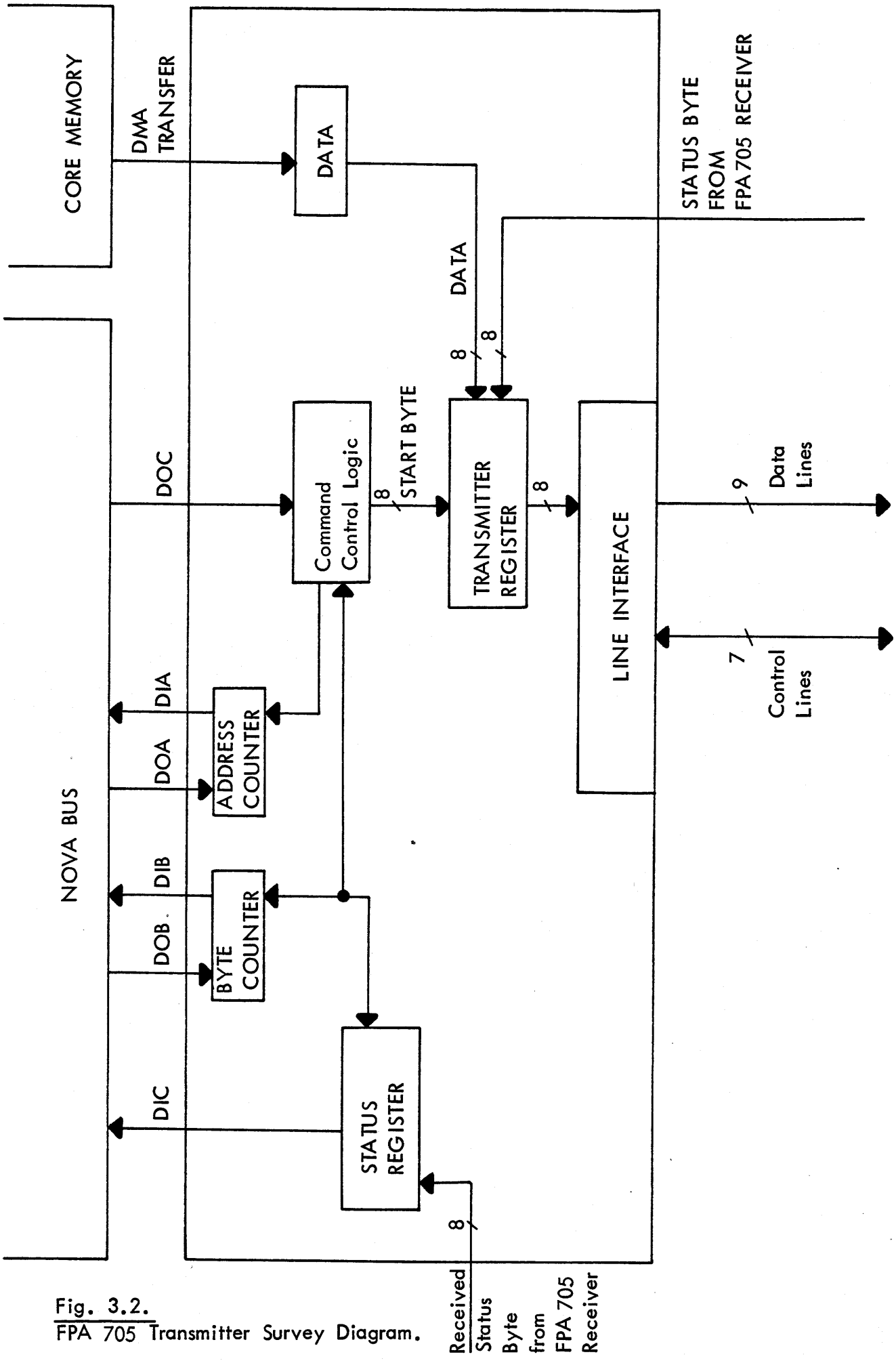
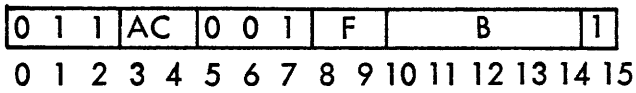


Fig. 3.2.
FPA 705 Transmitter Survey Diagram.

DIA Instruction



AC:

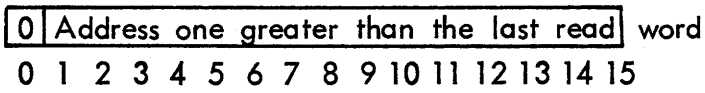


Fig. 3.2.2. DIA Instruction.

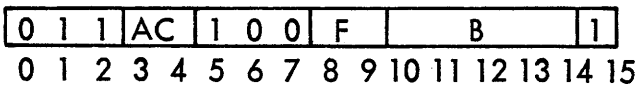
After the instruction has been executed, the selected AC contains the contents of the address counter.

The DIA instruction will not alter the contents of the address counter.

SET BYTE COUNTER Instruction. 3.2.3

The DOB AC, XMT instruction (see fig. 3.2 and 3.2.3) loads the byte counter with the contents of AC - i.e. the 16 bit negative byte count (two's complement).

DOB Instruction



AC:

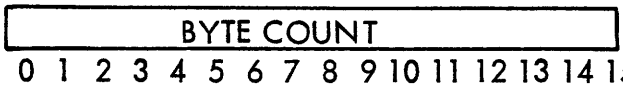
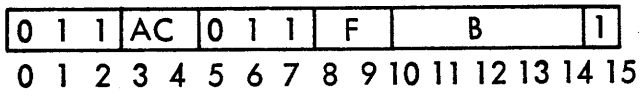


Fig. 3.2.3. DOB Instruction.

READ BYTE COUNTER Instruction. 3.2.4

The DIB AC, XMT instruction (see fig. 3.2 and 3.2.4) loads the contents of the Byte Counter into the specified AC.

DIB Instruction



AC:

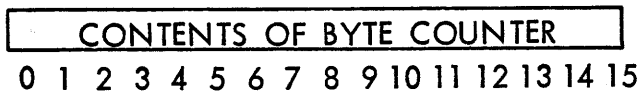
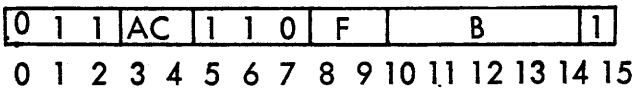


Fig. 3.2.4. DIB Instruction.

SET COMMAND Instruction. 3.2.5

The DOC AC, XMT instruction (see fig. 3.2 and 3.2.5) loads the contents of the specified AC into the Command register and the START BYTE register.

DOC Instruction



AC:

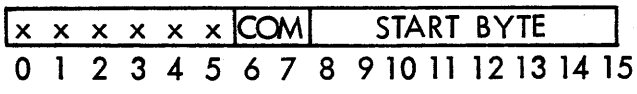


Fig. 3.2.5. DOC Instruction (x = not used).

The command field, bits (6 : 7), specifies the command to be executed.

The possible commands are listed below:

Command Code	Mnemonic
0	TRANSMIT - RECEIVE
1	RECEIVE STATUS
2	TRANSMIT BLOCK
3	NO OPERATION

The program starts an operation by executing an I/O instruction with modification S (F = 01, sets Busy and clears Done), and the actual contents of the command register specifies the type of operation to be executed.

If the start instruction is a DOC S, then the command register is loaded before the operation is executed.

TRANSMIT BLOCK Command. 3.2.5.1

The datablock specified by the START ADDRESS (section 3.2.1) and Byte COUNT (section 3.2.3) is transmitted byte by byte in an asynchronous manner, i.e. the next byte is not transmitted before an acknowledge is received for the preceding byte.

The first transmitted byte is not taken from memory, but from the START BYTE register (section 3.2.5).

Every transmitted byte consists of 8 data bits and one parity bit (ODD parity); the parity bit is generated by hardware in the FPA 705 transmitter.

The transmission continues until the byte counter overflows, or an error situation occurs.

Overflow from the Byte Counter indicates that the next byte to be transmitted is the last byte in the datablock. Together with this byte is the signal LAST CHAR sent to the remote receiver.

When the last byte is acknowledged, the TRANSMIT BLOCK command is terminated by clearing BUSY, setting DONE and causing an interrupt, if Interrupt Disable is clear.

If during transmission an acknowledge for the transmitted byte is not received within 1 ms., the command is terminated as mentioned above. This situation is indicated by setting status bit TIME OUT (bit 1).

If the signal CONNECTED from the remote receiver is false before the TRANSMIT BLOCK command starts, or the signal goes false during transmission, the command is terminated as mentioned above. This situation is indicated by the status bit DISCONNECTED (bit 0).

RECEIVE STATUS Command. 3.2.5.2

The transmitter waits for a STATUS BYTE from the remote receiver. When this STATUS BYTE is received, the RECEIVE STATUS Command is terminated. The received STATUS BYTE is loaded into the Status Byte register, where it can be sensed by a Read Status Command (section 3.2.6).

If a STATUS BYTE is received when the transmitter is not in the RECEIVE STATUS mode, this STATUS BYTE is ignored.

TRANSMIT - RECEIVE Command. 3.2.5.3

This command is a combination of the TRANSMIT BLOCK command and the RECEIVE STATUS command. First is a datablock transmitted as mentioned in section 3.2.5.1, then the transmitter shifts to RECEIVE STATUS mode. The command is terminated as mentioned in section 3.2.5.2. There is no termination interrupt when shifting from TRANSMIT BLOCK mode to RECEIVE STATUS mode. The transmitter stays busy during the whole operation.

If the error situations mentioned in section 3.2.5.1 (Time Out and Disconnected) occur in TRANSMIT BLOCK mode, the command is terminated as mentioned in section 3.2.5.1.

NO OPERATION. 3.5.2.4

The transmitter never terminates this command. When initiated by means of the I/O Start function, this command places the transmitter in the busy state, and nothing else happens.

This command must be terminated by means of the I/O Clear function (or IORST).

AUTOLOAD or RESET Command. 3.2.5.5

The DOC AC, XMT instruction (see fig. 3.2.5.5) together with the I/O function pulse (F = 11) initiates an AUTOLOAD or a RESET pulse to the remote receiver.

DOC Instruction

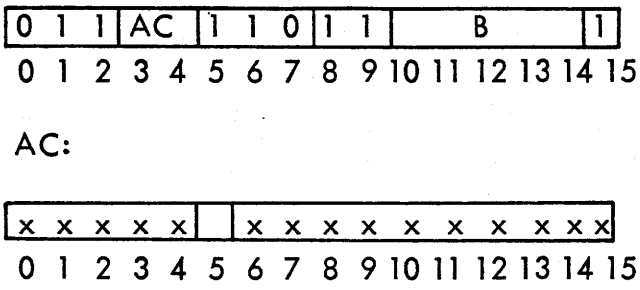


Fig. 3.2.5.5. DOC P-Instruction (x = not used).

Bit 5 in the AC specifies the command to be executed.

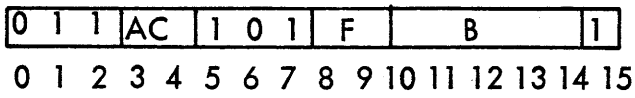
If bit 5 = 1, an AUTOLOAD pulse is sent to the remote receiver.

If bit 5 = 0, a RESET pulse is sent to the remote receiver.

The duration of the AUTOLOAD or RESET pulse is about 10 uS.

The DIC AC, XMT instruction (see fig. 3.2. and 3.2.6) transfers the current state of the transmitter into the specified AC. In addition it clears the status register bit 0 : 7.

DIC Instruction



AC:

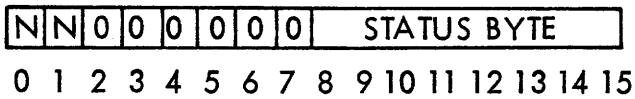


Fig. 3.2.6. DIC Instruction (N = status bit).

The status bits are listed in fig. 3.2.7.

The status bits are flag signals, and the mnemonics refer to the active onestate.

In the following, the meaning of each status bit is explained in detail.

Updating of the status register is performed automatically by the transmitter.

Bit No.	Mnemonic
0	DISCONNECT
1	TIME OUT
2	0
3	0
4	0
5	0
6	0
7	0
8	RECEIVED STATUS BYTE
9	
10	
11	
12	
13	
14	
15	

Fig. 3.2.7. Status Bit Allocation

DISCONNECT. 3.2.6.1

Indicates that the Connected Line from the remote receiver is or has been false.

TIME OUT. 3.2.6.2

Indicates during transmission of a datablock that acknowledge for the transmitted byte is not received within 1 ms.

STATUS BYTE. 3.2.6.3

The STATUS BYTE received in the Receive Status mode is available to the programmer as status bit 8 : 15.

Timing (Refer to Fig. 4.1). 4.1

As mentioned in section 1 "Main Characteristics", the communication with the front-end utilizes the handshake technique.

Note that the transmitting unit is allowed to rise the request signal, even if the request acknowledge signal is not lowered, which means that it is the rise of the leading edge of the request acknowledge that indicates the reception of the character.

This is done to speed up the transmission, since the transmitting unit does not need to wait for the propagation of the high to low transition of the acknowledge signal.

Upon the reception of the low to high transition of the request acknowledge signal the transmitting unit must lower the request signal. The request signal must be low for at least 100 ns.

The pulse width of request acknowledge must not be less than 30 ns.; however, the signal must not be lowered until the request signal has been lowered. The pulse width of request acknowledge depends on cable delay, driver/receiver propagation delays, and propagation delays in circuits, which utilizes the acknowledge signal. When using FPA 705 interface circuits and principle, the width of request acknowledge, measured at the output of the line driver, will not be less than 30 ns.

When measured at the outputs of line drivers, data must lead request with at least 20 ns., the same specification is valid for the last character signal. Data must not change as long as the request signal is true.

To compensate for max. cable and receiver skew, the receiving unit must delay the request signal at least 100 ns. before the character is stored.

The pulse width of RESET and AUTOLOAD signals shall be at least 300 ns.

The following line drivers and receivers are recommended:

Drivers:

TEXAS	:	SN 75183
NATIONAL	:	DM 8830
FAIRCHILD	:	9612E

Receivers:

TEXAS	:	SN 75182
NATIONAL	:	DM 8820A
FAIRCHILD	:	9613

The line drivers provide differential output signals, and are used to drive a twisted pair line with an impedance of app. 120Ω . The drivers are single supplied and use only + 5V.

SN 75183 and DM 8830 are compatible and include gates, which are useful when it is necessary to gate the signals; therefore this type of driver is used for the control signals.

9612E is used for the data, parity, and last character signals since these signals need no gating.

The line receivers are designed to sense small differential signals in the presence of large common-mode noise; up to $\pm$ 15V. common mode input voltage can be tolerated. The receivers are single supplied and use only + 5V.

SN 75182 and DM 8820A are compatible and include strobe and terminating resistor (170Ω). The strobe input is used to strobe all of the control signal receivers with the disconnected signal from the opposite end. This assures that the output of the control signal receivers is always logical 0, if the opposite computer is disconnected (power off or no cable installed etc.).

9613 is used as receiver for the data parity and last character signals, since these signals need no gating. No terminating resistor is included in the 9613.

Cable Characteristics. 4.3

The cable to be used should have the following characteristics:

Type: Shielded cable,
min. 16 pairs of twisted wires 0.25 mm^2.

Impedance: App. 120Ω .

Max. length: 20 m.

The shield of the cable must be connected to the common zero voltage. Refer to fig. 4.2. The cable should only be terminated in the receiving unit.

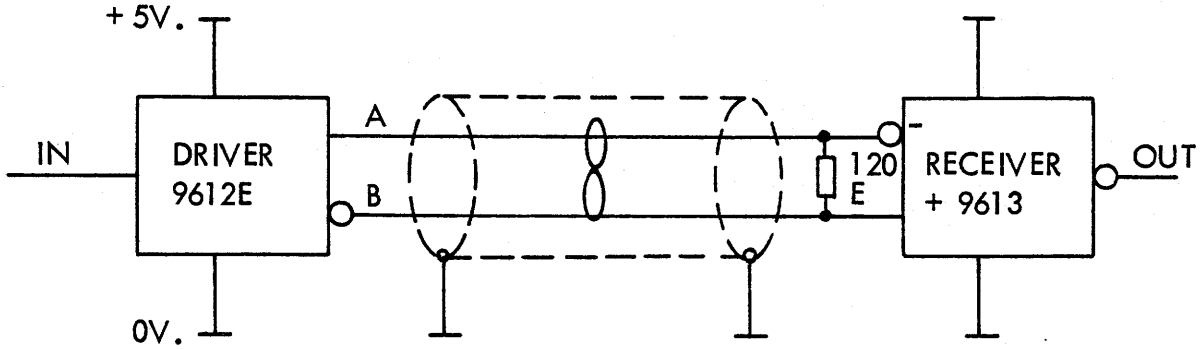


Fig. 4.2.

When a logical 1 exists on the line, A shall be positive in relation to B.

Signal Description. 4.4

DATA LINES 0 : 7 : Data line 0 is the most significant bit, and data line 7 the least significant bit.

PARITY LINE : This line is the parity line making the parity odd.

LAST CHAR LINE : When logical 1, this line indicates the end of the block. The LAST CHAR signal is generated simultaneously with the emission of the last character in the block and the STATUS BYTE.

DATA REQUEST LINE : This signal when logical 1 indicates to the receiving unit that a data character is ready on the data lines 0 : 7. The signal is generated by the transmitter in the transmitting unit.

STATUS REQUEST LINE : This signal when logical 1 indicates to the receiving unit that a status character is ready on the data lines 0 : 7. The signal is generated by the receiver in the transmitting unit.

REQUEST ACKNOWLEDGE LINE : When this signal changes from false to true state, it indicates to the transmitting unit that the character on the data lines has been stored in the receiving unit. Upon the reception of the rising edge of the acknowledge signal the transmitting unit is allowed to fetch the next character and place it on the data lines.

RESET LINE : This line when logical 1 indicates to the receiver in the receiving unit that the transmitter in the transmitting unit has been reset.

CONNECTED LINE : This line when logical 1 indicates to the receiving unit that power is on. The connected signal is used to strobe the following control signals:

RESET
REQUEST ACK
DATA REQUEST
STATUS REQUEST
AUTO LOAD

This assures that the output of these receivers is at logical 0 when power in the transmitting unit is turned off.

AUTOLOAD LINE : This line is necessary to be able to initiate an autoload procedure in the front end computer under RC 8000 program control.

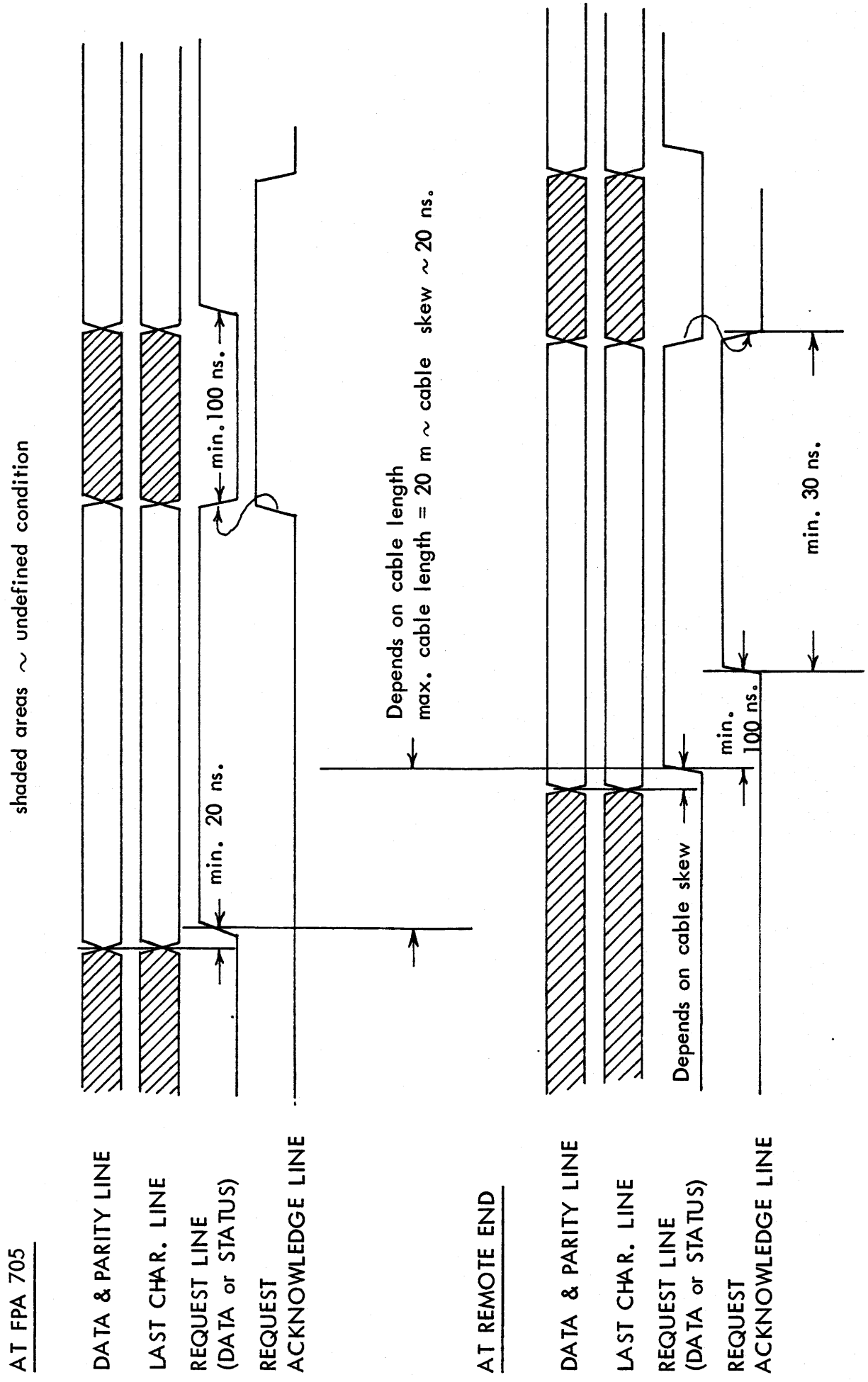


Fig. 4.1. Line Characteristics - Timing.

OPERATOR CONTROLS 5

Switches. 5.1

The only operator control is the DISABLE AUTO switch.

When this switch is in the ON-state, nothing happens, when an AUTO-LOAD pulse is received from the remote computer.

When this switch is in the OFF-state, a received AUTOLOAD pulse causes an AUTOLOAD sequence to be generated to the CPU.

Indicators. 5.2

The only indicator is an AUTO indicator; lighting from an AUTOLOAD pulse is received until the program loader is started (an IORST is received).

The AUTO indicator will not light when the DISABLE AUTO switch is in the ON-state.

MISCELLANEOUS INFORMATION 6

Technical Specification. 6.1

The FPA 705 Front Processor Adapter is designed for use in RC modular system CHS 701.

Only + 5V power supply is used.

Power consumption:

From the + 5V bus: 5.0 A.