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RC850 - TOTEM - Test System
User's Guide, Part 2

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Keywords:

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Abstract:

This manual describes further test programs for the RC850 terminal, which were not described in the first manual. These test programs are: the X.21 status signal test, the FDC-test, the FDD-test, the NVM-test and the flexible disk drive adjustment program.

(28 printed pages)

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1. INTRODUCTION 1.

This manual describes five test programs included in the RC850 test system, TOTEM, which were not described in the first manual.

The X.21 status test is an extension of the SIO-test, described in chapter 6 of the first manual.

The FDC-test is testing a few of the basic functions of the flexible disk controller without the need of any drive connected.

The FDD-test is testing the flexible diskette controller and up to four connected drives, either 8" or 5 1/4". It is not a complete test of the flexible disk, but rather a fast verification of the basic functions of the controller and drives.

The flexible disk adjustment program is a tool for the technician, which enables him to perform the three kinds of mechanical adjustments in question for the flexible diskette drives.

The NVM-test is testing the non volatile memory on the MIC board for data recovery.

Note: This test should normally not be used in the field, because it is destructive to the original configuration parameters in the non volatile memory.

2. SIO-TEST 2.

2.1 X.21 Status Test 2.1

The X.21 status test is an extension to the SIO-test described in chapter 6 of the first manual. It is testing the X.21 interface of the line connection.

The test is switching the selector on the COI board to X.21 SEL. When the RTS bit on the SIO is set and some data bytes are sent, the response of the SIO DTR bit on the CTS pin (I) is checked. It is also checked that the receiver character available bit of the SIO is set.

The response of the DCD pin (R) is checked as well.

The test cable to be used to test the X.21 signals as well as the V.24 signals is shown on fig. 1. If the test plug CBL998 is used the X.21 signals will not be checked.

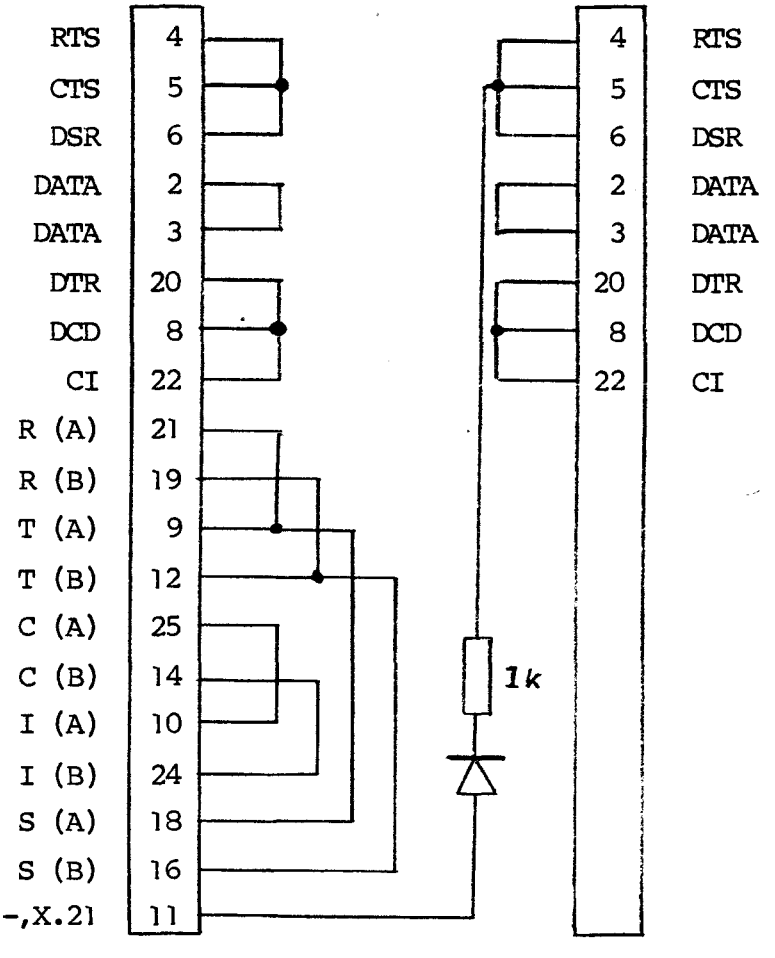

Figure 1: Line test cable for X.21 test (KBL508).

The X.21 status signals are the first which are tested as part of the SIO-test. If an error occurs it will end up with an error message and halt the execution if the halt bit is set to halt on error (see chapter 9 of the first manual). If not halted the execution will proceed with the SIO-test as described in chapter 6 of the first manual.

The possible error messages could be:

<X21 error, I*> : the CTS pin (I) has not responded correctly.

<X21 error, R*> : the DCD pin (R) has not responded correctly.

<X21 error, no data*> : data bytes cannot be transferred (no receiver character available after transmission).

2.2 COAX-Interface 2.2

When the terminal which is tested is equipped with a coax-interface instead of a circuit-interface, a test plug (KBL507) must be installed in the coax plug. This test plug is a delay line on a BNC-connector simulating approximate 30 meters of open circuit coax cable. This open circuit cable is reflecting the data stream with the right timing, so it can be correctly received.

3. FDC-TEST 3.

The FDC-test is a small test loop included in the big sequential loop of tests.

When the test is entered, it is checked that the main status register of the FDC has bit 7 set to indicate that the controller is ready.

After that, an invalid command is sent to the controller to see if it responds correctly.

The test is only run if a controller is installed. This is signalled to the program by setting the switches S1 through S4 to 55 hex.

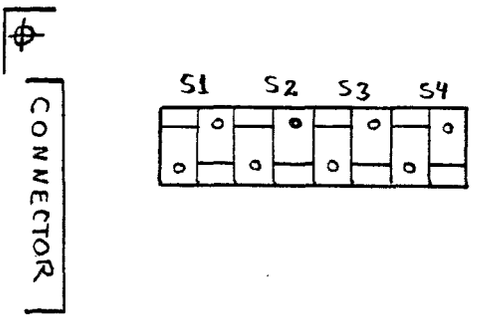

Figure 2: Switch setting for the FDC-controller.

The following three error messages could appear:

<not ready to receive or transmit>:
bit 7 of the main status register was not set when entering the test.

<the wrong data-direction in fdc>:
bit 6 of the main status register has wrong polarity.

<fault in status register>:
Status register 0 should indicate an invalid command (bit 7 = 1, bit 6 = 0).

4. FDD-TEST 4.

This test is testing the flexible disk controller and up to four connected drives, either 8" or 5 1/4". It is not a complete test of the flexible disk, but rather a fast verification of the basic functions of the controller and the drives connected to it.

The test is not included in the big sequential loop, but must be started by entering test No 9. If looping is not selected, the test will terminate by reentering the big sequential loop starting with the selftest.

The test will initialize the controller to a step rate time of maximum 10 ms., a head unload time of maximum 160 ms., and a head load time of maximum 40 ms.

When the testing is initiated the units which are ready, will be recalibrated. If no units are ready the text <* all drives: not ready> will be written, and the test enters an idle state. Whenever a unit changes its state from not ready to ready, the testing will start on this unit.

The testing sequence for a unit is first a recalibration and then the cyclic sequence, seek, write, read. Not the complete diskette is tested, but only the following 16 tracks are used for data recovery checkout:

For 8" units: 1, 76, 2, 75, 3, 74, 8, 40, 73, 9, 72, 36, 71, 37, 38, 39.

For 5 1/4" units: 1, 35, 2, 34, 3, 32, 8, 15, 31, 9, 30, 16, 29, 17, 25, 24.

The sector number varies from 1 throughout 9. On the first track the data checkout will be performed on sector 1, on the second track on sector 2 and so on.

For 8" diskette station connected to an RC850, it is recommendable only to use properly formatted diskettes of the type dual head, double side, soft sector, double density with the format 15 sectors/512 bytes.

The test pattern written on the diskette is a counting pattern of 512 bytes, which is transferred via the DMA-controller channel 1. When the data is read from the diskette, it is placed in a buffer in the memory, and the write- and read-buffers are compared.

When the test is in loop mode, each byte of the test buffer is incremented by one for each pass.

If an error is detected one of the following errortexts will be written.

4.1 FDD-Test Error Messages 4.1

<*fault in main status reg>

Indicates an error in the controller main status register bit 7 or 6.

<not ready>

Indicates that the ready state for a specified drive has been set to not ready (bit 3 of status register 0).

<write protected>

Indicates that the write protect bit has been set (bit 1 of status register 1).

<timeout>

The specified drive has not responded to an operation with an interrupt within approximate 2 s.

<*fault in fdc xx>

Indicates that the status bits of status register 0 are in an invalid state. xx is a hexadecimal number showing the contents of this register.

<seek error>

The drive could not find the specified track of the command issued (bit 5 of status register 0).

<command abort>

The command issued was invalid. The command was never started. It will appear if an earlier command was not terminated correctly (bit 7 = 1 and bit 6 = 0 of status register 0).

<door open>

The drive door has been opened during execution.

<recalibrate error>

The seek end bit did not occur after a recalibrate command (bit 5 of status register 0).

<track 0 signal not found>

The track 0 signal fails to occur after 77 step pulses (bit 4 of status register 0).

<missing address mark in datafield>

No address mark in the datafield (bit 0 of status register 2).

<missing address mark in id-field>

No address mark in the id field (bit 0 of status register 1).

<bad cylinder>

The contents of the cylinder number on the medium are different from the internal register and the cylinder number appears to be FF hex (bit 1 of status register 2).

<wrong cylinder>

The contents of the cylinder number on the medium are different from the internal register (bit 4 of status register 2).

<cannot find sector>

The controller cannot find the sector specified in the internal register (bit 2 of status register 1).

<crc fault in id-field>

The CRC check discovered an error in the id field (bit 5 of status register 1, when bit 5 of status register 2 is zero).

<crc fault in data field>

The CRC check discovered an error in the data field (bit 5 of both status register 1 and 2).

<overrun>

If the controller is not serviced by the DMA-controller within a certain time interval, the error occurs (bit 4 of status register 1).

<access beyond last sector>

The controller has tried to access a sector beyond the final sector of a cylinder (bit 7 of status register 1).

When one of the mentioned error messages, which has relation to a specific drive occurs, a heading is written before the message identifying the drive. The drives are numbered 0 through 3.

5. NVM-TEST 5.

The NVM-test is testing the non volatile memory on the MIC board for data recovery.

It is not included in the big sequential loop, but must be started by entering test No B. If loop mode is selected the test will only perform read operations from the non volatile memory.

When loop mode is not selected the test will only perform one write and one read operation on every 21 double bytes of the non volatile memory. This is done with the help of the standard procedures WRITE NVM and READ NVM.

The pattern written into the non volatile memory is 55 AA AA 55 55 and so on.

The data read from the non volatile memory is written into the main memory and this pattern is compared with the write buffer.

If an error occurs the following errortext will be written:

<data error, byte no: xx xx exp: xx rec: xx>

Note: This test should normally not be used in the field, because it is destructive to the original configuration parameters in the non volatile memory.

6. FLEXIBLE DISK ADJUSTMENT 6.

The flexible disk adjustment program is not a test program, but a tool for the technician, which enables him to perform the three kinds of mechanical adjustments in question for the flexible disk drives. This is why it is not included in the PROM's for the RC850 testsystem, TOTEM, (ROB097 and ROB098 or ROB231), but delivered as a separate PROM (ROB230). This means that TOTEM can operate wihout this PROM installed. In this case, if the test No A is selected, the big sequential loop is reentered. But the flexible disk adjustment program is an integrated part of TOTEM and cannot be used without the rest of TOTEM.

When the testsystem is loaded from flexible disk, this program will always be included.

To perform the needed adjustments, a CE diskette should be used. For 8" drives CED702 and for 5 1/4" CED701.

6.1 Parameter Selection for Adjustment Program 6.1

The adjustment program is started by entering test No A. When started the screen is cleared, and the following text is written on the screen

<Diskette drive adjustment>
<drive:>

This must be answered with one of the numbers 0, 1, 2 or 3.

Then the text

<, type (5) or (8):>, { <5> / <8> }

is written. <5> is written, when the controller is set to 5 1/4" drives, <8> is written when the controller is set to 8" drives.

To select the type of adjustment the following must be answered:

<(0) track 00 sensor>
<(1) index sensor>
<(2) head adjust>
<select:>

Only the mentioned numbers 0, 1 or 2 will be accepted.

If the selected adjustment is either index sensor or head adjust the following will be written:

<track:>

Which must be answered with an number less than 77 for 8" drives and less than 40 for 5 1/4" drives.

<, head:>

Must be either adjustment of head 0 or 1.

6.2 Adjustments 6.2

The following describes the three adjustment to be performed on flexible disk drives.

6.2.1 Head Adjust 6.2.1

When the adjustment is carried out, the CE diskette must be placed in the diskette drive. Normally there will be a signal in track 40 on 8" diskettes to adjust the heads, on 5 1/4" diskettes it is in track 16.

First head 0 must be adjusted. The oscilloscope must be connected as written in the manufacturer's manual. See sections 6.3 and 6.4.

The two parts of the position signal must be adjusted to be as equal as possible.

The same adjustment must be performed for head 1. These two adjustments are dependent of each other, which means that when head 1 is adjusted, head 0 is changed.

As there can be a slight difference in the adjustment depending on whether the heads come from the inner or outer side of the track, it is necessary to make the adjustment for both possibilities.

Because the adjustment program only performs a realibration once, a seek from the inner side can be performed, when adjusting heads, by restarting twice <CR>, first defining a track behind the adjustment track, and then defining the adjustment track again.

If the adjustment is not homogeneous enough for the head 0 and 1, this homogeneity may be achieved by re-adjusting the two heads. It may be necessary with several adjustments and controls.

Note: Never try to adjust the mutual positions of the heads. If it is impossible to make the heads good enough simultaneously, fulfilling the manufacturer's specifications with respect to the relation between the A and the B signal, the heads must be replaced. The heads must also be replaced if the output signal is too low.

6.2.2 Track '00' Sensor Adjustment 6.2.2

The track '00' sensor must change level halfway between track '0' and '1' for the 5 1/4" and halfway between track '1' and '2' for the 8" diskette.

To carry out this adjustment, the track '00' program must be selected.

The carriage will now step forwards and backwards between 0 and 1 (if it is an 8" it is between 1 and 2). The track '00' sensor must now be adjusted to a dutycycle of 50/50.

6.2.3 Index Sensor Adjustment 6.2.3

Normally burst signals are recorded besides the indexhole. These burst signals are used when the index sensor is going to be adjusted.

The adjustments take place by measuring the time from the indexpulse appears to the burst is read by the head.

These pulses are recorded on track '1' and '34' on the 5 1/4" and on track '1' and '76' on the 8", when a CE diskette is installed.

6.3 Adjustment of the Mini Diskette Drive (5 1/4") 6.3

6.3.1 Adjustment of the Speed of Rotation 6.3.1

The first thing to be adjusted is the speed of rotation. The drive is set on its left side, seen from the front, and the heads are loaded for example by choosing function (1). The velocity is controlled by the tachometer on the balance wheel and is adjusted by the potentiometer on the motor controlboard. If the black lines move one linewidth per second, the velocity deviation is 1% by the frequency 50 Hz.

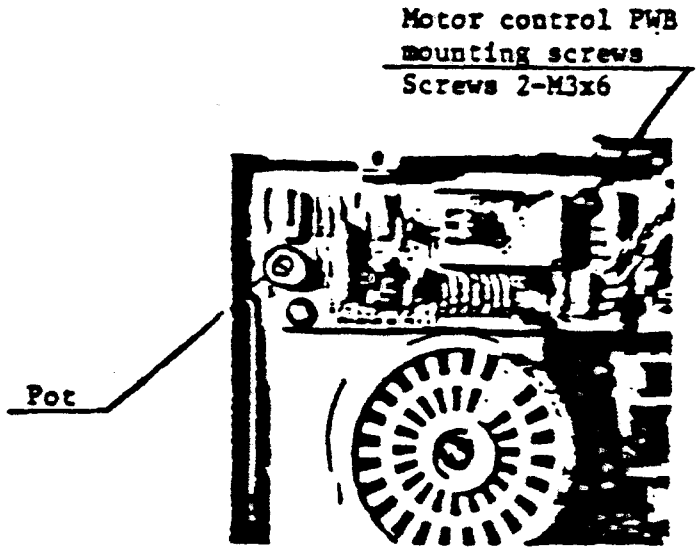

Figure 3: Motor control board, bottom view.

6.3.2 Adjustment of the Heads

6.3.2

When adjusting the heads, channel 1 on the oscilloscope is connected to the testpoint TP1A, channel 2 to the testpoint TP1B and the external trigger to the testpoint TP3. It is important that the groud connection is connected from both of the probes on channel 1 and channel 2.

The oscilloscope is set as follows:

Both of the channels in	AC mode
The vertical function in	ADD mode
Invert	ON
Time/div	20 msec.
Volt/div (ch1, ch2)	50 mV

The picture of the oscilloscope should look like this:

When B is larger than A,

$A/B > 0.8$

When A is larger than B,

$B/A > 0.8$

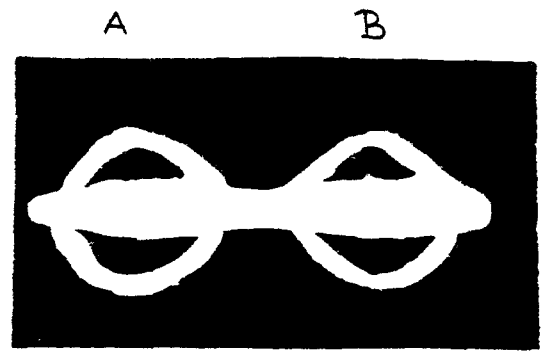

Figure 4: Oscilloscope picture of positioning signal.

To adjust the head position, the two screws keeping the stepper firm are loosened, and the motor is carefully turned until the two signals A and B are equal.

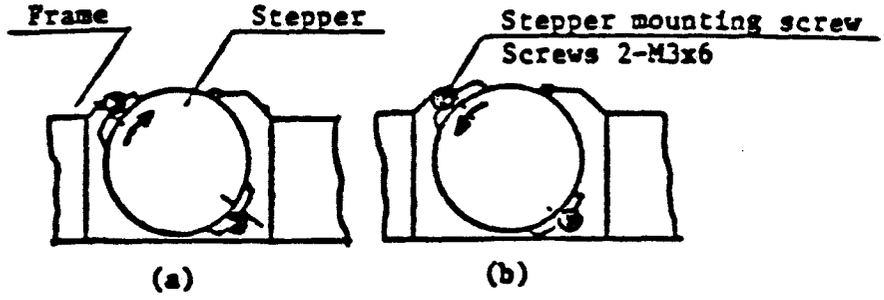

Figure 5: Stepper Motor.

6.3.3 Adjustment of the Indexpulse

6.3.3

When adjusting the indexpulse, the oscilloscope is connected in the same way as when adjusting of the heads. The setting of the oscilloscope is as follows:

Both the channels in	AC mode
The vertical function in	ADD mode
Invert	ON
Time/div	0.1 ms.
Volt/div (ch1, ch2)	100 mV

The indexsensor is moved until the burst signal is displaced from 300 µs. to 500 µs.

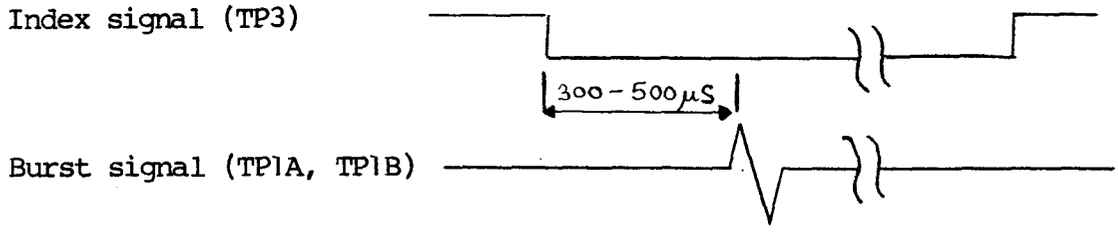

Figure 6: Index timing signal.

6.3.4 Adjustment of the Track '00' Sensor 6.3.4

When adjusting the track '00' sensor only channel 1 is used. The channel is connected to the testpoint TP5.

The setting of the oscilloscope is as follows:

The channel 1	DC mode
The vertical function	CH1 mode
Invert	OFF
Time/div	**
Volt/div	1 V

The time/div is set to be uncalibrated in such a way that one pulse is exactly 10 squares long.

After this, the track '00' sensor is loosened and is moved until the fraction between the time when the signal is high and the time when signal is low is 1:1. Then the sensor is tightened again.

When the adjustment is finished, the loosened screws are tightened and the adjustments are controlled again.

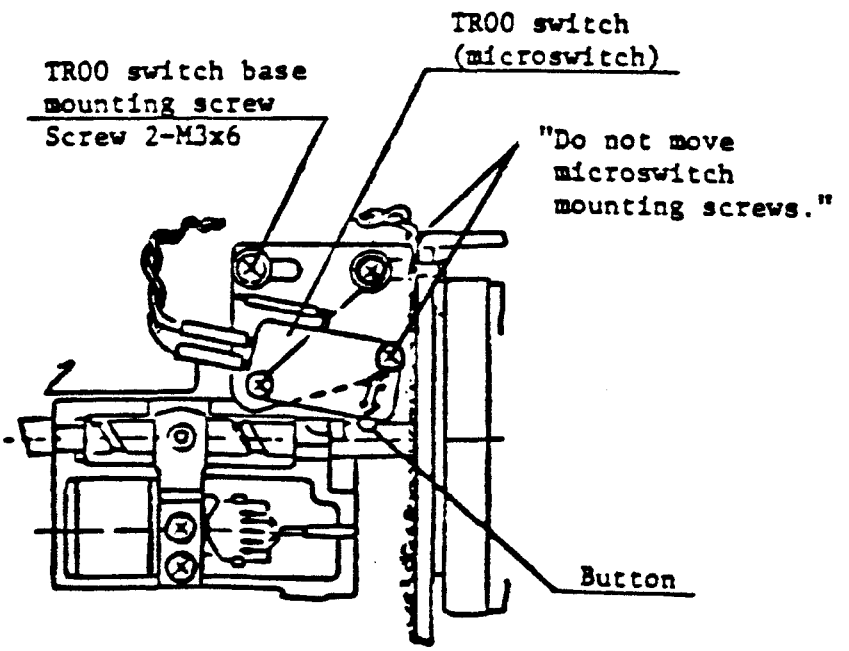

Figure 7: Track '00' switch, bottom view.

6.4 Adjustment of the Maxi Diskette Drive (8") 6.4

6.4.1 Adjustment of the Heads 6.4.1

When adjusting the heads, channel 1 on the oscilloscope is connected to the testpoint TP1A, channel 2 to the testpoint TP1B and the external trigger to the index signal on the connector J1, pin 20.

It is important that the ground connections are connected to the probes of both channel 1 and channel 2.

The oscilloscope is set as follows:

Both of the channels in	AC mode
The vertical function in	ADD mode
Invert	ON
Time/div	20 ms.
Volt/div (ch1, ch2)	50 mV

The picture of the oscilloscope should look like this:

When B is larger than A,
A/B > 0.8

When A is larger than B,
B/A > 0.8

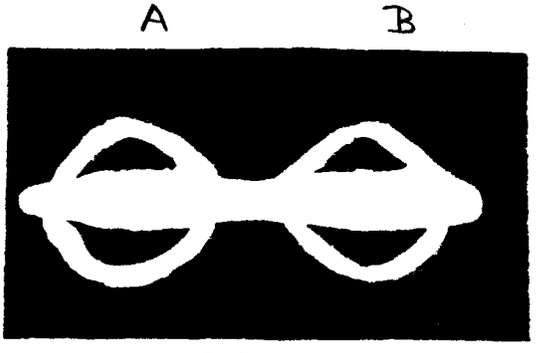

Figure 8: Oscilloscope picture of positioning signal.

When adjusting the head position, the two screws which squeeze the steelbelt, are loosened and now the head is carefully displaced until the two signals are equal. Note that it is probably half a millimeter the heads should be moved.

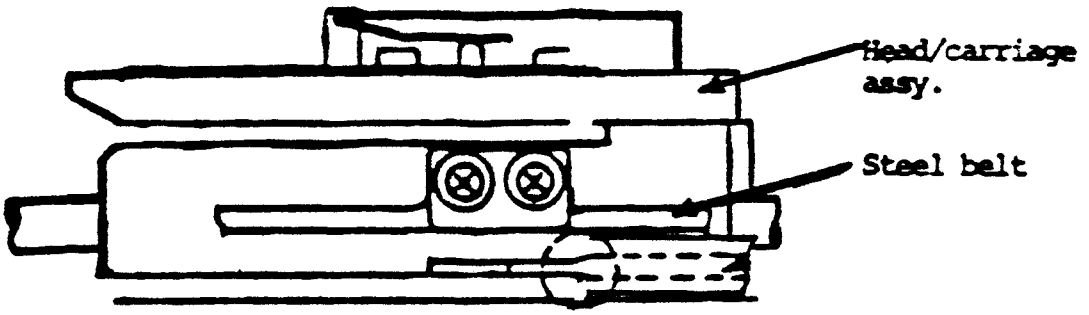

Figure 9: Adjustment of head on the steelbelt.

6.4.2 Adjustment of the Indexpulse 6.4.2

When adjusting the indexpulse, the oscilloscope is connected in the same way as when adjusting the heads. The oscilloscope is set as follows:

Both the channels in	AC mode
The vertical function in	ADD mode
Invert	ON
Time/div	0.1 ms.
Volt/div (ch1, ch2)	100 mV

The indexsensor is moved until the burst signal is displaced between 0 and 1000 µsec.

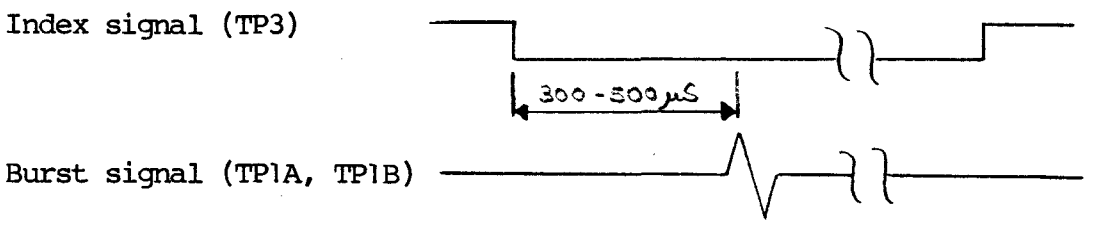

Figure 10: Index timing signal.

6.4.3 Adjustment of the Track '00' Sensor 6.3.4

When adjusting the track '00' sensor only channel 1 is used. Channel 1 is connected to the operational amplifier LM339N on pin 1.

The setting of the oscilloscope is as follows:

The channel 1	DC mode
The vertical function	CH1 mode
Invert	OFF
Time/div	**
Volt/div	1 V

Time/div is set to be uncalibrated in such a way that one pulse is exactly 10 squares long.

After this, the track '00' sensor is loosened and is moved until the fraction between the time the signal is high and the time when signal is low is 1:1.

When the adjustment is finished, the loosened screws must be tightened and the adjustments should be controlled again.

6.5 Changing the Adjustment 6.5

When the adjustment is selected the following is written.

<READY.><type <esc> to reset, <cr> to select:>

When the adjustment is terminated, the program can be restarted by typing carriage return. Note that the recalibrate command is only performed once, when entering the test. If typing <esc> the testsystem TOTEM will be started again with its switch parameters reset.

7. INFORMATION ABOUT THE TESTSYSTEM 'TOTEM' 7.

As this manual describes additional tests in the RC850 testsystem TOTEM, not described in the first manual, the complete list of relationship between test numbers and actual tests is as follows:

Test No	Test name
0	selftest
1	memory controller test
2	DMA test
3	CRT test
4	CTC test
5	SIO test (including X.21 test)
6	KEY test
7	FDC test
8	circuit test (part of the SIO test)
9	FDD test
A	flexible diskette adjustment
B	NVM test
C	not used yet
D	not used yet
E	not used yet
F	not used yet

The test numbers 'not used yet' will force the system to run the selftest.

7.1 'TOTEM' Situated in PROM 7.1

The RC850 testsystem can be delivered in PROM's either 2x4 k bytes (ROB097, ROB098) or 1x8 k bytes (ROB231).

The flexible disk adjustment program is delivered in a separate PROM (ROB230). Note that it is an integrated part of TOTEM, and cannot be used as a stand alone PROM.

Note furthermore that ROB230 cannot be used together with ROB231, which is the 1x8 k PROM for MIC507.

7.2 Further Errorcodes 7.2

The list of errorcodes shown in section 9.5 of the first manual is expanded with the following codes:

18: FDC not ready to receive or transmit
19: the wrong data-direction in FDC
20: FDC fault in status register
31: fault in FDC (in FDD test)
32: seek error
33: FDC command abort
34: open door
35: recalibration error
36: track 0 signal not found
37: missing address mark in data field
38: bad cylinder
39: wrong cylinder
3A: missing address mark in id-field
3B: cannot find sector
3C: crc fault in id-field
3D: crc fault in datafield
3E: drive not ready
3F: overrun in FDC
40: trying to access beyond last cylinder
41: drive is write protected
42: flexible disk drive timeout
43: flexible disk data error
E0: NVM data error
F0: X.21 status error

RETURN LETTER

Title: RC850 - TOTEM - Test System User's Guide, Part 2

RCSL No.: 30-M321

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