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RC850 - TOTEM - Test System
User's Guide

RCSL 42-i1905

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Abstract:

This manual describes the test system and the test programs for the RC850 terminal. The test programs described in this manual are: The selftest (memory-test), the main memory refresh test, the DMA test, the CRT test, the CTC test, the SIO test and the keyboard test. Further test programs may be described in separate manuals.

(30 printed pages)

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1. INTRODUCTION 1.

This manual describes the diagnostic test programs for the RC850 terminal.

The test programs are testing the basic functions of the different parts of the hardware in a terminal.

The sequence of the different test programs in the test system is organized with rising complexity. - As far as possible no part of the hardware is used before it is tested.

1.1 Configuration Requirement 1.1

The test system requires a main memory of 64 k bytes. Other test facilities are two test plugs for the line connections (CBL998) and a test plug for the keyboard connection (CBL999).

1.2 Load and Start 1.2

The test system is delivered on a flexible disc (RCSL No 30-M318) and as PROM's to be installed on the MIC board (ROB097 and ROB098)

Starting the test system situated in PROM:

- turn off power, remove hood, install PROM's in sockets and turn on power again.

Starting the test system from flexible disc:

- insert diskette in drive, push reset buttom, and type <T> when menu has appeared on the screen.

2. POWER UP SELFTEST 2.

This is a general test loop which is included in all terminals of the RC850 series. It is activated at power up or by pushing the reset buttom. Looping can be performed by selecting so from the keyboard when the program is running under control of the RC850 test root (TOTEM).

The selftest consists of two tests, a PROM checksum test and an RAM memory test.

2.1 PROM Checksum Test 2.1

A check on the contents of the PROM (containing bootprogram or tests) is performed by adding the contents of all locations in the PROM and checking that the result is zero.

If a difference from zero is found an attempt is made to write an error message on the bottom line of the display.

The error message has the following laytout

<RC850 checksum error>

Note that when loaded from flexible disc the checksum is checked on the loaded image.

2.2 RAM Memory Test 2.2

The power up test also performs a test of the dynamic RAM memory. Of cause all memory cells are tested by the memory test (all variables are kept in CPU registers).

First the upper part (addresses higher than the last PROM address) of the memory is tested. If this was found OK the test is moved from PROM to RAM memory and the memory space shaded by PROM is tested.

The test pattern for the dynamic RAM memory consisting of chips of 1 bit x 16 k is three times 00 followed by three times FF hex. When all memory cells have been tested, they are again tested with the inversed pattern. This means that all bits are tested for "zero" and "one" insertion. It is also the most convinient pattern for discovering addressing errors because this modulus 3 pattern will not be repeated equivalent in a higher modulus address.

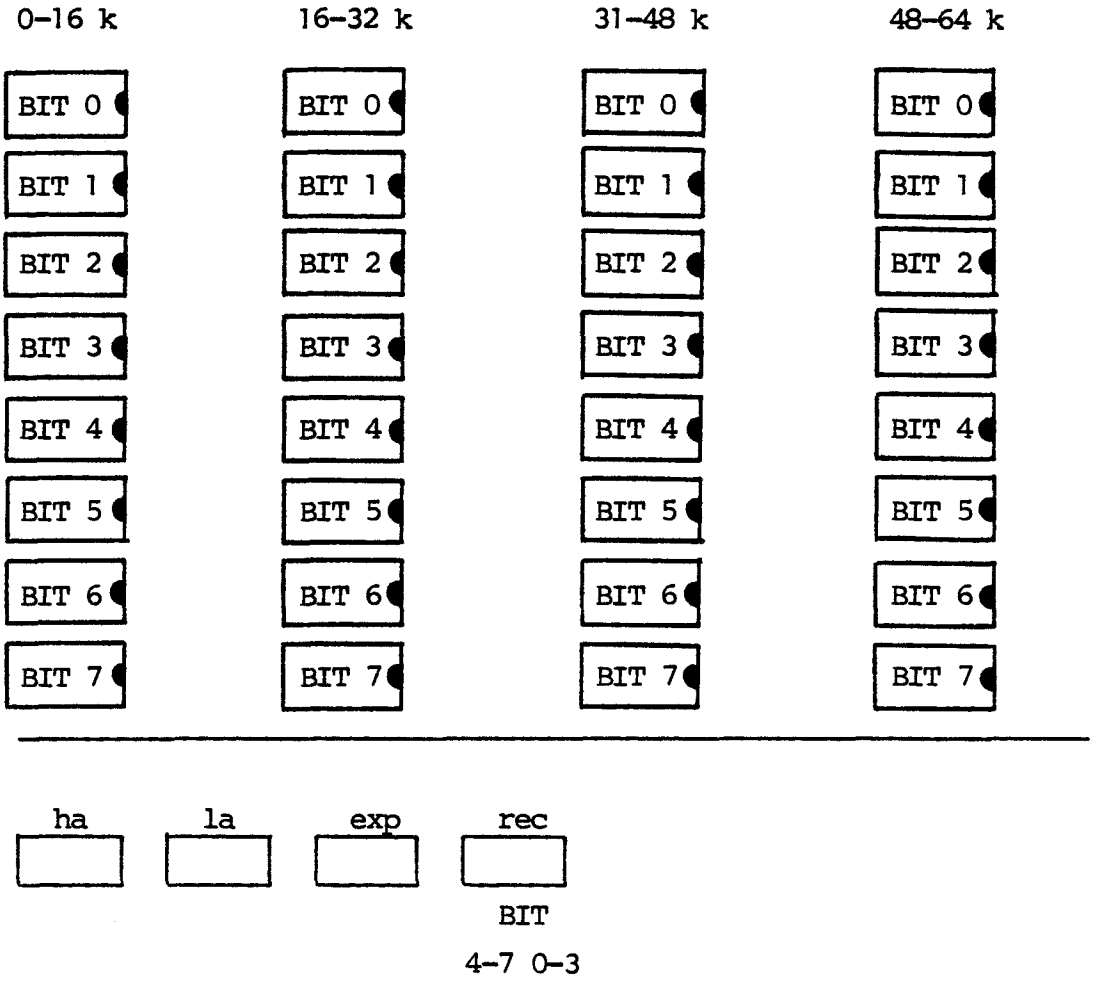
If an error occurs a message will be written on the bottom line of the display. The layout is the following:

<RC850 memory error ha la ex re>

where "ha" is high address, "lo" is low address, "ex" is expected value and "re" is received value. All numbers are in hexadecimal notation. (To find any defective chip consult fig. 1).

When both the PROM checksum test and the RAM memory test are terminated, an attempt is made to write on the display (whether there has been an error or not). This is done as simple as possible without any standard programs (without interrupt service). On the first 6 positions of the bottom line, the identification of the terminal type will be written followed by a possible error message.

The total turn around time for the selftest is 7.5 secs.



0 0 0 0 3 F F F	0-16 k
4 0 0 0 7 F F F	16-32 k
8 0 0 0 B F F F	32-48 k
C 0 0 0 F F F F	48-64 k

Figure 1: Layout of 64 k RAM memory.

3. DMA TEST 3.

The DMA test loop is testing DMA transfers between channel 0 and channel 1. This is done as a memory to memory transport. Channel 1 is receiving and channel 0 is transmitting.

When the transport is finished the receiving buffer is checked against the transmitted buffer byte by byte.

The DMA test will write its messages on the first line of the display.

Apart from the identification of the test, the possible messages from the DMA test are:

<OK>
<TC timeout 200 ms>
<data error, byte no: xx xx exp: xx rec: xx>

All numbers are in hexadecimal notation. "TC timeout 200 ms" is notification that the terminal count bit for channel 1 in the DMA status register has not been set within 200 ms and that the transport is therefore not successful.

The transmitted pattern is a buffer of 1 k containing a counting pattern. The pattern is as follows: 00 FF FE FD etc. repeated 4 times.

4. CRT TEST 4.

At first this test loop will print its identfication text on the second line of the display.

The test loop is split up into 3 parts, refresh RAM test, character RAM test and light effects.

4.1 Refresh RAM Test 4.1

The first part is, for those terminals having DMA connection between main memory and refresh memory, transmitting a test pattern of 4 k via DMA to the refresh memory and receiving it again.

After completion of the transport, it is tested that the terminal count on channel 0 is reached, and that no differences are discovered between the transmitted and received buffer.

If an error in the refresh RAM is discovered it should be interpreted in the following manner:

IC	address range (byte no:)	4 bits	even/odd addr.
55	0000-07FF hex	MSB	even
56	0800-0FFF hex	MSB	even
57	0000-07FF hex	LSB	even
58	0800-0FFF hex	LSB	even
59	0000-07FF hex	MSB	odd
60	0800-0FFF hex	MSB	odd
61	0000-07FF hex	LSB	odd
62	0800-0FFF hex	LSB	odd

If an error is discovered the related error message is written after the identification text and the test loop is terminated.

The layout of an error message is:

<CRT-test: refresh RAM data error, byte no: xx xx exp: xx rec: xx>

Be aware that messages written on the display can be unreadable, if there is an error in IC55 (and for some cases in IC57).

4.2 Character RAM Test 4.2

For those terminals containing character RAM memory, this will be tested in the same manner as for the refresh RAM. A buffer of 8 k bytes is transferred from main memory to the character RAM and back to main memory via DMA.

The test assumes that, if the high order 4 bits of byte 0 are all ones and the high order 4 bits of byte 4 are all ones in the test buffer, then there are character RAM's present. This could mean that if there where an error in IC30 of the CRT board the only identification of this error is that at the end of the loop the text "char RAM:OK" is not written (instead the text "OK" or "refresh RAM:OK" could be seen, just as if there was no character RAM present).

If an error in the character RAM is discovered, the message written should be interpreted in the following manner. Assuming the case of an error in IC 26, the address that is shown will be even and the errornous bit will be in the four least significant bits. For an error in IC 26 the address could be in several ranges. These ranges will all have bases of a multiplum of 20 hex. An example of an errormessage that is indicating an error in IC 26 will look as follows:

data error, byte no: 00 40 exp: FF rec FE.

IC	addresses (byte No:)	4 bits	even/odd bytes
26	0000-0007	LSB	even
	0020-0027		
	0040-0047		
	0060-0067		
	a.s.o.		
27	0008-000F	LSB	even
28	0010-0017	LSB	even
29	0018-001F	LSB	even
30	0000-0007	MSB	even
31	0008-000F	MSB	even
32	0010-0017	MSB	even
33	0018-001F	MSB	even
34	0000-0007	LSB	odd
35	0008-000F	LSB	odd
36	0010-0017	LSB	odd
37	0018-001F	LSB	odd
38	0000-0007	MSB	odd
39	0008-000F	MSB	odd
40	0010-0017	MSB	odd
41	0018-001F	MSB	odd

The layout of error messages is as for the refresh RAM.

4.3 Light Effects

There are three memory areas of the CRT board that cannot be verified by the CPU. These are the character ROM, the shadow RAM and the attribute RAM. It is possible to verify the operation of these parts by inspecting the display while running the test.

4.3.1 Character ROM

All 128 characters values are written on the display (12 times).

When this picture has been shown for 3 seconds, all attribute and shadow values in the main memory (odd bytes) are changed. This should not affect the picture, because the initial contents of the attribute and shadow RAM's are all zeroes. This unchanged picture is shown for 2 sec.

4.3.2 Shadow RAM 4.3.2

The contents of the shadow character RAM are changed to all ones in the bytes 0-32 and 64-95. Having filled all refresh characters with spaces and having the shadow values of the refresh characters addressing all the 4 characters of the shadow RAM, the screen will lighten up with a raftered pattern (2 squares light followed by 2 squares dark).

When this picture has been shown for 3 sec. it is changed so that all dark squares now lighten up and the other way around. This makes it possible to discover some errors in the shadow RAM. More sophisticated errors can be found with the help of the interactive keyboard test.

4.3.3 Attribute RAM 4.3.3

At last the attribute RAM is tested. This is done by placing a pattern in the RAM which makes the screen lighten up with the following effect:

dark, normal intensity blink, dark, high intensity blink, dark, normal intensity, dark, high intensity. This is repeated as a raftered pattern.

At the end of the test loop the normal picture is shown again.

5. CTC TEST 5.

This program is testing the counter timer circuit which is used for baud rate generator and as interrupt circuit for the CRT and the FDC controller.

It is tested that the circuit will generate interrupt and that the vector (interrupt address) is correct.

The channels 0, 1, 2 are tested. Channel 0 and 1 are tested in counter mode, counting on the fixed input clock giving interrupt after approx. 423 µsec. Channel 2 is tested in timer mode. The timer is started by terminal count from the DMA caused by a transfer to the shadow RAM of the CRT board. The timing is approx. 16 msec.

The test is based on a timeout loop, so it is checked if the interrupt was received within a specified time (300 msec.). It is also checked that only the specified channel interrupts.

The test can end up with 2 different error messages:

<illegal interrupt, port: xx>
Meaning that another channel than the specified has interrupted.

<no interrupt, ch:>
Meaning that the test has timed out before interrupt was received.

Texts will be written on the third line of the display.

6. SIO TEST 6.

The SIO test is testing all 4 SIO channels of the RC850 and it is also testing the modem signals of the line1, line2 and circuit channels.

6.1 Modem Signal Response 6.1

For the line1 and line2 SIO the responses of DTR and RTS are tested on the CI, DCD, CTS and DSR pins. All four combinations are tested. There must either be installed loop plugs as in fig. 2 on the terminal connections or the related signals must be looped on the MIC board.

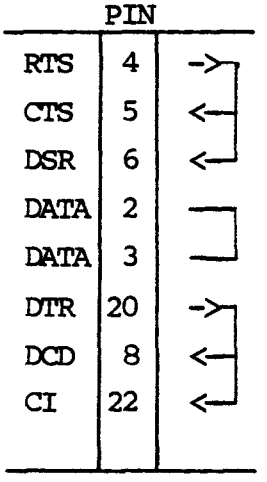
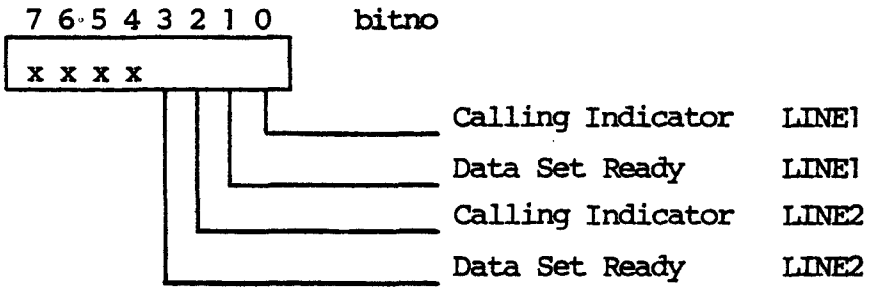


Figure 2: Line test loop plug (CBL998).

If an error occurs on the modem signals CTS, DCD, DSR or CI the received hex value should be interpreted as shown in fig. 3.



x = UNDEFINED.

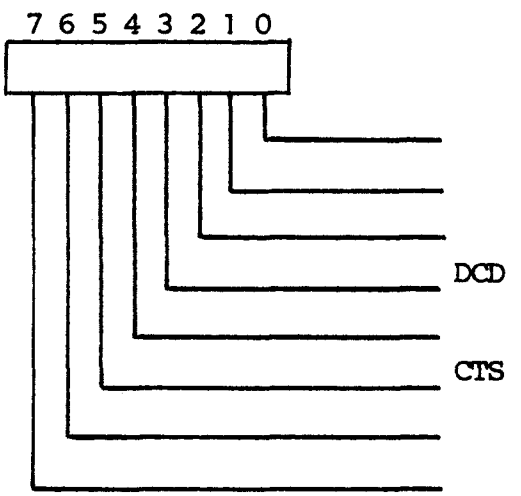


Figure 3: Modem signal response.

The response of the DCD signal of the circuit SIO is tested as a function of DTR and RTS.

Possible error messages from this part of the test are:

{ <line1:> / <line2:> / <circuit:> } , { <CTS or DCD error,> / <CI or DSR error,> } , { <exp: xx rec: xx> }

numbers xx are in hexadecimal notation.

6.2 Line, Printer and Keyboard SIO Test 6.2

When the modem signal response is checked the testing of line1, line2 and keyboard SIO channels is initiated. The keyboard plug must be looped as in fig. 4.

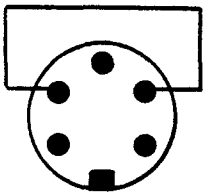


Figure 4: keyboard loop plug.

The testing procedure is as follows. Each of the three channels is started and the control is handed over to the interrupt system and a timeout loop.

The keyboard SIO channel is running on a baud rate of 300 bps. The line1 and line2 SIO channels are initiated to 9600 bps by the CTC. In the beginning the line1 channel tries to operate on an external clock. If this gives a timeout meaning that there was no external clock (e.g. loop plug installed) it automatically shifts to internal clock.

All three channels transmit a databuffer of 4 k bytes with a counting pattern (00 FF FE FD etc.). The timeout loop will check the received buffers as soon as they are transferred. It also monitors the three channels for timeout.

If test of keyboard SIO is not wanted the testsystem must have been informed about keyboard present (see section 9.2).

6.2.1 Baud Rate Measure 6.2.1

While the line1, line2 and keyboard SIO are active their respective baud rates will be measured. This is done over a period of 1 sec. by having the CTC channel 3 giving interrupt every (approx.) 16 msec. The number of bytes received in 1 sec. is multiplied by 11 and written (8 data bits, 1 start, 1 stop and 1 parity bit).

Be aware that when one channel is finished interrupts are disabled while the buffer is checked. This means that other channels' baud rates can be a little less than else.

6.3 Circuit Loop Back Test 6.3

When the first three channels are finished, the circuit SIO channel is tested. This is done by transmitting on every transmitter buffer empty until 4 k bytes is transmitted. The receiver is handled by the DMA channel 2. When all 4 k bytes are transferred the received buffer is checked.

It is possible to loop in the circuit test only (test No 8).

6.4 SIO Test Error Messages 6.4

<illegal interrupt, port: xx>:
meaning that an interrupt has occurred from a device that was not intended to interrupt, or that the SIO has given a status interrupt (any change on the modem signals during data transfer will respond with this message).

<parity error>:
meaning that a special receive interrupt with parity bit has occured.

<receiver overrun>:
meaning that a special receive interrupt with overrun bit has occured.

<data error, byte No: xx xx exp: xx rec: xx>:
meaning that the received buffer does not contain the expected pattern.

All of the three messages are identified by the channel heading: <line1:>, <line2:>, <keyb:> or <circuit:>.

These headings will also be shown as soon as the related channel has ended its transfer.

7. MEMORY REFRESH TEST 7.

The dynamic memory refresh test is a test which verifies the function of the memory controller chip.

It writes a pattern in memory consisting of an XOR of high and low address part. The pattern is written from the memory address 8000H until the hexadecimal address: F000H (where the display image starts).

When the pattern has been written, the test waits for 5 sec. in a waiting loop before it performs a check of data.

The main purpose of this test is to discover modification of data happened in the delay time, due to malfunction of the refresh counting in the memory controller.

Possible error message is:
<data modified in byte xx xx exp: xx rec: xx>

Output is placed on the last line of the display following the terminal identification name (TOTEM).

8. KEYBOARD TEST 8.

The keyboard test is an interactive test, which can be used to verify the hexadecimal values of the keys on the keyboard.

The keyboard test has a waiting loop in which it waits 5 seconds for a key to be hit. When a key is struck the related hexadecimal value is shown on the display and can be checked by consulting fig. 5. The reason why the test is not writing the related character is the fact that the keyboard layout is not given.

Struck the space bar will terminate the looping mode if the test was placed in the looping state.

There are 3 keys which have been assigned double values. These are the keys with the hexadecimal values A0, C6 and 89. The slip values are B3, B4 and B5.

A keyboard could hold up till 13 lamps and one audio output. The table below is informing about the relationship between key values and lamp output.

Fig. 6 shows lamp numbers.

Key No	Lamp No
66H	0
67H	1
68H	2
69H	3
6AH	4
6BH	5
E2H	6
C9H	7
8BH	8
8AH	9
89H	10
88H	11
87H	12
86H	13
85H	audio output

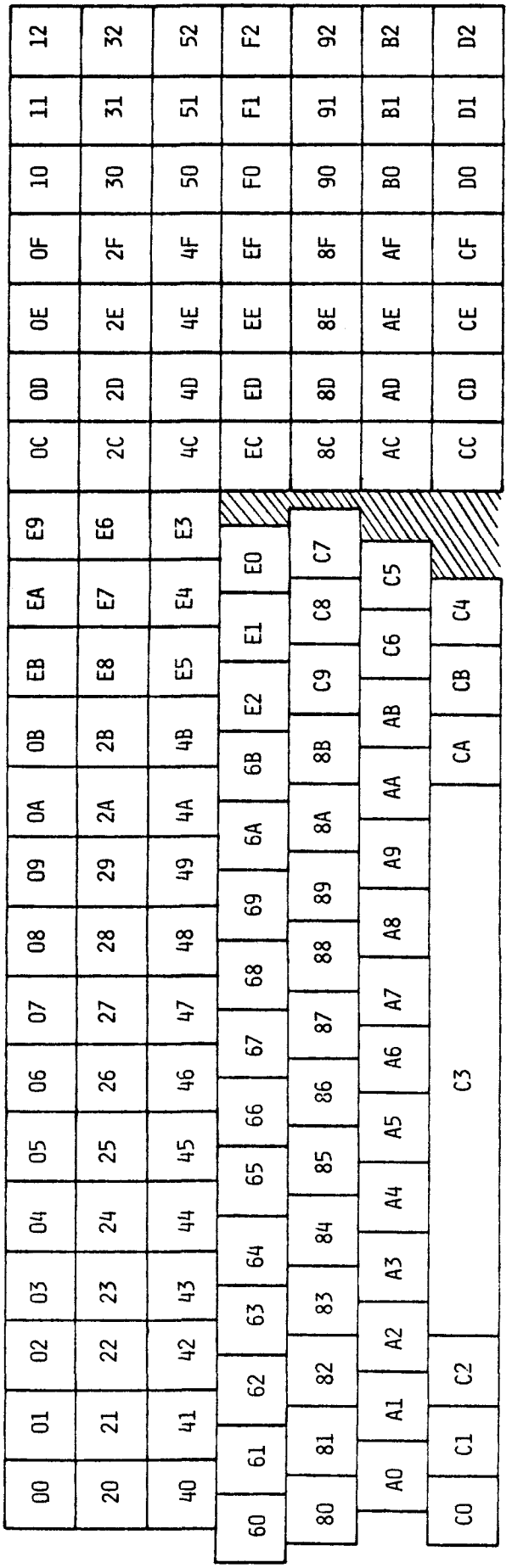


Figure 5: Key position values.

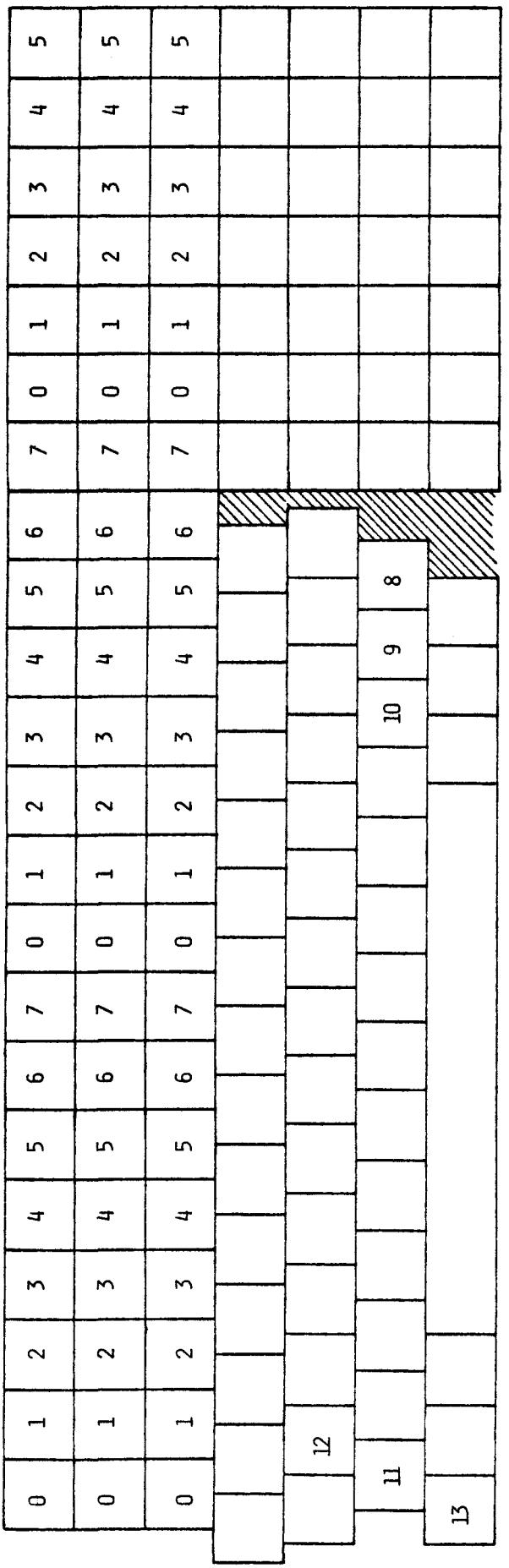


Figure 6: Specification of LED layout.

8.1 Shadow RAM Test 8.1

The keys with the hexadecimal values 62, 63, 64, 65 have special functions.

They are intended to be used to test the shadow RAM memory.

The shadow RAM contains 4 characters of 16 x 16 bits (128 bytes) organized as fig. 7.

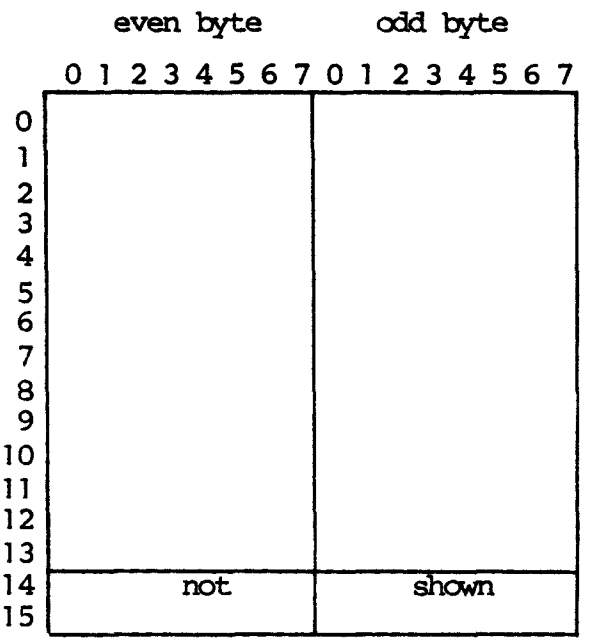


Figure 7: One character of the shadow RAM.

Due to the fact that there are 4 characters in the shadow RAM, 4 characters on the display will address the 4 shadow characters (shadow field values 0-3). The positions of these characters are 75, 76, 77 and 78 on the line of the keyboard test. Note that all other characters on the display will also address shadow character 0.

When key 62H is struck a horizontal bar (FF) will move from the highest address of the shadow RAM towards lower addresses (seen as a horizontal bar moving upwards shifting side from odd to even byte and back every second time).

Struck at key 63H is as 62H, but moving downwards.

When key 64H is struck a vertical bar (one bit) in one entire character of the shadow RAM will move from MSB towards LSB (seen as two vertical light bars moving).

Struck at key 64H is as 64H, but moving from LSB towards MSB.

9. ROOT 9.

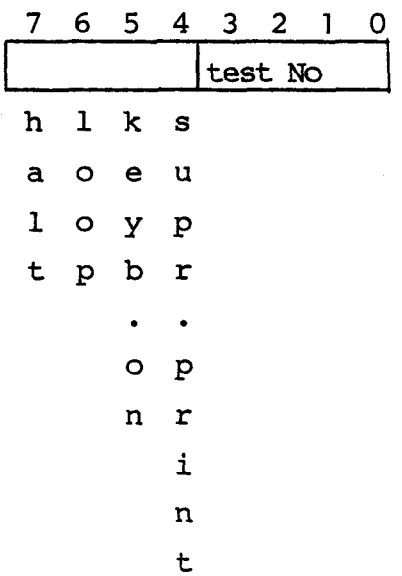
Besides the test programs, the RC850 test program system consists of a test router (TOTEM), which has the purpose to administer the mode in which a particular test is run. Furthermore a test library holds some commen routines.

9.1 The Router 9.1

The ROOT is a central loop for the test system. Every time a test program has ended, the ROOT is entered. The main purpose of the ROOT is to compute the address of the next test in sequence. The address of the next test is derived from a variable holding the present test number, normally incrementing the number by one.

9.2 Switch Parameters 9.2

The variable holding the test number also contains four switch bits, by which the ROOT decide how to administer the tests.



halt: 0: halt on error
1: proceed though error

loop: 0: sequencial, big loop of all tests
1: looping in the present test

keyb on: 0: the system has not been informed about an installed keyboard
1: a key on the keyboard has been struck at least once (testing the keyboard channel will be bypassed in the SIO test)

supr print: 0: messages are printed on the display
1: no messages are printed (usable for fast looping)

Initial values of the switch parameters are all zeroes.

9.3 Keyboard Management 9.3

The switch parameters and the test number can be changed by the keyboard except in the keyboard test.

Valid keys on the keyboard are as follows:

H: set halt bit to 0
R: set halt bit to 1
L: set loop bit to 1
G: set loop bit to 0
S: set suppress print bit to 1
P: set suppress print bit to 0

<esc>: will stop execution.

This is also the fact for any other key. Struck the <return> key will have the test system reentering the looping or running state.

Numbers between 0-F will insert a new test number into the variable.

All other keys are invalid and will respond with a <?>.

Relationship between test numbers and actual tests is as follows:

Test No	Test name
0	selftest
1	memory controller test
2	DMA test
3	CRT test
4	CTC test
5	SIO test
6	KEY test
7	FDC test
8	circuit test
9	flexible disc drive test
A	not used yet
B	not used yet
C	not used yet
D	not used yet
E	not used yet
F	not used yet

Test numbers 8 through F are not included in the sequencial test loop. The test numbers not used yet will force the test system to run the selftest.

9.4 Output 9.4

The ROOT will respond with some output. This is a version date and a test number. It also responds with the state of the test. This could be either running, stopped, looping or halted.

9.5 Specialities 9.5

The ROOT has a waiting point of 3 secs. when entered from the selftest to give the user time to key in some input to change parameters.

The ROOT also outputs an error code number, which is specific for the type of error discovered, on a not used port (50 hex). This enables the user to run the test system on an MIC board alone without display controller and although get some specific information, if a device which can decode the numbers is installed on the system bus (normally only used in the production phase).

These error code numbers are as follows:

0: OK, no error.
1: PROM checksum error.
2: Selftest memory error.
3: Data error in DMA test.
4: DMA channel 1 has not set the terminal count bit within 200 ms.
5: DMA channel 0 has not set the terminal count bit within 200 ms., when transporting data from memory to CRT refresh memory.
6: Data error in CRT refresh memory.
7: DMA channel 0 has not set the terminal count bit within 200 ms., when transporting data from memory to CRT character RAM.
8: Data error in CRT character RAM.
9: Not wanted interrupt in the CTC test.
A: Not used.
B: CTC test has timed out without interrupt.
C: Timeout, no receiver interrupts from line 1 (SIO).
D: Timeout, no receiver interrupts from line 2 (SIO).
E: Timeout, no receiver interrupts from keyboard line (SIO).
F: Modem signal response error.
10: Not wanted interrupt occurred in the SIO test.
11: Not used.
12: Parity or receiver overrun in the SIO test.
13: Data error in the line 1 (SIO) received buffer.
14: Data error in the line 2 (SIO) received buffer.
15: Data error in the circuit line (SIO) received buffer.
16: Data error in the keyboard line (SIO) received buffer.
17: Data error in main memory refresh test.

Further error code numbers will be described in the related manuals.

RETURN LETTER

Title: RC850 - TOTEM - Test System User's Guide

RCSL No.: 30-M317

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