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RC 3600 PERIPHERAL DEVICES
ASYNCHRONOUS MULTIPLEXER
REFERENCE MANUAL

Keywords : RC 3600 Manual, Asynchronous Multiplexer, Telemultiplexer, AMX 701, Reference Manual.

Abstract : This paper describes the logic structure of the Asynchronous Multiplexer AMX 701 for the RC 3600.

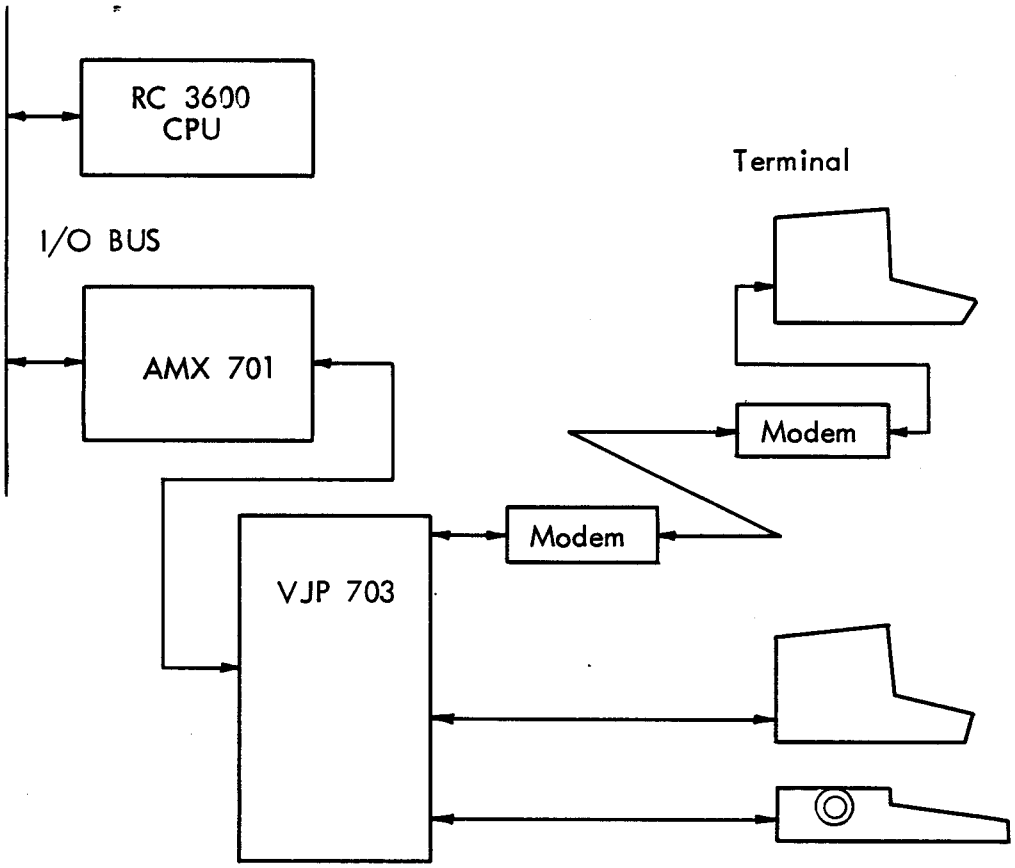
CONTENTS PAGE

1. MAIN CHARACTERISTICS

1.1. Description

The AMX 701 Asynchronous Multiplexer 701 is a controller to the RC 3600 computer which enables the computer to communicate with up to 8 asynchronous terminals.

Normally the multiplexer is connected to the terminals over a junction panel like the VJP 703. Fig. 1.1. shows the physical structure of the CPU, the AMX 701, and the VJP 703 connected to some terminals.



1.2. Data Formats

The transmission of characters between the asynchronous multiplexer and the terminals is serial-by-bit and asynchronous (start-stop transmission). A character consists of the following groups:

1. 1 start bit (logical zero).
2. 5, 6, 7, or 8 data bits.
3. Possibly a parity bit (odd or even parity).
4. 1 or 2 stop bits (logical one).

The program controls for each channel:

1. Number of data bits in the character.
2. Odd parity, even parity, or no parity.
3. 1 or 2 stop bits.
4. Bit rate for transmitter.
5. Bit rate for receiver.

The start bit and the stop bits and the parity bit are added to the characters before transmission and are deleted from the received characters before the characters are transferred to the CPU. An example of a character consisting of 1 start bit, 7 data bits, 1 parity bit, and 2 stop bits is shown in Fig. 1.2.

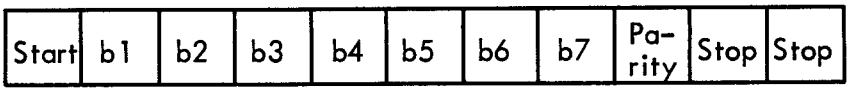


Fig. 1.2. 11-unit element character

The bits are transmitted in the order shown in Fig. 1.2. The start bit is transmitted as the first bit. The bit, b1, is the least significant bit of the data bits.

1.3. Applicable Documents

Additional information can be found in the following documents.

1. How to use the NOVA computers.
2. CCITT recommendation V24.

2. PERFORMANCE CHARACTERISTICS

2.1. Transmission Speeds

The AMX 701 can handle the following transmission speeds:

9600	b/s
4800	b/s
2400	b/s
1200	b/s
600	b/s
300	b/s
220	b/s
200	b/s
150	b/s
134,5	b/s
110	b/s
75	b/s
50	b/s
40	b/s

The speed stability is better than 0.1 per cent.

2.2 Distortion

Received Data : Max. 40 per cent
Transmitted Data : Max. 0.2 per cent

Spurious start pulses with a duration of less than 0.5 bit time are rejected.

2.3. Interface Signals

The controller, connected over junction panel VSP 703, has the following modem signals:

Protective Ground	Circuit	101	Cannon	pin	1
Signal Ground	-	102	-	-	7
Transmitted Data	-	103	-	-	2
Received Data	-	104	-	-	3
Request to Send	-	105	-	-	4
Ready for Sending	-	106	-	-	5
Data Set Ready	-	107	-	-	6
Carrier	-	109	-	-	8
Calling Indicator	-	125	-	-	22
Data Terminal Ready	-	108/2	-	-	20
Power On	-		-	-	23

3. LOGIC SPECIFICATION

3.1. Description

The AMX 701 is controlled by a DOA, a DOB, and a DOC command, and it can be sensed by a DIA instruction. The controller has no BUSY flag and no DONE flag, but it can send an INTERRUPT REQUEST. INTERRUPT DISABLE is controlled by Interrupt Priority Mask bit 2.

A clear function (F=01) clears the INTERRUPT REQUEST flip-flop. IORST clears the INTERRUPT REQUEST flip-flop and stops the controller, which means:

1.	Stops Receive-mode	See Section 3.3.1.
2.	Stops Transmit-mode	- - 3.3.3.
3.	Stops Break	- - 3.3.9.
4.	Sets Data Terminal Ready off	- - 3.3.7.

Fig. 3.1. on the next page shows the major parts of the controller.

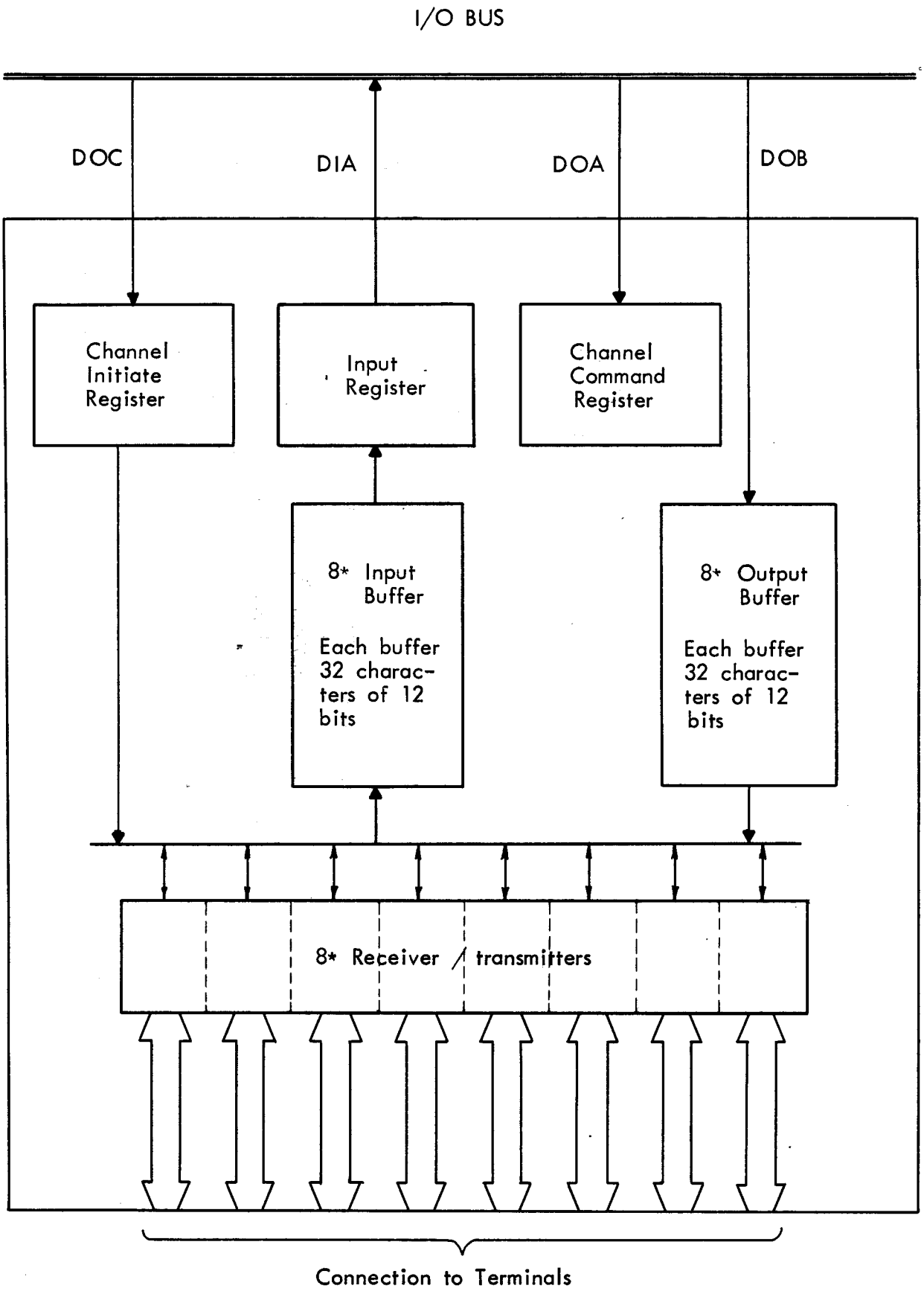
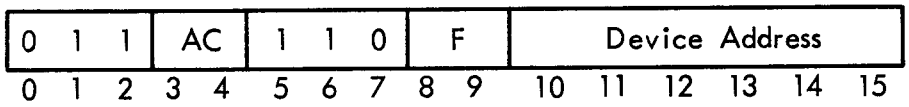


Fig. 3.1. Data paths of AMX 701

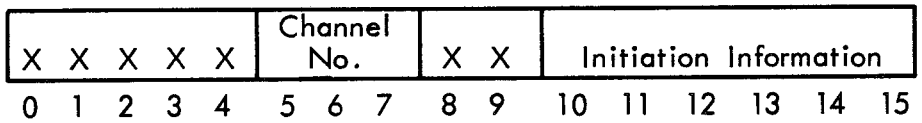
3.2. Channel Initiate Register

Prior to using the AMX 701 the channels must be initiated. This is done by means of three DOC commands which load the contents of the specified AC into the Initiation Register. The initiation can only be changed by a new DOC command.

DOC instruction



AC



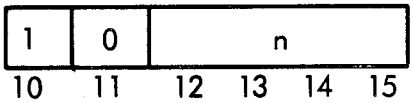
Channel No.

Bit (5:7) specifies which channel the program wants to initiate.

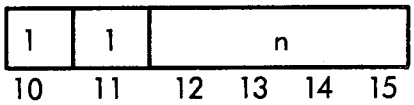
Initiation Information

There are three different initiations depending on the contents of the Initiation Field:

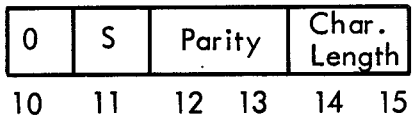
Initiation of Receiver:
bit rate



Initiation of Transmitter:
bit rate



Initiation of parameters:



Initiation of Receiver or Transmitter Bit Rate

Bit (12:15) specifies the bit rate in this way:

Bit (12:15)	Bit Rate b/s	Bit Time
0000	9600	104.2 us
0001	4800	208.3 us
0010	2400	417.0 us
0011	1200	833.0 us
0100	600	1.67 ms
0101	300	3.30 ms
0110	220	4.58 ms
0111	200	5.00 ms
1000	150	6.67 ms
1001	134.5	7.40 ms
1010	110	9.06 ms
1011	75	13.33 ms
1100	50	20.00 ms
1101	40	25.00 ms
1110	40	25.00 ms
1111	40	25.00 ms

Initiation of Parameters

Numbers of Stop Bits

Bit (11) specifies the number of stop bits to be transmitted as follows:

bit 11	Number of Stopbits
0	1 stopbit
1	2 stopbits

Parity

Bit (12:13) specifies the parity condition of the channel as follows:

bit 12	bit 13	Parity
0	0	Odd Parity
0	1	Even Parity
1	0	No Parity
1	1	No Parity

Character Length

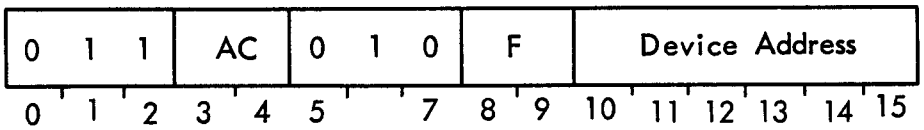
Bit (14:15) specifies the character length of the channel. The parity bit is not included in the character length. The character length is specified as follows:

bit 14	bit 15	Char. Length
0	0	5
1	0	6
0	1	7
1	1	8

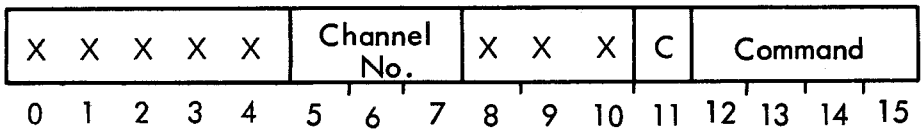
3.3. Channel Command Register

The operation of a channel is specified by means of a DOA command which loads the contents of the specified AC into a command register.

DOA instruction:



AC:



Channel No.

Bit (5:7) specifies which channel the program wants to command.

Command

Bit (12:15) specifies the commands.

The commands are:

Bit (12:15)	Command Name
0000	Receive
0001	Stop Receive
0010	Transmit
0011	Stop Transmit
0100	Select Input Buffer
0101	Select Modem Status
0110	Select In Buffer Status
0111	Select Out Buffer Status
1000	Set Data Term Ready On
1001	Set Data Term Ready Off
1010	Not Used
1011	Not Used
1100	Start Break
1101	Stop Break
1110	Enable Interrupt
1111	Clear One Character

3.3.1. Receive Command

The Receive command forces the addressed channel in Receive-mode, and the channel starts to receive characters and transfer them to the input buffer if Data Set Ready = 1. The channel stays in the Receive-mode until a Stop Receive command or an IORST arrives. If bit 11 is one during the Receive command, then the Input buffer is cleared, and the channel goes into Receive-mode.

3.3.2. Stop Receive Command

A Stop Receive command stops the channel if it is in Receive-mode. An input character possibly being effectuated when the command arrives is not received.

3.3.3. Transmit Command

The Transmit command forces the addressed channel into Transmit-mode, and the channel starts to output if there are data in its output buffer and if Data Set Ready = 1 and if Ready for Sending = 1. The channel stays in Transmit-mode until a Stop Transmit command or an IORST arrives.

If bit 11 is one during the Transmit command, then the Output buffer is cleared, and the Channel goes into Transmit-mode.

3.3.4. Stop Transmit Command

A Stop Transmit command stops the channel if it is in Transmit-mode. A character being transmitted when the command arrives is transmitted correctly.

3.3.5. Select Input Buffer Command

This command is used together with a DIA instruction to transfer information from the Input buffer to an accumulator. The Select Input Buffer command

loads the next character or status-word from the input buffer into the specified accumulator. The program has to send a Select Input Buffer command for each character or status-word the program wants to input. See Section 3.7.

3.3.6. Select Modem Status Command

This command is used together with a DIA instruction to transfer information about the modem signals to an accumulator. The Select Modem Status command loads information about the logical level of the modem signals into the Input Register, and the DIA instruction loads the Input Register into the specified accumulator. The program has to send the Select Modem Status command before each DIA instruction. See Section 3.4.1.

3.3.7. Select In Buffer Status Command & Select Out Buffer Status Command

These commands are used together with a DIA instruction to transfer information from the Buffer Status Register to an accumulator. The command loads the wanted status information into the Input Register, and the DIA command loads the status into the accumulator. The program has to send the command before each DIA instruction to load the correct status information into the Input Register. See Sections 3.4.2. and 3.4.3.

3.3.8. Set Data Term Ready On Command

This command sets the modem signal Data Terminal Ready On.

3.3.9. Set Data Term Ready Off Command

This command sets the modem signal Data Terminal Ready Off. An IORST sets Data Terminal Ready Off.

3.3.10. Start Break Command & Stop Break Command

Start Break command forces the addressed channel to output a break. The break is transmitted independently on modem input status signals and

Receive-mode or Transmit-mode.

Stop Break Command and an IORST terminates the break signal.

3.3.11. Enable Interrupt Command

This command controls the interrupt facility of the controller. After an Enable Interrupt command the controller is able to send an Interrupt Request. See Section 3.8.

After the controller has sent an Interrupt Request, the Interrupt is disabled until a new Enable Interrupt command is received. As the Interrupt facility is not a function of one channel but a function of all the Input Buffers or Output Buffers, the channel No. field (bit 5:7) is ignored. After an IORST the Interrupt is not enabled.

3.3.12. Clear One Character Command

This command clears one character in the Output Buffer and loads a status-word into the Input Register. A DIA instruction following the Clear One Character command loads the status-words into the specified accumulator. See Section 3.4.4.

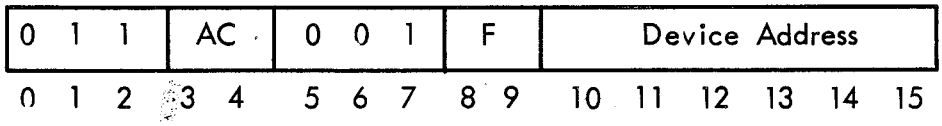
3.4. Input Register

The Input Register is updated by the following commands:

Select Input Buffer
Select Modem Status
Select in Buffer Status
Select Out Buffer Status
Clear One Character

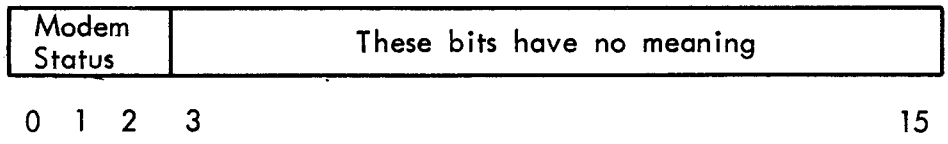
The content of the Input Register can be loaded into the specified accumulator by a DIA instruction. The Select Input Buffer command is described in Section 3.6.

DIA instruction



3.4.1. Select Modem Status Command

followed by a DIA instruction gives this content of the specified accumulator:



Bit (0) Calling Indicator

This status bit is logical one if the modem signal Calling Indicator is ON.

Bit (1) Carrier Off

This status bit is logical one if the modem signal Carrier is OFF.

Bit (2) Data Set Not Ready

This status bit is logical one if the modem signal Data Set Ready is OFF.

3.4.2. Select In Buffer Status Command

followed by a DIA instruction gives this content in the specified accumulator:

Bit (0) Not Input Buffer Full

This status bit is logical zero when the Input Buffer is FULL and logical one when the Input Buffer is not FULL.

Bit (1) Input Buffer Empty

This status is logical one when the Input Buffer is EMPTY.

3.4.3. Select Out Buffer Status Command

followed by a DIA instruction gives this content in the specified accumulator:

Bit (0) Not Output Buffer Full

This status bit is logical zero when the Output Buffer is FULL and logical one when the Output Buffer is not FULL.

Bit (1) Output Buffer Empty

This status bit is logical one when the Output Buffer is EMPTY.

3.4.4. Clear One Character Command

followed by a DIA instruction gives this content in the specified accumulator:

Bit (0) Not Last Character

This status bit is logical zero when the last character in the specified Output Buffer has been cleared by a Clear Command, and it is logical one when a character is cleared by a Clear Command and the cleared character was not the last character in the Output Buffer.

Because of the internal structure of the controller the program should not clear an empty Output Buffer.

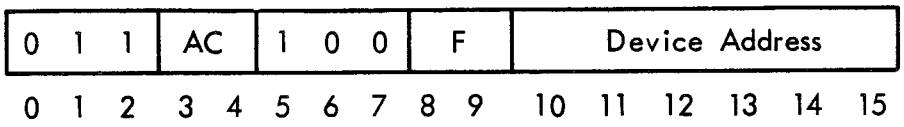
3.5. Output Buffer

The controller contains 8 output buffers, each 32 characters long. The Output Buffer is a first in first out buffer (FIFO). The channel starts to output data from its output buffer if:

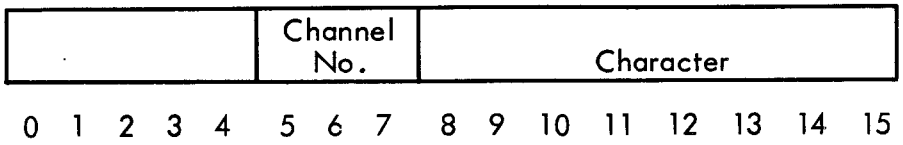
1. The channel is in Write-mode.
2. Data Set Ready = 1.
3. Ready for sending = 1.

Data is loaded into the output buffer by a DOB command:

DOB instruction



AC



Channel No.

Bit (5:7) specifies the channel No. of the output buffer in which the characters are to be stored. If the output buffer is already full, the character is lost.

Character

Bit (8:15) contains the character, and bit 15 is the least significant bit. If character length is 7 bit then bit 8 is ignored, if it is 6 bit then bit 8 and bit 9 are ignored, and if it is 5 bit then bit 8, bit 9, and bit 10 are ignored.

3.6. Input Buffer

The controller contains 8 input buffers, each 32 characters long. The Input Buffer has 12 bit words and contains both input characters and status words. The Input Buffer is a first in first out buffer (FIFO).

3.6.1. Input to the Input Buffer

Input to the Input Buffer arrives under the following conditions:

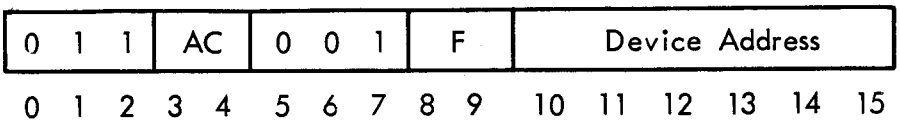
1. If the channel is in Receive-mode, and if Data Set Ready = 1, then the channel will receive characters and load them into the Input Buffer.

2. When some of the input modem signals change, one status word is sent to the Input Buffer, This is explained in detail later in this section.

3.6.2. Input to the Accumulator from the Input Buffer

To read information stored in the Input Buffer the program first has to send a Select Input Buffer command (Section 3.3.7.) which selects the wanted channel, and then a DIA instruction which loads the accumulator with the character or status word from the selected channel. The program has to send the Select Input Buffer command before each DIA instruction.

DIA instruction



3.6.3. The Input Is A Character

AC if the input is a character:

1	P	I/st	B	Not Used	Character
0	1	2	3	4 5 6 7	8 9 10 11 12 13 14 15

Bit (0) = logical one shows that the input is a character.

Bit (8:15) contains the received character, the character is right justified, and bit 15 is least significant bit. If the character length is smaller than 8, the most significant bits are zero. If the received character is a break, all characters are zero.

Bit (1). The received character is checked for the same parity as the parity set for the channel. If the channel is in the no parity mode, bit (1) is always zero, else bit (1) is one for wrong parity of the received character.

Bit (2). A logical one in bit (2) means that the received stopbit was logical zero instead of logical one. Bit (2) is always logical one when a break is received. (I/st = Invalid stopbit).

Bit (3). A logical one in this bit means that a break has been received.

3.6.4. The Input Is A Status Word

AC if the input is a status word

0	Modem Status	Not Used	Buffer Status	Undefined
0	1 2 3	4 5 6 7	8 9	10 11 12 13 14 15

Bit (0) = logical zero shows that the input is a status word.

Bit (8) Input Buffer Empty

This status word means that the Input Buffer is empty.

Bit (9) Input Buffer Overrun

This status word means that the Input Buffer has been full and that one or more characters or status words should have been stored in the Input Buffer. The program has been too slow to read the Input Buffer, and an unknown number of characters or status words are lost.

Bit (1) Calling Indicator

This status bit is logical one if the modem Signal Calling Indicator has changed from OFF to ON.

Bit (2) Carrier Off

This status bit is logical one if the modem signal Carrier has changed from ON to OFF.

Bit (3) Data Set Not Ready

This status bit is logical one if the modem signal Data Set Ready has changed from ON to OFF.

Status words containing information concerning bit (1), bit (2), and bit (3) are sent to the input buffer under the following conditions:

1. The modem signal Calling Indicator changes from OFF to ON

2. The modem signal Carrier changes from ON to OFF.

3. When a channel is in Receive-mode or in Transmit-mode and the modem signal Data Set Ready changes from ON to OFF. When Data Set Ready changes from ON to OFF, the Receiving and the Transmission are stopped (see Sections 3.3.1. and 3.3.3.), and this situation is locked in the controller until it is no more in Receive-mode or in Transmit-mode or until a Select Modem Status command arrives (see Section 3.3.5.).

3.7. Interrupt Request

The controller is able to send an Interrupt Request if the Interrupt Disable flag is clear and if the controller has received an Enable Interrupt command. This means that the controller contains three flags, viz.:

Interrupt Request flag
Interrupt Disable flag
Enable Interrupt flag

Interrupt Disable is controlled by mask bit 2 from the program.

The Interrupt Request flag is set to logical one, if Enable Interrupt is logical one and one of these two situations occurs:

1. One of the Input Buffers changes from empty to not empty.
2. One of the Output Buffers changes from not empty to empty.

When the Interrupt Request flag shifts to logical one, it clears the Enable Interrupt flag.

The Interrupt flag is cleared by an instruction with CLEAR modification.

3.8. Data Bus Timing

Caused by the internal structure of the AMX 701 there are some limitations of the program. Some of the commands are not effectuated by the controller during the I/O instruction time, and the program has to wait before a new command is sent to the controller.

The time, the program has to wait before a new instruction:

After IORST	the time is 32	us
- DOB instruction	- - - 6.8	us
- DOC -	- - - 0	us
- DIA -	- - - 0	us
- CLEAR modification	- - - 0	us
- DOA instruction followed by a DIA instruction	- - - 5.6	us
- DOA instruction followed by a DOA, DOB or DOC instruction	- - - 6.8	us