Title:

Technical Manual for 48K Words Upgrade Feature for RC 3601 D Central Unit.

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RCSL No: 44-RT 1386

Edition: January, 1977

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Keywords:

RC3600, RC3602D, Memory Expansion.

Abstract:

This paper contains drawings and description of the modifications which change the central processor RC3601D to RC3602D with 48K word memory.

Printed by A/S Regnecentralen, Copenhagen

CONTENTS Page

General Description

The Nova 2 memory communicates with the processor and the I/O devices via two 16-bit wide data paths, the $\overline{\text{DATA}}$ bus and the $\overline{\text{MAB}}$ bus. The bidirectional $\overline{\text{DATA}}$ bus handles data from and data to the memory while the $\overline{\text{MAB}}$ bus carries the address information to memory. But $\overline{\text{MAB0}}$ is not used for addressing, however, and it is the use of this bit which allows the 48K expansion described below.

The Nova 2 address space is limited to 32K because only 15 bits are available for the physical address to memory ($\overline{\text{MAB1}}$ - $\overline{\text{MAB15}}$). Bit $\overline{\text{MAB0}}$ is used to implement multi-level indirect address references.

If we are willing to use indirect addressing only in the first 32K, we can normally treat $\overline{\text{MAB0}}$ as a sixteenth address bit instead of an indirect bit. In DEFER STATE MAB0 is always logical zero which keeps multi-level indirect addressing in the first 32K. The accumulators used as base registers are both 16 bits wide, and the program counter will count to 64K, provided, of course, that <u>all</u> memory modules in the system will respond to $\overline{\text{MAB0}}$.

This modification is limited to 48K memory because we have only 3 slots to use for the 16K memory modules.

Modification in Central Processor

The modification supplies the central processor with a driver for the $\overline{MAB0}$ signal, and a switch which eliminates the memory extension.

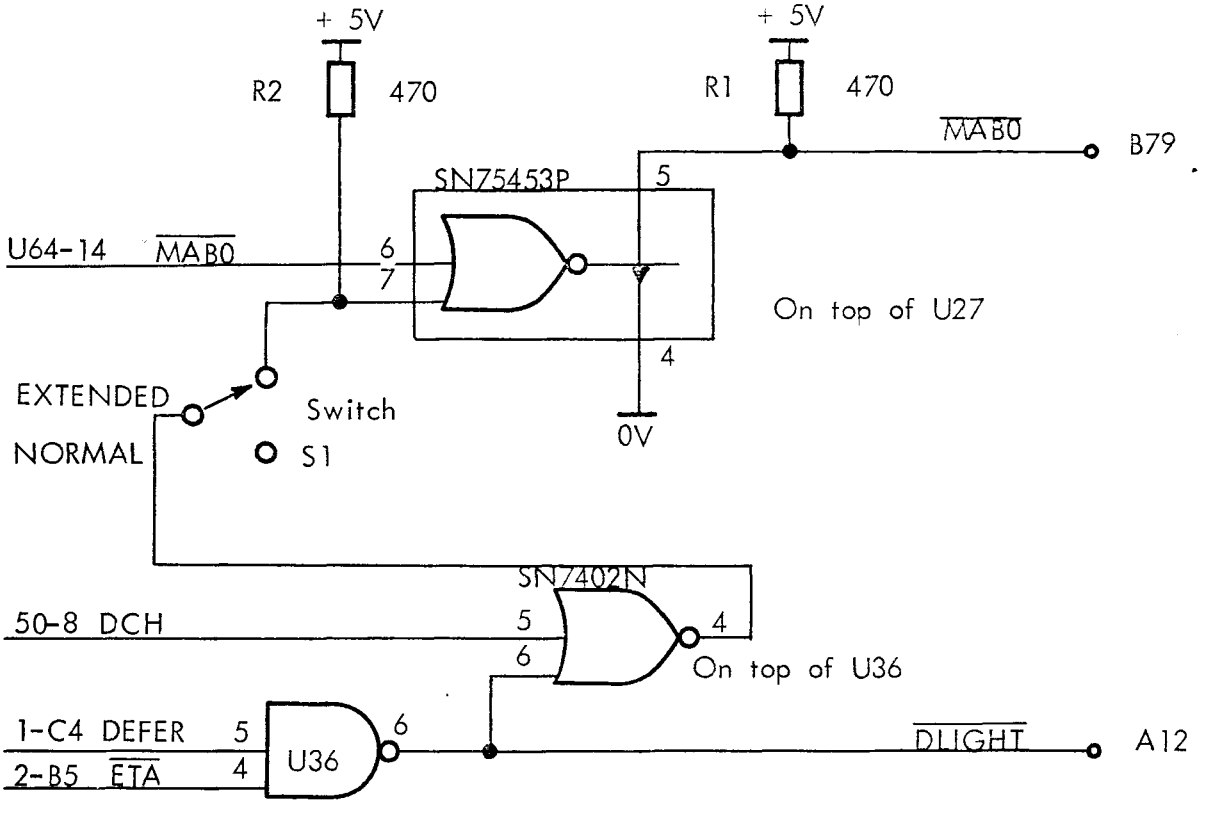


Fig. 1.1 Circuit diagram for driver for $\overline{MAB0}$

Modification in Memory

This modification makes the Memory DR124F respond to $\overline{MA80}$.

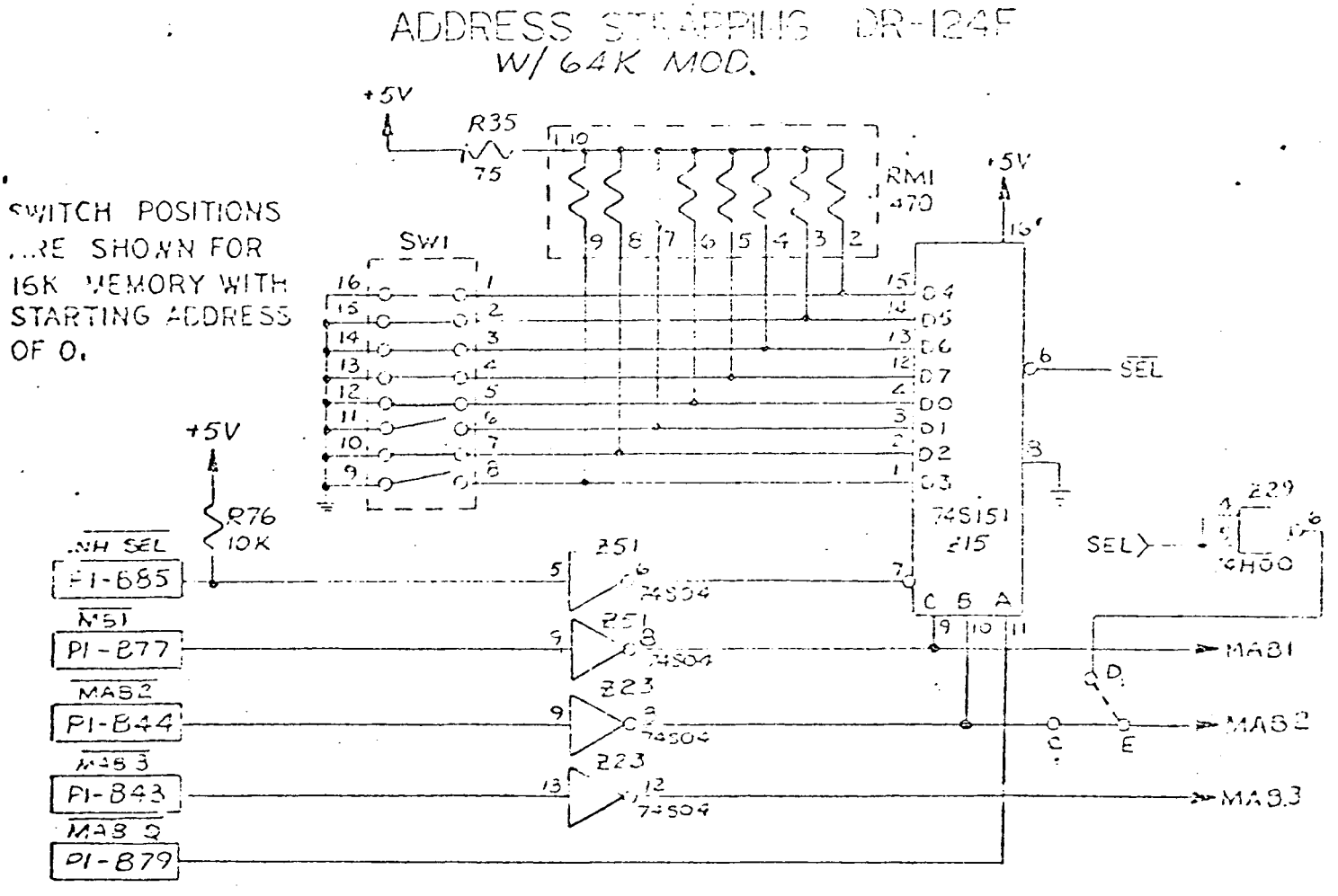


Fig. 2.: Circuit diagram with modification making the DR124F memory respond to MA80. The Diagram is to be used as Schematic Diagram Sheet 2 of 7 in the technical manual for DR124F.

Address switches on the memory modul is to be made accordance with fig. 3.

16K

ADDRESS ASSIGNMENT	SW1 SWITCH NUMBERS							
	1	2	3	4	5	6	7	8
0-16K	X	X	X	X	X		X	
8-24K	X		X	X	X	X	X	
16-32K	X		X		X	X	X	X
24-40K	X	X	X			X	X	X
32-48K	X	X	X	X		X		X
40-56K		X	X	X	X	X		X
48-64K		X		X	X	X	X	X

X = ON OR CLOSED

Fig. 3. Switch setting table

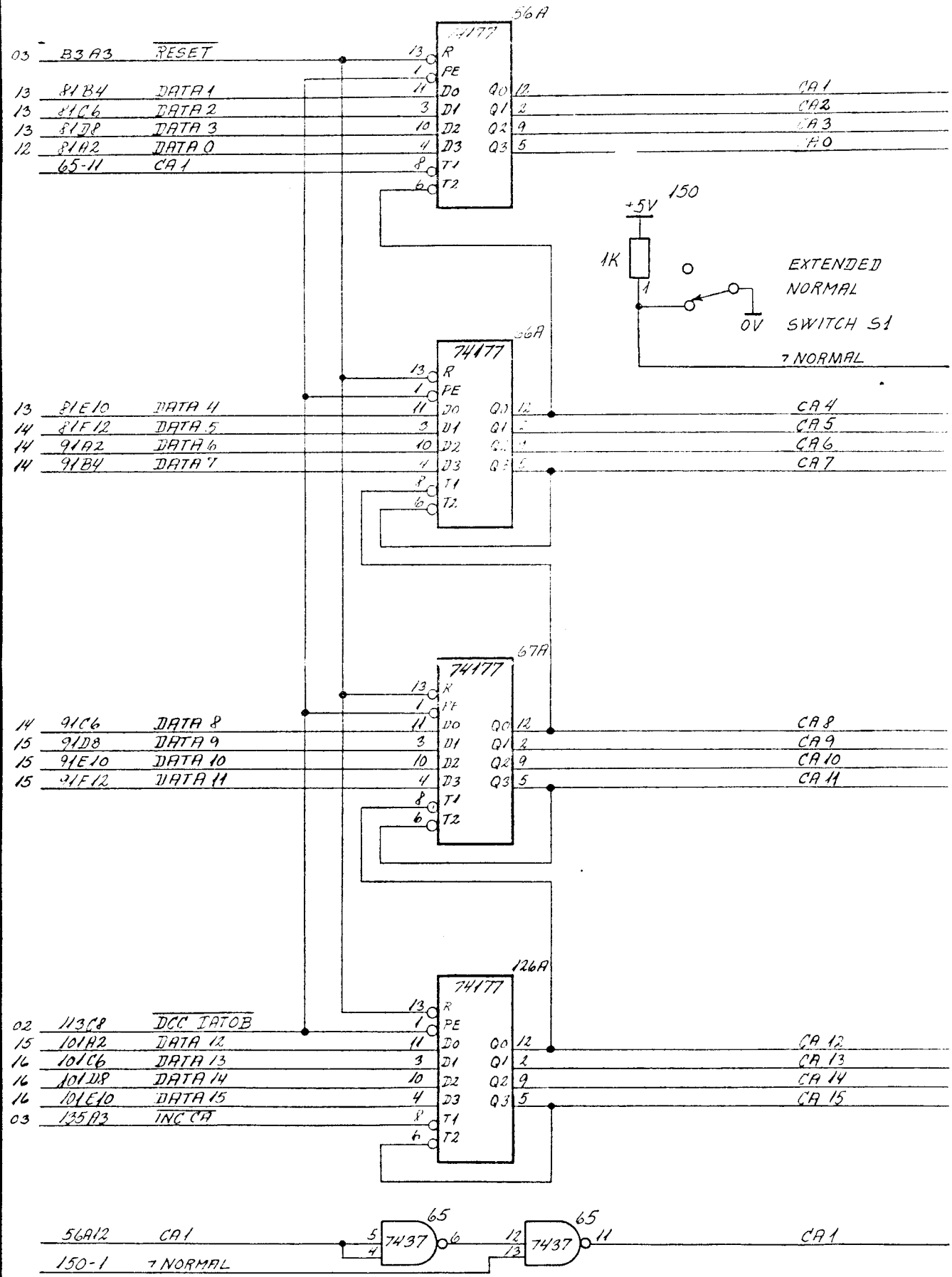
E.g. for 16 K memory with starting address of 0 turn switches 1,2,3,4,5 and 7 'on' or 'closed'.

Modification in Disc Controller DCC701

This modification changes the core address register from a 15-bit register/counter to a 16-bit register/counter.

The switch is used to force the CA0 output to logical zero when using the Testprogram.

Page 6 shows the new Logic Diagram for DCC701 page 09.



Unit	DCC 701
Dwg. No.	

COVE ADDRESS REGISTERS

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Designed by UFL HARTS TY | Drawn by | Dwg. Office Check | Design Check | Replaces Dwg. No. | due to ECN | Replaced by Dwg. No.

RC doc V8.140

Test of Equipment

Immediately on installation the memory extension can be tested from the switches on the front panel.

With the switch on the CPU board (page 2) in extended position, test that you can examine and deposit in all of the three memories and that the memory area from 48K to 64K does not exist.

Note: Many of the test programs for RC3600 will not run correctly with the switch in extended position. To test the memory with address from 32K to 48K you have to change address switches from 0K to 16K or 16K to 32K.