```
0001 .MAIN MACRO REV 02                19:31:17 07/20/78
01              ;
02
03
04
05
06                      p.n.99109232
07              ;       RCSL:   44-RT 1714
08
09              ;       VERSION:        15.05.78        JEP
10
11              ;               PROGRAM
12              ;               *******
13
14              ;       RC 3600 - CPU  LOGIC  TEST.
15
16              ;               PROGRAM SOURCE
17
18              ;       S-BINARY TAPE:  RCSL 44-RT 1715 (SELFSTART AUTOLOAD HEAD)
19              ;       ASCII SOURCE:   RCSL 44-RT 1716 TAPE 1 - 6
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44              ;0. INDEX
45              ;       1. ABSTRACT             PAGE 1
46              ;       2. MACHINE REQUIREMENTS PAGE 1
47              ;       3. THE TEST             PAGE 2
48
49              ;1. ABSTRACT
50              ;       THE CPU LOGIC TEST IS A LOW LEVEL MAINTENANCE PROCEDURE
51              ;       FOR DGC NOVA 2 CPU AND RC 3603 CPU 708.
52
53              ;2. MACHINE REQUIREMENTS
54              ;       CPU UNDER TEST          CPU
55              ;       32K WORDS MEMORY        MEM     (NOVA 2 MIN 4K)
56              ;       MAIN CONSOLE            TTY
57              ;       PAPER TAPE READER       PTR
58              ;       REAL TIME CLOCK         RTC
59              ;       (PAPER TAPE PUNCH       PTP)
60              ;       PROGRAM LOAD OPTION     ROM     (F01)
```

```
0002 .MAIN
01              ;3. THE TEST
02
03
04              ;       ************************************************
05              ;       *                                              *
06              ;       *       CPU 708  TROUBLESHOOTING / TEST        *
07              ;       *                                              *
08              ;       ************************************************
09
10
11              ;       SUGGESTED METHOD TO TROUBLESHOOT THE CPU 708.
12
13              ;       $$$$    TOOLS AND DOCUMENTS:
14
15              ;               LOGIC ANALYZER (OR OSCILLOSCOPE)
16              ;               TCP 701 DIAGNOSTIC PANEL
17              ;               CPU 708 TECHNICAL MANUAL
18
19              ;       $$$$    WHERE TO START:
20
21              ;               DEPENDS OF THE NATURE OF ERROR / TEST.
22              ;               IF IT IS POSSIBLE TO READ IN THE BINARY TAPE
23              ;               CONTAINING LOGIC TEST, DO THIS AND START THE
24              ;               PROGRAM. IF NOT POSSIBLE GO TO THE PRIMITIVE
25              ;               PART OF THIS TEST AND FOLLOW THE INSTRUCTIONS
26              ;               FOR STATIC TEST.
27
28
29              ;               1:      CPU 708 STATIC TEST     PAGE 3
30
31              ;               3:      LOGIC TEST              PAGE 59
32
33
34
35              ;       ************************************************
36              ;       *                                              *
37              ;       *       NOVA 2 TROUBLESHOOTING / TEST          *
38              ;       *                                              *
39              ;       ************************************************
40
41
42              ;       SUGGESTED METHOD TO TROUBLESHOOT THE NOVA 2 CPU.
43
44              ;       $$$$    TOOLS AND DOCUMENTS:
45
46              ;               OSCILLOSCOPE (OR LOGIC ANALYZER)
47              ;               NOVA 2 TECHNICAL MANUAL
48
49              ;       $$$$    WHERE TO START:
50
51              ;               DEPENDS OF THE NATURE OF ERROR / TEST.
52              ;               IF IT IS POSSIBLE TO READ IN THE BINARY TAPE
53              ;               CONTAINING LOGIC TEST, DO THIS AND START THE
54              ;               PROGRAM. IF NOT POSSIBLE GO TO THE PRIMITIVE
55              ;               PART OF THIS TEST AND FOLLOW THE INSTRUCTIONS
56              ;               FOR STATIC TEST.
57
58              ;               2:      NOVA 2 STATIC TEST      PAGE 58
59
60              ;               3:      LOGIC TEST              PAGE 59
```

```
0003 .MAIN
01
02
03
04
05
06              ;          *     ****************************************
07              ;         **     ***                                  ***
08              ;          *     ***    1:  CPU 708  STATIC TEST      ***
09              ;          *     ***                                  ***
10              ;        ****    ****************************************
11
12
13              ;       THIS PART IS USED TO TEST THE FRONT PANEL (DIAGN. PANEL)
14
15              ;       OPERATIONS (TCP 701 = EXAMINE, DEPOSIT ETC AND THE SMALL
16
17              ;       PANEL ON THE FRONT EDGE OF THE CPU PCBA), A FEW SIMPLE
18
19              ;       INSTRUCTIONS AND THE NESSACARY HARDWARE TO READ BINARY
20
21              ;       TAPES FROM THE PTR.
22
23              ;       IT IS A STEP BY STEP TEST WITH A LOT OF INFORMATION
24
25              ;       SUGGESTING WHAT TO DO IF A PARTICULAR STEP IS NOT
26
27              ;       WORKING.
28
29              ;       THE INFORMATION CONSISTS OF:
30
31              ;          A    CHECK PROCEDURE                  PAGE 4
32
33              ;          B    MESSURING METHOD                 PAGE 12
34
35              ;          C    SIGNAL LISTS FOR EACH STEP       PAGE 16
36
37              ;          D    BUS SYSTEM BLOCK SCHEME.         PAGE 27
38
39              ;          E    MIKROSTEP COMMANDS LIST, BUS     PAGE 29
40
41              ;          F    PULS SCHEMES FOR MEMORY CONTROL  PAGE 43
42
43              ;          G    INSTRUCTION MIKROSTEP FLOW /
44              ;                        TIME CONSUMPTION       PAGE 46
45
46              ;          H    ROM TYPE / POSITION LIST         PAGE 54
47
48              ;          I    MIKROPROGRAM MAIN PRIORITY       PAGE 56
```

```
10004 .MAIN
01
02
03
04
05
06                ;            **      ****************************************
07                ;          *  *      *                                      *
08                ;          ****      *   A:   CPU 708  CHECK PROCEDURE      *
09                ;          *  *      *                                      *
10                ;          *  *      ****************************************
11
12
13                ;       0.       CHECK POWER OK INDICATOR ON POWER PANEL
14                ;                (AUTOLOAD PANEL) AND ON EACH CHS (CHASSIS)
15                ;                INVOLVED IN THE SYSTEM.
16
17
18                ;       1.       SET THE BREAK SWITCH IN POSITION OFF.
19                ;                PRESS RESET. THE CPU NOW LOOPS IN MIKROPROGRAM
20                ;                ADDRESS 126, 127.
21                ;                CHECK MIKROPROGRAM LED INDICATORS ON TCP 701
22                ;                (MIKAD LED) SHOWING 127, RUN INDICATOR OFF.
23
24                ;       (1.)     IF ERRORS, CONSULT SIGNAL CHECK LIST 1.
25
26
27                ;       2.       DEPOSIT 000000 IN REGISTER AC 1,3,5,7,9,11,13,15.
28                ;                CHECK    MIKAD LED = 127
29                ;                         DATA  LED = 000000
30
31
32                ;       3.       DEPOSIT 177777 IN REGISTER AC 0,2,4,6,8,10,12,14.
33                ;                CHECK    MIKAD LED = 127
34                ;                         DATA LED  = 177777
35
36                ;       (2,3,)   IF ERRORS CONSULT SIGNAL CHECK LIST 2.
37
38
39                ;       4.       EXAMINE REGISTER AC 0,1,2,3,4,5,6,7,8,9,10...,15.
40                ;                CHECK    MIKAD LED = 127
41                ;                         DATA  LED = ALTERNATING 000000 AND 177777
42
43                ;       (4.)     IF ERRORS CONSULT SIGNAL CHECK LIST 3.
44
45
46                ;       5.       DEPOSIT 000000 IN AC 0,2,4,6,8,10,12,14.
47                ;                CHECK    MIKAD LED = 127
48                ;                         DATA  LED = 000000
49
50
51                ;       6.       DEPOSIT 177777 IN AC 1,3,5,7,9,11,13,15.
52                ;                CHECK    MIKAD LED = 127
53                ;                         DATA  LED = 177777
54
55
56                ;       7.       EXAMINE AC 0,1,2,3,4,5,6,7....15.
57                ;                CHECK    MIKAD LED = 127
58                ;                         DATA  LED = ALTERNATING 177777 AND 000000
59
60                ;       (5,6,7)  IF ERRORS CONSULT SIGNAL CHECK LIST 2 AND 3.
```

```
0005 .MAIN
31
32                ;       8.      DEPOSIT FLOATING 1 IN AC 0 - 15, I. E.
33                ;               BIT 15 IN AC0, BIT 14 IN AC1 ETC.
34                ;               CHECK   MIKAD LED = 127
35                ;                       DATA  LED = AC CONTENT
36
37                ;       9.      EXAMINE THE FLOATING 1 IN AC 0 - 15.
38                ;               CHECK   MIKAD LED = 127
39                ;                       DATA  LED = AC CONTENT
10
11                ;       (8,9,)  IF ERRORS CONSULT SIGNAL CHECK LIST 2 AND 3.
12
13
14                ;       10.     DEPOSIT AND THEN EXAMINE 177777 IN
15                ;               MEMORY LOCATION 0:
16                ;               SET SWITCHES RESET AND STOP PARITY ERROR UP
17                ;               (PASSIVE).
18                ;               CHECK                   MIKAD LED       DATA LED
19                ;               RESET                   127             X
20                ;               DATA SWITCHES:= 0
21                ;               EXAMINE                 127             X
22                ;               DATA SWITCHES:= 177777
23                ;               DEPOSIT                 127             177777
24                ;               DATA SWITCHES:= 0
25                ;               EXAMINE                 127             177777
26                ;               EXAMINE AC4 (PC)        127             000000
27                ;               POINTING AT LOCATION 0.
28
29                ;       11.     DEPOSIT AND THEN EXAMINE 000000 IN
30                ;               MEMORY LOCATION 0:
31                ;               CHECK                   MIKAD LED       DATA LED
32                ;               RESET                   127             X
33                ;               DATA SWITCHES:= 0
34                ;               EXAMINE                 127             X
35                ;               DEPOSIT                 127             000000
36                ;               EXAMINE                 127             000000
37
38                ;       (10,11) IF ERRORS CONSULT SIGNAL CHECK LIST 4.
39
40
41                ;       12.     PRESS START  (MEM LOC 0 = 000000 = JMP 0)
42                ;               CHECK   MIKAD LED       = 3
43                ;                       RUN INDICATOR   = 1
44                ;                       FETCH INDI      = 1
45                ;                       DEFER INDI      = 0
46                ;                       ION INDI        = 0
47                ;                       DATA LED        = 000000
48
49                ;       (12,)   IF ERRORS CONSULT SIGNAL CHECK LIST 5.
50
51
52                ;       13.     PRESS RESET.
53                ;               CHECK   MIKAD LED       = 127
54                ;                       RUN INDICATOR   = 0
55                ;                       FETCH INDI      = 0
56                ;                       DEFER INDI      = 0
57                ;                       ION INDI        = 0
58                ;                       DATA LED        = 000000
59
60                ;       (13,)   IF ERRORS CONSULT SIGNAL CHECK LIST XX
```

```
0006 .MAIN
01
02
03                ;       14.     PRESS START  (MEM LOC 0 = 000000 = JMP 0).
04                ;               CHECK AS IN 12.
05
06
07                ;       15.     PRESS STOP.
08                ;               CHECK AS IN 13.
09
10
11                ;       16.     DEPOSIT 037777 IN AC4 (PC).
12                ;               DEPOSIT NEXT, EXAMINE AC4 SEVERAL TIMES AND
13                ;               CHECK THAT PC INCREMENTS.
14
15                ;       (16.)   IF ERRORS CONSULT SIGNAL CHECK LIST XY.
16
17
18                ;       17.     DEPOSIT 000000 IN AC4 (PC).
19                ;               EXAMINE NEXT, EXAMINE AC4 SEVERAL TIMES AND
20                ;               CHECK THAT PC INCREMENTS.
21
22                ;       (17.)   IF ERRORS CONSULT SIGNAL CHECK LIST XZ.
23
24
25                ;       18.     DEPOSIT 000002 IN AC 5 (BREAK LOC)
26                ;                       063077 IN AC 6 (BREAK INSTR)
27                ;               (EXAMINE LOC 0)
28                ;               DEPOSIT 000001 IN LOC 0 ( JMP 1 )
29                ;               (NEXT)  000002 IN LOC 1 ( JMP 2 )
30                ;                       000003 IN LOC 2 ( JMP 3 )
31                ;                       000000 IN LOC 3 ( JMP 0 )
32                ;               PRESS START
33                ;               CHECK   MIKAD LED       = 3
34                ;                       RUN INDICATOR   = 1
35                ;                       FETCH INDI      = 1
36                ;                       DATA LED        = 000003
37
38                ;       (18.)   IF ERRORS CONSULT SIGNAL CHECK LIST YX.
39
40
41                ;       19.     SET THE BREAK SWITCH IN POSITION ON.
42                ;               CHECK   MIKAD LED       = 127
43                ;                       RUN INDICATOR   = 0
44                ;                       FETCH INDI      = 0
45                ;                       DATA LED        = 063077
46
47                ;       (19.)   IF ERRORS CONSULT SIGNAL CHECK LIST YY.
48
49
50                ;       20.     EXAMINE AC 4 (PC), ADDR+1 OF BREAK.
51                ;               CHECK   MIKAD LED       = 127
52                ;                       DATA LED        = 000003
53
54                ;       (20.)   IF ERRORS CONSULT SIGNAL CHECK LIST YZ.
```

```
!0007 .MAIN
01
02              ;       21.     SMALL ALU TEST (SWAP TEST).
03              ;               SET BREAK SWITCH IN POSITION OFF.
04              ;               DEPOSIT 000000 IN AC1   (START DATA)
05              ;               (EXAMINE LOC 0)
06              ;               DEPOSIT 131300 IN LOC 0 (MOVS 1,2)
07              ;               (NEXT)  155300 IN LOC 1 (MOVS 2,3)
08              ;                       136434 IN LOC 2 (SUBZ# 1,3,SZR)
09              ;                       063077 IN LOC 3 (HALT)
10              ;                       125400 IN LOC 4 (INC 1,1)
11              ;                       000000 IN LOC 5 (JMP 0 )
12              ;               DEPOSIT 000000 IN AC4   (PC, START ADDR)
13              ;               SET DATA SWITCHES:= 000003
14              ;               PRESS CONTINUE
15              ;               CHECK   MIKAD LED       = 377
16              ;                       RUN INDICATOR   = 1
17              ;                       ION INDI        = 0
18              ;                       CARRY INDI      = ALTERNATING 0 - 1 WITH
19              ;                                         A FREKVENS OF 1 HZ.
20              ;                       FETCH INDI      = 1
21              ;                       DEFER INDI      = 0
22              ;                       DATA LED        = 177777
23
24              ;       (21.)   IF ERRORS CONSULT SIGNAL CHECK LIST ZX.
25
26
27              ;       22.     SMALL STA INSTR TEST.
28              ;               DEPOSIT 125252 IN AC0
29              ;               (EXAMINE LOC 0)
30              ;               DEPOSIT 040002 IN LOC 0 (STA 0,2)
31              ;               (NEXT)  000000 IN LOC 1 (JMP 0)
32              ;               PRESS START
33              ;               CHECK   MIKAD LED       = 277
34              ;                       RUN INDICATOR   = 1
35              ;                       DATA LED        = 165252
36              ;               PRESS STOP
37              ;               EXAMINE LOC 2, DATA LED = 125252
38
39              ;       (22.)   IF ERRORS CONSULT SIGNAL CHECK LIST ZY.
40
41
42              ;       23.     SMALL LDA INSTR TEST.
43              ;               (EXAMINE LOC 0)
44              ;               DEPOSIT 034002 IN LOC 0 (LDA 3,2)
45              ;               (NEXT)  000000 IN LOC 1 (JMP 0)
46              ;               PRESS START
47              ;               CHECK   MIKAD LED       = 237
48              ;                       RUN INDICATOR   = 1
49              ;                       DATA LED        = 034002
50              ;               PRESS STOP
51              ;               EXAMINE AC3, DATA LED   = 125252
52
53              ;       (23.)   IF ERRORS CONSULT SIGNAL CHECK LIST ZZ.
54
55              ;       24.     SMALL STA INSTR TEST.
56              ;               AS 22. BUT DATAPATTERN 052525 AND
57              ;               DATA LED = 052527 WHEN RUNNING.
58
59              ;       25.     SMALL LDA INSTR TEST.
60              ;               AS 23. BUT DATAPATTERN 052525.
```

```
0008 .MAIN
01
02
03                ;       26.     DEFER INDICATOR TEST.
04                ;               (EXAMINE LOC 0)
05                ;               DEPOSIT 022002 IN LOC 0 (LDA 0,@2)
06                ;               (NEXT)  063077 IN LOC 1 (HALT)
07                ;                       100003 IN LOC 2 (@3)
08                ;                       100002 IN LOC 3 (@2)
09                ;                       000000 IN LOC 4 (JMP 0)
10                ;               PRESS START
11                ;               CHECK   MIKAD LED       = 036
12                ;                       RUN INDICATOR   = 1
13                ;                       FETCH INDI      = 0
14                ;                       DEFER INDI      = 1
15                ;                       DATA LED        = 100003
16                ;               PRESS STOP
17                ;               CHECK   MIKAD LED       = 036
18                ;                       RUN INDICATOR   = 0
19                ;                       FETCH INDI      = 0
20                ;                       DEFER INDI      = 1
21                ;               PRESS RESET
22                ;               CHECK   MIKAD LED       = 127
23                ;                       RUN INDICATOR   = 0
24                ;                       FETCH INDI      = 0
25                ;                       DEFER INDI      = 0
26
27                ;       (26.)   IF ERRORS CONSULT SIGNAL CHECK LIST XX.
28
29
30                ;       27.     RESET MEMORY PARITY PROGRAM.
31                ;               OBSERVE THE STATE OF THE CARRY INDICATOR.
32                ;               SET THE SWITCH 64K/128K IN 128K POSITION.
33                ;               DEPOSIT 063077 IN AC1   (DATA, HALT)
34                ;                       000004 IN AC3   (START ADDR)
35                ;               (EXAMINE LOC 0)
36                ;               DEPOSIT 072701 IN LOC 0 (DICP 2,1)
37                ;               (NEXT)  045400 IN LOC 1 (STA 1,0,3)
38                ;                       175400 IN LOC 2 (INC 3,3)
39                ;                       000000 IN LOC 3 (JMP 0)
40                ;               PRESS START
41                ;               THE RUN INDICATOR LIGHTS FOR ABOUT 1 SECOND. THEN
42                ;               CHECK   MIKAD LED       = 127
43                ;                       RUN INDICATOR   = 0
44                ;                       CARRY INDI      = THE OPPOSIT VALUE OF
45                ;                                         THE START OBSERVATION
46                ;                       DATA LED        = 063077
47                ;               EXAMINE AC4, DATA LED   = 1
48                ;               EXAMINE AC3, DATA LED   = 1
49                ;               IF REPEATED, AC3 + LOC 0 SHOULD BE REETABLISHED.
50                ;       (27.)   IF ERRORS CONSULT SIGNAL CHECK LIST XY.
```

```
10009 .MAIN
01
02
03                ;       28.     CHECK MEMORY PARITY PROGRAM.
04                ;               SET THE SWITCH STOP ON PARITYERROR DOWN (ACTIVE).
05                ;               DEPOSIT 063077 IN AC1   (HALT)
06                ;                       000004 IN AC3   (START ADDR)
07                ;               (EXAMINE LOC 0)
08                ;               DEPOSIT 072701 IN LOC 0 (DICP 2,1)
09                ;               (NEXT)  025400 IN LOC 1 (LDA 1,0,3)
10                ;                       175400 IN LOC 2 (INC 3,3)
11                ;                       000000 IN LOC 3 (JMP 0)
12                ;               PRESS START
13                ;               THE RUN INDICATOR LIGHTS FOR ABOUT 1 SECOND, THEN
14                ;               CHECK   PARITY ERROR INDICATOR LEFT, RIGHT = 0
15                ;                       MIKAD LED       = 127
16                ;                       RUN INDICATOR   = 0
17                ;                       DATA LED        = 063077
18                ;               EXAMINE AC4, DATA LED   = 1
19                ;               EXAMINE AC3, DATA LED   = 1
20                ;               IF REPEATED, AC3 + LOC 0 SHOULD BE REETABLISHED.
21                ;       (28,)   IF ERRORS, CONSULT SIGNAL CHECK LIST XZ.
22
23
24                ;       29.     SMALL RELATIVE ADDRESSSING AND MAR TEST.
25                ;               EXAMINE LOC 000052)
26                ;               DEPOSIT 000653 IN LOC 52        (JMP .-125)
27                ;               (EXAMINE LOC 077725)
28                ;               DEPOSIT 000525 IN LOC 77725     (JMP .+125)
29                ;               EXAMINE LOC 000052
30                ;               PRESS START
31                ;               CHECK   MIKAD LED       = 3
32                ;                       RUN INDICATOR   = 1
33                ;                       FETCH INDI      = 1
34                ;                       DATA LED        = 000777
35                ;       (29,)   IF ERRORS, CONSULT SIGNAL CHECK LIST YX.
36
37
38                ;       30.     SMALL TEST OF DIA WITHOUT SKP (READS)
39                ;               (EXAMINE LOC 0)
40                ;               DEPOSIT 060477 IN LOC 0 (DIA 0,CPU - READS 0)
41                ;               (NEXT)  000000 IN LOC 1 (JMP 0)
42                ;               PRESS START
43                ;               CHECK   MIKAD LED       = 177
44                ;                       RUN INDICATOR   = 1
45                ;                       DATA LED        = 060477
46                ;               RAISE AND LOWER ALL DATA SWITCHES AND
47                ;               CHECK   DATA LED        = SWITCH REACTION
48                ;               PRESS STOP
49                ;               EXAMINE AC0, DATA LED   = LAST DATA SWITCH STATE
50                ;       (30,)   IF ERRORS, CONSULT SIGNAL CHECK LIST YY.
```

```
;0010 .MAIN
01
02
03              ;       31.     SMALL TEST OF SKIP BUSY AND LEFT SHIFT USING RTC.
04              ;               DEPOSIT 000001 IN AC0   (RTC F = 10 HZ)
05              ;               (EXAMINE LOC 0)
06              ;               DEPOSIT 061014 IN LOC 0 (DOA 0,RTC)
07              ;               (NEXT)  060114 IN LOC 1 (NIOS RTC)
08              ;                       101000 IN LOC 2 (MOV 0,0)
09              ;                       063514 IN LOC 3 (SKPBZ RTC)
10              ;                       000002 IN LOC 4 (JMP 2)
11              ;                       101100 IN LOC 5 (MOVL 0,0)
12              ;                       000001 IN LOC 6 (JMP 1)
13              ;                       000000 IN LOC 7 (JMP 0)
14              ;               PRESS START
15              ;               CHECK   MIKAD LED       = 377
16              ;                       RUN INDICATOR   = 1
17              ;                       DATA + CARRY LED= LEFT MOVING "1"
18              ;                                         ONE PASS = 1,7 SEC
19              ;                       IF EACH LED IS CHECKED SEPARATELY IT IS
20              ;                       POSSIBLE TO SEE A LUMINANCE INCREASE
21              ;                       EVEN IN LEDS WITH LIGHT.
22              ;       (31,)   IF ERRORS CONSULT SIGNAL CHECK LIST YZ.
23
24              ;       32.     SMALL TEST OF SKIP DONE + RIGHT SHIFT USING RTC.
25              ;               DEPOSIT 000001 IN AC0   (RTC F = 10 HZ)
26              ;               (EXAMINE LOC 0)
27              ;               DEPOSIT 061014 IN LOC 0 (DOA 0,RTC)
28              ;               (NEXT)  060114 IN LOC 1 (NIOS RTC)
29              ;                       101000 IN LOC 2 (MOV 0,0)
30              ;                       063614 IN LOC 3 (SKPDN RTC)
31              ;                       000002 IN LOC 4 (JMP 2)
32              ;                       101200 IN LOC 5 (MOVR 0,0)
33              ;                       000001 IN LOC 6 (JMP 1)
34              ;                       000000 IN LOC 7 (JMP 0)
35              ;               PRESS START
36              ;               CHECK   MIKAD   = 377
37              ;                       RUN INDICATOR   = 1
38              ;                       DATA + CARRY LED= RIGHT MOVING "1"
39              ;                                         ONE PASS = 1,7 SEC
40              ;                       IF EACH LED IS CHECKED SEPARATELY IT IS
41              ;                       POSSIBLE TO SEE A LUMINANCE INCREASE
42              ;                       EVEN IN LEDS WITH LIGHT.
43              ;       (32,)   IF ERRORS CONSULT SIGNAL CHECK LIST ZX.
44
45              ;       33.     SMALL TEST OF TTO, INCREASING CHAR=VALUE.
46              ;               DEPOSIT 000000 IN AC0   (START DATA)
47              ;               (EXAMINE LOC 0)
48              ;               DEPOSIT 061011 IN LOC 0 (DOA 0,TTO ;STARTS XMIT)
49              ;               (NEXT)  060111 IN LOC 1 (NIOS TT0 ;SETS BUSY)
50              ;                       063511 IN LOC 2 (SKPBZ TT0)
51              ;                       000777 IN LOC 3 (JMP .-1)
52              ;                       101400 IN LOC 4 (INC 0,0 ;NEXT CHAR)
53              ;                       000000 IN LOC 5 (JMP 0)
54              ;               PRESS RESET, START
55              ;               CHECK   MIKAD LED       = 377
56              ;                       RUN INDICATOR   = 1
57              ;                       DATA LED        = 063777
58              ;                       TTO WRITING
59              ;                       !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJK.....
60              ;       (33,) IF ERRORS CONSULT SIGNAL CHECK LIST ZY.
```

```
 0011 .MAIN
01
02                ;       34.     SMALL TEST OF TTI, ECHO TEST.
03                ;               DEPOSIT 000012 IN AC0   (INITIALIZE CHAR = LF)
04                ;               (EXAMINE LOC 0)
05                ;               DEPOSIT 061011 IN LOC 0 (DOA 0,TTO)
06                ;               (NEXT)  060111 IN LOC 1 (NIOS TTO)
07                ;                       063511 IN LOC 2 (SKPBZ TTO)
08                ;                       000777 IN LOC 3 (JMP .-1)
09                ;                       063610 IN LOC 4 (SKPDN TTI)
10                ;                       000777 IN LOC 5 (JMP .-1)
11                ;                       060410 IN LOC 6 (DIA 0,TTI)
12                ;                       060110 IN LOC 7 (NIOS TTI ;CLEAR DONE)
13                ;                       000000 IN LOC 8 (JMP 0)
14                ;               PRESS RESET, START
15                ;               CHECK   MIKAD LED       = 377
16                ;                       RUN INDICATOR   = 1
17                ;                       DATA LED        = 063777
18                ;                       TTO WRITING LINEFEED
19                ;               TYPE DIFFERENT CHARS AND OBSERVE THE ECHO OUTPUT.
20                ;       (34.)   IF ERRORS CONSULT SIGNAL CHECK LIST ZZ.
21
22                ;       35.     PUNCH TEST TAPE PROGRAM.
23                ;               PUNCHES ALTERNATING ALL 1 AND ALL 0 CHARS.
24                ;               THE TAPE IS USED FOR MAKING AN ENDLESS
25                ;               LOOP FOR PAPER TAPE READER TEST.
26                ;
27                ;               DEPOSIT 000377 IN AC0   (DATA, 2 BYTES)
28                ;               (EXAMINE LOC 0)
29                ;               DEPOSIT 061013 IN LOC 0 (DOA 0,PTP)
30                ;               (NEXT)  060113 IN LOC 1 (NIOS PTP)
31                ;                       063513 IN LOC 2 (SKPBZ PTP)
32                ;                       000777 IN LOC 3 (JMP .-1)
33                ;                       101300 IN LOC 4 (MOVS 0,0)
34                ;                       000000 IN LOC 5 (JMP 0)
35                ;               PRESS RESET, START
36                ;               CHECK   MIKAD LED       = 377
37                ;                       RUN INDICATOR   = 1
38                ;                       DATA LED        = 063777
39                ;                       PUNCHING ABOUT MENTIONED TAPE.
40                ;       (35.)   IF ERRORS, CONSULT SIGNAL CHECK LIST XX.
41
42                ;       36.     SMALL TEST OF PTR.
43                ;               PUT AN ENDLESS LOOP OF TAPE IN THE READER
44                ;               WITH ALTERNATING DATA OF ALL 1 AND ALL 0.
45                ;               (EXAMINE LOC 0)
46                ;               DEPOSIT 060112 IN LOC 0 (NIOS PTR)
47                ;               (NEXT)  063512 IN LOC 1 (SKPBZ PTR)
48                ;                       000777 IN LOC 2 (JMP .-1)
49                ;                       060412 IN LOC 3 (DIA 0,PTR)
50                ;                       000000 IN LOC 4 (JMP 0)
51                ;               PRESS RESET, START
52                ;               CHECK   MIKAD LED       = 377
53                ;                       RUN INDICATOR   = 1
54                ;                       DATA LED        = 063777
55                ;               PRESS STOP, CONTINUE SEVERAL TIMES AND
56                ;               EXAMINE AC0 WHEN STOPPED,
57                ;                       DATA LED        = 000000 OR 000377
58                ;       (36.)   IF ERRORS, CONSULT SIGNAL CHECK LIST XY.
59
60                ;       37.     GO TO 31 LOGIC TEST, PAGE 59.
```

```
0012 .MAIN
01
02
03
04                ;          ***     ****************************************
05                ;          *  *    *                                      *
06                ;          ***     *   B:   CPU 708  MESSURING METHODS    *
07                ;          *  *    *                                      *
08                ;          ***     ****************************************
09
10
11                ;     A:       NO RETURN TO MIKROADDRESS 127 AFTER A TCP COMMAND
12                ;              OR NOT SHOWING THE CORRECT LOGICAL OR OF ALL
13                ;              MIKROSTEPS IN THE INSTRUCTION LOOPS.
14
15                ;     B:       NOT CORRECT EFFECTUATION (DATA, LED INDICATORS)
16                ;              OF TCP COMMAND OR INSTRUCTIONS, DUE TO NOT
17                ;              CORRECT FLOW IN MIKROPROGRAM.
18
19                ;     C:       NOT CORRECT EFFECTUATION (DATA, LED INDICATORS)
20                ;              OF TCP COMMAND OR INSTRUCTIONS, DUE TO BAD
21                ;              CONTROL OR DATA SIGNALS.
22
23
24
25                ;     A.       IF MIKROADDRESS LED IS NOT SHOWING THE LOGICAL
26                ;              OR OF ALL MIKROSTEPS IN THE INSTRUCTION LOOP OR
27                ;              IF NOT RETURNING TO MIKROADDRESS 127 AFTER RESET
28                ;              EXAMINE, DEPOSIT ETC CHECK FOLLOWING:
29
30                ;        A1.   IS RAR CLK RUNNING ?  CPU 040, 40-3
31
32                ;        A2.   IS -STOP CLOCK TRUE ?  CPU 019, 77-6
33                ;              ELSE THE MEMORY AND MEMORY INTERFACE CIRCUITS
34                ;              SHOULD BE CHECKED. (E: PULS SCHEMES)
35
36                ;        A3.   IF TCP COMMAND: IS THERE ANY REACTION ON THE
37                ;              STROBE SIGNAL FROM TCP ?  CPU 035, 19-9 AND
38                ;              INPUT/OUTPUT SIGNALS ON IC 19.
39
40                ;        A4.   IS THE SIGNALS FROM SIGNAL CHECK LIST TOGGLING
41                ;              OR AT CORRECT TTL LEVEL (NOT ZERO OR +5 VOLT) ?
42                ;              PERHAPS THEY SHOULD BE CONTROLLED FROM THE BOTTOM
43                ;              OF THE LIST AND UP. IF CONTROL SIGNALS FOR ROMS I
44                ;              OKAY, TRY WITH OTHER ROMS, THE NOT USED TOO.
45                ;              WHICH IS MENTIONED AFTER THE SIGNAL LIST.
46
47                ;        A5.   WHERE IN THE MIKROPROGRAM IS THE CPU WORKING ?
48                ;              WRITE DOWN SOME STEPS AND THINK.
49                ;              METHODS:
50                ;              1.  LOGIC ANALYZER:
51                ;                      CONNECT AND SET CONTROLS AS IN
52                ;                          SCHEME LOGIC ANALYZER A.
53                ;                      PRESS MANUAL RESET
54                ;                      PRESS MANUAL TRIGGER
55                ;                      READ OUT THE SEQUENCE OF MIKROSTEPS.
56                ;              2.  OSCILLOSCOPE:
57                ;                      ALMOST IMPOSSIBLE IF IT IS A LONG LOOP
58                ;                          IN THE MIKROPROGRAM.
59                ;                      FIND A SUITABLE RAR SIGNAL FOR TRIGGER,
60                ;                          WRITE DOWN THE OTHERS.
```

```
 0013 .MAIN
01
02                ;              3.  THE STATISTIC/WIRE METHOD:
03                ;                  STOP THE CPU BY REMOVING THE CLOCK:
04                ;                  PUT A SHORT WIRE FROM 77-7 TO 77-6
05                ;                      ( -STOP CLOCK, CPU 019).
06                ;                  WRITE DOWN MIKROSTEP FROM LEDS.
07                ;                  REPEAT SEVERAL TIMES (START/STOP).
08
09
10                ;        B.        NOT CORRECT EFFECTUATION DUE TO MIKRO PROGRAM
11                ;                  FLOW. CHECK FOLLOWING:
12
13                ;           B1.    LIKE A1.
14
15                ;           B2.    AS A2.
16
17                ;           B3.    AS A3.
18
19                ;           B4.    LIKE A4 BUT ONLY PART 1 OF SIGNAL CHECK LIST
20                ;                  WHICH IS DIVIDED INTO TWO PARTS:
21                ;                    1.  FOR MIKROPROGRAM FLOW, USE
22                ;                        MIKROPROGRAM MAIN PRIORITY SCHEME.
23                ;                    2.  FOR DATA FLOW.
24
25                ;           B5.    CONTROL THE MIKROPROGRAM FLOW.
26                ;                  METHODS:
27                ;                  1.  LOGIC ANALYZER:
28                ;                          CONNECT AND SET CONTROLS AS IN SCHEME
29                ;                              LOGIC ANALYZER B.
30                ;                          PRESS MANUAL RESET
31                ;                          PERFORM THE TCP ACTION.
32                ;                          READ OUT THE SEQUENCE OF MIKROSTEPS.
33
34                ;                  2.  OSCILLOSCOPE:
35                ;                          USE TRIGGER AS MENTIONED IN SIGNAL CHECK
36                ;                              LIST.
37                ;                          MESSURE THE SIGNALS.
38                ;                          BECAUSE ONLY ONE MIKROPROGRAM LOOP EACH
39                ;                              TIME THE TCP CONTROL IS PRESSED, A
40                ;                              SCOPE LOOP SHOULD BE MADE BY FORCING
41                ;                              THE MIKROPROGRAM TO STAY IN LOOP Y
42                ;                              AFTER FIRST TCP COMMAND BY CONNECTING
43                ;                              FPOP BUSY  CPU 037, IC 4-9
44                ;                              TO ZERO WITH A SHORT WIRE.
45
46
47                ;        C.        NOT CORRECT EFFECTUATION DUE TO BAD SIGNALS.
48                ;                  USE BUS SYSTEM BLOCK SCHEME AND MIKROSTEP
49                ;                  COMMANDS LIST TO HELP TROUBLESHOOTING.
50                ;                  CHECK FOLLOWING:
51
52                ;           C1.    LIKE A4 BUT ONLY PART 2 OF SIGNAL CHECK LIST
53                ;                  WHICH IS DIVIDED INTO TWO PARTS:
54                ;                    1.  FOR MIKROPROGRAM FLOW,
55                ;                    2.  FOR DATA FLOW.
56
57                ;           C2.    CONTROL THE DATA SIGNALS FLOW.
58                ;                  METHODS:
59                ;                  1.  LOGIC ANALYZER       AS B5 - 1
60                ;                  2.  OSCILLOSCOPE         AS B5 - 2
```

```
 0014 .MAIN
01
02
03              ;       LOGIC ANALYZER  SCHEME A.  (TEKTRONIX 7D01)
04
05
06              ;          1.   EXT CLOCK POLARITY:     POSITIVE EDGE
07
08              ;          2.   SAMPLE INTERVAL:        TO EXT POSITION
09
10              ;          3.   DISPLAY TIME:           ENDLESS LONG
11
12              ;          5.   DATA CHANNELS:          0 - 15
13
14              ;         12.   TRIGGER SOURCE:         EXT (NOT USED)
15
16              ;         23.   DATA CH 15 - 8:        USE FOR VIEWING CONTROL
17              ;                                          SIGNALS.
18
19              ;         24.   CLK + DATA 7 - 0:      CLK C TO IC 88-11
20              ;                       (CPU 008):    DATA TO IC 88 OUTPUTS.
21
22              ;         26.   THRESHOLD VOLTAGE:     TTL
```

```
10015 .MAIN
01
02
03              ;       LOGIC ANALYZER  SCHEME B.  (TEKTRONIX 7D01)
04
05
06
07              ;          1.   EXT CLOCK POLARITY:      POSITIVE EDGE
08
09              ;          2.   SAMPLE INTERVAL:         EXT
10
11              ;          3.   DISPLAY TIME:            ENDLESS LONG
12
13              ;          5.   DATA CHANNELS:           0 - 15
14
15              ;         11.   DATA POSITION:           CENTER
16
17              ;         12.   TRIGGER SOURCE:         W. R.
18
19              ;         15.   WORD RECOGNIZER CH SWITCHES:
20              ;                                       CH 0 TO HI IF POSITIVE
21              ;                                            TO LO IF NEGATIVE
22              ;                                  TRIGGER IN SIGNAL CHECK LIST
23              ;
24              ;                                       CH 1 - 15 TO X
25
26              ;         16.   EXTERNAL QUALIFIER SWITCH:  TO X
27
28              ;         17.   PROBE QUALIFIER SWITCH: TO X
29
30              ;         18.   W. R. MODE:             ASYNC
31
32              ;         23.   DATA 15 - 8:            USE FOR VIEWING SIGNALS
33
34              ;         24.   CLK + DATA 7 - 0:       CLK C TO IC 88-11
35              ;                                            (CPU 808)
36              ;                                       DATA CH 0 TO TRIGGER
37              ;                                            IN SIGNAL CHECK LIST.
38              ;                                       DATA CH 1 - 7 AS 15 - 8.
39
40              ;         26.   THRESHOLD VOLTAGE:      TTL
41
42
43              ;TAPE 1
44
45              .EOT
```

```
0016 .MAIN
01                ;TAPE 2
02
03
04
05
06
07                ;            ***     ************************************************
08                ;          *         *                                              *
09                ;          *         *   C:   CPU 708  SIGNAL CHECK LIST            *
10                ;          *         *                                              *
11                ;            ***     ************************************************
12
13
14
15                ;       THIS IS SIGNAL CHECK LISTS FOR THE STEPS IN CPU 708
16                ;       STATIC TEST. THEY CONTENT RELEVANT SIGNALS TO MESSURE
17                ;       IF ERRORS AND THE EXPECTED VALUE IN EACH MIKROSTEP.
18
19
20                ;       1.  PAGE 17     SIGNAL CHECK LIST 1
21                ;       2.  PAGE 18     SIGNAL CHECK LIST 2
22                ;       3.  PAGE 20     SIGNAL CHECK LIST 3
23                ;       4.  PAGE 23     SIGNAL CHECK LIST 4
24                ;       5.  PAGE 26     SIGNAL CHECK LIST 5
```

```
!0017 ,MAIN
01
02                  !       1.      SIGNAL CHECK LIST 1 FOR RESET.
03
04                  !       MESSURING METHOD A.
05
06                  !       PAGE    NAME              IC-PIN  MIKROSTEP
07
08                  !                                         126 127
09                  !       007     -RAR CLR B        150-12    1   1
10                  !       007     SEL 1ST OP        105-19    0   0
11                  !       007     NXAD SEL C (4)    105-16    1   0
12                  !       008     NXAD SEL B (2)    105-15    0   1
13                  !       007     NXAD SEL A (1)    105-12    0   0
14                  !
15                  !       TRIGGER, POSITIVE:
16                  !       008     RAR 7 (1) @1\      88-2     0   1
17
18                  !       008     RAR 6 (2) @2\      88-5     1   1
19                  !       008     RAR 5 (4) @4\      88-6     1   1
20                  !       008     RAR 4 (8) @10\     88-9     0   0
21                  !       008     RAR 3 (16) @20\    88-12    1   1
22                  !       008     RAR 2 (32) @40\    88-15    0   0
23                  !       008     RAR 1 (64) @100\   88-16    1   1
24                  !       008     RAR 0 (128) @200\  88-19    0   0
25                  !       008     SEL 0 (NX C)       89-4     1   0
26                  !       008     SEL 1 (NX B)       89-7     0   1
27                  !       008     SEL 2 (NX A)       89-9     0   0
28                  !       008     SEL 3 (2.OP 4)     89-12    0   0
29                  !       008     SEL 4 (2.OP 3)     90-4     X   1
30                  !       008     SEL 5 (2.OP 2)     90-7     X   1
31                  !       008     SEL 6 (2.OP 1)     90-9     X   1
32                  !       008     SEL 7 (2.OP 0)     90-12    1   1
33                  !       011     -BREAK            150-19    1   1
34                  !       011     ENABLE 1 ROM 660   75-4     0   0
35                  !       015     -SKIP B           135-19    1   1
36                  !       041     RUN B             150-15    0   0
37                  !       016     APL B              24-19    0   0
38                  !       016     -FPOP BUSY B       24-15    1   1
39                  !       016     -FPOP 2 B          24-12    1   1
40                  !       016     -FPOP 1 B          24-9     1   1
41                  !       016     -FPOP 0 B          24-6     1   1
42                  !   *   035     -CLR RUN           18-1     1   1
43                  !       035     -SET RUN           18-2     1   1
44                  !       035     -MIKRO STEP        18-3     1   1
45                  !       035     -INSTR STEP        18-4     1   1
46                  !       035     -CPU FUNC          18-5     1   1
47                  !       035     -PL TCP            18-6     1   1
48                  !   *   035     -SET DC RST        18-9     1   1
49
50                  !       *  ONE 50 NSEC PULSE TO ZERO WHEN PRESSING RESET,
51                  !          WHEN RUN IS CLEARED THE MIKROPROGRAM ENTERS THE
52                  !          RESET LOOP NEXT TIME IT PASSES CONDITION GROUP 4.
53
54                  !       FOLLOWING ROM'S ARE ACTIVATED:
55                  !       630 POS 98, 629 POS 97, 660 POS 106,
56                  !       (616 POS 18 PULS BEFORE ENTERING RESET MIKAD, *).
57
58                  !       FOLLOWING ROM'S ARE ABLE TO INTERFERE:
59                  !       648 POS 100, 649 POS 99, 650 POS 96, 661 POS 95,
60                  !       614 POS 144.
```

```
0018 .MAIN
01
02
03                ;       2.      SIGNAL CHECK LIST 2 FOR
04                ;               DEPOSIT REGISTER.
05
06                ;       THE MIKROPROGRAM FLOW IS:
07
08                ;       X  127, 126                 ;LOOPING AFTER RESET
09
10                ;       Y  127, 117, 250, 126       ;DEPOSIT REGISTER ONE LOOP
11
12                ;       Z  127, 126                 ;LOOPING AFTER DEPOSIT
13
14                ;                                   ;NEXT DEPOSIT: FROM Z126 TO Y127.
15
16                ;       IF ERROR IN MIKROPROGRAM USE MESSURING METHOD B FOR
17                ;       LOOP Y AND MESSURING METHOD A FOR LOOP Z:
18
19                ;       PAGE    NAME            IC-PIN  MIKROSTEP
20
21                ;                                       Y   Y   Y   Y   Z   Z
22                ;                                       127 117 250 126 127 126
23
24                ;       TRIGGER, POSITIVE:
25                ;       011     SEL 1.ST OP     105-19  0   1   1   0   0   0
26
27                ;       011     NXAD SEL C (4)  105-16  0   1   1   1   0   1
28                ;       011     NXAD SEL B (2)  105-15  1   X   X   0   1   0
29                ;       011     NXAD SEL A (1)  105-12  0   0   0   0   0   0
30                ;       008     RAR 0-7          88-X       MIKROSTEP ADDR
31                ;       008     SEL 0            89-4   0   1   1   1   0   1
32                ;       008     SEL 1            89-7   1   X   X   0   1   0
33                ;       008     SEL 2            89-9   0   0   0   0   0   0
34                ;       008     SEL 3            89-12  0   X   X   0   0   0
35                ;       008     SEL 4            90-4   0   X   X   X   1   X
36                ;       008     SEL 5            90-7   1   X   X   X   1   X
37                ;       008     SEL 6            90-9   0   X   X   X   0   X
38                ;       008     SEL 7            90-12  1   X   X   1   1   1
39                ;       015     -SKIP B         135-19  1   1   1   1   1   1
40                ;       041     RUN B           150-15  0   0   0   0   0   0
41                ;       016     APL B            24-19  0   0   0   0   0   0
42                ;       016     -FPOP BUSY B     24-15  0   0   1   1   1   1
43                ;       016     -FPOP 2 B        24-12  1   1   1   1   1   1
44                ;       016     -FPOP 1 B        24-9   0   0   0   0   0   0
45                ;       016     -FPOP 0 B        24-6   1   1   1   1   1   1
46                ;       037     -FPOP BUSY        4-9   0   1   1   1   1   1
47                ;   *   035     -CPU FUNC        18-5   1   1   1   1   1   1
48
49                ;       *  ONE 50 NSEC PULSE TO ZERO WHEN PRESSING DEPOSIT REG.
50                ;          IN THE LAST LOOP X OR Z 126,127 JUST BEFORE ENTERING
51                ;          LOOP Y.
52
53                ;       FOLLOWING ROM'S USED:
54                ;       630 POS 98, 629 POS 97, 648 POS 100, 649 POS 99,
55                ;       660 POS 106, 616 POS 18 (*).
56
57                ;       FOLLOWING ROM'S INTERFERING ?
58                ;       650 POS 96, 661 POS 95.
```

```
00019 .MAIN
01
02              ;       IF ERROR IN DATA LEDS USE MESSURING METHOD C:
03              ;               RA = REGISTER ADDR
04              ;               DS = DATA FROM SWITCH   **
05              ;               PC = DATA FROM PC, AC4 IN ALU   **
06
07              ;       PAGE    NAME            IC-PIN  MIKROSTEP
08
09              ;                                       Y   Y   Y   Y   Z   Z
10              ;                                       127 117 250 126 127 126
11
12              ;       TRIGGER, NEGATIVE:
13              ;       036     -LD DATA REG    78-2    1   0   0   1   1   1
14
15              ;       036     EN SWITCHES     87-3    0   1   1   0   0   0
16              ;       036     -BUS 0-15               RA  DS  DS  PC  RA  PC
17              ;       036     -PAN BUS 0-15           X   DS  DS  DS  DS  DS
18              ;       034     -CON DATA       35-6    1   0   0   1   1   1
19              ;       040     EN FP-BUS       36-11   1   1   1   1   1   1
20              ;       034     EN PAN-BUS      146-12  0   1   1   0   0   0
21
22              ;       **  NOTE THAT IT IS NOT TESTED HERE THAT DS GOES TO ALU
23              ;           AND PC COMES FROM ALU, THE CONTENTS OF LED DATA
24              ;           IS INDEPENDENT OF THE ALU, IF THIS DATA TO/FROM ALU
25              ;           IS NOT CORRECT SEE EXAMINE TEST.
26
27              ;       FOLLOWING ROM USED:
28              ;       651 POS 79.
```

```
10020 .MAIN
01
02                ;       3.      SIGNAL CHECK LIST 3 FOR
03                ;               EXAMINE REGISTER.
04
05                ;       THE MIKROPROGRAM FLOW IS:
06
07                ;       X  127, 126             ;LOOPING AFTER RESET
08
09                ;       Y  127, 116, 126        ;EXAMINE REGISTER ONE LOOP
10
11                ;       Z  127, 126             ;LOOPING AFTER EXAMINE
12
13                ;                               ;NEXT EXAMINE: FROM Z126 TO Y127.
14
15                ;       IF ERROR IN THE MIKROPROGRAM, THE METHOD, SIGNALS AND
16                ;       ROM'S ARE AS FOR DEPOSIT REGISTER (CHECK LIST 2), BUT
17                ;       STEP 116 INSTEAD OF 117 + 250, WITH ONLY THIS TWO
18                ;       SIGNALS DIFFERENT:
19
20                ;       PAGE    NAME            IC-PIN  MIKROSTEP
21
22                ;                                       Y   Y       Y   Z   Z
23                ;                                       127 116     126 127 126
24
25                ;       016     -FPOP 1 B        24-9   1   1       1   1   1
26                ;       016     -FPOP 0 B        24-6   0   0       0   0   0
27
28
29                ;       IF ERROR IN DATA LEDS USE MESSURING METHOD C:
30                ;               RA = REGISTER ADDR
31                ;               DA = DATA FROM ALU
32                ;               PC = DATA FROM PC, AC4 IN ALU
33
34                ;       PAGE    NAME            IC-PIN  MIKROSTEP
35
36                ;                                       Y   Y       Y   Z   Z
37                ;                                       127 116     126 127 126
38
39                ;       035     EN AC SEL BUS    36-3   0   1       1   0   1
40                ;       006     LD IR           108-6   1   0       0   1   0
41                ;       006     IR 1-4           55-X   X   RA      RA  RA  RA
42
43                ;       TRIGGER, NEGATIVE:
44                ;       013     -PAN ACN EN     108-16  1   0       1   1   1
45
46                ;       013     -GATE ACN       118-12  1   0       1   1   1
47                ;       015     -ALC CON        118-15  1   1       1   1   1
48                ;       010     -CIN            118-16  1   1       1   1   1
49                ;       010     -SWAP EN        141-12  0   0       0   0   0
50                ;       005     -3 STATE EN     105-6   1   0       0   1   0
51                ;       036     -LD DATA REG     78-2   1   0       1   1   1
52                ;       036     -BUS 0-15                RA  DA      PC  RA  PC
53                ;       036     -PAN BUS 0-15            X   X       DA  DA  DA
54
55                ;       FOLLOWING ROM'S USED:
56                ;       651 POS 79, 659 POS 107, 662 POS 119, 663 POS 110,
57                ;       664 POS 109.
58
59                ;       FOLLOWING ROM'S INTERFERING ?
60                ;       658 POS 117.
```

```
 0021 .MAIN
01
02
03                ;       IF STILL ERROR THE CONTROL SIGNALS TO THE ALU AND THE
04                ;       ALU ITSELF SHALL BE CONTROLLED, MESSURING METHOD C.
05                ;       IT IS IMPOSSIBLE TO KNOW WETHER THE ERROR IS IN
06                ;       DEPOSIT OR EXAMINE, THEREFORE BOTH SIGNAL LISTS IS
07                ;       GIVEN:
08                ;               RA = REGISTER ADDR
09
10
11                ;       EXAMINE:
12
13                ;       PAGE    NAME            IC-PIN  MIKROSTEP
14
15                ;                                       Y   Y       Y   Z   Z
16                ;                                       127 116     126 127 126
17
18                ;       010     CIN              41-3   0   0       0   0   0
19                ;       014     I0              125-16  1   1       0   1   0
20                ;       014     I1              125-15  1   1       0   1   0
21                ;       014     I2              125-12  1   0       1   1   1
22                ;       015     I3              135-16  1   0       0   1   0
23                ;       015     I4              135-15  0   0       0   0
24                ;       015     I5              135-12  1   0       0   1
25                ;       015     I6               94-9   1   1       1   1   1
26                ;       015     I7               94-7   0   0       0   0   0
27                ;       015     I8               94-4   0   0       0   0   0
28                ;               ALU FUNCTION             0   B+0     A+0 0   A+0
29                ;       013     ASEL 0 (1)       56-2   1   0       0   1   0
30                ;       013     ASEL 1 (2)       56-5   1   0       0   1   0
31                ;       013     ASEL 2 (4)       56-6   1   0       1   1   1
32                ;       013     ASEL 3 (8)       56-9   1   0       0   1   0
33                ;       013     BSEL 0 (1)      56-12   1   RA0     0   1   0
34                ;       013     BSEL 1 (2)      56-15   1   RA1     0   1   0
35                ;       013     BSEL 2 (4)      56-16   1   RA2     1   1   1
36                ;       013     BSEL 3 (8)      56-19   1   RA3     0   1   0
37
38                ;       TRIGGER, NEGATIVE:
39                ;       013     -PAN ACN EN     108-16  1   0       1   1   1
40
41                ;       FOLLOWING ROM'S USED:
42                ;       606 POS 57, 655 POS 126, 652 POS 137, 653 POS 136.
```

```
↓0022 .MAIN
01
02
03              ;               RA = REGISTER ADDR
04
05
06              ;       DEPOSIT:
07
08              ;       PAGE    NAME            IC-PIN  MIKROSTEP
09
10              ;                                       Y   Y   Y   Y   Z   Z
11              ;                                       127 117 250 126 127 126
12
13              ;       035     EN AC SEL-BUS    36-3   0   1   1   1   0   1
14              ;       006     LD IR           108-6   1   0   0   0   1   0
15              ;       006     IR 1-4           55-X   X   RA  RA  RA  RA  RA
16
17              ;       TRIGGER, NEGATIVE:
18              ;       013     -PAN ACN EN     108-16  1   0   0   1   1   1
19
20              ;       013     -GATE ACN       118-12  1   0   0   1   1   1
21              ;       015     -ALC CON        118-15  1   1   1   1   1   1
22              ;       010     -CIN            118-16  1   1   1   1   1   1
23              ;       010     -SWAP EN        141-12  0   0   0   0   0   0
24              ;       010     CIN              41-3   0   0   0   0   0   0
25              ;       014     I0              125-16  1   1   1   0   1   0
26              ;       014     I1              125-15  1   1   1   0   1   0
27              ;       014     I2              125-12  1   1   1   1   1   1
28              ;       015     I3              135-16  1   1   1   0   1   0
29              ;       015     I4              135-15  0   1   1   0   0   0
30              ;       015     I5              135-12  1   0   0   0   1   0
31              ;       015     I6               94-9   1   1   1   1   1   1
32              ;       015     I7               94-7   0   1   1   0   0   0
33              ;       015     I8               94-4   0   0   0   0   0   0
34              ;                                                   OUT:    OUT:
35              ;               ALU FUNCTION            0   D(OR 0) A+0  0   A+0
36              ;                                           LOAD RAM
37              ;       013     ASEL 0 (1)      56-2    1   0   0   0   1   0
38              ;       013     ASEL 1 (2)      56-5    1   0   0   0   1   0
39              ;       013     ASEL 2 (4)      56-6    1   0   0   1   1   1
40              ;       013     ASEL 3 (8)      56-9    1   0   0   0   1   0
41              ;       013     BSEL 0 (1)      56-12   1   RA0 RA0 0   1   0
42              ;       013     BSEL 1 (2)      56-15   1   RA1 RA1 0   1   0
43              ;       013     BSEL 2 (4)      56-16   1   RA2 RA2 1   1   1
44              ;       013     BSEL 3 (8)      56-19   1   RA3 RA3 0   1   0
45
46              ;       FOLLOWING ROM'S USED:
47              ;       606 POS 57, 655 POS 126, 652 POS 137, 653 POS 136,
48              ;       662 POS 119, 663 POS 110, 664 POS 109.
49
50              ;       FOLLOWING ROM'S INTERFERING ?
51              ;       658 POS 117.
```

```
!0023 ,MAIN
31
32
33                ;       4.      SIGNAL CHECK LIST 4 FOR
34                ;               DEPOSIT/EXAMINE MEMORY.
35
36                ;       THE MIKROPROGRAM FLOW IS:
37
38                ;       X  127, 126                         ;LOOPING AFTER RESET
39
40                ;       Y  127, 121, %122%, 224, 126        ;EXAMINE MEMORY ONE LOOP
41
42                ;       Z  127, 126                         ;LOOPING AFTER EXAMINE
43
44                ;       W  127, 124, %125%, 126             ;DEPOSIT MEMORY ONE LOOP
45
46                ;       Q  127, 126                         ;LOOPING AFTER DEPOSIT
47
48                ;       R  127, 121, %122%, 224, 126        ;EXAMINE MEMORY ONE LOOP
49
50                ;       S  127, 126                         ;LOOPING AFTER EXAMINE
51
52                ;       T  127, 116, 126                    ;EXAMINE REGISTER ONE
53                ;                                           ;LOOP   AC4 = PC
54
55                ;       U  127, 126                         ;LOOPING AFTER EX. REG.
56
57                ;  %-%  STEPS ABOUT 800 NSEC LONG, ONE COMPLETE MEM CYCLE.
58
59                ;       IF ERROR IN THE MIKROPROGRAM, THE METHOD, SIGNALS AND
60                ;       ROM'S ARE AS FOR DEPOSIT REGISTER (CHECK LIST 2), BUT
61                ;       STEP 124,125 OR STEP 121,122,124 INSTEAD OF 117,250,
62                ;       WITH ONLY THIS THREE SIGNALS DIFFERENT:
63
64                ;       PAGE    NAME            IC-PIN  MIKROSTEP
65
66                ;                                       W+Q     Y+Z, R+S
67                ;                                       DEPOSIT EXAMINE MEM
68
69                ;       816     -FPOP 2 B       24-12   0       1
70                ;       816     -FPOP 1 B       24-9    1       0
71                ;       816     -FPOP 0 B       24-6    0       0
72
73                ;       IF THE MIKROPROGRAM STOPS OR THERE ARE OTHER
74                ;       MEMORY CONTROL PROBLEMS, CONSULT THE PULS SCHEME
75                ;       FOR MEMORY CONTROL.
76
77                ;       IF ERROR IN DATA LEDS AFTER DEPOSIT, THE ONLY DIFFERENCE
78                ;       (CONCERNING DATA LEDS) FROM REGISTER DEPOSIT (CHECK LIST
79                ;       2) IS THAT THE ACTION IN STEP 117, 250 NOW TAKES PLACE
80                ;       IN STEP 125. JUST BEFORE STEP 125, IN STEP 124, THE BUS
81                ;       IS USED FOR SENDING PC FROM ALU (HERE = 0) TO THE MAR.
82                ;       NOTE THAT TEST OF DATA TO MEMORY IS DONE TOGETHER WITH
83                ;       EXAMINE. MORE ABOUT DEPOSIT IN MEMORY AFTER EXAMINE LIST.
84
85
86                ;ABREVIATIONS:
87                ;       RA = REGISTER ADDR
88                ;       DS = DATA FROM SWITCHES
89                ;       DM = DATA FROM MEMORY (AFTER DATA AVAILABLE)
90                ;       PC = DATA FROM PC, AC4 IN ALU
```

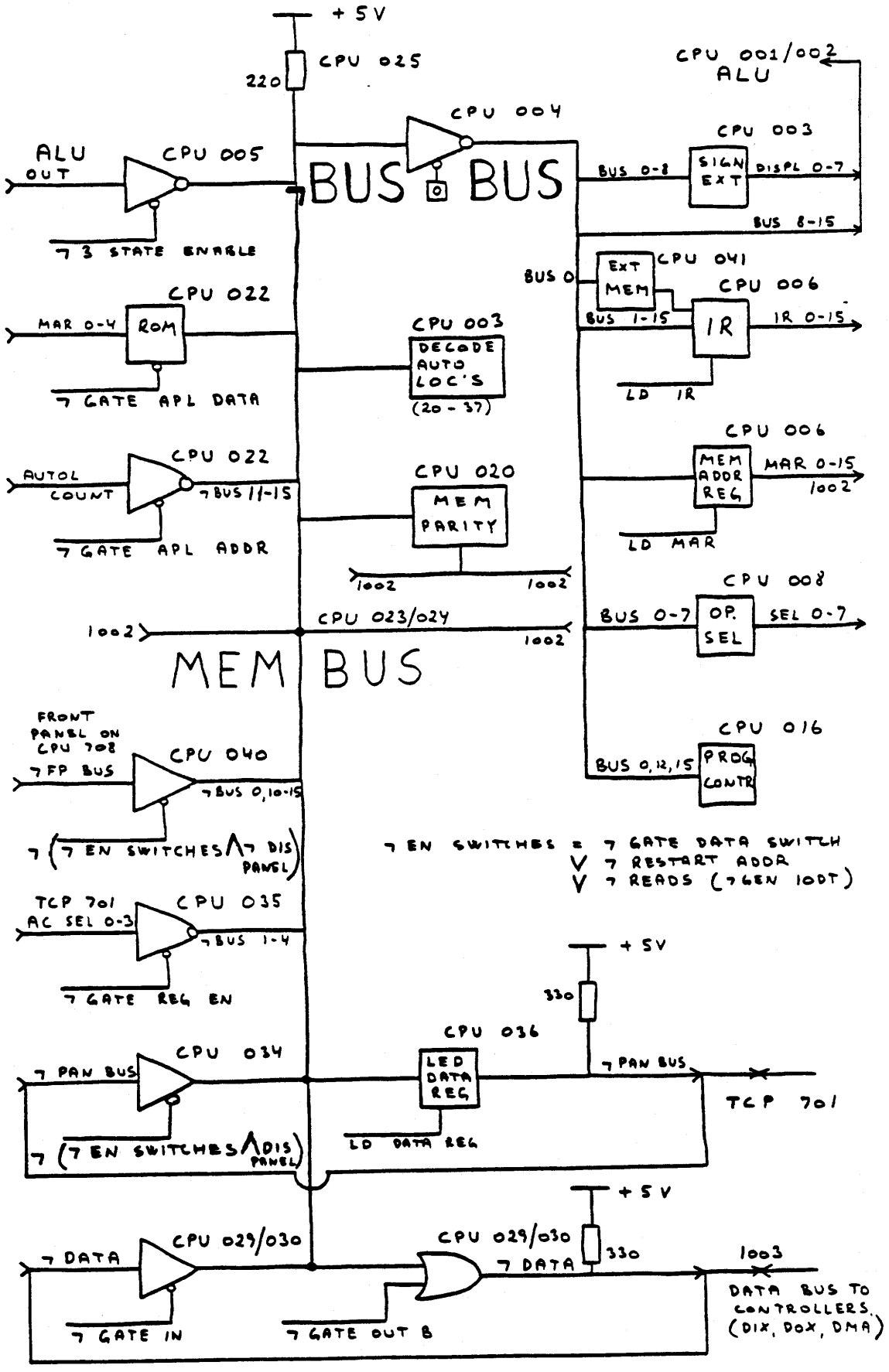
```
0024 .MAIN
01
02
03              ;       IF ERROR IN DATA LEDS AFTER EXAMINE MEMORY CHECK
04              ;       FOLLOWING SIGNALS: (RA,DS,DM AND PC SEE ABOVE)
05
06              ;  PAGE NAME              IC-PIN   MIKROSTEP
07
08              ;                                   R    R    R    R    R    S    S
09              ;                                  127  121  122  224  126  127  126
10              ;                                            LONG
11              ;  TRIGGER, POSITIVE:
12              ;  034  EN SWITCHES        87-3     0    1    0    0    0    0    0
13
14              ;  034  -BUS 0-15                   RA   DS   DM    1   PC   RA   PC
15              ;  006  LD MAR            108-9     0    1    0    0    1    0    1
16              ;  036  -LD DATA REG       78-2     1    1    0    1    1    1    1
17              ;  036  -PAN BUS 0-15              X   DS    X   DM   DM   DM   DM
18              ;  019  -MEM READ         118-19    1    1    0    1    1    1    1
19              ;  019  -TEST MEM         135-9     1    0    0    1    0    1    0
20
21
22              ;       IF ERROR IN DATA LEDS AFTER EXAMINE PC (AC4), CHECK
23              ;       SIGNALS ABOVE FOR EXAMINE AND FOLLOWING:
24
25              ;  PAGE NAME              IC-PIN   MIKROSTEP
26
27              ;                                   R    R    R    R    R    S    S
28              ;                                  127  121  122  224  126  127  126
29              ;                                            LONG
30
31              ;  013  -GATE ACN         118-12    1    1    1    1    1    1    1
32              ;  015  -ALC CON         118-15    1    1    1    1    1    1    1
33              ;  010  CIN               41-3     0    0    0    0    0    0    0
34              ;  014  I0               125-16    1    1    1    1    0    1    0
35              ;  014  I1               125-15    1    1    1    1    0    1    0
36              ;  014  I2               125-12    1    1    1    1    1    1    1
37              ;  015  I3               135-16    1    0    1    1    0    1    0
38              ;  015  I4               135-15    0    0    0    0    0    0    0
39              ;  015  I5               135-12    1    0    1    1    0    1    0
40              ;  015  I6                94-9     1    1    1    1    1    1    1
41              ;  015  I7                94-7     0    1    0    0    0    0    0
42              ;  015  I8                94-4     0    0    0    0    0    0    0
43              ;                                                     OUT:      OUT:
44              ;       ALU FUNCTION               0  D+0   0    0   A+0   0   A+0
45              ;                                   LOAD RAM
46              ;  013  ASEL 0 (1)         56-2     1    0    1    1    0    1    0
47              ;  013  ASEL 1 (2)         56-5     1    0    1    1    0    1    0
48              ;  013  ASEL 2 (4)         56-6     1    1    1    1    1    1    1
49              ;  013  ASEL 3 (8)         56-9     1    0    1    1    0    1    0
50              ;  013  BSEL 0 (1)        56-12     1    0    1    1    0    1    0
51              ;  013  BSEL 1 (2)        56-15     1    0    1    1    0    1    0
52              ;  013  BSEL 2 (4)        56-16     1    1    1    1    1    1    1
53              ;  013  BSEL 3 (8)        56-19     1    0    1    1    0    1    0
54
55              ;       FOLLOWING ROM'S USED:
56              ;       651 POS 79, 652 POS 137, 653 POS 136, 655 POS 126,
57              ;       656 POS 59, 657 POS 58, 662 POS 119, 663 POS 110.
58
59              ;       FOLLOWING ROM'S INTERFERING ?
60              ;       606 POS 57, 658 POS 117.
```

```
 0025 .MAIN
01
02
03              ;       IF STILL ERROR CHECK THAT DEPOSIT SENDS TO MEMORY:
04              ;               RA = REGISTER ADDR
05              ;               PC = DATA FROM PC, AC4 IN ALU
06              ;               DS = DATA FROM SWITCHES
07
08              ;       PAGE    NAME            IC-PIN  MIKROSTEP
09
10              ;                                       W   W   W   W   Q   Q
11              ;                                       127 124 125 126 127 126
12              ;                                               LONG
13
14              ;       005     -3 STATE EN     105-6   1   0   1   0   1   0
15              ;       036     -BUS 0-15               RA  PC  DS  PC  RA  PC
16              ;       006     LD MAR          108-9   0   1   0   1   0   1
17              ;       036     EN SWITCHES      87-3   0   0   1   0   0   0
18              ;       036     -LD DATA REG     78-2   1   1   0   1   1   1
19              ;       036     -PAN BUS 0-15            X   X   DS  DS  DS  DS
20
21              ;       TRIGGER, NEGATIVE:
22              ;       019     -MEM WRITE      108-5   1   1   0   1   1   1
23
24              ;       019     -TEST MEM       135-9   1   0   0   0   1   1
25              ;       013     -GATE ACN       118-12  1   1   1   1   1   1
26              ;       015     -ALC CON        118-15  1   1   1   1   1   1
27              ;       010     CIN              41-3   0   0   0   0   0   0
28              ;       014     I0              125-16  1   0   1   0   1   0
29              ;       014     I1              125-15  1   0   1   0   1   0
30              ;       014     I2              125-12  1   1   1   1   1   1
31              ;       015     I3              135-16  1   0   1   0   1   0
32              ;       015     I4              135-15  0   0   0   0   0   0
33              ;       015     I5              135-12  1   0   1   0   1   0
34              ;       015     I6               94-9   1   1   1   1   1   1
35              ;       015     I7               94-7   0   0   0   0   0   0
36              ;       015     I8               94-4   0   0   0   0   0   0
37              ;                                           OUT:    OUT:    OUT:
38              ;               ALU FUNCTION                0   A+0 0   A+0 0   A+0
39              ;
40              ;       013     ASEL 0 (1)       56-2   1   0   1   0   0   0
41              ;       013     ASEL 1 (2)       56-5   1   0   1   0   0   0
42              ;       013     ASEL 2 (4)       56-6   1   1   1   1   1   1
43              ;       013     ASEL 3 (8)       56-9   1   0   1   0   0   0
44              ;       013     BSEL 0 (1)      56-12   1   0   1   0   0   0
45              ;       013     BSEL 1 (2)      56-15   1   0   1   0   0   0
46              ;       013     BSEL 2 (4)      56-16   1   1   1   1   1   1
47              ;       013     BSEL 3 (8)      56-19   1   0   1   0   0   0
48
49              ;       FOLLOWING ROM'S USED:
50              ;       651 POS 79, 652 POS 137, 653 POS 136, 655 POS 126,
51              ;       656 POS 59, 657 POS 58, 659 POS 107, 663 POS 110.
52
53              ;       FOLLOWING ROM'S INTERFERING ?
54              ;       658 POS 117, 662 POS 119, 606 POS 57.
```

```
!0026 .MAIN
01
02              ;       5.      SIGNAL CHECK LIST 5 FOR
03              ;               JMP 0, PLACED IN MEM LOC 0.
04
05              ;       THE MIKROPROGRAM FLOW IS:
06
07              ;       X  127, 126             ;LOOPING AFTER DEPOSIT/EXAMINE
08
09              ;       Y  127, 207, 0          ;START SWITCH PRESSED, ONE LOOP
10
11              ;       Z  %1%, 2               ;LOOPING IN JMP 0
12
13              ;       %=%     STEP ABOUT 600-650 NSEC LONG WAITING FOR MEM.
14
15              ;       IF ERROR IN THE MIKROPROGRAM USE MEASURING METHOD B
16              ;       FOR LOOP Y AND MEASURING METHOD A FOR LOOP Z, SIGNALS:
17
18              ;       PAGE    NAME            IC-PIN  MIKROSTEP
19
20              ;                                       Y   Y   Y   Z   Z
21              ;                                       127 207 0   1   2
22
23              ;       TRIGGER, POSITIVE:
24              ;       011     SEL 1, ST OP    105-19  0   1   0   1   0
25
26              ;       011     NXAD SEL C(4)   105-6   0   1   1   0   1
27              ;       011     NXAD SEL B (2)  105-15  1   X   0   X   0
28              ;       011     NXAD SEL A (1)  105-12  0   0   0   1   0
29              ;       008     RAR 0-7          88-X   MIKROSTEP ADDR
30              ;       008     SEL 0            89-4   0   0   1   0   1
31              ;       008     SEL 1            89-7   1   0   0   0   0
32              ;       008     SEL 2            89-9   0   0   0   0   0
33              ;       008     SEL 3            89-12  0   0   1   0   1
34              ;       008     SEL 4            90-4   0   0   1   0   1
35              ;       008     SEL 5            90-7   1   0   0   0   0
36              ;       008     SEL 6            90-9   1   0   X   0   X
37              ;       008     SEL 7            90-12  1   0   1   0   1
38              ;       015     -SKIP B         135-19  1   1   1   1   1
39              ;       016     APL B           150-15  0   0   0   0   0
40
41              ;       IF ERROR IN DATALEDS OR FUNCTION, CHECK BUS,
42              ;       CHECK CONTROLSIGNALS FOR MIKROPROGRAM FLOW THROUGH
43              ;       FETCHCYCLE (START ADDR JUMP), CONDITION GROUP 4 AND 2,
44              ;       USE THE SCHEME CPU 708 MIKROPROGRAM MAIN PRIORITY
45              ;       AND THE PULSSCHEME FOR MEMORY CONTROL (HERE IS JMP 0,
46              ;       THE SCHEME IS FOR JMP .+0, ONLY DIFFERENCE IS STEP
47              ;       2 INSTEAD OF STEP 3).
```

```
10027 .MAIN
01
02
03
04
05
06                ;          ***     ****************************************
07                ;          *  *     *                                      *
08                ;          *  *     *   D:   BUS SYSTEM BLOCK SCHEME       *
09                ;          *  *     *                                      *
10                ;          ***     ****************************************
11
12
13                ;       THIS SCHEME IS USED TO HAVE A COMPLETE INFORMATION
14                ;       OF SIGNALS AND CONTROLSIGNALS GOING TO AND FROM
15                ;       THE MAIN BUS IN THE CPU.
```

RC 3603, CPU 708 BUS SYSTEM.



```
!0029 .MAIN
01
02
03
04
05
06                ;            ****    ****************************************
07                ;            *       *                                      *
08                ;            ***     *   E:   MIKROSTEP COMMANDS LIST       *
09                ;            *       *                                      *
10                ;            ****    ****************************************
11
12
13                ;       THIS IS NOT A COMPLETE LIST, IT IS MADE FOR
14                ;       THE BUS CONTROL SIGNALS AND THE SIGNALS MENTIONED
15                ;       IN SIGNAL CHECK LISTS. IT IS AN USEFUL LIST TO
16                ;       GIVE SURVEY AND TO CHECK FOR A GIVEN SIGNAL, WHICH
17                ;       YOU WANT TO GROUND OR DISCONNECT, WILL AFFECT THE
18                ;       OTHER MIKROSTEPS IN THE LOOP UNDER TEST.
19                ;       THE SIGNAL NAMES ARE WRITTEN WITHOUT THE NOT SIGN,
20                ;       BUT ALL SIGNALS ARE THE SIGNAL LEAVING THE ROM.
21                ;       THE FIRST PAGES ARE AN ALPHABETIC LIST, THEN FOLLOWS
22                ;       A LIST WITH THE SAME SIGNALS BUT IN MIKROSTEP ORDER.
```

```
10030 .MAIN
01
02
03
04              ;       ALC CON                         ACTIVE WHEN ZERO
05
06              ;       USED IN STEP    42,43,44,45,46,47,50,51.
07
08
09              ;       BLOCK BIT 0                     ACTIVE WHEN ZERO
10
11              ;       USED IN STEP    2,3,4,5,6,7,12,13,14,15,22,26,31,34,41,
12              ;                       75,106,110,126,131,217,242.
13
14
15              ;       CIN                             ACTIVE WHEN ZERO
16
17              ;       USED IN STEP    20,24,27,34,35,41,43,45,47,75,102,111,
18              ;                       120,123,130,131,134,135,137,144,217,
19              ;                       221,225.
20
21              ;       FPOP END                        ACTIVE WHEN ZERO
22
23              ;       USED IN STEP    116,117,122,125,250.
24
25
26              ;       GATE ACN                        ACTIVE WHEN ZERO
27
28              ;       USED IN STEP    32,33,42,43,44,45,46,47,50,51,61,66,71,
29              ;                       72,116,117,170,171,172,173,174,227,241,
30              ;                       250.
31
32
33              ;       GATE APL ADDR                   ACTIVE WHEN ZERO
34
35              ;       USED IN STEP    114.
36
37
38              ;       GATE APL DATA                   ACTIVE WHEN ZERO
39
40              ;       USED IN STEP    115.
41
42
43              ;       GATE DATA SWITCH                ACTIVE WHEN ZERO
44
45              ;       USED IN STEP    117,121,125,230,250.
46
47
48              ;       GATE IN                         ACTIVE WHEN ZERO
49
50              ;       USED IN STEP    57,60,61,71,77,155,166.
51
52
53              ;       GATE OUT                        ACTIVE WHEN ZERO
54
55              ;       USED IN STEP    101,105,156,157,160,161,162,163,
56              ;                       170,171,172,173,174.
```

```
10031 .MAIN
31
32
33              ;       GATE REG EN                         ACTIVE WHEN ZERO
34
35              ;       USED IN STEP    127.
36
37
38              ;       GEN IODT                            ACTIVE WHEN ZERO
39
10              ;       USED IN STEP    57,60,61,71,73,171,172,173,177,200,201.
11
12
13              ;       LD DATA REG                         ACTIVE WHEN ZERO
14
15              ;       USED IN STEP    0,1,16,17,20,21,23,24,25,27,30,32,33,
16              ;                       35,36,37,40,42,43,44,45,46,47,50,51,52,
17              ;                       53,54,55,57,60,61,62,63,64,65,66,67,71,
18              ;                       72,100,101,102,103,104,105,110,112,115,
19              ;                       116,117,122,123,125,133,142,143,217,230,
20              ;                       250.
21
22
23              ;       LD IR                               ACTIVE WHEN ONE !
24
25              ;       USED IN STEP    1,107,127,142,143,150,245.
26
27
28              ;       LD MAR                              ACTIVE WHEN ONE !
29
30              ;       USED IN STEP    0,2,3,4,5,6,7,10,11,12,13,14,15,22,26,
31              ;                       31,34,41,75,77,106,107,111,113,114,120,
32              ;                       121,124,126,130,131,210,216,217,220.
33
34
35              ;       MEM READ                            ACTIVE WHEN ZERO
36
37              ;       USED IN STEP    1,16,32,35,36,101,102,104,122,156,157,
38              ;                       160.
39
40
41              ;       MEM WRITE                           ACTIVE WHEN ZERO
42
43              ;       USED IN STEP    21,25,33,40,105,110,115,125,133,162,163,
44              ;                       237,240,241,242,243.
45
46
47              ;       PAN ACN EN                          ACTIVE WHEN ZERO
48
49              ;       USED IN STEP    33*,116,117,226,241*,250. (*FCO 11-025)
50
51
52              ;       RESTART ADDR                        ACTIVE WHEN ZERO
53
54              ;       USED IN STEP    0,207,213,246,247.
55
56
57              ;       SWAP EN                             ACTIVE WHEN ONE !
58
59              ;       USED IN STEP    53,54,55,206,214.
```

```
10032 .MAIN
01
02
03                  !       TEST MEM                        ACTIVE WHEN ZERO
04
05                  !       USED IN STEP    0,102,104,105,114,115,120,121,122,124,
06                  !                       125,126,151,166,210,213,220,230,232,
07                  !                       234,236.
08
09
10                  !       3 STATE EN                      ACTIVE WHEN ZERO
11
12                  !       USED IN STEP    2,3,4,5,6,7,10,11,12,13,14,15,17,20,21,
13                  !                       22,23,24,25,26,27,30,31,33,34,40,41,42,
14                  !                       43,44,45,46,47,50,51,52,53,54,55,56,62,
15                  !                       63,64,65,66,67,72,75,105,106,110,111,
16                  !                       116,120,123,124,126,130,131,133,135,137,
17                  !                       142,143,144,161,162,170,171,172,173,174,
18                  !                       206,210,216,217,220,221,225,237,240,241,
19                  !                       242,243.
```

```
10033 .MAIN
01
02
03              ; ALL USED RAR  COMMAND          FLOWCHART PAGE  FUNCTION
04
05
06              ;       0       START SWITCH     1       LOAD DATA REG, LED
07              ;                                        LOAD MAR
08              ;                                        TEST MEM
09              ;                                        RESTART ADDR
10
11              ;       1       FETCH INSTR      1       LOAD DATA REG, LED
12              ;                                        LOAD IR
13              ;                                        MEM READ
14
15              ;       2       JMP PAGE ZERO    2       3 STATE EN
16              ;                                        LOAD MAR
17              ;                                        BLOCK BIT 0
18
19              ;       3       JMP . (REL)      2       3 STATE EN
20              ;                                        LOAD MAR
21              ;                                        BLOCK BIT 0
22
23              ;       4       JMP 0,2 (INDEX)  2       3 STATE EN
24              ;                                        LOAD MAR
25              ;                                        BLOCK BIT 0
26
27              ;       5       JMP 0,3 (INDEX)  2       3 STATE EN
28              ;                                        LOAD MAR
29              ;                                        BLOCK BIT 0
30
31              ;       6       MEM REF INSTR    3       3 STATE EN
32              ;               PAGE ZERO                LOAD MAR
33              ;                                        BLOCK BIT 0
34
35              ;       7       MEM REF INSTR    3       3 STATE EN
36              ;               . (REL)                  LOAD MAR
37              ;                                        BLOCK BIT 0
38
39              ;       10      MEM REF INSTR    3       3 STATE EN
40              ;               0,2                      LOAD MAR
41
42              ;       11      MEM REF INSTR    3       3 STATE EN
43              ;               0,3                      LOAD MAR
44
45              ;       12      MEM REF INSTR    3       3 STATE EN
46              ;               @ PAGE ZERO              LOAD MAR
47              ;                                        BLOCK BIT 0
48
49              ;       13      MEM REF INSTR    3       3 STATE EN
50              ;               @ . (REL)                LOAD MAR
51              ;                                        BLOCK BIT 0
52
53              ;       14      MEM REF INSTR    3       3 STATE EN
54              ;               @ 0,2                    LOAD MAR
55              ;                                        BLOCK BIT 0
56
57              ;       15      MEM REF INSTR    3       3 STATE EN
58              ;               @ 0,3                    LOAD MAR
59              ;                                        BLOCK BIT 0
```

```
10034 .MAIN
21
22              ;       16      MEM REF INSTR   3       LOAD DATA REG, LED
23              ;               @ (INDIRECT)            MEM READ
24
25              ;       17      MEM REF INSTR   3       LOAD DATA REG, LED
26              ;               @ AUTO DEC, BIT 0=0     3 STATE EN
27
28              ;       20      MEM REF INSTR   3       LOAD DATA REG, LED
29              ;               @ AUTO INC, BIT 0=0     3 STATE EN
10              ;                                       CIN
11
12              ;       21      MEM REF INSTR   3       LOAD DATA REG, LED
13              ;               @ AUTO INC/DEC          3 STATE EN
14              ;               STORE ADDR              MEM WRITE
15
16              ;       22      MEM REF INSTR   3       3 STATE EN
17              ;               @ END                   LOAD MAR
18              ;                                       BLOCK BIT 0
19
20              ;       23      MEM REF INSTR   3       LOAD DATA REG, LED
21              ;               @ AUTO DEC, BIT 0=1     3 STATE EN
22
23              ;       24      MEM REF INSTR   3       LOAD DATA REG, LED
24              ;               @ AUTO INC, BIT 0=1     3 STATE EN
25              ;                                       CIN
26
27              ;       25      MEM REF INSTR   3       LOAD DATA REG, LED
28              ;               @ AUTO INC/DEC          3 STATE EN
29              ;               STORE ADDR              MEM WRITE
30
31              ;       26      MEM REF INSTR   3       3 STATE EN
32              ;               @ LOOP                  LOAD MAR
33
34              ;       27      JSR             4       LOAD DATA REG, LED
35              ;                                       3 STATE EN
36              ;                                       CIN
37
38              ;       30      JSR             4       LOAD DATA REG, LED
39              ;                                       3 STATE EN
40
41              ;       31      JMP @, JSR      4       3 STATE EN
42              ;                                       LOAD MAR
43              ;                                       BLOCK BIT 0
44
45              ;       32      LDA             4       LOAD DATA REG, LED
46              ;                                       GATE ACN
47              ;                                       MEM READ
48
49              ;       33      STA             4       LOAD DATA REG, LED
50              ;                                       GATE ACN
51              ;                                       3 STATE EN
52              ;                                       MEM WRITE
53
54              ;       34      I/O             6       3 STATE EN
55              ;               END                     CIN
56              ;                                       LOAD MAR
57              ;                                       BLOCK BIT 0
```

```
!0035 .MAIN
01
02                ;       35      ISZ             4       LOAD DATA REG, LED
03                ;                                       CIN
04                ;                                       MEM READ
05
06                ;       36      DSZ             4       LOAD DATA REG, LED
07                ;                                       MEM READ
08
09                ;       37      ISZ/DSZ         4       LOAD DATA REG, LED
10
11                ;       40      ISZ/DSZ         4       LOAD DATA REG, LED
12                ;                                       3 STATE EN
13                ;                                       MEM WRITE
14
15                ;       41      ALU             5       3 STATE EN
16                ;               END                     CIN
17                ;                                       LOAD MAR
18                ;                                       BLOCK BIT 0
19
20                ;       42      COM             5       LOAD DATA REG, LED
21                ;                                       GATE ACN
22                ;                                       3 STATE EN
23                ;                                       ALC CON
24
25                ;       43      NEG             5       LOAD DATA REG, LED
26                ;                                       GATE ACN
27                ;                                       3 STATE EN
28                ;                                       ALC CON
29                ;                                       CIN
30
31                ;       44      MOV             5       LOAD DATA REG, LED
32                ;                                       GATE ACN
33                ;                                       3 STATE EN
34                ;                                       ALC CON
35
36                ;       45      INC             5       LOAD DATA REG, LED
37                ;                                       GATE ACN
38                ;                                       3 STATE EN
39                ;                                       ALC CON
40                ;                                       CIN
41
42                ;       46      ADC             5       LOAD DATA REG, LED
43                ;                                       GATE ACN
44                ;                                       3 STATE EN
45                ;                                       ALC CON
46
47                ;       47      SUB             5       LOAD DATA REG, LED
48                ;                                       GATE ACN
49                ;                                       3 STATE EN
50                ;                                       ALC CON
51                ;                                       CIN
52
53                ;       50      ADD             5       LOAD DATA REG, LED
54                ;                                       GATE ACN
55                ;                                       3 STATE EN
56                ;                                       ALC CON
```

```
!0036 .MAIN
01
02              ;       51      AND             5       LOAD DATA REG, LED
03              ;                                       GATE ACN
04              ;                                       3 STATE EN
05              ;                                       ALC CON
06
07              ;       52      ALU SWAP        5       LOAD DATA REG, LED
08              ;                                       3 STATE EN
09
10              ;       53      ALU SWAP        5       LOAD DATA REG, LED
11              ;                                       3 STATE EN
12              ;                                       SWAP EN
13
14              ;       54      ALU SWAP        5       LOAD DATA REG, LED
15              ;                                       3 STATE EN
16              ;                                       SWAP EN
17
18              ;       55      ALU SWAP        5       LOAD DATA REG, LED
19              ;                                       3 STATE EN
20              ;                                       SWAP EN
21
22              ;       56      ALU             5
23
24              ;       60      DIX             6       LOAD DATA REG, LED
25              ;                                       GEN IODT
26              ;                                       GATE IN
27
28              ;       61      DIX             6       LOAD DATA REG, LED
29              ;                                       GATE ACN
30              ;                                       GEN IODT
31              ;                                       GATE IN
32
33              ;       62      ALU SHIFT LEFT  5       LOAD DATA REG, LED
34              ;                                       3 STATE EN
35
36              ;       63      ALU SHIFT RIGHT 5       LOAD DATA REG, LED
37              ;                                       3 STATE EN
38
39              ;       64      ALU SHIFT L, #  5       LOAD DATA REG, LED
40              ;                                       3 STATE EN
41
42              ;       65      ALU SHIFT R, #  5       LOAD DATA REG, LED
43              ;                                       3 STATE EN
44
45              ;       66      ALU SHIFT       5       LOAD DATA REG, LED
46              ;                                       GATE ACN
47              ;                                       3 STATE EN
48
49              ;       67      ALU SHIFT #     5       LOAD DATA REG, LED
50              ;                                       3 STATE EN
51
52              ;       70      I/O START       6
53
54              ;       71      DIX             6       LOAD DATA REG, LED
55              ;                                       GATE ACN
56              ;                                       GEN IODT
57              ;                                       GATE IN
```

```
10037 .MAIN
01
02              ;       72      DOX             6       LOAD DATA REG, LED
03              ;                                       GATE ACN
04              ;                                       3 STATE EN
05
06              ;       73      NIO             6       GEN IODT
07
08              ;       74      I/O             6
09
10              ;       75      I/O SKIP END    6       3 STATE EN
11              ;                                       CIN
12              ;                                       LOAD MAR
13              ;                                       BLOCK BIT 0
14
15              ;       76      DMA START       7
16
17              ;       77      DMA             7       LOAD MAR
18              ;                                       GATE IN
19
20              ;       100     DMA IN          8       LOAD DATA REG, LED
21
22              ;       101     DMA OUT         8       LOAD DATA REG, LED
23              ;                                       MEM READ
24              ;                                       GATE OUT
25
26              ;       102     DMA INC MEM     8       LOAD DATA REG, LED
27              ;                                       CIN
28              ;                                       MEM READ
29              ;                                       TEST MEM
30
31              ;       103     DMA ADD TO MEM  8       LOAD DATA REG, LED
32
33              ;       104     DMA ADD TO MEM  8       LOAD DATA REG, LED
34              ;                                       MEM READ
35              ;                                       TEST MEM
36
37              ;       105     DMA MEM         8       LOAD DATA REG, LED
38              ;                                       3 STATE EN
39              ;                                       TEST MEM
40              ;                                       MEM WRITE
41              ;                                       GATE OUT
42
43              ;       106     DMA END         8       3 STATE EN
44              ;                                       LOAD MAR
45              ;                                       BLOCK BIT 0
46
47              ;       107     INTR            7       LOAD IR
48              ;                                       LOAD MAR
49
50              ;       110     INTR            7       LOAD DATA REG, LED
51              ;                                       3 STATE EN
52              ;                                       BLOCK BIT 0
53              ;                                       MEM WRITE
54
55              ;       111     INTR            7       3 STATE EN
56              ;                                       CIN
57              ;                                       LOAD MAR
```

```
10038 .MAIN
01
02              ;       114     APL             9       LOAD MAR
03              ;                                       TEST MEM
04              ;                                       GATE APL ADDR
05
06              ;       115     APL             9       LOAD DATA REG, LED
07              ;                                       TEST MEM
08              ;                                       MEM WRITE
09              ;                                       GATE APL DATA
10
11              ;       116     REG EXAM        9       LOAD DATA REG, LED
12              ;                                       FP OP END
13              ;                                       PAN ACN EN
14              ;                                       GATE ACN
15              ;                                       3 STATE EN
16
17              ;       117     REG DEPO        9       LOAD DATA REG, LED
18              ;                                       GATE DATA SW
19              ;                                       FP OP END
20              ;                                       PAN ACN EN
21              ;                                       GATE ACN
22
23              ;       120     MEM EXAM NEXT   9       3 STATE EN
24              ;                                       CIN
25              ;                                       LOAD MAR
26              ;                                       TEST MEM
27
28              ;       121     MEM EXAM        9       GATE DATA SW
29              ;                                       LOAD MAR
30              ;                                       TEST MEM
31
32              ;       122     MEM EXAM        9       LOAD DATA REG, LED
33              ;                                       FP OP END
34              ;                                       MEM READ
35              ;                                       TEST MEM
36
37              ;       123     MEM DEPO NEXT   9       LOAD DATA REG, LED
38              ;                                       3 STATE EN
39              ;                                       CIN
40
41              ;       124     MEM DEPO        9       3 STATE EN
42              ;                                       LOAD MAR
43              ;                                       TEST MEM
44
45              ;       125     MEM DEPO        9       LOAD DATA REG, LED
46              ;                                       GATE DATA SW
47              ;                                       FP OP END
48              ;                                       TEST MEM
49              ;                                       MEM WRITE
50
51              ;       126     FRONT PANEL END 9       3 STATE EN
52              ;                                       LOAD MAR
53              ;                                       TEST MEM
54              ;                                       BLOCK BIT 0
55
56              ;       127     FRONT PANEL BEG 9       GATE REG EN, AC ADDR
57              ;                                       LOAD IR
```

```
10039 .MAIN
31
32              ;       130     PC SKIP         1       3 STATE EN
33              ;                                       CIN
34              ;                                       LOAD MAR
35
36              ;       131     ISZ/DSZ END     4       3 STATE EN
37              ;                                       CIN
38              ;                                       LOAD MAR
39              ;                                       BLOCK BIT 0
10
11              ;       132     I/O SKIP        6
12
13              ;       133     DMA IN          8       LOAD DATA REG, LED
14              ;                                       3 STATE EN
15              ;                                       MEM WRITE
16
17              ;       134     APL             9       CIN
18
19              ;       135     BREAK           10      3 STATE EN
20              ;                                       CIN
21
22              ;       136     BREAK           10
23
24              ;       137     BREAK           10      3 STATE EN
25              ;                                       CIN
26
27              ;       140                     10
28
29              ;       141     BREAK           10
30
31              ;       142     BREAK           10      LOAD DATA REG, LED
32              ;                                       LOAD IR
33              ;                                       3 STATE EN
34
35              ;       143     BREAK           10      LOAD DATA REG, LED
36              ;                                       LOAD IR
37              ;                                       3 STATE EN
38
39              ;       144     BREAK           10      3 STATE EN
40              ;                                       CIN
41
42              ;       145     BREAK           10
43
44              ;       146     DMA             7
45
46              ;       147     DMA             7
47
48              ;       150     BREAK           10      LOAD IR
49
50              ;       151     BREAK           10      TEST MEM
51
52              ;       152     DMA             7
53
54              ;       153     DMA IN          8
55
56              ;       154     DMA IN          8
57
58              ;       155     DMA IN          8       GATE IN
```

```
!0040 .MAIN
01
02              ;       156     DMA OUT         8       MEM READ
03              ;                                       GATE OUT
04
05              ;       157     DMA OUT         8       MEM READ
06              ;                                       GATE OUT
07
08              ;       160     DMA OUT         8       MEM READ
09              ;                                       GATE OUT
10
11              ;       161     DMA INCR        8       3 STATE EN
12              ;                                       GATE OUT
13
14              ;       162     DMA INCR        8       3 STATE EN
15              ;                                       MEM WRITE
16              ;                                       GATE OUT
17
18              ;       163     DMA INCR        8       MEM WRITE
19              ;                                       GATE OUT
20
21              ;       164     DMA ADD TO MEM  8
22
23              ;       165     DMA ADD TO MEM  8
24
25              ;       166     DMA ADD TO MEM  8       TEST MEM
26              ;                                       GATE IN
27
28              ;       167     DIX             6
29
30              ;       170     DOX             6       GATE ACN
31              ;                                       3 STATE EN
32              ;                                       GATE OUT
33
34              ;       171     DOX             6       GATE ACN
35              ;                                       3 STATE EN
36              ;                                       GEN IODT
37              ;                                       GATE OUT
38
39              ;       172     DOX             6       GATE ACN
40              ;                                       3 STATE EN
41              ;                                       GEN IODT
42              ;                                       GATE OUT
43
44              ;       173     DOX             6       GATE ACN
45              ;                                       3 STATE EN
46              ;                                       GEN IODT
47              ;                                       GATE OUT
48
49              ;       174     DOX             6       GATE ACN
50              ;                                       3 STATE EN
51              ;                                       GATE OUT
52
53              ;       175     I/O             6
54
55              ;       176     I/O             6
56
57              ;       177     NIO             6       GEN IODT
```

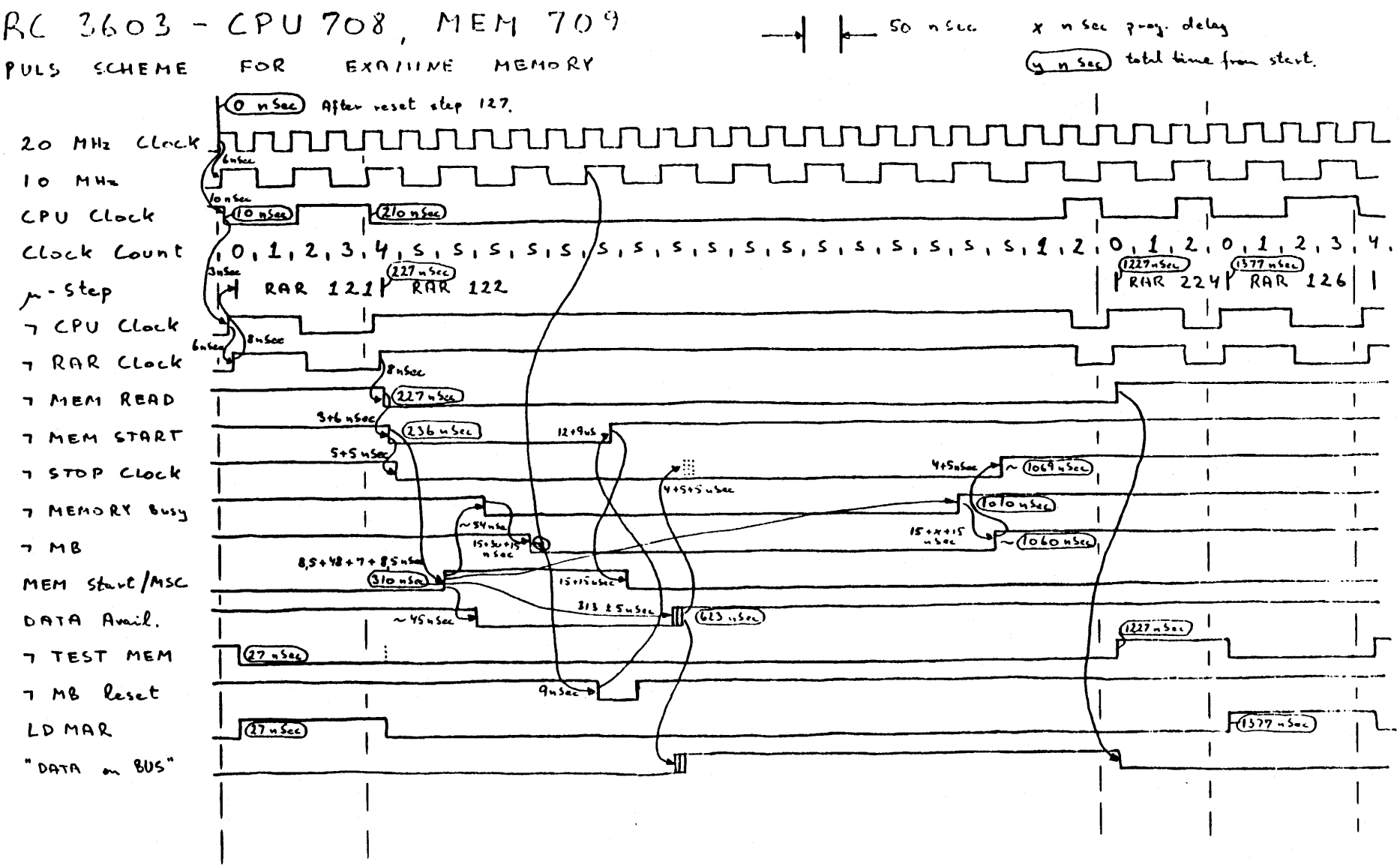
```
10041 .MAIN
01
02              ;       200     NIO             6       GEN IODT
03
04              ;       201     NIO             6       GEN IODT
05
06              ;       202     I/O SKIP        6
07
08              ;       205     I/O SKIP        6
09
10              ;       206     ALU SWAP        5       3 STATE EN
11              ;                                       SWAP EN
12
13              ;       207     START SWITCH    9       RESTART ADDR
14
15              ;       210     POWER           1       3 STATE EN
16              ;                                       LOAD MAR
17              ;                                       TEST MEM
18
19              ;       211     EXT MEM         6
20
21              ;       212     EXT MEM         6
22
23              ;       213     POWER           1       TEST MEM
24              ;                                       RESTART ADDR
25
26              ;       215     DMA INCR        8
27
28              ;       217     LDA/STA END     4       LOAD DATA REG, LED
29              ;                                       3 STATE EN
30              ;                                       CIN
31              ;                                       LOAD MAR
32              ;                                       BLOCK BIT 0
33
34              ;       221     BREAK           10      3 STATE EN
35              ;                                       CIN
36
37              ;       222     BREAK           10
38
39              ;       223     BREAK           10
40
41              ;       224     MEM EXAM        9
42
43              ;       225     BREAK           10      3 STATE EN
44              ;                                       CIN
45
46              ;       226     ALU SWAP        5       PAN ACN EN
47
48              ;       227     ALU SWAP        5       GATE ACN
49
50              ;       231     BREAK           10
51
52              ;       232     BREAK           10      TEST MEM
53
54              ;       233     BREAK           10
55
56              ;       234     BREAK           10      TEST MEM
57
58              ;       235     BREAK           10
```

```
10042 .MAIN
31
32              ;       236     BREAK           10      TEST MEM
33
34              ;       237     MEM REF INSTR   3       3 STATE EN
35              ;               @ AUTO INC/DEC          MEM WRITE
36
37              ;       240     MEM REF INSTR   3       3 STATE EN
38              ;               @ AUTO INC/DEC          MEM WRITE
39
10              ;       241     STA             4       GATE ACN
11              ;                                       3 STATE EN
12              ;                                       MEM WRITE
13
14              ;       242     INTR            7       3 STATE EN
15              ;                                       BLOCK BIT 0
16              ;                                       MEM WRITE
17
18              ;       243     ISZ/DSZ         4       3 STATE EN
19              ;                                       MEM WRITE
20
21              ;       244     DMA IN          8
22
23              ;       245     RESTART         7       LOAD IR
24
25              ;       246     RESTART         7       RESTART ADDR
26
27              ;       247     RESTART         7       RESTART ADDR
28
29              ;       250     REG DEPO        9       LOAD DATA REG, LED
30              ;                                       GATE DATA SW
31              ;                                       FP OP END
32              ;                                       PAN ACN EN
33              ;                                       GATE ACN
34
35              ;               160 MIKROSTEP USED.
```

```
10043 .MAIN
01
02
03
04
05
06                ;           ****    ********************************************
07                ;           *       *                                          *
08                ;           ***     *   F:   PULS SCHEMES FOR MEMORY CONTROL   *
09                ;           *       *                                          *
10                ;           *       ********************************************
11
12
13                ;       HERE FOLLOWS TWO PULS SCHEMES,
14                ;                ONE FOR EXAMINE MEMORY FROM TCP 701,
15                ;                ONE FOR JMP .+0 INSTRUCTION.
16                ;       USEFULL WHEN MEMORY CONTROL SIGNALS ARE TO BE CHECKED.
```

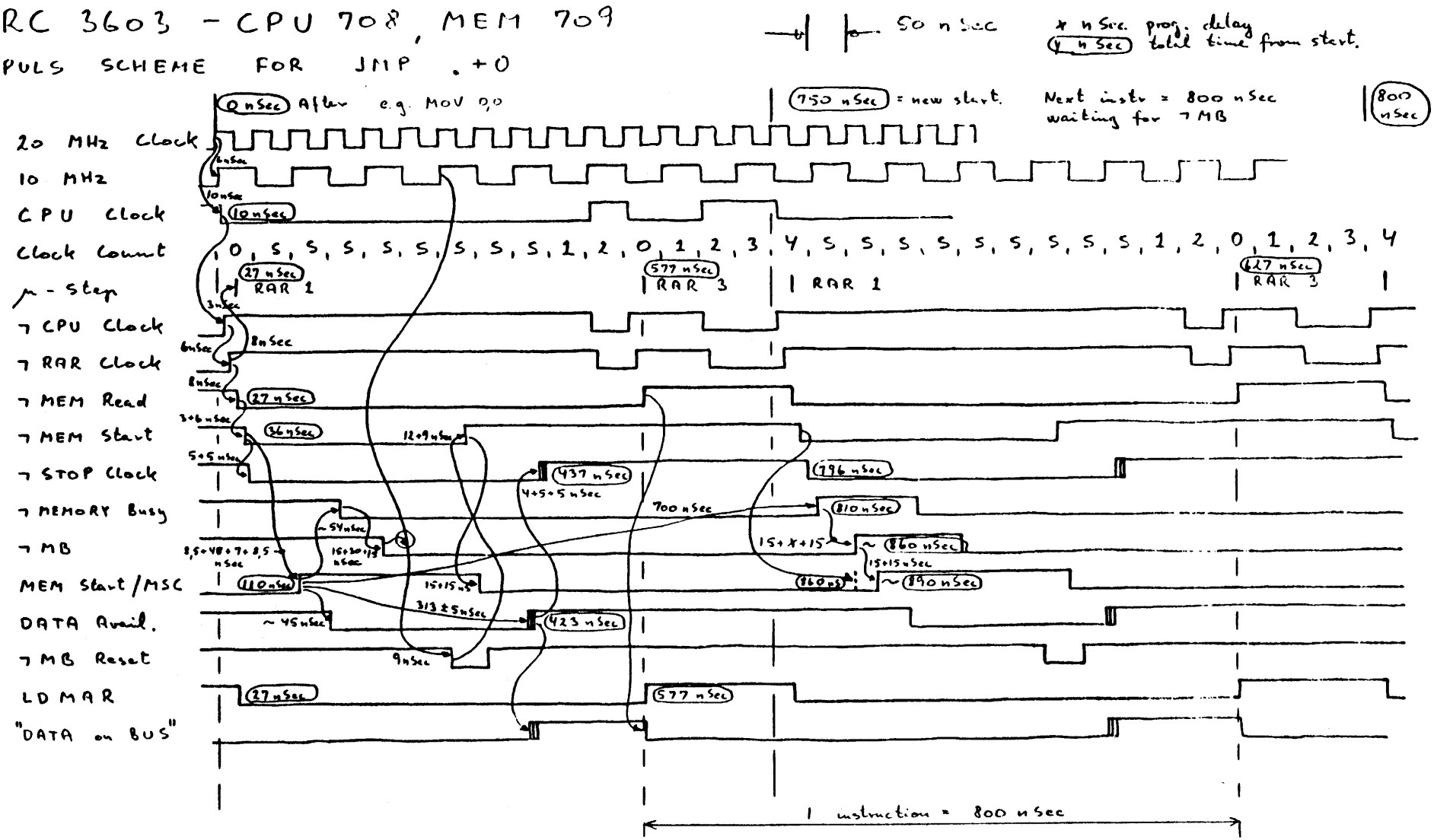
RC 3603 - CPU 708, MEM 709

PULS SCHEME FOR EXAMINE MEMORY



RC 3603 - CPU 708, MEM 709

PULS SCHEME FOR JMP .+0



MEM START/MSC WILL GO TO "1" ABOUT (15+48+15+15) nSec after ¬ MEM Start ‾|_ and about (15+15) n Sec after ¬ MB _|‾. Both signals should be present. It looks like an instruction time of 750 n Sec, but it is delayed until ¬ MB starts next MEM cycle. Because of ¬ STOP Clock the instruction time is a multiplum of 50 n Sec.

```
10046 .MAIN
01
02
03
04
05
06                ;            ***    ****************************************
07                ;          *        *                                      *
08                ;          * **     *   G:   INSTRUCTION MIKROSTEP FLOW/   *
09                ;          *  *     *           TIME CONSUMPTION           *
10                ;           ***     ****************************************
11
12
13                ;       THIS INFORMATION IS INTENDED FOR USE IF YOU WANT A FAST
14                ;       SURVEY OF DIFFERENT INSTRUCTION TYPES CONCERNING
15                ;       MIKROPROGRAM FLOW:
16                ;       WHICH STEPS AND THEIR TIME CONSUMPTION.
17                ;       FOLLOWING INSTRUCTIONS SHOWN:
18
19                ;       JMP
20                ;       JMP      @
21                ;       JMP      @@
22                ;       JSR
23                ;       ISZ/DSZ
24                ;       ISZ/DSZ  @
25                ;       JSR      @
26                ;       JSR      @@
27                ;       LDA
28                ;       LDA      @
29                ;       LDA      @@
30                ;       LDA      @ AUTO INC/DEC
31                ;       STA
32                ;       STA      @
33                ;       STA      @@
34                ;       STA      @ AUTO INC/DEC
35                ;       COM      (+SKIP)
36                ;       COMR
37                ;       COMS
38                ;       COMS#
39                ;       DIA
40                ;       DOA
41                ;       NIO
42                ;       SKPBZ    (+SKIP)
43
44                ;       LAST PAGE IS A COMPLETE INSTRUCTION TIMES SCHEME.
45                ;       IF INSTRUCTION TIMES ARE NOT CORRECT USE INSTR.
46                ;       TIMER TEST (44-RT 1557) AND READ PAGE 3 LINES 12-15.
47                ;       NOTE:  THERE ARE NO STANDARD FOR INSTR. TIMES.
```

RC 3603 Instruction Time in μ-Step.

← → 100 nSec | ONE μ Step | ONE Memory Cycle
16K = 700 nSec
32K = 800 nSec

FETCH 16K = 500 nSec
32K = 550 nSec

"MINIMUM" TIME SHOWN
VARIATION ~ 50 nSec / MEM Cycle

JMP

FETCH		
RAR 1	1	3

16K = 700 nSec

FETCH		
RAR 1	1	3

32K = 800 nSec

JMP @

FETCH			FETCH		
RAR 1	1	12	16	22	31

16K = 1600 nSec

FETCH			FETCH		
RAR 1	1	12	16	22	31

32K = 1750 nSec

JMP @@

FETCH			FETCH			FETCH		
RAR 1	1	12	16	1	26	16	22	31

16K = 2300 nSec

FETCH			FETCH			FETCH		
RAR 1	1	12	16	1	26	16	22	31

32K = 2550 nS

JSR

FETCH				
RAR 1	1	6	27	30	31

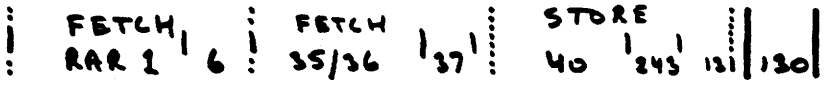
16K = 1200 nSec

FETCH				
RAR 1	1	6	27	30	31

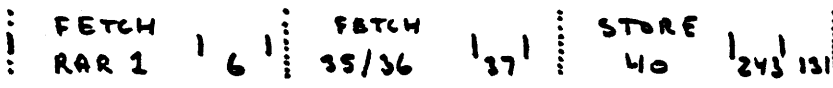
32K = 1250 nSec

ISZ, DSZ

SKIP



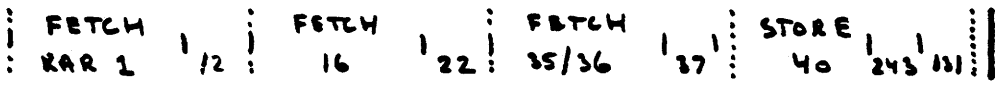
16K = 2150 nSec
SKIP = +200 nSec



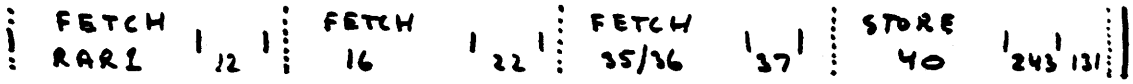
32K = 2450 nSec
SKIP = +200 nSec

ISZ, DSZ @

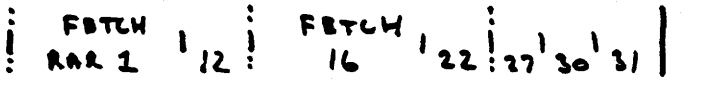
16K = 2850 nSec



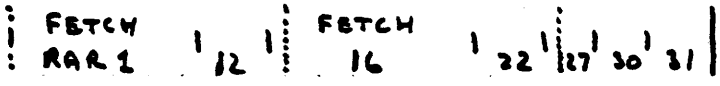
32K = 3250 nSec



JSR @



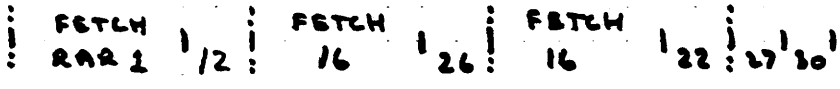
16K = 1900 nSec



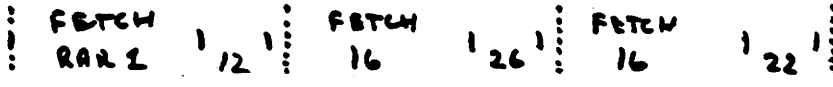
32K = 2050 nSec

JSR @@

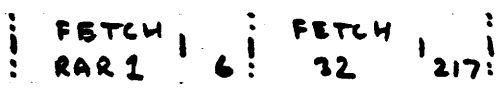
16K = 2600 nSec



32K = 2850 nSec



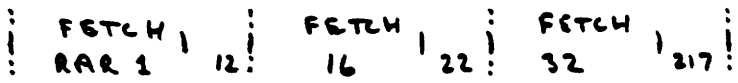
LDA



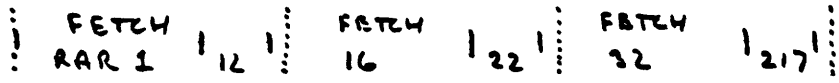
16K = 1400 nSec

32K = 1600 nSec

LDA @



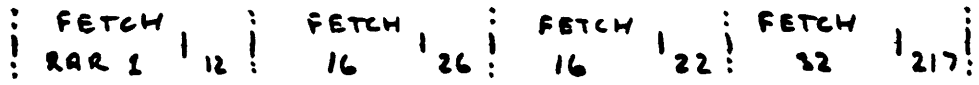
16K = 2100 nSec



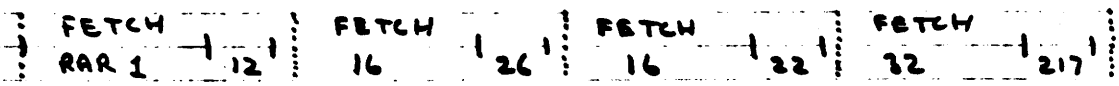
32K = 2400 nSec

LDA @@

16K = 2800 nSec

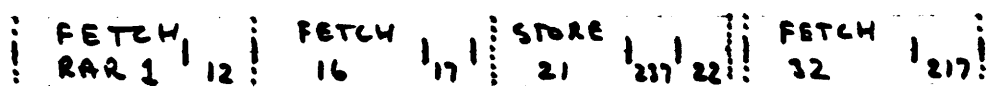


32K = 3200 nSec

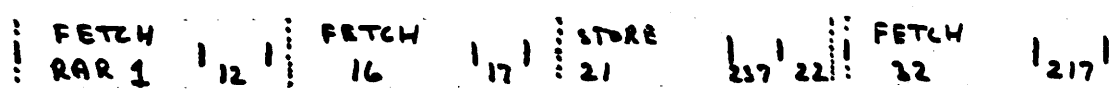


LDA @ Auto inc/dec

16K = 2850 nSec



32K = 3250 nSec



STA

FETCH RAR 1	6	STORE 33	241	217

16 K = 1450 u Sec

FETCH RAR 1	6	STORE 33	241	217

32 K = 1650 u Sec

STA @

FETCH RAR 1	12	FETCH 16	22	STORE 33	241	217

16 K = 2150 u Sec

FETCH RAR 1	12	FETCH 16	22	STORE 33	241	217

32 K = 2450 u Sec

STA @@

16 K = 2850 u Sec

FETCH RAR 1	12	FETCH 16	26	FETCH 16	22	STORE 33	241	217

32 K = 3250 u Sec

FETCH RAR 1	12	FETCH 16	26	FETCH 16	22	STORE 33	241	217

STA @ Auto inc/dec

16 K = 2900 u Sec

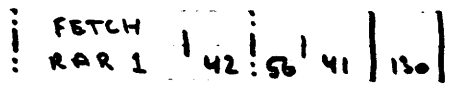
FETCH RAR 1	12	FETCH 16	17	STORE 21	217	22	STORE 33	241	217

32 K = 3300 u Sec

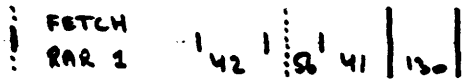
FETCH RAR 1	12	FETCH 16	17	STORE 21	217	22	STORE 33	241	217

COM

SKIP

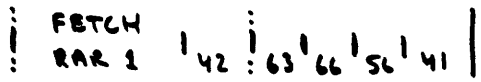


16 K = 1050 μSec
SKIP = + 200 μSec

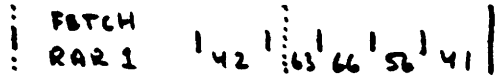


32 K = 1100 μSec
SKIP = + 200 μSec

COMR

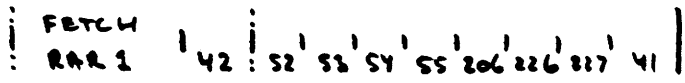


16 K = 1350 μSec

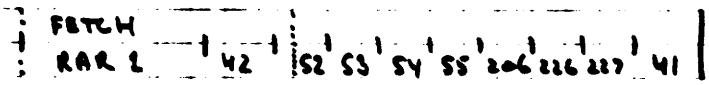


32 K = 1400 μSec

COMS

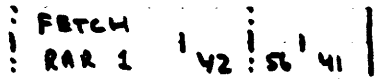


16 K = 1950 μSec

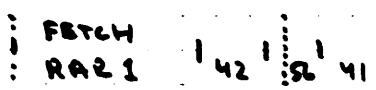


32 K = 2000 μSec

COMS



16 K = 1050 μSec



32 K = 1100 μSec

DIA

FETCH RAR 1	70 | 71 | 60 | 61 | 167 | 175 | 176 | 74 | 34		16 K = 1950 u Sec
FETCH RAR 1	70 | 71 | 60 | 61 | 167 | 175 | 176 | 74 | 34		32 K = 2000 u Sec

DOA

FETCH RAR 1	70 | 72 | 170 | 171 | 173 | 174 | 175 | 176 | 74 | 34		16 K = 2100 u Sec +150 2250
		172 FCO 11-021	
FETCH RAR 1	70 | 72 | 170 | 171 | 173 | 174 | 175 | 176 | 74 | 34		32 K = 2150 u Sec +150 2300

NIO

FETCH RAR 1	70 | 73 | 177 | 200 | 201 | 175 | 176 | 74 | 34		16 K = 1950 u Sec
FETCH RAR 1	70 | 73 | 177 | 200 | 201 | 175 | 176 | 74 | 34		32 K = 2000 u Sec

SKPBZ

SKIP

FETCH RAR 1	70 | 132 | 202 | 205 | 75 | 130		16 K = 1350 u Sec SKIP = +200 u Sec
FETCH RAR 1	70 | 132 | 202 | 205 | 75 | 130		32 K = 1400 u Sec SKIP = +200 u Sec

RC 3603 Instruction Execution Times in nSec

Instruction Mnemonic	RC 3609 16K	RC 3608 32K	RC 3609 16K-BREAK	RC 3608 32K-BREAK
JMP	700-750	800-850	1550	1600
1. level of @, add	900	950	900	1000
each further more levels, add	700	800	700	800
JSR	1200	1250	2050	2100
ISZ, DSZ	2100-2200	2400-2600	3000-3100	3200-3400
LDA	1400-1450	1600-1700	1950-2000	2100-2200
STA	1450-1500	1600-1750	2000-2100	2100-2300
each level of @, add	700-750	800-850	700-750	800-850
each auto index, add	700-750	800-850	700-750	800-850
index register addr., add	0	0	0	0
if skip occurs, add	200	200	200	200
COM, NEG, MOV, INC				
ADC, SUB, ADD, AND	1050	1100	1900	1950
Shift R, L, R#, L#, add	300	300	300	300
Swap, add	900	900	900	900
Swap #, R# SKP, L# SKP, add	0	0	0	0
if skip occurs, add	200	200	200	200
I/O INPUT (incl Reads, INTA)	1950	2000	2800	2850
I/O OUTPUT (incl MSKO)	2250 FCO 11-0021: ~~2100~~	2300 ~~2150~~	3100 ~~2950~~	3150 ~~3000~~
NIO (incl INTEN, INTDS)	1950	2000	2800	2850
I/O SKP	1350	1400	2200	2250
if skip occurs, add	200	200	200	200
for S, C, P add	0	0	0	0
DICP dev # 1	1250	1300	2100	2150
All other dev # 1 blind	1100	1150	1950	2000

```
10054 ,MAIN
01
02
03
04
05
06                ;            *  *    ****************************************
07                ;            *  *    *                                      *
08                ;            ****    *   H:   ROM TYPE/POSITION LIST        *
09                ;            *  *    *                                      *
10                ;            *  *    ****************************************
11
12
13                ;       THIS LIST IS HANDY IF THE ROM TYPE IN THE CPU IS NOT
14                ;       THE SAME AS IN THE DIAGRAMS AND IF A SIGNAL/FUNCTION
15                ;       IS SUSPECT, WHICH ROM THEN TO REPLACE.
```

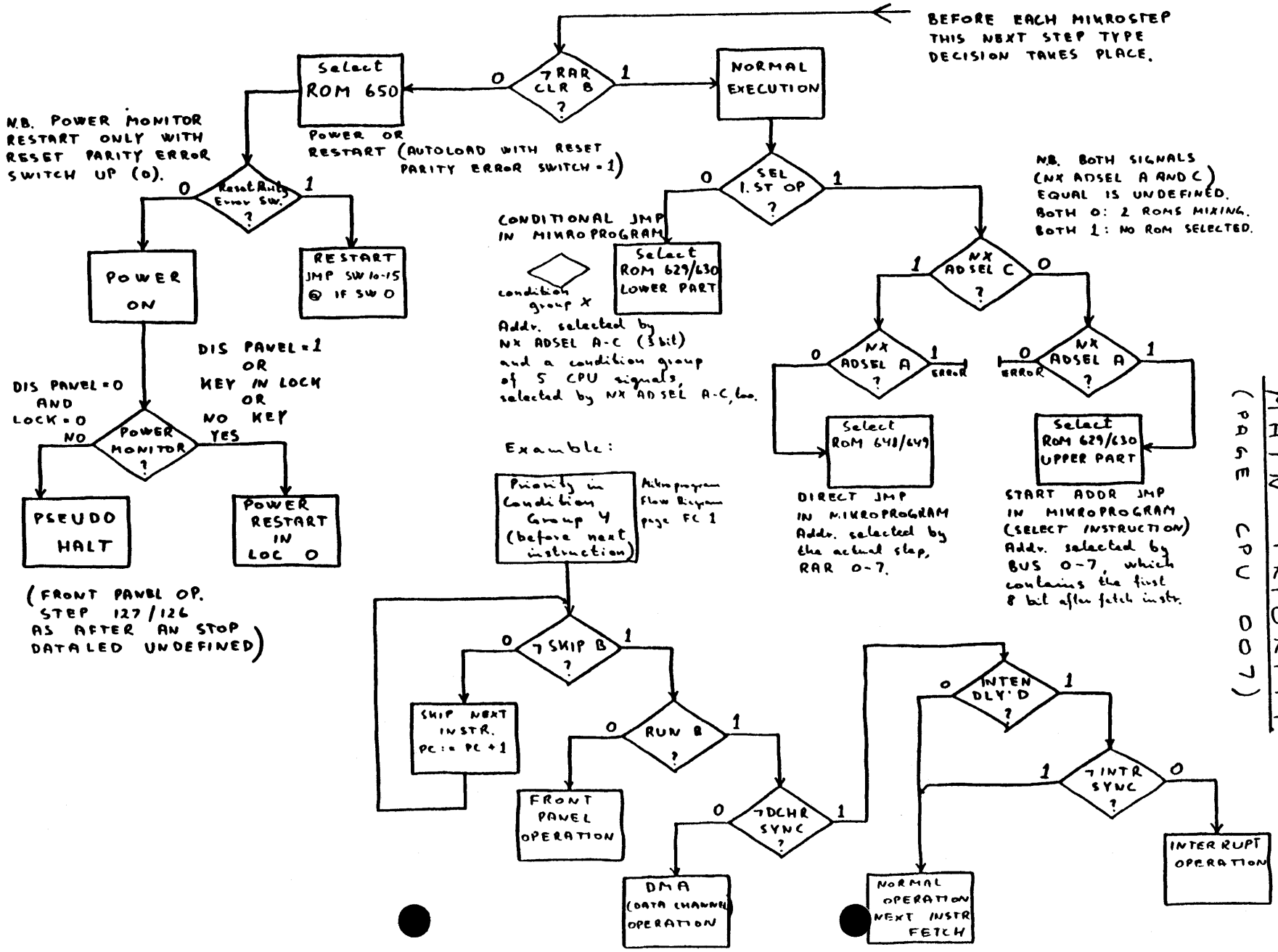
CPU 708 ROM TYPE AND POS.

SIGNAL FUNCTION	ROM #, ECO	CPU DIAGRAM			PROM LIST PAGE (P = CPU)
NXAD 0-7, DIRECT J'MP	619, 648, 707 620, 649, 708, 755	007	74S287	256×4	54
NXAD 0-7, COND. JMP + INSTR.	630 629	007	6306	512×4	↑ 31-38 ↑ 47-49
POWER REST	632, 650	007	74S288	32×8	↑ 50
BUS CONTR MEM WRITE ALU CONTR DATA CH + INTR	625, 663 624, 664, 762	009	74S287	256×4	1
APL ADDR MEM READ ALU CONTR	623 628, 662	010	74S287	256×4	1
NEXT ADDR SEL	617, 660	011	74S287	256×4	36
NEXT ADDR SEL BREAK	637, 661	011	74S287	256×4	45
APL DATA SKIP EN RQ ENB (DATACH + INTR) 3 STATE EN (ALU DATA)	626, 659	011	74S287	256×4	10
SHIFT, SWAP DATA CH	621, 658 622	012	74S287	256×4	10
AC A/B SEL INSTR.	606, 763	013	74S288	32×8	↑ 84
AC A SEL AC B SEL	607, 656 608, 657	013	74S287	256×4	54
BLOCK BIT 0 RESTART ADDR GATE I/O	610, 654	014	74S287	256×4	10
ALU COMMAND FETCH	609, 655	014	74S287	256×4	36
ALU COMMAND TEST MEM	611, 652, 760 612, 653, 761	015	74S287	256×4	36
FPOP END BUS CONTR.	613, 651	016	74S287	256×4	19
CARRY, SHIFT	631	016	6306	512×4	↑ 54-6
SKIP	614	018	74S287	256×4	28 + ↑ 65-66
DEV. CODE	615	033	74S287	256×4	28
FRONT PANEL	616	035	74S288	32×8	↑ 71
EXT, BIT 0 EN 'BREAK DEFER	627, 665	041	74S287	256×4	19

AUTOLOAD/PROGR LOAD	ROM #	RC PART #	CPU DIAGRAM	
MTC (30, 44) PTR (12), FPA (46)	007 008	47116 47117	022 74188 022 74S188 74S288	32×8
CDR (16)	005 006	55401 55402		
DKP (73)	026 027		DSC (20)	410 411
FDD (61)	037 038	50515 50516		

```
10056 .MAIN
01
02
03
04
05
06                ;          *****    ****************************************
07                ;            *      *                                      *
08                ;            *      *   I:   MIKROPROGRAM MAIN PRIORITY    *
09                ;            *      *                                      *
10                ;          *****    ****************************************
11
12
13                ;       THIS SCHEME IS MADE MAINLY FOR UNDERSTANDING THE
14                ;       CPU DIAGRAM PAGE 007, AND THE MIKROPROGRAM FLOWCHART
15                ;       PAGE FC 1. IT SHOULD EXPLAIN WHICH PATH TO TAKE
16                ;       THROUGH THE MIKROPROGRAM.
17                ;       ONE CONDITION GROUP (4) IS SHOWN TO EXPLAIN THE
18                ;       PRIORITY BETWEEN NORMAL INSTRUCTIONS AND DATACHANNEL,
19                ;       INTERRUPT ETC.
```

CPU 708 MIKROPROGRAM MAIN PRIORITY (PAGE CPU 007)



```
10058 .MAIN
01
02
03
04
05
06                ;            **      ****************************************
07                ;           * *      ***                                  ***
08                ;             *      ***    2:   NOVA 2 STATIC TEST       ***
09                ;            *       ***                                  ***
10                ;           ****     ****************************************
11
12
13                ;       THIS PART IS USED TO TEST THE FRONT PANEL
14
15                ;       OPERATIONS (EXAMINE, DEPOSIT ETC), A FEW SIMPLE
16
17                ;       INSTRUCTIONS AND THE NESSACARY HARDWARE TO READ BINARY
18
19                ;       TAPES FROM PTR.
20
21                ;       FOLLOW THE HINTS GIVEN IN THE DGC HARDWARE MANUAL FOR
22
23                ;       NOVA 2 CPU, OR FOLLOW THE PROCEDURE CPU 708 STATIC TEST
24
25                ;       KNOWING THAT NOT ALL ARE POSSIBLE, NO MIKROPROGRAM
26
27                ;       ADDRESS, NO BREAK, NO PARITY ON MEMORY, ONLY AC0-4 ETC.
28
29                ;       AFTER THIS GO TO 3: LOGIC TEST, PAGE XXXX.
30
31                ;       PLEASE READ ALTERNATIVE AFTER PARAGRAPH 6 IN DESCRIPTION
32
33                ;       FOR LOGIC TEST, CHAPTER 3.
```

```
!0059 .MAIN
01
02
03
04
05
06                ;          ***     ****************************************
07                ;             *    ***                                  ***
08                ;           **     ***    3:   LOGIC TEST               ***
09                ;             *    ***                                  ***
10                ;          ***     ****************************************
11
12
13                ;       THIS PART IS THE DESCRIPTION FOR THE BINARY TEST
14
15                ;       PROGRAM READ IN FROM PTR (FOR DISC, MAGTAPE ETC.
16
17                ;       SEE PARAGRAPH 6 BELOW).
18
19
20                ;       THE TAPE IS BUILD UP LIKE THIS:
21
22                ;       1. BLOCK:  S-BIN HEAD (BINARY LOADER)
23                ;       2. BLOCK:  ALL BINARY DATA READ BY BINARY LOADER
24                ;       3. BLOCK:  S-BIN HEAD
25                ;       4. BLOCK:  START BLOCK READ BY BINARY LOADER (,END BAUTO)
26
27                ;       S-BIN HEAD IS DESCRIBED IN RC 3600 PROGRAM LOAD FOR PTR,
28                ;                       RCSL 44 RT-1710
29                ;       WHEN LOADED THE BINARY LOADER IS STARTED AUTOMATICALLY.
30
31                ;       THE TEST IS DIVIDED INTO TWO PARTS:
32
33                ;       1. PART:  TESTING AUTOLOAD, POWER RESTART, RESTART ETC.
34                ;                       TOGETHER WITH THE OPERATOR.
35                ;       2. PART:  THE LOGIC TEST ITSELF WITHOUT OPERATOR.
36
37
38                ;       DO THIS:
39
40                ;       1.  LOAD THE PTR FROM START OF TAPE.
41                ;           KEY IN THE PROGRAM SELF, SEE ONE OF THE FOLLOWING
42                ;           PAGES, SA = 50, RSA = 50  (START, RESTART ADDR)
43
44                ;       A1: NOW BLOCK 1 AND 2 ARE READ IN, THE CONTROL IS GIV
45                ;           TO THE PROGRAM IN LABEL REBIN (LOC 220), WRITING
46
47                ;                       AUTOLOAD
48
49                ;       2.  CHECK THAT PROGRAM LOAD OPTION F01 IS INSTALLED:
50                ;               RC 3603: ROM 007/008 RC PART # 47116/47117
51                ;               NOVA 2:  ROM 022/023 RC PART # 55614/55615
52                ;           IF NOT START PROGRAM IN LABEL NOROM (251) AND
53                ;           GO TO PARAGRAPH 4.
54                ;           IF PRESENT: SET SWITCHES TO 000012 (PTR).
55                ;           PRESS AUTOLOAD ON OPERATORS CONTROL PANEL
56                ;           (OR RESET/AUTO OR PROGRAM LOAD ON CPU TECHN PANEL).
57
58                ;       A2: NOW BLOCK 3 AND 4 ARE READ IN, TKE CONTROL IS GIVEN
59                ;           TO THE PROGRAM IN LABEL BAUTO (LOC 232), BUT FIRST
60                ;           INSTRUCTION IS HALT. (IF NO TCP, SEE PAR 6).
```

```
0060 .MAIN
01
02              ;       3.  CHECK DATA LED = 063077, PRESS CONTINUE
03              ;           IF NO TCP, IT IS POSSIBLE TO RESTART, SEE PAR 6.
04
05              ;       A3: NOW LOC 0 - 37 ARE TESTED AFTER AUTOLOAD, IF ERRORS
06              ;           THE CPU WILL HALT, CONSULT THE LISTNING, AFTER
07              ;           TESTING THE MESSAGE OK IS WRITTEN, FOLLOWED BY
08
09              ;                       LOCK
10
11              ;       4.  IF KEY MOUNTED, TURN IT TO POSITION LOCKED.
12              ;           TURN MAIN POWER OFF/ON.
13              ;       A4: NOW THE POWER RESTART IS TESTED.
14              ;               NOTE ! ! !  CPU 708 WILL NOT PERFORM A POWER
15              ;               RESTART (JMP LOC 0) IF THE SWITCH "RESET PARITY
16              ;               ERROR" IS DOWN (ON). IN THAT CASE A RESTART IS
17              ;               PERFORMED (JMP @ SW10-15 OR JMP SW10-15 (SW0)).
18
19              ;           (IF CPU UNDER TEST IS NOVA 2 WITHOUT POWER MONITOR
20              ;           OPTION:     THE CPU HALTS.
21              ;                       SET SWITCHES = 000000
22              ;                       PRESS RESET/START)
23
24              ;           THEN THE MESSAGE POWER IS WRITTEN, FOLLOWED BY
25
26              ;                       RESTART
27
28              ;       5.  IF CPU 708:
29              ;               SET SWITCHES = 100077
30              ;               SET SWITCH "RESET PARITY ERROR" DOWN (ON)
31              ;               PRESS AUTOLOAD ON OPERATORS CONTROL PANEL
32              ;               (OR RESET/AUTO OR PROGRAMLOAD ON CPU TECHN PANEL)
33              ;               SET SWITCH "RESET PARITY ERROR" UP (OFF).
34              ;           IF NOVA 2:
35              ;               PRESS RESET
36              ;               SET SWITCHES TO 000101
37              ;               PRESS START
38
39              ;       A5: IN CPU 708 THE RESTART FEATURE IS TESTED, BUT IN
40              ;           NOVA 2 THE PROGRAM IS RESTARTED MANUALLY.
41              ;           THE MESSAGE OK IS WRITTEN AND PROCESSOR SHOULD
42              ;           CONTINUE TO RUN WITHOUT HALTING. TELETYPE SHOULD
43              ;           STUTTER FOR 60 CHARACTERS (DELETE), THEN THE MESSAGE
44              ;           "PASS" SHOULD OCCUR AND THE TEST SHOULD CONTINUE
45              ;           TO LOOP WITH THE TELETYPE RUNNING AT A SLOWER RATE,
46              ;           WRITING PASS WITH AN INTERVAL ABOUT 2 MINUTES,
47              ;           DEPENDING ON THE BAUD RATE.
48
49              ;       6.  RESTART:
50              ;           THE PROGRAM IS TO BE RESTARTED IN LOC 500 IF THE
51              ;           ABOVE PROCEDURE NOT IS WANTED AGAIN.
52              ;           RESTART POINTS (WITHOUT TCP), SEE 5 PAGES LATER,
53              ;           FROM LOC 40 AND ON.
54
55              ;       ALTERNATIVE:
56              ;           IF ONLY THE SECOND PART IS TO BE RUN, IT COULD BE
57              ;           LOADED FROM DISC, MAG. TAPE OR LOAD THE PROGRAM
58              ;           IN A WELL OPERATING MACHINE, MOVE THE MEMORY
59              ;           (THE LOWEST MODULE) CONTAINING THE TEST, TO THE CPU
60              ;           UNDER TEST AND START IN LOC 500.
```

```
0061 .MAIN
01
02                ;       7.  ERROR DESCRIPTION:
03                ;           DETECTED ERRORS WILL BE MANIFESTED BY A PROCESSOR
04                ;           HALT.
05                ;           RECORD THE STATE OF THE PROCESSOR AND REGISTERS AT
06                ;           THE TIME OF THE HALT. CONSULT THE LISTNING AT THE
07                ;           ADDRESS OF THE ERROR HALT FOR PROBABLE CAUSES OF THE
08                ;           FAILURE, CONSTRUCT A LOOP THAT WILL REPEAT THE
09                ;           FAILURE AND SCOPE AS REQUIRED. DO NOT PRESS CONTINUE
10                ;           BEFORE YOU ARE SURE THAT IT IS ALLOWED. IN MANY
11                ;           ERRORHALTS IT IS NOT POSSIBLE BECAUSE NEXT MEM LOC
12                ;           CONTAINS AN ADDR, NOT AN INSTRUCTION.
13
14                ;       8.  PROGRAM DESCRIPTION:
15                ;           FOLLOWING PROGRAM IS A COLLECTION OF SMALL TESTS,
16                ;           EACH TEST IN SEQUENCE BASED ON PREVIOUS TESTS
17                ;           WORKING AND DESIGNED TO TEST AS SMALL AN ADDITIONAL
18                ;           PIECE OF THE LOGIC AS POSSIBLE. THE COMMENTS
19                ;           CONCERNING HARDWARE SIGNALS ARE MOSTLY FOR NOVA 2,
20                ;           FOR CPU 708 THE COMMENT IN MOST CASES WOULD BE:
21                ;           CHANGE ROM DELIVERING SIGNALS FOR INSTRUCTION TESTED.
22
23
24                ;TAPE 2
25
26                .EOT
```

```
 0062 .MAIN
01
02                ;AUTOLOAD, A PROGRAM FOR AUTOMATIC PROGRAM LOAD, CONTAINED
03                ;IN TWO ROMS, SEE 2. IN ABOVE DESCRIPTION FOR NUMBERS.
04                ;THIS VERSION WILL HANDLE PTR (AND MTC (AND DKP DEV 73
05                ;IF ALLREADY AT TRACK ZERO, I. E. AFTER LOADING DISCPACK)).
06                ;THIS PROGRAM STARTS IN MEMORY LOC 0 AFTER AN AUTOLOAD.
07
08
09          000000 .LOC    0
10
11  00000 060477 ABEG:   READS   0         ;READ SWITCHES INTO AC0
12  00001 105120         MOVZL   0,1       ;ISOLATE DEVICE CODE
13  00002 124240         COMOR   1,1       ; =(DEVICE CODE - 1)
14
15  00003 010011 ALOOP:  ISZ     AOP1      ;COUNT DEVICE CODE IN ALL
16  00004 010031         ISZ     AOP2      ;I/O INSTRUCTIONS TO ACTUAL.
17  00005 010033         ISZ     AOP3      ;
18  00006 010014         ISZ     AOP4      ;
19  00007 125404         INC     1,1,SZR   ;DONE ?
20  00010 000003         JMP     ALOOP     ;NO, INCREMENT AGAIN
21                                         ;YES, START DEVICE
22  00011 060077 AOP1:   060077            ;(NIOS 0)=1, MTC=READ COMMAND (0)
23                                         ;AFTER RESET.
24  00012 030017         LDA     2,AC377   ;PUT JMP 377 INTO LOC 377 FOR LATER
25  00013 050377         STA     2,377     ;LOOPING, WAITING FOR MTC, DATACHANNEL
26  00014 063377 AOP4:   063377            ;(SKPBN 0)=1, BUSY ? IF MTC AND NOT
27                                         ;ONLINE: TERMINATED, NONBUSY.
28  00015 000011         JMP     AOP1      ;START AGAIN UNTIL MTC ONLINE.
29
30  00016 101102         MOVL    0,0,SZC   ;LOW SPEED DEVICE ? (SWITCH 0 = 0)
31  00017 000377 AC377:  JMP     377       ;NO, GO TO 377 AND WAIT FOR CHANNEL
32                                         ;NOW: CARRY = 0, AC1 = 0
33  00020 004031 ALOP2:  JSR     AGET1     ;GET A FRAME, AFTER RETURN: CARRY = 1
34  00021 101065         MOVC    0,0,SNR   ;IS IT NONZERO ? (SWAP CARRY TO 0)
35  00022 000020         JMP     ALOP2     ;NO, IGNORE AND GET ANOTHER BYTE.
36                                         ;YES, SYNCRONIZED,
37  00023 004030 ALOP4:  JSR     AGET      ;GET A FULL WORD (CARRY = 0)
38  00024 046027         STA     1,@AC77   ;STORE STARTING AT 100
39                                         ;FIRST WORD = 2'S COMPL OF WORD COUNT
40  00025 010100         ISZ     100       ;COUNT WORD, DONE ?
41  00026 000023         JMP     ALOP4     ;NO, GET ANOTHER WORD
42  00027 000077 AC77:   JMP     77        ;YES, FINISHED, JMP TO LAST WORD LOADED
43                                         ;LOC 27, LOCATION COUNTER AUTO INCRE.
44
45  00030 126420 AGET:   SUBZ    1,1       ;CLEAR AC1, SET CARRY
46               AGET1:
47               ALOP3:
48  00031 063577 AOP2:   063577            ;(SKPDN 0)=1, DONE ?
49  00032 000031         JMP     ALOP3     ;NO, WAIT
50  00033 060477 AOP3:   060477            ;(DIAS 0,0)=1, YES, READ INTO AC0
51  00034 107363         ADDCS   0,1,SNC   ;ADD 2 FRAMES SWAPPED, GOT SECOND ?
52  00035 000031         JMP     ALOP3     ;NO, GO BACK AFTER IT (CARRY = 0)
53  00036 125300         MOVS    1,1       ;YES, SWAP AC1 (FOR TAPE FORMAT)
54  00037 001400         JMP     0,3       ;RETURN WITH WORD = BYTE 1 + BYTE 2
55                                         ;OR WORD = BYTE SYNCHRONIZER.
56
57                    ;ALL LABELS CHANGED FROM ORIGINAL TO AXXXX TO
58                    ;ASEMBLE TOGETHER WITH REST OF PROGRAM.
```

```
!0063 .MAIN
01
02                                  ;THIS LOCATIONS IS USED FIRST BY
03                                  ;THE AUTOLOAD PROGRAM, SECOND BY
04                                  ;THE TEST PROGRAM.
05
06              ;       .LOC    0       ;LOC0 IS USED FOR POWER INTR (LOC 76).
07              ;LOC0:  0               ;LOC0 AND LOC1 IS USED FOR
08              ;LOC1:  0               ;TESTING INTERRUPT TOO.
09              ;LOC2:  0
10              ;LOC3:  0
11              ;LOC4:  0
12
13              ;       .LOC    17
14              ;LOC17: 0               ;ALL AIL + ADL LOC'S USED IN LOOP STA12
15              ;AIL20: 0               ;AUTO INCREMENT LOC
16              ;AIL21: 0
17              ;AIL22: 0
18              ;AIL23: 0
19              ;AIL24: 0
20              ;AIL25: 0
21              ;AIL26: 0
22              ;AIL27: 0
23              ;ADL30: 0               ;AUTO DECREMENT LOC
24              ;ADL31: 0
25              ;ADL32: 0
26              ;ADL33: 0
27              ;ADL34: 0
28              ;ADL35: 0
29              ;ADL36: 0
30              ;ADL37: 0
31                      ;ALL ABOVE LOCATIONS ARE USED BY THE TESTPROGRAM
32                      ;AS WORKING AREA. FOR ASM TECHNICS THEY ARE USED
33                      ;FOR AUTOLOAD PROGRAM, THEREFORE THE LABELS MUST
34                      ;BE DEFINED:
35      000000 LOC0=0
36      000001 LOC1=1
37      000002 LOC2=2
38      000003 LOC3=3
39      000004 LOC4=4
40
41      000017 LOC17=17
42      000020 AIL20=20
43      000021 AIL21=21
44      000022 AIL22=22
45      000023 AIL23=23
46      000024 AIL24=24
47      000025 AIL25=25
48      000026 AIL26=26
49      000027 AIL27=27
50      000030 ADL30=30
51      000031 ADL31=31
52      000032 ADL32=32
53      000033 ADL33=33
54      000034 ADL34=34
55      000035 ADL35=35
56      000036 ADL36=36
57      000037 ADL37=37
58
59      000400 LO400=400
60      000401 LO401=401
```

```
 0064 .MAIN
01
02                ;SELF, A PROGRAM SIMILAR TO AUTOLOAD PROM FOR PTR, BUT
03                ;READ TO MEMORY BY THE OPERATOR THROUGH FRONT PANEL SWITCHES.
04
05                ;FIRST: IN LOC 30 DEPOSIT 000064  (JMP 64).
06                ;       (ONLY USED IF AN OLD VERSION OF S-BIN OR H-BIN
07                ;       (IS LOADED. PROGRAMS ISSUED BEFORE JUNE 1978 ARE
08                ;       (WITHOUT READ ROUTINE IN PREAMBLE PROGRAM AND
09                ;       (USES GET ROUTINE IN AUTOLOAD INSTEAD, ASSUMED
10                ;       (PRESENT IN LOC 30, THEREFORE JSR 30. )))))
11                ;               OLD VERSIONS:   FIRST CHAR ON TAPE = 1
12                ;               THIS VERSION:   FIRST CHAR ON TAPE = 377
13                ;THEN DEPOSIT SELF PROGRAM.
14                ;START IN LOCATION 50, NOT 10050 AS IN LISTNING.
15
16
17          010050 .LOC     10050           ;ONLY FOR ASM, ACTUAL LOC = 50 .
18
19  10050 060112 BEGIN: NIOS    PTR         ;START READER
20  10051 126440        SUBO    1,1         ;CLEAR AC1, CLEAR CARRY
21  10052 004413 LOOP:  JSR     GET1        ;GET A BYTE
22  10053 101065        MOVC    0,0,SNR     ;IS IT ZERO ?
23  10054 000776        JMP     LOOP        ;YES, IGNORE AND GET NEXT
24  10055 030420        LDA     2,SAPRE     ;NO, IT WAS TAPE SYNCRONIZER, DROP IT
25                                          ;AND SET AC2 TO FIRST MEM LOC FOR PREAM
26  10056 004406 LOOP1: JSR     GET         ;GET A FULL WORD, FIRST = WORD COUNT
27  10057 045000        STA     1,0,2       ;STORE INTO MEMORY FROM COUNT
28  10060 151400        INC     2,2         ;INCREMENT ADDR TO NEXT
29  10061 010417        ISZ     COUNT       ;BUMP WORD COUNT, DONE ?
30  10062 000774        JMP     LOOP1       ;NO, REPEAT, STILL DATA
31  10063 000416        JMP     PREAM       ;YES, FINISHED, GIVE CONTROL TO
32                                          ;FIRST WORD IN PREAM PROGRAM
33  10064 126420 GET:   SUBZ    1,1         ;CLEAR AC1, SET CARRY
34  10065 063512 GET1:  SKPBZ   PTR         ;
35  10066 000777        JMP     .-1         ;WAIT NON-BUSY
36  10067 060412        DIA     0,PTR       ;READ A BYTE TO AC0
37  10070 060112        NIOS    PTR         ;START READER FOR NEXT BYTE
38  10071 107363        ADDCS   0,1,SNC     ;ADD 2 BYTES SWAPPED, GOT SECOND ?
39  10072 000773        JMP     GET1        ;NO, GO BACK AFTER IT
40  10073 125300        MOVS    1,1         ;YES, SWAP AC1
41  10074 001400        JMP     0,3         ;RETURN WITH FULL WORD
42  10075 000100 SAPRE: .+3-10000           ;START ADDR FOR LOADING PREAM
43  10076 000050 SADDR: 50                  ;SPARE, NOT USED ,(START ADDR FOR SELF)
44
45                ;AFTER DEPOSITING ABOVE PROGRAM, SET SWITCHES TO 000050 AND
46                ;LOAD THE PAPER TAPE READER WITH SUITABLE TAPE (S-BIN OR H-BIN).
47                ;PRESS RESET, START. NOW THE BINARY LOADER IN NORMAL OR
48                ;SELFSTART VERSION IS READ IN, THEN THE MAIN PROGRAM.
49
50
51                ;NOTE:  THIS PROGRAM IS NOT DESTROYED (LOC 50 - 75 INCL)
52                ;       BY AUTOLOAD OR LOADING WITH SELF OR BINARY
53                ;       LOADER, AND NOT DESTROYED BY RUNNING THE TEST !
```

```
00065 .MAIN
01
02        000040          .LOC    40
03
04                        ;THIS LOCATIONS ARE USED FOR RESTARTING THE PROGRAM
05                        ;IN DIFFERENT LOCATIONS, USED IF NO TECHNICAL
06                        ;CONTROL PANEL ETC.
07
08                        ;METHOD LIKE PARAGRAPH 5, 5 PAGES BEFORE THIS, BUT
09                        ;WITH OTHER SWITCH SETTINGS:
10
11                        ;AFTER HALT (NO RUN LIGHT) AFTER AUTOLOAD.
12                        ;PAR. 3.
13
14 00040 000233           BAUTO+1           ;CPU 708, SW = 100040 OR 000041
15 00041 002040           JMP     .,-1      ;NOVA 2, SW = 000041
16
17                        ;AFTER WRITING AUTOLOAD, BUT NO ROMS.
18                        ;PAR. 2.
19
20                        ;OR
21
22                        ;AT ANY TIME IF RESTART OF POWER MONITOR IS WANTED.
23                        ;PAR. 4.
24
25 00042 000251           NOROM             ;CPU 708, SW = 100042 OR 000043
26 00043 002042           JMP     .,-1      ;NOVA 2, SW = 000043
27
28                        ;AT ANY TIME IF RESTART OF AUTOLOAD TEST IS WANTED.
29                        ;LOAD PTR WITH BLOCK 3 (+4).  PAR. 2.
30
31 00044 000220           REBIN             ;CPU 708, SW = 100044 OR 000045
32 00045 002044           JMP     .,-1      ;NOVA 2, SW = 000045
33
34                        ;AT ANY TIME IF RESTART OF RESTART TEST IS WANTED.
35                        ;PAR. 5.
36
37 00046 000320           RESTA             ;CPU 708, SW = 100046 OR 000047
38 00047 002046           JMP     .,-1      ;NOVA 2, SW = 000047
39
40                        ;AT ANY TIME IF RESTART OF SECOND PART OF TEST IS
41                        ;WANTED (WITHOUT OPERATOR) = MANUAL RESTART IN LOC 500.
42
43                                          ;CPU 708, SW = 100077 OR 000101
44                                          ;NOVA 2, SW = 000101
45
46                        ;THIS LOCATIONS ARE USED FIRST BY THE
47                        ;PREAMBLE PROGRAM WHEN AUTOLOADING/LOADING
48                        ;TEST, SECOND BY THE TEST PROGRAM.
49
50        000076          .LOC    76
51
52 00076 002100 POWZE:    JMP     @POWRE    ;INSTRUCTION TO BE STORED IN CELL ZERO
53 00077 000323 IRESA:    SWISA             ;PROGRAM RESTART ADDR
54 00100 000307 POWRE:    POWON             ;POWER RESTART ADDR
55 00101 002077 RETAB:    JMP     @IRESA    ;NOVA 2 RESTART
```

```
10066 .MAIN
01
02                ;PREAMBLE PROGRAM READ TO MEMORY FROM PTR BY
03                ;                                          1, AUTOLOAD PTR
04                ;                                   OR     2, PRIM PROGRAM
05
06        010077 .LOC     10077             ;ONLY FOR ASM, FIRST LOC ACTUAL
07                                          ;USED IS 100, AS THE TAPE SYNC CHAR
08                                          ;READ FROM TAPE NOT IS STORED.
09
10 10077 000377 SYNCH:  000377              ;TAPE SYNC CHAR
11
12 10100 177743 COUNT:  PREAM-END-2         ;NEG WORD COUNT FOR PREAMBLE-1
13
14 10101 020421 PREAM:  LDA     0,C4K       ;MEMORY SIZING INCREMENT
15 10102 176221         ADCZR   3,3,SKP     ;FORM HIGHEST ADDR = 077777
16 10103 116400 LOOP2:  SUB     0,3         ;DECREMENT ADDR (SKIPPED FIRST TIME)
17 10104 055400         STA     3,0,3       ;STORE ADDR
18 10105 031400         LDA     2,0,3       ;GET IT BACK
19 10106 172414         SUB#    3,2,SZR     ;SAME ?
20 10107 000774         JMP     LOOP2       ;NO, NO MEMORY
21 10110 004414         JSR     READ        ;YES, READ FIRST DATA
22 10111 044412         STA     1,LENG      ;SAVE LENGTH OF BINARY LOADER
23 10112 133000         ADD     1,2         ;FORM FIRST ADDRESS-1
24 10113 151400 LOOP3:  INC     2,2         ;INCREMENT ADDR TO NEXT
25 10114 004410         JSR     READ        ;READ BINARY LOADER DATA
26 10115 045000         STA     1,0,2       ;STORE INTO MEMORY
27 10116 010405         ISZ     LENG        ;BUMP LENGTH COUNT
28 10117 000774         JMP     LOOP3       ;REPEAT IF STILL DATA
29
30 10120 000401         JMP     .+1         ;;;ONLY TO USE SAME LOC'S AS THE
31                                          ;NOT SELFSTARTING VERSION:
32
33                ;;10120 063077            ;;OLD LOC, CONTENT
34                ;;;     HALT              ;LOAD PTR, PRESS CONTINUE OR
35                                          ;START BINARY LOADER IN LAST
36                                          ;LOC: 0X7777 OR 1X7777, SWITCH 0
37                                          ;NO LONGER USED (PTR/TTI).
38
39 10121 001000         JMP     0,2         ;FINISHED, GIVE CONTROL TO LAST
40                                          ;USED MEM LOC, LAST LOC IN
41                                          ;BINARY LOADER (AND IN MEMORY).
42
43 10122 004000 C4K:    4000                ;MEMORY SIZING STEP
44 10123 000000 LENG:   0                   ;LENGTH COUNT
45
46 10124 126420 READ:   SUBZ    1,1         ;CLEAR AC1, SET CARRY
47 10125 063512 READ1:  SKPBZ   PTR         ;
48 10126 000777         JMP     .-1         ;WAIT NON-BUSY
49 10127 060412         DIA     0,PTR       ;READ A BYTE
50 10130 060112         NIOS    PTR         ;START READER FOR NEXT BYTE
51 10131 107363         ADDCS   0,1,SNC     ;ADD 2 BYTES SWAPPED, GOT SECOND ?
52 10132 000773         JMP     READ1       ;NO, GO BACK AFTER IT
53 10133 001400         JMP     0,3         ;YES, RETURN WITH FULL WORD
54
55 10134 000745 END:    JMP     PREAM       ;GETS CONTROL HERE IF AUTOLOADED.
56
57                ;NEXT LOCATION ONLY FOR ASM TO HAVE DATA ON PAPER TAPE:
58 10135 177635         BUILD-BEND-1        ;NEG WORD COUNT FOR BINARY LOADER
59                                          ;LOADED FROM TAPE TO LABEL LENG
60                                          ;IN PREAM PROGRAM
```

```
0067 .MAIN
01
02                ;BINARY LOADER TS CHANGED TO ONLY PTR, SEE ;;;
03                ;ERRORHALT XX7751 FOR OVERWRITE LOADER OR CHECKSUM ERROR.
04                ;READYHALT XX7676 IF LOADED PROG ISN'T SELFSTARTING.
05                ;ERRORBLOCK=IGNORE BLOCK
06                ;REPEAT BLOCK=MULTIPLE DATA BLOCK
07                ;COUNT=WORD COUNT IN BLOCK
08
09        062677 ALRST=IORST
10        060477 .DIAC RDSWI=READS 0
11
12        017635 .LOC 17635                 ;ONLY FOR ASM, MOVED TO END OF MEMORY.
13
14                ;SUBROUTINE TO BUILD A WORD IN AC2
15 17635 054425 BUILD: STA     3,BTMP1 ;SAVE RETURN
16 17636 004406        JSR     GTCHR   ;GET FIRST BYTE
17 17637 171300        MOVS    3,2     ;PUT INTO LH OF AC2
18 17640 004404        JSR     GTCHR   ;GET NEXT BYTE
19 17641 173300        ADDS    3,2     ;FORM WORD IN AC2
20 17642 143000        ADD     2,0     ;ADD INTO CHECKSUM
21 17643 002417        JMP     @BTMP1  ;AND RETURN
22
23                ;READ A BYTE INTO AC3
24                ;IF SWITCH0=0 USE TELETYPE ELSE USE PTR
25 17644 054417 GTCHR: STA     3,BTMP2 ;SAVE RETURN
26 17645 034417        LDA     3,BSAVE ;TEST WHICH DEVICE
27 17646 175103        MOVL    3,3,SNC
28 17647 000406        JMP     GTTTI   ;TTI
29 17650 063612        SKPDN   PTR     ;PTR
30 17651 000777        JMP     .-1
31 17652 074412        DIA     3,PTR   ;READ AND START
32 17653 060112        NIOS    PTR
33 17654 002407        JMP     @BTMP2  ;AND RETURN
34
35 17655 063610 GTTTI: SKPDN   TTI
36 17656 000777        JMP     .-1
37 17657 074410        DIA     3,TTI   ;READ AND START
38 17660 060110        NIOS    TTI
39 17661 002402        JMP     @BTMP2  ;AND RETURN
40 17662 000000 BTMP1: 0
41 17663 000000 BTMP2: 0
42 17664 000000 BSAVE: 0
43
44                ;TEST BLOCK TYPE
45 17665 125224 TEST:  MOVZR   1,1,SZR ;1=START BLOCK (,END XX)
46 17666 000411        JMP     IGNOR   ;NO, IGNORE BLOCK
47 17667 101004        MOV     0,0,SZR ;TEST THE CHECKSUM
48 17670 000460        JMP     CHKER   ;ERROR
49 17671 030505        LDA     2,ADDRS ;GET ADDR
50 17672 062677        ALRST           ;DO A RESET (IORST)
51 17673 151113        MOVL#   2,2,SNC ;TEST BIT 0
52 17674 001000        JMP     0,2     ;0=START PROGRAM
53 17675 063077        HALT            ;1=HALT
54 17676 000777        JMP     .-1     ;DON'T PROCEED
```

```
!0068 .MAIN
01
02                      ;IGNORE BLOCK
03 17677 004745 IGNOR:  JSR     GTCHR   ;READ UNTIL AN ALL
04 17700 020404         LDA     0,BC377 ;ONES BYTE IS SEEN
05 17701 116404         SUB     0,3,SZR ;IGNORING ERROR MESS
06 17702 000775         JMP     IGNOR
07 17703 000407         JMP     BLOCK   ;OK, GO INTO BLOCK MODE
08 17704 000377 BC377:  377
09
10                      ;START OF PROGRAM BINARY LOADER TS
11 17705 062677 BBEGIN: ALRST           ;RESET (IORST)
12                      ;;;     RDSWI   0       ;READ THE SWITCH REGISTER (READS 0)
13                      ;;17706 060477          ;;OLD LOC, CONTENT
14 17706 102620         SUBZR   0,0     ;;;ONLY PTR, AC0:=100000
15 17707 040755         STA     0,BSAVE ;AND SAVE IT FOR GTCHR
16 17710 060110         NIOS TTI        ;START BOTH READERS
17 17711 060112         NIOS PTR
18
19                      ;READ IN A BLOCK
20 17712 004732 BLOCK:  JSR     GTCHR   ;GET A BYTE
21 17713 165305         MOVS    3,1,SNR ;AND TEST FOR NUL
22 17714 000776         JMP     BLOCK   ;YES, KEEP READING
23 17715 004727         JSR     GTCHR   ;OK, GET NEXT BYTE
24 17716 167500         ADDS    3,1     ;AND FORM COUNT, AC1:=# OF WORDS
25 17717 121000         MOV     1,0     ;SET CHECKSUM, AC0:=CHECKSUM TILL NOW
26 17720 004715         JSR     BUILD   ;GET ADDRESS
27 17721 050455         STA     2,ADDRS
28 17722 004713         JSR     BUILD   ;ADD IN THE CHECKSUM FROM TAPE
29 17723 125113         MOVL#   1,1,SNC ;TEST BLOCK TYPE
30 17724 000741         JMP     TEST    ;NOT A DATABLOCK
31 17725 044427         STA     1,BCOUN ;STORE WORD COUNT
32
33                      ;READ IN THE DATA BLOCK
34 17726 030735 BDATA:  LDA     2,BTMP2 ;LAST STA IN BTMP2 WAS JSR RETURN
35 17727 034423         LDA     3,DIFF  ;ADDR 4 CELLS AFTER PROGRAM START:
36 17730 172400         SUB     3,2     ;AC2:=FIRST ADDR IN LOADER
37 17731 034445         LDA     3,ADDRS ;ADDR IN WHICH TO STORE
38 17732 136400         SUB     1,3     ;ADD NEG WC TO CHECK SPACE
39 17733 172023         ADCZ    3,2,SNC ;FOR WHOLE BLOCK
40 17734 000414         JMP     CHKER   ;NO, HALT THE LOADER
41 17735 030416         LDA     2,BC20  ;IF WC > 20 (OCTAL, NEG) IT IS A
42 17736 147033         ADDZ#   2,1,SNC ;A REPEAT BLOCK (CARRY=ZERO, BIT0=ONE)
43 17737 010415         ISZ     BCOUN   ;WHERE WC IS ONE LESS THAN COUNT
44 17740 147022         ADDZ    2,1,SZC ;IF REPEAT BLOCK SKIP NEXT TO READ DATA
45 17741 125113 STORE:  MOVL#   1,1,SNC ;SKIP READ IN NEW DATA IF REPEAT BLOCK
46 17742 004673         JSR     BUILD   ;READ DATA TO AC2
47 17743 052433         STA     2,@ADDRS ;STORE INTO MEMORY
48 17744 010432         ISZ     ADDRS   ;NEXT ADDR
49 17745 010407         ISZ     BCOUN   ;TEST COUNT
50 17746 000773         JMP     STORE   ;MORE DATA
51 17747 101004         MOV     0,0,SZR ;TEST CHECKSUM, AC0=VALUE
52 17750 063077 CHKER:  HALT            ;OVERWRITING OR ERROR IN CHECKSUM
53 17751 000741         JMP     BLOCK   ;OK,GET NEXT BLOCK
54
55 17752 000004 DIFF:   4
56 17753 000020 BC20:   20              ;REPEAT BLOCKS HAVE WC>20
57 17754 000000 BCOUN:  0               ;WORD COUNT
58 17755 000000         0               ;NOT USED
```

```
10069 .MAIN
01
02                ;BOOTSTRAP LOADER TS FOR PTR:
03                ;ENTER AT BSTRP
04
05 17756 126440 BBGET:  SUBO    1,1
06 17757 063612 BGET1:  SKPDN   12          ;10 FOR TTI
07 17760 000777         JMP     .-1
08 17761 060412         DIA     0,12        ;10 FOR TTI
09 17762 060112         NIOS    12          ;10 FOR TTI
10 17763 127100         ADDL    1,1
11 17764 127100         ADDL    1,1
12 17765 107003         ADD     0,1,SNC
13 17766 000771         JMP     BGET1
14 17767 001400         JMP     0,3
15 17770 060112 BSTRP:  NIOS    12          ;10 FOR TTI
16 17771 004765         JSR     BBGET
17 17772 044402         STA     1,.+2
18 17773 004763         JSR     BBGET
19 17774 000000         0
20 17775 000000         0                   ;FOR BOOTSTRAP
21 17776 000000 ADDRS:  0
22 17777 000706 BEND:   JMP     BBEGIN      ;START OF BINARY LOADER
```

```
10070 .MAIN
01
02                          ;CONSTANTS FOR TESTPROGRAM:
03
04          000135          .LOC    135     ;NOT REALLY USED BY PREAMBLE PROGRAM
05
06 00135 000001 K1:         1
07 00136 000002 K2:         2
08 00137 000004 K4:         4
09 00140 000010 K10:        10
10 00141 000020 K20:        20
11 00142 000040 K40:        40
12 00143 000100 K100:       100
13 00144 000200 K200:       200
14 00145 000400 K400:       400
15 00146 001000 K1000:      1000
16 00147 002000 K2000:      2000
17 00150 004000 K4000:      4000
18 00151 010000 K10K:       10000
19 00152 020000 K20K:       20000
20 00153 040000 K40K:       40000
21 00154 100000 K100K:      100000
22 00155 020400 KLDA,:      20400           ;= TO AN LDA    0,, OFF PAGE0
23 00156 000005 K5:         5
24 00157 000007 K7:         7
25 00160 000300 K300:       300
26 00161 100017 KD17:       #17
27 00162 177770 KM8:        -8.
28 00163 100021 KD21:       #21
29 00164 100037 KD37:       #37
30 00165 125251 KCBE:       125251          ;EVEN # BITS
31 00166 052525 KCBO:       052525          ;ODD # BITS
32 00167 000420 K420:       420
33 00170 001400 KJRET:      JMP     0,3     ;JSR    RETURNS TYPE JMP
34 00171 000000 KLOC0:      LOC0
35 00172 000074 K60:        60.
36 00173 000074 TESTK:      060.
37
38          000177          .LOC    177     ;TESTPROGRAM WORKING AREA
39
40 00177 000000 LO177:      0
41 00200 000000 LO200:      0
42 00201 000000 LO201:      0
43
44 00202 000215 K215:       215
45 00203 000212 K212:       212
46 00204 000323 K323:       323
47 00205 000011 KTTO:       TTO
48 00206 000320 K320:       320
49 00207 002300 JMP3K:      JMP     #300
50 00210 000001 PKR00:      1
51 00211 000001 PKR01:      1
52
53                          ;CONSTANTS FOR NEXT PAGE:
54
55 00212 002213 IN400:      JMP     .+1
56 00213 000500 IN401:      A1A
57 00214 000357 POK:        TOK
58 00215 000361 PLOCK:      TLOCK
59 00216 000365 PPOW:       TPOW
60 00217 000371 PREST:      TREST
```

```
 0071 .MAIN
01
02                          ;HERE AFTER LOADING BLOCK 2 (+1), MAIN TESTPROGRAM.
03
04 00220 020076 REBIN:  LDA     0,POWZE ;SET POWER RESTART
05 00221 040000         STA     0,LOC0
06 00222 024212         LDA     1,IN400 ;SET RESTART ADDR = 400
07 00223 044555         STA     1,LO400
08 00224 024213         LDA     1,IN401
09 00225 044554         STA     1,LO401
10 00226 030231         LDA     2,PAUTO ;WRITE AUTOLOAD
11 00227 004332         JSR     WRITE
12 00230 000230         JMP     .       ;WAIT
13 00231 000351 PAUTO:  TAUTO
14
15                          ;HERE AFTER AUTOLOADING BLOCK 4 (+3).
16
17                          ;DESCRIPTION OF THE AUTOLOAD TEST CALLED BY
18                          ;THE LAST BLOCK ON THE BINARY TAPE (.END BAUTO)
19                          ;RESTART: AUTOLOAD BLOCK 3 AND 4 FROM PTR.
20                          ;IF NO ROMS, PASS THIS TEST BY STARTING IN NOROM
21
22 00232 063077 BAUTO:  HALT            ;TO TEST CPU HALT, DATALED =063077
23                                      ;PRESS CONTINUE.
24
25                          ;NOW THE CONTENT OF LOC 0 TO 37 IS TESTED.
26
27 00233 020272         LDA     0,LAUTO ;LENGTH TO TEST
28 00234 040273         STA     0,CAUTO
29 00235 030274         LDA     2,SAUTO ;START ADDR TO TEST
30 00236 034275         LDA     3,DAUTO ;DATA EXP. ADDR
31 00237 021000 NAUTO:  LDA     0,0,2
32 00240 025400         LDA     1,0,3
33 00241 106414         SUB#    0,1,SZR
34 00242 063077         HALT            ;AC0=DATA FROM ROM TO MEM
35                                      ;AC1=EXPECTED DATA
36                                      ;AC2=ADDR FOR AC0 DATA
37                                      ;AC3=ADDR FOR AC1 DATA
38 00243 151400         INC     2,2
39 00244 175400         INC     3,3
40 00245 014273         DSZ     CAUTO   ;COUNT/TEST LENGTH COUNTER
41 00246 000237         JMP     NAUTO   ;NEXT
42 00247 030214         LDA     2,POK   ;WRITE OK
43 00250 004332         JSR     WRITE
44 00251 020270 NOROM:  LDA     0,LPOW  ;RESTORE LOC 76 - 101
45 00252 040273         STA     0,CAUTO
46 00253 030302         LDA     2,DPOW
47 00254 034271         LDA     3,APOW
48 00255 025000 NPOW:   LDA     1,0,2
49 00256 045400         STA     1,0,3
50 00257 151400         INC     2,2
51 00260 175400         INC     3,3
52 00261 014273         DSZ     CAUTO
53 00262 000255         JMP     NPOW    ;NEXT
54 00263 020076         LDA     0,POWZE ;SET POWER RESTART
55 00264 040000         STA     0,LOC0
56 00265 030215         LDA     2,PLOCK ;WRITE LOCK
57 00266 004332         JSR     WRITE
58 00267 000267         JMP     .       ;WAIT
59 00270 000004 LPOW:   4               ;LENGT OF AREA
60 00271 000076 APOW:   POWZE           ;LOC 76
```

```
 0072 .MAIN
01
02 00272 000040 LAUTO:  40
03 00273 000000 CAUTO:  0
04 00274 000000 SAUTO:  0
05 00275 000440 DAUTO:  KAUTO
06
07       000277         .LOC    277      ;TESTPROGRAM WORKING AREA
08
09 00277 000000 LO277:  0
10 00300 000000 LO300:  0
11 00301 000000 LO301:  0
12
13                      ;TABLE FOR INSTR TO LOC 76 - 101
14 00302 000303 DPOW:   .+1
15 00303 002100         JMP     @POWRE   ;DATA TO LOC 76
16 00304 000323         SWISA
17 00305 000307         POWON
18 00306 002077         JMP     @IRESA
19
20                      ;HERE AFTER POWER ON
21
22 00307 062677 POWON:  IORST
23 00310 024376         LDA     1,RPOW   ;# OF REPEATINGS (NEG)
24 00311 102440         SUBO    0,0      ;AC0:=0, CARRY :=0
25 00312 101403         INC     0,0,SNC  ;WAIT SOME TIME
26 00313 000312         JMP     .-1      ;ABOUT 100 MSEC
27 00314 125404         INC     1,1,SZR  ;COUNT # OF REPEATINGS
28 00315 000311         JMP     .-4      ;REPEAT
29 00316 030216         LDA     2,PPOW   ;WRITE POWER
30 00317 004332         JSR     WRITE
31 00320 030217 RESTA:  LDA     2,PREST  ;WRITE RESTART
32 00321 004332         JSR     WRITE
33 00322 000322         JMP     .        ;WAIT
34
35                      ;HERE AFTER RESTART
36
37 00323 030214 SWISA:  LDA     2,POK    ;WRITE OK
38 00324 004332         JSR     WRITE
39 00325 063611         SKPDN   TTO
40 00326 000325         JMP     .-1      ;WAIT TTO
41 00327 062677         IORST
42 00330 002331         JMP     @.+1     ;START TEST
43 00331 000500         A1A              ;WITHOUT OPERATOR INVOLMENT.
44
45                      ;TEXT WRITING ROUTINE, INPUT AC2 = ADDR OF TEXT
46 00332 024350 WRITE:  LDA     1,CHMAS  ;AN 8 BIT MASK
47 00333 021000 WRINX:  LDA     0,0,2    ;AC0:=TEXT WORD
48 00334 125112         MOVL#   1,1,SZC
49 00335 123701         ANDS    1,0,SKP
50 00336 123401         AND     1,0,SKP  ;AC0:=DATA CHAR
51 00337 151400         INC     2,2      ;COUNT TO NEXT TEXT WORD
52 00340 124000         COM     1,1      ;FLIP MASK
53 00341 101015         MOV#    0,0,SNR  ;TEST: LAST CHAR ?
54 00342 001400         JMP     0,3      ;YES, RETURN
55 00343 063511         SKPBZ   TTO      ;NO, WRITE
56 00344 000343         JMP     .-1
57 00345 061011         DOA     0,TTO
58 00346 060111         NIOS    TTO
59 00347 000333         JMP     WRINX    ;NEXT CHAR
60 00350 000377 CHMAS:  377
```

```
 0073 .MAIN
01
02 00351 005215 TAUTO:  .TXTE |<15><12>AUTOLOAD|
03       052501
04       147724
05       147714
06       042101
07       000000
08 00357 147640 TOK:    .TXTE | OK|
09       000113
10 00361 005215 TLOCK:  .TXTE |<15><12>LOCK|
11       147714
12       045703
13       000000
14 00365 050240 TPOW:   .TXTE | POWER|
15       153717
16       151305
17       000000
18 00371 005215 TREST:  .TXTE |<15><12>RESTART|
19       142722
20       152123
21       151101
22       000324
23
24 00376 177761 RPOW:   -15.            ;TIME CONSTANT FOR POWER UP
25
26
27
28               ;000400 .LOC    400    ;GENERATING SYSTEM USES LOC 400 TO 416.
29                                      ;WHEN LOADING PROGRAM IT WILL SET
30                                      ;THIS 2 LOC'S ITSELF.
31
32               ;002401 JMP    .,+1    ;FOOLS RESTART ADDR
33               ;000500 A1A
34
35       000420          .LOC    420
36
37 00420 000000 L0420:  0               ;USED IN LOOP AEQB7
38
```

```
10074 .MAIN
31
32          000440              .LOC    440
33
34                              ;DATA IN LOC 0 - 37 AFTER AN AUTOLOAD.
35                              ;SEE AUTOLOAD PROGRAM STARTING IN LABEL
36                              ;ABEG (LOC0) FOR FUTHER COMMENT.
37 00440 060477 KAUTO:  READS   0           ;LOC 0
38 00441 105120         MOVZL   0,1
39 00442 124240         COMCR   1,1
10
11 00443 010011         ISZ     11          ;LOC 3
12 00444 010031         ISZ     31
13 00445 010033         ISZ     33
14 00446 010014         ISZ     14
15 00447 125404         INC     1,1,SZR
16 00450 000003         JMP     3
17
18 00451 060112         NIOS    PTR         ;LOC 11
19
20 00452 030017         LDA     2,17
21 00453 050377         STA     2,377
22 00454 063412         SKPBN   PTR         ;LOC 14
23
24 00455 000011         JMP     11
25
26 00456 101102         MOVL    0,0,SZC
27 00457 000377         JMP     377         ;LOC 17
28
29 00460 004031         JSR     31          ;LOC 20
30 00461 101065         MOVC    0,0,SNR
31 00462 000020         JMP     20
32
33 00463 004030         JSR     30          ;LOC 23
34 00464 046027         STA     1,@27
35
36 00465 010100         ISZ     100
37 00466 000023         JMP     23
38 00467 000[illegible]134  JMP     [illegible]134  ;LOC 27
39
40 00470 126420         SUBZ    1,1         ;LOC 30
41
42 00471 063612         SKPDN   PTR         ;LOC 31
43 00472 000031         JMP     31
44 00473 060512         DIAS    0,PTR       ;LOC 33
45 00474 107363         ADDCS   0,1,SNC
46 00475 000031         JMP     31
47 00476 125300         MOVS    1,1
48 00477 001400         JMP     0,3         ;LOC 37
49
50
51                  ;TAPE 3
52
53                  .EOT
```

```
 0075 .MAIN
01
02                ;TAPE 4
03
04                        ;START OF TEST PROGRAM
05
06        000500          .LOC 500
07
08
09                ;DEFINE SKIP TEST MACRO FOR FIRST TEST SERIES
10                ;THIS SERIES WILL VERIFY THAT THAT EACH ALC
11                ;INSTRUCTION WILL NOT SKIP/THEN SKIP UNCONDITIONALLY
12
13                        .MACRO STES1
14                ;ERR HALT INDICATES EXTRANEOUS SKIP
15                A11:
16                        I2      0,0     ;I2 SHD NOT CAUSE SKIP IR13,14,15=000
17                        I2      0,0,SKP ;I2 SKIP ALWAYS IR13,14,15=001
18                        HALT
19                %
20                        .MACRO STES2
21
22                ;TEST OF I2 INSTRUCTION WITH ALL MODIFICATIONS
23                ;FOR NOT SKIP/THEN SKIP UNCONDITIONNALLY.
24
25
26
27                        STES1   I1A     I2
28
29                        STES1   I1B     I2Z
30
31                        STES1   I1C     I20
32
33                        STES1   I1D     I2C
34
35                        STES1   I1E     I2L
36
37                        STES1   I1F     I2R
38
39                        STES1   I1G     I2S
40
41
42
43
44                %
```

```
00076 .MAIN
01
02                      STES2   1       COM
03
04              ;TEST OF COM INSTRUCTION WITH ALL MODIFICATIONS
05              ;FOR NOT SKIP/THEN SKIP UNCONDITIONNALLY.
06
07
08
09                      STES1   1A      COM
10                      ;ERR HALT INDICATES EXTRANEOUS SKIP
11                  A1A:
12 00500 100000         COM     0,0     ;COM SHD NOT CAUSE SKIP IR13,14,15=000
13 00501 100001         COM     0,0,SKP ;COM SKIP ALWAYS IR13,14,15=001
14 00502 063077         HALT
15
16                      STES1   1B      COMZ
17                      ;ERR HALT INDICATES EXTRANEOUS SKIP
18                  A1B:
19 00503 100020         COMZ    0,0     ;COMZ SHD NOT CAUSE SKIP IR13,14,15=000
20 00504 100021         COMZ    0,0,SKP ;COMZ SKIP ALWAYS IR13,14,15=001
21 00505 063077         HALT
22
23                      STES1   1C      COMO
24                      ;ERR HALT INDICATES EXTRANEOUS SKIP
25                  A1C:
26 00506 100040         COMO    0,0     ;COMO SHD NOT CAUSE SKIP IR13,14,15=000
27 00507 100041         COMO    0,0,SKP ;COMO SKIP ALWAYS IR13,14,15=001
28 00510 063077         HALT
29
30                      STES1   1D      COMC
31                      ;ERR HALT INDICATES EXTRANEOUS SKIP
32                  A1D:
33 00511 100060         COMC    0,0     ;COMC SHD NOT CAUSE SKIP IR13,14,15=000
34 00512 100061         COMC    0,0,SKP ;COMC SKIP ALWAYS IR13,14,15=001
35 00513 063077         HALT
36
37                      STES1   1E      COML
38                      ;ERR HALT INDICATES EXTRANEOUS SKIP
39                  A1E:
40 00514 100100         COML    0,0     ;COML SHD NOT CAUSE SKIP IR13,14,15=000
41 00515 100101         COML    0,0,SKP ;COML SKIP ALWAYS IR13,14,15=001
42 00516 063077         HALT
43
44                      STES1   1F      COMR
45                      ;ERR HALT INDICATES EXTRANEOUS SKIP
46                  A1F:
47 00517 100200         COMR    0,0     ;COMR SHD NOT CAUSE SKIP IR13,14,15=000
48 00520 100201         COMR    0,0,SKP ;COMR SKIP ALWAYS IR13,14,15=001
49 00521 063077         HALT
50
51                      STES1   1G      COMS
52                      ;ERR HALT INDICATES EXTRANEOUS SKIP
53                  A1G:
54 00522 100300         COMS    0,0     ;COMS SHD NOT CAUSE SKIP IR13,14,15=000
55 00523 100301         COMS    0,0,SKP ;COMS SKIP ALWAYS IR13,14,15=001
56 00524 063077         HALT
57
58
59
60
```

```
0077 .MAIN
01
02                      STES2   2       NEG
03
04              ;TEST OF NEG INSTRUCTION WITH ALL MODIFICATIONS
05              ;FOR NOT SKIP/THEN SKIP UNCONDITIONNALLY.
06
07
08
09                      STES1   2A      NEG
10                      ;ERR HALT INDICATES EXTRANEOUS SKIP
11                  A2A:
12 00525 100400         NEG     0,0     ;NEG SHD NOT CAUSE SKIP IR13,14,15=000
13 00526 100401         NEG     0,0,SKP ;NEG SKIP ALWAYS IR13,14,15=001
14 00527 063077         HALT
15
16                      STES1   2B      NEGZ
17                      ;ERR HALT INDICATES EXTRANEOUS SKIP
18                  A2B:
19 00530 100420         NEGZ    0,0     ;NEGZ SHD NOT CAUSE SKIP IR13,14,15=000
20 00531 100421         NEGZ    0,0,SKP ;NEGZ SKIP ALWAYS IR13,14,15=001
21 00532 063077         HALT
22
23                      STES1   2C      NEGO
24                      ;ERR HALT INDICATES EXTRANEOUS SKIP
25                  A2C:
26 00533 100440         NEGO    0,0     ;NEGO SHD NOT CAUSE SKIP IR13,14,15=000
27 00534 100441         NEGO    0,0,SKP ;NEGO SKIP ALWAYS IR13,14,15=001
28 00535 063077         HALT
29
30                      STES1   2D      NEGC
31                      ;ERR HALT INDICATES EXTRANEOUS SKIP
32                  A2D:
33 00536 100460         NEGC    0,0     ;NEGC SHD NOT CAUSE SKIP IR13,14,15=000
34 00537 100461         NEGC    0,0,SKP ;NEGC SKIP ALWAYS IR13,14,15=001
35 00540 063077         HALT
36
37                      STES1   2E      NEGL
38                      ;ERR HALT INDICATES EXTRANEOUS SKIP
39                  A2E:
40 00541 100500         NEGL    0,0     ;NEGL SHD NOT CAUSE SKIP IR13,14,15=000
41 00542 100501         NEGL    0,0,SKP ;NEGL SKIP ALWAYS IR13,14,15=001
42 00543 063077         HALT
43
44                      STES1   2F      NEGR
45                      ;ERR HALT INDICATES EXTRANEOUS SKIP
46                  A2F:
47 00544 100600         NEGR    0,0     ;NEGR SHD NOT CAUSE SKIP IR13,14,15=000
48 00545 100601         NEGR    0,0,SKP ;NEGR SKIP ALWAYS IR13,14,15=001
49 00546 063077         HALT
50
51                      STES1   2G      NEGS
52                      ;ERR HALT INDICATES EXTRANEOUS SKIP
53                  A2G:
54 00547 100700         NEGS    0,0     ;NEGS SHD NOT CAUSE SKIP IR13,14,15=000
55 00550 100701         NEGS    0,0,SKP ;NEGS SKIP ALWAYS IR13,14,15=001
56 00551 063077         HALT
57
58
59
60
```

```
 0078 .MAIN
01
02                      STES2   3       MOV
03
04              ;TEST OF MOV INSTRUCTION WITH ALL MODIFICATIONS
05              ;FOR NOT SKIP/THEN SKIP UNCONDITIONNALLY.
06
07
08
09                      STES1   3A      MOV
10                      ;ERR HALT INDICATES EXTRANEOUS SKIP
11                  A3A:
12 00552 101000         MOV     0,0     ;MOV SHD NOT CAUSE SKIP IR13,14,15=000
13 00553 101001         MOV     0,0,SKP ;MOV SKIP ALWAYS IR13,14,15=001
14 00554 063077         HALT
15
16                      STES1   3B      MOVZ
17                      ;ERR HALT INDICATES EXTRANEOUS SKIP
18                  A3B:
19 00555 101020         MOVZ    0,0     ;MOVZ SHD NOT CAUSE SKIP IR13,14,15=000
20 00556 101021         MOVZ    0,0,SKP ;MOVZ SKIP ALWAYS IR13,14,15=001
21 00557 063077         HALT
22
23                      STES1   3C      MOVO
24                      ;ERR HALT INDICATES EXTRANEOUS SKIP
25                  A3C:
26 00560 101040         MOVO    0,0     ;MOVO SHD NOT CAUSE SKIP IR13,14,15=000
27 00561 101041         MOVO    0,0,SKP ;MOVO SKIP ALWAYS IR13,14,15=001
28 00562 063077         HALT
29
30                      STES1   3D      MOVC
31                      ;ERR HALT INDICATES EXTRANEOUS SKIP
32                  A3D:
33 00563 101060         MOVC    0,0     ;MOVC SHD NOT CAUSE SKIP IR13,14,15=000
34 00564 101061         MOVC    0,0,SKP ;MOVC SKIP ALWAYS IR13,14,15=001
35 00565 063077         HALT
36
37                      STES1   3E      MOVL
38                      ;ERR HALT INDICATES EXTRANEOUS SKIP
39                  A3E:
40 00566 101100         MOVL    0,0     ;MOVL SHD NOT CAUSE SKIP IR13,14,15=000
41 00567 101101         MOVL    0,0,SKP ;MOVL SKIP ALWAYS IR13,14,15=001
42 00570 063077         HALT
43
44                      STES1   3F      MOVR
45                      ;ERR HALT INDICATES EXTRANEOUS SKIP
46                  A3F:
47 00571 101200         MOVR    0,0     ;MOVR SHD NOT CAUSE SKIP IR13,14,15=000
48 00572 101201         MOVR    0,0,SKP ;MOVR SKIP ALWAYS IR13,14,15=001
49 00573 063077         HALT
50
51                      STES1   3G      MOVS
52                      ;ERR HALT INDICATES EXTRANEOUS SKIP
53                  A3G:
54 00574 101300         MOVS    0,0     ;MOVS SHD NOT CAUSE SKIP IR13,14,15=000
55 00575 101301         MOVS    0,0,SKP ;MOVS SKIP ALWAYS IR13,14,15=001
56 00576 063077         HALT
57
58
59
60
```

```
 0079 .MAIN
01
02                      STES2   4       INC
03
04              ;TEST OF INC INSTRUCTION WITH ALL MODIFICATIONS
05              ;FOR NOT SKIP/THEN SKIP UNCONDITIONNALLY.
06
07
08
09                      STES1   4A      INC
10                      ;ERR HALT INDICATES EXTRANEOUS SKIP
11                  A4A:
12 00577 101400         INC     0,0     ;INC SHD NOT CAUSE SKIP IR13,14,15=000
13 00600 101401         INC     0,0,SKP ;INC SKIP ALWAYS IR13,14,15=001
14 00601 063077         HALT
15
16                      STES1   4B      INCZ
17                      ;ERR HALT INDICATES EXTRANEOUS SKIP
18                  A4B:
19 00602 101420         INCZ    0,0     ;INCZ SHD NOT CAUSE SKIP IR13,14,15=000
20 00603 101421         INCZ    0,0,SKP ;INCZ SKIP ALWAYS IR13,14,15=001
21 00604 063077         HALT
22
23                      STES1   4C      INCO
24                      ;ERR HALT INDICATES EXTRANEOUS SKIP
25                  A4C:
26 00605 101440         INCO    0,0     ;INCO SHD NOT CAUSE SKIP IR13,14,15=000
27 00606 101441         INCO    0,0,SKP ;INCO SKIP ALWAYS IR13,14,15=001
28 00607 063077         HALT
29
30                      STES1   4D      INCC
31                      ;ERR HALT INDICATES EXTRANEOUS SKIP
32                  A4D:
33 00610 101460         INCC    0,0     ;INCC SHD NOT CAUSE SKIP IR13,14,15=000
34 00611 101461         INCC    0,0,SKP ;INCC SKIP ALWAYS IR13,14,15=001
35 00612 063077         HALT
36
37                      STES1   4E      INCL
38                      ;ERR HALT INDICATES EXTRANEOUS SKIP
39                  A4E:
40 00613 101500         INCL    0,0     ;INCL SHD NOT CAUSE SKIP IR13,14,15=000
41 00614 101501         INCL    0,0,SKP ;INCL SKIP ALWAYS IR13,14,15=001
42 00615 063077         HALT
43
44                      STES1   4F      INCR
45                      ;ERR HALT INDICATES EXTRANEOUS SKIP
46                  A4F:
47 00616 101600         INCR    0,0     ;INCR SHD NOT CAUSE SKIP IR13,14,15=000
48 00617 101601         INCR    0,0,SKP ;INCR SKIP ALWAYS IR13,14,15=001
49 00620 063077         HALT
50
51                      STES1   4G      INCS
52                      ;ERR HALT INDICATES EXTRANEOUS SKIP
53                  A4G:
54 00621 101700         INCS    0,0     ;INCS SHD NOT CAUSE SKIP IR13,14,15=000
55 00622 101701         INCS    0,0,SKP ;INCS SKIP ALWAYS IR13,14,15=001
56 00623 063077         HALT
57
58
59
60
```

```
 0080 .MAIN
01
02                      STES2   5       ADC
03
04              ;TEST OF ADC INSTRUCTION WITH ALL MODIFICATIONS
05              ;FOR NOT SKIP/THEN SKIP UNCONDITIONNALLY.
06
07
08
09                      STES1   5A      ADC
10                      ;ERR HALT INDICATES EXTRANEOUS SKIP
11                  A5A:
12 00624 102000         ADC     0,0     ;ADC SHD NOT CAUSE SKIP IR13,14,15=000
13 00625 102001         ADC     0,0,SKP ;ADC SKIP ALWAYS IR13,14,15=001
14 00626 063077         HALT
15
16                      STES1   5B      ADCZ
17                      ;ERR HALT INDICATES EXTRANEOUS SKIP
18                  A5B:
19 00627 102020         ADCZ    0,0     ;ADCZ SHD NOT CAUSE SKIP IR13,14,15=000
20 00630 102021         ADCZ    0,0,SKP ;ADCZ SKIP ALWAYS IR13,14,15=001
21 00631 063077         HALT
22
23                      STES1   5C      ADCO
24                      ;ERR HALT INDICATES EXTRANEOUS SKIP
25                  A5C:
26 00632 102040         ADCO    0,0     ;ADCO SHD NOT CAUSE SKIP IR13,14,15=000
27 00633 102041         ADCO    0,0,SKP ;ADCO SKIP ALWAYS IR13,14,15=001
28 00634 063077         HALT
29
30                      STES1   5D      ADCC
31                      ;ERR HALT INDICATES EXTRANEOUS SKIP
32                  A5D:
33 00635 102060         ADCC    0,0     ;ADCC SHD NOT CAUSE SKIP IR13,14,15=000
34 00636 102061         ADCC    0,0,SKP ;ADCC SKIP ALWAYS IR13,14,15=001
35 00637 063077         HALT
36
37                      STES1   5E      ADCL
38                      ;ERR HALT INDICATES EXTRANEOUS SKIP
39                  A5E:
40 00640 102100         ADCL    0,0     ;ADCL SHD NOT CAUSE SKIP IR13,14,15=000
41 00641 102101         ADCL    0,0,SKP ;ADCL SKIP ALWAYS IR13,14,15=001
42 00642 063077         HALT
43
44                      STES1   5F      ADCR
45                      ;ERR HALT INDICATES EXTRANEOUS SKIP
46                  A5F:
47 00643 102200         ADCR    0,0     ;ADCR SHD NOT CAUSE SKIP IR13,14,15=000
48 00644 102201         ADCR    0,0,SKP ;ADCR SKIP ALWAYS IR13,14,15=001
49 00645 063077         HALT
50
51                      STES1   5G      ADCS
52                      ;ERR HALT INDICATES EXTRANEOUS SKIP
53                  A5G:
54 00646 102300         ADCS    0,0     ;ADCS SHD NOT CAUSE SKIP IR13,14,15=000
55 00647 102301         ADCS    0,0,SKP ;ADCS SKIP ALWAYS IR13,14,15=001
56 00650 063077         HALT
57
58
59
60
```

```
0001 .MAIN
01
02                      STES2   6       SUB
03
04              ;TEST OF SUB INSTRUCTION WITH ALL MODIFICATIONS
05              ;FOR NOT SKIP/THEN SKIP UNCONDITIONNALLY.
06
07
08
09                      STES1   6A      SUB
10                      ;ERR HALT INDICATES EXTRANEOUS SKIP
11                  A6A:
12 00651 102400         SUB     0,0     ;SUB SHD NOT CAUSE SKIP IR13,14,15=000
13 00652 102401         SUB     0,0,SKP ;SUB SKIP ALWAYS IR13,14,15=001
14 00653 063077         HALT
15
16                      STES1   6B      SUBZ
17                      ;ERR HALT INDICATES EXTRANEOUS SKIP
18                  A6B:
19 00654 102420         SUBZ    0,0     ;SUBZ SHD NOT CAUSE SKIP IR13,14,15=000
20 00655 102421         SUBZ    0,0,SKP ;SUBZ SKIP ALWAYS IR13,14,15=001
21 00656 063077         HALT
22
23                      STES1   6C      SUBO
24                      ;ERR HALT INDICATES EXTRANEOUS SKIP
25                  A6C:
26 00657 102440         SUBO    0,0     ;SUBO SHD NOT CAUSE SKIP IR13,14,15=000
27 00660 102441         SUBO    0,0,SKP ;SUBO SKIP ALWAYS IR13,14,15=001
28 00661 063077         HALT
29
30                      STES1   6D      SUBC
31                      ;ERR HALT INDICATES EXTRANEOUS SKIP
32                  A6D:
33 00662 102460         SUBC    0,0     ;SUBC SHD NOT CAUSE SKIP IR13,14,15=000
34 00663 102461         SUBC    0,0,SKP ;SUBC SKIP ALWAYS IR13,14,15=001
35 00664 063077         HALT
36
37                      STES1   6E      SUBL
38                      ;ERR HALT INDICATES EXTRANEOUS SKIP
39                  A6E:
40 00665 102500         SUBL    0,0     ;SUBL SHD NOT CAUSE SKIP IR13,14,15=000
41 00666 102501         SUBL    0,0,SKP ;SUBL SKIP ALWAYS IR13,14,15=001
42 00667 063077         HALT
43
44                      STES1   6F      SUBR
45                      ;ERR HALT INDICATES EXTRANEOUS SKIP
46                  A6F:
47 00670 102600         SUBR    0,0     ;SUBR SHD NOT CAUSE SKIP IR13,14,15=000
48 00671 102601         SUBR    0,0,SKP ;SUBR SKIP ALWAYS IR13,14,15=001
49 00672 063077         HALT
50
51                      STES1   6G      SUBS
52                      ;ERR HALT INDICATES EXTRANEOUS SKIP
53                  A6G:
54 00673 102700         SUBS    0,0     ;SUBS SHD NOT CAUSE SKIP IR13,14,15=000
55 00674 102701         SUBS    0,0,SKP ;SUBS SKIP ALWAYS IR13,14,15=001
56 00675 063077         HALT
57
58
59
60
```

```
0082 .MAIN
01
02                      STES2   7       ADD
03
04              ;TEST OF ADD INSTRUCTION WITH ALL MODIFICATIONS
05              ;FOR NOT SKIP/THEN SKIP UNCONDITIONNALLY.
06
07
08
09                      STES1   7A      ADD
10                      ;ERR HALT INDICATES EXTRANEOUS SKIP
11                  A7A:
12 00676 103000         ADD     0,0     ;ADD SHD NOT CAUSE SKIP IR13,14,15=000
13 00677 103001         ADD     0,0,SKP ;ADD SKIP ALWAYS IR13,14,15=001
14 00700 063077         HALT
15
16                      STES1   7B      ADDZ
17                      ;ERR HALT INDICATES EXTRANEOUS SKIP
18                  A7B:
19 00701 103020         ADDZ    0,0     ;ADDZ SHD NOT CAUSE SKIP IR13,14,15=000
20 00702 103021         ADDZ    0,0,SKP ;ADDZ SKIP ALWAYS IR13,14,15=001
21 00703 063077         HALT
22
23                      STES1   7C      ADDO
24                      ;ERR HALT INDICATES EXTRANEOUS SKIP
25                  A7C:
26 00704 103040         ADDO    0,0     ;ADDO SHD NOT CAUSE SKIP IR13,14,15=000
27 00705 103041         ADDO    0,0,SKP ;ADDO SKIP ALWAYS IR13,14,15=001
28 00706 063077         HALT
29
30                      STES1   7D      ADDC
31                      ;ERR HALT INDICATES EXTRANEOUS SKIP
32                  A7D:
33 00707 103060         ADDC    0,0     ;ADDC SHD NOT CAUSE SKIP IR13,14,15=000
34 00710 103061         ADDC    0,0,SKP ;ADDC SKIP ALWAYS IR13,14,15=001
35 00711 063077         HALT
36
37                      STES1   7E      ADDL
38                      ;ERR HALT INDICATES EXTRANEOUS SKIP
39                  A7E:
40 00712 103100         ADDL    0,0     ;ADDL SHD NOT CAUSE SKIP IR13,14,15=000
41 00713 103101         ADDL    0,0,SKP ;ADDL SKIP ALWAYS IR13,14,15=001
42 00714 063077         HALT
43
44                      STES1   7F      ADDR
45                      ;ERR HALT INDICATES EXTRANEOUS SKIP
46                  A7F:
47 00715 103200         ADDR    0,0     ;ADDR SHD NOT CAUSE SKIP IR13,14,15=000
48 00716 103201         ADDR    0,0,SKP ;ADDR SKIP ALWAYS IR13,14,15=001
49 00717 063077         HALT
50
51                      STES1   7G      ADDS
52                      ;ERR HALT INDICATES EXTRANEOUS SKIP
53                  A7G:
54 00720 103300         ADDS    0,0     ;ADDS SHD NOT CAUSE SKIP IR13,14,15=000
55 00721 103301         ADDS    0,0,SKP ;ADDS SKIP ALWAYS IR13,14,15=001
56 00722 063077         HALT
57
58
59
60
```

```
0003 ,MAIN
01
02                      STES2   8       AND
03
04              ;TEST OF AND INSTRUCTION WITH ALL MODIFICATIONS
05              ;FOR NOT SKIP/THEN SKIP UNCONDITIONNALLY,
06
07
08
09                      STES1   8A      AND
10                      ;ERR HALT INDICATES EXTRANEOUS SKIP
11                  A8A:
12 00723 103400         AND     0,0     ;AND SHD NOT CAUSE SKIP IR13,14,15=000
13 00724 103401         AND     0,0,SKP ;AND SKIP ALWAYS IR13,14,15=001
14 00725 063077         HALT
15
16                      STES1   8B      ANDZ
17                      ;ERR HALT INDICATES EXTRANEOUS SKIP
18                  A8B:
19 00726 103420         ANDZ    0,0     ;ANDZ SHD NOT CAUSE SKIP IR13,14,15=000
20 00727 103421         ANDZ    0,0,SKP ;ANDZ SKIP ALWAYS IR13,14,15=001
21 00730 063077         HALT
22
23                      STES1   8C      ANDO
24                      ;ERR HALT INDICATES EXTRANEOUS SKIP
25                  A8C:
26 00731 103440         ANDO    0,0     ;ANDO SHD NOT CAUSE SKIP IR13,14,15=000
27 00732 103441         ANDO    0,0,SKP ;ANDO SKIP ALWAYS IR13,14,15=001
28 00733 063077         HALT
29
30                      STES1   8D      ANDC
31                      ;ERR HALT INDICATES EXTRANEOUS SKIP
32                  A8D:
33 00734 103460         ANDC    0,0     ;ANDC SHD NOT CAUSE SKIP IR13,14,15=000
34 00735 103461         ANDC    0,0,SKP ;ANDC SKIP ALWAYS IR13,14,15=001
35 00736 063077         HALT
36
37                      STES1   8E      ANDL
38                      ;ERR HALT INDICATES EXTRANEOUS SKIP
39                  A8E:
40 00737 103500         ANDL    0,0     ;ANDL SHD NOT CAUSE SKIP IR13,14,15=000
41 00740 103501         ANDL    0,0,SKP ;ANDL SKIP ALWAYS IR13,14,15=001
42 00741 063077         HALT
43
44                      STES1   8F      ANDR
45                      ;ERR HALT INDICATES EXTRANEOUS SKIP
46                  A8F:
47 00742 103600         ANDR    0,0     ;ANDR SHD NOT CAUSE SKIP IR13,14,15=000
48 00743 103601         ANDR    0,0,SKP ;ANDR SKIP ALWAYS IR13,14,15=001
49 00744 063077         HALT
50
51                      STES1   8G      ANDS
52                      ;ERR HALT INDICATES EXTRANEOUS SKIP
53                  A8G:
54 00745 103700         ANDS    0,0     ;ANDS SHD NOT CAUSE SKIP IR13,14,15=000
55 00746 103701         ANDS    0,0,SKP ;ANDS SKIP ALWAYS IR13,14,15=001
56 00747 063077         HALT
57
58
59
60
```

```
 0084 .MAIN
01
02                    ;TEST CARRY (CRY FLOP) AND SKIP LOGIC
03 00750 102022 A9A:  ADCZ    0,0,SZC ;ZC,IR14,NOT IR15
04 00751 063077       HALT            ;ZERO INPUT TO CARRY FAILED
05 00752 102023       ADCZ    0,0,SNC ;ANC NOT SEE CALC<IR15
06 00753 102002       ADC     0,0,SZC ;ALSO TEST ZERON HOLD AF CRY
07 00754 063077       HALT            ;IF CRY=1 SEE NOT IR12 OR
08
09                    ;ABOVE FAILURE IF CRY=1 MIGHT BE IN "NOT SCI" NOT IR10
10 00755 102026 A9B:  ADCZ    0,0,SEZ ;CARRY=0 ZC,IR14,NOT IR15
11 00756 063077       HALT            ;INVOLVES SAME GATES AS SZC (?)
12 00757 102043       ADCO    0,0,SNC ;TEST FOR TRUE CALC=IR15
13 00760 063077       HALT            ;1' INPUT TO CRY CALC WAS NOT 1
14 00761 102042       ADCO    0,0,SZC ;TEST FOR CALC<IR15 FALSE
15 00762 102003       ADC     0,0,SNC ;ALSO TEST ONES HOLD AF CRY
16 00763 063077       HALT            ;IF CRY=0 SEE NOT IR12
17
18                    ;ABOVE FAILURE IF CRY=0 MIGHT BE IN "NOT SCI" IR11
19 00764 102046 A9C:  ADCO    0,0,SEZ ;AGAIN TEST NOT ZC<IR14<NOT IR15
20 00765 102003       ADC     0,0,SNC ;SAME GATES AS LAST TEST (SZC)
21 00766 063077       HALT            ;EXCEPT FOR ZR<IR13
22
23                    ;CARRY SHOULD=1 COMING INTO NEXT TEST CHECK
24                    ;OF TRANSITION TO 0 ON ZC
25 00767 102022 A9D:  ADCZ    0,0,SZC ;SKIP ON ZC<IR14<NOT IR15
26 00770 063077       HALT            ;SEE CRY<IR11 THROUGH NOT SCI
27 00771 102040       ADCO    0,0     ;SET CRY=1
28 00772 102023       ADCZ    0,0,SNC ;TRANSITION CRY TO 0
29 00773 102002       ADC     0,0,SZC ;CHECK 0 REALLY GO THERE
30 00774 063077       HALT            ;CRY=0 IS SNC FAILED
31                    ;CRY=1 SEE CRY,IR11 IN "NOT SCI" GATTES OR ZC,LOAD CARRY
32
33                    ;CARRY=0 COMING INTO NEXT TEST CHECK NOT CRY,NOT IR10
34 00775 102023 A9E:  ADCZ    0,0,SNC ;ALSO NOT (CRY,IR11)
35 00776 102002       ADC     0,0,SZC ;CRY SHD HAVE STAYED 0
36 00777 063077       HALT            ;ALSO ZC NAD LOAD CARRY USED
```

```
!0085 .MAIN
01
02                      ;TEST CARRY TO TRANSITION FROM 0 TO 1
03 01000 102020 A9F:    ADCZ    0,0         ;SET CRY=1
04 01001 102042         ADCO    0,0,SZC     ;MAKE IT=1 AGAIN NOT CRY,IR10
05 01002 102003         ADC     0,0,SNC     ;DID I REALLY GET TO CRY
06 01003 063077         HALT                ;IF CRY=1 SZC FAILED
07                      ;IF CRY=0 SEE CALC,NOR IR12
08
09                      ;TEST COMPLIMENT OF CARRY IR11,IR10
10 01004 102020 A9G:    ADCZ    0,0         ;STE CRY=0
11 01005 102062         ADCC    0,0,SZC     ;TRANS CRY 0 TO 1 (SZC NOT)
12 01006 102003         ADC     0,0,SNC     ;CRY SHD=1
13 01007 063077         HALT                ;CRY=0 SEE CALC,LOOAD CARRY
14                      ;CARRY=0 SEE NOT SCI
15
16 01010 102040 A9H:    ADCO    0,0         ;SET CRY=1
17 01011 102063         ADCC    0,0,SNC     ;ZC SHD BE TRUE (NOT SNC)
18 01012 102002         ADC     0,0,SZC     ;CARRY SHD REALLY=0
19 01013 063077         HALT                ;CRY=1 SEE ZC AND LOAD CARRY
20
21                      ;TEST CARRY NO LOAD IR12=1 TO PREVENT CARRY CHANGE
22 01014 102020 A9I:    ADCZ    0,0
23 01015 102052         ADCO#   0,0,SZC     ;NO LOAD CRY IR12=1
24 01016 102002         ADC     0,0,SZC
25 01017 063077         HALT                ;CALC,IR12
26
27 01020 102040 A9J:    ADCO    0,0
28 01021 102033         ADCZ#   0,0,SNC     ;CRY SHD STAY=1 IR12=1
29 01022 102003         ADC     0,0,SNC
30 01023 063077         HALT                ;ZC,NOT LOAD CARRY
```

```
;0086 .MAIN
01
02                      ;TEST FOR ADC TO SET AC0=MOSTLY U'S AND SNR TO/ SKIP
03                      ;START BUILDING INSTRUCTIONS TO CREATE CONSTANTS
04                      ;VERY LITTLE LOGIC IS VERIFIED YET
05 01024 102005 A20:    ADC     0,0,SNR ;ANY RESULT IN AX0 SHD CAUSE SKP
06 01025 063077         HALT            ;AC0 ANYTHING BUT 0 IS SNR FAILED
07                      ;AC0 NOT=0 SEE IR15 IN SKIP CONTROL AND ZR AND GATES
08                      ;AC0=0 ADC MAY=SUB SEE ALU ROM NOT IR7 INPUT
09
10                  ;SZR SHOULD NOT SKIP WHEN AC0 NOT=0
11 01026 102004 A21:    ADC     0,0,SZR ;TEST A2 INDICATES AC0 NOT=0
12 01027 102005         ADC     0,0,SNR ;AS RESULT AF AN ADC
13 01030 063077         HALT            ;SZR SKIPPED IF AC0 NOT=0
14
15                  ;ATTEMPT TO GENERATE AN ALL 0'S CONSTANT VIA ADC+COM
16                  ;ALSO TESTS SZR TO SKIP IN GROSS CASE
17 01031 102000 A22:    ADC     0,0     ;ADC MAY NOT YET=-1
18 01032 100004         COM     0,0,SZR ;OR COM MAY ALSO FAIL
19 01033 063077         HALT            ;RESULT DOES NOT=0
20                      ;RESULT IN AC0 SHOULD HELP TO
21                      ;ISOLATE PROBLEM TO A BIT OR CARRY GATE THROUGH THE ALU
22                      ;AC0=0 IS FAILED TO SKIP IR15=0 IN SKIP LOGIC
23                      ;IF COM 0,0=-1 THEN COM MAY=MOV OR ADC IR5+IR6
24
25                  ;TEST ZERO CARRY SKIP FROM COM 0,0
26 01034 102020 A23:    ADCZ    0,0     ;0 TO CARRY=1 TO AC0
27 01035 100002         COM     0,0,SZC ;CARRY SHD STILL=0
28 01036 063077         HALT
29
30                  ;TEST SKIP EITHER ZERO WITH BOTH AC AND CARRY=0
31 01037 102020 A24:    ADCZ    0,0
32 01040 100006         COM     0,0,SEZ ;BOTH RESULT AND CARRY=0
33 01041 063077         HALT            ;SEZ FAILED BOTH=0
34                      ;SEE IR13,ZR+IR14,ZC,NOT IR15 ((NEG AND) SKIP CONTROL)
35
36                  ;TEST SKIP EITHER ZERO WITH AC=0 AND    CARRY=1
37 01042 102040 A25:    ADCO    0,0
38 01043 100006         COM     0,0,SEZ ;RES=0 BUT CARRY=1
39 01044 063077         HALT            ;SEE ZR,IR13,NOT IR15
```

```
10087 .MAIN
01
02                ;THE NEXT SERIES OF TESTS VERIFY
03                ;THAT REFERENCING ONE AC DOES NOT DISTRUB THE OTHERS
04
05                        .MACRO ACITS
06
07                ;AC ISOLATION TEST11
08                ;AC111:
09                        ADC     12,12
10                        COM     12,12   ;SET SC12 TO 0
11                        ADC     13,13   ;SET SC13 TO -1
12                        MOV     12,12,SZR       ;TEST AC12 TO STILL=0
13                        HALT            ;AC13 DESTINATION DISTURBED AC12
14                %
15
16
17
18
19
20
21
22                        ACITS   00      0       1
23
24                ;AC ISOLATION TEST00
25                ;AC100:
26 01045 102000           ADC     0,0
27 01046 100000           COM     0,0     ;SET SC0 TO 0
28 01047 126000           ADC     1,1     ;SET SC1 TO -1
29 01050 101004           MOV     0,0,SZR ;TEST AC0 TO STILL=0
30 01051 063077           HALT            ;AC1 DESTINATION DISTURBED AC0
31
32                        ACITS   01      0       2
33
34                ;AC ISOLATION TEST01
35                ;AC101:
36 01052 102000           ADC     0,0
37 01053 100000           COM     0,0     ;SET SC0 TO 0
38 01054 152000           ADC     2,2     ;SET SC2 TO -1
39 01055 101004           MOV     0,0,SZR ;TEST AC0 TO STILL=0
40 01056 063077           HALT            ;AC2 DESTINATION DISTURBED AC0
41
42                        ACITS   02      0       3
43
44                ;AC ISOLATION TEST02
45                ;AC102:
46 01057 102000           ADC     0,0
47 01060 100000           COM     0,0     ;SET SC0 TO 0
48 01061 176000           ADC     3,3     ;SET SC3 TO -1
49 01062 101004           MOV     0,0,SZR ;TEST AC0 TO STILL=0
50 01063 063077           HALT            ;AC3 DESTINATION DISTURBED AC0
51
52                        ACITS   03      1       0
53
54                ;AC ISOLATION TEST03
55                ;AC103:
56 01064 126000           ADC     1,1
57 01065 124000           COM     1,1     ;SET SC1 TO 0
58 01066 102000           ADC     0,0     ;SET SC0 TO -1
59 01067 125004           MOV     1,1,SZR ;TEST AC1 TO STILL=0
60 01070 063077           HALT            ;AC0 DESTINATION DISTURBED AC1
```

```
 0088 .MAIN
01
02                      ACITS   04      1       2
03
04              ;AC ISOLATION TEST04
05              ;ACI04:
06 01071 126000         ADC     1,1
07 01072 124000         COM     1,1     ;SET SC1 TO 0
08 01073 152000         ADC     2,2     ;SET SC2 TO -1
09 01074 125004         MOV     1,1,SZR ;TEST AC1 TO STILL=0
10 01075 063077         HALT            ;AC2 DESTINATION DISTURBED AC1
11
12                      ACITS   05      1       3
13
14              ;AC ISOLATION TEST05
15              ;ACI05:
16 01076 126000         ADC     1,1
17 01077 124000         COM     1,1     ;SET SC1 TO 0
18 01100 176000         ADC     3,3     ;SET SC3 TO -1
19 01101 125004         MOV     1,1,SZR ;TEST AC1 TO STILL=0
20 01102 063077         HALT            ;AC3 DESTINATION DISTURBED AC1
21
22                      ACITS   06      2       0
23
24              ;AC ISOLATION TEST06
25              ;ACI06:
26 01103 152000         ADC     2,2
27 01104 150000         COM     2,2     ;SET SC2 TO 0
28 01105 102000         ADC     0,0     ;SET SC0 TO -1
29 01106 151004         MOV     2,2,SZR ;TEST AC2 TO STILL=0
30 01107 063077         HALT            ;AC0 DESTINATION DISTURBED AC2
31
32                      ACITS   07      2       1
33
34              ;AC ISOLATION TEST07
35              ;ACI07:
36 01110 152000         ADC     2,2
37 01111 150000         COM     2,2     ;SET SC2 TO 0
38 01112 126000         ADC     1,1     ;SET SC1 TO -1
39 01113 151004         MOV     2,2,SZR ;TEST AC2 TO STILL=0
40 01114 063077         HALT            ;AC1 DESTINATION DISTURBED AC2
41
42                      ACITS   08      2       3
43
44              ;AC ISOLATION TEST08
45              ;ACI08:
46 01115 152000         ADC     2,2
47 01116 150000         COM     2,2     ;SET SC2 TO 0
48 01117 176000         ADC     3,3     ;SET SC3 TO -1
49 01120 151004         MOV     2,2,SZR ;TEST AC2 TO STILL=0
50 01121 063077         HALT            ;AC3 DESTINATION DISTURBED AC2
51
52                      ACITS   09      3       0
53
54              ;AC ISOLATION TEST09
55              ;ACI09:
56 01122 176000         ADC     3,3
57 01123 174000         COM     3,3     ;SET SC3 TO 0
58 01124 102000         ADC     0,0     ;SET SC0 TO -1
59 01125 175004         MOV     3,3,SZR ;TEST AC3 TO STILL=0
60 01126 063077         HALT            ;AC0 DESTINATION DISTURBED AC3
```

```
 0089 .MAIN
01
02                      ACITS   10      3       1
03
04              ;AC ISOLATION TEST10
05              ;ACI10:
06 01127 176000         ADC     3,3
07 01130 174000         COM     3,3     ;SET SC3 TO 0
08 01131 126000         ADC     1,1     ;SET SC1 TO -1
09 01132 175004         MOV     3,3,SZR ;TEST AC3 TO STILL=0
10 01133 063077         HALT            ;AC1 DESTINATION DISTURBED AC3
11
12                      ACITS   11      3       2
13
14              ;AC ISOLATION TEST11
15              ;ACI11:
16 01134 176000         ADC     3,3
17 01135 174000         COM     3,3     ;SET SC3 TO 0
18 01136 152000         ADC     2,2     ;SET SC2 TO -1
19 01137 175004         MOV     3,3,SZR ;TEST AC3 TO STILL=0
20 01140 063077         HALT            ;AC2 DESTINATION DISTURBED AC3
21
22
23
```

```
10090 .MAIN
01
02                ;THE FOLLOWING TESTS INSURE 0'S ISOLATION
03                ;OF AC TO AC
04
05                        .MACRO ACIT2    ;0'S ISOLATION TEST
06                ACI11:  ADC     12,12   ;SET AC12=-1
07                        COM     12,13   ;SET 0'S TO AC13
08                        COM     12,12,SZR       ;AC12 SHD STILL=-1
09                        HALT            ;0'S TO AC13 DISTURBED AC12
10                %
11
12
13
14                        ACIT2   12      0       1
15 01141 102000 ACI12:  ADC     0,0     ;SET AC0=-1
16 01142 104000         COM     0,1     ;SET 0'S TO AC1
17 01143 100004         COM     0,0,SZR ;AC0 SHD STILL=-1
18 01144 063077         HALT            ;0'S TO AC1 DISTURBED AC0
19
20                        ACIT2   13      0       2
21 01145 102000 ACI13:  ADC     0,0     ;SET AC0=-1
22 01146 110000         COM     0,2     ;SET 0'S TO AC2
23 01147 100004         COM     0,0,SZR ;AC0 SHD STILL=-1
24 01150 063077         HALT            ;0'S TO AC2 DISTURBED AC0
25
26                        ACIT2   14      0       3
27 01151 102000 ACI14:  ADC     0,0     ;SET AC0=-1
28 01152 114000         COM     0,3     ;SET 0'S TO AC3
29 01153 100004         COM     0,0,SZR ;AC0 SHD STILL=-1
30 01154 063077         HALT            ;0'S TO AC3 DISTURBED AC0
31
32                        ACIT2   15      1       0
33 01155 126000 ACI15:  ADC     1,1     ;SET AC1=-1
34 01156 120000         COM     1,0     ;SET 0'S TO AC0
35 01157 124004         COM     1,1,SZR ;AC1 SHD STILL=-1
36 01160 063077         HALT            ;0'S TO AC0 DISTURBED AC1
37
38                        ACIT2   16      1       2
39 01161 126000 ACI16:  ADC     1,1     ;SET AC1=-1
40 01162 130000         COM     1,2     ;SET 0'S TO AC2
41 01163 124004         COM     1,1,SZR ;AC1 SHD STILL=-1
42 01164 063077         HALT            ;0'S TO AC2 DISTURBED AC1
43
44                        ACIT2   17      1       3
45 01165 126000 ACI17:  ADC     1,1     ;SET AC1=-1
46 01166 134000         COM     1,3     ;SET 0'S TO AC3
47 01167 124004         COM     1,1,SZR ;AC1 SHD STILL=-1
48 01170 063077         HALT            ;0'S TO AC3 DISTURBED AC1
49
50                        ACIT2   18      2       0
51 01171 152000 ACI18:  ADC     2,2     ;SET AC2=-1
52 01172 140000         COM     2,0     ;SET 0'S TO AC0
53 01173 150004         COM     2,2,SZR ;AC2 SHD STILL=-1
54 01174 063077         HALT            ;0'S TO AC0 DISTURBED AC2
55
56                        ACIT2   19      2       1
57 01175 152000 ACI19:  ADC     2,2     ;SET AC2=-1
58 01176 144000         COM     2,1     ;SET 0'S TO AC1
59 01177 150004         COM     2,2,SZR ;AC2 SHD STILL=-1
60 01200 063077         HALT            ;0'S TO AC1 DISTURBED AC2
```

```
 0091 .MAIN
01
02                              ACIT2   20      2       3
03 01201 152000 ACI20:  ADC     2,2             ;SET AC2=-1
04 01202 154000         COM     2,3             ;SET 0'S TO AC3
05 01203 150004         COM     2,2,SZR         ;AC2 SHD STILL=-1
06 01204 063077         HALT                    ;0'S TO AC3 DISTURBED AC2
07
08                              ACIT2   21      3       0
09 01205 176000 ACI21:  ADC     3,3             ;SET AC3=-1
10 01206 160000         COM     3,0             ;SET 0'S TO AC0
11 01207 174004         COM     3,3,SZR         ;AC3 SHD STILL=-1
12 01210 063077         HALT                    ;0'S TO AC0 DISTURBED AC3
13
14                              ACIT2   22      3       1
15 01211 176000 ACI22:  ADC     3,3             ;SET AC3=-1
16 01212 164000         COM     3,1             ;SET 0'S TO AC1
17 01213 174004         COM     3,3,SZR         ;AC3 SHD STILL=-1
18 01214 063077         HALT                    ;0'S TO AC1 DISTURBED AC3
19
20                              ACIT2   23      3       2
21 01215 176000 ACI23:  ADC     3,3             ;SET AC3=-1
22 01216 170000         COM     3,2             ;SET 0'S TO AC2
23 01217 174004         COM     3,3,SZR         ;AC3 SHD STILL=-1
24 01220 063077         HALT                    ;0'S TO AC2 DISTURBED AC3
25
26
27
```

```
;0092 .MAIN
01
02                ;AT THIS POINT IN THE TEST THE FOLLOWING
03                ;ITEMS HAVE BEEN VERIFIED
04                ;1. NONE OF THE ALC INSTRUCTIONS SKIP EXTRANEOUSLY
05                ;2. CRY CAN BE SET TO 1 OR 0 AND CRY SKIPS
06                        ;FUNCTION CORRECTLY
07                ;3. A CONSTANT OTHER THAN 0 CAN BE GENERATED
08                        ;BY AN ADC ANY AC TO ITSELF
09                ;4. A CONSTANT THAT AT LEAST APPEARS TO=0 CAN
10                        ;BE GENERATED BY AN ADC+COM ANY AC TO ITSELF
11                ;5. ANY AC MAY BE REFERENCED BY EITHER
12                        ;AN ADC OR COM WITHOUT DISTURBING THE OTHERS
13                ;6. SNR SKIPS ON =1 DOES NOT SKIP ON 0
14                ;7. SZR SKIPS ON 0 DOES NOT SKIP ON =1
15                ;8. NO TRANSFER (IR 12=1) INHIBITS CARRY CHANGE
16
17                ;TEST LEFT SHIFT OF A 1 INTO 0 CRY
18 01221 102020 A40:    ADCZ    0,0
19 01222 101102         MOVL    0,0,SZC ;MAKE LEFT SHIFT CRY IN=1
20 01223 101003         MOV     0,0,SNC ;TEST FOR CRY REALLY=1
21 01224 063077         HALT            ;LEFT SHIFT IR9 FAILED
22                      ;IF GATE IR8=1 AND CALC IS TRUE TEST WILL ALSO FAIL (SWAP
23
24                ;TEST LEFT SHIFT OF A 0 INTO A 1 CRY
25 01225 102040 A41:    ADCO    0,0
26 01226 100103         COML    0,0,SNC ;CRY INPUT (ZC)
27 01227 101002         MOV     0,0,SZC ;DID 0 REALLY GET TO CRY
28 01230 063077         HALT            ;LEFT SHIFT (IR9) 0 INTO CRY
29
30                ;TEST FOR NO BITS TO PICK UP ON SHIFT LEFT
31 01231 102020 A42:    ADCZ    0,0     ;AC0=-1 CRY =0
32 01232 100105         COML    0,0,SNR ;TEST RESULT LEVELS=0
33 01233 101004         MOV     0,0,SZR ;AND    ACTUAL RESULT=0
34 01234 063077         HALT            ;AC0 L SHOULD=0
35
36                ;TEST THE TRANSFER OF A CRY=1 INTO BIT 15 AC 0
37 01235 102040 A43:    ADCO    0,0
38 01236 100105         COML    0,0,SNR ;CRY SHOULD=1 TO AC 15
39 01237 063077         HALT            ;IF AC0=0 SEE ALU15
40                      ;IF AC0=+1 SEE NOT SUM 15 INTO SKIP LOGIC
41                      ;IN ABOVE TEST ALU LEVEL INPUT IS NOT SCI (FALSE)
42                      ;NOT SUM 15 GOES LOW FOR LEFT SHIFT ALSO
43
44                ;TEST BIT 15=1 STRAIGHT TRANSFER THROUGH
45 01240 102040 A44:    ADCO    0,0
46 01241 100104         COML    0,0,SZR ;IN CASE LEVEL NOT SUM 15 FAILS
47 01242 101005         MOV     0,0,SNR ;AC0=+1 RESULT IS NON ZERO
48 01243 063077         HALT
49                      ;ABOVE FAILURE IS MOST PROBABLY "NOT ALU 15" FALSE WAS
50                      ;TRUE OR "NOT SUM 15" FALSE INTO ZR AND'S IN SKP LOGIC
```

```
10093 .MAIN
01
02                ;TEST RIGHT SHIFT LOGIC INTO CRY
03                ;TEST ONES SHIFT INTO A 0 CRY
04                ;TEST OF IR8=1 ENABLES RIGHT SHIFT INPUTS
05 01244 102223 A45:    ADCZR   0,0,SNC ;TEST INPUT TO CRY=1
06 01245 063077         HALT
07                      ;IF IR9 AND CALC GATE IS TRUE TEST WILL ALSO FAIL (SWAP)
08
09 01246 102222 A46:    ADCZR   0,0,SZC ;INPUT TO CRY=1
10 01247 100003         COM     0,0,SNC ;CRY RIGHT SHD STILL=1
11 01250 063077         HALT
12                      ;TEST RIGHT 0 INPUT TO CRY=1
13
14 01251 102040 A47:    ADCO    0,0
15 01252 100203         COMR    0,0,SNC
16 01253 100002         COM     0,0,SZC
17 01254 063077         HALT            ;CRY SHOULD=0
18                      ;TEST OF NOT ALU0 INPUT TO ZC AND IR*8=1
19
20                ;TEST FOR NO BITS TO PICK UP ON RIGHT SHIFT
21 01255 102020 A48:    ADCZ    0,0     ;(AC0)=-1 CRY=0
22 01256 100205         COMR    0,0,SNR ;SHIFT 0'S RIGHT
23 01257 101004         MOV     0,0,SZR ;RESULT SHOULD REMAIN=0
24 01260 063077         HALT            ;RIGHT SHIFT ALL 0'S FAILED
25                      ;EXAMINE AC0 TO DETERMINE BITS PICKED SHIFT RIGHT
26                      ;SHIFT CRY=1 RIGHT INTO BIT 0
27                      ;ALSO TEST BIT 0=1 INTO NOT ZR
28
29 01261 102040 A49:    ADCO    0,0     ;CRY=1 AC0=-1
30 01262 100204         COMR    0,0,SZR ;RIGHT SHIFT 0'S CRY=1 TO BIT 0
31 01263 101205         MOVR    0,0,SNR ;TEST RESULT TO REALLY HOLD
32 01264 063077         HALT            ;RIGHT SHIFT CRY=1 FAILED
33                      ;ABOVE HALT CAN BE NOT SCI INTO NOT SUM 0 (AC0 WILL=0)
34                      ;OR NOT SUM 0 INTO ZR AND GATES IN SKIP LOGIC (AC0=10000)
35
36                ;TEST RIGHT SHIFT OF AC0=0'S INTO AC1
37                ;START BUILDING DOUBLE REGISTERS FOR TEST USAGE
38 01265 102000 A50:    ADC     0,0
39 01266 126020         ADCZ    1,1
40 01267 104200         COMR    0,1
41 01270 125004         MOV     1,1,SZR
42 01271 063077         HALT            ;RIGHT SHIFT ALL 0'S TO AC1
43
44                ;TRANSFER CRY=1 INTO AC1 BIT 0 SHIFT RIGHT
45 01272 102000 A51:    ADC     0,0     ;AC0=-1
46 01273 104040         COMO    0,1     ;AC1=0 CRY=1
47 01274 104200         COMR    0,1     ;RIGHT SHIFT NOT(0) TO AC1
48 01275 125005         MOV     1,1,SNR ;RESULT SHD=NOT 0 BIT 0=1
49 01276 063077         HALT            ;AC1 SHD=10000
50                      ;ABOVE TESTS WERE TO VERIFY TRANSFER OF AC0 TO AC OCCURS
51                      ;RIGHT SHIFT OR CRY=1 TO BIT 0 WAS PREV. VERIFIED
```

```
10094 .MAIN
01                      ;DEFINE MACRO TO TEST SHIFTS OF
02                      ;A SINGLE ONE BIT INTO THE NEXT POSITION
03
04                              .MACRO SHIFT
05                              ;THIS IS A 15 SHIFT TEST OF BIT 12 TO BIT 13
06                              ;AC0 SHD = 14 COMING INTO THE TEST
07                      ;AS11:
08                              MOV15   0,1,SZR ;TEST NOT ALU12 INTO SUM13
09                              MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
10                              HALT            ;RESULT IN AC1 SHD=16
11                              MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
12                              HALT            ;STRAIGHT TRANSFER BIT 13 FAILED
13                                              ;BIT 13 15 SHIFT FAILED IF AC1=0
14                                              ;IF AC1=16 B13 TO ZR AND GATES FAILED.
15                      %
16
17                              ;RIGHT SHIFT SINGLE BIT TESTS
18                              ;SETUP A 1 IN BIT0
19 01277 102040                 ADCO    0,0
20 01300 100200                 COMR    0,0
21 01301 101005                 MOV     0,0,SNR
22 01302 063077                 HALT            ;BIT 0 SETUP FAILED
23
24
25
26                              SHIFT   R00,0,1,100000,R,040000
27                              ;THIS IS A R SHIFT TEST OF BIT 0 TO BIT 1
28                              ;AC0 SHD = 100000 COMING INTO THE TEST
29                      ;ASR00:
30 01303 105204                 MOVR    0,1,SZR ;TEST NOT ALU0 INTO SUM1
31 01304 125005                 MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
32 01305 063077                 HALT            ;RESULT IN AC1 SHD=040000
33 01306 121005                 MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
34 01307 063077                 HALT            ;STRAIGHT TRANSFER BIT 1 FAILED
35                                              ;BIT 1 R SHIFT FAILED IF AC1=0
36                                              ;IF AC1=040000 B1 TO ZR AND GATES FAILED.
37
38                              SHIFT   R01,1,2,040000,R,020000
39                              ;THIS IS A R SHIFT TEST OF BIT 1 TO BIT 2
40                              ;AC0 SHD = 040000 COMING INTO THE TEST
41                      ;ASR01:
42 01310 105204                 MOVR    0,1,SZR ;TEST NOT ALU1 INTO SUM2
43 01311 125005                 MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
44 01312 063077                 HALT            ;RESULT IN AC1 SHD=020000
45 01313 121005                 MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
46 01314 063077                 HALT            ;STRAIGHT TRANSFER BIT 2 FAILED
47                                              ;BIT 2 R SHIFT FAILED IF AC1=0
48                                              ;IF AC1=020000 B2 TO ZR AND GATES FAILED.
49
50                              SHIFT   R02,2,3,020000,R,010000
51                              ;THIS IS A R SHIFT TEST OF BIT 2 TO BIT 3
52                              ;AC0 SHD = 020000 COMING INTO THE TEST
53                      ;ASR02:
54 01315 105204                 MOVR    0,1,SZR ;TEST NOT ALU2 INTO SUM3
55 01316 125005                 MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
56 01317 063077                 HALT            ;RESULT IN AC1 SHD=010000
57 01320 121005                 MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
58 01321 063077                 HALT            ;STRAIGHT TRANSFER BIT 3 FAILED
59                                              ;BIT 3 R SHIFT FAILED IF AC1=0
60                                              ;IF AC1=010000 B3 TO ZR AND GATES FAILED.
```

```
 0095 ,MAIN
01
02                          SHIFT   R03,3,4,010000,R,004000
03                          ;THIS IS A R SHIFT TEST OF BIT 3 TO BIT 4
04                          ;AC0 SHD = 010000 COMING INTO THE TEST
05                    ;ASR03:
06 01322 105204             MOVR    0,1,SZR ;TEST NOT ALU3 INTO SUM4
07 01323 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
08 01324 063077             HALT            ;RESULT IN AC1 SHD=004000
09 01325 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
10 01326 063077             HALT            ;STRAIGHT TRANSFER BIT 4 FAILED
11                                          ;BIT 4 R SHIFT FAILED IF AC1=0
12                                          ;IF AC1=004000 B4 TO ZR AND GATES FAILED.
13
14                          SHIFT   R04,4,5,004000,R,002000
15                          ;THIS IS A R SHIFT TEST OF BIT 4 TO BIT 5
16                          ;AC0 SHD = 004000 COMING INTO THE TEST
17                    ;ASR04:
18 01327 105204             MOVR    0,1,SZR ;TEST NOT ALU4 INTO SUM5
19 01330 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
20 01331 063077             HALT            ;RESULT IN AC1 SHD=002000
21 01332 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
22 01333 063077             HALT            ;STRAIGHT TRANSFER BIT 5 FAILED
23                                          ;BIT 5 R SHIFT FAILED IF AC1=0
24                                          ;IF AC1=002000 B5 TO ZR AND GATES FAILED.
25
26                          SHIFT   R05,5,6,002000,R,001000
27                          ;THIS IS A R SHIFT TEST OF BIT 5 TO BIT 6
28                          ;AC0 SHD = 002000 COMING INTO THE TEST
29                    ;ASR05:
30 01334 105204             MOVR    0,1,SZR ;TEST NOT ALU5 INTO SUM6
31 01335 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
32 01336 063077             HALT            ;RESULT IN AC1 SHD=001000
33 01337 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
34 01340 063077             HALT            ;STRAIGHT TRANSFER BIT 6 FAILED
35                                          ;BIT 6 R SHIFT FAILED IF AC1=0
36                                          ;IF AC1=001000 B6 TO ZR AND GATES FAILED.
37
38                          SHIFT   R06,6,7,001000,R,000400
39                          ;THIS IS A R SHIFT TEST OF BIT 6 TO BIT 7
40                          ;AC0 SHD = 001000 COMING INTO THE TEST
41                    ;ASR06:
42 01341 105204             MOVR    0,1,SZR ;TEST NOT ALU6 INTO SUM7
43 01342 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
44 01343 063077             HALT            ;RESULT IN AC1 SHD=000400
45 01344 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
46 01345 063077             HALT            ;STRAIGHT TRANSFER BIT 7 FAILED
47                                          ;BIT 7 R SHIFT FAILED IF AC1=0
48                                          ;IF AC1=000400 B7 TO ZR AND GATES FAILED.
49
50                          SHIFT   R07,7,8,000400,R,000200
51                          ;THIS IS A R SHIFT TEST OF BIT 7 TO BIT 8
52                          ;AC0 SHD = 000400 COMING INTO THE TEST
53                    ;ASR07:
54 01346 105204             MOVR    0,1,SZR ;TEST NOT ALU7 INTO SUM8
55 01347 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
56 01350 063077             HALT            ;RESULT IN AC1 SHD=000200
57 01351 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
58 01352 063077             HALT            ;STRAIGHT TRANSFER BIT 8 FAILED
59                                          ;BIT 8 R SHIFT FAILED IF AC1=0
60                                          ;IF AC1=000200 B8 TO ZR AND GATES FAILED.
```

```
 0096 .MAIN
01
02                      SHIFT   R08,8,9,000200,R,000100
03                      ;THIS IS A R SHIFT TEST OF BIT 8 TO BIT 9
04                      ;AC0 SHD = 000200 COMING INTO THE TEST
05                  ;ASR08:
06 01353 105204         MOVR    0,1,SZR ;TEST NOT ALU8 INTO SUM9
07 01354 125005         MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
08 01355 063077         HALT            ;RESULT IN AC1 SHD=000100
09 01356 121005         MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
10 01357 063077         HALT            ;STRAIGHT TRANSFER BIT 9 FAILED
11                                      ;BIT 9 R SHIFT FAILED IF AC1=0
12                                      ;IF AC1=000100 B9 TO ZR AND GATES FAILED.
13
14                      SHIFT   R09,9,10,000100,R,000040
15                      ;THIS IS A R SHIFT TEST OF BIT 9 TO BIT 10
16                      ;AC0 SHD = 000100 COMING INTO THE TEST
17                  ;ASR09:
18 01360 105204         MOVR    0,1,SZR ;TEST NOT ALU9 INTO SUM10
19 01361 125005         MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
20 01362 063077         HALT            ;RESULT IN AC1 SHD=000040
21 01363 121005         MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
22 01364 063077         HALT            ;STRAIGHT TRANSFER BIT 10 FAILED
23                                      ;BIT 10 R SHIFT FAILED IF AC1=0
24                                      ;IF AC1=000040 B10 TO ZR AND GATES FAILED
25
26                      SHIFT   R10,10,11,000040,R,000020
27                      ;THIS IS A R SHIFT TEST OF BIT 10 TO BIT 11
28                      ;AC0 SHD = 000040 COMING INTO THE TEST
29                  ;ASR10:
30 01365 105204         MOVR    0,1,SZR ;TEST NOT ALU10 INTO SUM11
31 01366 125005         MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
32 01367 063077         HALT            ;RESULT IN AC1 SHD=000020
33 01370 121005         MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
34 01371 063077         HALT            ;STRAIGHT TRANSFER BIT 11 FAILED
35                                      ;BIT 11 R SHIFT FAILED IF AC1=0
36                                      ;IF AC1=000020 B11 TO ZR AND GATES FAILED
37
38                      SHIFT   R11,11,12,000020,R,000010
39                      ;THIS IS A R SHIFT TEST OF BIT 11 TO BIT 12
40                      ;AC0 SHD = 000020 COMING INTO THE TEST
41                  ;ASR11:
42 01372 105204         MOVR    0,1,SZR ;TEST NOT ALU11 INTO SUM12
43 01373 125005         MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
44 01374 063077         HALT            ;RESULT IN AC1 SHD=000010
45 01375 121005         MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
46 01376 063077         HALT            ;STRAIGHT TRANSFER BIT 12 FAILED
47                                      ;BIT 12 R SHIFT FAILED IF AC1=0
48                                      ;IF AC1=000010 B12 TO ZR AND GATES FAILED
49
50                      SHIFT   R12,12,13,000010,R,000004
51                      ;THIS IS A R SHIFT TEST OF BIT 12 TO BIT 13
52                      ;AC0 SHD = 000010 COMING INTO THE TEST
53                  ;ASR12:
54 01377 105204         MOVR    0,1,SZR ;TEST NOT ALU12 INTO SUM13
55 01400 125005         MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
56 01401 063077         HALT            ;RESULT IN AC1 SHD=000004
57 01402 121005         MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
58 01403 063077         HALT            ;STRAIGHT TRANSFER BIT 13 FAILED
59                                      ;BIT 13 R SHIFT FAILED IF AC1=0
60                                      ;IF AC1=000004 B13 TO ZR AND GATES FAILED
```

```
0097 ,MAIN
31
32                              SHIFT   R13,13,14,000004,R,000002
33                              ;THIS IS A R SHIFT TEST OF BIT 13 TO BIT 14
34                              ;AC0 SHD = 000004 COMING INTO THE TEST
35                      ;ASR13:
36 01404 105204                 MOVR    0,1,SZR ;TEST NOT ALU13 INTO SUM14
37 01405 125005                 MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
38 01406 063077                 HALT            ;RESULT IN AC1 SHD=000002
39 01407 121005                 MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
10 01410 063077                 HALT            ;STRAIGHT TRANSFER BIT 14 FAILED
11                                              ;BIT 14 R SHIFT FAILED IF AC1=0
12                                              ;IF AC1=000002 B14 TO ZR AND GATES FAILED
13
14                              SHIFT   R14,14,15,000002,R,000001
15                              ;THIS IS A R SHIFT TEST OF BIT 14 TO BIT 15
16                              ;AC0 SHD = 000002 COMING INTO THE TEST
17                      ;ASR14:
18 01411 105204                 MOVR    0,1,SZR ;TEST NOT ALU14 INTO SUM15
19 01412 125005                 MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
20 01413 063077                 HALT            ;RESULT IN AC1 SHD=000001
21 01414 121005                 MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
22 01415 063077                 HALT            ;STRAIGHT TRANSFER BIT 15 FAILED
23                                              ;BIT 15 R SHIFT FAILED IF AC1=0
24                                              ;IF AC1=000001 B15 TO ZR AND GATES FAILED
25
26
27 01416 105205 ASR15:  MOVR    0,1,SNR ;TEST BIT 15=1 TO CRY
28 01417 125004                 MOV     1,1,SZR ;AC1 SHD=0'S
29 01420 063077                 HALT
30 01421 125003                 MOV     1,1,SNC ;AND CRY SHD=1
31 01422 063077                 HALT
32
33                              ;LEFT SHIFT SINGLE BIT TESTS
34                              ;SET UP A 1 IN BIT 15
35 01423 102040                 ADCO 0,0
36 01424 100104                 COML 0,0,SZR
37 01425 101005                 MOV     0,0,SNR
38 01426 063077                 HALT            ;AC0 SHD=1 SETUP FAILED
```

```
10098 .MAIN
01
02                          SHIFT   L00,15,14,000001,L,000002
03                          ;THIS IS A L SHIFT TEST OF BIT 15 TO BIT 14
04                          ;AC0 SHD = 000001 COMING INTO THE TEST
05                    ;ASL00:
06 01427 105104             MOVL    0,1,SZR ;TEST NOT ALU15 INTO SUM14
07 01430 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
08 01431 063077             HALT            ;RESULT IN AC1 SHD=000002
09 01432 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
10 01433 063077             HALT            ;STRAIGHT TRANSFER BIT 14 FAILED
11                                          ;BIT 14 L SHIFT FAILED IF AC1=0
12                                          ;IF AC1=000002 B14 TO ZR AND GATES FAILED
13
14                          SHIFT   L01,14,13,000002,L,000004
15                          ;THIS IS A L SHIFT TEST OF BIT 14 TO BIT 13
16                          ;AC0 SHD = 000002 COMING INTO THE TEST
17                    ;ASL01:
18 01434 105104             MOVL    0,1,SZR ;TEST NOT ALU14 INTO SUM13
19 01435 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
20 01436 063077             HALT            ;RESULT IN AC1 SHD=000004
21 01437 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
22 01440 063077             HALT            ;STRAIGHT TRANSFER BIT 13 FAILED
23                                          ;BIT 13 L SHIFT FAILED IF AC1=0
24                                          ;IF AC1=000004 B13 TO ZR AND GATES FAILED
25
26                          SHIFT   L02,13,12,000004,L,000010
27                          ;THIS IS A L SHIFT TEST OF BIT 13 TO BIT 12
28                          ;AC0 SHD = 000004 COMING INTO THE TEST
29                    ;ASL02:
30 01441 105104             MOVL    0,1,SZR ;TEST NOT ALU13 INTO SUM12
31 01442 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
32 01443 063077             HALT            ;RESULT IN AC1 SHD=000010
33 01444 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
34 01445 063077             HALT            ;STRAIGHT TRANSFER BIT 12 FAILED
35                                          ;BIT 12 L SHIFT FAILED IF AC1=0
36                                          ;IF AC1=000010 B12 TO ZR AND GATES FAILED
37
38                          SHIFT   L03,12,11,000010,L,000020
39                          ;THIS IS A L SHIFT TEST OF BIT 12 TO BIT 11
40                          ;AC0 SHD = 000010 COMING INTO THE TEST
41                    ;ASL03:
42 01446 105104             MOVL    0,1,SZR ;TEST NOT ALU12 INTO SUM11
43 01447 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
44 01450 063077             HALT            ;RESULT IN AC1 SHD=000020
45 01451 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
46 01452 063077             HALT            ;STRAIGHT TRANSFER BIT 11 FAILED
47                                          ;BIT 11 L SHIFT FAILED IF AC1=0
48                                          ;IF AC1=000020 B11 TO ZR AND GATES FAILED
49
50                          SHIFT   L04,11,10,000020,L,000040
51                          ;THIS IS A L SHIFT TEST OF BIT 11 TO BIT 10
52                          ;AC0 SHD = 000020 COMING INTO THE TEST
53                    ;ASL04:
54 01453 105104             MOVL    0,1,SZR ;TEST NOT ALU11 INTO SUM10
55 01454 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
56 01455 063077             HALT            ;RESULT IN AC1 SHD=000040
57 01456 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
58 01457 063077             HALT            ;STRAIGHT TRANSFER BIT 10 FAILED
59                                          ;BIT 10 L SHIFT FAILED IF AC1=0
60                                          ;IF AC1=000040 B10 TO ZR AND GATES FAILED
```

```
 0099 .MAIN
01
02                              SHIFT   L05,10,9,000040,L,000100
03                              ;THIS IS A L SHIFT TEST OF BIT 10 TO BIT 9
04                              ;AC0 SHD = 000040 COMING INTO THE TEST
05                      ;ASL05:
06 01460 105104                 MOVL    0,1,SZR ;TEST NOT ALU10 INTO SUM9
07 01461 125005                 MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
08 01462 063077                 HALT            ;RESULT IN AC1 SHD=000100
09 01463 121005                 MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
10 01464 063077                 HALT            ;STRAIGHT TRANSFER BIT 9 FAILED
11                                              ;BIT 9 L SHIFT FAILED IF AC1=0
12                                              ;IF AC1=000100 B9 TO ZR AND GATES FAILED.
13
14                              SHIFT   L06,9,8,000100,L,000200
15                              ;THIS IS A L SHIFT TEST OF BIT 9 TO BIT 8
16                              ;AC0 SHD = 000100 COMING INTO THE TEST
17                      ;ASL06:
18 01465 105104                 MOVL    0,1,SZR ;TEST NOT ALU9 INTO SUM8
19 01466 125005                 MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
20 01467 063077                 HALT            ;RESULT IN AC1 SHD=000200
21 01470 121005                 MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
22 01471 063077                 HALT            ;STRAIGHT TRANSFER BIT 8 FAILED
23                                              ;BIT 8 L SHIFT FAILED IF AC1=0
24                                              ;IF AC1=000200 B8 TO ZR AND GATES FAILED.
25
26                              SHIFT   L07,8,7,000200,L,000400
27                              ;THIS IS A L SHIFT TEST OF BIT 8 TO BIT 7
28                              ;AC0 SHD = 000200 COMING INTO THE TEST
29                      ;ASL07:
30 01472 105104                 MOVL    0,1,SZR ;TEST NOT ALU8 INTO SUM7
31 01473 125005                 MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
32 01474 063077                 HALT            ;RESULT IN AC1 SHD=000400
33 01475 121005                 MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
34 01476 063077                 HALT            ;STRAIGHT TRANSFER BIT 7 FAILED
35                                              ;BIT 7 L SHIFT FAILED IF AC1=0
36                                              ;IF AC1=000400 B7 TO ZR AND GATES FAILED.
37
38                              SHIFT   L08,7,6,000400,L,001000
39                              ;THIS IS A L SHIFT TEST OF BIT 7 TO BIT 6
40                              ;AC0 SHD = 000400 COMING INTO THE TEST
41                      ;ASL08:
42 01477 105104                 MOVL    0,1,SZR ;TEST NOT ALU7 INTO SUM6
43 01500 125005                 MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
44 01501 063077                 HALT            ;RESULT IN AC1 SHD=001000
45 01502 121005                 MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
46 01503 063077                 HALT            ;STRAIGHT TRANSFER BIT 6 FAILED
47                                              ;BIT 6 L SHIFT FAILED IF AC1=0
48                                              ;IF AC1=001000 B6 TO ZR AND GATES FAILED.
49
50                              SHIFT   L09,6,5,001000,L,002000
51                              ;THIS IS A L SHIFT TEST OF BIT 6 TO BIT 5
52                              ;AC0 SHD = 001000 COMING INTO THE TEST
53                      ;ASL09:
54 01504 105104                 MOVL    0,1,SZR ;TEST NOT ALU6 INTO SUM5
55 01505 125005                 MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
56 01506 063077                 HALT            ;RESULT IN AC1 SHD=002000
57 01507 121005                 MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
58 01510 063077                 HALT            ;STRAIGHT TRANSFER BIT 5 FAILED
59                                              ;BIT 5 L SHIFT FAILED IF AC1=0
60                                              ;IF AC1=002000 B5 TO ZR AND GATES FAILED.
```

```
 0100 .MAIN
01
02                          SHIFT   L10,5,4,002000,L,004000
03                          ;THIS IS A L SHIFT TEST OF BIT 5 TO BIT 4
04                          ;AC0 SHD = 002000 COMING INTO THE TEST
05                    ;ASL10:
06 01511 105104             MOVL    0,1,SZR ;TEST NOT ALU5 INTO SUM4
07 01512 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
08 01513 063077             HALT            ;RESULT IN AC1 SHD=004000
09 01514 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
10 01515 063077             HALT            ;STRAIGHT TRANSFER BIT 4 FAILED
11                                          ;BIT 4 L SHIFT FAILED IF AC1=0
12                                          ;IF AC1=004000 B4 TO ZR AND GATES FAILED.
13
14                          SHIFT   L11,4,3,004000,L,010000
15                          ;THIS IS A L SHIFT TEST OF BIT 4 TO BIT 3
16                          ;AC0 SHD = 004000 COMING INTO THE TEST
17                    ;ASL11:
18 01516 105104             MOVL    0,1,SZR ;TEST NOT ALU4 INTO SUM3
19 01517 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
20 01520 063077             HALT            ;RESULT IN AC1 SHD=010000
21 01521 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
22 01522 063077             HALT            ;STRAIGHT TRANSFER BIT 3 FAILED
23                                          ;BIT 3 L SHIFT FAILED IF AC1=0
24                                          ;IF AC1=010000 B3 TO ZR AND GATES FAILED.
25
26                          SHIFT   L12,3,2,010000,L,020000
27                          ;THIS IS A L SHIFT TEST OF BIT 3 TO BIT 2
28                          ;AC0 SHD = 010000 COMING INTO THE TEST
29                    ;ASL12:
30 01523 105104             MOVL    0,1,SZR ;TEST NOT ALU3 INTO SUM2
31 01524 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
32 01525 063077             HALT            ;RESULT IN AC1 SHD=020000
33 01526 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
34 01527 063077             HALT            ;STRAIGHT TRANSFER BIT 2 FAILED
35                                          ;BIT 2 L SHIFT FAILED IF AC1=0
36                                          ;IF AC1=020000 B2 TO ZR AND GATES FAILED.
37
38                          SHIFT   L13,2,1,020000,L,040000
39                          ;THIS IS A L SHIFT TEST OF BIT 2 TO BIT 1
40                          ;AC0 SHD = 020000 COMING INTO THE TEST
41                    ;ASL13:
42 01530 105104             MOVL    0,1,SZR ;TEST NOT ALU2 INTO SUM1
43 01531 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
44 01532 063077             HALT            ;RESULT IN AC1 SHD=040000
45 01533 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
46 01534 063077             HALT            ;STRAIGHT TRANSFER BIT 1 FAILED
47                                          ;BIT 1 L SHIFT FAILED IF AC1=0
48                                          ;IF AC1=040000 B1 TO ZR AND GATES FAILED.
49
50                          SHIFT   L14,1,0,040000,L,100000
51                          ;THIS IS A L SHIFT TEST OF BIT 1 TO BIT 0
52                          ;AC0 SHD = 040000 COMING INTO THE TEST
53                    ;ASL14:
54 01535 105104             MOVL    0,1,SZR ;TEST NOT ALU1 INTO SUM0
55 01536 125005             MOV     1,1,SNR ;STRAIGHT TRANSFER COULD ALSO FAIL
56 01537 063077             HALT            ;RESULT IN AC1 SHD=100000
57 01540 121005             MOV     1,0,SNR ;MOVE RESULT BACK TO AC0 NXT TST
58 01541 063077             HALT            ;STRAIGHT TRANSFER BIT 0 FAILED
59                                          ;BIT 0 L SHIFT FAILED IF AC1=0
60                                          ;IF AC1=100000 B0 TO ZR AND GATES FAILED.
```

```
 0101 .MAIN
21
22 01542 105105 ASL15: MOVL    0,1,SNR ;AC0=100000
23 01543 125004        MOV     1,1,SZR ;RESULT LEFT SHD=0'S
24 01544 063077        HALT            ;PICKED UP EXTRA BITS LEFT
25 01545 125003        MOV     1,1,SNC
26 01546 063077        HALT            ;LOST CARRY LAST LEFTSHIFT
27
28              ;SHIFT A 0 BIT FIELD OF ONES
29              ;DEFINITION OF MACRO FOR TESTING SAME
10
11                      .MACRO SHIFZ
12                      ;THIS IS A 15 SHIFT TEST OF NOT BIT 12 TO NOT BIT 13
13              ;AS11:
14                      MOVO15  0,1     ;AC0 SHD=14 COMING INTO TEST
15                      COMZ15  0,2,SNR ;AC2 SHD=COM OF 16
16                      HALT
17                      COM     2,2     ;AC2 SHD NOW=AC1
18                      ADC     1,2     ;THE ADDITION OF COM SHD=-1
19                      COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
20                      HALT            ;BIT 12 15 TO BIT 13 FAILED
21                      ;AC0=14 ORIGINAL TO 16 IN AC1 AC2 WAS COM OF AC1
22                      ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
23                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU12 INTO NOT SUM1
24                      MOV     1,0     ;SET UP NEXT TEST
25              %
26
27                      ;SET UP SERIES OF RIGHT SHIFT TESTS
28                      ;BY SETTING AC0 TO 077777
29 01547 102000         ADC     0,0
30 01550 100240         COMOR   0,0     ;SEQUENCE MOST LIKELY TO
31 01551 100000         COM     0,0     ;SET AC0=077777
32 01552 110005         COM     0,2,SNR
33 01553 063077         HALT            ;SETUP FAILED CRY=0 TO BIT 0
34 01554 105000         MOV     0,1
35 01555 150000         COM     2,2     ;RETEST INSTRUCTION
36 01556 132000         ADC     1,2     ;CHECK SEQUENCE
37 01557 150004         COM     2,2,SZR ;JUST TO MAKE SURE IT WORKS
38 01560 063077         HALT            ;COMPARE OF AC0=077777 FAILED
```

```
!0102 .MAIN
01
02                          SHIFZ R16,0,1,077777,R,137777
03                          ;THIS IS A R SHIFT TEST OF NOT BIT 0 TO NOT BIT 1
04                    ;ASR16:
05 01561 105240             MOVOR   0,1       ;AC0 SHD=077777 COMING INTO TEST
06 01562 110225             COMZR   0,2,SNR   ;AC2 SHD=COM OF 137777
07 01563 063077             HALT
08 01564 150000             COM     2,2       ;AC2 SHD NOW=AC1
09 01565 132000             ADC     1,2       ;THE ADDITION OF COM SHD=-1
10 01566 150004             COM     2,2,SZR   ;AND RESULT SHD=0 ALL SHIFTS ON
11 01567 063077             HALT              ;BIT 0 R TO BIT 1 FAILED
12                          ;AC0=077777 ORIGINAL TO 137777 IN AC1 AC2 WAS COM OF AC1
13                          ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
14                          ;WAS PREVIOUSLY VERIFIED SEE NOT ALU0 INTO NOT SUM1
15 01570 121000             MOV     1,0       ;SET UP NEXT TEST
16
17                          SHIFZ R17,1,2,137777,R,157777
18                          ;THIS IS A R SHIFT TEST OF NOT BIT 1 TO NOT BIT 2
19                    ;ASR17:
20 01571 105240             MOVOR   0,1       ;AC0 SHD=137777 COMING INTO TEST
21 01572 110225             COMZR   0,2,SNR   ;AC2 SHD=COM OF 157777
22 01573 063077             HALT
23 01574 150000             COM     2,2       ;AC2 SHD NOW=AC1
24 01575 132000             ADC     1,2       ;THE ADDITION OF COM SHD=-1
25 01576 150004             COM     2,2,SZR   ;AND RESULT SHD=0 ALL SHIFTS ON
26 01577 063077             HALT              ;BIT 1 R TO BIT 2 FAILED
27                          ;AC0=137777 ORIGINAL TO 157777 IN AC1 AC2 WAS COM OF AC1
28                          ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
29                          ;WAS PREVIOUSLY VERIFIED SEE NOT ALU1 INTO NOT SUM2
30 01600 121000             MOV     1,0       ;SET UP NEXT TEST
31
32                          SHIFZ R18,2,3,157777,R,167777
33                          ;THIS IS A R SHIFT TEST OF NOT BIT 2 TO NOT BIT 3
34                    ;ASR18:
35 01601 105240             MOVOR   0,1       ;AC0 SHD=157777 COMING INTO TEST
36 01602 110225             COMZR   0,2,SNR   ;AC2 SHD=COM OF 167777
37 01603 063077             HALT
38 01604 150000             COM     2,2       ;AC2 SHD NOW=AC1
39 01605 132000             ADC     1,2       ;THE ADDITION OF COM SHD=-1
40 01606 150004             COM     2,2,SZR   ;AND RESULT SHD=0 ALL SHIFTS ON
41 01607 063077             HALT              ;BIT 2 R TO BIT 3 FAILED
42                          ;AC0=157777 ORIGINAL TO 167777 IN AC1 AC2 WAS COM OF AC1
43                          ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
44                          ;WAS PREVIOUSLY VERIFIED SEE NOT ALU2 INTO NOT SUM3
45 01610 121000             MOV     1,0       ;SET UP NEXT TEST
46
47                          SHIFZ R19,3,4,167777,R,173777
48                          ;THIS IS A R SHIFT TEST OF NOT BIT 3 TO NOT BIT 4
49                    ;ASR19:
50 01611 105240             MOVOR   0,1       ;AC0 SHD=167777 COMING INTO TEST
51 01612 110225             COMZR   0,2,SNR   ;AC2 SHD=COM OF 173777
52 01613 063077             HALT
53 01614 150000             COM     2,2       ;AC2 SHD NOW=AC1
54 01615 132000             ADC     1,2       ;THE ADDITION OF COM SHD=-1
55 01616 150004             COM     2,2,SZR   ;AND RESULT SHD=0 ALL SHIFTS ON
56 01617 063077             HALT              ;BIT 3 R TO BIT 4 FAILED
57                          ;AC0=167777 ORIGINAL TO 173777 IN AC1 AC2 WAS COM OF AC1
58                          ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
59                          ;WAS PREVIOUSLY VERIFIED SEE NOT ALU3 INTO NOT SUM4
60 01620 121000             MOV     1,0       ;SET UP NEXT TEST
```

```
0103 .MAIN
01
02                      SHIFZ R20,4,5,173777,R,175777
03                      ;THIS IS A R SHIFT TEST OF NOT BIT 4 TO NOT BIT 5
04                  ;ASR20:
05 01621 105240         MOVOR   0,1     ;AC0 SHD=173777 COMING INTO TEST
06 01622 110225         COMZR   0,2,SNR ;AC2 SHD=COM OF 175777
07 01623 063077         HALT
08 01624 150000         COM     2,2     ;AC2 SHD NOW=AC1
09 01625 132000         ADC     1,2     ;THE ADDITION OF COM SHD=-1
10 01626 150004         COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
11 01627 063077         HALT            ;BIT 4 R TO BIT 5 FAILED
12                      ;AC0=173777 ORIGINAL TO 175777 IN AC1 AC2 WAS COM OF AC1
13                      ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
14                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU4 INTO NOT SUM5
15 01630 121000         MOV     1,0     ;SET UP NEXT TEST
16
17                      SHIFZ R21,5,6,175777,R,176777
18                      ;THIS IS A R SHIFT TEST OF NOT BIT 5 TO NOT BIT 6
19                  ;ASR21:
20 01631 105240         MOVOR   0,1     ;AC0 SHD=175777 COMING INTO TEST
21 01632 110225         COMZR   0,2,SNR ;AC2 SHD=COM OF 176777
22 01633 063077         HALT
23 01634 150000         COM     2,2     ;AC2 SHD NOW=AC1
24 01635 132000         ADC     1,2     ;THE ADDITION OF COM SHD=-1
25 01636 150004         COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
26 01637 063077         HALT            ;BIT 5 R TO BIT 6 FAILED
27                      ;AC0=175777 ORIGINAL TO 176777 IN AC1 AC2 WAS COM OF AC1
28                      ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
29                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU5 INTO NOT SUM6
30 01640 121000         MOV     1,0     ;SET UP NEXT TEST
31
32                      SHIFZ R22,6,7,176777,R,177377
33                      ;THIS IS A R SHIFT TEST OF NOT BIT 6 TO NOT BIT 7
34                  ;ASR22:
35 01641 105240         MOVOR   0,1     ;AC0 SHD=176777 COMING INTO TEST
36 01642 110225         COMZR   0,2,SNR ;AC2 SHD=COM OF 177377
37 01643 063077         HALT
38 01644 150000         COM     2,2     ;AC2 SHD NOW=AC1
39 01645 132000         ADC     1,2     ;THE ADDITION OF COM SHD=-1
40 01646 150004         COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
41 01647 063077         HALT            ;BIT 6 R TO BIT 7 FAILED
42                      ;AC0=176777 ORIGINAL TO 177377 IN AC1 AC2 WAS COM OF AC1
43                      ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
44                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU6 INTO NOT SUM7
45 01650 121000         MOV     1,0     ;SET UP NEXT TEST
46
47                      SHIFZ R23,7,8,177377,R,177577
48                      ;THIS IS A R SHIFT TEST OF NOT BIT 7 TO NOT BIT 8
49                  ;ASR23:
50 01651 105240         MOVOR   0,1     ;AC0 SHD=177377 COMING INTO TEST
51 01652 110225         COMZR   0,2,SNR ;AC2 SHD=COM OF 177577
52 01653 063077         HALT
53 01654 150000         COM     2,2     ;AC2 SHD NOW=AC1
54 01655 132000         ADC     1,2     ;THE ADDITION OF COM SHD=-1
55 01656 150004         COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
56 01657 063077         HALT            ;BIT 7 R TO BIT 8 FAILED
57                      ;AC0=177377 ORIGINAL TO 177577 IN AC1 AC2 WAS COM OF AC1
58                      ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
59                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU7 INTO NOT SUM8
60 01660 121000         MOV     1,0     ;SET UP NEXT TEST
```

```
 0104 .MAIN
01
02                          SHIFZ R24,8,9,177577,R,177677
03                          ;THIS IS A R SHIFT TEST OF NOT BIT 8 TO NOT BIT 9
04                    ;ASR24:
05 01661 105240             MOVOR   0,1       ;AC0 SHD=177577 COMING INTO TEST
06 01662 110225             COMZR   0,2,SNR   ;AC2 SHD=COM OF 177677
07 01663 063077             HALT
08 01664 150000             COM     2,2       ;AC2 SHD NOW=AC1
09 01665 132000             ADC     1,2       ;THE ADDITION OF COM SHD=-1
10 01666 150004             COM     2,2,SZR   ;AND RESULT SHD=0 ALL SHIFTS ON
11 01667 063077             HALT              ;BIT 8 R TO BIT 9 FAILED
12                          ;AC0=177577 ORIGINAL TO 177677 IN AC1 AC2 WAS COM OF AC1
13                          ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
14                          ;WAS PREVIOUSLY VERIFIED SEE NOT ALU8 INTO NOT SUM9
15 01670 121000             MOV     1,0       ;SET UP NEXT TEST
16
17                          SHIFZ R25,9,10,177677,R,177737
18                          ;THIS IS A R SHIFT TEST OF NOT BIT 9 TO NOT BIT 10
19                    ;ASR25:
20 01671 105240             MOVOR   0,1       ;AC0 SHD=177677 COMING INTO TEST
21 01672 110225             COMZR   0,2,SNR   ;AC2 SHD=COM OF 177737
22 01673 063077             HALT
23 01674 150000             COM     2,2       ;AC2 SHD NOW=AC1
24 01675 132000             ADC     1,2       ;THE ADDITION OF COM SHD=-1
25 01676 150004             COM     2,2,SZR   ;AND RESULT SHD=0 ALL SHIFTS ON
26 01677 063077             HALT              ;BIT 9 R TO BIT 10 FAILED
27                          ;AC0=177677 ORIGINAL TO 177737 IN AC1 AC2 WAS COM OF AC1
28                          ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
29                          ;WAS PREVIOUSLY VERIFIED SEE NOT ALU9 INTO NOT SUM10
30 01700 121000             MOV     1,0       ;SET UP NEXT TEST
31
32                          SHIFZ R26,10,11,177737,R,177757
33                          ;THIS IS A R SHIFT TEST OF NOT BIT 10 TO NOT BIT 11
34                    ;ASR26:
35 01701 105240             MOVOR   0,1       ;AC0 SHD=177737 COMING INTO TEST
36 01702 110225             COMZR   0,2,SNR   ;AC2 SHD=COM OF 177757
37 01703 063077             HALT
38 01704 150000             COM     2,2       ;AC2 SHD NOW=AC1
39 01705 132000             ADC     1,2       ;THE ADDITION OF COM SHD=-1
40 01706 150004             COM     2,2,SZR   ;AND RESULT SHD=0 ALL SHIFTS ON
41 01707 063077             HALT              ;BIT 10 R TO BIT 11 FAILED
42                          ;AC0=177737 ORIGINAL TO 177757 IN AC1 AC2 WAS COM OF AC1
43                          ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
44                          ;WAS PREVIOUSLY VERIFIED SEE NOT ALU10 INTO NOT SUM11
45 01710 121000             MOV     1,0       ;SET UP NEXT TEST
46
47                          SHIFZ R27,11,12,177757,R,177767
48                          ;THIS IS A R SHIFT TEST OF NOT BIT 11 TO NOT BIT 12
49                    ;ASR27:
50 01711 105240             MOVOR   0,1       ;AC0 SHD=177757 COMING INTO TEST
51 01712 110225             COMZR   0,2,SNR   ;AC2 SHD=COM OF 177767
52 01713 063077             HALT
53 01714 150000             COM     2,2       ;AC2 SHD NOW=AC1
54 01715 132000             ADC     1,2       ;THE ADDITION OF COM SHD=-1
55 01716 150004             COM     2,2,SZR   ;AND RESULT SHD=0 ALL SHIFTS ON
56 01717 063077             HALT              ;BIT 11 R TO BIT 12 FAILED
57                          ;AC0=177757 ORIGINAL TO 177767 IN AC1 AC2 WAS COM OF AC1
58                          ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
59                          ;WAS PREVIOUSLY VERIFIED SEE NOT ALU11 INTO NOT SUM12
60 01720 121000             MOV     1,0       ;SET UP NEXT TEST
```

```
0105 .MAIN
01
02                      SHIFZ R28,12,13,177767,R,177773
03                      ;THIS IS A R SHIFT TEST OF NOT BIT 12 TO NOT BIT 13
04                  ;ASR28:
05 01721 105240         MOVOR   0,1     ;AC0 SHD=177767 COMING INTO TEST
06 01722 110225         COMZR   0,2,SNR ;AC2 SHD=COM OF 177773
07 01723 063077         HALT
08 01724 150000         COM     2,2     ;AC2 SHD NOW=AC1
09 01725 132000         ADC     1,2     ;THE ADDITION OF COM SHD=-1
10 01726 150004         COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
11 01727 063077         HALT            ;BIT 12 R TO BIT 13 FAILED
12                      ;AC0=177767 ORIGINAL TO 177773 IN AC1 AC2 WAS COM OF AC1
13                      ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
14                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU12 INTO NOT SUM13
15 01730 121000         MOV     1,0     ;SET UP NEXT TEST
16
17                      SHIFZ R29,13,14,177773,R,177775
18                      ;THIS IS A R SHIFT TEST OF NOT BIT 13 TO NOT BIT 14
19                  ;ASR29:
20 01731 105240         MOVOR   0,1     ;AC0 SHD=177773 COMING INTO TEST
21 01732 110225         COMZR   0,2,SNR ;AC2 SHD=COM OF 177775
22 01733 063077         HALT
23 01734 150000         COM     2,2     ;AC2 SHD NOW=AC1
24 01735 132000         ADC     1,2     ;THE ADDITION OF COM SHD=-1
25 01736 150004         COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
26 01737 063077         HALT            ;BIT 13 R TO BIT 14 FAILED
27                      ;AC0=177773 ORIGINAL TO 177775 IN AC1 AC2 WAS COM OF AC1
28                      ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
29                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU13 INTO NOT SUM14
30 01740 121000         MOV     1,0     ;SET UP NEXT TEST
31
32                      SHIFZ R30,14,15,177775,R,177776
33                      ;THIS IS A R SHIFT TEST OF NOT BIT 14 TO NOT BIT 15
34                  ;ASR30:
35 01741 105240         MOVOR   0,1     ;AC0 SHD=177775 COMING INTO TEST
36 01742 110225         COMZR   0,2,SNR ;AC2 SHD=COM OF 177776
37 01743 063077         HALT
38 01744 150000         COM     2,2     ;AC2 SHD NOW=AC1
39 01745 132000         ADC     1,2     ;THE ADDITION OF COM SHD=-1
40 01746 150004         COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
41 01747 063077         HALT            ;BIT 14 R TO BIT 15 FAILED
42                      ;AC0=177775 ORIGINAL TO 177776 IN AC1 AC2 WAS COM OF AC1
43                      ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
44                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU14 INTO NOT SUM15
45 01750 121000         MOV     1,0     ;SET UP NEXT TEST
46
47 01751 105240 ASR31:  MOVOR   0,1     ;TEST 177776 TO -1
48 01752 130004         COM     1,2,SZR ;ALSO RETEST ABOVE SEQ
49 01753 063077         HALT            ;AN R16 TO R30 MAY HAVE LOST
50 01754 101002         MOV     0,0,SZC
51 01755 063077         HALT            ;CRY SHD=0 FROM LAST MOVOR
52                  ;SETUP SERIES OF LEFT SHIFT TESTS SET AC0=177776
53 01756 102000         ADC     0,0     ;AC0=-1
54 01757 100140         COMOL   0,0     ;SHD NOW=+1
55 01760 100000         COM     0,0
56 01761 104224         COMZR   0,1,SZR
57 01762 063077         HALT            ;LEFT SHIFT SETUP FAILED
58 01763 125003         MOV     1,1,SNC
59 01764 063077         HALT            ;LEFT SHIFT SETUP FAILED
60                  ;LEFT SHIFT SINGLE 0 BIT TESTS.
```

```
 0106 .MAIN
 01
 02                             SHIFZ L16,15,14,177776,L,177775
 03                             ;THIS IS A L SHIFT TEST OF NOT BIT 15 TO NOT BIT 14
 04                     ;ASL16:
 05 01765 105140                MOVOL   0,1     ;AC0 SHD=177776 COMING INTO TEST
 06 01766 110125                COMZL   0,2,SNR ;AC2 SHD=COM OF 177775
 07 01767 063077                HALT
 08 01770 150000                COM     2,2     ;AC2 SHD NOW=AC1
 09 01771 132000                ADC     1,2     ;THE ADDITION OF COM SHD=-1
 10 01772 150004                COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
 11 01773 063077                HALT            ;BIT 15 L TO BIT 14 FAILED
 12                             ;AC0=177776 ORIGINAL TO 177775 IN AC1 AC2 WAS COM OF AC1
 13                             ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
 14                             ;WAS PREVIOUSLY VERIFIED SEE NOT ALU15 INTO NOT SUM14
 15 01774 121000                MOV     1,0     ;SET UP NEXT TEST
 16
 17                             SHIFZ L17,14,13,177775,L,177773
 18                             ;THIS IS A L SHIFT TEST OF NOT BIT 14 TO NOT BIT 13
 19                     ;ASL17:
 20 01775 105140                MOVOL   0,1     ;AC0 SHD=177775 COMING INTO TEST
 21 01776 110125                COMZL   0,2,SNR ;AC2 SHD=COM OF 177773
 22 01777 063077                HALT
 23 02000 150000                COM     2,2     ;AC2 SHD NOW=AC1
 24 02001 132000                ADC     1,2     ;THE ADDITION OF COM SHD=-1
 25 02002 150004                COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
 26 02003 063077                HALT            ;BIT 14 L TO BIT 13 FAILED
 27                             ;AC0=177775 ORIGINAL TO 177773 IN AC1 AC2 WAS COM OF AC1
 28                             ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
 29                             ;WAS PREVIOUSLY VERIFIED SEE NOT ALU14 INTO NOT SUM13
 30 02004 121000                MOV     1,0     ;SET UP NEXT TEST
 31
 32                             SHIFZ L18,13,12,177773,L,177767
 33                             ;THIS IS A L SHIFT TEST OF NOT BIT 13 TO NOT BIT 12
 34                     ;ASL18:
 35 02005 105140                MOVOL   0,1     ;AC0 SHD=177773 COMING INTO TEST
 36 02006 110125                COMZL   0,2,SNR ;AC2 SHD=COM OF 177767
 37 02007 063077                HALT
 38 02010 150000                COM     2,2     ;AC2 SHD NOW=AC1
 39 02011 132000                ADC     1,2     ;THE ADDITION OF COM SHD=-1
 40 02012 150004                COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
 41 02013 063077                HALT            ;BIT 13 L TO BIT 12 FAILED
 42                             ;AC0=177773 ORIGINAL TO 177767 IN AC1 AC2 WAS COM OF AC1
 43                             ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
 44                             ;WAS PREVIOUSLY VERIFIED SEE NOT ALU13 INTO NOT SUM12
 45 02014 121000                MOV     1,0     ;SET UP NEXT TEST
 46
 47                             SHIFZ L19,12,11,177767,L,177757
 48                             ;THIS IS A L SHIFT TEST OF NOT BIT 12 TO NOT BIT 11
 49                     ;ASL19:
 50 02015 105140                MOVOL   0,1     ;AC0 SHD=177767 COMING INTO TEST
 51 02016 110125                COMZL   0,2,SNR ;AC2 SHD=COM OF 177757
 52 02017 063077                HALT
 53 02020 150000                COM     2,2     ;AC2 SHD NOW=AC1
 54 02021 132000                ADC     1,2     ;THE ADDITION OF COM SHD=-1
 55 02022 150004                COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
 56 02023 063077                HALT            ;BIT 12 L TO BIT 11 FAILED
 57                             ;AC0=177767 ORIGINAL TO 177757 IN AC1 AC2 WAS COM OF AC1
 58                             ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
 59                             ;WAS PREVIOUSLY VERIFIED SEE NOT ALU12 INTO NOT SUM11
 60 02024 121000                MOV     1,0     ;SET UP NEXT TEST
```

```
 0107 .MAIN
01
02                              SHIFZ L20,11,10,177757,L,177737
03                              ;THIS IS A L SHIFT TEST OF NOT BIT 11 TO NOT BIT 10
04                      ;ASL20:
05 02025 105140                 MOVOL   0,1     ;AC0 SHD=177757 COMING INTO TEST
06 02026 110125                 COMZL   0,2,SNR ;AC2 SHD=COM OF 177737
07 02027 063077                 HALT
08 02030 150000                 COM     2,2     ;AC2 SHD NOW=AC1
09 02031 132000                 ADC     1,2     ;THE ADDITION OF COM SHD=-1
10 02032 150004                 COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
11 02033 063077                 HALT            ;BIT 11 L TO BIT 10 FAILED
12                              ;AC0=177757 ORIGINAL TO 177737 IN AC1 AC2 WAS COM OF AC1
13                              ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
14                              ;WAS PREVIOUSLY VERIFIED SEE NOT ALU11 INTO NOT SUM10
15 02034 121000                 MOV     1,0     ;SET UP NEXT TEST
16
17                              SHIFZ L21,10,09,177737,L,177677
18                              ;THIS IS A L SHIFT TEST OF NOT BIT 10 TO NOT BIT 09
19                      ;ASL21:
20 02035 105140                 MOVOL   0,1     ;AC0 SHD=177737 COMING INTO TEST
21 02036 110125                 COMZL   0,2,SNR ;AC2 SHD=COM OF 177677
22 02037 063077                 HALT
23 02040 150000                 COM     2,2     ;AC2 SHD NOW=AC1
24 02041 132000                 ADC     1,2     ;THE ADDITION OF COM SHD=-1
25 02042 150004                 COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
26 02043 063077                 HALT            ;BIT 10 L TO BIT 09 FAILED
27                              ;AC0=177737 ORIGINAL TO 177677 IN AC1 AC2 WAS COM OF AC1
28                              ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
29                              ;WAS PREVIOUSLY VERIFIED SEE NOT ALU10 INTO NOT SUM09
30 02044 121000                 MOV     1,0     ;SET UP NEXT TEST
31
32                              SHIFZ L22,09,08,077677,L,177577
33                              ;THIS IS A L SHIFT TEST OF NOT BIT 09 TO NOT BIT 08
34                      ;ASL22:
35 02045 105140                 MOVOL   0,1     ;AC0 SHD=077677 COMING INTO TEST
36 02046 110125                 COMZL   0,2,SNR ;AC2 SHD=COM OF 177577
37 02047 063077                 HALT
38 02050 150000                 COM     2,2     ;AC2 SHD NOW=AC1
39 02051 132000                 ADC     1,2     ;THE ADDITION OF COM SHD=-1
40 02052 150004                 COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
41 02053 063077                 HALT            ;BIT 09 L TO BIT 08 FAILED
42                              ;AC0=077677 ORIGINAL TO 177577 IN AC1 AC2 WAS COM OF AC1
43                              ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
44                              ;WAS PREVIOUSLY VERIFIED SEE NOT ALU09 INTO NOT SUM08
45 02054 121000                 MOV     1,0     ;SET UP NEXT TEST
46
47                              SHIFZ L23,08,07,177577,L,177377
48                              ;THIS IS A L SHIFT TEST OF NOT BIT 08 TO NOT BIT 07
49                      ;ASL23:
50 02055 105140                 MOVOL   0,1     ;AC0 SHD=177577 COMING INTO TEST
51 02056 110125                 COMZL   0,2,SNR ;AC2 SHD=COM OF 177377
52 02057 063077                 HALT
53 02060 150000                 COM     2,2     ;AC2 SHD NOW=AC1
54 02061 132000                 ADC     1,2     ;THE ADDITION OF COM SHD=-1
55 02062 150004                 COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
56 02063 063077                 HALT            ;BIT 08 L TO BIT 07 FAILED
57                              ;AC0=177577 ORIGINAL TO 177377 IN AC1 AC2 WAS COM OF AC1
58                              ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
59                              ;WAS PREVIOUSLY VERIFIED SEE NOT ALU08 INTO NOT SUM07
60 02064 121000                 MOV     1,0     ;SET UP NEXT TEST
```

```
 0108 .MAIN
01
02                          SHIFZ L24,07,06,177377,L,176777
03                          ;THIS IS A L SHIFT TEST OF NOT BIT 07 TO NOT BIT 06
04                  ;ASL24:
05 02065 105140             MOVOL   0,1     ;AC0 SHD=177377 COMING INTO TEST
06 02066 110125             COMZL   0,2,SNR ;AC2 SHD=COM OF 176777
07 02067 063077             HALT
08 02070 150000             COM     2,2     ;AC2 SHD NOW=AC1
09 02071 132000             ADC     1,2     ;THE ADDITION OF COM SHD=-1
10 02072 150004             COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
11 02073 063077             HALT            ;BIT 07 L TO BIT 06 FAILED
12                          ;AC0=177377 ORIGINAL TO 176777 IN AC1 AC2 WAS COM OF AC1
13                          ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
14                          ;WAS PREVIOUSLY VERIFIED SEE NOT ALU07 INTO NOT SUM06
15 02074 121000             MOV     1,0     ;SET UP NEXT TEST
16
17                          SHIFZ L25,06,05,176777,L,175777
18                          ;THIS IS A L SHIFT TEST OF NOT BIT 06 TO NOT BIT 05
19                  ;ASL25:
20 02075 105140             MOVOL   0,1     ;AC0 SHD=176777 COMING INTO TEST
21 02076 110125             COMZL   0,2,SNR ;AC2 SHD=COM OF 175777
22 02077 063077             HALT
23 02100 150000             COM     2,2     ;AC2 SHD NOW=AC1
24 02101 132000             ADC     1,2     ;THE ADDITION OF COM SHD=-1
25 02102 150004             COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
26 02103 063077             HALT            ;BIT 06 L TO BIT 05 FAILED
27                          ;AC0=176777 ORIGINAL TO 175777 IN AC1 AC2 WAS COM OF AC1
28                          ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
29                          ;WAS PREVIOUSLY VERIFIED SEE NOT ALU06 INTO NOT SUM05
30 02104 121000             MOV     1,0     ;SET UP NEXT TEST
31
32                          SHIFZ L26,05,04,175777,L,173777
33                          ;THIS IS A L SHIFT TEST OF NOT BIT 05 TO NOT BIT 04
34                  ;ASL26:
35 02105 105140             MOVOL   0,1     ;AC0 SHD=175777 COMING INTO TEST
36 02106 110125             COMZL   0,2,SNR ;AC2 SHD=COM OF 173777
37 02107 063077             HALT
38 02110 150000             COM     2,2     ;AC2 SHD NOW=AC1
39 02111 132000             ADC     1,2     ;THE ADDITION OF COM SHD=-1
40 02112 150004             COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
41 02113 063077             HALT            ;BIT 05 L TO BIT 04 FAILED
42                          ;AC0=175777 ORIGINAL TO 173777 IN AC1 AC2 WAS COM OF AC1
43                          ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
44                          ;WAS PREVIOUSLY VERIFIED SEE NOT ALU05 INTO NOT SUM04
45 02114 121000             MOV     1,0     ;SET UP NEXT TEST
46
47                          SHIFZ L27,04,03,173777,L,167777
48                          ;THIS IS A L SHIFT TEST OF NOT BIT 04 TO NOT BIT 03
49                  ;ASL27:
50 02115 105140             MOVOL   0,1     ;AC0 SHD=173777 COMING INTO TEST
51 02116 110125             COMZL   0,2,SNR ;AC2 SHD=COM OF 167777
52 02117 063077             HALT
53 02120 150000             COM     2,2     ;AC2 SHD NOW=AC1
54 02121 132000             ADC     1,2     ;THE ADDITION OF COM SHD=-1
55 02122 150004             COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
56 02123 063077             HALT            ;BIT 04 L TO BIT 03 FAILED
57                          ;AC0=173777 ORIGINAL TO 167777 IN AC1 AC2 WAS COM OF AC1
58                          ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
59                          ;WAS PREVIOUSLY VERIFIED SEE NOT ALU04 INTO NOT SUM03
60 02124 121000             MOV     1,0     ;SET UP NEXT TEST
```

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 0109 .MAIN
01
02                      SHIFZ L28,03,02,167777,L,157777
03                      ;THIS IS A L SHIFT TEST OF NOT BIT 03 TO NOT BIT 02
04                  ;ASL28:
05 02125 105140         MOVOL   0,1     ;AC0 SHD=167777 COMING INTO TEST
06 02126 110125         COMZL   0,2,SNR ;AC2 SHD=COM OF 157777
07 02127 063077         HALT
08 02130 150000         COM     2,2     ;AC2 SHD NOW=AC1
09 02131 132000         ADC     1,2     ;THE ADDITION OF COM SHD=-1
10 02132 150004         COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
11 02133 063077         HALT            ;BIT 03 L TO BIT 02 FAILED
12                      ;AC0=167777 ORIGINAL TO 157777 IN AC1 AC2 WAS COM OF AC1
13                      ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
14                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU03 INTO NOT SUM02
15 02134 121000         MOV     1,0     ;SET UP NEXT TEST
16
17                      SHIFZ L29,02,01,157777,L,137777
18                      ;THIS IS A L SHIFT TEST OF NOT BIT 02 TO NOT BIT 01
19                  ;ASL29:
20 02135 105140         MOVOL   0,1     ;AC0 SHD=157777 COMING INTO TEST
21 02136 110125         COMZL   0,2,SNR ;AC2 SHD=COM OF 137777
22 02137 063077         HALT
23 02140 150000         COM     2,2     ;AC2 SHD NOW=AC1
24 02141 132000         ADC     1,2     ;THE ADDITION OF COM SHD=-1
25 02142 150004         COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
26 02143 063077         HALT            ;BIT 02 L TO BIT 01 FAILED
27                      ;AC0=157777 ORIGINAL TO 137777 IN AC1 AC2 WAS COM OF AC1
28                      ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
29                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU02 INTO NOT SUM01
30 02144 121000         MOV     1,0     ;SET UP NEXT TEST
31
32                      SHIFZ L30,01,00,137777,L,077777
33                      ;THIS IS A L SHIFT TEST OF NOT BIT 01 TO NOT BIT 00
34                  ;ASL30:
35 02145 105140         MOVOL   0,1     ;AC0 SHD=137777 COMING INTO TEST
36 02146 110125         COMZL   0,2,SNR ;AC2 SHD=COM OF 077777
37 02147 063077         HALT
38 02150 150000         COM     2,2     ;AC2 SHD NOW=AC1
39 02151 132000         ADC     1,2     ;THE ADDITION OF COM SHD=-1
40 02152 150004         COM     2,2,SZR ;AND RESULT SHD=0 ALL SHIFTS ON
41 02153 063077         HALT            ;BIT 01 L TO BIT 00 FAILED
42                      ;AC0=137777 ORIGINAL TO 077777 IN AC1 AC2 WAS COM OF AC1
43                      ;PROBALITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
44                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU01 INTO NOT SUM00
45 02154 121000         MOV     1,0     ;SET UP NEXT TEST
46
47                  ;IF AC0 DOES NOT=077777 HERE SOME L16 TO L30 FAILED
48
49
50 02155 105140 ASL31:  MOVOL   0,1     ;SHD RESULT IN AC1=-1
51 02156 130004         COM     1,2,SZR ;TEST FOR AC2 RESULT =0
52 02157 063077         HALT            ;COULD HAVE FAILED L16 TO L30
53 02160 151002         MOV     2,2,SZC ;CRY SHD=0 FROM BIT 0
54 02161 063077         HALT            ;BIT 0 TO CRY FAILED
```

```
!0110 .MAIN
01                ;SINGLE BIT ADD WITHOUT CARRY TESTS
02                ;DEFINE MACRO ENCOMPASSING SOURCE OR DEST=NON ZERO
03
04                        .MACRO ADDT1
05                        ;TEST ADD INSTRUCTION NO CARRY WHEN !1 IS NON ZERO
06                        ;!2 IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
07                        ;AC0=!3 COMING INTO THE TEST
08                ANC!7:  MOV     0,!4    ;SET UP !1 AC!4
09                        ADC     !5,!5
10                        COM     !5,!5   ;SET AC!5 !2=0
11                        ADD     !1,!2   ;PERFORM ADD WITH NO CARRIES
12                        MOV     2,3     ;THE !1 AC WAS NON ZERO
13                        ADC     0,3     ;AC3 SHD NOW=-1
14                        COM     3,3,SZR ;WITH COM =0
15                        HALT            ;ADD WITHOUT CARRY FAILED
16                        MOVZL   0,0     ;SET UP NEXT TEST
17                        ;AC2 SHD=!3 AS A RESULT OF ABOVE TEST
18                %
19
20                ;TEST ADD OF ALL 0'S TO GENERATE NO CARRIES
21  02162 102000  ANC00:  ADC     0,0
22  02163 100000          COM     0,0     ;SETS AC0=0
23  02164 103004          ADD     0,0,SZR ;RESULT OF ADD SHD STILL=0
24  02165 063077          HALT            ;ADD 0+0 GENERATED A CARRY
25  02166 101002          MOV     0,0,SZC ;ABOVE ADD SHD LVE CRY=0
26  02167 063077          HALT            ;INTO CRY SEE CARRY OUT
27                ;SET UP AC0 TO=+1 FOR FIRST TEST
28  02170 102000          ADC     0,0
29  02171 100145          COMOL   0,0,SNR
30  02172 063077          HALT            ;SETUP FAILED
31
32                        ADDT1 SRC,DEST,1,1,2,Z,01
33                        ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
34                        ;DEST IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
35                        ;AC0=1 COMING INTO THE TEST
36  02173 105000  ANC01:  MOV     0,1     ;SET UP SRC AC1
37  02174 152000          ADC     2,2
38  02175 150000          COM     2,2     ;SET AC2 DEST=0
39  02176 133000          ADD     1,2     ;PERFORM ADD WITH NO CARRIES
40  02177 155000          MOV     2,3     ;THE SRC AC WAS NON ZERO
41  02200 116000          ADC     0,3     ;AC3 SHD NOW=-1
42  02201 174004          COM     3,3,SZR ;WITH COM =0
43  02202 063077          HALT            ;ADD WITHOUT CARRY FAILED
44  02203 101120          MOVZL   0,0     ;SET UP NEXT TEST
45                        ;AC2 SHD=1 AS A RESULT OF ABOVE TEST
46
47                        ADDT1 SRC,DEST,2,1,2,Z,02
48                        ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
49                        ;DEST IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
50                        ;AC0=2 COMING INTO THE TEST
51  02204 105000  ANC02:  MOV     0,1     ;SET UP SRC AC1
52  02205 152000          ADC     2,2
53  02206 150000          COM     2,2     ;SET AC2 DEST=0
54  02207 133000          ADD     1,2     ;PERFORM ADD WITH NO CARRIES
55  02210 155000          MOV     2,3     ;THE SRC AC WAS NON ZERO
56  02211 116000          ADC     0,3     ;AC3 SHD NOW=-1
57  02212 174004          COM     3,3,SZR ;WITH COM =0
58  02213 063077          HALT            ;ADD WITHOUT CARRY FAILED
59  02214 101120          MOVZL   0,0     ;SET UP NEXT TEST
60                        ;AC2 SHD=2 AS A RESULT OF ABOVE TEST
```

```
 0111 .MAIN
01
02                          ADDT1 SRC,DEST,4,1,2,Z,03
03                          ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
04                          ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
05                          ;AC0=4 COMING INTO THE TEST
06 02215 105000 ANC03:      MOV     0,1     ;SET UP SRC AC1
07 02216 152000             ADC     2,2
08 02217 150000             COM     2,2     ;SET AC2 DEST=0
09 02220 133000             ADD     1,2     ;PERFORM ADD WITH NO CARRIES
10 02221 155000             MOV     2,3     ;THE SRC AC WAS NON ZERO
11 02222 116000             ADC     0,3     ;AC3 SHD NOW=-1
12 02223 174004             COM     3,3,SZR ;WITH COM =0
13 02224 063077             HALT            ;ADD WITHOUT CARRY FAILED
14 02225 101120             MOVZL   0,0     ;SET UP NEXT TEST
15                          ;AC2 SHD=4 AS A RESULT OF ABOVE TEST
16
17                          ADDT1 SRC,DEST,10,1,2,Z,04
18                          ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
19                          ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
20                          ;AC0=10 COMING INTO THE TEST
21 02226 105000 ANC04:      MOV     0,1     ;SET UP SRC AC1
22 02227 152000             ADC     2,2
23 02230 150000             COM     2,2     ;SET AC2 DEST=0
24 02231 133000             ADD     1,2     ;PERFORM ADD WITH NO CARRIES
25 02232 155000             MOV     2,3     ;THE SRC AC WAS NON ZERO
26 02233 116000             ADC     0,3     ;AC3 SHD NOW=-1
27 02234 174004             COM     3,3,SZR ;WITH COM =0
28 02235 063077             HALT            ;ADD WITHOUT CARRY FAILED
29 02236 101120             MOVZL   0,0     ;SET UP NEXT TEST
30                          ;AC2 SHD=10 AS A RESULT OF ABOVE TEST
31
32                          ADDT1 SRC,DEST,20,1,2,Z,05
33                          ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
34                          ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
35                          ;AC0=20 COMING INTO THE TEST
36 02237 105000 ANC05:      MOV     0,1     ;SET UP SRC AC1
37 02240 152000             ADC     2,2
38 02241 150000             COM     2,2     ;SET AC2 DEST=0
39 02242 133000             ADD     1,2     ;PERFORM ADD WITH NO CARRIES
40 02243 155000             MOV     2,3     ;THE SRC AC WAS NON ZERO
41 02244 116000             ADC     0,3     ;AC3 SHD NOW=-1
42 02245 174004             COM     3,3,SZR ;WITH COM =0
43 02246 063077             HALT            ;ADD WITHOUT CARRY FAILED
44 02247 101120             MOVZL   0,0     ;SET UP NEXT TEST
45                          ;AC2 SHD=20 AS A RESULT OF ABOVE TEST
46
47                          ADDT1 SRC,DEST,40,1,2,Z,06
48                          ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
49                          ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
50                          ;AC0=40 COMING INTO THE TEST
51 02250 105000 ANC06:      MOV     0,1     ;SET UP SRC AC1
52 02251 152000             ADC     2,2
53 02252 150000             COM     2,2     ;SET AC2 DEST=0
54 02253 133000             ADD     1,2     ;PERFORM ADD WITH NO CARRIES
55 02254 155000             MOV     2,3     ;THE SRC AC WAS NON ZERO
56 02255 116000             ADC     0,3     ;AC3 SHD NOW=-1
57 02256 174004             COM     3,3,SZR ;WITH COM =0
58 02257 063077             HALT            ;ADD WITHOUT CARRY FAILED
59 02260 101120             MOVZL   0,0     ;SET UP NEXT TEST
60                          ;AC2 SHD=40 AS A RESULT OF ABOVE TEST
```

```
 0112 .MAIN
01
02                          ADDT1 SRC,DEST,100,1,2,Z,07
03                          ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
04                          ;DEST IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
05                          ;AC0=100 COMING INTO THE TEST
06 02261 105000 ANC07:      MOV     0,1       ;SET UP SRC AC1
07 02262 152000             ADC     2,2
08 02263 150000             COM     2,2       ;SET AC2 DEST=0
09 02264 133000             ADD     1,2       ;PERFORM ADD WITH NO CARRIES
10 02265 155000             MOV     2,3       ;THE SRC AC WAS NON ZERO
11 02266 116000             ADC     0,3       ;AC3 SHD NOW=-1
12 02267 174004             COM     3,3,SZR   ;WITH COM =0
13 02270 063077             HALT              ;ADD WITHOUT CARRY FAILED
14 02271 101120             MOVZL   0,0       ;SET UP NEXT TEST
15                          ;AC2 SHD=100 AS A RESULT OF ABOVE TEST
16
17                          ADDT1 SRC,DEST,200,1,2,Z,08
18                          ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
19                          ;DEST IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
20                          ;AC0=200 COMING INTO THE TEST
21 02272 105000 ANC08:      MOV     0,1       ;SET UP SRC AC1
22 02273 152000             ADC     2,2
23 02274 150000             COM     2,2       ;SET AC2 DEST=0
24 02275 133000             ADD     1,2       ;PERFORM ADD WITH NO CARRIES
25 02276 155000             MOV     2,3       ;THE SRC AC WAS NON ZERO
26 02277 116000             ADC     0,3       ;AC3 SHD NOW=-1
27 02300 174004             COM     3,3,SZR   ;WITH COM =0
28 02301 063077             HALT              ;ADD WITHOUT CARRY FAILED
29 02302 101120             MOVZL   0,0       ;SET UP NEXT TEST
30                          ;AC2 SHD=200 AS A RESULT OF ABOVE TEST
31
32                          ADDT1 SRC,DEST,400,1,2,Z,09
33                          ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
34                          ;DEST IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
35                          ;AC0=400 COMING INTO THE TEST
36 02303 105000 ANC09:      MOV     0,1       ;SET UP SRC AC1
37 02304 152000             ADC     2,2
38 02305 150000             COM     2,2       ;SET AC2 DEST=0
39 02306 133000             ADD     1,2       ;PERFORM ADD WITH NO CARRIES
40 02307 155000             MOV     2,3       ;THE SRC AC WAS NON ZERO
41 02310 116000             ADC     0,3       ;AC3 SHD NOW=-1
42 02311 174004             COM     3,3,SZR   ;WITH COM =0
43 02312 063077             HALT              ;ADD WITHOUT CARRY FAILED
44 02313 101120             MOVZL   0,0       ;SET UP NEXT TEST
45                          ;AC2 SHD=400 AS A RESULT OF ABOVE TEST
46
47                          ADDT1 SRC,DEST,1000,1,2,Z,10
48                          ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
49                          ;DEST IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
50                          ;AC0=1000 COMING INTO THE TEST
51 02314 105000 ANC10:      MOV     0,1       ;SET UP SRC AC1
52 02315 152000             ADC     2,2
53 02316 150000             COM     2,2       ;SET AC2 DEST=0
54 02317 133000             ADD     1,2       ;PERFORM ADD WITH NO CARRIES
55 02320 155000             MOV     2,3       ;THE SRC AC WAS NON ZERO
56 02321 116000             ADC     0,3       ;AC3 SHD NOW=-1
57 02322 174004             COM     3,3,SZR   ;WITH COM =0
58 02323 063077             HALT              ;ADD WITHOUT CARRY FAILED
59 02324 101120             MOVZL   0,0       ;SET UP NEXT TEST
60                          ;AC2 SHD=1000 AS A RESULT OF ABOVE TEST
```

```
 0113 .MAIN
01
02                          ADDT1 SRC,DEST,2000,1,2,Z,11
03                          ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
04                          ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
05                          ;AC0=2000 COMING INTO THE TEST
06 02325 105000 ANC11:      MOV     0,1     ;SET UP SRC AC1
07 02326 152000             ADC     2,2
08 02327 150000             COM     2,2     ;SET AC2 DEST=0
09 02330 133000             ADD     1,2     ;PERFORM ADD WITH NO CARRIES
10 02331 155000             MOV     2,3     ;THE SRC AC WAS NON ZERO
11 02332 116000             ADC     0,3     ;AC3 SHD NOW=-1
12 02333 174004             COM     3,3,SZR ;WITH COM =0
13 02334 063077             HALT            ;ADD WITHOUT CARRY FAILED
14 02335 101120             MOVZL   0,0     ;SET UP NEXT TEST
15                          ;AC2 SHD=2000 AS A RESULT OF ABOVE TEST
16
17                          ADDT1 SRC,DEST,4000,1,2,Z,12
18                          ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
19                          ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
20                          ;AC0=4000 COMING INTO THE TEST
21 02336 105000 ANC12:      MOV     0,1     ;SET UP SRC AC1
22 02337 152000             ADC     2,2
23 02340 150000             COM     2,2     ;SET AC2 DEST=0
24 02341 133000             ADD     1,2     ;PERFORM ADD WITH NO CARRIES
25 02342 155000             MOV     2,3     ;THE SRC AC WAS NON ZERO
26 02343 116000             ADC     0,3     ;AC3 SHD NOW=-1
27 02344 174004             COM     3,3,SZR ;WITH COM =0
28 02345 063077             HALT            ;ADD WITHOUT CARRY FAILED
29 02346 101120             MOVZL   0,0     ;SET UP NEXT TEST
30                          ;AC2 SHD=4000 AS A RESULT OF ABOVE TEST
31
32                          ADDT1 SRC,DEST,10000,1,2,Z,13
33                          ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
34                          ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
35                          ;AC0=10000 COMING INTO THE TEST
36 02347 105000 ANC13:      MOV     0,1     ;SET UP SRC AC1
37 02350 152000             ADC     2,2
38 02351 150000             COM     2,2     ;SET AC2 DEST=0
39 02352 133000             ADD     1,2     ;PERFORM ADD WITH NO CARRIES
40 02353 155000             MOV     2,3     ;THE SRC AC WAS NON ZERO
41 02354 116000             ADC     0,3     ;AC3 SHD NOW=-1
42 02355 174004             COM     3,3,SZR ;WITH COM =0
43 02356 063077             HALT            ;ADD WITHOUT CARRY FAILED
44 02357 101120             MOVZL   0,0     ;SET UP NEXT TEST
45                          ;AC2 SHD=10000 AS A RESULT OF ABOVE TEST
46
47                          ADDT1 SRC,DEST,20000,1,2,Z,14
48                          ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
49                          ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
50                          ;AC0=20000 COMING INTO THE TEST
51 02360 105000 ANC14:      MOV     0,1     ;SET UP SRC AC1
52 02361 152000             ADC     2,2
53 02362 150000             COM     2,2     ;SET AC2 DEST=0
54 02363 133000             ADD     1,2     ;PERFORM ADD WITH NO CARRIES
55 02364 155000             MOV     2,3     ;THE SRC AC WAS NON ZERO
56 02365 116000             ADC     0,3     ;AC3 SHD NOW=-1
57 02366 174004             COM     3,3,SZR ;WITH COM =0
58 02367 063077             HALT            ;ADD WITHOUT CARRY FAILED
59 02370 101120             MOVZL   0,0     ;SET UP NEXT TEST
60                          ;AC2 SHD=20000 AS A RESULT OF ABOVE TEST
```

```
 0114 .MAIN
01
02                              ADDT1 SRC,DEST,40000,1,2,Z,15
03                              ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
04                              ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
05                              ;AC0=40000 COMING INTO THE TEST
06 02371 105000 ANC15:  MOV     0,1     ;SET UP SRC AC1
07 02372 152000         ADC     2,2
08 02373 150000         COM     2,2     ;SET AC2 DEST=0
09 02374 133000         ADD     1,2     ;PERFORM ADD WITH NO CARRIES
10 02375 155000         MOV     2,3     ;THE SRC AC WAS NON ZERO
11 02376 116000         ADC     0,3     ;AC3 SHD NOW=-1
12 02377 174004         COM     3,3,SZR ;WITH COM =0
13 02400 063077         HALT            ;ADD WITHOUT CARRY FAILED
14 02401 101120         MOVZL   0,0     ;SET UP NEXT TEST
15                              ;AC2 SHD=40000 AS A RESULT OF ABOVE TEST
16
17                              ADDT1 SRC,DEST,100000,1,2,Z,16
18                              ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
19                              ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
20                              ;AC0=100000 COMING INTO THE TEST
21 02402 105000 ANC16:  MOV     0,1     ;SET UP SRC AC1
22 02403 152000         ADC     2,2
23 02404 150000         COM     2,2     ;SET AC2 DEST=0
24 02405 133000         ADD     1,2     ;PERFORM ADD WITH NO CARRIES
25 02406 155000         MOV     2,3     ;THE SRC AC WAS NON ZERO
26 02407 116000         ADC     0,3     ;AC3 SHD NOW=-1
27 02410 174004         COM     3,3,SZR ;WITH COM =0
28 02411 063077         HALT            ;ADD WITHOUT CARRY FAILED
29 02412 101120         MOVZL   0,0     ;SET UP NEXT TEST
30                              ;AC2 SHD=100000 AS A RESULT OF ABOVE TEST
31
32
33                              ;RESET UP AC0 FOR DEST NOT = 0 ADD TEST
34
35 02413 102000         ADC     0,0
36 02414 100145         COMOL   0,0,SNR
37 02415 063077         HALT
```

```
10115 .MAIN
01
02                      ADDT1 DEST,SRC,1,2,1,Z,17
03                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
04                      ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
05                      ;AC0=1 COMING INTO THE TEST
06 02416 111000 ANC17:  MOV     0,2     ;SET UP DEST AC2
07 02417 126000         ADC     1,1
08 02420 124000         COM     1,1     ;SET AC1 SRC=0
09 02421 133000         ADD     1,2     ;PERFORM ADD WITH NO CARRIES
10 02422 155000         MOV     2,3     ;THE DEST AC WAS NON ZERO
11 02423 116000         ADC     0,3     ;AC3 SHD NOW=-1
12 02424 174004         COM     3,3,SZR ;WITH COM =0
13 02425 063077         HALT            ;ADD WITHOUT CARRY FAILED
14 02426 101120         MOVZL   0,0     ;SET UP NEXT TEST
15                      ;AC2 SHD=1 AS A RESULT OF ABOVE TEST
16
17                      ADDT1 DEST,SRC,2,2,1,Z,18
18                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
19                      ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
20                      ;AC0=2 COMING INTO THE TEST
21 02427 111000 ANC18:  MOV     0,2     ;SET UP DEST AC2
22 02430 126000         ADC     1,1
23 02431 124000         COM     1,1     ;SET AC1 SRC=0
24 02432 133000         ADD     1,2     ;PERFORM ADD WITH NO CARRIES
25 02433 155000         MOV     2,3     ;THE DEST AC WAS NON ZERO
26 02434 116000         ADC     0,3     ;AC3 SHD NOW=-1
27 02435 174004         COM     3,3,SZR ;WITH COM =0
28 02436 063077         HALT            ;ADD WITHOUT CARRY FAILED
29 02437 101120         MOVZL   0,0     ;SET UP NEXT TEST
30                      ;AC2 SHD=2 AS A RESULT OF ABOVE TEST
31
32                      ADDT1 DEST,SRC,4,2,1,Z,19
33                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
34                      ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
35                      ;AC0=4 COMING INTO THE TEST
36 02440 111000 ANC19:  MOV     0,2     ;SET UP DEST AC2
37 02441 126000         ADC     1,1
38 02442 124000         COM     1,1     ;SET AC1 SRC=0
39 02443 133000         ADD     1,2     ;PERFORM ADD WITH NO CARRIES
40 02444 155000         MOV     2,3     ;THE DEST AC WAS NON ZERO
41 02445 116000         ADC     0,3     ;AC3 SHD NOW=-1
42 02446 174004         COM     3,3,SZR ;WITH COM =0
43 02447 063077         HALT            ;ADD WITHOUT CARRY FAILED
44 02450 101120         MOVZL   0,0     ;SET UP NEXT TEST
45                      ;AC2 SHD=4 AS A RESULT OF ABOVE TEST
46
47                      ADDT1 DEST,SRC,10,2,1,Z,20
48                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
49                      ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
50                      ;AC0=10 COMING INTO THE TEST
51 02451 111000 ANC20:  MOV     0,2     ;SET UP DEST AC2
52 02452 126000         ADC     1,1
53 02453 124000         COM     1,1     ;SET AC1 SRC=0
54 02454 133000         ADD     1,2     ;PERFORM ADD WITH NO CARRIES
55 02455 155000         MOV     2,3     ;THE DEST AC WAS NON ZERO
56 02456 116000         ADC     0,3     ;AC3 SHD NOW=-1
57 02457 174004         COM     3,3,SZR ;WITH COM =0
58 02460 063077         HALT            ;ADD WITHOUT CARRY FAILED
59 02461 101120         MOVZL   0,0     ;SET UP NEXT TEST
60                      ;AC2 SHD=10 AS A RESULT OF ABOVE TEST
```

```
 0116 ,MAIN
01
02                          ADDT1 DEST,SRC,20;2,1,Z,21
03                          ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
04                          ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
05                          ;AC0=20 COMING INTO THE TEST
06 02462 111000 ANC21:      MOV     0,2       ;SET UP DEST AC2
07 02463 126000             ADC     1,1
08 02464 124000             COM     1,1       ;SET AC1 SRC=0
09 02465 133000             ADD     1,2       ;PERFORM ADD WITH NO CARRIES
10 02466 155000             MOV     2,3       ;THE DEST AC WAS NON ZERO
11 02467 116000             ADC     0,3       ;AC3 SHD NOW=-1
12 02470 174004             COM     3,3,SZR   ;WITH COM =0
13 02471 063077             HALT              ;ADD WITHOUT CARRY FAILED
14 02472 101120             MOVZL   0,0       ;SET UP NEXT TEST
15                          ;AC2 SHD=20 AS A RESULT OF ABOVE TEST
16
17                          ADDT1 DEST,SRC,40,2,1,Z,22
18                          ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
19                          ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
20                          ;AC0=40 COMING INTO THE TEST
21 02473 111000 ANC22:      MOV     0,2       ;SET UP DEST AC2
22 02474 126000             ADC     1,1
23 02475 124000             COM     1,1       ;SET AC1 SRC=0
24 02476 133000             ADD     1,2       ;PERFORM ADD WITH NO CARRIES
25 02477 155000             MOV     2,3       ;THE DEST AC WAS NON ZERO
26 02500 116000             ADC     0,3       ;AC3 SHD NOW=-1
27 02501 174004             COM     3,3,SZR   ;WITH COM =0
28 02502 063077             HALT              ;ADD WITHOUT CARRY FAILED
29 02503 101120             MOVZL   0,0       ;SET UP NEXT TEST
30                          ;AC2 SHD=40 AS A RESULT OF ABOVE TEST
31
32                          ADDT1 DEST,SRC,100,2,1,Z,23
33                          ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
34                          ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
35                          ;AC0=100 COMING INTO THE TEST
36 02504 111000 ANC23:      MOV     0,2       ;SET UP DEST AC2
37 02505 126000             ADC     1,1
38 02506 124000             COM     1,1       ;SET AC1 SRC=0
39 02507 133000             ADD     1,2       ;PERFORM ADD WITH NO CARRIES
40 02510 155000             MOV     2,3       ;THE DEST AC WAS NON ZERO
41 02511 116000             ADC     0,3       ;AC3 SHD NOW=-1
42 02512 174004             COM     3,3,SZR   ;WITH COM =0
43 02513 063077             HALT              ;ADD WITHOUT CARRY FAILED
44 02514 101120             MOVZL   0,0       ;SET UP NEXT TEST
45                          ;AC2 SHD=100 AS A RESULT OF ABOVE TEST
46
47                          ADDT1 DEST,SRC,200,2,1,Z,24
48                          ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
49                          ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
50                          ;AC0=200 COMING INTO THE TEST
51 02515 111000 ANC24:      MOV     0,2       ;SET UP DEST AC2
52 02516 126000             ADC     1,1
53 02517 124000             COM     1,1       ;SET AC1 SRC=0
54 02520 133000             ADD     1,2       ;PERFORM ADD WITH NO CARRIES
55 02521 155000             MOV     2,3       ;THE DEST AC WAS NON ZERO
56 02522 116000             ADC     0,3       ;AC3 SHD NOW=-1
57 02523 174004             COM     3,3,SZR   ;WITH COM =0
58 02524 063077             HALT              ;ADD WITHOUT CARRY FAILED
59 02525 101120             MOVZL   0,0       ;SET UP NEXT TEST
60                          ;AC2 SHD=200 AS A RESULT OF ABOVE TEST
```

```
 0117 .MAIN
01
02                          ADDT1 DEST,SRC,400,2,1,Z,25
03                          ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
04                          ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
05                          ;AC0=400 COMING INTO THE TEST
06 02526 111000 ANC25:      MOV     0,2         ;SET UP DEST AC2
07 02527 126000             ADC     1,1
08 02530 124000             COM     1,1         ;SET AC1 SRC=0
09 02531 133000             ADD     1,2         ;PERFORM ADD WITH NO CARRIES
10 02532 155000             MOV     2,3         ;THE DEST AC WAS NON ZERO
11 02533 116000             ADC     0,3         ;AC3 SHD NOW=-1
12 02534 174004             COM     3,3,SZR     ;WITH COM =0
13 02535 063077             HALT                ;ADD WITHOUT CARRY FAILED
14 02536 101120             MOVZL   0,0         ;SET UP NEXT TEST
15                          ;AC2 SHD=400 AS A RESULT OF ABOVE TEST
16
17                          ADDT1 DEST,SRC,1000,2,1,Z,26
18                          ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
19                          ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
20                          ;AC0=1000 COMING INTO THE TEST
21 02537 111000 ANC26:      MOV     0,2         ;SET UP DEST AC2
22 02540 126000             ADC     1,1
23 02541 124000             COM     1,1         ;SET AC1 SRC=0
24 02542 133000             ADD     1,2         ;PERFORM ADD WITH NO CARRIES
25 02543 155000             MOV     2,3         ;THE DEST AC WAS NON ZERO
26 02544 116000             ADC     0,3         ;AC3 SHD NOW=-1
27 02545 174004             COM     3,3,SZR     ;WITH COM =0
28 02546 063077             HALT                ;ADD WITHOUT CARRY FAILED
29 02547 101120             MOVZL   0,0         ;SET UP NEXT TEST
30                          ;AC2 SHD=1000 AS A RESULT OF ABOVE TEST
31
32                          ADDT1 DEST,SRC,2000,2,1,Z,27
33                          ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
34                          ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
35                          ;AC0=2000 COMING INTO THE TEST
36 02550 111000 ANC27:      MOV     0,2         ;SET UP DEST AC2
37 02551 126000             ADC     1,1
38 02552 124000             COM     1,1         ;SET AC1 SRC=0
39 02553 133000             ADD     1,2         ;PERFORM ADD WITH NO CARRIES
40 02554 155000             MOV     2,3         ;THE DEST AC WAS NON ZERO
41 02555 116000             ADC     0,3         ;AC3 SHD NOW=-1
42 02556 174004             COM     3,3,SZR     ;WITH COM =0
43 02557 063077             HALT                ;ADD WITHOUT CARRY FAILED
44 02560 101120             MOVZL   0,0         ;SET UP NEXT TEST
45                          ;AC2 SHD=2000 AS A RESULT OF ABOVE TEST
46
47                          ADDT1 DEST,SRC,4000,2,1,Z,28
48                          ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
49                          ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
50                          ;AC0=4000 COMING INTO THE TEST
51 02561 111000 ANC28:      MOV     0,2         ;SET UP DEST AC2
52 02562 126000             ADC     1,1
53 02563 124000             COM     1,1         ;SET AC1 SRC=0
54 02564 133000             ADD     1,2         ;PERFORM ADD WITH NO CARRIES
55 02565 155000             MOV     2,3         ;THE DEST AC WAS NON ZERO
56 02566 116000             ADC     0,3         ;AC3 SHD NOW=-1
57 02567 174004             COM     3,3,SZR     ;WITH COM =0
58 02570 063077             HALT                ;ADD WITHOUT CARRY FAILED
59 02571 101120             MOVZL   0,0         ;SET UP NEXT TEST
60                          ;AC2 SHD=4000 AS A RESULT OF ABOVE TEST
```

```
 0118 .MAIN
01
02                          ADDT1 DEST,SRC,10000,2,1,Z,29
03                          ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
04                          ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
05                          ;AC0=10000 COMING INTO THE TEST
06 02572 111000 ANC29:      MOV     0,2     ;SET UP DEST AC2
07 02573 126000             ADC     1,1
08 02574 124000             COM     1,1     ;SET AC1 SRC=0
09 02575 133000             ADD     1,2     ;PERFORM ADD WITH NO CARRIES
10 02576 155000             MOV     2,3     ;THE DEST AC WAS NON ZERO
11 02577 116000             ADC     0,3     ;AC3 SHD NOW=-1
12 02600 174004             COM     3,3,SZR ;WITH COM =0
13 02601 063077             HALT            ;ADD WITHOUT CARRY FAILED
14 02602 101120             MOVZL   0,0     ;SET UP NEXT TEST
15                          ;AC2 SHD=10000 AS A RESULT OF ABOVE TEST
16
17                          ADDT1 DEST,SRC,20000,2,1,Z,30
18                          ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
19                          ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
20                          ;AC0=20000 COMING INTO THE TEST
21 02603 111000 ANC30:      MOV     0,2     ;SET UP DEST AC2
22 02604 126000             ADC     1,1
23 02605 124000             COM     1,1     ;SET AC1 SRC=0
24 02606 133000             ADD     1,2     ;PERFORM ADD WITH NO CARRIES
25 02607 155000             MOV     2,3     ;THE DEST AC WAS NON ZERO
26 02610 116000             ADC     0,3     ;AC3 SHD NOW=-1
27 02611 174004             COM     3,3,SZR ;WITH COM =0
28 02612 063077             HALT            ;ADD WITHOUT CARRY FAILED
29 02613 101120             MOVZL   0,0     ;SET UP NEXT TEST
30                          ;AC2 SHD=20000 AS A RESULT OF ABOVE TEST
31
32                          ADDT1 DEST,SRC,40000,2,1,Z,31
33                          ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
34                          ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
35                          ;AC0=40000 COMING INTO THE TEST
36 02614 111000 ANC31:      MOV     0,2     ;SET UP DEST AC2
37 02615 126000             ADC     1,1
38 02616 124000             COM     1,1     ;SET AC1 SRC=0
39 02617 133000             ADD     1,2     ;PERFORM ADD WITH NO CARRIES
40 02620 155000             MOV     2,3     ;THE DEST AC WAS NON ZERO
41 02621 116000             ADC     0,3     ;AC3 SHD NOW=-1
42 02622 174004             COM     3,3,SZR ;WITH COM =0
43 02623 063077             HALT            ;ADD WITHOUT CARRY FAILED
44 02624 101120             MOVZL   0,0     ;SET UP NEXT TEST
45                          ;AC2 SHD=40000 AS A RESULT OF ABOVE TEST
46
47                          ADDT1 DEST,SRC,100000,2,1,Z,32
48                          ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
49                          ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
50                          ;AC0=100000 COMING INTO THE TEST
51 02625 111000 ANC32:      MOV     0,2     ;SET UP DEST AC2
52 02626 126000             ADC     1,1
53 02627 124000             COM     1,1     ;SET AC1 SRC=0
54 02630 133000             ADD     1,2     ;PERFORM ADD WITH NO CARRIES
55 02631 155000             MOV     2,3     ;THE DEST AC WAS NON ZERO
56 02632 116000             ADC     0,3     ;AC3 SHD NOW=-1
57 02633 174004             COM     3,3,SZR ;WITH COM =0
58 02634 063077             HALT            ;ADD WITHOUT CARRY FAILED
59 02635 101120             MOVZL   0,0     ;SET UP NEXT TEST
60                          ;AC2 SHD=100000 AS A RESULT OF ABOVE TEST
```

```
 0119 .MAIN
01                ;SINGLE BIT CARRY TESTS DEFINE MACRO
02                ;CONSTANTS ARE SET UP BY ALREADY TESTED SHIFT
03                        .MACRO ADDT0
04                        ;TEST SINGLE BIT CARRY ADD BIT 12 TO ITSELF
05                        ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 13
06                        ;AND SUM BIT 12 TO GO TO 0 RESULT SHD=15
07
08                ;AC11:
09                        MOV     0,1       ;AC0=14 COMING INTO TEST
10                        ADD     1,1       ;USE IT TO SET UP AC1+AC1
11                        MOVZL   0,2       ;AC2 SHD NOW=RESULT OF ADD
12                        ADC     1,2       ;AC2 SHD NOW=-1
13                        COM     2,2,SZR   ;NOT 0 IS BIT 12 CARRY FAILED
14                        HALT              ;BIT 12+12 FAILED ADD SEE ALU13
15                                          ;AND ALU12
16                        MOVZL   0,0       ;SET UP NEXT TEST
17                %
18
19
20                ;SET UP BIT 15 FOR ADD TESTS
21
22 02636 102000           ADC     0,0
23 02637 100145           COMOL   0,0,SNR
24 02640 063077           HALT              ;AC0 SHD=+1
25
26
27
28
29
30
31
32                        ADDT0 00,15,14,1,2
33                        ;TEST SINGLE BIT CARRY ADD BIT 15 TO ITSELF
34                        ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 14
35                        ;AND SUM BIT 15 TO GO TO 0 RESULT SHD=2
36
37                ;AC00:
38 02641 105000           MOV     0,1       ;AC0=1 COMING INTO TEST
39 02642 127000           ADD     1,1       ;USE IT TO SET UP AC1+AC1
40 02643 111120           MOVZL   0,2       ;AC2 SHD NOW=RESULT OF ADD
41 02644 132000           ADC     1,2       ;AC2 SHD NOW=-1
42 02645 150004           COM     2,2,SZR   ;NOT 0 IS BIT 15 CARRY FAILED
43 02646 063077           HALT              ;BIT 15+15 FAILED ADD SEE ALU14
44                                          ;AND ALU15
45 02647 101120           MOVZL   0,0       ;SET UP NEXT TEST
46
47                        ADDT0 01,14,13,2,4
48                        ;TEST SINGLE BIT CARRY ADD BIT 14 TO ITSELF
49                        ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 13
50                        ;AND SUM BIT 14 TO GO TO 0 RESULT SHD=4
51
52                ;AC01:
53 02650 105000           MOV     0,1       ;AC0=2 COMING INTO TEST
54 02651 127000           ADD     1,1       ;USE IT TO SET UP AC1+AC1
55 02652 111120           MOVZL   0,2       ;AC2 SHD NOW=RESULT OF ADD
56 02653 132000           ADC     1,2       ;AC2 SHD NOW=-1
57 02654 150004           COM     2,2,SZR   ;NOT 0 IS BIT 14 CARRY FAILED
58 02655 063077           HALT              ;BIT 14+14 FAILED ADD SEE ALU13
59                                          ;AND ALU14
60 02656 101120           MOVZL   0,0       ;SET UP NEXT TEST
```

```
 0120 .MAIN
 01
 02                     ADDT0 02,13,12,4,10
 03                     ;TEST SINGLE BIT CARRY ADD BIT 13 TO ITSELF
 04                     ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 12
 05                     ;AND SUM BIT 13 TO GO TO 0 RESULT SHD=10
 06
 07                ;AC02:
 08 02657 105000         MOV     0,1     ;AC0=4 COMING INTO TEST
 09 02660 127000         ADD     1,1     ;USE IT TO SET UP AC1+AC1
 10 02661 111120         MOVZL   0,2     ;AC2 SHD NOW=RESULT OF ADD
 11 02662 132000         ADC     1,2     ;AC2 SHD NOW=-1
 12 02663 150004         COM     2,2,SZR ;NOT 0 IS BIT 13 CARRY FAILED
 13 02664 063077         HALT            ;BIT 13+13 FAILED ADD SEE ALU12
 14                                      ;AND ALU13
 15 02665 101120         MOVZL   0,0     ;SET UP NEXT TEST
 16
 17                     ADDT0 03,12,11,10,20
 18                     ;TEST SINGLE BIT CARRY ADD BIT 12 TO ITSELF
 19                     ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 11
 20                     ;AND SUM BIT 12 TO GO TO 0 RESULT SHD=20
 21
 22                ;AC03:
 23 02666 105000         MOV     0,1     ;AC0=10 COMING INTO TEST
 24 02667 127000         ADD     1,1     ;USE IT TO SET UP AC1+AC1
 25 02670 111120         MOVZL   0,2     ;AC2 SHD NOW=RESULT OF ADD
 26 02671 132000         ADC     1,2     ;AC2 SHD NOW=-1
 27 02672 150004         COM     2,2,SZR ;NOT 0 IS BIT 12 CARRY FAILED
 28 02673 063077         HALT            ;BIT 12+12 FAILED ADD SEE ALU11
 29                                      ;AND ALU12
 30 02674 101120         MOVZL   0,0     ;SET UP NEXT TEST
 31
 32                     ADDT0 04,11,10,20,40
 33                     ;TEST SINGLE BIT CARRY ADD BIT 11 TO ITSELF
 34                     ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 10
 35                     ;AND SUM BIT 11 TO GO TO 0 RESULT SHD=40
 36
 37                ;AC04:
 38 02675 105000         MOV     0,1     ;AC0=20 COMING INTO TEST
 39 02676 127000         ADD     1,1     ;USE IT TO SET UP AC1+AC1
 40 02677 111120         MOVZL   0,2     ;AC2 SHD NOW=RESULT OF ADD
 41 02700 132000         ADC     1,2     ;AC2 SHD NOW=-1
 42 02701 150004         COM     2,2,SZR ;NOT 0 IS BIT 11 CARRY FAILED
 43 02702 063077         HALT            ;BIT 11+11 FAILED ADD SEE ALU10
 44                                      ;AND ALU11
 45 02703 101120         MOVZL   0,0     ;SET UP NEXT TEST
 46
 47                     ADDT0 05,10,9,40,100
 48                     ;TEST SINGLE BIT CARRY ADD BIT 10 TO ITSELF
 49                     ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 9
 50                     ;AND SUM BIT 10 TO GO TO 0 RESULT SHD=100
 51
 52                ;AC05:
 53 02704 105000         MOV     0,1     ;AC0=40 COMING INTO TEST
 54 02705 127000         ADD     1,1     ;USE IT TO SET UP AC1+AC1
 55 02706 111120         MOVZL   0,2     ;AC2 SHD NOW=RESULT OF ADD
 56 02707 132000         ADC     1,2     ;AC2 SHD NOW=-1
 57 02710 150004         COM     2,2,SZR ;NOT 0 IS BIT 10 CARRY FAILED
 58 02711 063077         HALT            ;BIT 10+10 FAILED ADD SEE ALU9
 59                                      ;AND ALU10
 60 02712 101120         MOVZL   0,0     ;SET UP NEXT TEST
```

```
 0121 .MAIN
01
02                          ADDT0 06,9,8,100,200
03                          ;TEST SINGLE BIT CARRY ADD BIT 9 TO ITSELF
04                          ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 8
05                          ;AND SUM BIT 9 TO GO TO 0 RESULT SHD=200
06
07                    ;AC06:
08 02713 105000             MOV     0,1       ;AC0=100 COMING INTO TEST
09 02714 127000             ADD     1,1       ;USE IT TO SET UP AC1+AC1
10 02715 111120             MOVZL   0,2       ;AC2 SHD NOW=RESULT OF ADD
11 02716 132000             ADC     1,2       ;AC2 SHD NOW=-1
12 02717 150004             COM     2,2,SZR   ;NOT 0 IS BIT 9 CARRY FAILED
13 02720 063077             HALT              ;BIT 9+9 FAILED ADD SEE ALU8
14                                            ;AND ALU9
15 02721 101120             MOVZL   0,0       ;SET UP NEXT TEST
16
17                          ADDT0 07,8,7,200,400
18                          ;TEST SINGLE BIT CARRY ADD BIT 8 TO ITSELF
19                          ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 7
20                          ;AND SUM BIT 8 TO GO TO 0 RESULT SHD=400
21
22                    ;AC07:
23 02722 105000             MOV     0,1       ;AC0=200 COMING INTO TEST
24 02723 127000             ADD     1,1       ;USE IT TO SET UP AC1+AC1
25 02724 111120             MOVZL   0,2       ;AC2 SHD NOW=RESULT OF ADD
26 02725 132000             ADC     1,2       ;AC2 SHD NOW=-1
27 02726 150004             COM     2,2,SZR   ;NOT 0 IS BIT 8 CARRY FAILED
28 02727 063077             HALT              ;BIT 8+8 FAILED ADD SEE ALU7
29                                            ;AND ALU8
30 02730 101120             MOVZL   0,0       ;SET UP NEXT TEST
31
32                          ADDT0 08,7,6,400,1000
33                          ;TEST SINGLE BIT CARRY ADD BIT 7 TO ITSELF
34                          ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 6
35                          ;AND SUM BIT 7 TO GO TO 0 RESULT SHD=1000
36
37                    ;AC08:
38 02731 105000             MOV     0,1       ;AC0=400 COMING INTO TEST
39 02732 127000             ADD     1,1       ;USE IT TO SET UP AC1+AC1
40 02733 111120             MOVZL   0,2       ;AC2 SHD NOW=RESULT OF ADD
41 02734 132000             ADC     1,2       ;AC2 SHD NOW=-1
42 02735 150004             COM     2,2,SZR   ;NOT 0 IS BIT 7 CARRY FAILED
43 02736 063077             HALT              ;BIT 7+7 FAILED ADD SEE ALU6
44                                            ;AND ALU7
45 02737 101120             MOVZL   0,0       ;SET UP NEXT TEST
46
47                          ADDT0 09,6,5,1000,2000
48                          ;TEST SINGLE BIT CARRY ADD BIT 6 TO ITSELF
49                          ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 5
50                          ;AND SUM BIT 6 TO GO TO 0 RESULT SHD=2000
51
52                    ;AC09:
53 02740 105000             MOV     0,1       ;AC0=1000 COMING INTO TEST
54 02741 127000             ADD     1,1       ;USE IT TO SET UP AC1+AC1
55 02742 111120             MOVZL   0,2       ;AC2 SHD NOW=RESULT OF ADD
56 02743 132000             ADC     1,2       ;AC2 SHD NOW=-1
57 02744 150004             COM     2,2,SZR   ;NOT 0 IS BIT 6 CARRY FAILED
58 02745 063077             HALT              ;BIT 6+6 FAILED ADD SEE ALU5
59                                            ;AND ALU6
60 02746 101120             MOVZL   0,0       ;SET UP NEXT TEST
```

```
 0122 .MAIN
01
02                          ADDT0 10,5,4,2000,4000
03                          ;TEST SINGLE BIT CARRY ADD BIT 5 TO ITSELF
04                          ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 4
05                          ;AND SUM BIT 5 TO GO TO 0 RESULT SHD=4000
06
07                    ;AC10:
08 02747 105000             MOV     0,1       ;AC0=2000 COMING INTO TEST
09 02750 127000             ADD     1,1       ;USE IT TO SET UP AC1+AC1
10 02751 111120             MOVZL   0,2       ;AC2 SHD NOW=RESULT OF ADD
11 02752 132000             ADC     1,2       ;AC2 SHD NOW=-1
12 02753 150004             COM     2,2,SZR   ;NOT 0 IS BIT 5 CARRY FAILED
13 02754 063077             HALT              ;BIT 5+5 FAILED ADD SEE ALU4
14                                            ;AND ALU5
15 02755 101120             MOVZL   0,0       ;SET UP NEXT TEST
16
17                          ADDT0 11,4,3,4000,10000
18                          ;TEST SINGLE BIT CARRY ADD BIT 4 TO ITSELF
19                          ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 3
20                          ;AND SUM BIT 4 TO GO TO 0 RESULT SHD=10000
21
22                    ;AC11:
23 02756 105000             MOV     0,1       ;AC0=4000 COMING INTO TEST
24 02757 127000             ADD     1,1       ;USE IT TO SET UP AC1+AC1
25 02760 111120             MOVZL   0,2       ;AC2 SHD NOW=RESULT OF ADD
26 02761 132000             ADC     1,2       ;AC2 SHD NOW=-1
27 02762 150004             COM     2,2,SZR   ;NOT 0 IS BIT 4 CARRY FAILED
28 02763 063077             HALT              ;BIT 4+4 FAILED ADD SEE ALU3
29                                            ;AND ALU4
30 02764 101120             MOVZL   0,0       ;SET UP NEXT TEST
31
32                          ADDT0 12,3,2,10000,20000
33                          ;TEST SINGLE BIT CARRY ADD BIT 3 TO ITSELF
34                          ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 2
35                          ;AND SUM BIT 3 TO GO TO 0 RESULT SHD=20000
36
37                    ;AC12:
38 02765 105000             MOV     0,1       ;AC0=10000 COMING INTO TEST
39 02766 127000             ADD     1,1       ;USE IT TO SET UP AC1+AC1
40 02767 111120             MOVZL   0,2       ;AC2 SHD NOW=RESULT OF ADD
41 02770 132000             ADC     1,2       ;AC2 SHD NOW=-1
42 02771 150004             COM     2,2,SZR   ;NOT 0 IS BIT 3 CARRY FAILED
43 02772 063077             HALT              ;BIT 3+3 FAILED ADD SEE ALU2
44                                            ;AND ALU3
45 02773 101120             MOVZL   0,0       ;SET UP NEXT TEST
46
47                          ADDT0 13,2,1,20000,40000
48                          ;TEST SINGLE BIT CARRY ADD BIT 2 TO ITSELF
49                          ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 1
50                          ;AND SUM BIT 2 TO GO TO 0 RESULT SHD=40000
51
52                    ;AC13:
53 02774 105000             MOV     0,1       ;AC0=20000 COMING INTO TEST
54 02775 127000             ADD     1,1       ;USE IT TO SET UP AC1+AC1
55 02776 111120             MOVZL   0,2       ;AC2 SHD NOW=RESULT OF ADD
56 02777 132000             ADC     1,2       ;AC2 SHD NOW=-1
57 03000 150004             COM     2,2,SZR   ;NOT 0 IS BIT 2 CARRY FAILED
58 03001 063077             HALT              ;BIT 2+2 FAILED ADD SEE ALU1
59                                            ;AND ALU2
60 03002 101120             MOVZL   0,0       ;SET UP NEXT TEST
```

```
 0123 .MAIN
01
02                      ADDT0 14,1,0,40000,100000
03                      ;TEST SINGLE BIT CARRY ADD BIT 1 TO ITSELF
04                      ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 0
05                      ;AND SUM BIT 1 TO GO TO 0 RESULT SHD=100000
06
07                ;AC14:
08 03003 105000         MOV     0,1     ;AC0=40000 COMING INTO TEST
09 03004 127000         ADD     1,1     ;USE IT TO SET UP AC1+AC1
10 03005 111120         MOVZL   0,2     ;AC2 SHD NOW=RESULT OF ADD
11 03006 132000         ADC     1,2     ;AC2 SHD NOW=-1
12 03007 150004         COM     2,2,SZR ;NOT 0 IS BIT 1 CARRY FAILED
13 03010 063077         HALT            ;BIT 1+1 FAILED ADD SEE ALU0
14                                      ;AND ALU1
15 03011 101120         MOVZL   0,0     ;SET UP NEXT TEST
16
17                ;TEST ADD BIT 0 TO BIT0 AC0=100000
18                ;SEE THAT CRYOUT GETS TO CRY
19
20 03012 105020 AC15:   MOVZ    0,1
21 03013 127004         ADD     1,1,SZR ;ADD BIT 0 TO 0 FAILED
22 03014 063077         HALT
23 03015 125003         MOV     1,1,SNC ;BIT 0+BIT 0 DID NOT CRY OUT
24 03016 063077         HALT
```

```
10124 .MAIN
31
32                ;TEST AND INSTRUCTION AND VARIATIONS
33                ;FIRST TEST GROSS CASE AND -1 TO -1
34
35 03017 102000 AND00:  ADC     0,0       ;SET AC0=-1
36 03020 103405        AND     0,0,SNR   ;FIRST USE OF "AND"
37 03021 063077        HALT              ;RESULT SHD STILL BE NON 0
38                     ;IF RESULT=0 "AND" LOOKS LIKE "SUB" OR "INC"
39                     ;SEE NOT IR16 OR NOT IR15 AT ALU ROM
10 03022 104004        COM     0,1,SZR
11 03023 063077        HALT              ;RESULT OF PREV AND NOT=-1
12                     ;IF RESULT IN AC0=-2 "AND" LOOKS LIKE "ADD"
13                     ;SEE NOT IR7 ALU ROM
14
15                ;TEST AND 0'S TO 0'S RESULT SHD REMAIN=0
16
17 03024 102000 AND01: ADC     0,0
18 03025 100000        COM     0,0       ;AC=0
19 03026 103404        AND     0,0,SZR   ;RESULT OF AND SHD=0
20 03027 063077        HALT
21 03030 101004        MOV     0,0,SZR   ;RECHECK RESULT
22 03031 063077        HALT
23                     ;SEE RESULT IN AC0 TO DETERMINE ALU BIT(S) IN ERR
24
25                ;AND -1 TO 0 WITH 0 AS DISTINATION
26                ;RESULT SHOULD AGAIN=0'S
27
28 03032 102000 AND02: ADC     0,0
29 03033 104000        COM     0,1
30 03034 107404        AND     0,1,SZR   ;DEST REG AC1=0'S
31 03035 063077        HALT              ;RESULT OF ABOVE AND NOT=0
32 03036 125024        MOV     1,1,SZR   ;RECHECK RESULT
33 03037 063077        HALT
34                     ;EXAMINE AC1 TO DETERMINE ALU BIT(S) IN ERROR
35
36                ;TEST AND OF 0 TO -1 WITH -1 ORIGINAL DESTINATION
37
38 03040 102000 AND03: ADC     0,0
39 03041 104000        COM     0,1
40 03042 123404        AND     1,0,SZR   ;DEST=-1  SRC=0  RES SHD=0
41 03043 063077        HALT
42 03044 101004        MOV     0,0,SZR   ;RECHECK RESULT
43 03045 063077        HALT
44                     ;EXAMINE AC0 TO DETERMINE ALU BIT(S) IN ERROR
```

```
10125 .MAIN
01                ;DEFINE BIT TEST MACRO FOR AND INSTRUCTION
02                        .MACRO ANDTS
03                        ;THE NEXT SERIES IS AN TST OF BIT 12
04                        ;AC0=13 COMING INTO THE TEST
05                ;AND11:
06                        MOV     0,1     ;AC0=13
07                        AND     0,1,SNR ;BIT 12 SHD REMAIN=1
08                        HALT
09                        MOV     1,2
10                        ADC     0,2
11                        COM     2,2,SZR ;TEST FOR EXTRA BITS
12                        HALT            ;MORE THAN 1 BIT IN AND OF 13
13                        ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=13
14
15                ;NOW TEST AND OF COMPLIMENTS
16                ;SOURCE WILL=13 DEST WILL=COMPLIMENT
17                ;AN11A:
18                        COM     0,1
19                        AND     0,1,SZR
20                        HALT            ;AND OF 13 AND ITS COM FAILED
21                        ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
22
23                ;TEST AND OF COMPLIMENTS WITH DEST=13 AND SRC=COM
24                ;AN11B:
25                        MOV     0,1
26                        COM     1,2
27                        AND     2,1,SZR
28                        HALT            ;AND OF 13 AND ITS COM FAILED
29                        ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
30                        MOVZL   0,0     ;SET UP NEXT TEST
31                %
32
33
34                        ;SET UP AC0=1 FOR FIRST AND TEST
35 03046 102000           ADC     0,0
36 03047 100145           COMCL   0,0,SNR
37 03050 063077           HALT
```

```
10126 .MAIN
01
02                      ANDTS 04,15,1
03                      ;THE NEXT SERIES IS AN TST OF BIT 15
04                      ;AC0=1 COMING INTO THE TEST
05                  ;AND04:
06 03051 105000         MOV     0,1     ;AC0=1
07 03052 107405         AND     0,1,SNR ;BIT 15 SHD REMAIN=1
08 03053 063077         HALT
09 03054 131000         MOV     1,2
10 03055 112000         ADC     0,2
11 03056 150004         COM     2,2,SZR ;TEST FOR EXTRA BITS
12 03057 063077         HALT            ;MORE THAN 1 BIT IN AND OF 1
13                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=1
14
15                  ;NOW TEST AND OF COMPLIMENTS
16                  ;SOURCE WILL=1 DEST WILL=COMPLIMENT
17                  ;AN04A:
18 03060 104000         COM     0,1
19 03061 107404         AND     0,1,SZR
20 03062 063077         HALT            ;AND OF 1 AND ITS COM FAILED
21                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
22
23                  ;TEST AND OF COMPLIMENTS WITH DEST=1 AND SRC=COM
24                  ;AN04B:
25 03063 105000         MOV     0,1
26 03064 130000         COM     1,2
27 03065 147404         AND     2,1,SZR
28 03066 063077         HALT            ;AND OF 1 AND ITS COM FAILED
29                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
30 03067 101120         MOVZL   0,0     ;SET UP NEXT TEST
31
32                      ANDTS 05,14,2
33                      ;THE NEXT SERIES IS AN TST OF BIT 14
34                      ;AC0=2 COMING INTO THE TEST
35                  ;AND05:
36 03070 105000         MOV     0,1     ;AC0=2
37 03071 107405         AND     0,1,SNR ;BIT 14 SHD REMAIN=1
38 03072 063077         HALT
39 03073 131000         MOV     1,2
40 03074 112000         ADC     0,2
41 03075 150004         COM     2,2,SZR ;TEST FOR EXTRA BITS
42 03076 063077         HALT            ;MORE THAN 1 BIT IN AND OF 2
43                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=2
44
45                  ;NOW TEST AND OF COMPLIMENTS
46                  ;SOURCE WILL=2 DEST WILL=COMPLIMENT
47                  ;AN05A:
48 03077 104000         COM     0,1
49 03100 107404         AND     0,1,SZR
50 03101 063077         HALT            ;AND OF 2 AND ITS COM FAILED
51                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
52
53                  ;TEST AND OF COMPLIMENTS WITH DEST=2 AND SRC=COM
54                  ;AN05B:
55 03102 105000         MOV     0,1
56 03103 130000         COM     1,2
57 03104 147404         AND     2,1,SZR
58 03105 063077         HALT            ;AND OF 2 AND ITS COM FAILED
59                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
60 03106 101120         MOVZL   0,0     ;SET UP NEXT TEST
```

```
 0127 .MAIN
01
02                          ANDTS 06,13,4
03                          ;THE NEXT SERIES IS AN TST OF BIT 13
04                          ;AC0=4 COMING INTO THE TEST
05                    ;AND06:
06 03107 105000             MOV     0,1       ;AC0=4
07 03110 107405             AND     0,1,SNR ;BIT 13 SHD REMAIN=1
08 03111 063077             HALT
09 03112 131000             MOV     1,2
10 03113 112000             ADC     0,2
11 03114 150004             COM     2,2,SZR ;TEST FOR EXTRA BITS
12 03115 063077             HALT              ;MORE THAN 1 BIT IN AND OF 4
13                          ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=4
14
15                    ;NOW TEST AND OF COMPLIMENTS
16                    ;SOURCE WILL=4 DEST WILL=COMPLIMENT
17                    ;AN06A:
18 03116 104000             COM     0,1
19 03117 107404             AND     0,1,SZR
20 03120 063077             HALT              ;AND OF 4 AND ITS COM FAILED
21                          ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
22
23                    ;TEST AND OF COMPLIMENTS WITH DEST=4 AND SRC=COM
24                    ;AN06B:
25 03121 105000             MOV     0,1
26 03122 130000             COM     1,2
27 03123 147404             AND     2,1,SZR
28 03124 063077             HALT              ;AND OF 4 AND ITS COM FAILED
29                          ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
30 03125 101120             MOVZL   0,0       ;SET UP NEXT TEST
31
32                          ANDTS 07,12,10
33                          ;THE NEXT SERIES IS AN TST OF BIT 12
34                          ;AC0=10 COMING INTO THE TEST
35                    ;AND07:
36 03126 105000             MOV     0,1       ;AC0=10
37 03127 107405             AND     0,1,SNR ;BIT 12 SHD REMAIN=1
38 03130 063077             HALT
39 03131 131000             MOV     1,2
40 03132 112000             ADC     0,2
41 03133 150004             COM     2,2,SZR ;TEST FOR EXTRA BITS
42 03134 063077             HALT              ;MORE THAN 1 BIT IN AND OF 10
43                          ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=10
44
45                    ;NOW TEST AND OF COMPLIMENTS
46                    ;SOURCE WILL=10 DEST WILL=COMPLIMENT
47                    ;AN07A:
48 03135 104000             COM     0,1
49 03136 107404             AND     0,1,SZR
50 03137 063077             HALT              ;AND OF 10 AND ITS COM FAILED
51                          ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
52
53                    ;TEST AND OF COMPLIMENTS WITH DEST=10 AND SRC=COM
54                    ;AN07B:
55 03140 105000             MOV     0,1
56 03141 130000             COM     1,2
57 03142 147404             AND     2,1,SZR
58 03143 063077             HALT              ;AND OF 10 AND ITS COM FAILED
59                          ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
60 03144 101120             MOVZL   0,0       ;SET UP NEXT TEST
```

```
 0128 .MAIN
01
02                      ANDTS 08,11,20
03                      ;THE NEXT SERIES IS AN TST OF BIT 11
04                      ;AC0=20 COMING INTO THE TEST
05                  ;AND08:
06 03145 105000         MOV     0,1     ;AC0=20
07 03146 107405         AND     0,1,SNR ;BIT 11 SHD REMAIN=1
08 03147 063077         HALT
09 03150 131000         MOV     1,2
10 03151 112000         ADC     0,2
11 03152 150004         COM     2,2,SZR ;TEST FOR EXTRA BITS
12 03153 063077         HALT            ;MORE THAN 1 BIT IN AND OF 20
13                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=20
14
15                  ;NOW TEST AND OF COMPLIMENTS
16                  ;SOURCE WILL=20 DEST WILL=COMPLIMENT
17                  ;AN08A:
18 03154 104000         COM     0,1
19 03155 107404         AND     0,1,SZR
20 03156 063077         HALT            ;AND OF 20 AND ITS COM FAILED
21                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
22
23                  ;TEST AND OF COMPLIMENTS WITH DEST=20 AND SRC=COM
24                  ;AN08B:
25 03157 105000         MOV     0,1
26 03160 130000         COM     1,2
27 03161 147404         AND     2,1,SZR
28 03162 063077         HALT            ;AND OF 20 AND ITS COM FAILED
29                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
30 03163 101120         MOVZL   0,0     ;SET UP NEXT TEST
31
32                      ANDTS 09,10,40
33                      ;THE NEXT SERIES IS AN TST OF BIT 10
34                      ;AC0=40 COMING INTO THE TEST
35                  ;AND09:
36 03164 105000         MOV     0,1     ;AC0=40
37 03165 107405         AND     0,1,SNR ;BIT 10 SHD REMAIN=1
38 03166 063077         HALT
39 03167 131000         MOV     1,2
40 03170 112000         ADC     0,2
41 03171 150004         COM     2,2,SZR ;TEST FOR EXTRA BITS
42 03172 063077         HALT            ;MORE THAN 1 BIT IN AND OF 40
43                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=40
44
45                  ;NOW TEST AND OF COMPLIMENTS
46                  ;SOURCE WILL=40 DEST WILL=COMPLIMENT
47                  ;AN09A:
48 03173 104000         COM     0,1
49 03174 107404         AND     0,1,SZR
50 03175 063077         HALT            ;AND OF 40 AND ITS COM FAILED
51                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
52
53                  ;TEST AND OF COMPLIMENTS WITH DEST=40 AND SRC=COM
54                  ;AN09B:
55 03176 105000         MOV     0,1
56 03177 130000         COM     1,2
57 03200 147404         AND     2,1,SZR
58 03201 063077         HALT            ;AND OF 40 AND ITS COM FAILED
59                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
60 03202 101120         MOVZL   0,0     ;SET UP NEXT TEST
```

```
 0129 .MAIN
01
02                          ANDTS 10,9,100
03                          ;THE NEXT SERIES IS AN TST OF BIT 9
04                          ;AC0=100 COMING INTO THE TEST
05                  ;AND10:
06 03203 105000             MOV     0,1       ;AC0=100
07 03204 107405             AND     0,1,SNR   ;BIT 9 SHD REMAIN=1
08 03205 063077             HALT
09 03206 131000             MOV     1,2
10 03207 112000             ADC     0,2
11 03210 150004             COM     2,2,SZR   ;TEST FOR EXTRA BITS
12 03211 063077             HALT              ;MORE THAN 1 BIT IN AND OF 100
13                          ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=100
14
15                  ;NOW TEST AND OF COMPLIMENTS
16                  ;SOURCE WILL=100 DEST WILL=COMPLIMENT
17                  ;AN10A:
18 03212 104000             COM     0,1
19 03213 107404             AND     0,1,SZR
20 03214 063077             HALT              ;AND OF 100 AND ITS COM FAILED
21                          ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
22
23                  ;TEST AND OF COMPLIMENTS WITH DEST=100 AND SRC=COM
24                  ;AN10B:
25 03215 105000             MOV     0,1
26 03216 130000             COM     1,2
27 03217 147404             AND     2,1,SZR
28 03220 063077             HALT              ;AND OF 100 AND ITS COM FAILED
29                          ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
30 03221 101120             MOVZL   0,0       ;SET UP NEXT TEST
31
32                          ANDTS 11,8,200
33                          ;THE NEXT SERIES IS AN TST OF BIT 8
34                          ;AC0=200 COMING INTO THE TEST
35                  ;AND11:
36 03222 105000             MOV     0,1       ;AC0=200
37 03223 107405             AND     0,1,SNR   ;BIT 8 SHD REMAIN=1
38 03224 063077             HALT
39 03225 131000             MOV     1,2
40 03226 112000             ADC     0,2
41 03227 150004             COM     2,2,SZR   ;TEST FOR EXTRA BITS
42 03230 063077             HALT              ;MORE THAN 1 BIT IN AND OF 200
43                          ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=200
44
45                  ;NOW TEST AND OF COMPLIMENTS
46                  ;SOURCE WILL=200 DEST WILL=COMPLIMENT
47                  ;AN11A:
48 03231 104000             COM     0,1
49 03232 107404             AND     0,1,SZR
50 03233 063077             HALT              ;AND OF 200 AND ITS COM FAILED
51                          ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
52
53                  ;TEST AND OF COMPLIMENTS WITH DEST=200 AND SRC=COM
54                  ;AN11B:
55 03234 105000             MOV     0,1
56 03235 130000             COM     1,2
57 03236 147404             AND     2,1,SZR
58 03237 063077             HALT              ;AND OF 200 AND ITS COM FAILED
59                          ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
60 03240 101120             MOVZL   0,0       ;SET UP NEXT TEST
```

```
 0130 .MAIN
01
02                          ANDTS 12,7,400
03                          ;THE NEXT SERIES IS AN TST OF BIT 7
04                          ;AC0=400 COMING INTO THE TEST
05                    ;AND12:
06 03241 105000             MOV     0,1       ;AC0=400
07 03242 107405             AND     0,1,SNR   ;BIT 7 SHD REMAIN=1
08 03243 063077             HALT
09 03244 131000             MOV     1,2
10 03245 112000             ADC     0,2
11 03246 150004             COM     2,2,SZR   ;TEST FOR EXTRA BITS
12 03247 063077             HALT              ;MORE THAN 1 BIT IN AND OF 400
13                          ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=400
14
15                    ;NOW TEST AND OF COMPLIMENTS
16                    ;SOURCE WILL=400 DEST WILL=COMPLIMENT
17                    ;AN12A:
18 03250 104000             COM     0,1
19 03251 107404             AND     0,1,SZR
20 03252 063077             HALT              ;AND OF 400 AND ITS COM FAILED
21                          ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
22
23                    ;TEST AND OF COMPLIMENTS WITH DEST=400 AND SRC=COM
24                    ;AN12B:
25 03253 105000             MOV     0,1
26 03254 130000             COM     1,2
27 03255 147404             AND     2,1,SZR
28 03256 063077             HALT              ;AND OF 400 AND ITS COM FAILED
29                          ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
30 03257 101120             MOVZL   0,0       ;SET UP NEXT TEST
31
32                          ANDTS 13,6,1000
33                          ;THE NEXT SERIES IS AN TST OF BIT 6
34                          ;AC0=1000 COMING INTO THE TEST
35                    ;AND13:
36 03260 105000             MOV     0,1       ;AC0=1000
37 03261 107405             AND     0,1,SNR   ;BIT 6 SHD REMAIN=1
38 03262 063077             HALT
39 03263 131000             MOV     1,2
40 03264 112000             ADC     0,2
41 03265 150004             COM     2,2,SZR   ;TEST FOR EXTRA BITS
42 03266 063077             HALT              ;MORE THAN 1 BIT IN AND OF 1000
43                          ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=1000
44
45                    ;NOW TEST AND OF COMPLIMENTS
46                    ;SOURCE WILL=1000 DEST WILL=COMPLIMENT
47                    ;AN13A:
48 03267 104000             COM     0,1
49 03270 107404             AND     0,1,SZR
50 03271 063077             HALT              ;AND OF 1000 AND ITS COM FAILED
51                          ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
52
53                    ;TEST AND OF COMPLIMENTS WITH DEST=1000 AND SRC=COM
54                    ;AN13B:
55 03272 105000             MOV     0,1
56 03273 130000             COM     1,2
57 03274 147404             AND     2,1,SZR
58 03275 063077             HALT              ;AND OF 1000 AND ITS COM FAILED
59                          ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
60 03276 101120             MOVZL   0,0       ;SET UP NEXT TEST
```

```
 0131 .MAIN
01
02                          ANDTS 14,5,2000
03                          ;THE NEXT SERIES IS AN TST OF BIT 5
04                          ;AC0=2000 COMING INTO THE TEST
05                    ;AND14:
06 03277 105000             MOV     0,1       ;AC0=2000
07 03300 107405             AND     0,1,SNR   ;BIT 5 SHD REMAIN=1
08 03301 063077             HALT
09 03302 131000             MOV     1,2
10 03303 112000             ADC     0,2
11 03304 150004             COM     2,2,SZR   ;TEST FOR EXTRA BITS
12 03305 063077             HALT              ;MORE THAN 1 BIT IN AND OF 2000
13                          ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=2000
14
15                    ;NOW TEST AND OF COMPLIMENTS
16                    ;SOURCE WILL=2000 DEST WILL=COMPLIMENT
17                    ;AN14A:
18 03306 104000             COM     0,1
19 03307 107404             AND     0,1,SZR
20 03310 063077             HALT              ;AND OF 2000 AND ITS COM FAILED
21                          ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
22
23                    ;TEST AND OF COMPLIMENTS WITH DEST=2000 AND SRC=COM
24                    ;AN14B:
25 03311 105000             MOV     0,1
26 03312 130000             COM     1,2
27 03313 147404             AND     2,1,SZR
28 03314 063077             HALT              ;AND OF 2000 AND ITS COM FAILED
29                          ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
30 03315 101120             MOVZL   0,0       ;SET UP NEXT TEST
31
32                          ANDTS 15,4,4000
33                          ;THE NEXT SERIES IS AN TST OF BIT 4
34                          ;AC0=4000 COMING INTO THE TEST
35                    ;AND15:
36 03316 105000             MOV     0,1       ;AC0=4000
37 03317 107405             AND     0,1,SNR   ;BIT 4 SHD REMAIN=1
38 03320 063077             HALT
39 03321 131000             MOV     1,2
40 03322 112000             ADC     0,2
41 03323 150004             COM     2,2,SZR   ;TEST FOR EXTRA BITS
42 03324 063077             HALT              ;MORE THAN 1 BIT IN AND OF 4000
43                          ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=4000
44
45                    ;NOW TEST AND OF COMPLIMENTS
46                    ;SOURCE WILL=4000 DEST WILL=COMPLIMENT
47                    ;AN15A:
48 03325 104000             COM     0,1
49 03326 107404             AND     0,1,SZR
50 03327 063077             HALT              ;AND OF 4000 AND ITS COM FAILED
51                          ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
52
53                    ;TEST AND OF COMPLIMENTS WITH DEST=4000 AND SRC=COM
54                    ;AN15B:
55 03330 105000             MOV     0,1
56 03331 130000             COM     1,2
57 03332 147404             AND     2,1,SZR
58 03333 063077             HALT              ;AND OF 4000 AND ITS COM FAILED
59                          ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
60 03334 101120             MOVZL   0,0       ;SET UP NEXT TEST
```

```
 0132 .MAIN
01
02                      ANDTS 16,3,10000
03                      ;THE NEXT SERIES IS AN TST OF BIT 3
04                      ;AC0=10000 COMING INTO THE TEST
05                  ;AND16:
06 03335 105000         MOV     0,1     ;AC0=10000
07 03336 107405         AND     0,1,SNR ;BIT 3 SHD REMAIN=1
08 03337 063077         HALT
09 03340 131000         MOV     1,2
10 03341 112000         ADC     0,2
11 03342 150004         COM     2,2,SZR ;TEST FOR EXTRA BITS
12 03343 063077         HALT            ;MORE THAN 1 BIT IN AND OF 10000
13                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=10000
14
15                  ;NOW TEST AND OF COMPLIMENTS
16                  ;SOURCE WILL=10000 DEST WILL=COMPLIMENT
17                  ;AN16A:
18 03344 104000         COM     0,1
19 03345 107404         AND     0,1,SZR
20 03346 063077         HALT            ;AND OF 10000 AND ITS COM FAILED
21                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
22
23                  ;TEST AND OF COMPLIMENTS WITH DEST=10000 AND SRC=COM
24                  ;AN16B:
25 03347 105000         MOV     0,1
26 03350 130000         COM     1,2
27 03351 147404         AND     2,1,SZR
28 03352 063077         HALT            ;AND OF 10000 AND ITS COM FAILED
29                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
30 03353 101120         MOVZL   0,0     ;SET UP NEXT TEST
31
32                      ANDTS 17,2,20000
33                      ;THE NEXT SERIES IS AN TST OF BIT 2
34                      ;AC0=20000 COMING INTO THE TEST
35                  ;AND17:
36 03354 105000         MOV     0,1     ;AC0=20000
37 03355 107405         AND     0,1,SNR ;BIT 2 SHD REMAIN=1
38 03356 063077         HALT
39 03357 131000         MOV     1,2
40 03360 112000         ADC     0,2
41 03361 150004         COM     2,2,SZR ;TEST FOR EXTRA BITS
42 03362 063077         HALT            ;MORE THAN 1 BIT IN AND OF 20000
43                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=20000
44
45                  ;NOW TEST AND OF COMPLIMENTS
46                  ;SOURCE WILL=20000 DEST WILL=COMPLIMENT
47                  ;AN17A:
48 03363 104000         COM     0,1
49 03364 107404         AND     0,1,SZR
50 03365 063077         HALT            ;AND OF 20000 AND ITS COM FAILED
51                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
52
53                  ;TEST AND OF COMPLIMENTS WITH DEST=20000 AND SRC=COM
54                  ;AN17B:
55 03366 105000         MOV     0,1
56 03367 130000         COM     1,2
57 03370 147404         AND     2,1,SZR
58 03371 063077         HALT            ;AND OF 20000 AND ITS COM FAILED
59                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
60 03372 101120         MOVZL   0,0     ;SET UP NEXT TEST
```

```
 0133 ,MAIN
01
02                          ANDTS   18,1,40000
03                          ;THE NEXT SERIES IS AN TST OF BIT 1
04                          ;AC0=40000 COMING INTO THE TEST
05                  ;AND18:
06 03373 105000             MOV     0,1     ;AC0=40000
07 03374 107405             AND     0,1,SNR ;BIT 1 SHD REMAIN=1
08 03375 063077             HALT
09 03376 131000             MOV     1,2
10 03377 112000             ADC     0,2
11 03400 150004             COM     2,2,SZR ;TEST FOR EXTRA BITS
12 03401 063077             HALT            ;MORE THAN 1 BIT IN AND OF 40000
13                          ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=40000
14
15                  ;NOW TEST AND OF COMPLIMENTS
16                  ;SOURCE WILL=40000 DEST WILL=COMPLIMENT
17                  ;AN18A:
18 03402 104000             COM     0,1
19 03403 107404             AND     0,1,SZR
20 03404 063077             HALT            ;AND OF 40000 AND ITS COM FAILED
21                          ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
22
23                  ;TEST AND OF COMPLIMENTS WITH DEST=40000 AND SRC=COM
24                  ;AN18B:
25 03405 105000             MOV     0,1
26 03406 130000             COM     1,2
27 03407 147404             AND     2,1,SZR
28 03410 063077             HALT            ;AND OF 40000 AND ITS COM FAILED
29                          ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
30 03411 101120             MOVZL   0,0     ;SET UP NEXT TEST
31
32                          ANDTS   19,0,100000
33                          ;THE NEXT SERIES IS AN TST OF BIT 0
34                          ;AC0=100000 COMING INTO THE TEST
35                  ;AND19:
36 03412 105000             MOV     0,1     ;AC0=100000
37 03413 107405             AND     0,1,SNR ;BIT 0 SHD REMAIN=1
38 03414 063077             HALT
39 03415 131000             MOV     1,2
40 03416 112000             ADC     0,2
41 03417 150004             COM     2,2,SZR ;TEST FOR EXTRA BITS
42 03420 063077             HALT            ;MORE THAN 1 BIT IN AND OF 100000
43                          ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=100000
44
45                  ;NOW TEST AND OF COMPLIMENTS
46                  ;SOURCE WILL=100000 DEST WILL=COMPLIMENT
47                  ;AN19A:
48 03421 104000             COM     0,1
49 03422 107404             AND     0,1,SZR
50 03423 063077             HALT            ;AND OF 100000 AND ITS COM FAILED
51                          ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
52
53                  ;TEST AND OF COMPLIMENTS WITH DEST=100000 AND SRC=COM
54                  ;AN19B:
55 03424 105000             MOV     0,1
56 03425 130000             COM     1,2
57 03426 147404             AND     2,1,SZR
58 03427 063077             HALT            ;AND OF 100000 AND ITS COM FAILED
59                          ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
60 03430 101120             MOVZL   0,0     ;SET UP NEXT TEST
```

```
 0134 .MAIN
 01
 02                ;THE NEXT SERIES OF TESTS VERYFI THAT "AND"
 03                ;DOES NOT EFFECT CRY
 04
 05 03431 102020 AND20:  ADCZ    0,0       ;CRY = 0  AC0:= -1
 06 03432 103402         AND     0,0,SZC   ;CRY SHD STILL=0
 07 03433 063077         HALT              ;AND SET CRY=1
 08                      ;SEE "NOT AND" AND WITH CRY OUT
 09
 10 03434 102040 AND21:  ADCO    0,0       ;AND=1 WITH CRY=1
 11 03435 103403         AND     0,0,SNC   ;CRY SHD STILL=1
 12 03436 063077         HALT              ;AND OF -1=1 CLRD CRY
 13
 14                      ;TEST AND WITH 00 TO NOT CHNG CRY 0 TO 1
 15
 16 03437 102000 AND22:  ADC     0,0
 17 03440 100020         COMZ    0,0
 18 03441 103402         AND     0,0,SZC
 19 03442 063077         HALT
 20
 21                      ;TEST AND WITH 00 TO NOT CHNG CRY 1 TO 0
 22
 23 03443 102000 AND23:  ADC     0,0
 24 03444 100040         COMO    0,0
 25 03445 103403         AND     0,0,SNC
 26 03446 063077         HALT
 27
 28
 29
 30                ;REPEAT TESTS CHANGING STATE OF CRY DURING AND
 31
 32 03447 102040 AND24:  ADCO    0,0
 33 03450 103422         ANDZ    0,0,SZC
 34 03451 063077         HALT              ;SEE IR11 NOT IR10 IN NOT SCI
 35                      ;POSSIBLY TRANSITION TIMING AS AND DID NOT PREV CHNG CRY
 36
 37 03452 102020 AND25:  ADCZ    0,0
 38 03453 103443         ANDO    0,0,SNC   ;SEE NOT OF ABOVE TEST IR10-11
 39 03454 063077         HALT              ;CRY WENT TO 0 AND -1 TO -1
 40
 41 03455 102000 AND26:  ADC     0,0
 42 03456 100040         COMO    0,0
 43 03457 103422         ANDZ    0,0,SZC   ;FURTHER TEST AND IN SCI LOGIC
 44 03460 063077         HALT              ;CRY WENT TO 1 AND 0 TO 0
 45
 46 03461 102000 AND27:  ADC     0,0
 47 03462 100020         COMZ    0,0
 48 03463 103443         ANDO    0,0,SNC
 49 03464 063077         HALT              ;CRY WENT 1 TO 0 AND OF 0 TO 0
 50
```

```
↓0135 .MAIN
01
02                ;VERIFY THE EXISTENCE OF INC INSTRUCTION
03                ;FIRST TIME FOR "INC" INSTRUCTION
04
05 03465 102000 INC00:  ADC     0,0
06 03466 100000         COM     0,0
07 03467 101405         INC     0,0,SNR ;RESULT POSSIBLY ALU CRY NOT
08 03470 063077         HALT            ;AC0 SHD=+1
09 03471 101005         MOV     0,0,SNR
10 03472 063077         HALT            ;MAKE SURE RESULT GOT BACK TO 0
11 03473 105224         MOVZR   0,1,SZR ;MAKE SURE ONLY +1 NO EXTRAS
12 03474 063077         HALT            ;EXAMINE AC0 FOR EXTRA BITS INC
13                      ;AC0=0 POSSIBLY "NOT" IR6 INC LOOKS LIKE NEG
14                      ;OR "NOT" IR7 INC LOOKS LIKE MOV SEE ALU ROM
15                      ;OR IR5 INTO IO ALC ROM INC LOOKS LIKE AND
16
17                ;TEST INC OF +1 TO +2 (2ND TIME FOR INC)
18 03475 102000 INC01:  ADC     0,0
19 03476 100140         COMOL   0,0     ;AC0=+1
20 03477 105120         MOVZL   0,1     ;AC1=+2
21 03500 101405         INC     0,0,SNR ;1+1 SHD = 2
22 03501 063077         HALT            ;BIT 15 CARRY TO BIT14(?)
23 03502 106000         ADC     0,1     ;AC1 SHD NOW =-1 (IF INC WORKED)
24 03503 124004         COM     1,1,SZR ;AND COM SHD BE 0
25 03504 063077         HALT            ;AC0 INC'D+1 INCORRECT
26                      ;EXAMINE AC0 FOR ALU FAILURE IT SHD=+2
27                      ;IF AC0 DOES=+2 EXAMINE AC1 FOR ADC+COM FAILURE
28
29                ;TEST TO INSURE ONLY SRC REG IS INVOLVED IN INC
30 03505 102000 INC02:  ADC     0,0
31 03506 100000         COM     0,0     ;AC0=0
32 03507 104140         COMOL   0,1     ;AC1=1
33 03510 125140         MOVOL   1,1     ;=3
34 03511 105405         INC     0,1,SNR ;0+1 SHD =1
35 03512 063077         HALT            ;ALU CRY FAILED (?) ALDRY TESTED
36 03513 131224         MOVZR   1,2,SZR ;AC1 SHD ONLY=1
37 03514 063077         HALT            ;PROBABLY DESTINATION REG ALSO ADDED
38                      ;SEE 2 REN IO ALC ROM INC ALSO CAUSES ADD OR AND
39
```

```
10136 .MAIN
01
02
03                ;TEST INC TO CARRY THROUGH ALL 1 BITS
04                ;DEFINE MACRO FOR CARRY TESTS
05
06                        .MACRO INCTS
07                        ;AC0=14 COMING INTO TEST,+1=AC=15
08                        ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
09                        ;BIT 12 INTO BIT 13 WITH RESULT=AC1
10
11                ;INC11:
12                        INC     0,2,SNR ;AC0=14+1 AND BE NON ZERO
13                        HALT            ;INC RESULT SHD=15
14                        MOV     2,3
15                        ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
16                        COM     3,3,SZR ;THEN 0
17                        HALT
18                        MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
19                        MOVZL   1,1     ;SET UP RESULT NEXT TEST
20                %
21
22
23
24                        ;SET UP FIRST CARRY TEST
25
26 03515 102000           ADC     0,0
27 03516 100000           COM     0,0
28 03517 105140           MOVOL   0,1
29
30
31
32                        INCTS 03,ALUCRY,15,0,1
33                        ;AC0=0 COMING INTO TEST,+1=AC=1
34                        ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
35                        ;BIT ALUCRY INTO BIT 15 WITH RESULT=AC1
36
37                ;INC03:
38 03520 111405           INC     0,2,SNR ;AC0=0+1 AND BE NON ZERO
39 03521 063077           HALT            ;INC RESULT SHD=1
40 03522 155000           MOV     2,3
41 03523 136000           ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
42 03524 174004           COM     3,3,SZR ;THEN 0
43 03525 063077           HALT
44 03526 101140           MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
45 03527 125120           MOVZL   1,1     ;SET UP RESULT NEXT TEST
46
47                        INCTS 04,15,14,1,2
48                        ;AC0=1 COMING INTO TEST,+1=AC=2
49                        ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
50                        ;BIT 15 INTO BIT 14 WITH RESULT=AC1
51
52                ;INC04:
53 03530 111405           INC     0,2,SNR ;AC0=1+1 AND BE NON ZERO
54 03531 063077           HALT            ;INC RESULT SHD=2
55 03532 155000           MOV     2,3
56 03533 136000           ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
57 03534 174004           COM     3,3,SZR ;THEN 0
58 03535 063077           HALT
59 03536 101140           MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
60 03537 125120           MOVZL   1,1     ;SET UP RESULT NEXT TEST
```

```
0137 .MAIN
)1
)2                          INCTS 05,14,13,3,4
)3                          ;AC0=3 COMING INTO TEST,+1=AC=4
)4                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
)5                          ;BIT 14 INTO BIT 13 WITH RESULT=AC1
)6
)7                  ;INC05:
)8 03540 111405             INC     0,2,SNR ;AC0=3+1 AND BE NON ZERO
)9 03541 063077             HALT            ;INC RESULT SHD=4
:0 03542 155000             MOV     2,3
:1 03543 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
:2 03544 174004             COM     3,3,SZR ;THEN 0
:3 03545 063077             HALT
:4 03546 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
:5 03547 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
:6
:7                          INCTS 06,13,12,7,10
:8                          ;AC0=7 COMING INTO TEST,+1=AC=10
:9                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
:0                          ;BIT 13 INTO BIT 12 WITH RESULT=AC1
:1
:2                  ;INC06:
:3 03550 111405             INC     0,2,SNR ;AC0=7+1 AND BE NON ZERO
:4 03551 063077             HALT            ;INC RESULT SHD=10
:5 03552 155000             MOV     2,3
:6 03553 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
:7 03554 174004             COM     3,3,SZR ;THEN 0
:8 03555 063077             HALT
:9 03556 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
;0 03557 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
;1
;2                          INCTS 07,12,11,17,20
;3                          ;AC0=17 COMING INTO TEST,+1=AC=20
;4                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
;5                          ;BIT 12 INTO BIT 11 WITH RESULT=AC1
;6
;7                  ;INC07:
;8 03560 111405             INC     0,2,SNR ;AC0=17+1 AND BE NON ZERO
;9 03561 063077             HALT            ;INC RESULT SHD=20
;0 03562 155000             MOV     2,3
;1 03563 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
;2 03564 174004             COM     3,3,SZR ;THEN 0
;3 03565 063077             HALT
;4 03566 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
;5 03567 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
;6
;7                          INCTS 08,11,10,37,40
;8                          ;AC0=37 COMING INTO TEST,+1=AC=40
;9                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
;0                          ;BIT 11 INTO BIT 10 WITH RESULT=AC1
;1
;2                  ;INC08:
;3 03570 111405             INC     0,2,SNR ;AC0=37+1 AND BE NON ZERO
;4 03571 063077             HALT            ;INC RESULT SHD=40
;5 03572 155000             MOV     2,3
;6 03573 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
;7 03574 174004             COM     3,3,SZR ;THEN 0
;8 03575 063077             HALT
;9 03576 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
>0 03577 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
```

```
 0138 ,MAIN
01
02                          INCTS 09,10,9,77,100
03                          ;AC0=77 COMING INTO TEST,+1=AC=100
04                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
05                          ;BIT 10 INTO BIT 9 WITH RESULT=AC1
06
07                    ;INC09:
08 03600 111405             INC     0,2,SNR ;AC0=77+1 AND BE NON ZERO
09 03601 063077             HALT            ;INC RESULT SHD=100
10 03602 155000             MOV     2,3
11 03603 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
12 03604 174004             COM     3,3,SZR ;THEN 0
13 03605 063077             HALT
14 03606 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
15 03607 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
16
17                          INCTS 10,9,8,177,200
18                          ;AC0=177 COMING INTO TEST,+1=AC=200
19                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
20                          ;BIT 9 INTO BIT 8 WITH RESULT=AC1
21
22                    ;INC10:
23 03610 111405             INC     0,2,SNR ;AC0=177+1 AND BE NON ZERO
24 03611 063077             HALT            ;INC RESULT SHD=200
25 03612 155000             MOV     2,3
26 03613 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
27 03614 174004             COM     3,3,SZR ;THEN 0
28 03615 063077             HALT
29 03616 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
30 03617 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
31
32                          INCTS 11,8,7,377,400
33                          ;AC0=377 COMING INTO TEST,+1=AC=400
34                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
35                          ;BIT 8 INTO BIT 7 WITH RESULT=AC1
36
37                    ;INC11:
38 03620 111405             INC     0,2,SNR ;AC0=377+1 AND BE NON ZERO
39 03621 063077             HALT            ;INC RESULT SHD=400
40 03622 155000             MOV     2,3
41 03623 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
42 03624 174004             COM     3,3,SZR ;THEN 0
43 03625 063077             HALT
44 03626 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
45 03627 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
46
47                          INCTS 12,7,6,777,1000
48                          ;AC0=777 COMING INTO TEST,+1=AC=1000
49                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
50                          ;BIT 7 INTO BIT 6 WITH RESULT=AC1
51
52                    ;INC12:
53 03630 111405             INC     0,2,SNR ;AC0=777+1 AND BE NON ZERO
54 03631 063077             HALT            ;INC RESULT SHD=1000
55 03632 155000             MOV     2,3
56 03633 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
57 03634 174004             COM     3,3,SZR ;THEN 0
58 03635 063077             HALT
59 03636 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
60 03637 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
```

```
 0139 .MAIN
01
02                          INCTS 13,6,5,1777,2000
03                          ;AC0=1777 COMING INTO TEST,+1=AC=2000
04                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
05                          ;BIT 6 INTO BIT 5 WITH RESULT=AC1
06
07                    ;INC13:
08 03640 111405             INC     0,2,SNR ;AC0=1777+1 AND BE NON ZERO
09 03641 063077             HALT            ;INC RESULT SHD=2000
10 03642 155000             MOV     2,3
11 03643 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
12 03644 174004             COM     3,3,SZR ;THEN 0
13 03645 063077             HALT
14 03646 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
15 03647 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
16
17                          INCTS 14,5,4,3777,4000
18                          ;AC0=3777 COMING INTO TEST,+1=AC=4000
19                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
20                          ;BIT 5 INTO BIT 4 WITH RESULT=AC1
21
22                    ;INC14:
23 03650 111405             INC     0,2,SNR ;AC0=3777+1 AND BE NON ZERO
24 03651 063077             HALT            ;INC RESULT SHD=4000
25 03652 155000             MOV     2,3
26 03653 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
27 03654 174004             COM     3,3,SZR ;THEN 0
28 03655 063077             HALT
29 03656 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
30 03657 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
31
32                          INCTS 15,4,3,7777,10000
33                          ;AC0=7777 COMING INTO TEST,+1=AC=10000
34                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
35                          ;BIT 4 INTO BIT 3 WITH RESULT=AC1
36
37                    ;INC15:
38 03660 111405             INC     0,2,SNR ;AC0=7777+1 AND BE NON ZERO
39 03661 063077             HALT            ;INC RESULT SHD=10000
40 03662 155000             MOV     2,3
41 03663 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
42 03664 174004             COM     3,3,SZR ;THEN 0
43 03665 063077             HALT
44 03666 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
45 03667 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
46
47                          INCTS 16,3,2,17777,20000
48                          ;AC0=17777 COMING INTO TEST,+1=AC=20000
49                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
50                          ;BIT 3 INTO BIT 2 WITH RESULT=AC1
51
52                    ;INC16:
53 03670 111405             INC     0,2,SNR ;AC0=17777+1 AND BE NON ZERO
54 03671 063077             HALT            ;INC RESULT SHD=20000
55 03672 155000             MOV     2,3
56 03673 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
57 03674 174004             COM     3,3,SZR ;THEN 0
58 03675 063077             HALT
59 03676 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
60 03677 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
```

```
 0140 .MAIN
01
02                          INCTS 17,2,1,37777,40000
03                          ;AC0=37777 COMING INTO TEST,+1=AC=40000
04                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
05                          ;BIT 2 INTO BIT 1 WITH RESULT=AC1
06
07                    ;INC17:
08 03700 111405             INC     0,2,SNR ;AC0=37777+1 AND BE NON ZERO
09 03701 063077             HALT            ;INC RESULT SHD=40000
10 03702 155000             MOV     2,3
11 03703 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
12 03704 174004             COM     3,3,SZR ;THEN 0
13 03705 063077             HALT
14 03706 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
15 03707 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
16
17                          INCTS 18,1,0,77777,100000
18                          ;AC0=77777 COMING INTO TEST,+1=AC=100000
19                          ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
20                          ;BIT 1 INTO BIT 0 WITH RESULT=AC1
21
22                    ;INC18:
23 03710 111405             INC     0,2,SNR ;AC0=77777+1 AND BE NON ZERO
24 03711 063077             HALT            ;INC RESULT SHD=100000
25 03712 155000             MOV     2,3
26 03713 136000             ADC     1,3     ;ADC SUM OF 1+3 SHD=-1
27 03714 174004             COM     3,3,SZR ;THEN 0
28 03715 063077             HALT
29 03716 101140             MOVOL   0,0     ;SET UP CONSTANTS NEXT TEST
30 03717 125120             MOVZL   1,1     ;SET UP RESULT NEXT TEST
31
32                    ;TEST INC OF -1 AC TO=0 WITH CRY COMP 0 TO 1
33
34 03720 102040 INC20:  ADCO    0,0
35 03721 101424             INCZ    0,0,SZR
36 03722 063077             HALT            ;INC=1 DID NOT=0
37 03723 101003             MOV     0,0,SNC
38 03724 063077             HALT            ;CRY OUT DID NOT COM 0 TO 1
39                          ;EXAMINE AC0 FOR ALU FAILURE IF FIRST HALT
40
41                    ;TEST INC OF-1 AC TO=0 AND CRY TO COMP 1 TO 0
42
43 03725 102020 INC21:  ADCZ    0,0
44 03726 101444             INCO    0,0,SZR
45 03727 063077             HALT            ;INC=1 DID NOT=0
46 03730 101002             MOV     0,0,SZC
47 03731 063077             HALT            ;CRY OUT DID NOT COM 1 TO 0
48                          ;EXAMINE AC0 FOR ALU FAILURE IF FIRST HALT
```

```
!0141 .MAIN
01
02                ;FIRST USE OF NEG INSTRUCTION
03
04                ;NEG-1 TO -1 TO VERIFY CORRECT INSTR REF
05
06 03732 102000 NEG00:  ADC     0,0
07 03733 100405         NEG     0,0,SNR
08 03734 063077         HALT            ;NEG MAY=COM+INC+SUB
09 03735 105224         MOVZR   0,1,SZR
10 03736 063077         HALT            ;NEG OF -1 SOMETHING OTHER THAN +1
11                      ;EXAMINE AC0 FOR ALU ERROR
12
13                ;THE NEGATION OF +1 SHD=-1
14
15 03737 102000 NEG01:  ADC     0,0     ;SET=-1
16 03740 100140         COMOL   0,0     ;MAKES AC0=1
17 03741 100405         NEG     0,0,SNR ;MAKES AC0=-1
18 03742 063077         HALT            ;(1)
19 03743 104004         COM     0,1,SZR ;RESULT REALLY=-1
20 03744 063077         HALT            ;NEG OF +1 SOMETHING OTHER THAN -1
21                      ;EXAMINE AC0 FOR ALU ERROR OR AC1 FOR COM
22
23
24                ;DEFINE MACRO FOR FURTHER TESTS OF NEG
25
26                      .MACRO NEGTS
27                      ;AC0=14 COMING INTO TEST IT SHD NEG TO=15
28                      ;NEG IS EQUIVALENT TO COM+INC
29                      ;CARRY IS THROUGH BIT 12 BUT SHOULD STORE AT BIT 13
30                      ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
31                NEG11:  NEG     0,2,SNR ;14+1 SHD=15
32                      HALT            ;CARRY WENT THROUGH BIT 13
33                      MOV     2,3
34                      ADC     1,3     ;AC1=COM OF 15 AC3 SHD=-1
35                      COM     3,3,SZR ;RESULT COM -1 SHD=0
36                      HALT            ;EXAM AC2 FOR ALU ERR SHD=15
37                      ;AC2=15 TI SHOULD NEG AGAIN TO=AC0 OR 14
38                NG11A:  NEG     2,3     ;AC2=15 3 SHD=14
39                      ADC     0,3     ;AC3 SHD NOW=-1
40                      COM#    3,3,SZR ;AND ITS COM=0
41                      HALT            ;15 DID NOT NEG TO 14
42                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 14
43                      MOVZL   0,0
44                      MOVZL   1,1     ;SET UP NEXT TEST
45                %
46
47
48
49                      ;SET UP NEG TESTS
50                      ;START WITH AC0=1 AC1=0
51                      ;2ND TEST AC0=2 AC1=1
52
53 03745 126000         ADC     1,1     ;SET UP AC1=-1
54 03746 120140         COMOL   1,0     ;AC0=+1
```

```
;0142 .MAIN
01
02                          NEGTS 03,ALUCRY,15,1,177777
03                          ;AC0=1 COMING INTO TEST IT SHD NEG TO=177777
04                          ;NEG IS EQUIVALENT TO COM+INC
05                          ;CARRY IS THROUGH BIT ALUCRY BUT SHOULD STORE AT BIT 15
06                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
07 03747 110405 NEG03:      NEG     0,2,SNR ;1+1 SHD=177777
08 03750 063077             HALT            ;CARRY WENT THROUGH BIT 15
09 03751 155000             MOV     2,3
10 03752 136000             ADC     1,3     ;AC1=COM OF 177777 AC3 SHD=-1
11 03753 174004             COM     3,3,SZR ;RESULT COM -1 SHD=0
12 03754 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=177777
13                          ;AC2=177777 TI SHOULD NEG AGAIN TO=AC0 OR 1
14 03755 154400 NG03A:      NEG     2,3     ;AC2=177777 3 SHD=1
15 03756 116000             ADC     0,3     ;AC3 SHD NOW=-1
16 03757 174014             COM#    3,3,SZR ;AND ITS COM=0
17 03760 063077             HALT            ;177777 DID NOT NEG TO 1
18                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 1
19 03761 101120             MOVZL   0,0
20 03762 125120             MOVZL   1,1     ;SET UP NEXT TEST
21
22                          NEGTS 04,15,14,2,177776
23                          ;AC0=2 COMING INTO TEST IT SHD NEG TO=177776
24                          ;NEG IS EQUIVALENT TO COM+INC
25                          ;CARRY IS THROUGH BIT 15 BUT SHOULD STORE AT BIT 14
26                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
27 03763 110405 NEG04:      NEG     0,2,SNR ;2+1 SHD=177776
28 03764 063077             HALT            ;CARRY WENT THROUGH BIT 14
29 03765 155000             MOV     2,3
30 03766 136000             ADC     1,3     ;AC1=COM OF 177776 AC3 SHD=-1
31 03767 174004             COM     3,3,SZR ;RESULT COM -1 SHD=0
32 03770 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=177776
33                          ;AC2=177776 TI SHOULD NEG AGAIN TO=AC0 OR 2
34 03771 154400 NG04A:      NEG     2,3     ;AC2=177776 3 SHD=2
35 03772 116000             ADC     0,3     ;AC3 SHD NOW=-1
36 03773 174014             COM#    3,3,SZR ;AND ITS COM=0
37 03774 063077             HALT            ;177776 DID NOT NEG TO 2
38                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 2
39 03775 101120             MOVZL   0,0
40 03776 125120             MOVZL   1,1     ;SET UP NEXT TEST
41
42                          NEGTS 05,14,13,4,177774
43                          ;AC0=4 COMING INTO TEST IT SHD NEG TO=177774
44                          ;NEG IS EQUIVALENT TO COM+INC
45                          ;CARRY IS THROUGH BIT 14 BUT SHOULD STORE AT BIT 13
46                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
47 03777 110405 NEG05:      NEG     0,2,SNR ;4+1 SHD=177774
48 04000 063077             HALT            ;CARRY WENT THROUGH BIT 13
49 04001 155000             MOV     2,3
50 04002 136000             ADC     1,3     ;AC1=COM OF 177774 AC3 SHD=-1
51 04003 174004             COM     3,3,SZR ;RESULT COM -1 SHD=0
52 04004 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=177774
53                          ;AC2=177774 TI SHOULD NEG AGAIN TO=AC0 OR 4
54 04005 154400 NG05A:      NEG     2,3     ;AC2=177774 3 SHD=4
55 04006 116000             ADC     0,3     ;AC3 SHD NOW=-1
56 04007 174014             COM#    3,3,SZR ;AND ITS COM=0
57 04010 063077             HALT            ;177774 DID NOT NEG TO 4
58                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 4
59 04011 101120             MOVZL   0,0
60 04012 125120             MOVZL   1,1     ;SET UP NEXT TEST
```

```
 0143 .MAIN
01
02                          NEGTS 06,13,12,10,177770
03                          ;AC0=10 COMING INTO TEST IT SHD NEG TO=177770
04                          ;NEG IS EQUIVALENT TO COM+INC
05                          ;CARRY IS THROUGH BIT 13 BUT SHOULD STORE AT BIT 12
06                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
07 04013 110405 NEG06:      NEG     0,2,SNR ;10+1 SHD=177770
08 04014 063077             HALT            ;CARRY WENT THROUGH BIT 12
09 04015 155000             MOV     2,3
10 04016 136000             ADC     1,3     ;AC1=COM OF 177770 AC3 SHD=-1
11 04017 174004             COM     3,3,SZR ;RESULT COM -1 SHD=0
12 04020 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=177770
13                          ;AC2=177770 TI SHOULD NEG AGAIN TO=AC0 OR 10
14 04021 154400 NG06A:      NEG     2,3     ;AC2=177770 3 SHD=10
15 04022 116000             ADC     0,3     ;AC3 SHD NOW=-1
16 04023 174014             COM#    3,3,SZR ;AND ITS COM=0
17 04024 063077             HALT            ;177770 DID NOT NEG TO 10
18                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 10
19 04025 101120             MOVZL   0,0
20 04026 125120             MOVZL   1,1     ;SET UP NEXT TEST
21
22                          NEGTS 07,12,11,20,177760
23                          ;AC0=20 COMING INTO TEST IT SHD NEG TO=177760
24                          ;NEG IS EQUIVALENT TO COM+INC
25                          ;CARRY IS THROUGH BIT 12 BUT SHOULD STORE AT BIT 11
26                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
27 04027 110405 NEG07:      NEG     0,2,SNR ;20+1 SHD=177760
28 04030 063077             HALT            ;CARRY WENT THROUGH BIT 11
29 04031 155000             MOV     2,3
30 04032 136000             ADC     1,3     ;AC1=COM OF 177760 AC3 SHD=-1
31 04033 174004             COM     3,3,SZR ;RESULT COM -1 SHD=0
32 04034 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=177760
33                          ;AC2=177760 TI SHOULD NEG AGAIN TO=AC0 OR 20
34 04035 154400 NG07A:      NEG     2,3     ;AC2=177760 3 SHD=20
35 04036 116000             ADC     0,3     ;AC3 SHD NOW=-1
36 04037 174014             COM#    3,3,SZR ;AND ITS COM=0
37 04040 063077             HALT            ;177760 DID NOT NEG TO 20
38                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 20
39 04041 101120             MOVZL   0,0
40 04042 125120             MOVZL   1,1     ;SET UP NEXT TEST
41
42                          NEGTS 08,11,10,40,177740
43                          ;AC0=40 COMING INTO TEST IT SHD NEG TO=177740
44                          ;NEG IS EQUIVALENT TO COM+INC
45                          ;CARRY IS THROUGH BIT 11 BUT SHOULD STORE AT BIT 10
46                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
47 04043 110405 NEG08:      NEG     0,2,SNR ;40+1 SHD=177740
48 04044 063077             HALT            ;CARRY WENT THROUGH BIT 10
49 04045 155000             MOV     2,3
50 04046 136000             ADC     1,3     ;AC1=COM OF 177740 AC3 SHD=-1
51 04047 174004             COM     3,3,SZR ;RESULT COM -1 SHD=0
52 04050 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=177740
53                          ;AC2=177740 TI SHOULD NEG AGAIN TO=AC0 OR 40
54 04051 154400 NG08A:      NEG     2,3     ;AC2=177740 3 SHD=40
55 04052 116000             ADC     0,3     ;AC3 SHD NOW=-1
56 04053 174014             COM#    3,3,SZR ;AND ITS COM=0
57 04054 063077             HALT            ;177740 DID NOT NEG TO 40
58                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 40
59 04055 101120             MOVZL   0,0
60 04056 125120             MOVZL   1,1     ;SET UP NEXT TEST
```

```
 0144 .MAIN
01
02                          NEGTS 09,10,9,100,177700
03                          ;AC0=100 COMING INTO TEST IT SHD NEG TO=177700
04                          ;NEG IS EQUIVALENT TO COM+INC
05                          ;CARRY IS THROUGH BIT 10 BUT SHOULD STORE AT BIT 9
06                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
07 04057 110405 NEG09:      NEG     0,2,SNR ;100+1 SHD=177700
08 04060 063077             HALT            ;CARRY WENT THROUGH BIT 9
09 04061 155000             MOV     2,3
10 04062 136000             ADC     1,3     ;AC1=COM OF 177700 AC3 SHD=-1
11 04063 174004             COM     3,3,SZR ;RESULT COM -1 SHD=0
12 04064 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=177700
13                          ;AC2=177700 TI SHOULD NEG AGAIN TO=AC0 OR 100
14 04065 154400 NG09A:      NEG     2,3     ;AC2=177700 3 SHD=100
15 04066 116000             ADC     0,3     ;AC3 SHD NOW=-1
16 04067 174014             COM#    3,3,SZR ;AND ITS COM=0
17 04070 063077             HALT            ;177700 DID NOT NEG TO 100
18                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 100
19 04071 101120             MOVZL   0,0
20 04072 125120             MOVZL   1,1     ;SET UP NEXT TEST
21
22                          NEGTS 10,9,8,200,177600
23                          ;AC0=200 COMING INTO TEST IT SHD NEG TO=177600
24                          ;NEG IS EQUIVALENT TO COM+INC
25                          ;CARRY IS THROUGH BIT 9 BUT SHOULD STORE AT BIT 8
26                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
27 04073 110405 NEG10:      NEG     0,2,SNR ;200+1 SHD=177600
28 04074 063077             HALT            ;CARRY WENT THROUGH BIT 8
29 04075 155000             MOV     2,3
30 04076 136000             ADC     1,3     ;AC1=COM OF 177600 AC3 SHD=-1
31 04077 174004             COM     3,3,SZR ;RESULT COM -1 SHD=0
32 04100 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=177600
33                          ;AC2=177600 TI SHOULD NEG AGAIN TO=AC0 OR 200
34 04101 154400 NG10A:      NEG     2,3     ;AC2=177600 3 SHD=200
35 04102 116000             ADC     0,3     ;AC3 SHD NOW=-1
36 04103 174014             COM#    3,3,SZR ;AND ITS COM=0
37 04104 063077             HALT            ;177600 DID NOT NEG TO 200
38                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 200
39 04105 101120             MOVZL   0,0
40 04106 125120             MOVZL   1,1     ;SET UP NEXT TEST
41
42                          NEGTS 11,8,7,400,177400
43                          ;AC0=400 COMING INTO TEST IT SHD NEG TO=177400
44                          ;NEG IS EQUIVALENT TO COM+INC
45                          ;CARRY IS THROUGH BIT 8 BUT SHOULD STORE AT BIT 7
46                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
47 04107 110405 NEG11:      NEG     0,2,SNR ;400+1 SHD=177400
48 04110 063077             HALT            ;CARRY WENT THROUGH BIT 7
49 04111 155000             MOV     2,3
50 04112 136000             ADC     1,3     ;AC1=COM OF 177400 AC3 SHD=-1
51 04113 174004             COM     3,3,SZR ;RESULT COM -1 SHD=0
52 04114 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=177400
53                          ;AC2=177400 TI SHOULD NEG AGAIN TO=AC0 OR 400
54 04115 154400 NG11A:      NEG     2,3     ;AC2=177400 3 SHD=400
55 04116 116000             ADC     0,3     ;AC3 SHD NOW=-1
56 04117 174014             COM#    3,3,SZR ;AND ITS COM=0
57 04120 063077             HALT            ;177400 DID NOT NEG TO 400
58                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 400
59 04121 101120             MOVZL   0,0
60 04122 125120             MOVZL   1,1     ;SET UP NEXT TEST
```

```
 0145 .MAIN
01
02                          NEGTS 12,7,6,100,177000
03                          ;AC0=100 COMING INTO TEST IT SHD NEG TO=177000
04                          ;NEG IS EQUIVALENT TO COM+INC
05                          ;CARRY IS THROUGH BIT 7 BUT SHOULD STORE AT BIT 6
06                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
07 04123 110405 NEG12:      NEG     0,2,SNR ;100+1 SHD=177000
08 04124 063077             HALT            ;CARRY WENT THROUGH BIT 6
09 04125 155000             MOV     2,3
10 04126 136000             ADC     1,3     ;AC1=COM OF 177000 AC3 SHD=-1
11 04127 174004             COM     3,3,SZR ;RESULT COM =1 SHD=0
12 04130 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=177000
13                          ;AC2=177000 TI SHOULD NEG AGAIN TO=AC0 OR 100
14 04131 154400 NG12A:      NEG     2,3     ;AC2=177000 3 SHD=100
15 04132 116000             ADC     0,3     ;AC3 SHD NOW=-1
16 04133 174014             COM#    3,3,SZR ;AND ITS COM=0
17 04134 063077             HALT            ;177000 DID NOT NEG TO 100
18                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 100
19 04135 101120             MOVZL   0,0
20 04136 125120             MOVZL   1,1     ;SET UP NEXT TEST
21
22                          NEGTS 13,6,5,2000,176000
23                          ;AC0=2000 COMING INTO TEST IT SHD NEG TO=176000
24                          ;NEG IS EQUIVALENT TO COM+INC
25                          ;CARRY IS THROUGH BIT 6 BUT SHOULD STORE AT BIT 5
26                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
27 04137 110405 NEG13:      NEG     0,2,SNR ;2000+1 SHD=176000
28 04140 063077             HALT            ;CARRY WENT THROUGH BIT 5
29 04141 155000             MOV     2,3
30 04142 136000             ADC     1,3     ;AC1=COM OF 176000 AC3 SHD=-1
31 04143 174004             COM     3,3,SZR ;RESULT COM =1 SHD=0
32 04144 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=176000
33                          ;AC2=176000 TI SHOULD NEG AGAIN TO=AC0 OR 2000
34 04145 154400 NG13A:      NEG     2,3     ;AC2=176000 3 SHD=2000
35 04146 116000             ADC     0,3     ;AC3 SHD NOW=-1
36 04147 174014             COM#    3,3,SZR ;AND ITS COM=0
37 04150 063077             HALT            ;176000 DID NOT NEG TO 2000
38                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 2000
39 04151 101120             MOVZL   0,0
40 04152 125120             MOVZL   1,1     ;SET UP NEXT TEST
41
42                          NEGTS 14,5,4,4000,174000
43                          ;AC0=4000 COMING INTO TEST IT SHD NEG TO=174000
44                          ;NEG IS EQUIVALENT TO COM+INC
45                          ;CARRY IS THROUGH BIT 5 BUT SHOULD STORE AT BIT 4
46                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
47 04153 110405 NEG14:      NEG     0,2,SNR ;4000+1 SHD=174000
48 04154 063077             HALT            ;CARRY WENT THROUGH BIT 4
49 04155 155000             MOV     2,3
50 04156 136000             ADC     1,3     ;AC1=COM OF 174000 AC3 SHD=-1
51 04157 174004             COM     3,3,SZR ;RESULT COM =1 SHD=0
52 04160 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=174000
53                          ;AC2=174000 TI SHOULD NEG AGAIN TO=AC0 OR 4000
54 04161 154400 NG14A:      NEG     2,3     ;AC2=174000 3 SHD=4000
55 04162 116000             ADC     0,3     ;AC3 SHD NOW=-1
56 04163 174014             COM#    3,3,SZR ;AND ITS COM=0
57 04164 063077             HALT            ;174000 DID NOT NEG TO 4000
58                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 4000
59 04165 101120             MOVZL   0,0
60 04166 125120             MOVZL   1,1     ;SET UP NEXT TEST
```

```
 0146 .MAIN
01
02                          NEGTS 15,4,3,10000,170000
03                          ;AC0=10000 COMING INTO TEST IT SHD NEG TO=170000
04                          ;NEG IS EQUIVALENT TO COM+INC
05                          ;CARRY IS THROUGH BIT 4 BUT SHOULD STORE AT BIT 3
06                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
07 04167 110405 NEG15:      NEG     0,2,SNR ;10000+1 SHD=170000
08 04170 063077             HALT            ;CARRY WENT THROUGH BIT 3
09 04171 155000             MOV     2,3
10 04172 136000             ADC     1,3     ;AC1=COM OF 170000 AC3 SHD=-1
11 04173 174004             COM     3,3,SZR ;RESULT COM =1 SHD=0
12 04174 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=170000
13                          ;AC2=170000 TI SHOULD NEG AGAIN TO=AC0 OR 10000
14 04175 154400 NG15A:      NEG     2,3     ;AC2=170000 3 SHD=10000
15 04176 116000             ADC     0,3     ;AC3 SHD NOW=-1
16 04177 174014             COM#    3,3,SZR ;AND ITS COM=0
17 04200 063077             HALT            ;170000 DID NOT NEG TO 10000
18                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 10000
19 04201 101120             MOVZL   0,0
20 04202 125120             MOVZL   1,1     ;SET UP NEXT TEST
21
22                          NEGTS 16,3,1,20000,160000
23                          ;AC0=20000 COMING INTO TEST IT SHD NEG TO=160000
24                          ;NEG IS EQUIVALENT TO COM+INC
25                          ;CARRY IS THROUGH BIT 3 BUT SHOULD STORE AT BIT 1
26                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
27 04203 110405 NEG16:      NEG     0,2,SNR ;20000+1 SHD=160000
28 04204 063077             HALT            ;CARRY WENT THROUGH BIT 1
29 04205 155000             MOV     2,3
30 04206 136000             ADC     1,3     ;AC1=COM OF 160000 AC3 SHD=-1
31 04207 174004             COM     3,3,SZR ;RESULT COM =1 SHD=0
32 04210 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=160000
33                          ;AC2=160000 TI SHOULD NEG AGAIN TO=AC0 OR 20000
34 04211 154400 NG16A:      NEG     2,3     ;AC2=160000 3 SHD=20000
35 04212 116000             ADC     0,3     ;AC3 SHD NOW=-1
36 04213 174014             COM#    3,3,SZR ;AND ITS COM=0
37 04214 063077             HALT            ;160000 DID NOT NEG TO 20000
38                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 20000
39 04215 101120             MOVZL   0,0
40 04216 125120             MOVZL   1,1     ;SET UP NEXT TEST
41
42                          NEGTS 17,2,1,40000,140000
43                          ;AC0=40000 COMING INTO TEST IT SHD NEG TO=140000
44                          ;NEG IS EQUIVALENT TO COM+INC
45                          ;CARRY IS THROUGH BIT 2 BUT SHOULD STORE AT BIT 1
46                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
47 04217 110405 NEG17:      NEG     0,2,SNR ;40000+1 SHD=140000
48 04220 063077             HALT            ;CARRY WENT THROUGH BIT 1
49 04221 155000             MOV     2,3
50 04222 136000             ADC     1,3     ;AC1=COM OF 140000 AC3 SHD=-1
51 04223 174004             COM     3,3,SZR ;RESULT COM =1 SHD=0
52 04224 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=140000
53                          ;AC2=140000 TI SHOULD NEG AGAIN TO=AC0 OR 40000
54 04225 154400 NG17A:      NEG     2,3     ;AC2=140000 3 SHD=40000
55 04226 116000             ADC     0,3     ;AC3 SHD NOW=-1
56 04227 174014             COM#    3,3,SZR ;AND ITS COM=0
57 04230 063077             HALT            ;140000 DID NOT NEG TO 40000
58                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 40000
59 04231 101120             MOVZL   0,0
60 04232 125120             MOVZL   1,1     ;SET UP NEXT TEST
```

```
 0147 .MAIN
01
02                          NEGTS 18,1,0,100000,100000
03                          ;AC0=100000 COMING INTO TEST IT SHD NEG TO=100000
04                          ;NEG IS EQUIVALENT TO COM+INC
05                          ;CARRY IS THROUGH BIT 1 BUT SHOULD STORE AT BIT 0
06                          ;AND HIGHER ORDER BITS SHOULD REAMIN 1'S
07 04233 110405 NEG18:      NEG     0,2,SNR ;100000+1 SHD=100000
08 04234 063077             HALT            ;CARRY WENT THROUGH BIT 0
09 04235 155000             MOV     2,3
10 04236 136000             ADC     1,3     ;AC1=COM OF 100000 AC3 SHD=-1
11 04237 174004             COM     3,3,SZR ;RESULT COM -1 SHD=0
12 04240 063077             HALT            ;EXAM AC2 FOR ALU ERR SHD=100000
13                          ;AC2=100000 TI SHOULD NEG AGAIN TO=AC0 OR 100000
14 04241 154400 NG18A:      NEG     2,3     ;AC2=100000 3 SHD=100000
15 04242 116000             ADC     0,3     ;AC3 SHD NOW=-1
16 04243 174014             COM#    3,3,SZR ;AND ITS COM=0
17 04244 063077             HALT            ;100000 DID NOT NEG TO 100000
18                          ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC 100000
19 04245 101120             MOVZL   0,0
20 04246 125120             MOVZL   1,1     ;SET UP NEXT TEST
21
22                  ;AC0=0 COMING INTO TEST IT SHD NEG TO =0
23                  ;CARRY IT SHROUGH BIT 0 AND SHOULD COM CRY
24
25 04247 110404 NEG19:      NEG     0,2,SZR ;-0+1=0
26 04250 063077             HALT            ;SEE AC2 NOT=0
27 04251 155000             MOV     2,3
28 04252 136000             ADC     1,3
29 04253 174004             COM     3,3,SZR ;SKP AC2 REALLY=0
30 04254 063077             HALT            ;SEE AC2 SHD =0
31
32                          ;AC2 =0 IT SHD BNEGATE TO =0- IN AC3
33 04255 154400 NG19A:      NEG     2,3
34 04256 116000             ADC     0,3
35 04257 174014             COM#    3,3,SZR
36 04260 063077             HALT            ;0 DID NOT NEG TO 0
37                          ;EXAMINE AC3 FOR ALU FAILURE SD =-1 CREATED BY ADC OF 0
38
39                  ;NEGATING 0 SHOULD COMPLIMENT CRY 0 TO 1
40 04261 102000 NEG20:      ADC     0,0
41 04262 100040             COMO    0,0
42 04263 100423             NEGZ    0,0,SNC
43 04264 063077             HALT            ;NEG 0 DID NOT SET CRY
44
45                  ;NEGATING 0 SHOULD COM CRY 1 TO 0
46 04265 102000 NEG21:      ADC     0,0
47 04266 100020             COMZ    0,0
48 04267 100442             NEGO    0,0,SZC
49 04270 063077             HALT            ;NEG 0 DID NOT CLR CRY
```

```
;0148 ,MAIN
01
02                ;TEST FOR EXISTANCE OF SUB INSTRUCTION
03                ;FIRST TIME FOR SUB
04
05 04271 102000 SUB00:  ADC     0,0       ;AC0=-1
06 04272 102404         SUB     0,0,SZR   ;SUB -1 FROM -1
07 04273 063077         HALT              ;EXAMINE AC0 FOR ERR SHD=0
08
09                      ;SUBTRACT +1 FROM +1 CHECK FOR 0 RESULT (2ND SUB)
10 04274 102000 SUB01:  ADC     0,0
11 04275 100405         NEG     0,0,SNR   ;SET AC0=+1
12 04276 063077         HALT              ;SET UP FAILED AC0 SHD=+1
13 04277 102404         SUB     0,0,SZR   ;+1-+1 SHD=0
14 04300 063077         HALT              ;SUB +1-+1 FAILED SEE AC0
15
16                ;DEFINE SUBTRACT "SUR" TEST MACRO
17
18                      .MACRO SUBTS
19                      ;AC0=12 COMING INTO THIS TEST 12-12 SHOULD=0
20                      ;RESULT 0-12 NEGATED-12 SHD=0 INTO AC3
21                ;SUB11:
22                      MOVO    0,1
23                      SUBZ    0,1,SZR
24                      HALT              ;12-12 SEE AC1 SHD=0
25                      MOV     0,0,SBN   ;0 CRY SHD =1 FROM CRYOUT
26                      HALT              ;AC0=12(?) CRY SHD=1
27                      ADC     2,2
28                      COM     2,2       ;MAKE AC2=0 FOR TEST
29                                        ;0-T2 SHOULD=-12 NEGATED TO AC3
30                      SUB     0,2       ;0-T2
31                      NEGZ    2,3       ;NEGATED SHD=12
32                      SUBO    0,3,SZR   ;12-12 SHD=0 AGAIN
33                      HALT
34                      MOV     0,0,SZC   ;CRY SHD COMP 1 TO 0
35                      HALT              ;CRY OUT FAILED
36                      MOVZL   0,0       ;SET UP NEXT TEST
37                .
38                  ;SET UP SUBTRACT TESTS
39 04301 102000         ADC     0,0
40 04302 100140         COMOL   0,0
41
42                      SUBTS 02,1
43                      ;AC0=1 COMING INTO THIS TEST 1-1 SHOULD=0
44                      ;RESULT 0-1 NEGATED-1 SHD=0 INTO AC3
45                ;SUB02:
46 04303 105040         MOVO    0,1
47 04304 106424         SUBZ    0,1,SZR
48 04305 063077         HALT              ;1-1 SEE AC1 SHD=0
49 04306 101007         MOV     0,0,SBN   ;0 CRY SHD =1 FROM CRYOUT
50 04307 063077         HALT              ;AC0=1(?) CRY SHD=1
51 04310 152000         ADC     2,2
52 04311 150000         COM     2,2       ;MAKE AC2=0 FOR TEST
53                                        ;0-1 SHOULD=-1 NEGATED TO AC3
54 04312 112400         SUB     0,2       ;0-1
55 04313 154420         NEGZ    2,3       ;NEGATED SHD=1
56 04314 116444         SUBO    0,3,SZR   ;1-1 SHD=0 AGAIN
57 04315 063077         HALT
58 04316 101002         MOV     0,0,SZC   ;CRY SHD COMP 1 TO 0
59 04317 063077         HALT              ;CRY OUT FAILED
60 04320 101120         MOVZL   0,0       ;SET UP NEXT TEST
```

```
 0149 .MAIN
01
02                              SUBTS   03,2
03                              ;AC0=2 COMING INTO THIS TEST 2-2 SHOULD=0
04                              ;RESULT 0-2 NEGATED-2 SHD=0 INTO AC3
05                      ;SUB03:
06 04321 105040                 MOVO    0,1
07 04322 106424                 SUBZ    0,1,SZR
08 04323 063077                 HALT                ;2-2 SEE AC1 SHD=0
09 04324 101007                 MOV     0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
10 04325 063077                 HALT                ;AC0=2(?) CRY SHD=1
11 04326 152000                 ADC     2,2
12 04327 150000                 COM     2,2         ;MAKE AC2=0 FOR TEST
13                                                  ;0-2 SHOULD=-2 NEGATED TO AC3
14 04330 112400                 SUB     0,2         ;0-2
15 04331 154420                 NEGZ    2,3         ;NEGATED SHD=2
16 04332 116444                 SUBO    0,3,SZR     ;2-2 SHD=0 AGAIN
17 04333 063077                 HALT
18 04334 101002                 MOV     0,0,SZC     ;CRY SHD COMP 1 TO 0
19 04335 063077                 HALT                ;CRY OUT FAILED
20 04336 101120                 MOVZL   0,0         ;SET UP NEXT TEST
21
22                              SUBTS 04,4
23                              ;AC0=4 COMING INTO THIS TEST 4-4 SHOULD=0
24                              ;RESULT 0-4 NEGATED-4 SHD=0 INTO AC3
25                      ;SUB04:
26 04337 105040                 MOVO    0,1
27 04340 106424                 SUBZ    0,1,SZR
28 04341 063077                 HALT                ;4-4 SEE AC1 SHD=0
29 04342 101007                 MOV     0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
   04343 063077                 HALT                ;AC0=4(?) CRY SHD=1
   04344 152000                 ADC     2,2
   04345 150000                 COM     2,2         ;MAKE AC2=0 FOR TEST
                                                    ;0-4 SHOULD=-4 NEGATED TO AC3
   04346 112400                 SUB     0,2         ;0-4
   04347 154420                 NEGZ    2,3         ;NEGATED SHD=4
36 04350 116444                 SUBO    0,3,SZR     ;4-4 SHD=0 AGAIN
37 04351 063077                 HALT
38 04352 101002                 MOV     0,0,SZC     ;CRY SHD COMP 1 TO 0
39 04353 063077                 HALT                ;CRY OUT FAILED
40 04354 101120                 MOVZL   0,0         ;SET UP NEXT TEST
41
42                              SUBTS 05,10
43                              ;AC0=10 COMING INTO THIS TEST 10-10 SHOULD=0
44                              ;RESULT 0-10 NEGATED-10 SHD=0 INTO AC3
45                      ;SUB05:
46 04355 105040                 MOVO    0,1
47 04356 106424                 SUBZ    0,1,SZR
48 04357 063077                 HALT                ;10-10 SEE AC1 SHD=0
49 04360 101007                 MOV     0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
50 04361 063077                 HALT                ;AC0=10(?) CRY SHD=1
51 04362 152000                 ADC     2,2
52 04363 150000                 COM     2,2         ;MAKE AC2=0 FOR TEST
53                                                  ;0-10 SHOULD=-10 NEGATED TO AC3
54 04364 112400                 SUB     0,2         ;0-10
55 04365 154420                 NEGZ    2,3         ;NEGATED SHD=10
56 04366 116444                 SUBO    0,3,SZR     ;10-10 SHD=0 AGAIN
57 04367 063077                 HALT
58 04370 101002                 MOV     0,0,SZC     ;CRY SHD COMP 1 TO 0
59 04371 063077                 HALT                ;CRY OUT FAILED
60 04372 101120                 MOVZL   0,0         ;SET UP NEXT TEST
```

```
 0150 .MAIN
01
02                              SUBTS 06,20
03                              ;AC0=20 COMING INTO THIS TEST 20-20 SHOULD=0
04                              ;RESULT 0-20 NEGATED-20 SHD=0 INTO AC3
05                      ;SUB06:
06 04373 105040                 MOVO    0,1
07 04374 106424                 SUBZ    0,1,SZR
08 04375 063077                 HALT                    ;20-20 SEE AC1 SHD=0
09 04376 101007                 MOV     0,0,SBN ;0 CRY SHD =1 FROM CRYOUT
10 04377 063077                 HALT                    ;AC0=20(?) CRY SHD=1
11 04400 152000                 ADC     2,2
12 04401 150000                 COM     2,2     ;MAKE AC2=0 FOR TEST
13                                              ;0-20 SHOULD=-20 NEGATED TO AC3
14 04402 112400                 SUB     0,2     ;0-20
15 04403 154420                 NEGZ    2,3     ;NEGATED SHD=20
16 04404 116444                 SUBO    0,3,SZR ;20-20 SHD=0 AGAIN
17 04405 063077                 HALT
18 04406 101002                 MOV     0,0,SZC ;CRY SHD COMP 1 TO 0
19 04407 063077                 HALT                    ;CRY OUT FAILED
20 04410 101120                 MOVZL   0,0     ;SET UP NEXT TEST
21
22                              SUBTS 07,40
23                              ;AC0=40 COMING INTO THIS TEST 40-40 SHOULD=0
24                              ;RESULT 0-40 NEGATED-40 SHD=0 INTO AC3
25                      ;SUB07:
26 04411 105040                 MOVO    0,1
27 04412 106424                 SUBZ    0,1,SZR
28 04413 063077                 HALT                    ;40-40 SEE AC1 SHD=0
29 04414 101007                 MOV     0,0,SBN ;0 CRY SHD =1 FROM CRYOUT
30 04415 063077                 HALT                    ;AC0=40(?) CRY SHD=1
31 04416 152000                 ADC     2,2
32 04417 150000                 COM     2,2     ;MAKE AC2=0 FOR TEST
33                                              ;0-40 SHOULD=-40 NEGATED TO AC3
34 04420 112400                 SUB     0,2     ;0-40
35 04421 154420                 NEGZ    2,3     ;NEGATED SHD=40
36 04422 116444                 SUBO    0,3,SZR ;40-40 SHD=0 AGAIN
37 04423 063077                 HALT
38 04424 101002                 MOV     0,0,SZC ;CRY SHD COMP 1 TO 0
39 04425 063077                 HALT                    ;CRY OUT FAILED
40 04426 101120                 MOVZL   0,0     ;SET UP NEXT TEST
41
42                              SUBTS 08,100
43                              ;AC0=100 COMING INTO THIS TEST 100-100 SHOULD=0
44                              ;RESULT 0-100 NEGATED-100 SHD=0 INTO AC3
45                      ;SUB08:
46 04427 105040                 MOVO    0,1
47 04430 106424                 SUBZ    0,1,SZR
48 04431 063077                 HALT                    ;100-100 SEE AC1 SHD=0
49 04432 101007                 MOV     0,0,SBN ;0 CRY SHD =1 FROM CRYOUT
50 04433 063077                 HALT                    ;AC0=100(?) CRY SHD=1
51 04434 152000                 ADC     2,2
52 04435 150000                 COM     2,2     ;MAKE AC2=0 FOR TEST
53                                              ;0-100 SHOULD=-100 NEGATED TO AC3
54 04436 112400                 SUB     0,2     ;0-100
55 04437 154420                 NEGZ    2,3     ;NEGATED SHD=100
56 04440 116444                 SUBO    0,3,SZR ;100-100 SHD=0 AGAIN
57 04441 063077                 HALT
58 04442 101002                 MOV     0,0,SZC ;CRY SHD COMP 1 TO 0
59 04443 063077                 HALT                    ;CRY OUT FAILED
60 04444 101120                 MOVZL   0,0     ;SET UP NEXT TEST
```

```
 0151 .MAIN
01
02                          SUBTS 09,200
03                          ;AC0=200 COMING INTO THIS TEST 200-200 SHOULD=0
04                          ;RESULT 0-200 NEGATED-200 SHD=0 INTO AC3
05                    ;SUB09:
06 04445 105040             MOVO    0,1
07 04446 106424             SUBZ    0,1,SZR
08 04447 063077             HALT                ;200-200 SEE AC1 SHD=0
09 04450 101007             MOV     0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
10 04451 063077             HALT                ;AC0=200(?) CRY SHD=1
11 04452 152000             ADC     2,2
12 04453 150000             COM     2,2         ;MAKE AC2=0 FOR TEST
13                                              ;0-200 SHOULD=-200 NEGATED TO AC3
14 04454 112400             SUB     0,2         ;0-200
15 04455 154420             NEGZ    2,3         ;NEGATED SHD=200
16 04456 116444             SUBO    0,3,SZR     ;200-200 SHD=0 AGAIN
17 04457 063077             HALT
18 04460 101002             MOV     0,0,SZC     ;CRY SHD COMP 1 TO 0
19 04461 063077             HALT                ;CRY OUT FAILED
20 04462 101120             MOVZL   0,0         ;SET UP NEXT TEST
21
22                          SUBTS 10,400
23                          ;AC0=400 COMING INTO THIS TEST 400-400 SHOULD=0
24                          ;RESULT 0-400 NEGATED-400 SHD=0 INTO AC3
25                    ;SUB10:
26 04463 105040             MOVO    0,1
27 04464 106424             SUBZ    0,1,SZR
28 04465 063077             HALT                ;400-400 SEE AC1 SHD=0
29 04466 101007             MOV     0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
30 04467 063077             HALT                ;AC0=400(?) CRY SHD=1
31 04470 152000             ADC     2,2
32 04471 150000             COM     2,2         ;MAKE AC2=0 FOR TEST
33                                              ;0-400 SHOULD=-400 NEGATED TO AC3
34 04472 112400             SUB     0,2         ;0-400
35 04473 154420             NEGZ    2,3         ;NEGATED SHD=400
36 04474 116444             SUBO    0,3,SZR     ;400-400 SHD=0 AGAIN
37 04475 063077             HALT
38 04476 101002             MOV     0,0,SZC     ;CRY SHD COMP 1 TO 0
39 04477 063077             HALT                ;CRY OUT FAILED
40 04500 101120             MOVZL   0,0         ;SET UP NEXT TEST
41
42                          SUBTS 11,1000
43                          ;AC0=1000 COMING INTO THIS TEST 1000-1000 SHOULD=0
44                          ;RESULT 0-1000 NEGATED-1000 SHD=0 INTO AC3
45                    ;SUB11:
46 04501 105040             MOVO    0,1
47 04502 106424             SUBZ    0,1,SZR
48 04503 063077             HALT                ;1000-1000 SEE AC1 SHD=0
49 04504 101007             MOV     0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
50 04505 063077             HALT                ;AC0=1000(?) CRY SHD=1
51 04506 152000             ADC     2,2
52 04507 150000             COM     2,2         ;MAKE AC2=0 FOR TEST
53                                              ;0-1000 SHOULD=-1000 NEGATED TO AC3
54 04510 112400             SUB     0,2         ;0-1000
55 04511 154420             NEGZ    2,3         ;NEGATED SHD=1000
56 04512 116444             SUBO    0,3,SZR     ;1000-1000 SHD=0 AGAIN
57 04513 063077             HALT
58 04514 101002             MOV     0,0,SZC     ;CRY SHD COMP 1 TO 0
59 04515 063077             HALT                ;CRY OUT FAILED
60 04516 101120             MOVZL   0,0         ;SET UP NEXT TEST
```

```
 0152 .MAIN
 01
 02                     SUBTS 12,2000
 03                     ;AC0=2000 COMING INTO THIS TEST 2000-2000 SHOULD=0
 04                     ;RESULT 0-2000 NEGATED-2000 SHD=0 INTO AC3
 05                ;SUB12:
 06 04517 105040        MOVO    0,1
 07 04520 106424        SUBZ    0,1,SZR
 08 04521 063077        HALT            ;2000-2000 SEE AC1 SHD=0
 09 04522 101007        MOV     0,0,SBN ;0 CRY SHD =1 FROM CRYOUT
 10 04523 063077        HALT            ;AC0=2000(?) CRY SHD=1
 11 04524 152000        ADC     2,2
 12 04525 150000        COM     2,2     ;MAKE AC2=0 FOR TEST
 13                                     ;0-2000 SHOULD=-2000 NEGATED TO AC3
 14 04526 112400        SUB     0,2     ;0-2000
 15 04527 154420        NEGZ    2,3     ;NEGATED SHD=2000
 16 04530 116444        SUBO    0,3,SZR ;2000-2000 SHD=0 AGAIN
 17 04531 063077        HALT
 18 04532 101002        MOV     0,0,SZC ;CRY SHD COMP 1 TO 0
 19 04533 063077        HALT            ;CRY OUT FAILED
 20 04534 101120        MOVZL   0,0     ;SET UP NEXT TEST
 21
 22                     SUBTS 13,4000
 23                     ;AC0=4000 COMING INTO THIS TEST 4000-4000 SHOULD=0
 24                     ;RESULT 0-4000 NEGATED-4000 SHD=0 INTO AC3
 25                ;SUB13:
 26 04535 105040        MOVO    0,1
 27 04536 106424        SUBZ    0,1,SZR
 28 04537 063077        HALT            ;4000-4000 SEE AC1 SHD=0
 29 04540 101007        MOV     0,0,SBN ;0 CRY SHD =1 FROM CRYOUT
 30 04541 063077        HALT            ;AC0=4000(?) CRY SHD=1
 31 04542 152000        ADC     2,2
 32 04543 150000        COM     2,2     ;MAKE AC2=0 FOR TEST
 33                                     ;0-4000 SHOULD=-4000 NEGATED TO AC3
 34 04544 112400        SUB     0,2     ;0-4000
 35 04545 154420        NEGZ    2,3     ;NEGATED SHD=4000
 36 04546 116444        SUBO    0,3,SZR ;4000-4000 SHD=0 AGAIN
 37 04547 063077        HALT
 38 04550 101002        MOV     0,0,SZC ;CRY SHD COMP 1 TO 0
 39 04551 063077        HALT            ;CRY OUT FAILED
 40 04552 101120        MOVZL   0,0     ;SET UP NEXT TEST
 41
 42                     SUBTS 14,10000
 43                     ;AC0=10000 COMING INTO THIS TEST 10000-10000 SHOULD=0
 44                     ;RESULT 0-10000 NEGATED-10000 SHD=0 INTO AC3
 45                ;SUB14:
 46 04553 105040        MOVO    0,1
 47 04554 106424        SUBZ    0,1,SZR
 48 04555 063077        HALT            ;10000-10000 SEE AC1 SHD=0
 49 04556 101007        MOV     0,0,SBN ;0 CRY SHD =1 FROM CRYOUT
 50 04557 063077        HALT            ;AC0=10000(?) CRY SHD=1
 51 04560 152000        ADC     2,2
 52 04561 150000        COM     2,2     ;MAKE AC2=0 FOR TEST
 53                                     ;0-10000 SHOULD=-10000 NEGATED TO AC3
 54 04562 112400        SUB     0,2     ;0-10000
 55 04563 154420        NEGZ    2,3     ;NEGATED SHD=10000
 56 04564 116444        SUBO    0,3,SZR ;10000-10000 SHD=0 AGAIN
 57 04565 063077        HALT
 58 04566 101002        MOV     0,0,SZC ;CRY SHD COMP 1 TO 0
 59 04567 063077        HALT            ;CRY OUT FAILED
 60 04570 101120        MOVZL   0,0     ;SET UP NEXT TEST
```

```
 0153 .MAIN
01
02                              SUBTS 15,20000
03                              ;AC0=20000 COMING INTO THIS TEST 20000-20000 SHOULD=
04                              ;RESULT 0-20000 NEGATED-20000 SHD=0 INTO AC3
05                      ;SUB15:
06 04571 105040                 MOVO    0,1
07 04572 106424                 SUBZ    0,1,SZR
08 04573 063077                 HALT                ;20000-20000 SEE AC1 SHD=0
09 04574 101007                 MOV     0,0,SBN ;0 CRY SHD =1 FROM CRYOUT
10 04575 063077                 HALT                ;AC0=20000(?) CRY SHD=1
11 04576 152000                 ADC     2,2
12 04577 150000                 COM     2,2         ;MAKE AC2=0 FOR TEST
13                                                  ;0-20000 SHOULD=-20000 NEGATED TO AC3
14 04600 112400                 SUB     0,2         ;0-20000
15 04601 154420                 NEGZ    2,3         ;NEGATED SHD=20000
16 04602 116444                 SUBO    0,3,SZR ;20000-20000 SHD=0 AGAIN
17 04603 063077                 HALT
18 04604 101002                 MOV     0,0,SZC ;CRY SHD COMP 1 TO 0
19 04605 063077                 HALT                ;CRY OUT FAILED
20 04606 101120                 MOVZL   0,0         ;SET UP NEXT TEST
21
22                              SUBTS 16,40000
23                              ;AC0=40000 COMING INTO THIS TEST 40000-40000 SHOULD=
24                              ;RESULT 0-40000 NEGATED-40000 SHD=0 INTO AC3
25                      ;SUB16:
26 04607 105040                 MOVO    0,1
27 04610 106424                 SUBZ    0,1,SZR
28 04611 063077                 HALT                ;40000-40000 SEE AC1 SHD=0
29 04612 101007                 MOV     0,0,SBN ;0 CRY SHD =1 FROM CRYOUT
30 04613 063077                 HALT                ;AC0=40000(?) CRY SHD=1
31 04614 152000                 ADC     2,2
32 04615 150000                 COM     2,2         ;MAKE AC2=0 FOR TEST
33                                                  ;0-40000 SHOULD=-40000 NEGATED TO AC3
34 04616 112400                 SUB     0,2         ;0-40000
35 04617 154420                 NEGZ    2,3         ;NEGATED SHD=40000
36 04620 116444                 SUBO    0,3,SZR ;40000-40000 SHD=0 AGAIN
37 04621 063077                 HALT
38 04622 101002                 MOV     0,0,SZC ;CRY SHD COMP 1 TO 0
39 04623 063077                 HALT                ;CRY OUT FAILED
40 04624 101120                 MOVZL   0,0         ;SET UP NEXT TEST
41
42                              SUBTS 17,100000
43                              ;AC0=100000 COMING INTO THIS TEST 100000-100000 SHOULD=0
44                              ;RESULT 0-100000 NEGATED-100000 SHD=0 INTO AC3
45                      ;SUB17:
46 04625 105040                 MOVO    0,1
47 04626 106424                 SUBZ    0,1,SZR
48 04627 063077                 HALT                ;100000-100000 SEE AC1 SHD=0
49 04630 101007                 MOV     0,0,SBN ;0 CRY SHD =1 FROM CRYOUT
50 04631 063077                 HALT                ;AC0=100000(?) CRY SHD=1
51 04632 152000                 ADC     2,2
52 04633 150000                 COM     2,2         ;MAKE AC2=0 FOR TEST
53                                                  ;0-100000 SHOULD=-100000 NEGATED TO AC3
54 04634 112400                 SUB     0,2         ;0-100000
55 04635 154420                 NEGZ    2,3         ;NEGATED SHD=100000
56 04636 116444                 SUBO    0,3,SZR ;100000-100000 SHD=0 AGAIN
57 04637 063077                 HALT
58 04640 101002                 MOV     0,0,SZC ;CRY SHD COMP 1 TO 0
59 04641 063077                 HALT                ;CRY OUT FAILED
60 04642 101120                 MOVZL   0,0         ;SET UP NEXT TEST
```

```
 0154 .MAIN
01
02                ;TAPE 5
03
04                ;LOAD ACCUMULATOR TESTS FIRST MRI FIRST LDA
05                ;IF LDA HANGS TRY SETFETCH OR PTGHOLD ROM 0
06
07 04643 102400 LDA00:  SUB     0,0
08 04644 105040          MOVO    0,1
09 04645 020135          LDA     0,K1
10 04646 101005          MOV     0,0,SNR
11 04647 063077          HALT             ;DID NOT LOAD AC0 WITH+1
12 04650 105234          MOVZR#  0,1,SZR  ;CHECK AC0 TO TEALLY=+1
13 04651 063077          HALT             ;SEE AC0 NOT=+1
14
15                       ;FIRST USE OF MRI OR LDA INSTRUCTION
16                       ;INCORRECT RESULT IN AC0 COULD BE DUE TO ANY OF
17                       ;A VARIETY OF PROBLEMS INCLUDING EFA
18                       ;IF MRI DOES NOT SET ALC INSTRUCTION DECODES AS COMZ 1,0
19                       ;AC0 WILL=-1 AND CARRY WILL=0
20                       ;IF INSTRUCTION DECODES AS I/O IT='S NTO 40(AC0=0)
21                       ;IF DATA IN AC0 IS OTHER THAN 0 OR -1 EFA
22
23                ;DEFINE MACRO TO VERIFY LDA DOES NOT DISTURB OTHER AC'S
24
25                       .MACRO LDAT1
26                LDA11: ADC     13,13    ;SET AC13=-1
27                       LDA     12,K1    ;LOAD +1 TO AC12
28                       COM     13,13,SZR        ;AC13 SHD STILL=-1
29                       HALT             ;LDA OF AC12 DIST AC13
30                %
31
32                       LDAT1 01,0,1
33 04652 126000 LDA01:  ADC     1,1      ;SET AC1=-1
34 04653 020135          LDA     0,K1     ;LOAD +1 TO AC0
35 04654 124004          COM     1,1,SZR  ;AC1 SHD STILL=-1
36 04655 063077          HALT             ;LDA OF AC0 DIST AC1
37
38                       LDAT1 02,0,2
39 04656 152000 LDA02:  ADC     2,2      ;SET AC2=-1
40 04657 020135          LDA     0,K1     ;LOAD +1 TO AC0
41 04660 150004          COM     2,2,SZR  ;AC2 SHD STILL=-1
42 04661 063077          HALT             ;LDA OF AC0 DIST AC2
43
44                       LDAT1 03,0,3
45 04662 176000 LDA03:  ADC     3,3      ;SET AC3=-1
46 04663 020135          LDA     0,K1     ;LOAD +1 TO AC0
47 04664 174004          COM     3,3,SZR  ;AC3 SHD STILL=-1
48 04665 063077          HALT             ;LDA OF AC0 DIST AC3
49
50                       LDAT1 04,1,0
51 04666 102000 LDA04:  ADC     0,0      ;SET AC0=-1
52 04667 024135          LDA     1,K1     ;LOAD +1 TO AC1
53 04670 100004          COM     0,0,SZR  ;AC0 SHD STILL=-1
54 04671 063077          HALT             ;LDA OF AC1 DIST AC0
55
56                       LDAT1 05,1,2
57 04672 152000 LDA05:  ADC     2,2      ;SET AC2=-1
58 04673 024135          LDA     1,K1     ;LOAD +1 TO AC1
59 04674 150004          COM     2,2,SZR  ;AC2 SHD STILL=-1
60 04675 063077          HALT             ;LDA OF AC1 DIST AC2
```

```
 0155 .MAIN
 01
 02                             LDAT1 06,1,3
 03 04676 176000 LDA06:  ADC      3,3      ;SET AC3=-1
 04 04677 024135         LDA      1,K1     ;LOAD +1 TO AC1
 05 04700 174004         COM      3,3,SZR  ;AC3 SHD STILL=-1
 06 04701 063077         HALT              ;LDA OF AC1 DIST AC3
 07
 08                             LDAT1 07,2,0
 09 04702 102000 LDA07:  ADC      0,0      ;SET AC0=-1
 10 04703 030135         LDA      2,K1     ;LOAD +1 TO AC2
 11 04704 100004         COM      0,0,SZR  ;AC0 SHD STILL=-1
 12 04705 063077         HALT              ;LDA OF AC2 DIST AC0
 13
 14                             LDAT1 08,2,1
 15 04706 126000 LDA08:  ADC      1,1      ;SET AC1=-1
 16 04707 030135         LDA      2,K1     ;LOAD +1 TO AC2
 17 04710 124004         COM      1,1,SZR  ;AC1 SHD STILL=-1
 18 04711 063077         HALT              ;LDA OF AC2 DIST AC1
 19
 20                             LDAT1 09,2,3
 21 04712 176000 LDA09:  ADC      3,3      ;SET AC3=-1
 22 04713 030135         LDA      2,K1     ;LOAD +1 TO AC2
 23 04714 174004         COM      3,3,SZR  ;AC3 SHD STILL=-1
 24 04715 063077         HALT              ;LDA OF AC2 DIST AC3
 25
 26                             LDAT1 10,3,0
 27 04716 102000 LDA10:  ADC      0,0      ;SET AC0=-1
 28 04717 034135         LDA      3,K1     ;LOAD +1 TO AC3
 29 04720 100004         COM      0,0,SZR  ;AC0 SHD STILL=-1
 30 04721 063077         HALT              ;LDA OF AC3 DIST AC0
 31
 32                             LDAT1 11,3,1
 33 04722 126000 LDA11:  ADC      1,1      ;SET AC1=-1
 34 04723 034135         LDA      3,K1     ;LOAD +1 TO AC3
 35 04724 124004         COM      1,1,SZR  ;AC1 SHD STILL=-1
 36 04725 063077         HALT              ;LDA OF AC3 DIST AC1
 37
 38                             LDAT1 12,3,2
 39 04726 152000 LDA12:  ADC      2,2      ;SET AC2=-1
 40 04727 034135         LDA      3,K1     ;LOAD +1 TO AC3
 41 04730 150004         COM      2,2,SZR  ;AC2 SHD STILL=-1
 42 04731 063077         HALT              ;LDA OF AC3 DIST AC2
```

```
;0156 .MAIN
01
02                ;DEFINE MACRO TO FURTHER TEST LDA INST
03                        .MACRO LDAT2
04                        ;SINGLE BIT LOAD TEST
05
06                ;LDA11:
07                        LDA     1,I2    ;GET 13 TO AC
08                        MOV     1,2
09                        SUB     0,2,SZR ;AC0=13 COMING INTO TEST
10                        HALT
11                        MOVZL   0,0     ;POSITION FOR NEXT TEST
12                %
13
14
15 04732 102525           SUBZL   0,0,SNR ;SET UP LDA     TESTS
16 04733 063077           HALT            ;SET UP FAILED SEE AC0
17
18
19
20
21                        LDAT2 13,K1,1
22                        ;SINGLE BIT LOAD TEST
23
24                ;LDA13:
25 04734 024135           LDA     1,K1    ;GET 1 TO AC
26 04735 131000           MOV     1,2
27 04736 112404           SUB     0,2,SZR ;AC0=1 COMING INTO TEST
28 04737 063077           HALT
29 04740 101120           MOVZL   0,0     ;POSITION FOR NEXT TEST
30
31                        LDAT2 14,K2,2
32                        ;SINGLE BIT LOAD TEST
33
34                ;LDA14:
35 04741 024136           LDA     1,K2    ;GET 2 TO AC
36 04742 131000           MOV     1,2
37 04743 112404           SUB     0,2,SZR ;AC0=2 COMING INTO TEST
38 04744 063077           HALT
39 04745 101120           MOVZL   0,0     ;POSITION FOR NEXT TEST
40
41                        LDAT2 15,K4,4
42                        ;SINGLE BIT LOAD TEST
43
44                ;LDA15:
45 04746 024137           LDA     1,K4    ;GET 4 TO AC
46 04747 131000           MOV     1,2
47 04750 112404           SUB     0,2,SZR ;AC0=4 COMING INTO TEST
48 04751 063077           HALT
49 04752 101120           MOVZL   0,0     ;POSITION FOR NEXT TEST
50
51                        LDAT2 16,K10,10
52                        ;SINGLE BIT LOAD TEST
53
54                ;LDA16:
55 04753 024140           LDA     1,K10   ;GET 10 TO AC
56 04754 131000           MOV     1,2
57 04755 112404           SUB     0,2,SZR ;AC0=10 COMING INTO TEST
58 04756 063077           HALT
59 04757 101120           MOVZL   0,0     ;POSITION FOR NEXT TEST
60
```

```
 0157 .MAIN
01                      LDAT2 17,K20,20
02                      ;SINGLE BIT LOAD TEST
03
04                ;LDA17:
05 04760 024141         LDA     1,K20   ;GET 20 TO AC
06 04761 131000         MOV     1,2
07 04762 112404         SUB     0,2,SZR ;AC0=20 COMING INTO TEST
08 04763 063077         HALT
09 04764 101120         MOVZL   0,0     ;POSITION FOR NEXT TEST
10
11                      LDAT2 18,K40,40
12                      ;SINGLE BIT LOAD TEST
13
14                ;LDA18:
15 04765 024142         LDA     1,K40   ;GET 40 TO AC
16 04766 131000         MOV     1,2
17 04767 112404         SUB     0,2,SZR ;AC0=40 COMING INTO TEST
18 04770 063077         HALT
19 04771 101120         MOVZL   0,0     ;POSITION FOR NEXT TEST
20
21                      LDAT2 19,K100,100
22                      ;SINGLE BIT LOAD TEST
23
24                ;LDA19:
25 04772 024143         LDA     1,K100  ;GET 100 TO AC
26 04773 131000         MOV     1,2
27 04774 112404         SUB     0,2,SZR ;AC0=100 COMING INTO TEST
28 04775 063077         HALT
29 04776 101120         MOVZL   0,0     ;POSITION FOR NEXT TEST
30
31                      LDAT2 20,K200,200
32                      ;SINGLE BIT LOAD TEST
33
34                ;LDA20:
35 04777 024144         LDA     1,K200  ;GET 200 TO AC
36 05000 131000         MOV     1,2
37 05001 112404         SUB     0,2,SZR ;AC0=200 COMING INTO TEST
38 05002 063077         HALT
39 05003 101120         MOVZL   0,0     ;POSITION FOR NEXT TEST
40
41                      LDAT2 21,K400,400
42                      ;SINGLE BIT LOAD TEST
43
44                ;LDA21:
45 05004 024145         LDA     1,K400  ;GET 400 TO AC
46 05005 131000         MOV     1,2
47 05006 112404         SUB     0,2,SZR ;AC0=400 COMING INTO TEST
48 05007 063077         HALT
49 05010 101120         MOVZL   0,0     ;POSITION FOR NEXT TEST
50
51                      LDAT2 22,K1000,1000
52                      ;SINGLE BIT LOAD TEST
53
54                ;LDA22:
55 05011 024146         LDA     1,K1000 ;GET 1000 TO AC
56 05012 131000         MOV     1,2
57 05013 112404         SUB     0,2,SZR ;AC0=1000 COMING INTO TEST
58 05014 063077         HALT
59 05015 101120         MOVZL   0,0     ;POSITION FOR NEXT TEST
60
```

```
 0158 ,MAIN
01                      LDAT2 23,K2000,2000
02                      ;SINGLE BIT LOAD TEST
03
04                ;LDA23:
05 05016 024147         LDA     1,K2000 ;GET 2000 TO AC
06 05017 131000         MOV     1,2
07 05020 112404         SUB     0,2,SZR ;AC0=2000 COMING INTO TEST
08 05021 063077         HALT
09 05022 101120         MOVZL   0,0     ;POSITION FOR NEXT TEST
10
11                      LDAT2 24,K4000,4000
12                      ;SINGLE BIT LOAD TEST
13
14                ;LDA24:
15 05023 024150         LDA     1,K4000 ;GET 4000 TO AC
16 05024 131000         MOV     1,2
17 05025 112404         SUB     0,2,SZR ;AC0=4000 COMING INTO TEST
18 05026 063077         HALT
19 05027 101120         MOVZL   0,0     ;POSITION FOR NEXT TEST
20
21                      LDAT2 25,K10K,10000
22                      ;SINGLE BIT LOAD TEST
23
24                ;LDA25:
25 05030 024151         LDA     1,K10K  ;GET 10000 TO AC
26 05031 131000         MOV     1,2
27 05032 112404         SUB     0,2,SZR ;AC0=10000 COMING INTO TEST
28 05033 063077         HALT
29 05034 101120         MOVZL   0,0     ;POSITION FOR NEXT TEST
30
31                      LDAT2 26,K20K,20000
32                      ;SINGLE BIT LOAD TEST
33
34                ;LDA26:
35 05035 024152         LDA     1,K20K  ;GET 20000 TO AC
36 05036 131000         MOV     1,2
37 05037 112404         SUB     0,2,SZR ;AC0=20000 COMING INTO TEST
38 05040 063077         HALT
39 05041 101120         MOVZL   0,0     ;POSITION FOR NEXT TEST
40
41                      LDAT2 27,K40K,40000
42                      ;SINGLE BIT LOAD TEST
43
44                ;LDA27:
45 05042 024153         LDA     1,K40K  ;GET 40000 TO AC
46 05043 131000         MOV     1,2
47 05044 112404         SUB     0,2,SZR ;AC0=40000 COMING INTO TEST
48 05045 063077         HALT
49 05046 101120         MOVZL   0,0     ;POSITION FOR NEXT TEST
50
51                      LDAT2 28,K100K,100000
52                      ;SINGLE BIT LOAD TEST
53
54                ;LDA28:
55 05047 024154         LDA     1,K100K ;GET 100000 TO AC
56 05050 131000         MOV     1,2
57 05051 112404         SUB     0,2,SZR ;AC0=100000 COMING INTO TEST
58 05052 063077         HALT
59 05053 101120         MOVZL   0,0     ;POSITION FOR NEXT TEST
```

```
10159 .MAIN
01                ;FIRST TEST OF BYTE SWAP "S"
02
03                        ;CALC .1R8,1R9 INTO ALU SHIFTER
04 05054 102745 SWP00:    SUBOS   0,0,SNR
05 05055 101324           MOVZS   0,0,SZR ;FIRST USE FO "S" AC0=0
06 05056 063077           HALT
07 05057 102323 SWP01:    ADCZS   0,0,SNC ;CRY SHD REMAIN=0
08 05060 101302           MOVS    0,0,SZC ;SAME
09 05061 063077           HALT              ;SEE ZC SHIFTER
10 05062 102722 SWP02:    SUBZS   0,0,SZC ;CRY SHD REMAIN=1
11 05063 101303           MOVS    0,0,SNC ;SAME
12 05064 063077           HALT              ;SEE CZ SHIFTER
13 05065 102725 SWP03:    SUBZS   0,0,SNR ;A 1 IN CRY SHD NOT AFFECT "S"
14 05066 101344           MOVOS   0,0,SZR ;TRY SWAP 0'S WITH CRY=1
15 05067 063077           HALT              ;EXAMINE AC0 FOR CRY "S"
16                        ;ERROR DEPENDS ON A 1 IN BIT 0 OR 15 SEE ALU SHIFTER
17
18
19                ;DEFINE SWAP TEST MACRO
20                        .MACRO SWPTS
21
22                        ;TEST SWAP BIT 14 TO BIT 15
23                        ;AC0=16 AC1=17 EXPECTED RESULT IN AC2 IS 17
24                ;SWP11:
25                        LDA     0,12    ;GET 16
26                        LDA     1,13    ;17 EXPECTED RESULT
27                        MOVZS   0,2,SZR ;"S" BIT 14 TO BIT 15
28                        MOV     2,3,SNR
29                        HALT              ;POSS, "ZR" AND FAILURE "S"
30                        SUB     1,3,SZR
31                        HALT              ;"S" BIT 14 TO 15 FAILED EX AC
32                ;SW11A :
33                        COMOS   0,2     ;REPEAT TEST WITH A0
34                        COM     2,3     ;EXPECTED RESULT HERE IS "7
35                        SUB     1,3,SZR
36                        HALT              ;"S" A0 IN BIT 14 TO 15 SEE AC2
37                        ;SW11A TEST SWAP OF COM 16
38
39                %
40
41
42                        SWPTS 04,K1,K400,15,7,1,400
43
44                        ;TEST SWAP BIT 15 TO BIT 7
45                        ;AC0=1 AC1=400 EXPECTED RESULT IN AC2 IS 400
46                ;SWP04:
47 05070 020135           LDA     0,K1    ;GET 1
48 05071 024145           LDA     1,K400  ;400 EXPECTED RESULT
49 05072 111324           MOVZS   0,2,SZR ;"S" BIT 15 TO BIT 7
50 05073 155005           MOV     2,3,SNR
51 05074 063077           HALT              ;POSS, "ZR" AND FAILURE "S"
52 05075 136404           SUB     1,3,SZR
53 05076 063077           HALT              ;"S" BIT 15 TO 7 FAILED EX AC
54                ;SW04A :
55 05077 110340           COMOS   0,2     ;REPEAT TEST WITH A0
56 05100 154000           COM     2,3     ;EXPECTED RESULT HERE IS "7
57 05101 136404           SUB     1,3,SZR
58 05102 063077           HALT              ;"S" A0 IN BIT 15 TO 7 SEE AC2
59                        ;SW04A TEST SWAP OF COM 1
60
```

```
 0160 .MAIN
01
02                      SWPTS 05,K2,K1000,14,6,2,1000
03
04                      ;TEST SWAP BIT 14 TO BIT 6
05                      ;AC0=2 AC1=1000 EXPECTED RESULT IN AC2 IS 1000
06                  ;SWP05:
07 05103 020136         LDA     0,K2    ;GET 2
08 05104 024146         LDA     1,K1000         ;1000 EXPECTED RESULT
09 05105 111324         MOVZS   0,2,SZR ;"S" BIT 14 TO BIT 6
10 05106 155005         MOV     2,3,SNR
11 05107 063077         HALT            ;POSS, "ZR" AND FAILURE "S"
12 05110 136404         SUB     1,3,SZR
13 05111 063077         HALT            ;"S" BIT 14 TO 6 FAILED EX AC
14                  ;SW05A :
15 05112 110340         COMOS   0,2     ;REPEAT TEST WITH A0
16 05113 154000         COM     2,3     ;EXPECTED RESULT HERE IS "7
17 05114 136404         SUB     1,3,SZR
18 05115 063077         HALT            ;"S" A0 IN BIT 14 TO 6 SEE AC2
19                      ;SW05A TEST SWAP OF COM 2
20
21
22                      SWPTS 06,K4,K2000,13,4,2000
23
24                      ;TEST SWAP BIT 13 TO BIT 4
25                      ;AC0=2000 AC1= EXPECTED RESULT IN AC2 IS
26                  ;SWP06:
27 05116 020137         LDA     0,K4    ;GET 2000
28 05117 024147         LDA     1,K2000         ; EXPECTED RESULT
29 05120 111324         MOVZS   0,2,SZR ;"S" BIT 13 TO BIT 4
30 05121 155005         MOV     2,3,SNR
31 05122 063077         HALT            ;POSS, "ZR" AND FAILURE "S"
32 05123 136404         SUB     1,3,SZR
33 05124 063077         HALT            ;"S" BIT 13 TO 4 FAILED EX AC
34                  ;SW06A :
35 05125 110340         COMOS   0,2     ;REPEAT TEST WITH A0
36 05126 154000         COM     2,3     ;EXPECTED RESULT HERE IS "7
37 05127 136404         SUB     1,3,SZR
38 05130 063077         HALT            ;"S" A0 IN BIT 13 TO 4 SEE AC2
39                      ;SW06A TEST SWAP OF COM 2000
40
41
42                      SWPTS 07,K10,K4000,12,4,10,4000
43
44                      ;TEST SWAP BIT 12 TO BIT 4
45                      ;AC0=10 AC1=4000 EXPECTED RESULT IN AC2 IS 4000
46                  ;SWP07:
47 05131 020140         LDA     0,K10   ;GET 10
48 05132 024150         LDA     1,K4000         ;4000 EXPECTED RESULT
49 05133 111324         MOVZS   0,2,SZR ;"S" BIT 12 TO BIT 4
50 05134 155005         MOV     2,3,SNR
51 05135 063077         HALT            ;POSS, "ZR" AND FAILURE "S"
52 05136 136404         SUB     1,3,SZR
53 05137 063077         HALT            ;"S" BIT 12 TO 4 FAILED EX AC
54                  ;SW07A :
55 05140 110340         COMOS   0,2     ;REPEAT TEST WITH A0
56 05141 154000         COM     2,3     ;EXPECTED RESULT HERE IS "7
57 05142 136404         SUB     1,3,SZR
58 05143 063077         HALT            ;"S" A0 IN BIT 12 TO 4 SEE AC2
59                      ;SW07A TEST SWAP OF COM 10
60
```

```
 0161 .MAIN
01
02                      SWPTS 08,K20,K10K,11,3,20,1000
03
04                      ;TEST SWAP BIT 11 TO BIT 3
05                      ;AC0=20 AC1=1000 EXPECTED RESULT IN AC2 IS 1000
06                  ;SWP08:
07 05144 020141         LDA     0,K20   ;GET 20
08 05145 024151         LDA     1,K10K  ;1000 EXPECTED RESULT
09 05146 111324         MOVZS   0,2,SZR ;"S" BIT 11 TO BIT 3
10 05147 155005         MOV     2,3,SNR
11 05150 063077         HALT            ;POSS. "ZR" AND FAILURE "S"
12 05151 136404         SUB     1,3,SZR
13 05152 063077         HALT            ;"S" BIT 11 TO 3 FAILED EX AC
14                  ;SW08A :
15 05153 110340         COMOS   0,2     ;REPEAT TEST WITH A0
16 05154 154000         COM     2,3     ;EXPECTED RESULT HERE IS "7
17 05155 136404         SUB     1,3,SZR
18 05156 063077         HALT            ;"S" A0 IN BIT 11 TO 3 SEE AC2
19                      ;SW08A TEST SWAP OF COM 20
20
21
22                      SWPTS 09,K40,K20K,10,2,40,20000
23
24                      ;TEST SWAP BIT 10 TO BIT 2
25                      ;AC0=40 AC1=20000 EXPECTED RESULT IN AC2 IS 20000
26                  ;SWP09:
27 05157 020142         LDA     0,K40   ;GET 40
28 05160 024152         LDA     1,K20K  ;20000 EXPECTED RESULT
29 05161 111324         MOVZS   0,2,SZR ;"S" BIT 10 TO BIT 2
30 05162 155005         MOV     2,3,SNR
31 05163 063077         HALT            ;POSS. "ZR" AND FAILURE "S"
32 05164 136404         SUB     1,3,SZR
33 05165 063077         HALT            ;"S" BIT 10 TO 2 FAILED EX AC
34                  ;SW09A :
35 05166 110340         COMOS   0,2     ;REPEAT TEST WITH A0
36 05167 154000         COM     2,3     ;EXPECTED RESULT HERE IS "7
37 05170 136404         SUB     1,3,SZR
38 05171 063077         HALT            ;"S" A0 IN BIT 10 TO 2 SEE AC2
39                      ;SW09A TEST SWAP OF COM 40
40
41
42                      SWPTS 10,K100,K40K,9,1,100,40000
43
44                      ;TEST SWAP BIT 9 TO BIT 1
45                      ;AC0=100 AC1=40000 EXPECTED RESULT IN AC2 IS 40000
46                  ;SWP10:
47 05172 020143         LDA     0,K100  ;GET 100
48 05173 024153         LDA     1,K40K  ;40000 EXPECTED RESULT
49 05174 111324         MOVZS   0,2,SZR ;"S" BIT 9 TO BIT 1
50 05175 155005         MOV     2,3,SNR
51 05176 063077         HALT            ;POSS. "ZR" AND FAILURE "S"
52 05177 136404         SUB     1,3,SZR
53 05200 063077         HALT            ;"S" BIT 9 TO 1 FAILED EX AC
54                  ;SW10A :
55 05201 110340         COMOS   0,2     ;REPEAT TEST WITH A0
56 05202 154000         COM     2,3     ;EXPECTED RESULT HERE IS "7
57 05203 136404         SUB     1,3,SZR
58 05204 063077         HALT            ;"S" A0 IN BIT 9 TO 1 SEE AC2
59                      ;SW10A TEST SWAP OF COM 100
60
```

```
 0162 ,MAIN
01
02                          SWPTS 11,K200,K100K,8,0,200,100000
03
04                          ;TEST SWAP BIT 8 TO BIT 0
05                          ;AC0=200 AC1=100000 EXPECTED RESULT IN AC2 IS 100000
06                  ;SWP11:
07 05205 020144             LDA     0,K200  ;GET 200
08 05206 024154             LDA     1,K100K         ;100000 EXPECTED RESULT
09 05207 111324             MOVZS   0,2,SZR ;"S" BIT 8 TO BIT 0
10 05210 155005             MOV     2,3,SNR
11 05211 063077             HALT            ;POSS, "ZR" AND FAILURE "S"
12 05212 136404             SUB     1,3,SZR
13 05213 063077             HALT            ;"S" BIT 8 TO 0 FAILED EX AC
14                  ;SW11A :
15 05214 110340             COMOS   0,2     ;REPEAT TEST WITH A0
16 05215 154000             COM     2,3     ;EXPECTED RESULT HERE IS "7
17 05216 136404             SUB     1,3,SZR
18 05217 063077             HALT            ;"S" A0 IN BIT 8 TO 0 SEE AC2
19                          ;SW11A TEST SWAP OF COM 200
20
21
22                          SWPTS 12,K400,K1,7,15,400,1
23
24                          ;TEST SWAP BIT 7 TO BIT 15
25                          ;AC0=400 AC1=1 EXPECTED RESULT IN AC2 IS 1
26                  ;SWP12:
27 05220 020145             LDA     0,K400  ;GET 400
28 05221 024135             LDA     1,K1    ;1 EXPECTED RESULT
29 05222 111324             MOVZS   0,2,SZR ;"S" BIT 7 TO BIT 15
30 05223 155005             MOV     2,3,SNR
31 05224 063077             HALT            ;POSS, "ZR" AND FAILURE "S"
32 05225 136404             SUB     1,3,SZR
33 05226 063077             HALT            ;"S" BIT 7 TO 15 FAILED EX AC
34                  ;SW12A :
35 05227 110340             COMOS   0,2     ;REPEAT TEST WITH A0
36 05230 154000             COM     2,3     ;EXPECTED RESULT HERE IS "7
37 05231 136404             SUB     1,3,SZR
38 05232 063077             HALT            ;"S" A0 IN BIT 7 TO 15 SEE AC2
39                          ;SW12A TEST SWAP OF COM 400
40
41
42                          SWPTS 13,K1000,K2,6,14,1000,2
43
44                          ;TEST SWAP BIT 6 TO BIT 14
45                          ;AC0=1000 AC1=2 EXPECTED RESULT IN AC2 IS 2
46                  ;SWP13:
47 05233 020146             LDA     0,K1000         ;GET 1000
48 05234 024136             LDA     1,K2    ;2 EXPECTED RESULT
49 05235 111324             MOVZS   0,2,SZR ;"S" BIT 6 TO BIT 14
50 05236 155005             MOV     2,3,SNR
51 05237 063077             HALT            ;POSS, "ZR" AND FAILURE "S"
52 05240 136404             SUB     1,3,SZR
53 05241 063077             HALT            ;"S" BIT 6 TO 14 FAILED EX AC
54                  ;SW13A :
55 05242 110340             COMOS   0,2     ;REPEAT TEST WITH A0
56 05243 154000             COM     2,3     ;EXPECTED RESULT HERE IS "7
57 05244 136404             SUB     1,3,SZR
58 05245 063077             HALT            ;"S" A0 IN BIT 6 TO 14 SEE AC2
59                          ;SW13A TEST SWAP OF COM 1000
60
```

```
 0163 .MAIN
01
02                          SWPTS 14,K2000,K4,5,13,2000,4
03
04                          ;TEST SWAP BIT 5 TO BIT 13
05                          ;AC0=2000 AC1=4 EXPECTED RESULT IN AC2 IS 4
06                    ;SWP14:
07 05246 020147             LDA     0,K2000         ;GET 2000
08 05247 024137             LDA     1,K4    ;4 EXPECTED RESULT
09 05250 111324             MOVZS   0,2,SZR ;"S" BIT 5 TO BIT 13
10 05251 155005             MOV     2,3,SNR
11 05252 063077             HALT                    ;POSS, "ZR" AND FAILURE "S"
12 05253 136404             SUB     1,3,SZR
13 05254 063077             HALT                    ;"S" BIT 5 TO 13 FAILED EX AC
14                    ;SW14A :
15 05255 110340             COMOS   0,2     ;REPEAT TEST WITH A0
16 05256 154000             COM     2,3     ;EXPECTED RESULT HERE IS "7
17 05257 136404             SUB     1,3,SZR
18 05260 063077             HALT                    ;"S" A0 IN BIT 5 TO 13 SEE AC2
19                          ;SW14A TEST SWAP OF COM 2000
20
21
22                          SWPTS 15,K4000,K10,4,12,4000,10
23
24                          ;TEST SWAP BIT 4 TO BIT 12
25                          ;AC0=4000 AC1=10 EXPECTED RESULT IN AC2 IS 10
26                    ;SWP15:
27 05261 020150             LDA     0,K4000         ;GET 4000
28 05262 024140             LDA     1,K10   ;10 EXPECTED RESULT
29 05263 111324             MOVZS   0,2,SZR ;"S" BIT 4 TO BIT 12
30 05264 155005             MOV     2,3,SNR
31 05265 063077             HALT                    ;POSS, "ZR" AND FAILURE "S"
32 05266 136404             SUB     1,3,SZR
33 05267 063077             HALT                    ;"S" BIT 4 TO 12 FAILED EX AC
34                    ;SW15A :
35 05270 110340             COMOS   0,2     ;REPEAT TEST WITH A0
36 05271 154000             COM     2,3     ;EXPECTED RESULT HERE IS "7
37 05272 136404             SUB     1,3,SZR
38 05273 063077             HALT                    ;"S" A0 IN BIT 4 TO 12 SEE AC2
39                          ;SW15A TEST SWAP OF COM 4000
40
41
42                          SWPTS 16,K10K,K20,3,11,10000,20
43
44                          ;TEST SWAP BIT 3 TO BIT 11
45                          ;AC0=10000 AC1=20 EXPECTED RESULT IN AC2 IS 20
46                    ;SWP16:
47 05274 020151             LDA     0,K10K  ;GET 10000
48 05275 024141             LDA     1,K20   ;20 EXPECTED RESULT
49 05276 111324             MOVZS   0,2,SZR ;"S" BIT 3 TO BIT 11
50 05277 155005             MOV     2,3,SNR
51 05300 063077             HALT                    ;POSS, "ZR" AND FAILURE "S"
52 05301 136404             SUB     1,3,SZR
53 05302 063077             HALT                    ;"S" BIT 3 TO 11 FAILED EX AC
54                    ;SW16A :
55 05303 110340             COMOS   0,2     ;REPEAT TEST WITH A0
56 05304 154000             COM     2,3     ;EXPECTED RESULT HERE IS "7
57 05305 136404             SUB     1,3,SZR
58 05306 063077             HALT                    ;"S" A0 IN BIT 3 TO 11 SEE AC2
59                          ;SW16A TEST SWAP OF COM 10000
60
```

```
 0164 .MAIN
01
02                      SWPTS 17,K20K,K40,2,10,20000,40
03
04                      ;TEST SWAP BIT 2 TO BIT 10
05                      ;AC0=20000 AC1=40 EXPECTED RESULT IN AC2 IS 40
06                  ;SWP17:
07 05307 020152         LDA     0,K20K  ;GET 20000
08 05310 024142         LDA     1,K40   ;40 EXPECTED RESULT
09 05311 111324         MOVZS   0,2,SZR ;"S" BIT 2 TO BIT 10
10 05312 155005         MOV     2,3,SNR
11 05313 063077         HALT            ;POSS, "ZR" AND FAILURE "S"
12 05314 136404         SUB     1,3,SZR
13 05315 063077         HALT            ;"S" BIT 2 TO 10 FAILED EX AC
14                  ;SW17A :
15 05316 110340         COMOS   0,2     ;REPEAT TEST WITH A0
16 05317 154000         COM     2,3     ;EXPECTED RESULT HERE IS "7
17 05320 136404         SUB     1,3,SZR
18 05321 063077         HALT            ;"S" A0 IN BIT 2 TO 10 SEE AC2
19                      ;SW17A TEST SWAP OF COM 20000
20
21
22                      SWPTS 18,K40K,K100,1,9,40000,100
23
24                      ;TEST SWAP BIT 1 TO BIT 9
25                      ;AC0=40000 AC1=100 EXPECTED RESULT IN AC2 IS 100
26                  ;SWP18:
27 05322 020153         LDA     0,K40K  ;GET 40000
28 05323 024143         LDA     1,K100  ;100 EXPECTED RESULT
29 05324 111324         MOVZS   0,2,SZR ;"S" BIT 1 TO BIT 9
30 05325 155005         MOV     2,3,SNR
31 05326 063077         HALT            ;POSS, "ZR" AND FAILURE "S"
32 05327 136404         SUB     1,3,SZR
33 05330 063077         HALT            ;"S" BIT 1 TO 9 FAILED EX AC
34                  ;SW18A :
35 05331 110340         COMOS   0,2     ;REPEAT TEST WITH A0
36 05332 154000         COM     2,3     ;EXPECTED RESULT HERE IS "7
37 05333 136404         SUB     1,3,SZR
38 05334 063077         HALT            ;"S" A0 IN BIT 1 TO 9 SEE AC2
39                      ;SW18A TEST SWAP OF COM 40000
40
41
42                      SWPTS 19,K100K,K200,0,8,100000,200
43
44                      ;TEST SWAP BIT 0 TO BIT 8
45                      ;AC0=100000 AC1=200 EXPECTED RESULT IN AC2 IS 200
46                  ;SWP19:
47 05335 020154         LDA     0,K100K         ;GET 100000
48 05336 024144         LDA     1,K200  ;200 EXPECTED RESULT
49 05337 111324         MOVZS   0,2,SZR ;"S" BIT 0 TO BIT 8
50 05340 155005         MOV     2,3,SNR
51 05341 063077         HALT            ;POSS, "ZR" AND FAILURE "S"
52 05342 136404         SUB     1,3,SZR
53 05343 063077         HALT            ;"S" BIT 0 TO 8 FAILED EX AC
54                  ;SW19A :
55 05344 110340         COMOS   0,2     ;REPEAT TEST WITH A0
56 05345 154000         COM     2,3     ;EXPECTED RESULT HERE IS "7
57 05346 136404         SUB     1,3,SZR
58 05347 063077         HALT            ;"S" A0 IN BIT 0 TO 8 SEE AC2
59                      ;SW19A TEST SWAP OF COM 100000
60
```

```
 0165 .MAIN
01
02                ;DEFINE MACRO FOR NO LOAD TESTS (IR12=1)
03                        .MACRO NOLOD
04                        ;TEST NOLOAD AC12
05                NLD11:  ADC     12,12   ;AC12=-1
06                        COM#    12,12,SNR       ;ATTEMPT TO MAKE ZERO
07                        COM     12,12,SZR       ;AC12 SHD HAVE =-1
08                        HALT            ;AC12 ALTERED IR 12=1
09                        ADC#    12,12,SZR       ;NOLOAD I'S
10                        MOV     12,12,SZR       ;AC12 SHD STILL=0'S
11                        HALT            ;IR12=1 DID NOT NLOCK I'S
12                %
13
14
15
16
17
18
19
20
21
22                        NOLOD 1,0
23                        ;TEST NOLOAD AC0
24 05350 102000 NLD1:     ADC     0,0     ;AC0=-1
25 05351 100015           COM#    0,0,SNR ;ATTEMPT TO MAKE ZERO
26 05352 100004           COM     0,0,SZR ;AC0 SHD HAVE =-1
27 05353 063077           HALT            ;AC0 ALTERED IR 12=1
28 05354 102014           ADC#    0,0,SZR ;NOLOAD I'S
29 05355 101004           MOV     0,0,SZR ;AC0 SHD STILL=0'S
30 05356 063077           HALT            ;IR12=1 DID NOT NLOCK I'S
31
32                        NOLOD 2,1
33                        ;TEST NOLOAD AC1
34 05357 126000 NLD2:     ADC     1,1     ;AC1=-1
35 05360 124015           COM#    1,1,SNR ;ATTEMPT TO MAKE ZERO
36 05361 124004           COM     1,1,SZR ;AC1 SHD HAVE =-1
37 05362 063077           HALT            ;AC1 ALTERED IR 12=1
38 05363 126014           ADC#    1,1,SZR ;NOLOAD I'S
39 05364 125004           MOV     1,1,SZR ;AC1 SHD STILL=0'S
40 05365 063077           HALT            ;IR12=1 DID NOT NLOCK I'S
41
42                        NOLOD 3,2
43                        ;TEST NOLOAD AC2
44 05366 152000 NLD3:     ADC     2,2     ;AC2=-1
45 05367 150015           COM#    2,2,SNR ;ATTEMPT TO MAKE ZERO
46 05370 150004           COM     2,2,SZR ;AC2 SHD HAVE =-1
47 05371 063077           HALT            ;AC2 ALTERED IR 12=1
48 05372 152014           ADC#    2,2,SZR ;NOLOAD I'S
49 05373 151004           MOV     2,2,SZR ;AC2 SHD STILL=0'S
50 05374 063077           HALT            ;IR12=1 DID NOT NLOCK I'S
51
52                        NOLOD 4,3
53                        ;TEST NOLOAD AC3
54 05375 176000 NLD4:     ADC     3,3     ;AC3=-1
55 05376 174015           COM#    3,3,SNR ;ATTEMPT TO MAKE ZERO
56 05377 174004           COM     3,3,SZR ;AC3 SHD HAVE =-1
57 05400 063077           HALT            ;AC3 ALTERED IR 12=1
58 05401 176014           ADC#    3,3,SZR ;NOLOAD I'S
59 05402 175004           MOV     3,3,SZR ;AC3 SHD STILL=0'S
60 05403 063077           HALT            ;IR12=1 DID NOT NLOCK I'S
```

```
 0166 .MAIN
01
02                ;FIRST USE OF STA INSTRUCTION
03                ;ALSO, FIRST LDA WITH 0 AS EFFECTIVE ADDRESS
04
05 05404 102000 STA00:  ADC     0,0
06 05405 040000         STA     0,LOC0   ;FIRST USE OF STA
07 05406 024000         LDA     1,LOC0   ;FIRST LDA OF LOC "0"
08 05407 130004         COM     1,2,SZR  ;SKIP IF LDA GOT =1 BACK
09 05410 063077         HALT             ;LDA FROM OC "0" IS IN AC1
10
11                ;NOW STORE 0'S IN LOC 0 RETRY LDA       0
12 05411 102400 STA01:  SUB     0,0
13 05412 040000         STA     0,LOC0   ;2ND STA IN LOC "0"
14 05413 024000         LDA     1,LOC0   ;2ND LDA OF LOC "0"
15 05414 125004         MOV     1,1,SZR  ;SKP IS LDA GOT 0'S BACK
16 05415 063077         HALT
17                      ;IF EITHER OF ABOVE HALTS EXAMINE LOC CONTAINING STA
18                      ;IN CASE ADDRESSING MODE I ENABLED
19                      ;IF STA00+1=-1 OR STA01+1=0 SEE IR7 ALU ROM
20
21                ;CONTINUATION OF LDA TESTS
22                ;ADDRESSING MODE 01 (IR7=1 IR6=0)
23 05416 102000 LDA29:  ADC     0,0      ;SET AC0=-1
24 05417 020400         LDA     0,.      ;FIRST LDA WITH IR7=1
25 05420 024155         LDA     1,KLDA,  ;GET LDA 0,, FROM PAGE 0
26 05421 106404         SUB     0,1,SZR  ;RESULT LAST 2 LOADS SHD BE=
27 05422 063077         HALT             ;LDA 0 IR7=1 FAILED
28                      ;EXPECTED RESULT IN AC0 PROBABLY LADED LOC "0" INSTEAD
29                      ;AT THIS POINT IN TEST "LOC 0"=0
30
31                ;NOW TEST FORWARD "LDA .+1" +1 OFFSET
32 05423 126000 LDA30:  ADC     1,1
33 05424 024401         LDA     1,.+1    ;GET NEXT MEM LOC
34 05425 020400         LDA     0,.+0    ;ALSO 0=LDA 0,.
35 05426 131000         MOV     1,2      ;SAVE LDA RESULTS
36 05427 112404         SUB     0,2,SZR  ;SKP BOHT LDA'S CORRECT
37 05430 063077         HALT             ;AC0 AND 1 SHD BOTH=LDA 0,.
38
39                ;USE NEGATIVE OFFEST FOR THE FIRST TIME
40                ;NOW TEST MODE 01 NEGATIVE OFFSET OF=1
41 05431 126000 LDA31:  ADC     1,1      ;SEE DISPCTND IF TEST FAILS
42 05432 020400         LDA     0,.      ;GET THIS INST TO AC0
43 05433 024777         LDA     1,.-1    ;FIRST USE - OFFSET TO AC1
44 05434 131000         MOV     1,2      ;SAVE LDA RESULTS
45 05435 112404         SUB     0,2,SZR  ;SKP BOTH LDA'S CORRECT
46 05436 063077         HALT             ;SEE DISP XTND +
47
48                ;LDA    ALL AC'S WITH LDA 0,. USING FORWARD OFFSETS
49 05437 034403 LDA32:  LDA     3,.+3
50 05440 030402         LDA     2,.+2
51 05441 024401         LDA     1,.+1
52 05442 020400         LDA     0,.
53 05443 106414         SUB#    0,1,SZR
54 05444 063077         HALT             ;LDA 1,.+1 FAILED
55 05445 112414         SUB#    0,2,SZR
56 05446 063077         HALT             ;LDA 2,.+2 FAILED
57 05447 116414         SUB#    0,3,SZR
58 05450 063077         HALT             ;LDA 3,.+3 FAILED
```

```
!0167 .MAIN
01
02                    ;TEST LDA SEQUENCE OF - OFFSETS
03 05451 020400 LDA33:  LDA     0,.
04 05452 024777         LDA     1,.-1
05 05453 030776         LDA     2,.-2
06 05454 034775         LDA     3,.-3
07 05455 106414         SUB#    0,1,SZR
08 05456 063077         HALT                ;LDA .-1 FAILED
09 05457 112414         SUB#    0,2,SZR
10 05460 063077         HALT                ;LDA .-2 FAILED
11 05461 116414         SUB#    0,3,SZR
12 05462 063077         HALT                ;LDA .-3 FAILED
```

```
10168 .MAIN
01
02                ;TEST FOR EXISTENCE OF ISZ INSTR
03                ;FIRST USE OF ISZ INSTRUCTION
04 05463 102400 ISZ00:  SUB     0,0
05 05464 040000         STA     0,LOC0
06 05465 152000         ADC     2,2       ;SET AC2=-1 ISZ COULD=LDA OR STA
07 05466 010000         ISZ     LOC0      ;+1 LOC 0 SHD NOW=+1
08 05467 105001         MOV     0,1,SKP   ;ALU CRY MIGHT NOT=1
09 05470 063077         HALT              ;ISZ (0+1) SKIPPED
10 05471 024000         LDA     1,LOC0    ;SEE SETSKP AND ZR SKIP
11 05472 121225         MOVZR   1,0,SNR   ;MAKE SURE ISZ RESULT
12 05473 101003         MOV     0,0,SNC   ;IS=TO+1
13 05474 063077         HALT              ;0+1 DID NOT=+1
14 05475 154004         COM     2,3,SZR
15 05476 063077         HALT              ;ISZ CHANGED AC2
16
17                ;TEST FOR EXISTENCE OF DSZ INSTRUCTION
18                ;-1 TO 0 IN LOC 0 SHD=-1
19                ;FIRST USE OF DSZ INST
20 05477 176400 DSZ00:  SUB     3,3
21 05500 040000         STA     0,LOC0
22 05501 014000         DSZ     LOC0      ;-1 TO 0 IN LOC 0
23 05502 105001         MOV     0,1,SKP
24 05503 063077         HALT              ;DSZ SKIPPED 0-1
25 05504 024000         LDA     1,LOC0    ;GET DSZ RESULTS SHD=-1
26 05505 120004         COM     1,0,SZR
27 05506 063077         HALT              ;DSZ RESULT NOT=-1
28 05507 175004         MOV     3,3,SZR   ;AC3 SHD BE DISTURBED
29 05510 063077         HALT              ;DSZ CHANGED AC3
30
31                ;RETEST ISZ TO SKIP AND NOT CHANGE VRY
32                ;+1 TO -1 IN LOC 0
33 05511 102000 ISZ01:  ADC     0,0
34 05512 040000         STA     0,LOC0    ;(0)=-1
35 05513 111120         MOVZL   0,2       ;(AC2=-2) CRY=1
36 05514 010000         ISZ     LOC0      ;+1-1=SETSKIP,ZR
37 05515 063077         HALT              ;ISZ=1 SIS NOT SKIP
38 05516 101003         MOV     0,0,SNC   ;TEST CALC
39 05517 063077         HALT              ;CRY OUT CHANGED CRY
40 05520 020000         LDA     0,LOC0
41 05521 101004         MOV     0,0,SZR
42 05522 063077         HALT              ;(LOC 0) DID NOT=- AFTER ISZ
43 05523 140225         COMZR   2,0,SNR   ;MAKE SURE AC2 STILL=-2
44 05524 101003         MOV     0,0,SNC
45 05525 063077         HALT              ;ISZ CHANGED AC2
46
47                ;TEST DSZ SETSKP , ZR IN SKIP LOGIC
48 05526 102520 DSZ01:  SUBZL   0,0
49 05527 040000         STA     0,LOC0    ;(LOC 0=+1)
50 05530 114000         COM     0,3       ;(AC3=-2)
51 05531 014000         DSZ     LOC0      ;+1-1=SETSKP , ZR
52 05532 063077         HALT              ;DSZ DID NOT SKIP
53 05533 101002         MOV     0,0,SZC   ;TEST NOT CALC TO STOP CRYOUT
54 05534 063077         HALT              ;CRYOUT CHANGED CRY
55 05535 160225         COMZR   3,0,SNR
56 05536 101003         MOV     0,0,SNC   ;AC3 SHD STILL=-2
57 05537 063077         HALT              ;DSZ CHANGED AC3
```

```
!0169 .MAIN
01
02                ;FIRST USE OF JMP INSTRUCTION JMP .+2
03                ;ADDRS OF JMP TESTS ARE STORED IN LOC 0
04 05540 020402 JMP00:  LDA     0,.+2
05 05541 115001         MOV     0,3,SKP
06 05542 005540         JMP00
07 05543 040000         STA     0,LOC0  ;ADDRS OF JMP TST TO LOC 0
08 05544 000402         JMP     .+2
09 05545 063077         HALT            ;HMP DID NOT JMP
10 05546 116414         SUB#    0,3,SZR ;AC0 AND AC 3 SHD BEV
11 05547 063077         HALT            ;JMP CHANGED AC3 (JRS?)
12
13                ;TEST JMP WITH A NEG OFFSET
14 05550 020402 JMP01:  LDA     0,.+2
15 05551 115001         MOV     0,3,SKP
16 05552 005550         JMP01
17 05553 040000         STA     0,LOC0  ;LOC 0=ADDRS JMP TEST
18 05554 111001         MOV     0,2,SKP ;GET TO JMP -
19 05555 000403         JMP     .+3
20 05556 000777         JMP     .-1
21 05557 063077         HALT
22 05560 116414         SUB#    0,3,SZR
23 05561 063077         HALT            ;JMP CHANGED AC0 OR AC3
```

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!0170 .MAIN
01
02                      ;FIRST USE OF JSR INSTRUCTION
03 05562 020402 JSR00:  LDA     0,.+2
04 05563 115001         MOV     0,3,SKP
05 05564 005562         JSR00           ;ADRS THIS TEST
06 05565 040000         STA     0,LOC0  ;TO LOC 0
07 05566 004402         JSR     .+2     ;FIRST USE JSR
08 05567 063077         HALT            ;JST DID NOT CHNG PC
09 05570 024156         LDA     1,K5
10 05571 123000         ADD     1,0     ;NOW AC0 AND AC3 SHD BEV
11 05572 116414         SUB#    0,3,SZR
12 05573 063077         HALT            ;JSR FAILED TO LOAD AC3
13
14                      ;TEST JSR WITH NEG OFFSET
15 05574 020402 JSR01:  LDA     0,.+2
16 05575 115001         MOV     0,3,SKP
17 05576 005574         JSR01           ;ADRS THIS TEST
18 05577 040000         STA     0,LOC0  ;TO LOC 0
19 05600 111001         MOV     0,2,SKP
20 05601 000403         JMP     .+3
21 05602 004777         JSR     .-1     ;FIRST JSR - OFFSET
22 05603 063077         HALT            ;JST DID NOT CHNG PC
23 05604 024157         LDA     1,K7
24 05605 123000         ADD     1,0
25 05606 116414         SUB#    0,3,SZR
26 05607 063077         HALT
27
28                      ;NOW TEST LDA USING INDEX MODE 2
29                      ;FIRST USE OF INDEXING OFFSET AND INDEX 0
30 05610 102000 LDA34:  ADC     0,0
31 05611 040000         STA     0,LOC0  ;OREOARE AC'S
32 05612 110000         COM     0,2     ;0=-1 1 AND 2=0
33 05613 145000         MOV     2,1     ;AC3=+1
34 05614 050001         STA     2,LOC1  ;(LOC 1)=0
35 05615 155400         INC     2,3
36 05616 025000         LDA     1,0,2
37 05617 167014         ADD#    3,1,SZR ;AC3=+1 (AC1)=-1 IF LDA CORRECT
38 05620 063077         HALT            ;LDA 1,0,2 FAILED
39                      ;MAY HAVE USED AC3 AS INDEX (AC1) WILL=(LOC 1)
40
41                      ;TEST TO MAKE SURE EFA REALLY INDEXES MODE 2
42 05621 102000 LDA35:  ADC     0,0
43 05622 104000         COM     0,1
44 05623 131400         INC     1,2     ;AC2=1
45 05624 155400         INC     2,3     ;AC3=2
46 05625 044000         STA     1,LOC0  ;LOC 0=0
47 05626 040001         STA     0,LOC1  ;LOC 1=-1
48 05627 025000         LDA     1,0,2   ;GET (LOC 1) TO AC1*
49 05630 106414         SUB#    0,1,SZR
50 05631 063077         HALT
51                      ;ALSO FIRST USE OF AN LDA PAGE 0 BIT 0=1
52
53 05632 030144 STA02:  LDA     2,K200  ;THIS LDA PREV TESTED
54 05633 051000         STA     2,0,2   ;STORE 200 IN LOC 200
55 05634 024200         LDA     1,L0200 ;DIRECT ACCESS 200
56 05635 132414         SUB#    1,2,SZR ;NOT=LDA OR STA
57 05636 063077         HALT            ;COULD FAIL EFA DISPCTND
58                      ;IR8=1 SHD BE BLOCKED BY ALU ROM IR6,7=0 ,EFA
```

```
10171 .MAIN
01
02                ;TRY STA AGAIN WITH + OFFSET
03                ;CONTENTS OF LOC 200 STILL=200
04 05637 030144 STA03:  LDA     2,K200
05 05640 141400         INC     2,0
06 05641 041001         STA     0,1,2
07 05642 024201         LDA     1,LO201
08 05643 122414         SUB#    1,0,SZR
09 05644 063077         HALT            ;STA 0,1,2 FAILED
10
11                ;TRY STA AGAIN WITH - OFFSET
12 05645 030144 STA04:  LDA     2,K200
13 05646 144000         COM     2,1
14 05647 045377         STA     1,-1,2  ;COM 200 TO LOC 177
15 05650 020177         LDA     0,LO177 ;GET IT BACK
16 05651 106414         SUB#    0,1,SZR ;(LOC 177) SHD=COM 200
17 05652 063077         HALT            ;STA 1,-1,2 FAILED
18                      ;DISPXTND MAY HAVE FAILED EFA IR8=1 AND NOT INDES 00
19                      ;ALU ROM IR6=1 AND EFA
20
21                ;USE STA DIRECT TO 300
22                ;AND LDA INDEXED MODE 3 TO RETRIEVE
23 05653 034144 STA05:  LDA     3,K200  ;PREP AC2 AND AC3 FOR
24 05654 030143         LDA     2,K100  ;RESTING INDEX 3 GETS AC3
25 05655 054300         STA     3,LO300 ;DOUBTFUL THAT DISPXTND FAILS
26 05656 160000         COM     3,0
27 05657 040200         STA     0,LO200 ;PREP LOC 200 IN CASE INDEXS AC2
28 05660 025500         LDA     1,100,3 ;FIRST USE OF INDEX 3
29 05661 136414         SUB#    1,3,SZR ;AC1 AND AC3 SHD=200
30 05662 063077         HALT            ;LDA DIDN'T GET (LOC 300)
31                      ;IF (AC1)=COM OF 200 INDEX 2 WAS USED INSTEAD
32
33                ;TEST LDA INDEXED AC 3 WITH - OFFSET
34 05663 034160 STA06:  LDA     3,K300
35 05664 030144         LDA     2,K200
36 05665 160400         NEG     3,0
37 05666 040277         STA     0,LO277 ;-300 TO LOC 277
38 05667 025777         LDA     1,-1,3  ;LDC 277 TO AC1
39 05670 122414         SUB#    1,0,SZR ;AC1 SDH=AC0
40 05671 063077         HALT            ;LDA 1,-1,3 FAILED
```

```
10172 ,MAIN
01
02                ;START TESTING AUTC INDEX AND INDIRECTS
03                ;USING MODE 2 SAFEST WAY TO LOAD LOC 20
04                ;AND AVOID "AUTO"
05 05672 030141 STA07:  LDA     2,K20
06 05673 020145         LDA     0,K400
07 05674 114400         NEG     0,3
08 05675 041000         STA     0,0,2   ;FIRST REF MEM LOC 20
09 05676 055001         STA     3,1,2
10 05677 024020         LDA     1,20    ;FIRST DIRECT REG LOC 20
11 05700 122414         SUB#    1,0,SZR ;AC1 0 AND LOC 20 SHD=400
12 05701 063077         HALT            ;REFERENCE LOC 20 FAILED
13                      ;AUTO ENABLED INTO SET AUTO COULD FAIL IR11=1
14                      ;720) AC1 AND AC0 SHOULD ALL=400
15
16                ;FIRST USE OF DEFER FOLLOWS
17                ;NOT AUTO INDEXED VOULD HANG UP VIA NOT CP80
18 05702 024144 STA08:  LDA     1,K200  ;PREPARE REGISTERS
19 05703 044000         STA     1,0     ;FOR TEST
20 05704 130400         NEG     1,2
21 05705 050200         STA     2,200   ;200=-200
22 05706 044177         STA     1,177   ;177 AND 201
23 05707 044201         STA     1,201   ;=+1--
24 05710 022000         LDA     0,00    ;FIRST TIME IR5=1
25 05711 112414         SUB#    0,2,SZR ;AC2 AND AC0 SHD=-200
26 05712 063077         HALT            ;FIRST DEFER FAILED
27 05713 020000         LDA     0,0
28 05714 106414         SUB#    0,1,SZR ;LOC 0 SHD=200
29 05715 063077         HALT            ;AUTO INC OR DEC LOC 0
30                      ;SEE NOT IR11 INTO SET AUTO
31                      ;AC0=201 AUTO SET PREMATURELY
```

```
10173 .MAIN
01
02                ;NOW TEST DEFER VIA AUTO LOC 20
03                ;FIRST TIME FOR AUTO INC
04                ;IF IT DOESN'T CLEAR GOOD LUCK +1 INST'S STARTS
05 05716 024160 STA09:  LDA     1,K300
06 05717 044020         STA     1,AIL20 ;PREPARE LOC'S
07 05720 120400         NEG     1,0     ;(20)=300 AND (277)=300 AND (300)=300
08 05721 040301         STA     0,LO301 ;(301)=-300
09 05722 044300         STA     1,LO300
10 05723 044277         STA     1,LO277
11 05724 036020         LDA     3,@AIL20 ;FIRST TIME AUTO
12 05725 116414         SUB#    0,3,SZR ;(301) 0 AND AC 3 SHD=-300
13 05726 063077         HALT            ;AUTO (@20) FAILED LDA
14 05727 030020         LDA     2,AIL20
15 05730 125400         INC     1,1
16 05731 146414         SUB#    2,1,SZR ;(20) SHD +1 TO=301
17 05732 063077         HALT            ;@20 DID NOT +1
18                      ;AUTO DEC COULD HAVE STE SEE "NOT ALU12" AND SET AUTO
19                      ;CONTENTS OF LOC 20 WILL=277
20                      ;OR IF DEFER CLRS PREMATURE AC3 WILL=301
21                      ;SEE "SET AUTO" INTO CLR DEFER TO BLOCK 0 TO DEFER
22
23                ;NOW TEST AUTO DEC @30
24                ;FIRST TIME FOR AUTO DEC
25 05733 024144 STA10:  LDA     1,K200  ;NEXT STA COULD HURT IR12=1
26 05734 044030         STA     1,ADL30 ;NO SET AUTO SO AUTO DEC SHD=0
27 05735 134400         NEG     1,3     ;ALU 12 HAS=1 PREVIOUSLY THOUGH
28 05736 054177         STA     3,LO177 ;177=-200
29 05737 044200         STA     1,LO200 ;200 201=+200
30 05740 044201         STA     1,LO201
31 05741 022030         LDA     0,@ADL30 ;FIRST AUTO DEC
32 05742 116414         SUB#    0,3,SZR ;AC0 AND 3 SHD=-200
33 05743 063077         HALT            ;FIRST AUTO DEC FAILED
34 05744 020030         LDA     0,ADL30
35 05745 115400         INC     0,3
36 05746 136414         SUB#    1,3,SZR
37 05747 063077         HALT            ;(30) NOT=177 AUTO DEC
38                      ;IF CONTENTS (30)=201 SEE ALU12,SET AUTO INTO AUTO DEC
```

```
10174 .MAIN
31
32                ;CASCADE DEFFRS THROUGH 0 AND 1
33                ;FIRST DEFER DEFERRED
34 05750 102620 STA11:  SUBZR   0,0       ;AC0:=100000
35 05751 101400         INC     0,0       ;CREATE #1
36 05752 040000         STA     0,LOC0    ;(LOC 0)=#1
37 05753 024160         LDA     1,K300    ;(LOC 1)=300
38 05754 044001         STA     1,LOC1
39 05755 134400         NEG     1,3
10 05756 054300         STA     3,LO300 ;(300)=-300
11 05757 044301         STA     1,LO301 ;(301)=300
12 05760 044277         STA     1,LO277 ;(277)=300
13 05761 032000         LDA     2,#LOC0 ;SHD ALSO DEFER #1 TO LOC 300
14 05762 156414         SUB#    2,3 SZR ;AC2,3 SHD BOTH=-300
15 05763 063077         HALT            ;DEFER DEFERRED FAILED
16                      ;IF AC2=300 SEE NOT CPB0 INTO CLEAR DEFER
17                      ;CPH0=1 SHD INHIBIT CLR DEFER
18
19                ;CASCADE DEFERS THROUGH 20 TO 37
20                ;20 TO 27 START=#17+1 TO 020 (20) EVENT=#37
21                ;30 TO 36=#21-1 TO 020
22                ;37=300-1 TO 277
23 05764 030141 STA12:  LDA     2,K20   ;SET UP AUTO REGISTERS 20 - 37
24 05765 020161         LDA     0,KD17  ;AC0:=#17
25 05766 176400         SUB     3,3     ;AC3:=0
26 05767 024162         LDA     1,KM8   ;AC1:=-8
27 05770 041000         STA     0,0,2   ;FIRST 20 TO 27=#17
28 05771 151400         INC     2,2     ;THEN 30 TO 37=#21
29 05772 125404         INC     1,1,SZR
30 05773 000775         JMP     STA12+4
31 05774 174005         COM     3,3,SNR
32 05775 000403         JMP     .+3
33 05776 020163         LDA     0,KD21  ;AC0:=#21
34 05777 000770         JMP     STA12+3
35 06000 020160         LDA     0,K300
36 06001 041377         STA     0,-1,2  ;(37)=300
37 06002 040300         STA     0,LO300 ;(300)=300
38 06003 040301         STA     0,LO301 ;(301)=300
39 06004 040017         STA     0,LOC17 ;(17)=300
40 06005 114400         NEG     0,3     ;AC3:=-300
41 06006 054277         STA     3,LO277 ;(277)=-300
42 06007 027360         LDA     1,#-20,2 ;EFA #20-#'S THROUGH
43                                       ;20,20,21,20,22,20,23,20,24,20,25,
44                                       ;20,26,20,27,20,30,20,31,20,32,20,33,
45                                       ;20,34,20,35,20,36,20,37,277
46 06010 136414         SUB#    1,3,SZR ;AC1 AND 3 SHD=-300
47 06011 063077         HALT            ;CASCADED DEFERS AUTO FAILED
48 06012 021360         LDA     0,-20,2 ;GET (20)AGAIN
49 06013 024164         LDA     1,KD37  ;AC1:= #37
50 06014 106414         SUB#    0,1,SZR
51 06015 063077         HALT            ;AUTO LOC 20 INCORRECT
```

```
10175 .MAIN
01
02                ;TEST JMP "0" TO BLOCK SETFETXH AND 2WRADR1
03 06016 020402 JMP02:  LDA     0,.+2
04 06017 115001         MOV     0,3,SKP
05 06020 006016         JMP02
06 06021 040000         STA     0,LOC0  ;ADRS OF JMPTST TO LOC 0
07 06022 002403         JMP     @JMP2L
08 06023 063077         HALT            ;JMP @ FAILED TO JMP AT ALL
09 06024 063077         HALT            ;MAY BE SKIP ALSO
10 06025 106030 JMP2L:  @.+3            ;OR ADCZ# 0,1,SKP
11 06026 063077         HALT            ;@ WAS IGNORED IN JMP @JMP2L
12 06027 063077         HALT            ;@.+3 MAY BE SKIP ALSO
13 06030 006031         .+1             ;OR JSR @32 ?
14 06031 116414         SUB#    0,3,SZR ;AC0 OR 3 CHANGED ON A JMP@
15 06032 063077         HALT
16
17                ;JMP SHOULD NOT GENERATE SETSKIP "JMP 0"
18 06033 020413 JMP03:  LDA     0,JM3K  ;JMP @300
19 06034 040001         STA     0,LOC1  ;TO LOC 1
20 06035 101400         INC     0,0
21 06036 040000         STA     0,LOC0  ;JMP @301 TO 0
22 06037 024410         LDA     1,JM3K+1
23 06040 044300         STA     1,LO300 ;ERROR RETURN TO LOC 1
24 06041 125400         INC     1,1
25 06042 044301         STA     1,LO301 ;OK RETURN TO LOC 0
26                                      ;(0)    JMP @301
27                                      ;(1)    JMP @300
28                                      ;(300)  JM3K+2  ADDR OF HALT
29                                      ;(301)  JM3K+3  ADDR OF HALT+1
30                                      ;(KLOC0) LOC0
31
32                                      ;(HERE) JMP @KLOC0
33 06043 002171         JMP     @KLOC0
34 06044 063077         HALT
35 06045 063077         HALT
36 06046 002300 JM3K:   JMP     @LO300
37 06047 006050         .+1
38 06050 063077         HALT            ;JMP @KLOC0 ZR,SETSKP
39
40                ;LDA INDEXED WITH BIT0=1 SHOULD
41                ;NOT DEFER WHEN IR5=0.
42 06051 030160 LDA36:  LDA     2,K300
43 06052 144400         NEG     2,1
44 06053 044301         STA     1,LO301 ;(301)=-300
45 06054 044277         STA     1,LO277 ;(277)=-300
46 06055 141400         INC     2,0
47 06056 040300         STA     0,LO300 ;@ WILL GET 301 IN ERROR
48 06057 153240         ADDOR   2,2     ;SET BIT 0=1, AC2:=100300
49                                      ;(277)  -300
50                                      ;(300)  301
51                                      ;(301)  -300
52                                      ;AC0    301
53                                      ;AC2    @300
54
55                                      ;(HERE) LDA 3,0,2
56                                      ;       SUB# 0,3,SZR
57                                      ;       HALT
58 06060 035000         LDA     3,0,2   ;IR5=0 SHD NOT DEFER
59 06061 116414         SUB#    0,3,SZR
60 06062 063077         HALT            ;INDEX "CPB0" DEFERRED
```

```
 0176 .MAIN
01
02                ;LDA AUTO REG 20 WITH BIT0=1 SHOULD NOT DEFER
03                ;WHEN IR5=0 AND (20) BIT 0=1
04 06063 030141 LDA37:  LDA     2,K20
05 06064 034160         LDA     3,K300
06 06065 054300         STA     3,LO320
07 06066 054301         STA     3,LO301
08 06067 177240         ADDOR   3,3       ;AC3:=100300=#300
09 06070 055000         STA     3,0,2     ;LOC20:=#300
10 06071 153240         ADDOR   2,2       ;AC2:=100020=#20
11                                        ;(20)   #300
12                                        ;(300)  300
13                                        ;(301)  300
14                                        ;AC3    #300
15                                        ;AC2    #20
16
17                                        ;(HERE) LDA 0,0,2
18                                        ;       SUB# 0,3,SZR
19                                        ;       HALT
20 06072 021000         LDA     0,0,2     ;IR5=0 SHOULD NOT DEFER
21 06073 116414         SUB#    0,3,SZR
22 06074 063077         HALT              ;DEFERRED
23
24                ;JSR WITH BIT 0=1 INDEX REG
25                ;SHOULD NOT DEFER AND SHOULD NOT
26                ;ALLOW BIT 0 INTO AC3
27 06075 020402 JSR02:  LDA     0,.+2
28 06076 152621         SUBZR   2,2,SKP ;AC2:=100000=COM 0,0=#0
29 06077 006113         JS02K
30 06100 151400         INC     2,2       ;AC2:=100001=COM 0,0,SKP=#1
31 06101 050000         STA     2,LOC0    ;TO LOC 0
32 06102 024160         LDA     1,K300
33 06103 127240         ADDOR   1,1       ;AC1:=100300=#300
34 06104 044001         STA     1,LOC1    ;#300 (TO KEEP INVALID #)
35 06105 040300         STA     0,LO300   ;DEFER INCORRECT RETURN
36 06106 034170         LDA     3,KJRET   ;(JMP 0,3)
37 06107 054002         STA     3,LOC2    ;TO GET US BACK
38 06110 100000         COM     0,2       ;AC0:=-JS02K-1, BUT IF LOC 0
39                                        ;IS USED AS INSTRUCTION: AC0:=JS02K
40                                        ;(0)  .  COM 0,0,SKP = #1
41                                        ;(1)     #300
42                                        ;(2)     JMP 0,3
43                                        ;(300)   JS02K = ADDR OF HALT
44                                        ;AC0     -JS02K-1
45                                        ;AC2     100001 = #1
46
47                                        ;(HERE) JSR -1,2
48                                        ;       MOVL# 3,3,SZC
49                                        ;JS02K: HALT
50 06111 005377         JSR     -1,2      ;AC2 BIT0=1 IRS=0 (JSR 0)
51                                        ;ABOVE JSR SHOULD NOT DEFER BUT JMP 0,3 IN LOC 2
52                                        ;SHOULD BRING US BACK TO NEXT LOC.
53 06112 175112         MOVL#   3,3,SZC ;AC3 BIT 0 SHOULD = 0
54 06113 063077 JS02K:  HALT              ;DEFERRED OR AC3 BIT0=1
55 06114 126000         ADC     1,1       ;AC1:=-1, AC0 = JS02K
56 06115 107000         ADD     0,1       ;AC1:=JS02K-1
57 06116 136414         SUB#    1,3,SZR ;AC3 SHOULD = NEXT LOC, ADDR JS02K-1
58 06117 063077         HALT              ;WRONG ADDRESS IN AC3
```

```
;0177 .MAIN
01
02                ;TEST ISZ TO NOT ALTER AC'S
03                ;TEMP 00
04 06120 102120 ISZ02:  ADCZL   0,0       ;AC0:=177776=-2
05 06121 040000         STA     0,LOC0    ;(0):=-2
06 06122 102400         SUB     0,0
07 06123 126400         SUB     1,1       ;ALL AC'S = 0
08 06124 152400         SUB     2,2
09 06125 176400         SUB     3,3
10 06126 010000         ISZ     LOC0      ;(0):=177777=-1
11 06127 101004         MOV     0,0,SZR
12 06130 063077         HALT              ;AC0 NOT=0 OR ISZ SKIPPED
13 06131 123000         ADD     1,0
14 06132 143000         ADD     2,0
15 06133 163014         ADD#    3,0,SZR
16 06134 063077         HALT              ;AC1,2 OR 3 ALTERED BY ISZ
17 06135 020000         LDA     0,LOC0    ;(0) = 177777
18 06136 100004         COM     0,0,SZR   ;AC0 SHOULD = 0 (SEE RMW)
19 06137 063077         HALT              ;ISZ 0 DID NOT CHANGE (0)
20
21                ;TEST AGAIN 0'S TO NOT ALTER ONES
22 06140 102400 ISZ03:  SUB     0,0       ;AC0:=0
23 06141 040000         STA     0,LOC0
24 06142 100000         COM     0,0       ;AC0:=177777=-1
25 06143 126000         ADC     1,1       ;AC1:=177777
26 06144 152000         ADC     2,2       ;AC2:=177777
27 06145 176040         ADCO    3,3       ;AC3:=177777, CARRY = 1
28 06146 010000         ISZ     LOC0      ;(0):=1
29 06147 175404         INC     3,3,SZR   ;AC3:=0, CARRY = 0
30 06150 063077         HALT
31 06151 136000         ADC     1,3       ;AC3:=0, CARRY UNCHANGED
32 06152 156003         ADC     2,3,SNC   ;AC3:=0, CARRY UNCHANGED
33 06153 116014         ADC#    0,3,SZR   ;AC3:=0
34 06154 063077         HALT              ;AC1,2 OR 3 ALTERED BY ISZ
```

```
!0178 .MAIN
01
02                      ;TEST DSZ TO NOT ALTER AC'S
03                      ;TEMP REG IS USED IN DSZ
04 06155 102000 DSZ02:  ADC     0,0     ;AC0:=177777=-1
05 06156 040000         STA     0,LOC0
06 06157 100000         COM     0,0     ;AC0:=0
07 06160 104400         NEG     0,1     ;ALL AC'S=0
08 06161 130400         NEG     1,2     ;TWOES COMPL OF 0 = 0: 177777+1
09 06162 154400         NEG     2,3
10 06163 014000         DSZ     LOC0    ;-1 TO -2
11 06164 150404         NEG     2,2,SZR
12 06165 063077         HALT            ;DSZ CHANGED AC2
13 06166 132400         SUB     1,2
14 06167 112400         SUB     0,2
15 06170 172414         SUB#    3,2,SZR
16 06171 063077         HALT            ;DSZ CHANGED AC0,1 OR 3
17
18                      ;AGAIN TEST DSZ TO NOT ALTER AC'S
19 06172 176520 DSZ03:  SUBZL   3,3     ;AC3:=000001
20 06173 054000         STA     3,LOC0  ;TO LOC 0
21 06174 164400         NEG     3,1     ;AC1:=177777
22 06175 170240         COMOR   3,2     ;AC'S=-1
23 06176 176000         ADC     3,3
24 06177 161240         MOVOR   3,0
25 06200 014000         DSZ     LOC0    ;1 TO 0
26 06201 063077         HALT            ;DSZ DID NOT SKIP
27 06202 166400         SUB     3,1
28 06203 146000         ADC     2,1
29 06204 106014         ADC#    0,1,SZR
30 06205 063077         HALT            ;AC0, 1, 2 OR 3 ALTERED BY DSZ
31 06206 020000         LDA     0,LOC0
32 06207 101004         MOV     0,0,SZR ;(0) CHANGED TO = 0?
33 06210 063077         HALT            ;DSZ DID NOT CHANGE (0)
```

```
↓0179 .MAIN
01
02                ;AUTO INCREMENT SHOULD NOT ALTER AC'S
03                ;TEMP IS USED FOR AUTO INC
04 06211 152220 STA13:  ADCZR   2,2       ;AC2:=077777
05 06212 050023         STA     2,AIL23
06 06213 126400         SUB     1,1       ;AC1:=0
07 06214 044000         STA     1,LOC0
08 06215 020165         LDA     0,KCBE    ;AC0:=125252 (EVEN BITS)
09 06216 104000         COM     0,1       ;AC1:=052525 (ODD BITS)
10 06217 111000         MOV     0,2       ;AC2:=125252
11 06220 154000         COM     2,3       ;AC3:=052525
12 06221 042023         STA     0,@AIL23  ;125252 GOES TO LOC 0
13 06222 117000         ADD     0,3
14 06223 133000         ADD     1,2
15 06224 156414         SUB#    2,3,SZR
16 06225 063077         HALT              ;AUTO INC ALTERED AN AC
17
18                ;AUTO DEC SHD NOT ALTER ANY AC
19 06226 176520 STA14:  SUBZL   3,3       ;AC3:=000001
20 06227 054037         STA     3,ADL37   ;TO AN AUTO DEC LOC
21 06230 030166         LDA     2,KCBO    ;AC2:=052525 (ODD BITS)
22 06231 140000         COM     2,0       ;AC0:=125252 (EVEN BITS)
23 06232 105000         MOV     0,1       ;AC1:=125252
24 06233 134000         COM     1,3       ;AC3:=052525
25 06234 052037         STA     2,@ADL37  ;AUTO DEC TO LOC 0
26 06235 106414         SUB#    0,1,SZR
27 06236 063077         HALT              ;AC0 OR 1 ALTERED
28 06237 156414         SUB#    2,3,SZR
29 06240 063077         HALT              ;AC2 OR 3 ALTERED
30
31                ;AN LDA WITH IR12=1 SHD NOT "NO LOAD"
32                ;CALC=0
33 06241 102000 LDA38:  ADC     0,0       ;AC0:=177777
34 06242 040030         STA     0,ADL30   ;TO AN AUTO DEC LOC
35 06243 100000         COM     0,0       ;AC0:=0
36 06244 020030         LDA     0,ADL30   ;IR 12=1 SHD STILL LOAD
37 06245 100014         COM#    0,0,SZR
38 06246 063077         HALT              ;IR 12=1 STOPPED LOAD AC0
```

```
10180 .MAIN
01
02                ;TEST ISZ AND DSZ TO NOT SKIP
03                ;DEFINE MACRO FOR TESTING
04
05                        .MACRO ISDST
06                        ;TEST OF ISZ DSZ TO NOT SKIP AROUND I2
07                ;IDSI1:
08                        LDA     0,KI2   ;GET I2
09                        STA     0,IDI1K
10                        ISZ     IDI1K   ;+1
11                        DSZ     IDI1K   ;-1
12                        DSZ     IDI1K   ;-1
13                        ISZ     IDI1K   ;+1
14                        LDA     1,IDI1K ;SHD=I2 AGAIN
15                        SUB#    0,1,SZR
16                        HALT            ;IS DS SEQ FAILED I2
17                        MOV     0,0,SKP
18                IDI1K:  0
19                %
20
21
22
23
24.
25
26
27
28
29
30
31
32                        ISDST 00,2
33                        ;TEST OF ISZ DSZ TO NOT SKIP AROUND 2
34                ;IDS00:
35 06247 020136           LDA     0,K2    ;GET 2
36 06250 040411           STA     0,ID00K
37 06251 010410           ISZ     ID00K   ;+1
38 06252 014407           DSZ     ID00K   ;-1
39 06253 014406           DSZ     ID00K   ;-1
40 06254 010405           ISZ     ID00K   ;+1
41 06255 024404           LDA     1,ID00K ;SHD=2 AGAIN
42 06256 106414           SUB#    0,1,SZR
43 06257 063077           HALT            ;IS DS SEQ FAILED 2
44 06260 101001           MOV     0,0,SKP
45 06261 000000 ID00K:    0
46
47                        ISDST 01,4
48                        ;TEST OF ISZ DSZ TO NOT SKIP AROUND 4
49                ;IDS01:
50 06262 020137           LDA     0,K4    ;GET 4
51 06263 040411           STA     0,ID01K
52 06264 010410           ISZ     ID01K   ;+1
53 06265 014407           DSZ     ID01K   ;-1
54 06266 014406           DSZ     ID01K   ;-1
55 06267 010405           ISZ     ID01K   ;+1
56 06270 024404           LDA     1,ID01K ;SHD=4 AGAIN
57 06271 106414           SUB#    0,1,SZR
58 06272 063077           HALT            ;IS DS SEQ FAILED 4
59 06273 101001           MOV     0,0,SKP
60 06274 000000 ID01K:    0
```

```
 0181 .MAIN
01
02                              ISDST 02,10
03                              ;TEST OF ISZ DSZ TO NOT SKIP AROUND 10
04                    ;IDS02:
05 06275 020140               LDA     0,K10   ;GET 10
06 06276 040411               STA     0,ID02K
07 06277 010410               ISZ     ID02K   ;+1
08 06300 014407               DSZ     ID02K   ;-1
09 06301 014406               DSZ     ID02K   ;-1
10 06302 010405               ISZ     ID02K   ;+1
11 06303 024404               LDA     1,ID02K ;SHD=10 AGAIN
12 06304 106414               SUB#    0,1,SZR
13 06305 063077               HALT            ;IS DS SEQ FAILED 10
14 06306 101001               MOV     0,0,SKP
15 06307 000000 ID02K:        0
16
17                              ISDST 03,20
18                              ;TEST OF ISZ DSZ TO NOT SKIP AROUND 20
19                    ;IDS03:
20 06310 020141               LDA     0,K20   ;GET 20
21 06311 040411               STA     0,ID03K
22 06312 010410               ISZ     ID03K   ;+1
23 06313 014407               DSZ     ID03K   ;-1
24 06314 014406               DSZ     ID03K   ;-1
25 06315 010405               ISZ     ID03K   ;+1
26 06316 024404               LDA     1,ID03K ;SHD=20 AGAIN
27 06317 106414               SUB#    0,1,SZR
28 06320 063077               HALT            ;IS DS SEQ FAILED 20
29 06321 101001               MOV     0,0,SKP
30 06322 000000 ID03K:        0
31
32                              ISDST 04,40
33                              ;TEST OF ISZ DSZ TO NOT SKIP AROUND 40
34                    ;IDS04:
35 06323 020142               LDA     0,K40   ;GET 40
36 06324 040411               STA     0,ID04K
37 06325 010410               ISZ     ID04K   ;+1
38 06326 014407               DSZ     ID04K   ;-1
39 06327 014406               DSZ     ID04K   ;-1
40 06330 010405               ISZ     ID04K   ;+1
41 06331 024404               LDA     1,ID04K ;SHD=40 AGAIN
42 06332 106414               SUB#    0,1,SZR
43 06333 063077               HALT            ;IS DS SEQ FAILED 40
44 06334 101001               MOV     0,0,SKP
45 06335 000000 ID04K:        0
46
47                              ISDST 05,100
48                              ;TEST OF ISZ DSZ TO NOT SKIP AROUND 100
49                    ;IDS05:
50 06336 020143               LDA     0,K100  ;GET 100
51 06337 040411               STA     0,ID05K
52 06340 010410               ISZ     ID05K   ;+1
53 06341 014407               DSZ     ID05K   ;-1
54 06342 014406               DSZ     ID05K   ;-1
55 06343 010405               ISZ     ID05K   ;+1
56 06344 024404               LDA     1,ID05K ;SHD=100 AGAIN
57 06345 106414               SUB#    0,1,SZR
58 06346 063077               HALT            ;IS DS SEQ FAILED 100
59 06347 101001               MOV     0,0,SKP
60 06350 000000 ID05K:        0
```

```
 0182 .MAIN
01
02                              ISDST 06,200
03                              ;TEST OF ISZ DSZ TO NOT SKIP AROUND 200
04                    ;IDS06:
05 06351 020144                 LDA     0,K200  ;GET 200
06 06352 040411                 STA     0,ID06K
07 06353 010410                 ISZ     ID06K   ;+1
08 06354 014407                 DSZ     ID06K   ;-1
09 06355 014406                 DSZ     ID06K   ;-1
10 06356 010405                 ISZ     ID06K   ;+1
11 06357 024404                 LDA     1,ID06K ;SHD=200 AGAIN
12 06360 106414                 SUB#    0,1,SZR
13 06361 063077                 HALT            ;IS DS SEQ FAILED 200
14 06362 101001                 MOV     0,0,SKP
15 06363 000000 ID06K:  0
16
17                              ISDST 07,400
18                              ;TEST OF ISZ DSZ TO NOT SKIP AROUND 400
19                    ;IDS07:
20 06364 020145                 LDA     0,K400  ;GET 400
21 06365 040411                 STA     0,ID07K
22 06366 010410                 ISZ     ID07K   ;+1
23 06367 014407                 DSZ     ID07K   ;-1
24 06370 014406                 DSZ     ID07K   ;-1
25 06371 010405                 ISZ     ID07K   ;+1
26 06372 024404                 LDA     1,ID07K ;SHD=400 AGAIN
27 06373 106414                 SUB#    0,1,SZR
28 06374 063077                 HALT            ;IS DS SEQ FAILED 400
29 06375 101001                 MOV     0,0,SKP
30 06376 000000 ID07K:  0
31
32                              ISDST 08,1000
33                              ;TEST OF ISZ DSZ TO NOT SKIP AROUND 1000
34                    ;IDS08:
35 06377 020146                 LDA     0,K1000 ;GET 1000
36 06400 040411                 STA     0,ID08K
37 06401 010410                 ISZ     ID08K   ;+1
38 06402 014407                 DSZ     ID08K   ;-1
39 06403 014406                 DSZ     ID08K   ;-1
40 06404 010405                 ISZ     ID08K   ;+1
41 06405 024404                 LDA     1,ID08K ;SHD=1000 AGAIN
42 06406 106414                 SUB#    0,1,SZR
43 06407 063077                 HALT            ;IS DS SEQ FAILED 1000
44 06410 101001                 MOV     0,0,SKP
45 06411 000000 ID08K:  0
46
47                              ISDST 09,2000
48                              ;TEST OF ISZ DSZ TO NOT SKIP AROUND 2000
49                    ;IDS09:
50 06412 020147                 LDA     0,K2000 ;GET 2000
51 06413 040411                 STA     0,ID09K
52 06414 010410                 ISZ     ID09K   ;+1
53 06415 014407                 DSZ     ID09K   ;-1
54 06416 014406                 DSZ     ID09K   ;-1
55 06417 010405                 ISZ     ID09K   ;+1
56 06420 024404                 LDA     1,ID09K ;SHD=2000 AGAIN
57 06421 106414                 SUB#    0,1,SZR
58 06422 063077                 HALT            ;IS DS SEQ FAILED 2000
59 06423 101001                 MOV     0,0,SKP
60 06424 000000 ID09K:  0
```

```
 0183 .MAIN
01
02                              ISDST 10,4000
03                              ;TEST OF ISZ DSZ TO NOT SKIP AROUND 4000
04                      ;IDS10:
05 06425 020150                 LDA     0,K4000 ;GET 4000
06 06426 040411                 STA     0,ID10K
07 06427 010410                 ISZ     ID10K   ;+1
08 06430 014407                 DSZ     ID10K   ;-1
09 06431 014406                 DSZ     ID10K   ;-1
10 06432 010405                 ISZ     ID10K   ;+1
11 06433 024404                 LDA     1,ID10K ;SHD=4000 AGAIN
12 06434 106414                 SUB#    0,1,SZR
13 06435 063077                 HALT            ;IS DS SEQ FAILED 4000
14 06436 101001                 MOV     0,0,SKP
15 06437 000000 ID10K:  0
16
17                              ISDST 11,10K
18                              ;TEST OF ISZ DSZ TO NOT SKIP AROUND 10K
19                      ;IDS11:
20 06440 020151                 LDA     0,K10K  ;GET 10K
21 06441 040411                 STA     0,ID11K
22 06442 010410                 ISZ     ID11K   ;+1
23 06443 014407                 DSZ     ID11K   ;-1
24 06444 014406                 DSZ     ID11K   ;-1
25 06445 010405                 ISZ     ID11K   ;+1
26 06446 024404                 LDA     1,ID11K ;SHD=10K AGAIN
27 06447 106414                 SUB#    0,1,SZR
28 06450 063077                 HALT            ;IS DS SEQ FAILED 10K
29 06451 101001                 MOV     0,0,SKP
30 06452 000000 ID11K:  0
31
32                              ISDST 12,20K
33                              ;TEST OF ISZ DSZ TO NOT SKIP AROUND 20K
34                      ;IDS12:
35 06453 020152                 LDA     0,K20K  ;GET 20K
36 06454 040411                 STA     0,ID12K
37 06455 010410                 ISZ     ID12K   ;+1
38 06456 014407                 DSZ     ID12K   ;-1
39 06457 014406                 DSZ     ID12K   ;-1
40 06460 010405                 ISZ     ID12K   ;+1
41 06461 024404                 LDA     1,ID12K ;SHD=20K AGAIN
42 06462 106414                 SUB#    0,1,SZR
43 06463 063077                 HALT            ;IS DS SEQ FAILED 20K
44 06464 101001                 MOV     0,0,SKP
45 06465 000000 ID12K:  0
46
47                              ISDST 13,40K
48                              ;TEST OF ISZ DSZ TO NOT SKIP AROUND 40K
49                      ;IDS13:
50 06466 020153                 LDA     0,K40K  ;GET 40K
51 06467 040411                 STA     0,ID13K
52 06470 010410                 ISZ     ID13K   ;+1
53 06471 014407                 DSZ     ID13K   ;-1
54 06472 014406                 DSZ     ID13K   ;-1
55 06473 010405                 ISZ     ID13K   ;+1
56 06474 024404                 LDA     1,ID13K ;SHD=40K AGAIN
57 06475 106414                 SUB#    0,1,SZR
58 06476 063077                 HALT            ;IS DS SEQ FAILED 40K
59 06477 101001                 MOV     0,0,SKP
60 06500 000000 ID13K:  0
```

```
 0184 .MAIN
01
02                          ISDST 14,100K
03                          ;TEST OF ISZ DSZ TO NOT SKIP AROUND 100K
04                  ;IDS14:
05 06501 020154             LDA     0,K100K ;GET 100K
06 06502 040411             STA     0,ID14K
07 06503 010410             ISZ     ID14K   ;+1
08 06504 014407             DSZ     ID14K   ;-1
09 06505 014406             DSZ     ID14K   ;-1
10 06506 010405             ISZ     ID14K   ;+1
11 06507 024404             LDA     1,ID14K ;SHD=100K AGAIN
12 06510 106414             SUB#    0,1,SZR
13 06511 063077             HALT            ;IS DS SEQ FAILED 100K
14 06512 101001             MOV     0,0,SKP
15 06513 000000 ID14K:      0
16
17
18
19
20
21                  ;TEST AEQB TO REALLY ASSERT FOR BIT 7
22                  ;CAN ONLY BE TESTED VIA @ 420 "SUM 7" IS OTHER ZR AND
23 06514 030167 AEQB7:      LDA     2,K420  ;TO GET AT 420
24 06515 024160             LDA     1,K300  ;TEST CONSTANT = 300
25 06516 045000             STA     1,0,2   ;(420)=300
26 06517 044277             STA     1,LO277 ;AUTO DEC SHOULDN'T, (277) = 300
27 06520 120400             NEG     1,0     ;AC0:=-300
28 06521 040300             STA     0,LO300 ;(300)=-300
29 06522 044301             STA     1,LO301 ;(301)=300
30 06523 037000             LDA     3,@0,2  ;
31 06524 162414             SUB#    3,0,SZR ;420 SHD NOT BE AUTO REG
32 06525 063077             HALT            ;LDA @420 "AEQB" FAILED
33 06526 021000             LDA     0,0,2   ;GET (420) SHD STIL=300
34 06527 106414             SUB#    0,1,SZR
35 06530 063077             HALT            ;(420) WERE ALTERED
```

```
10185 .MAIN
01
02                      ;PROCESSOR I/O INSTR TESTS
03 06531 102620         IO.00:  SUBZR   0,0         ;AC0:=100000=#0
04 06532 040001                 STA     0,LOC1      ;INTA'S WILL #0
05
06                      ;ION SHD=0 NO SKIP ON BUSY NON ZERO
07 06533 063477         IO.00:  SKPBN   CPU         ;ION=0 SHD NOT SKP
08 06534 101001                 MOV     0,0,SKP
09 06535 063077                 HALT                ;IR8,IR9=00 NO SKIP BN
10
11                      ;POWER LOW SHD=0 NO SKIP ON DONE NON ZERO
12 06536 063677         IO.01:  SKPDN   CPU         ;SHD NOT SKP
13 06537 101001                 MOV     0,0,SKP     ;DIDN'T IR8,IR9=10
14 06540 063077                 HALT                ;SEE PWR LOW=1(SHDN'T)
15
16                      ;SKPBZ TO SKIP ION=0 FIRST I/O SKIP TRUE
17 06541 063577         IO.02:  SKPBZ   CPU         ;IR8,IR9=01
18 06542 063077                 HALT                ;BUSY=0 DID NOT SKP
19
20                      ;TEST SKPDZ POWER LOW SHD=0
21 06543 063777         IO.03:  SKPDZ   CPU         ;IR8,IR9=11
22 06544 063077                 HALT                ;DONE=0 NO SKP (PWR LOW)
23
24                      ;NIO SHD NEITHER SKP NOR ALTER ANY AC'S
25 06545 102000         IO.04:  ADC     0,0         ;AC0:=177777
26 06546 105000                 MOV     0,1         ;ALL AC'S=-1
27 06547 131000                 MOV     1,2
28 06550 155000                 MOV     2,3
29 06551 060077                 NIO     CPU         ;MAKE SURE IO SKP=0
30 06552 122001                 ADC     1,0,SKP
31 06553 063077                 HALT                ;NIO CPU SKIPPED
32 06554 156000                 ADC     2,3
33 06555 162414                 SUB#    3,0,SZR
34 06556 063077                 HALT                ;NIO CHANGED AN AC
35
36
37
38                              .MACRO IOTS1
39                              ;DI16 12 CPU SHOULD ONLY ALTER AC12
40                      ;IO.11:
41                              ADC     0,0
42                              MOV     0,1         ;ALL AC'S=-1
43                              MOV     0,2
44                              MOV     0,3
45                              DI16    12,CPU      ;17 12
46                              ADC     13,14,SKP           ;-1+0 SHD=-1
47                              HALT                ;DIT6 SKPD
48                              SUB#    15,14,SZR
49                              HALT                ;AC 13,14 OR 15 ALTERED
50                              COM#    12,12,SNR           ;DID AC12 CHANGE?
51                              HALT                ;ACT2 NOT LOADED
52                      %
53
54                              ;DIA    X,CPU       = READS X
55                              ;DIB    X,CPU       = INTA  X
```

```
!0186 .MAIN
01
02                              IOTS1 05,0,1,2,3,A,READS
03                              ;DIA 0 CPU SHOULD ONLY ALTER AC0
04                      ;IO,05:
05 06557 102000                 ADC     0,0
06 06560 105000                 MOV     0,1     ;ALL AC'S=-1
07 06561 111000                 MOV     0,2
08 06562 115000                 MOV     0,3
09 06563 060477                 DIA     0,CPU   ;READS 0
10 06564 132001                 ADC     1,2,SKP ;-1+0 SHD=-1
11 06565 063077                 HALT            ;DIA SKPD
12 06566 172414                 SUB#    3,2,SZR
13 06567 063077                 HALT            ;AC 1,2 OR 3 ALTERED
14 06570 100015                 COM#    0,0,SNR ;DID AC0 CHANGE?
15 06571 063077                 HALT            ;AC0 NOT LOADED
16
17                              IOTS1 06,1,0,2,3,A,READS
18                              ;DIA 1 CPU SHOULD ONLY ALTER AC1
19                      ;IO,06:
20 06572 102000                 ADC     0,0
21 06573 105000                 MOV     0,1     ;ALL AC'S=-1
22 06574 111000                 MOV     0,2
23 06575 115000                 MOV     0,3
24 06576 064477                 DIA     1,CPU   ;READS 1
25 06577 112001                 ADC     0,2,SKP ;-1+0 SHD=-1
26 06600 063077                 HALT            ;DIA SKPD
27 06601 172414                 SUB#    3,2,SZR
28 06602 063077                 HALT            ;AC 0,2 OR 3 ALTERED
29 06603 124015                 COM#    1,1,SNR ;DID AC1 CHANGE?
30 06604 063077                 HALT            ;AC1 NOT LOADED
31
32                              IOTS1 07,2,3,0,1,A,READS
33                              ;DIA 2 CPU SHOULD ONLY ALTER AC2
34                      ;IO,07:
35 06605 102000                 ADC     0,0
36 06606 105000                 MOV     0,1     ;ALL AC'S=-1
37 06607 111000                 MOV     0,2
38 06610 115000                 MOV     0,3
39 06611 070477                 DIA     2,CPU   ;READS 2
40 06612 162001                 ADC     3,0,SKP ;-1+0 SHD=-1
41 06613 063077                 HALT            ;DIA SKPD
42 06614 122414                 SUB#    1,0,SZR
43 06615 063077                 HALT            ;AC 3,0 OR 1 ALTERED
44 06616 150015                 COM#    2,2,SNR ;DID AC2 CHANGE?
45 06617 063077                 HALT            ;AC2 NOT LOADED
46
47                              IOTS1 08,3,0,1,2,A,READS
48                              ;DIA 3 CPU SHOULD ONLY ALTER AC3
49                      ;IO,08:
50 06620 102000                 ADC     0,0
51 06621 105000                 MOV     0,1     ;ALL AC'S=-1
52 06622 111000                 MOV     0,2
53 06623 115000                 MOV     0,3
54 06624 074477                 DIA     3,CPU   ;READS 3
55 06625 106001                 ADC     0,1,SKP ;-1+0 SHD=-1
56 06626 063077                 HALT            ;DIA SKPD
57 06627 146414                 SUB#    2,1,SZR
58 06630 063077                 HALT            ;AC 0,1 OR 2 ALTERED
59 06631 174015                 COM#    3,3,SNR ;DID AC3 CHANGE?
60 06632 063077                 HALT            ;AC3 NOT LOADED
```

```
 0187 .MAIN
01
02                              IOTS1 09,0,1,2,3,B,INTA
03                              ;DIB 0 CPU SHOULD ONLY ALTER AC0
04                    ;IO.09:
05 06633 102000                 ADC     0,0
06 06634 105000                 MOV     0,1     ;ALL AC'S=-1
07 06635 111000                 MOV     0,2
08 06636 115000                 MOV     0,3
09 06637 061477                 DIB     0,CPU   ;INTA 0
10 06640 132001                 ADC     1,2,SKP ;-1+0 SHD=-1
11 06641 063077                 HALT            ;DIB SKPD
12 06642 172414                 SUB#    3,2,SZR
13 06643 063077                 HALT            ;AC 1,2 OR 3 ALTERED
14 06644 100015                 COM#    0,0,SNR ;DID AC0 CHANGE?
15 06645 063077                 HALT            ;AC0 NOT LOADED
16
17                              IOTS1 10,1,0,3,2,B INTA
18                              ;DIB 1 CPU SHOULD ONLY ALTER AC1
19                    ;IO.10:
20 06646 102000                 ADC     0,0
21 06647 105000                 MOV     0,1     ;ALL AC'S=-1
22 06650 111000                 MOV     0,2
23 06651 115000                 MOV     0,3
24 06652 065477                 DIB     1,CPU   ;INTA 1
25 06653 116001                 ADC     0,3,SKP ;-1+0 SHD=-1
26 06654 063077                 HALT            ;DIB SKPD
27 06655 156414                 SUB#    2,3,SZR
28 06656 063077                 HALT            ;AC 0,3 OR 2 ALTERED
29 06657 124015                 COM#    1,1,SNR ;DID AC1 CHANGE?
30 06660 063077                 HALT            ;AC1 NOT LOADED
31
32                              IOTS1 11,2,3,1,0,B,INTA
33                              ;DIB 2 CPU SHOULD ONLY ALTER AC2
34                    ;IO.11:
35 06661 102000                 ADC     0,0
36 06662 105000                 MOV     0,1     ;ALL AC'S=-1
37 06663 111000                 MOV     0,2
38 06664 115000                 MOV     0,3
39 06665 071477                 DIB     2,CPU   ;INTA 2
40 06666 166001                 ADC     3,1,SKP ;-1+0 SHD=-1
41 06667 063077                 HALT            ;DIB SKPD
42 06670 106414                 SUB#    0,1,SZR
43 06671 063077                 HALT            ;AC 3,1 OR 0 ALTERED
44 06672 150015                 COM#    2,2,SNR ;DID AC2 CHANGE?
45 06673 063077                 HALT            ;AC2 NOT LOADED
46
47                              IOTS1 12,3,2,0,1,B,INTA
48                              ;DIB 3 CPU SHOULD ONLY ALTER AC3
49                    ;IO.12:
50 06674 102000                 ADC     0,0
51 06675 105000                 MOV     0,1     ;ALL AC'S=-1
52 06676 111000                 MOV     0,2
53 06677 115000                 MOV     0,3
54 06700 075477                 DIB     3,CPU   ;INTA 3
55 06701 142001                 ADC     2,0,SKP ;-1+0 SHD=-1
56 06702 063077                 HALT            ;DIB SKPD
57 06703 122414                 SUB#    1,0,SZR
58 06704 063077                 HALT            ;AC 2,0 OR 1 ALTERED
59 06705 174015                 COM#    3,3,SNR ;DID AC3 CHANGE?
60 06706 063077                 HALT            ;AC3 NOT LOADED
```

```
 0188 .MAIN
01
02                ;DOA 0, CPU SHOULD NOT HANG "OUT TIME"
03                ;OUT GOES THROUGH T/S "TQD"
04                ;FIRST TIME FOR ANY DATA OUT (A, B OR C)
05 06707 176000 IO,13:  ADC     3,3       ;AC3:=177777
06 06710 102000         ADC     0,0
07 06711 061077         DOA     0,CPU     ;SHD NOT SKP HALT OR ALTER AC'S
08 06712 100004         COM     0,0,SZR
09 06713 063077         HALT              ;DOA SKPD OR ALTERED AC0
10 06714 174004         COM     3,3,SZR
11 06715 063077         HALT              ;DOA ALTERED AC3
12
13                ;DETERMINE WHICH PATH TO TAKE
14                ;IN TESTING FROM THIS POINT ON
15                ;TTO "DONE" IS USED FOR "TRUE" INTERRUPT TESTING
16                ;TTO DONE=0 AND BUSY=0 "FALSE" INTERRUPT TESTS
17                ;TTO DONE=0 AND BUSY=1 LOOP BACK TO A1A
18 06716 176000 IOX00:  ADC     3,3       ;SET PASS SWITCH = 177777
19 06717 063611         SKPDN   TTO       ;DONE=?
20 06720 000414         JMP     IOX01     ;=0
21 06721 063511         SKPBZ   TTO       ;DONE=1 BUSY MUST=0
22 06722 063077         HALT              ;BUSY=0 OR DONE=1 FAILED
23 06723 063711         SKPDZ   TTO       ;DONE=1 ZERO SHD NOT SKP
24 06724 101001         MOV     0,0,SKP
25 06725 063077         HALT              ;"DZ" ERROR OR MAYBE "DN"
26 06726 063411         SKPBN   TTO       ;DONE=1 BUSY CAN'T=1
27 06727 002403         JMP     .ICX01-2  ;OK TO DO INTR TSTS
28 06730 063077         HALT              ;TTO IS NOT BUSY, BN ERROR
29 06731 000765         JMP     IOX00     ;LOOP BACK TEST TTO
30 06732 007157         INT00             ;DONE = 1, BUSY = 0, GO TO INTR TEST
31 06733 000500         A1A               ;START OF LOGIC TEST
32 06734 063511 IOX01:  SKPBZ   TTO       ;WAITING TTO TO FINISH ?
33 06735 002776         JMP     .,-2      ;BUSY, DON'T WAIT FOR TTO DONE
34 06736 175404         INC     3,3,SZR   ;NOT BUSY, DONE SET SINCE LAST TESTED ?
35 06737 063077         HALT              ;COUNT TO 0 FIRST TIME, 2ND TRY
36 06740 063711         SKPDZ   TTO       ;FINITE TIME TWXT "D" AND "BS"
37 06741 000756         JMP     IOX00+1   ;MAYBE DONE=1 (TIME LAPSE)
38
39                ;FALSE INTERRUPT TESTING:
40
41                ;TTO DONE AND BUSY=0
42                ;PERFORM TESTS THAT REQUIRE INTERRUPT TO BE FALSE
43 06742 102620 NIN00:  SUBZR   0,0       ;AC0:=100000
44 06743 040001         STA     0,LOC1    ;1=#0
45 06744 060177         NIOS    CPU       ;1 TO ION "SHD NOT SKP", INTEN
46 06745 063477         SKPBN   CPU       ;BUSY SHD=1 FOR CPU
47 06746 063077         HALT              ;ION DID NOT SET (NIOS SKPD)
48 06747 063477         SKPBN   CPU       ;ION=0 HERE IS FALSE INTR
49 06750 063077         HALT              ;SEE PI AND NOT INTR
50
51                ;THERE SHD BE NO INTR REQUESTS PENDING
52                ;NIOC SHD CLR ION SKPBZ SHD NOT SKP
53 06751 060177 NIN01:  NIOS    CPU       ;1 TO ION, INTEN
54 06752 063577         SKPBZ   CPU       ;BUSY=1
55 06753 063477         SKPBN   CPU       ;SHD NOT CLR ION
56 06754 063077         HALT              ;BZ SKPD OR BN DIDN'T
57 06755 060277 NIN02:  NIOC    CPU       ;SHD CLR ION
58 06756 063477         SKPBN   CPU       ;BUSY=0
59 06757 063577         SKPBZ   CPU
60 06760 063077         HALT              ;"C" DID NOT CLR ION
```

```
 0189 .MAIN
01
02                      ;IORST SHD CLR ION
03 06761 060177 NIN03:  NIOS    CPU     ;INTEN
04 06762 062677         IORST           ;DICC 0,CPU
05 06763 063577         SKPBZ   CPU
06 06764 063077         HALT            ;IORST FAILED CLR ION
07
08                      ;DIC SHD ONLY CLR IO BUS NOT ION
09 06765 060177 NIN04:  NIOS    CPU     ;INTEN
10 06766 062477         DIC     0,CPU   ;NO "C" ION SHD STILL=1
11 06767 063477         SKPBN   CPU     ;IR8,9=00 DID ION CLR
12 06770 063077         HALT            ;DIS CLRD ION IR8,9=00
13
14                      ;SAME TEST WITH "P" SHD NOT CLR ION IR8,9=11
15 06771 060177 NIN05:  NIOS    CPU     ;INTEN
16 06772 062777         DICP    0,CPU   ;IR8,9=11 "P" NOT "C"
17 06773 063477         SKPBN   CPU
18 06774 063077         HALT            ;"P" CLRD ION
19
20                      ;"P" PULSE SHD NOT SET ION
21 06775 060277 NIN06:  NIOC    CPU     ;INTDS
22 06776 060377         NIOP    CPU     ;IR8,9=11 "P" NOT "S"
23 06777 063577         SKPBZ   CPU
24 07000 063077         HALT            ;"P" SET ION
25
26                      ;"S" WITH ION=1 SHD LEAVE IT=1
27 07001 060177 NIN07:  NIOS    CPU     ;1 TO ION, INTEN
28 07002 062577         DICS    0,CPU   ;AGAIN WITH IORST
29 07003 063477         SKPBN   CPU
30 07004 063077         HALT            ;2ND "S" CLRD ION
31
32                      ;ION=1 AND SKPDN ON DEV 0 SHOULD NOT SKIP
33 07005 062677 NIN08:  IORST
34 07006 060177         NIOS    CPU     ;SET ION, INTEN
35 07007 063600         SKPDN   0       ;DEV #0 SHD NOT SKP
36 07010 101001         MOV     0,0,SKP
37 07011 063077         HALT            ;CPUINST IN IO SKIP
38
39                      ;TEST "AND'S" DECODING CPU INST FOR "FALSE"
40
41                              .MACRO IOTS2
42                              ;TEST DEVICE # 77, CPU DECODING,
43                      ;NIN11:
44                              IORST
45                              NIOS    CPU     ;SET ION FOR DEV 12, INTEN
46                              SKPBN    12     ;TEST NOT BIT 13
47                              MOV     0,0,SKP
48                              HALT            ;ONLY DEV 77 SHD SKP
49                              ;IF ABOVE HALT SEE BIT13 INTO "CPU INST" AND'S
50                      %
51
52                              IOTS2 09,76,15
53                              ;TEST DEVICE # 77, CPU DECODING,
54                      ;NIN09:
55 07012 062677         IORST
56 07013 060177         NIOS    CPU     ;SET ION FOR DEV 76, INTEN
57 07014 063476         SKPBN    76     ;TEST NOT BIT 15
58 07015 101001         MOV     0,0,SKP
59 07016 063077         HALT            ;ONLY DEV 77 SHD SKP
60                              ;IF ABOVE HALT SEE BIT15 INTO "CPU INST" AND'S
```

```
 0190 .MAIN
01
02                              IOTS2 10,75,14
03                              ;TEST DEVICE # 77, CPU DECODING.
04                    ;NIN10:
05 07017 062677                 IORST
06 07020 060177                 NIOS    CPU     ;SET ION FOR DEV 75, INTEN
07 07021 063475                 SKPBN    75     ;TEST NOT BIT 14
08 07022 101001                 MOV     0,0,SKP
09 07023 063077                 HALT            ;ONLY DEV 77 SHD SKP
10                              ;IF ABOVE HALT SEE BIT14 INTO "CPU INST" AND'S
11
12                              IOTS2 11,73,13
13                              ;TEST DEVICE # 77, CPU DECODING.
14                    ;NIN11:
15 07024 062677                 IORST
16 07025 060177                 NIOS    CPU     ;SET ION FOR DEV 73, INTEN
17 07026 063473                 SKPBN    73     ;TEST NOT BIT 13
18 07027 101001                 MOV     0,0,SKP
19 07030 063077                 HALT            ;ONLY DEV 77 SHD SKP
20                              ;IF ABOVE HALT SEE BIT13 INTO "CPU INST" AND'S
21
22                              IOTS2 12,67,12
23                              ;TEST DEVICE # 77, CPU DECODING.
24                    ;NIN12:
25 07031 062677                 IORST
26 07032 060177                 NIOS    CPU     ;SET ION FOR DEV 67, INTEN
27 07033 063467                 SKPBN    67     ;TEST NOT BIT 12
28 07034 101001                 MOV     0,0,SKP
29 07035 063077                 HALT            ;ONLY DEV 77 SHD SKP
30                              ;IF ABOVE HALT SEE BIT12 INTO "CPU INST" AND'S
31
32                              IOTS2 13,57,11
33                              ;TEST DEVICE # 77, CPU DECODING.
34                    ;NIN13:
35 07036 062677                 IORST
36 07037 060177                 NIOS    CPU     ;SET ION FOR DEV 57, INTEN
37 07040 063457                 SKPBN    57     ;TEST NOT BIT 11
38 07041 101001                 MOV     0,0,SKP
39 07042 063077                 HALT            ;ONLY DEV 77 SHD SKP
40                              ;IF ABOVE HALT SEE BIT11 INTO "CPU INST" AND'S
41
42                              IOTS2 14,37,10
43                              ;TEST DEVICE # 77, CPU DECODING.
44                    ;NIN14:
45 07043 062677                 IORST
46 07044 060177                 NIOS    CPU     ;SET ION FOR DEV 37, INTEN
47 07045 063437                 SKPBN    37     ;TEST NOT BIT 10
48 07046 101001                 MOV     0,0,SKP
49 07047 063077                 HALT            ;ONLY DEV 77 SHD SKP
50                              ;IF ABOVE HALT SEE BIT10 INTO "CPU INST" AND'S
```

```
!0191 .MAIN
01
02                      ;AN "S" PULSE WITH DEV 0 (NOT CPU INST)
03                      ;SHD NOT SET ION
04 07050 062677 NIN15:  IORST
05 07051 060100         NIOS    0       ;"NOT" CPU BUT "S"
06 07052 063577         SKPBZ   CPU     ;SEE 9301 GENERATIOG SETION
07 07053 063077         HALT            ;ION=1 ILLEGAL (CPU INST NOT)
08
09                      ;A "C" PULSE WITH DEV 0 (NOT CPU INST) SHD NOT CLR ION
10 07054 062677 NIN16:  IORST
11 07055 060177         NIOS    CPU
12 07056 060200         NIOC    0       ;NOT CPU BUT "C"
13 07057 063477         SKPBN   CPU     ;ION SHD STILL=1
14 07060 063077         HALT            ;"C" CLRD ION (NOT CPU=DEV 0)
15
16                      ;IO SKIPS SHD NOT GET TO PTS1 "S" SHO NOT BE GEN
17 07061 062677 NIN17:  IORST
18 07062 063577         SKPBZ   CPU     ;IR8,9=01 BUT IS NOT "S"
19 07063 063077         HALT
20 07064 063577         SKPBZ   CPU     ;ION SHD STILL=0
21 07065 063077         HALT            ;FIRST BZ GEN'D "S"
22
23                      ;IO SKIP "DN" SHD NOT="C" NO PTS1
24 07066 060177 NIN18:  NIOS    CPU
25 07067 063677         SKPDN   CPU     ;IR8,9=10 BUT IS NOT "C"
26 07070 101001         MOV     0,0,SKP ;POWER LOW=0 SHD NOT SKP
27 07071 063077         HALT            ;ON SKP'D WITH ION=1
28 07072 063477         SKPBN   CPU     ;ABOVE HALT SEE NOT IR8
29 07073 063077         HALT            ;"DN" CLRD ION
30
31                      ;SET UP ALL CONDITIONS FOR IO SKP EXCEPT IN/OUT TIME
32 07074 062677 NIN19:  IORST
33 07075 102420         SUBZ    0,0
34 07076 103577         ANDCL#  0,0,SBN ;EVERYTHING=0 NO SKP
35 07077 101001         MOV     0,0,SKP
36 07100 063077         HALT            ;AND=SKPBZ CPU
37
38                      ;SET UP ALL CONDITIONS FOR NIOS CPU EXCEPT PTS1
39 07101 062677 NIN20:  IORST
40 07102 102040         ADCO    0,0
41 07103 103177         COMCL#  0,0,SBN ;ALL=0 NO SKP
42 07104 063577         SKPBZ   CPU     ;ION SHD STILL=0
43 07105 063077         HALT            ;COMCL#=NIOS CPU
44
45                      ;SET UP ALL CONDITIONS FOR NIOS CPU
46                      ;EXCEPT ID ALCEN=0
47 07106 062677 NIN21:  IORST
48 07107 020177         LDA     0,177   ;NO IOALCEN
49 07110 063577         SKPBZ   CPU     ;SEE IOALCEN (NOT),PTS1
50 07111 063077         HALT            ;LDA=NIOS CPU
```

```
!0192 .MAIN
01
02                    ;SET UP ALL CONDITIONS FOR IO SKPBZ CPU EX(IN/OUT)
03 07112 176400 NIN22:  SUB     3,3       ;USING AN LDA
04 07113 054177         STA     3,LO177 ;MAKE SURE SKIP DOESN'T SET
05 07114 054000         STA     3,LOC0
06 07115 023577         LDA     0,#177,3 ;ALMOST AN SKPBZ CPU
07 07116 101004         MOV     0,0,SZR
08 07117 063077         HALT              ;LDA=SKPBZ CPU
09 07120 014210         DSZ     PKR00
10 07121 002404         JMP     #,+4
11 07122 020211         LDA     0,PKR01
12 07123 040210         STA     0,PKR00
13 07124 101001         MOV     0,0,SKP
14 07125 000500         A1A
15
16                    ;START DEL CODE TO TTO
17                    ;FOR INTERRUPT TESTING WHEN DONE=1
18 07126 102000 TTO00:  ADC     0,0       ;=1
19 07127 061011         DOA     0,TTO     ;OUT TO TTO, START XMIT
20 07130 060111         NIOS    TTO       ;SET BUSY
21 07131 063411         SKPBN   TTO       ;BUSY SHOULD = 1
22 07132 063077         HALT              ;NO SKIP TTO "BN"
23 07133 176440         SUBO    3,3       ;WAIT FOR UART TO MOVE
24 07134 063411         SKPBN   TTO       ;FIRST CHAR FROM
25 07135 000404         JMP     .+4       ;DATA BITS HOLDING REGISTER
26 07136 175403         INC     3,3,SNC ;TO TRANSMITTER SHIFT REGISTER,
27 07137 000775         JMP     .-3       ;WAIT SOME TIME, MAX ABOUT 120 MSEC,
28 07140 063077         HALT              ;NOT READY FOR NEXT CHAR,
29 07141 061011         DOA     0,TTO     ;OUT TO TTO, START XMIT
30 07142 060111         NIOS    TTO       ;SET BUSY
31 07143 063411         SKPBN   TTO       ;BUSY SHD=1
32 07144 063077         HALT              ;NO SKP TTO "BN"
33 07145 063511         SKPBZ   TTO       ;
34 07146 100004         COM     0,0,SZR
35 07147 063077         HALT              ;TTO "BZ" ERR
36 07150 063711         SKPDZ   TTO       ;DONE SHD=0 TTO
37 07151 063077         HALT              ;TTO "DS" ERR
38 07152 063611         SKPDN   TTO       ;TTO DONE SHD=0
39 07153 002403         JMP     #,+3      ;OK LOOP THROUGH TEST
40 07154 063077         HALT              ;TTO DONE=1 IN ERR
41 07155 002401         JMP     #,+1
42 07156 000500         A1A
```

```
!0193 .MAIN
01
02                ;TRUE INTERRUPT TESTING, COMING FROM LOOP IOX00
03
04                ;TTO DONE=1 USE TO TEST INTERRUPTS
05 07157 020416 INT00:  LDA     0,INT0K ;ADDR INT0K +1
06 07160 024207         LDA     1,JMP3K ;JMP @300
07 07161 030136         LDA     2,K2    ;SET UP FOR
08 07162 050001         STA     2,LOC1  ;TEST FIRST
09 07163 044002         STA     1,LOC2  ;REAL INTERRUPT
10 07164 040300         STA     0,LO300
11 07165 176400         SUB     3,3
12 07166 076077         DOB     3,CPU   ;@ MSK0
13 07167 054000         STA     3,LOC0  ;@ ADRS 0
14 07170 060177         NIOS    CPU     ;ION
15 07171 000401         JMP     .+1     ;WAIT
16 07172 063077         HALT            ;INTERRUPT DID NOT OCCUR
17 07173 063077         HALT
18 07174 007172         .-2
19 07175 007176 INT0K:  .+1
20 07176 034000         LDA     3,LOC0
21 07177 020775         LDA     0,INT0K-1
22 07200 116414         SUB#    0,3,SZR
23 07201 063077         HALT            ;(0) NOT=NIOS+2
24
25                ;TEST TO MAKE @IN LOC WILL DEFER
26 07202 020136 INT01:  LDA     0,K2    ;AND KEEP DEFERING
27 07203 103240         ADDOR   0,0     ;AC0:=100002
28 07204 040001         STA     0,LOC1  ;@2 ALSO=COM 0,0,SZC
29 07205 024207         LDA     1,JMP3K ;JMP @300
30 07206 044003         STA     1,LOC3  ;WILL EXECUTE IN ERR
31 07207 030414         LDA     2,INT1K ;IF FETCH IS DIRECTLY TO 1
32 07210 050300         STA     2,LO300 ;OR 2ND DEFER FAILS
33 07211 151400         INC     2,2     ;LEGAL RET
34 07212 050004         STA     2,LOC4  ;WILL BE IN 4
35 07213 103000         ADD     0,0     ;@4=COM 0,0,SZR (WON'T SKIP)
36 07214 103240         ADDOR   0,0     ;AC0:=100004
37 07215 040002         STA     0,LOC2  ;@4 TO LOC 2
38 07216 101020         MOVZ    0,0     ;0 CRY JMP @300 IN0
39 07217 060177         NIOS    CPU
40 07220 000401         JMP     .+1     ;FIRST INTR @@
41 07221 063077         HALT
42 07222 063077         HALT
43 07223 007224 INT1K:  .+1
44 07224 063077         HALT            ;LOC 1 OR 2 EXECUTED
45                      ;ABOVE HALT INTERRUPT IS NOT DOING @1
46                      ;OR DEFER BIT IN LOC 1 WAS NOT RECOGNIZED
47
48                ;ION/IOF SHOULD NOT INTR
49 07225 102400 INT02:  SUB     0,0     ;AC0:=000000
50 07226 040000         STA     0,LOC0
51 07227 101240         MOVOR   0,0     ;AC0:=100000=@0
52 07230 040001         STA     0,LOC1
53 07231 060177         NIOS    CPU     ;ION
54 07232 060277         NIOC    CPU     ;IOF
55 07233 000401         JMP     .+1     ;STALL
56 07234 024000         LDA     1,LOC0
57 07235 125004         MOV     1,1,SZR
58 07236 063077         HALT            ;INTR AFTER IOF
```

```
!0194 .MAIN
01
02                      ;MSKO=-1 SHD NOT ALLOW TTO INTR
03 07237 102000 INT03:  ADC     0,0
04 07240 062177         DOBS    0,CPU   ;MSKO=-1
05 07241 000401         JMP     .+1     ;STALL
06 07242 024000         LDA     1,LOC0  ;AWHILE
07 07243 063477         SKPBN   CPU
08 07244 063077         HALT            ;MASK0=1 ALLOWED TTO INTR
09 07245 125004         MOV     1,1,SZR
10 07246 063077         HALT            ;LOC 0 ALTERED
11 07247 102400         SUB     0,0
12 07250 062077         DOB     0,CPU   ;0'S TOM MASK 0
13 07251 000401         JMP     .+1     ;STALL WAIT FOT INTR
14 07252 024000         LDA     1,LOC0  ;INTR DID NOT OCCUR
15 07253 063577         SKPBZ   CPU     ;IF BZ NO SKP
16 07254 063077         HALT
17 07255 125005         MOV     1,1,SNR ;OR LOC0
18 07256 063077         HALT            ;WAS STILL=0
19
20                      ;INTERRUPT OVER A SKIP INSTRUCTION
21                      ;SDH STORE THE CORRECT ADDRESS IN LOC 0
22 07257 024407 INT04:  LDA     1,INT4K ;RET ADRS
23 07260 044001         STA     1,LOC1  ;TO LOC 1
24 07261 060177         NIOS    CPU     ;ION
25 07262 125005         MOV     1,1,SNR ;SET SKIP
26 07263 063077         HALT
27 07264 063077         HALT
28 07265 007264         .-1
29 07266 007267 INT4K:  .+1
30 07267 101001         MOV     0,0,SKP
31 07270 063077         HALT            ;INTR SKIPD
32 07271 020000         LDA     0,LOC0
33 07272 030773         LDA     2,INT4K-1 ;ADRS (LOC 0) SHD=
34 07273 142414         SUB#    2,0,SZR
35 07274 063077         HALT            ;(LOC 0) INCOR
36                      ;INTERRUPT OVER SKIP INST FAILED
37
38                      ;INTERRUPT AFTER AN I/O SKIP
39                      ;SHD STORE CORRECT RESULT IN LOC 0
40 07275 024407 INT05:  LDA     1,INT5K
41 07276 044001         STA     1,LOC1  ;RET ADRS
42 07277 060177         NIOS    CPU     ;ION
43 07300 063477         SKPBN   CPU     ;IO SKIP SET SKIP
44 07301 063077         HALT
45 07302 063077         HALT
46 07303 007302         .-1
47 07304 007305 INT5K:  .+1
48 07305 020000         LDA     0,LOC0  ;INTR SKP WILL MISS THIS
49 07306 030775         LDA     2,INT5K-1 ;VALID INTR ADRS
50 07307 142414         SUB#    2,0,SZR
51 07310 063077         HALT            ;INC PC IN LOC 0
```

```
!0195 .MAIN
01
02                ;INTERRUPT AFTER A JSR SHD STORE
03                ;THE CORRECT ADDRESS IN LOC 0
04 07311 030410 INT06:  LDA     2,INT6K
05 07312 050001         STA     2,LOC1
06 07313 153240         ADDOR   2,2       ;BIT 0 OF AC2=1
07 07314 060177         NIOS    CPU       ;ION JSR GOES .+2
08 07315 005375         JSR     -3,2      ;JSR ADRS CALC BIT 0=1
09 07316 063077         HALT
10 07317 063077         HALT              ;JSR/INT PREVENTS
11 07320 063077         HALT              ;EITHER HALT
12 07321 007322 INT6K:  .+1
13 07322 165401         INC     3,1,SKP   ;JSR+1 SHD=INTR ADRS
14 07323 063077         HALT
15 07324 020000         LDA     0,LOC0    ;GET (LOC 0)
16 07325 101112         MOVL#   0,0,SZC   ;BIT 0 MUST=0
17 07326 063077         HALT              ;BIT / LOC 0=1
18 07327 106414         SUB#    0,1,SZR   ;
19 07330 063077         HALT              ;LOC 0 OR AC3 INCORRECT
20                      ;LOC SHD=PC AFTER JSR (JSR+2)
21                      ;AC3 SHD=PC BEFORE JSR (JSR+1)
22                      ;NEITHER SHOULD HAVE BIT 0=1 -SEE CPB0-
23                      ;NOT SJR OR NOT ZEROBIT FORCES NOT CPB0
24 07331 014210         DSZ     PKR00
25 07332 002404         JMP     .,+4
26 07333 020211         LDA     0,PKR01
27 07334 040210         STA     0,PKR00
28 07335 101001         MOV     0,0,SKP
29 07336 000500         A1A
30 07337 014173         DSZ     TESTK
31 07340 101001         MOV     0,0,SKP
32 07341 000431         JMP     PASSC
33
34                .     ;FIRST LEVEL INTERRUPT TESTS COMPLETE'
35                ;CLR TTO DONE AND ION
36                ;REDO NON INT TESTS
37 07342 102620 INT07:  SUBZR   0,0       ;AC0:=100000=#0
38 07343 040001         STA     0,LOC1
39 07344 101120         MOVZL   0,0       ;AC0:=000000
40 07345 040000         STA     0,LOC0
41 07346 060177         NIOS    CPU
42 07347 062677         IORST
43 07350 000401         JMP     .+1
44 07351 024000         LDA     1,LOC0
45 07352 101004         MOV     0,0,SZR
46 07353 063077         HALT              ;IORST FAILED TO STOP INTERRUPT
47 07354 063511         SKPBZ   TTO
48 07355 063077         HALT              ;IORST DID NOT MAKE TTY BUSY=0
49 07356 063411         SKPBN   TTO
50 07357 101001         MOV     0,0,SKP
51 07360 063077         HALT              ;TTO DUSY SHD =0
52 07361 063711         SKPDZ   TTO
53 07362 063077         HALT              ;TTO DONE SHD =0 IORST
54 07363 063611         SKPDN   TTO
55 07364 101001         MOV     0,0,SKP
56 07365 063077         HALT
57 07366 063577         SKPBZ   CPU
58 07367 063077         HALT
59 07370 002401         JMP     .,+1
60 07371 006533         IO.00
```

```
 0196 .MAIN
01
02 07372 024172 PASSC:  LDA     1,K60
03 07373 044173         STA     1,TESTK
04 07374 024145         LDA     1,K400
05 07375 044211         STA     1,PKR01
06 07376 044210         STA     1,PKR00
07
08                      ;60 PASSES THROUGH INTERRUPT TESTS - PASS COMPLETE
09 07377 020202 PASST:  LDA     0,K215  ;TRY VARIOUS WAIT LOOPS
10 07400 061011         DOA     0,TTO   ;OUT CAR RET
11 07401 060111         NIOS    TTO
12 07402 063411         SKPBN   TTO     ;BUSY SHD=1
13 07403 063077         HALT
14 07404 063711         SKPDZ   TTO     ;DONE SHD=0
15 07405 063077         HALT
16 07406 063511         SKPBZ   TTO     ;WAIT LOOP
17 07407 000777         JMP     .-1     ;FIRST TIME THIS WAY
18 07410 063611         SKPDN   TTO     ;DONE=1 IF REAL "BZ"
19 07411 063077         HALT
20
21                      ;NOW OUTPUT LINE FEED
22 07412 024203         LDA     1,K212
23 07413 065011         DOA     1,TTO
24 07414 060111         NIOS    TTO
25 07415 063711         SKPDZ   TTO
26 07416 063077         HALT
27 07417 063411         SKPBN   TTO
28 07420 063077         HALT
29 07421 063611         SKPDN   TTO     ;FIRST SKIDN
30 07422 000777         JMP     .-1     ;WAIT LOOP
31 07423 063511         SKPBZ   TTO     ;BUSY=0 IF REAL DONE
32 07424 063077         HALT
33 07425 126620         SUBZR   1,1     ;AC1:=100000=-0
34 07426 044001         STA     1,LOC1
35
36                      ;TTO DONE=1 DO RESET WITHOUT "C" FOR CLR ION
37 07427 060177         NIOS    CPU     ;INTEN
38 07430 062477         DIC     0,CPU   ;IORST LESS "C" FOR ION
39 07431 000401         JMP     .+1     ;SHOULD CLEAR TTO DONE
40 07432 063477         SKPBN   CPU     ;INTERRUPT?
41 07433 063077         HALT            ;ION SHD STILL=1
42 07434 063711         SKPDZ   TTO
43 07435 063077         HALT            ;TTO DONE SHD=0
44
45                      ;OUTPUT P
46 07436 030206         LDA     2,K320
47 07437 071011         DOA     2,TTO
48 07440 060111         NIOS    TTO
49 07441 063577         SKPBZ   CPU     ;ION STILL=1
50 07442 000777         JMP     .-1     ;WHEN IT=0 TTO DONE
51 07443 063611         SKPDN   TTO     ;TTO DONE=0
52 07444 063077         HALT            ;BZ BEFORE INTR
53 07445 075477         INTA    3
54 07446 024205         LDA     1,KTTO
55 07447 136414         SUB#    1,3,SZR ;KSP DEV# OK
56 07450 063077         HALT            ;NOT "TTO" ON INTA
57 07451 060211         NIOC    TTO     ;CLEAR TTO DONE
```

```
!0197 .MAIN
01
02                    ;OUTPUT "A"
03 07452 034160       LDA     3,K300
04 07453 175400       INC     3,3
05 07454 060177       NIOS    CPU
06 07455 075011       DOA     3,TTO
07 07456 060111       NIOS    TTO
08 07457 000401       JMP     .+1
09 07460 063477       SKPBN   CPU       ;ION SHD STILL=1
10 07461 063077       HALT
11 07462 020166 PASL1: LDA    0,KCBO
12 07463 126000       ADC     1,1       ;DO ZOR'S
13 07464 131000       MOV     1,2       ;WHILE WAITING
14 07465 113520       ANDZL   0,2       ;ODD BITS XOR'D TO
15 07466 107000       ADD     0,1       ;-1=EVEN BITS
16 07467 146400       SUB     2,1       ;XOR'D TO -1
17 07470 152000       ADC     2,2       ;AGAIN SHOULD=
18 07471 155000       MOV     2,3       ;THE ODD BITS
19 07472 137520       ANDZL   1,3
20 07473 133000       ADD     1,2
21 07474 172400       SUB     3,2
22 07475 142414       SUB#    2,0,SZR
23 07476 063077       HALT              ;PROCESSOR ARITH ERROR
24 07477 063577       SKPBZ   CPU       ;INTR OCCUR YET
25 07500 000762       JMP     PASL1     ;NO
26 07501 063611       SKPDN   TTO       ;TTO YES DONE=1
27 07502 063077       HALT              ;NO ERROR AT "BZ"
28
29                    ;INTERRUPT SHOULD OCCUR DURING A
30                    ;STRING OF IO INSTRUCTIONS OUTPUT FIRST S
31 07503 030204       LDA     2,K323
32 07504 102400       SUB     0,0
33 07505 040000       STA     0,LOC0
34 07506 061000       DOA     0,0
35 07507 071011       DOA     2,TTO     ;OUTPUT FIRST S
36 07510 060111       NIOS    TTO
37 07511 060177 PASL2: NIOS   CPU
38 07512 060200       NIOC    0
39 07513 063577       SKPBZ   CPU
40 07514 063477       SKPBN   CPU
41 07515 060000       NIO     0
42 07516 065477       INTA    1
43 07517 060300       NIOP    0
44 07520 074477       DIA     3,CPU
45 07521 060400       DIA     0,0
46 07522 060100       NIOS    0
47 07523 061000       DOA     0,0
48 07524 060277       NIOC    CPU
49 07525 034000       LDA     3,LOC0
50 07526 175005       MOV     3,3,SNR
51 07527 000762       JMP     PASL2     ;WAIT FOR INTR
52 07530 024204       LDA     1,K323
53 07531 132414       SUB#    1,2,SZR
54 07532 063077       HALT
55 07533 101004       MOV     0,0,SZR
56 07534 063077       HALT
57 07535 071011       DOA     2,TTO     ;OUTPUT SECOND S IN PASS
58 07536 060111       NIOS    TTO
59 07537 002401       JMP     .,+1
60 07540 000500       A1A
```

```
 0198 .MAIN
01
02
03                          ;TAPE 5          ;REBIN;=220 IN MKABS (RDOS) WILL GIVE
04
05                          .END REBIN       ;BINARY TAPE THIS SELFSTART BLOCK
```

A1A	000500	70/56	72/43	76/11	188/31	192/14	192/42	195/29
		197/60						
A1B	000503	76/18						
A1C	000506	76/25						
A1D	000511	76/32						
A1E	000514	76/39						
A1F	000517	76/46						
A1G	000522	76/53						
A20	001024	86/05						
A21	001026	86/11						
A22	001031	86/17						
A23	001034	86/26						
A24	001037	86/31						
A25	001042	86/37						
A2A	000525	77/11						
A2B	000530	77/18						
A2C	000533	77/25						
A2D	000536	77/32						
A2E	000541	77/39						
A2F	000544	77/46						
A2G	000547	77/53						
A3A	000552	78/11						
A3B	000555	78/18						
A3C	000560	78/25						
A3D	000563	78/32						
A3E	000566	78/39						
A3F	000571	78/46						
A3G	000574	78/53						
A40	001221	92/18						
A41	001225	92/25						
A42	001231	92/31						
A43	001235	92/37						
A44	001240	92/45						
A45	001244	93/05						
A46	001246	93/09						
A47	001251	93/14						
A48	001255	93/21						
A49	001261	93/29						
A4A	000577	79/11						
A4B	000602	79/18						
A4C	000605	79/25						
A4D	000610	79/32						
A4E	000613	79/39						
A4F	000616	79/46						
A4G	000621	79/53						
A50	001265	93/38						
A51	001272	93/45						
A5A	000624	80/11						
A5B	000627	80/18						
A5C	000632	80/25						
A5D	000635	80/32						
A5E	000640	80/39						
A5F	000643	80/46						
A5G	000646	80/53						
A6A	000651	81/11						
A6B	000654	81/18						
A6C	000657	81/25						
A6D	000662	81/32						
A6E	000665	81/39						

```
01
02                ;TAPE 6
03                        ;THIS TAPE IS USED TO PRODUCE THE FOURTH BLOCK ON THE
04                        ;BINARY TAPE FOR RC 3600 CPU LOGIC TEST.
05                        ;THIS TAPE SHOULD BE ASSEMBLED ALONE BY THE EXT. ASM,
06                        ;PRODUCING A START BLOCK IN ABS-BIN FORMAT.
07
08
09                        ;THE BINARY TAPE FOR RC 3600 CPU LOGIC TEST IS PRODUCED
10                        ;BY PUNCHING THIS 4 BLOCKS AS ONE BINARY TAPE:
11                        ;       1. S-BIN HEAD
12                        ;       2. ABS-BIN BLOCK PRODUCED FROM ASCII TAPE 1 - 5
13                        ;          BY MACRO ASM, RLDR AND MKABS.
14                        ;          (MKABS DEFINES START ADDR = 220)
15                        ;       3. S-BIN HEAD
16                        ;       4. START BLOCK PRODUCED FROM ASCII TAPE 6.
17
18                        ;IF GENERATING DISC OR MAG. TAPE WITH THIS PROGRAM
19                        ;INCLUDED, ONLY BLOCK 2 SHOULD BE USED.
20
21        000232          BAUTO=232
22
23                ;TAPE 6
24
25
26        000232 ,END BAUTO
0002  ,MAIN

BAUTO   000232      1/21    1/26
```