Title:

Technical Manual for FDC 705 Flexible Disk Controller

A/S REGNECENTRALEN

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FDC 705, FDD 705

Abstract:

This paper contains drawings and technical information for the FDC 705 Flexible Disk Controller.

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1. Description. 1.

The FDC 705 Flexible Disk Controller is designed to interface up to four flexible disk drivers to the CPU with a minimum of software handling. This is achieved by transfer of data, parameters and commands via the DMA channel. As an extra feature data is converted using a RAM code conversion table loaded from the CPU.

Besides the DMA channel the CPU and the controller communicates by means of several flags (refer to fig. 1.1). The control of the flags and a base address is the only information transferred by programmed I/O instructions.

Flag Name	Number of flags	Description
START	4	Set by the CPU to start the execution of a command
STOP	4	Set by the CPU to stop the execution of a command
DONE	4	Set by the FDC to indicate the execution of a command has ended
AUTOLOAD	1	Set by the CPU to make the FDC perform an autoload function

Fig. 1.1 CPU communication flags

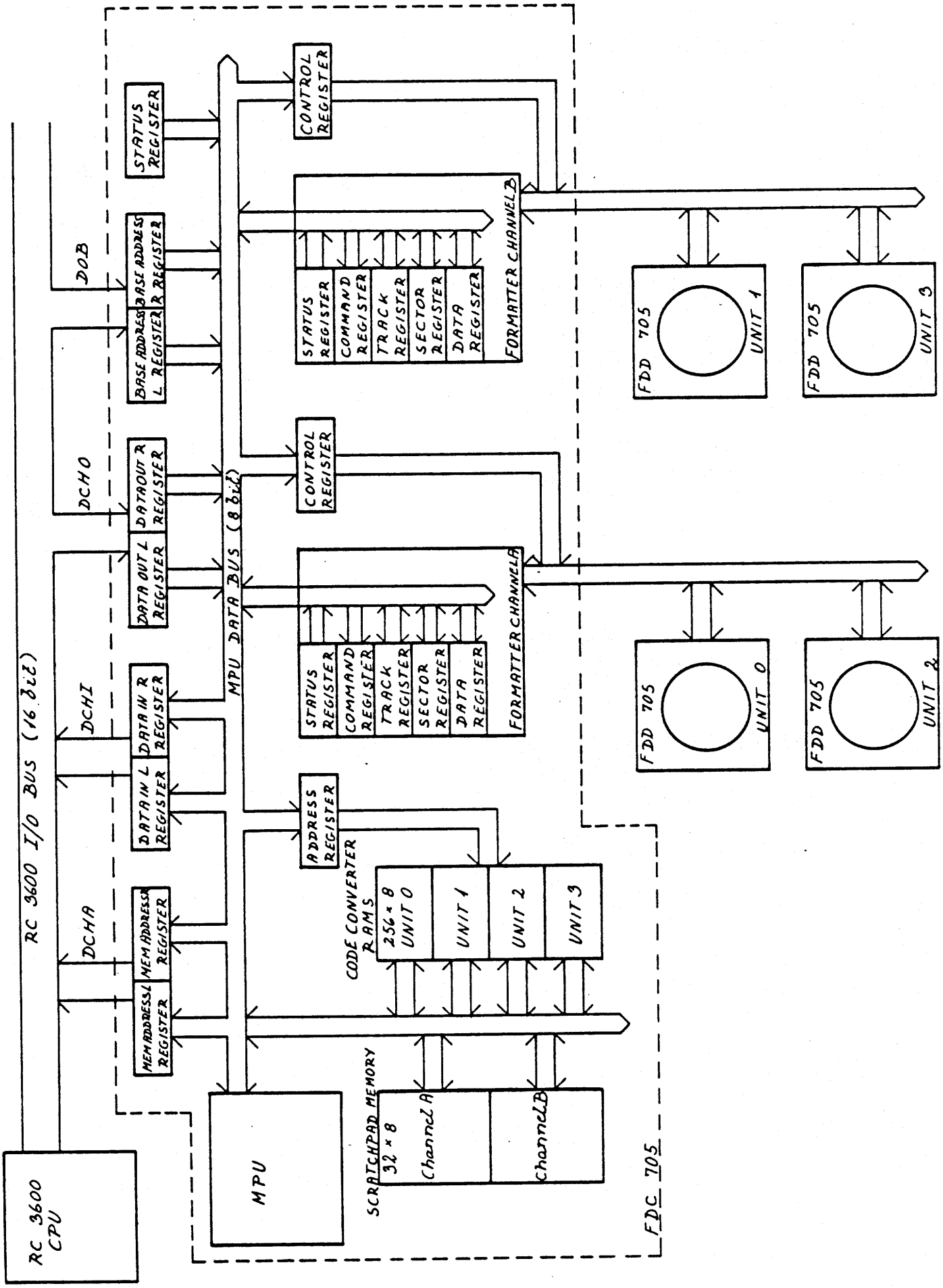
The heart of the FDC 705 is microprocessor which controls all the logic and data flow inside the controller. A 2K x 8 bit Read Only Memory contains the microprogram.

Two Floppy Disk Formatter chips are used in the controller. These chips perform the seriel/parallel data translation, the CRC generating and checking, the address mark detection and verification as well as other Flexible

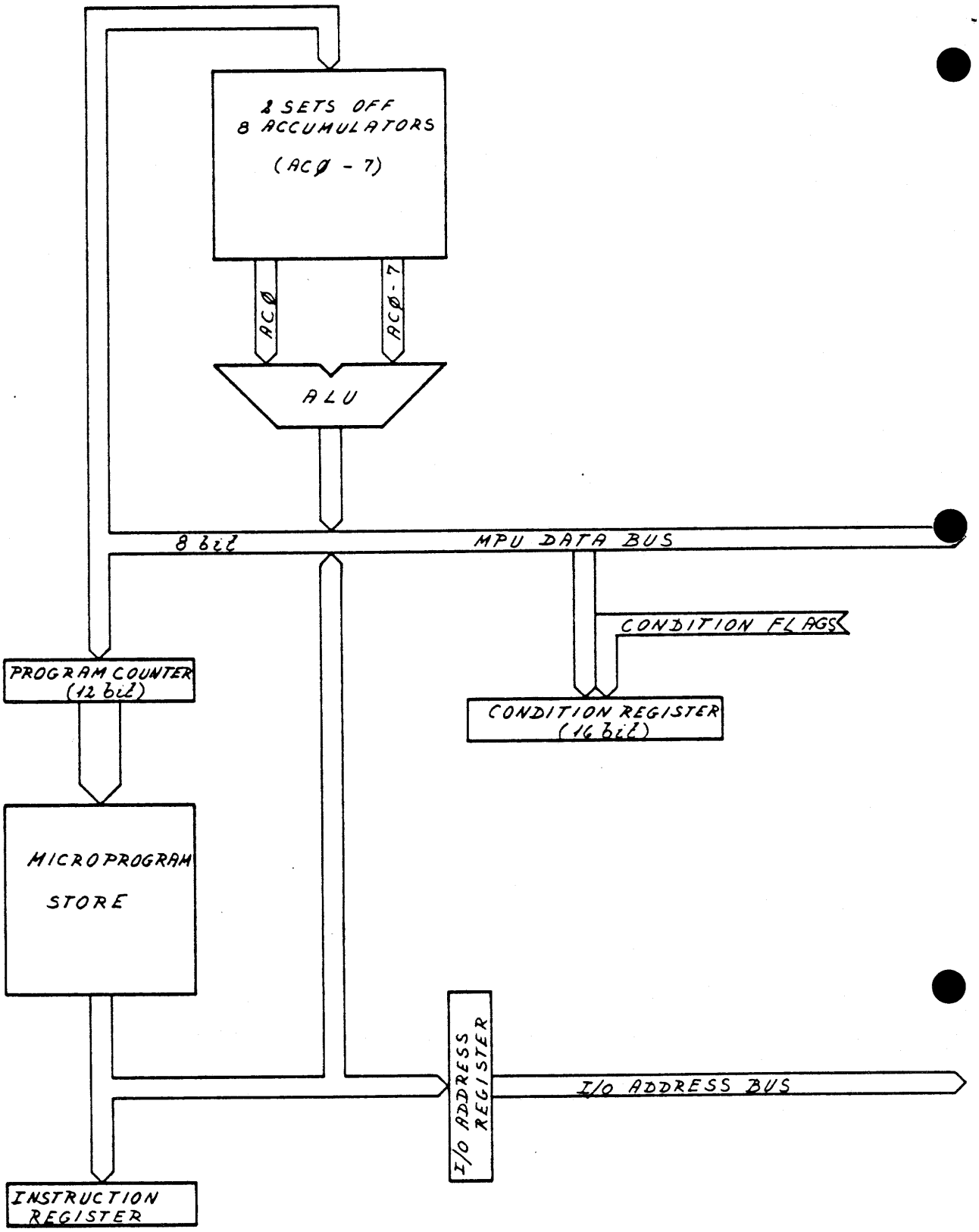
Disk interface control functions.

The two formatter chips make up two channels to which drives can be connected. Two drives can be connected to each channel, but drives connected to the same channel cannot be operated simultaneously. The daisy-chained drives are operated alternately whereas drives at different channels (having their own formatter) are time-sliced by the microprocessor and operated simultaneously.

2. BLOCK DIAGRAMS



Logic Structure of FDC 705



FDC 705 Logic Structure of Micro Processor Unit (MPU)

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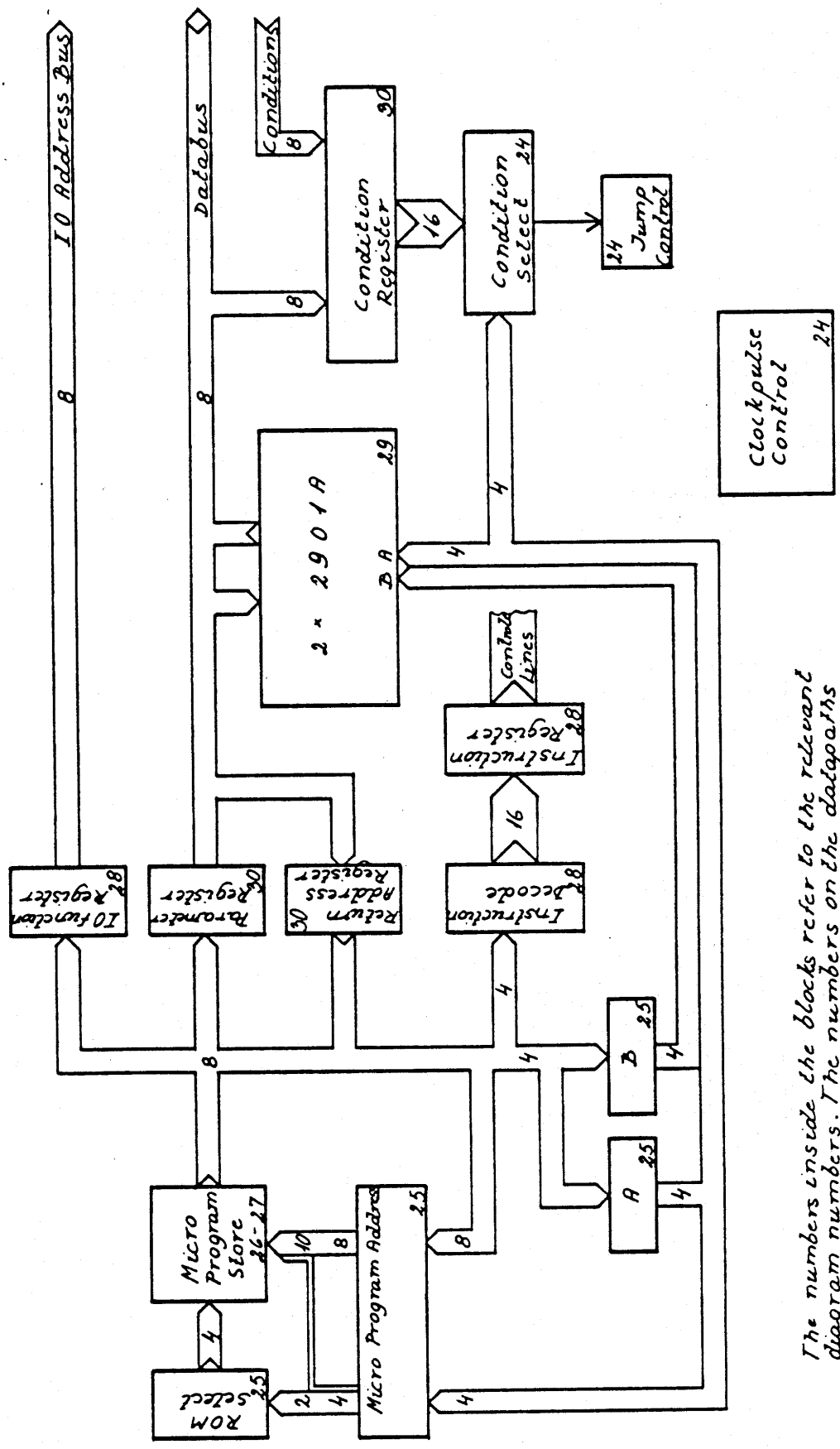

The numbers inside the blocks refer to the relevant diagram numbers. The numbers on the datapaths indicates the path-width.

FDC 705 Internal Microprocessor Datapaths

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3. The Microprocessor.

Section 2.2 contains a block diagram of the logic structure of the microprocessor and section 2.3 contains a functional block diagram. The logic diagrams are found on page 21 to 81. (Diagram numbers FDC24-FDC30)

3.1 MPU Programmers Reference.

The microprocessor used in the FDC 705 (hereafter called MPU) is a 8 bit processor, containing 2 sets (one for each channel) of 8 accumulators (ACØ-AC7).

The instruction repertoire is made up by sixteen instructions. (Refer to fig. 3.1).

The program address-space is 4K bytes of which all 4K must be Read-Only-Memory. Besides the accumulators random access storage is not provided within the MPU. However, a scratchpad memory (32 bytes for each channel) connected to the data bus is available for data storage. This RAM is treated as 32 external registers.

The program store is divided into pages each containing 256 bytes. Conditional branching and subroutine returns are only possible within the current page.

The various registers in the FDC 705 controller are accessed from the MPU using the input/output instructions (IN, OUT and FUT). In fig. 3.2 the four main groups of addresses are listed. Fig. 3.3 contains a complete I/O address list.

Some of the addresses are shared by two identical registers, one for each channel (e.g. the formatter chip registers). A Flip Flop determins whether the channel A or B register is selected. The flip flop is toggled by

an output instruction to address 7 octal. Also identical status signals from the two channels are demultiplexed by the flip flop.

This means that reentrant program code can be used to serve both channels. The program need not worry whether channel A or B is operated: The two channels are logically identical.

Besides the channel select flip flop, another select flag (actually two, one for each channel) is provided.

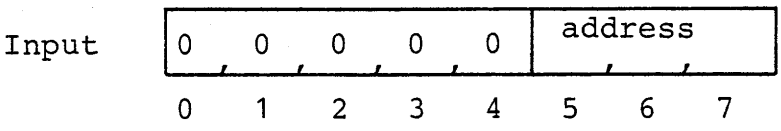
This select flag together with the channel select flip flop indicates the current unit (one of four), and the two bits are used to divide the code converter into four as well as to demultiplex identical status signals from the four units (e.g. the start flag).

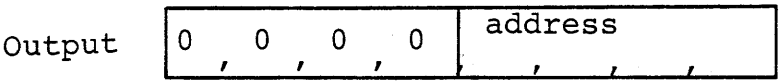
When resetting the controller by a CLEAR-pulse or an IORST instruction the program counter is reset. The MPU therefore always starts the program execution in location Ø. The instruction stored in this location must be a single byte instruction.

Mnemonic	Instruction layout	Execution time (msec)	Description
ADD A	0 0 0 0 | X | A	160	AC(Ø): = AC(Ø)+ AC(A)
SUB A	0 0 0 1 | X | A	160	AC(Ø): = AC(Ø)- AC(A)
AND A	0 0 1 0 | X | A	120	AC(Ø): = AC(Ø) AND AC(A)
XOR A	0 0 1 1 | X | A	120	AC(Ø): = AC(Ø) EXOR AC(A)
INC A	0 1 0 0 | X | A	160	AC(A): = AC(A) + 1
DEC A	0 1 0 1 | X | A	160	AC(A): = AC(A) - 1
OR A	0 1 1 0 | X | A	120	AC(A): = AC(A) OR AC(Ø)
MOV A	0 1 1 1 | X | A	120	AC(A): = AC(Ø)
LD A,D	1 0 0 0 | X | A D	200	AC(A): = D (load immediate)
IN A,EXT	1 0 0 1 | X | A EXT	min. 240	AC(A): = Register (EXT) (Input)
OUT A,EXT	1 0 1 0 | X | A EXT	min. 240	Register (EXT): = AC(A) (output)
FUT A,EXT	1 0 1 1 | X | A EXT	200	Operates as OUT, but cannot wait for external events
JMP L	1 1 0 0 | MSB(L) LSB(L)	200	MPA: = L (Jump to L)
BRT COND,L	1 1 0 1 | COND L	200	If condition (COND) then LSB(MPA): = L (Branch on condition true)
BRF COND,L	1 1 1 0 | COND L	200	If -, condition (COND) then LSB(MPA): = L (Branch on condition false)
RTN A	1 1 1 1 | X | A	200	LSB(MPA): = AC(A) (Subroutine Return)

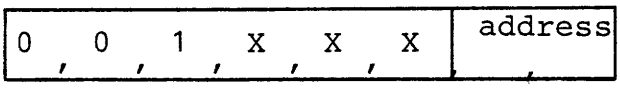
Fig. 3.1 MPU Instruction set

Descrete registers and Control Signals

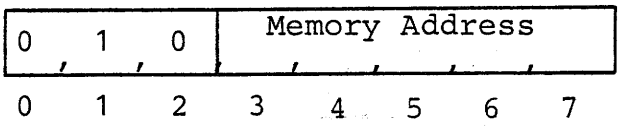




Formatter Chip



Scratchpad Memory



Code Converter

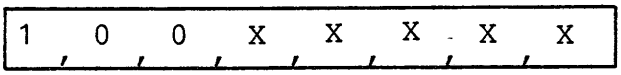


Fig. 3.2
I/O address groups

Address (octal)	Input	Mnemonics	Output	Mnemonics
0	BASE ADDRESS R	BSADR	MEM ADDRESS R	MADDR
1	BASE ADDRESS L	BSADL	MEM ADDRESS L	MADDL
2	DATA OUT R	DOUTR	DATA IN R	DAINR
3	DATA OUT L	DOUTL	DATA IN L	DAINL
4	STATUS	STATS	CONTROL REG	CNTRL
5	SPARE		ADDRESS REG	ADDRG
6	SPARE		CHANGE UNIT	CUNIT
7	SPARE		CHANGE CHANNEL	CCHNL
10			SET DONE	SDONE
11			CLEAR START	CSTRT
12			CLEAR STOP	CLSTP
13			CLR INDEX COUNTER	CICNT
14				
15				
16				
17				
20-37	Not used			
40	FORMATTER STATUS	FSTAT	FORMATTER COMMAND	FCMD
41	TRACK REGISTER	FTRCK	TRACK REGISTER	FTRCK
42	SECTOR REGISTER	FSCTR	SECTOR REGISTER	FSCTR
43	READ DATA	FDATA	WRITE DATA	FDATA
44-77	Not used			
100-137	Scratchpad Memory			
140-177	Not used			
200-237	CODE CONVERTER	CDCNV	CODE CONVERTER	CDCNV
240-377	Not used			

Fig. 3.3

Microprocessor I/O Address-assignment

BRANCH CONDITIONS

Value of COND field (octal)	Selected condition	Mnemonics
0	MPU DATA BUS (0)	DATAØ
1	- (1)	- 1
2	- (2)	- 2
3	- (3)	- 3
4	- (4)	- 4
5	- (5)	- 5
6	- (6)	- 6
7	- (7)	- 7
10	Formatter Data request	DRQ
11	Stop flag	STOP
12	Data channel busy	DMABS
13	Autoload flag	AUTLD
14	Formatter interrupt	INT
15	ALU overflow	OVFLW
16	ALU carry out	CARRY
17	ALU result zero	ZERO

Fig. 3.4 Condition Register bit assignment

STATUS REGISTER (STATS)

Bit No.	Definition
0	Index cnt 16
1	start flag
2	Drive ready
3	Drive spindle motor off
4	HLD
5	Diskette not double sided
6	Unit (0)
7	Unit (1) (= channel)

Fig. 3.5 Status Register bit assignment

CONTROL REGISTER (CNTRL)

Bit No.	Definition
0	Select unit 0 (or 1)
1	Select unit 2 (or 3)
2	Head Load 0 (or 1)
3	Head Load 2 (or 3)
4	Not used
5	Not used
6	Not used
7	Select side two

Fig. 3.6 Control Register Bit assignment

3.2 Program Description. 3.2

The following section contains flowcharts to illustrate the fundamental program flow. On the charts relevant labels from the program source text is listed.

Except for the Power Up Modul and the Autoload Modul the microprogram is in fact two reentrant coroutines and a coroutine monitor. The mechanism of the shifts between the two coroutines is illustrated by the following example.

Assume the processor operates on channel A (i.e. coroutine A is activ) and that accumulator 7 (AC7) for channel B contains the address RTN2. The coroutine now executes a monitor call:

```
        JMP    CH1
LAB1:   ....
```

To this call a specific monitor atom corresponds (located on page Ø):

```
CH1:    LD    7,RTN1
        FUT   0,CCHNL
        RTN   7
RTN1:   JMP   LAB1
```

This program segment performs the following function:

1. The program counter for coroutine A is saved in AC 7

2. The channel select flip flop is toggled causing among other things the channel A and B accumulators to be swapped

3. The contents of AC7 (for channel B) are loaded into the program counter causing a jump to RTN2.

The address RTN2 is an address in another monitor atom (it might be the same):

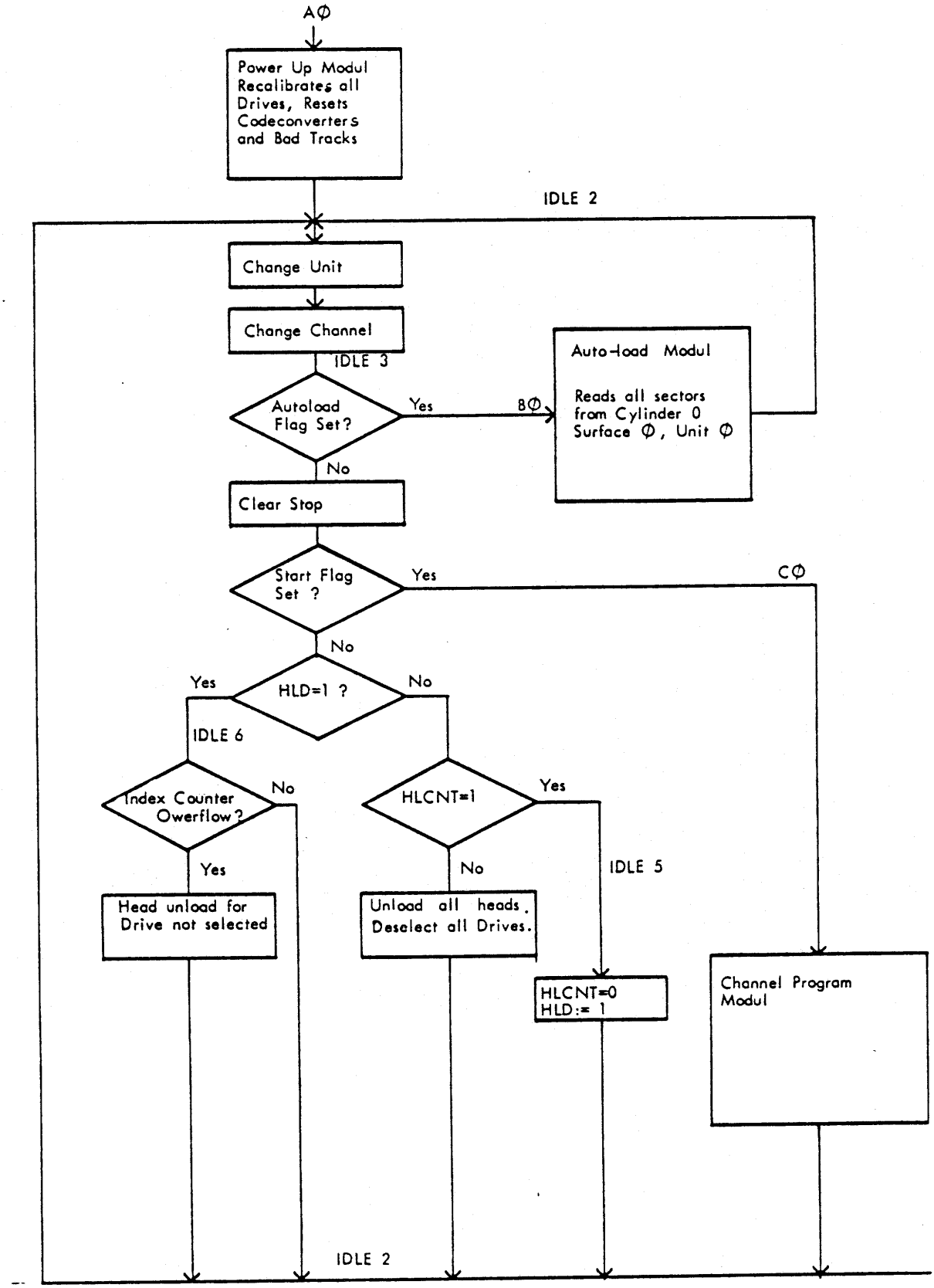
```
CH2:    LD    7,RTN2
        FUT   0,CCHNL
        RTN   7
RTN2:   JMP   LAB2
```

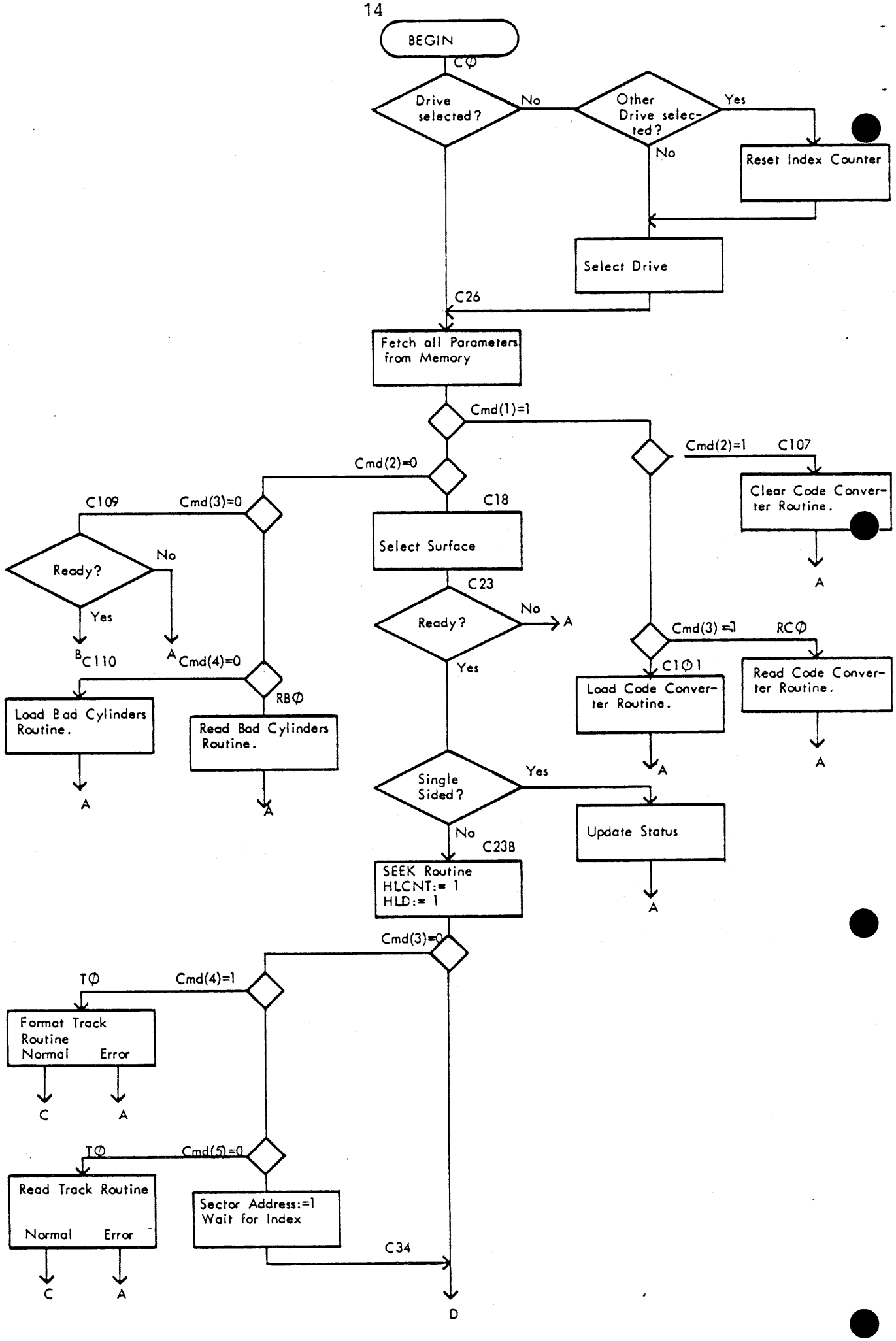
The program execution now continues in coroutine B from the last monitor call:

```
        JMP   CH2
LAB2:
```

The situation is now similar to the start conditions except that coroutine B is active. When routine B reaches a monitor call, routine A is started in address LAB1.

3.3 Flow Diagrams





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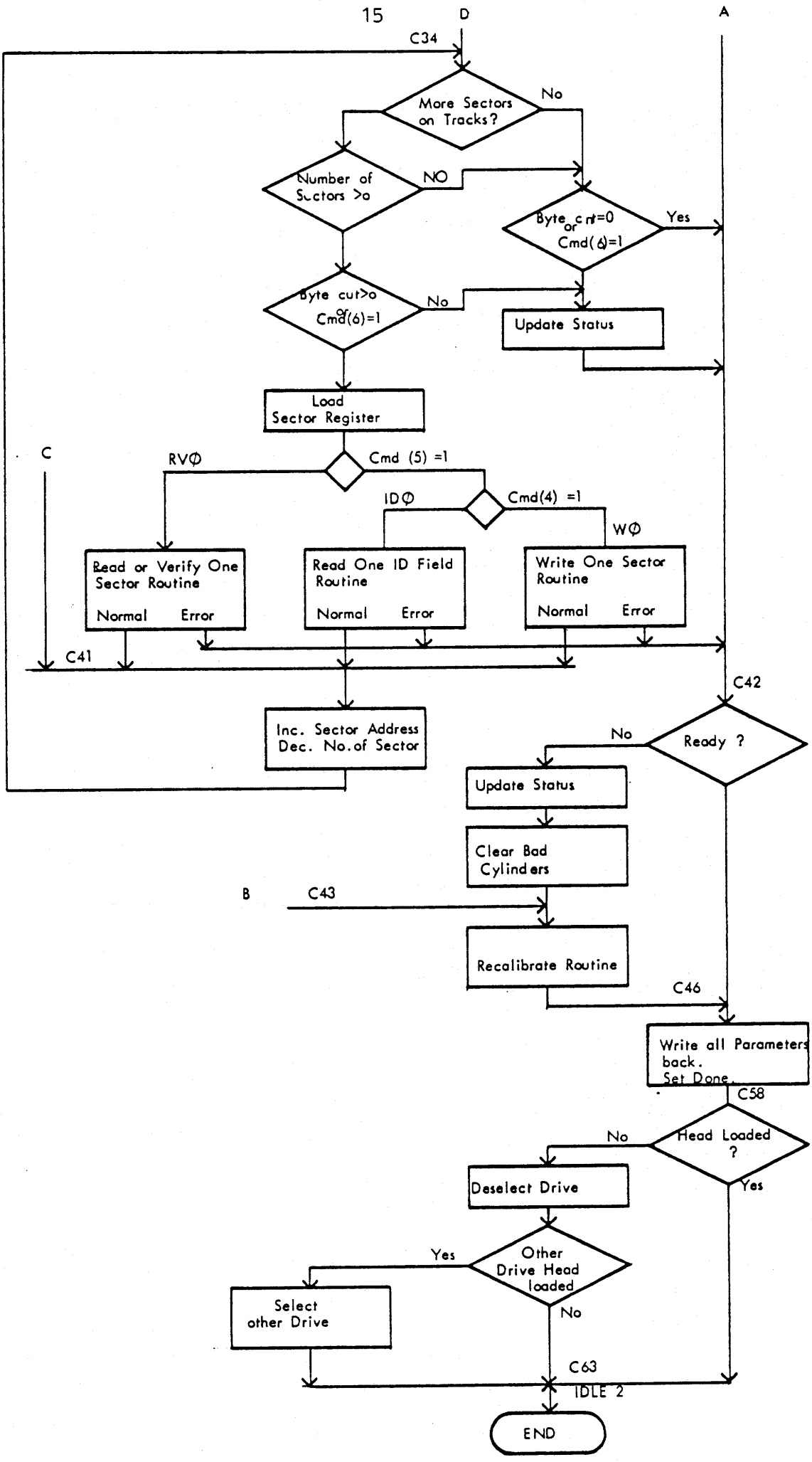
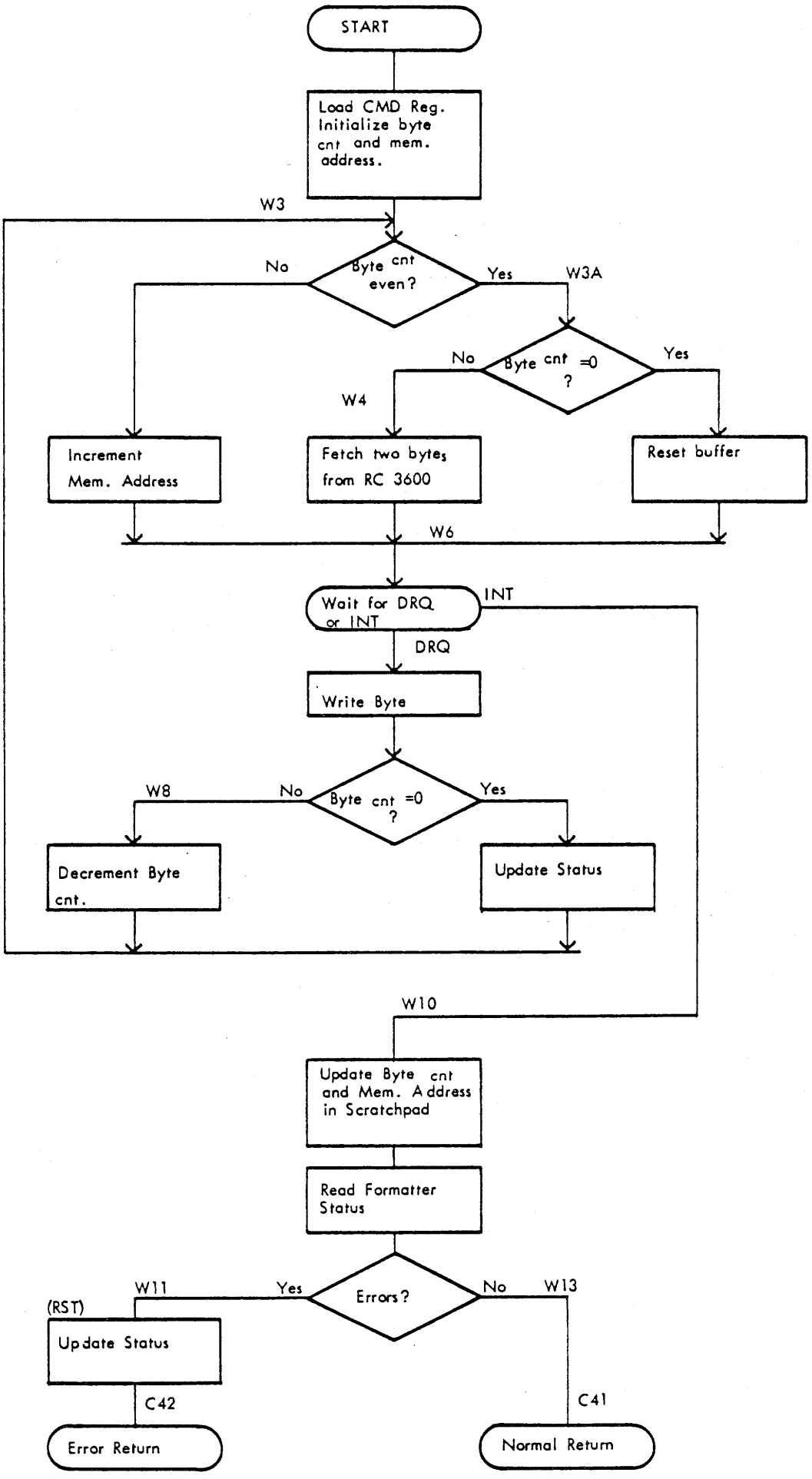
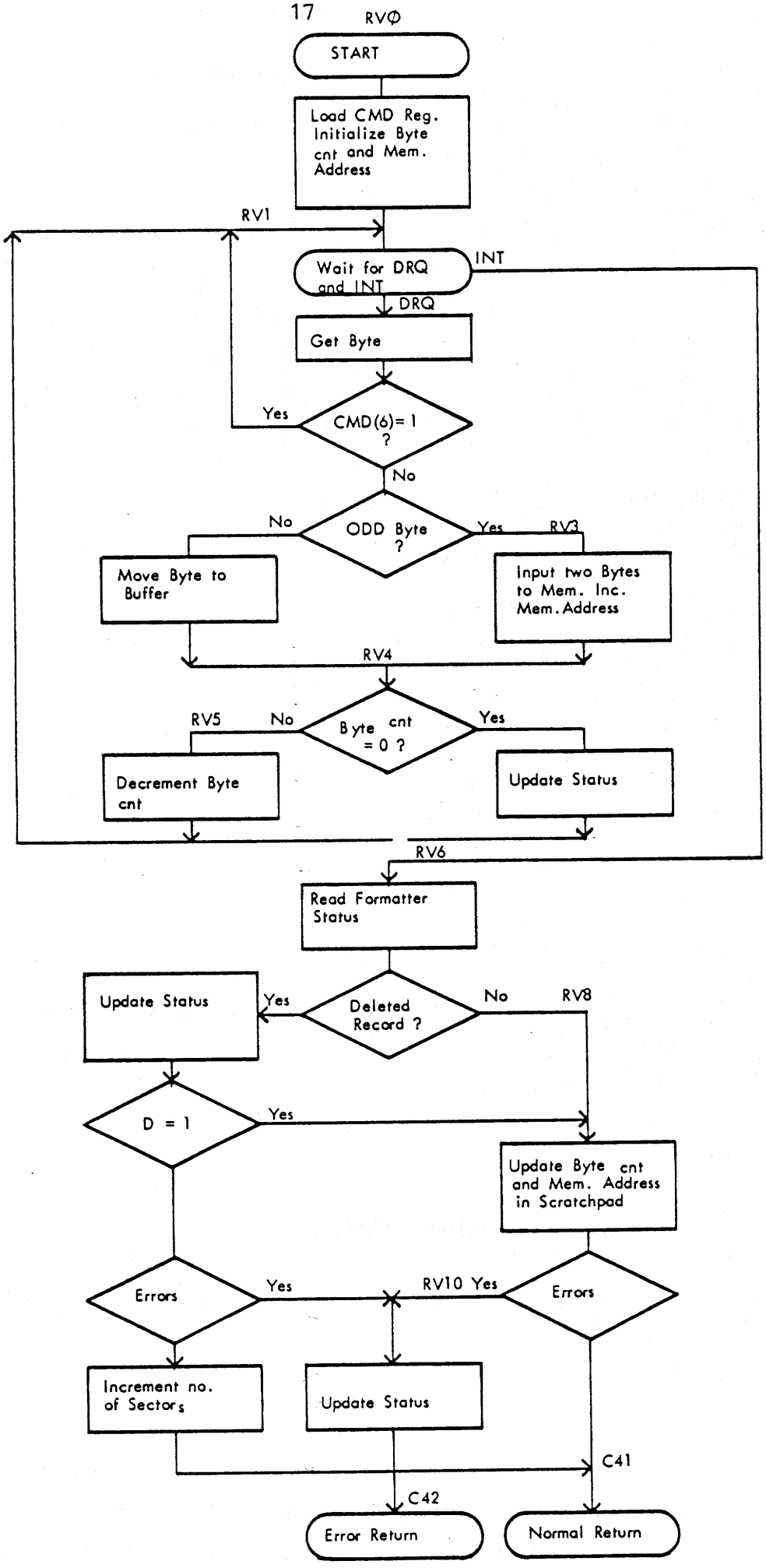
MICROPROGRAM STRUCTURE
CHANNEL PROGRAM MODUL I



MICROPROGRAM STRUCTURE
CHANNEL PROGRAM MODUL II



MICROPROGRAM STRUCTURE
WRITE ONE SECTOR ROUTINE.



MICROPROGRAM STRUCTURE
READ OR VERIFY ONE SECTOR ROUTINE

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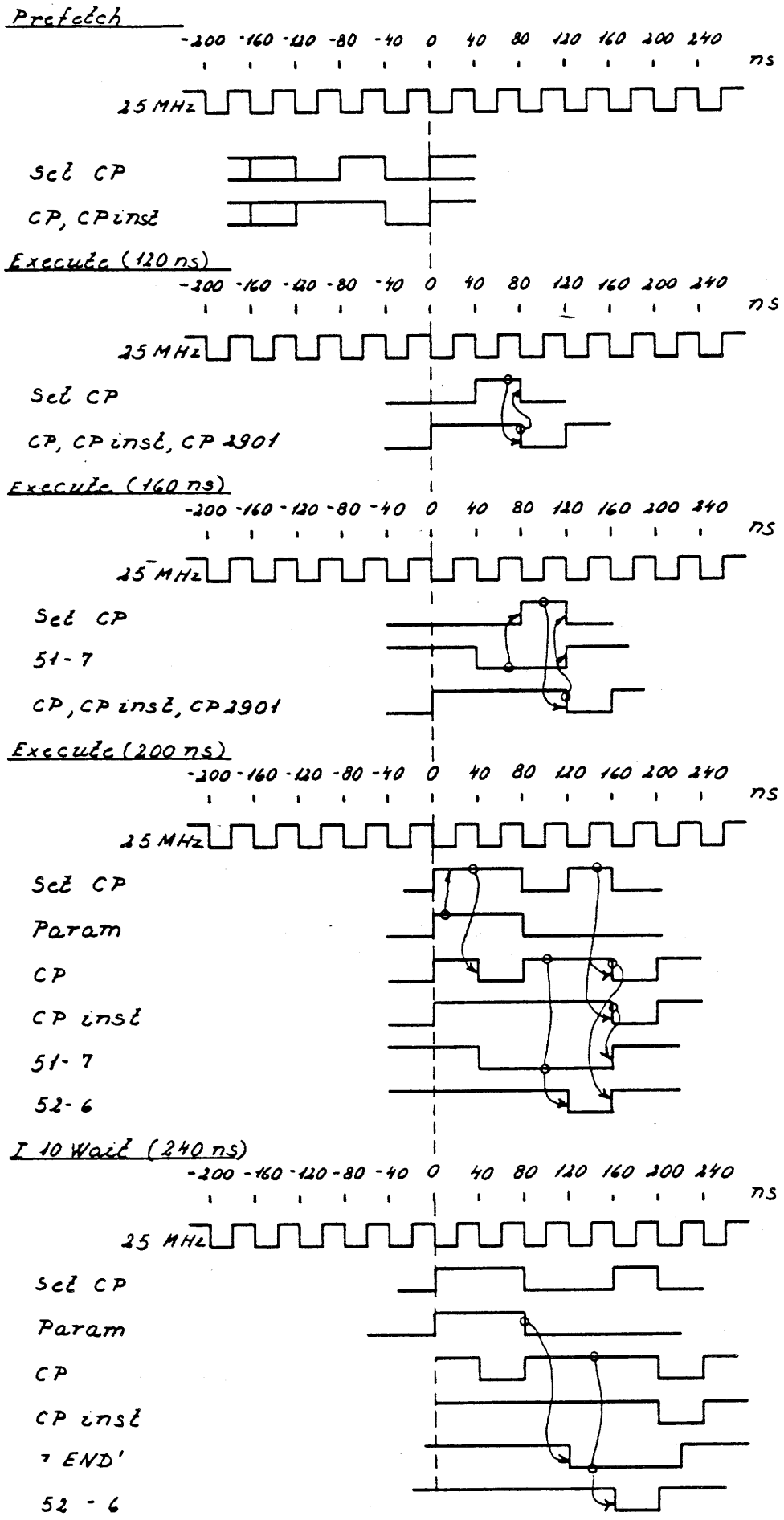

FDC 705 MPU Clock Control Timing

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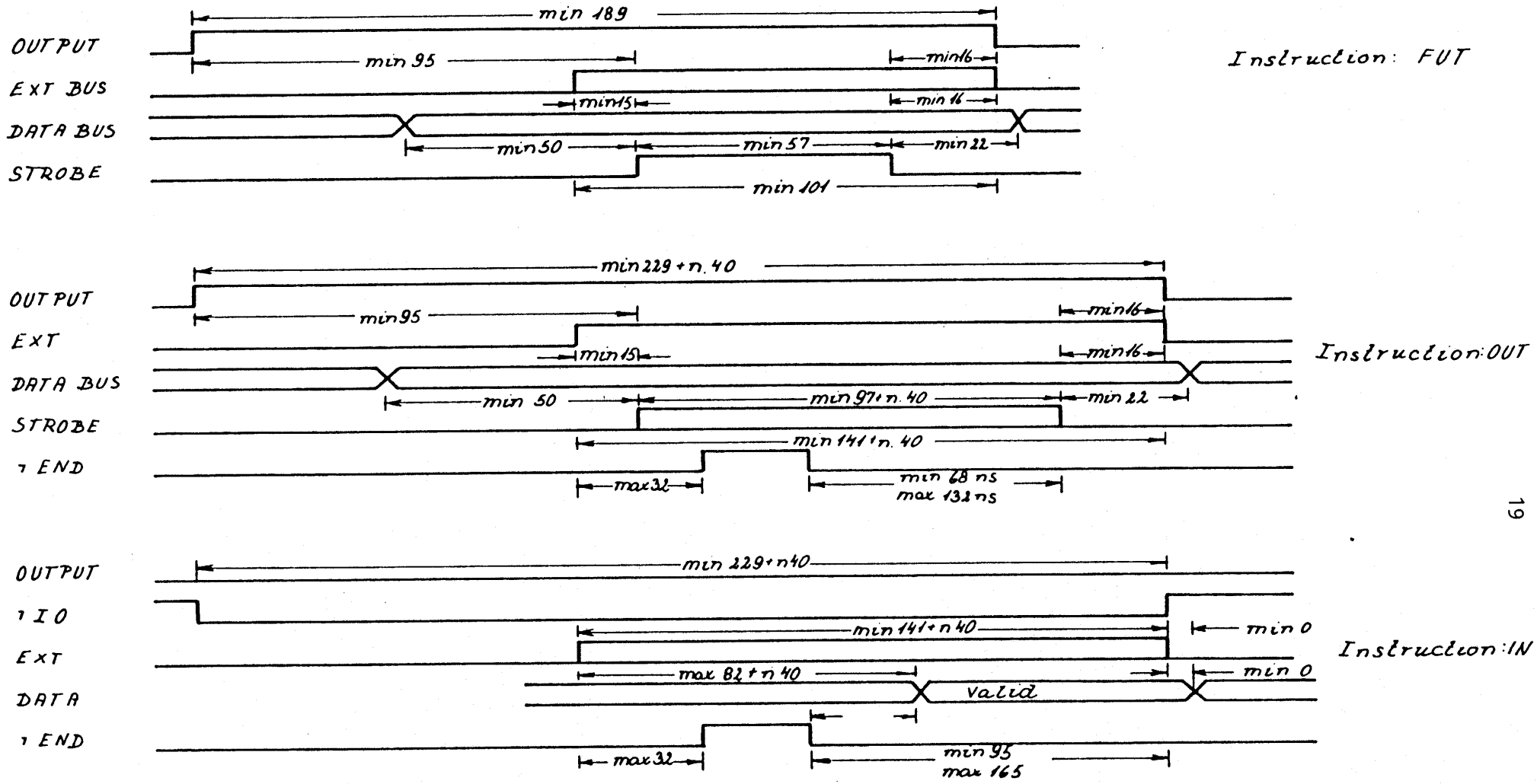
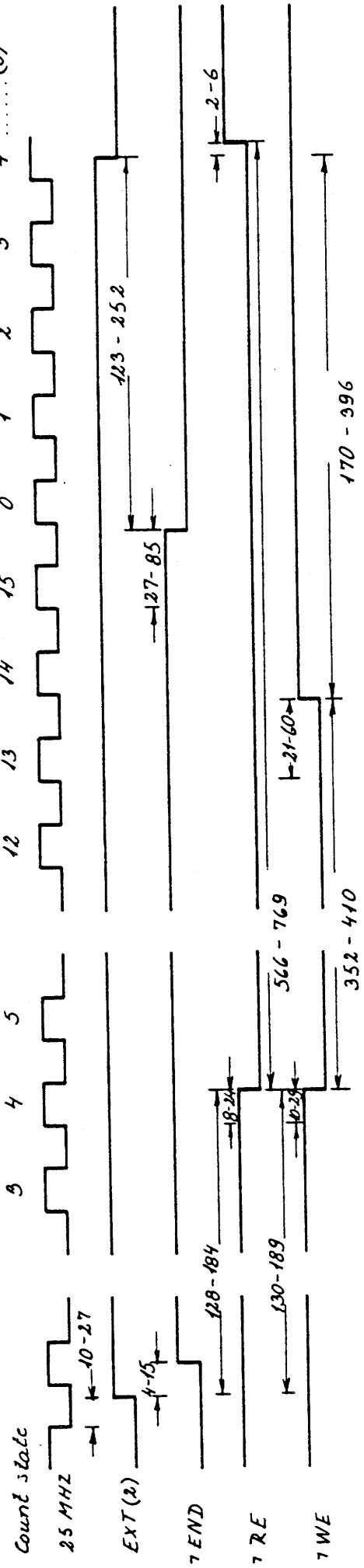
I/O TIMING FOR MPU



(All Times in nanoseconds)



Formatter Timing Logic
Timing Diagram

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5. Logic Diagram and Functional Description. 5.

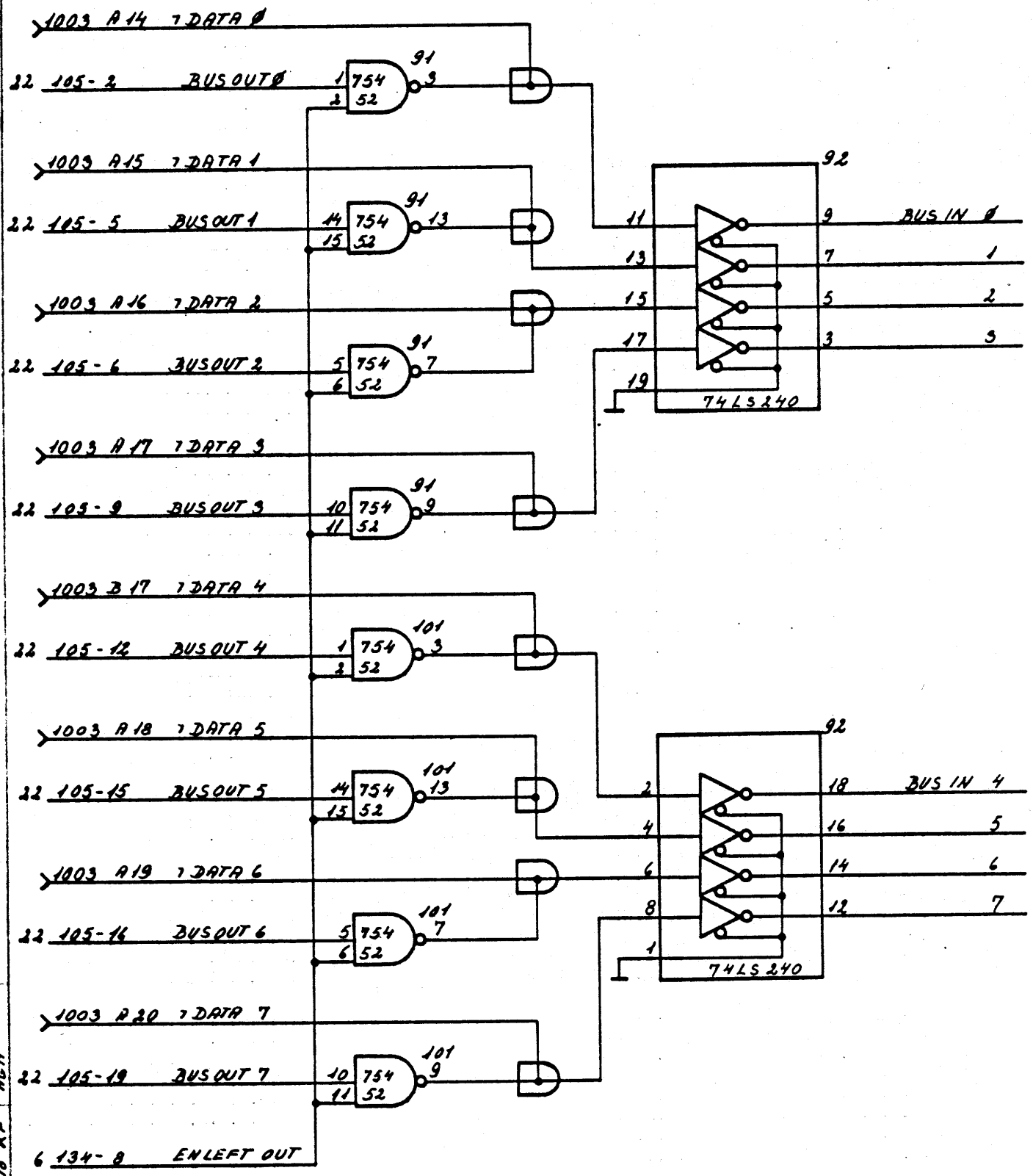
The following 30 pages contain logic diagrams for FDC 705. A functional description for every sheet of diagram is found on the corresponding left hand page.

The functional description consists of a schematic listing of all signals generated on the page. A short description and a listing of the diagrams to which the signal is transferred is given for each signal.

NOTE: All references between individual diagrams make use of diagram numbers (lower right corner) and not page numbers (upper right corner).

SIGNAL	DESTI-NATION	DESCRIPTION
-, DATA Ø-7	1003	I/O Databus
BUSIN Ø-7	9	Received I/O Databus

Unit		
FDC 705		FDC 1

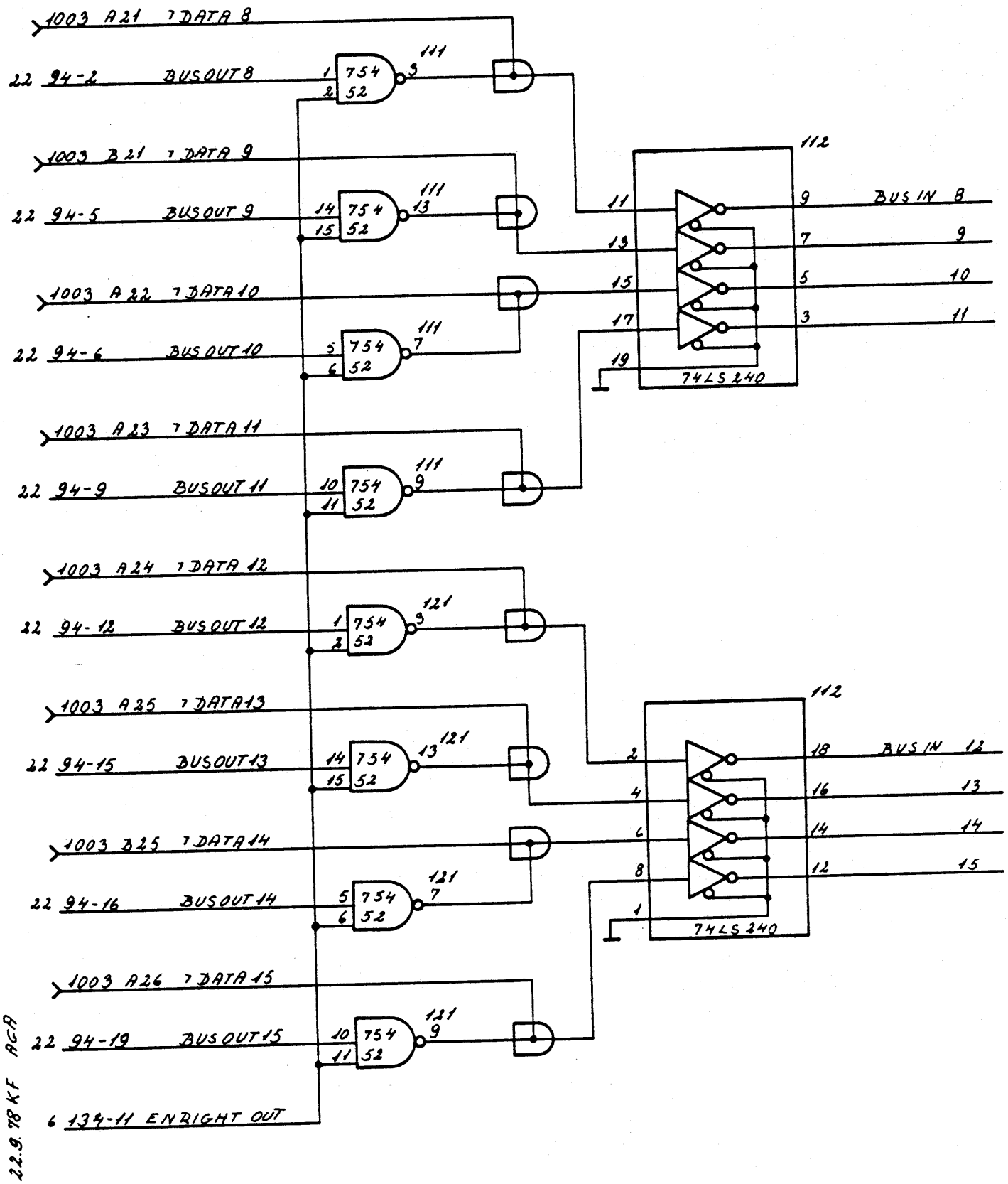


FDC 705 Data Bus Receivers and Drivers <0-7> FDC 1

R 12 523

SIGNAL	DESTI-NATION	DESCRIPTION
-, DATA 8-15	1003	I/O Data Bus
BUSIN 8-12	9	Received I/O Data Bus
BUSIN 13-15	7,9	

Unit FDC 705		FDC 2



FDC 705

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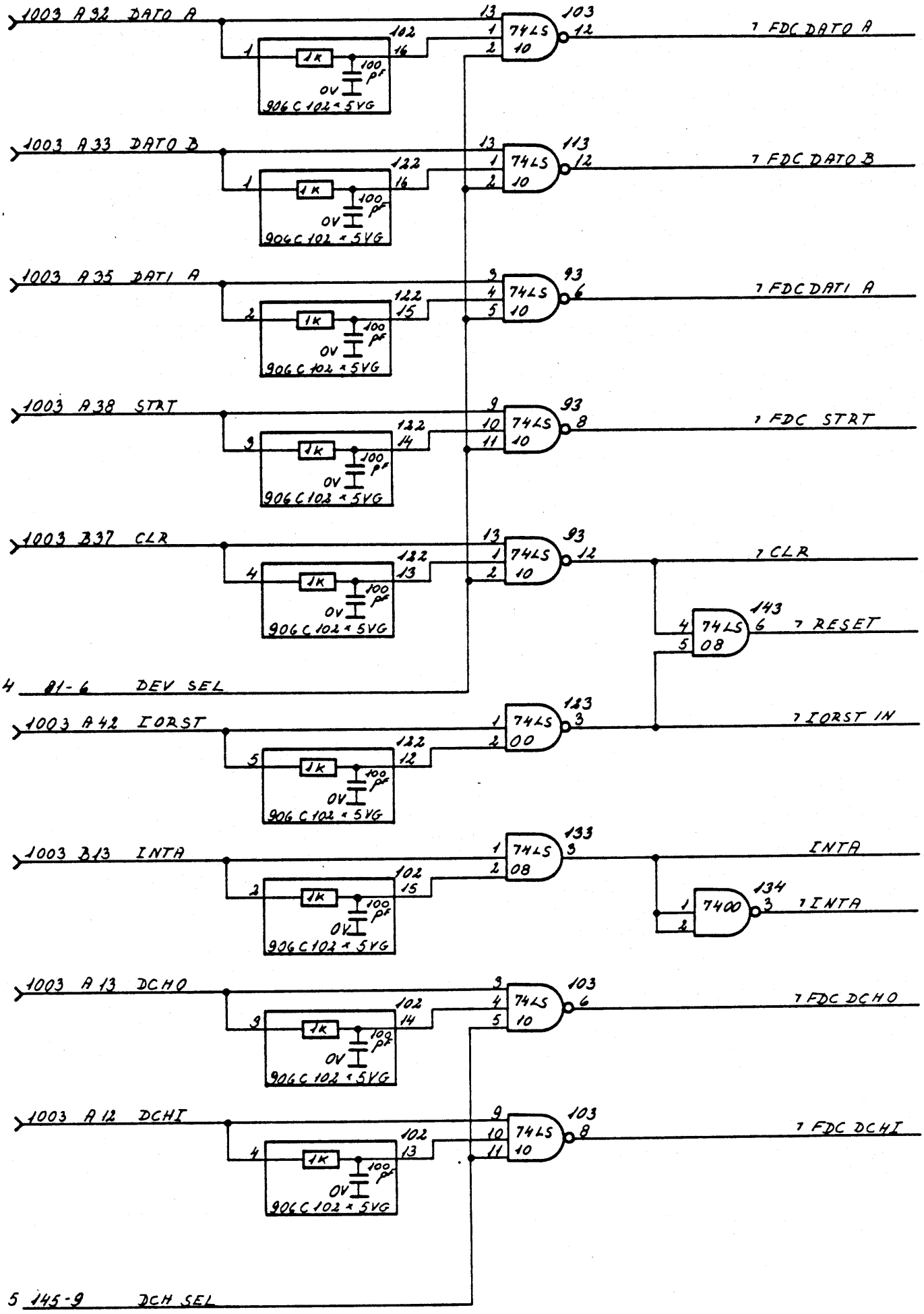
Data Bus Receivers and Drivers <8-15>

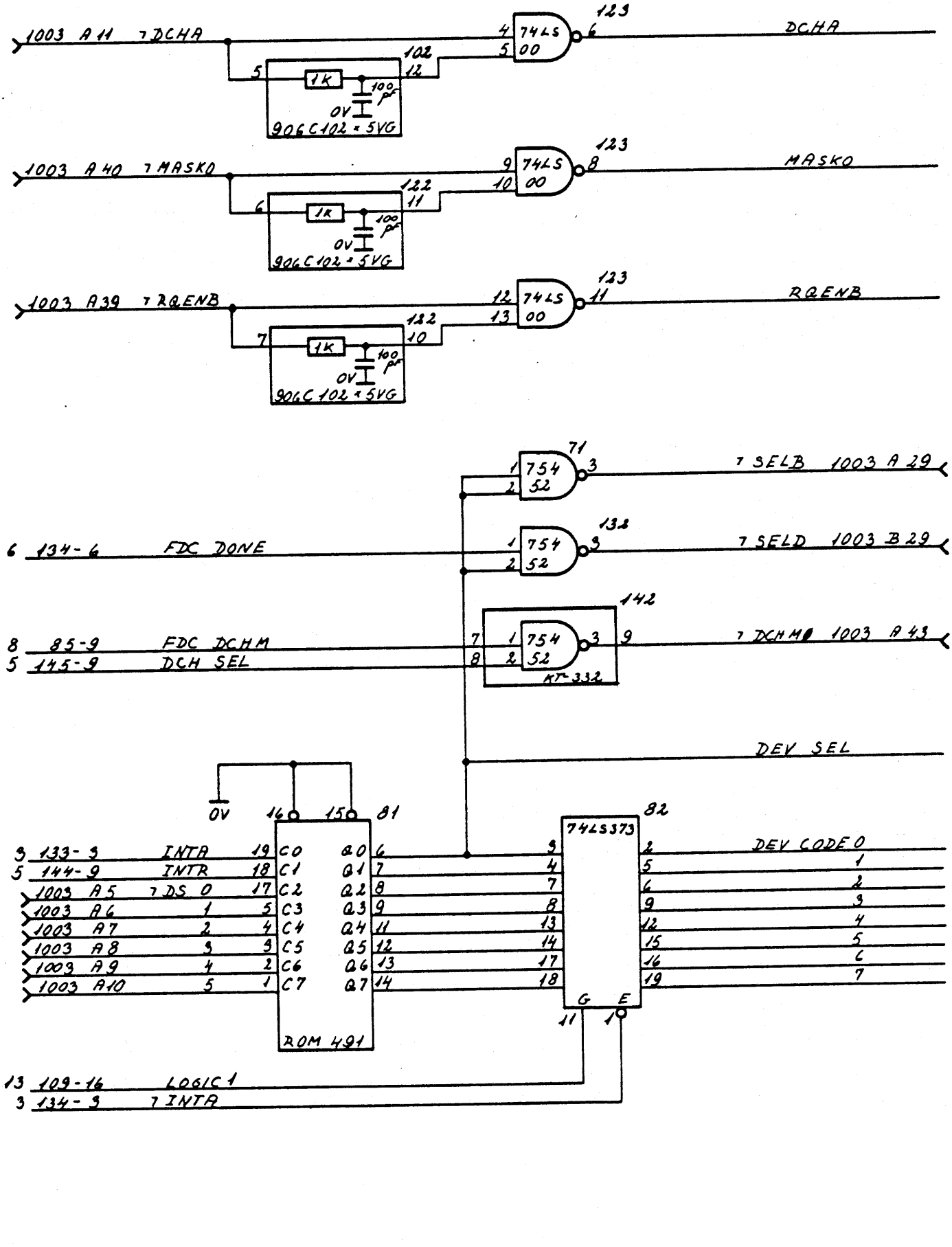
FDC 2

SIGNAL	DESTI-NATION	DESCRIPTION
-, FDC DATO A	7	Selected DATO A signal
-, FDC DATO B	7,9	- DATO B -
-, FDC DATI A	6	- DATIA -
-, FDC STRT	7	- STRT pulse
-, CLR		- CLR -
-, RESET	5	Clear the entire controller
-, IORST IN		Received I/O reset pulse
INTA	4,6	Received Interrupt Acknowledge Signal
-, INTA	4	-"-
-, FDC DCHO	6,9	Selected DCHO signal
-, FDC DCHI	6,10	- DCHI -


1003 A32 DATO A
1K
100 pf
0V
906C102-5VG
74LS 10
74LS 08
7400
7 FDC DATO A
1003 A33 DATO B
7 FDC DATO B
1003 A35 DATI A
7 FDC DATI A
1003 A38 STRT
7 FDC STRT
1003 B37 CLR
7 CLR
7 RESET
4 81-6 DEV SEL
1003 A42 IORST
7 IORST IN
1003 B13 INTA
INTA
7 INTA
1003 A13 DCHO
7 FDC DCHO
1003 A12 DCHI
7 FDC DCHI
5 145-9 DCH SEL

22.9.78 KF AGA

SIGNAL	DESTI-NATION	DESCRIPTION
DCHA	5,6	Received -, DCHA signal
MASKO	5	Received -, MASKO signal
RQENB	5	Received -, RQENB signal
-,SELB	1003	Select Busy
-,SELD	1003	Select Done
-,DCHMØ	1003	DCH Direction (1⇒Input,Ø⇒Output)
DEV SEL	3,4	FDC selected (DSØ-5 = Dev. code)
DEV CODE	22	INTA device code
-,DS Ø-5	1003	Device select address signals



FDC 705

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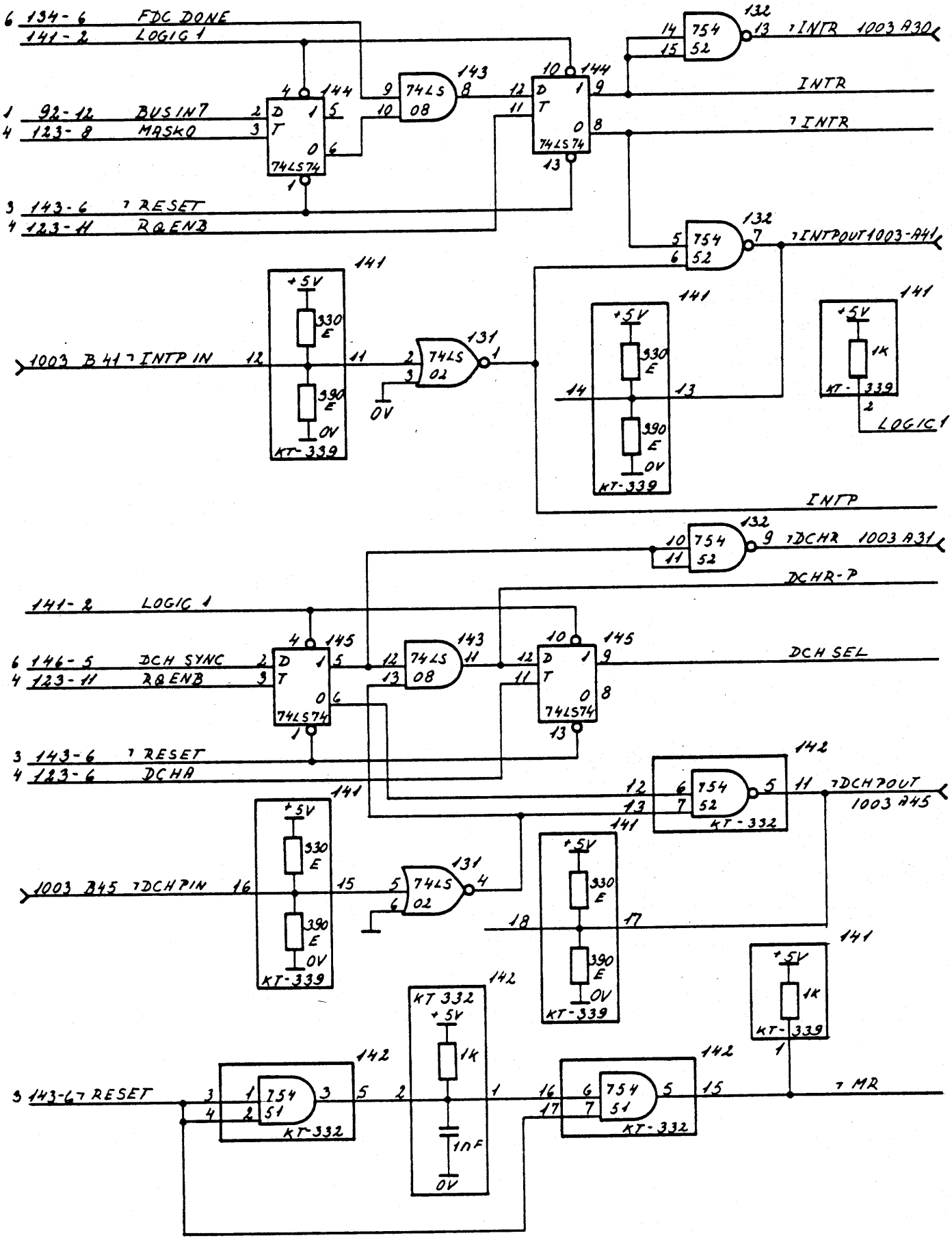
Control Signal Receivers
Device Select Logic

FDC 4

SIGNAL	DESTI-NATION	DESCRIPTION
-,INTR	1003	FDC Interrupt Request
INTR	4,6	-"-
-,INTP Out	1003	Interrupt Priority Out
-,INTP In	1003	-"- In
INTP	6	Received -,INTP In
-,DCHR	1003	Data Channel Request
DCHR-P	6	DCH request and priority
-,DCHPOUT	1003	DCH priority out
-,DCHPIN	1003	DCH priority in
-,MR	6,7,8,11 12,16,20 24, 28	Master Reset. Resets the entire controller



12.9.78 KF AG A

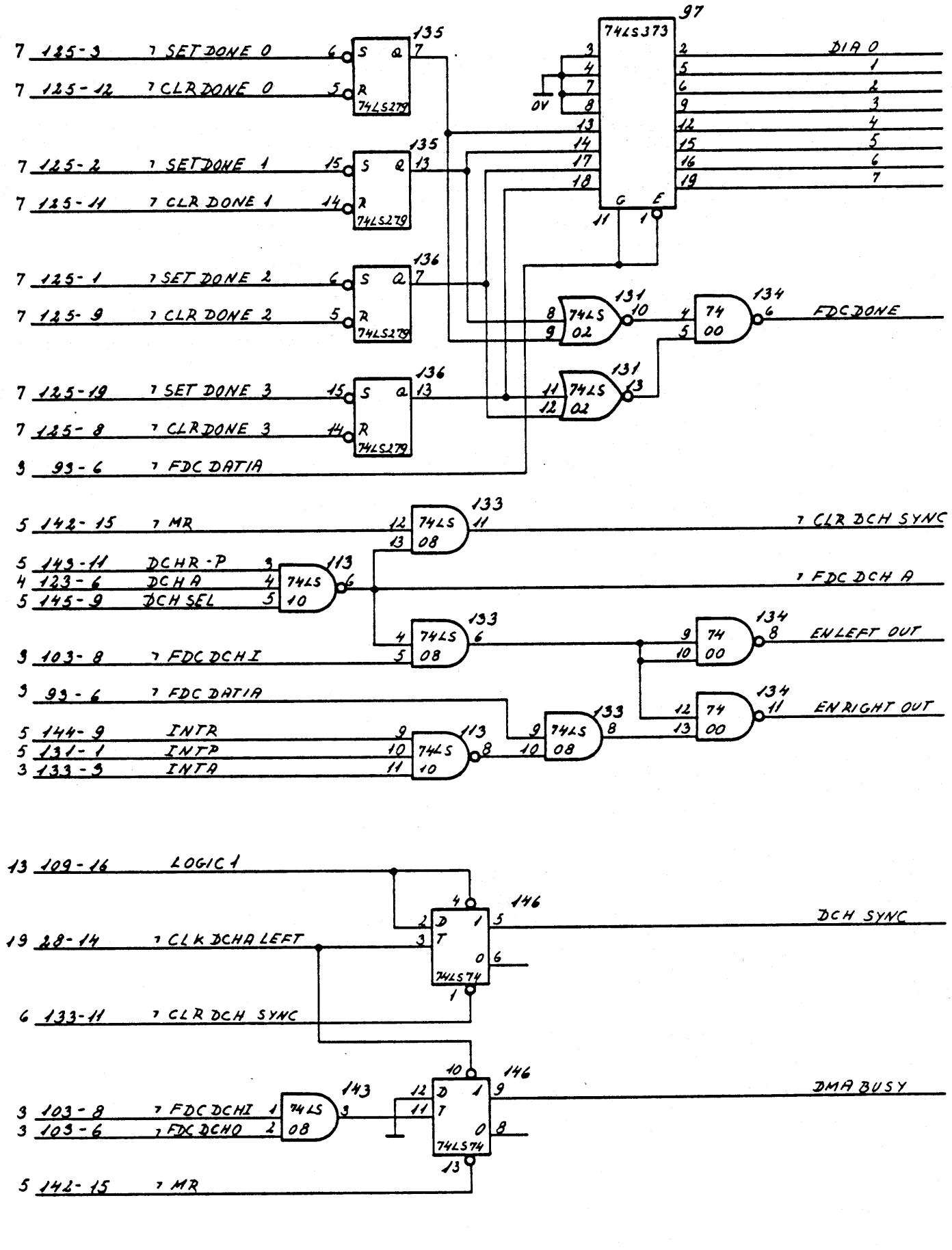
FDC 705

R 12 527

Interrupt and Data Channel Priority Logic

FDC 5

SIGNAL	DESTI-NATION	DESCRIPTION
DIAØ-7	22	Interrupt identification
FDC DONE	4	DONE flag
-,CLR DCH SYNC	6,7	Clear DCH SYNC and AUTOLOAD flip flop
-,FDC DCHA	6,7,10	Selected DCHA signal
EN LEFT OUT	1	Gate MSByte to I/O Databus
EN RIGHT OUT	2	Gate LSByte to I/O Databus
DCH SYNC	5	
DMA BUSY	30	Pending DMA cycle



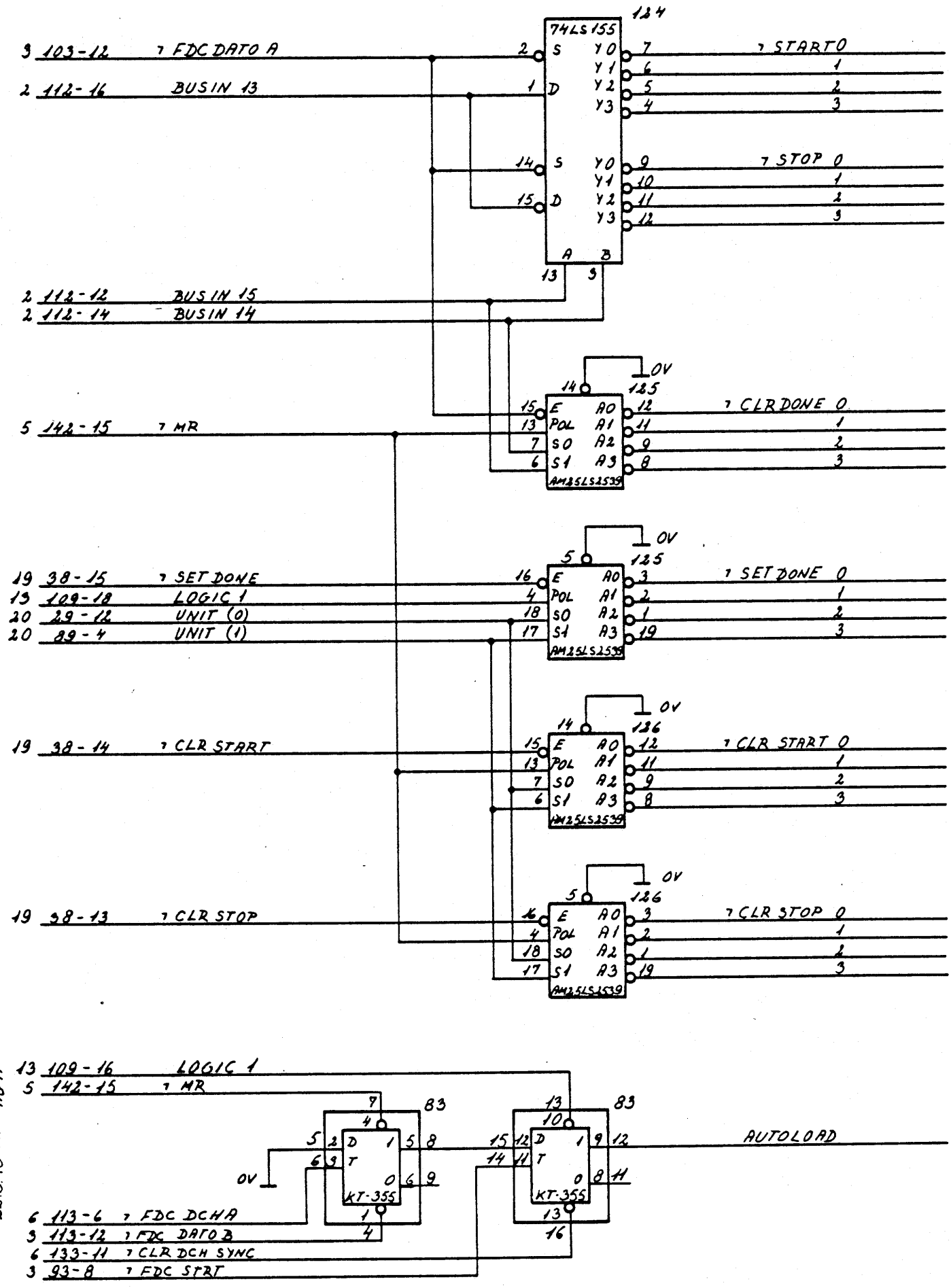
FDC 705

Done Flip Flops. Busout Enable Logic
DCH SYNC FLIP FLOP.

FDC 6

R 12528

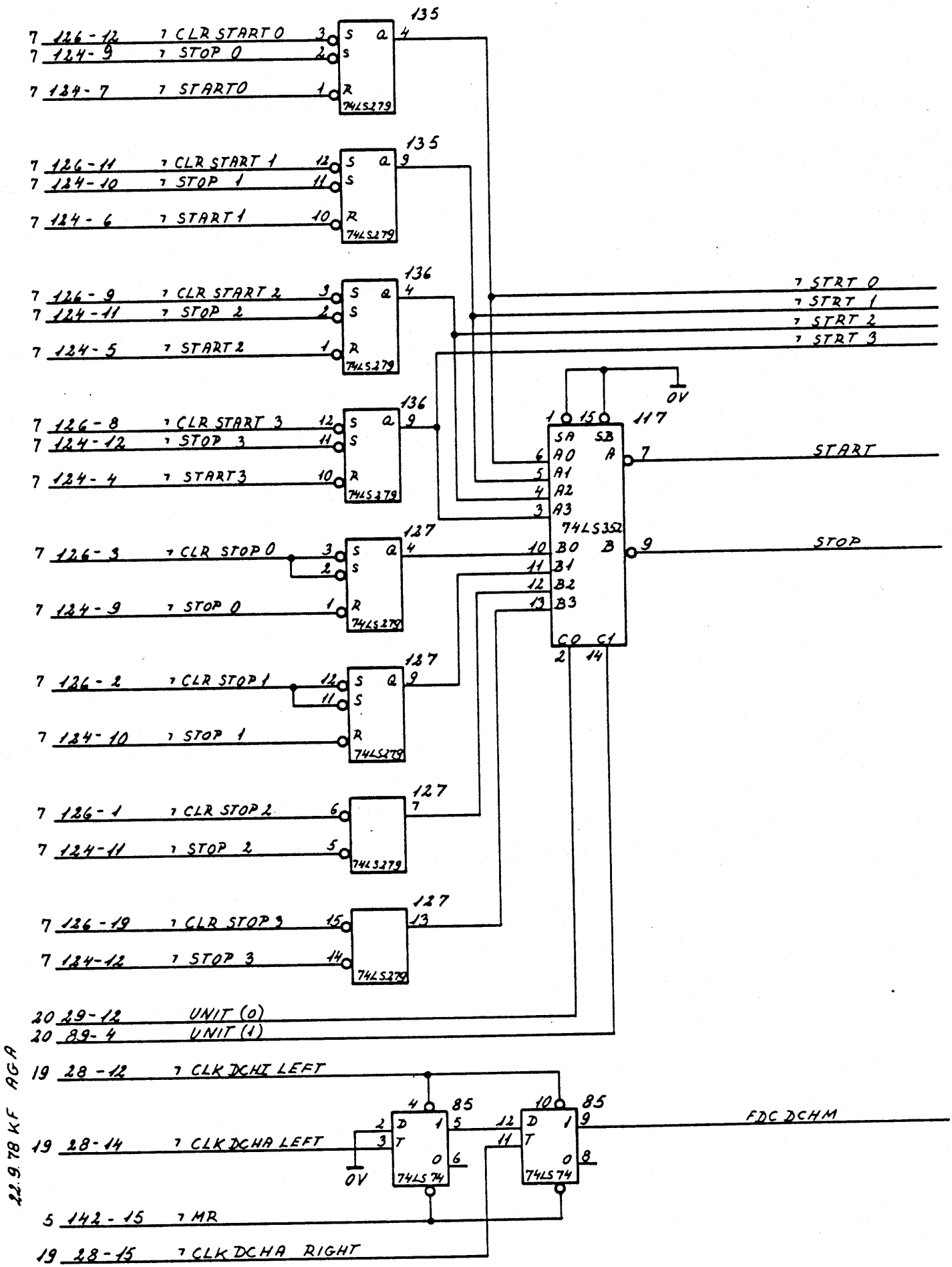
SIGNAL	DESTI-NATION	DESCRIPTION
-,START(Ø-3)	8	Set Start flag
-,STOP (Ø-3)	8	Set Stop flag and clear Start flag
-,CLR DONE (Ø-3)	6	Clear DONE flag (from CPU)
-,SET DONE (Ø-3)	6	Set DONE flag (from MPU)
-,CLR START (Ø-3)	8	Clear Start flag (from MPU)
-,CLR STOP (Ø-3)	8	Clear Stop flag (from MPU)
AUTOLOAD	30	Autoload signal to the MPU



FDC 705 SET/Clear Done, Start and Stop Logic FDC 7

R 12529

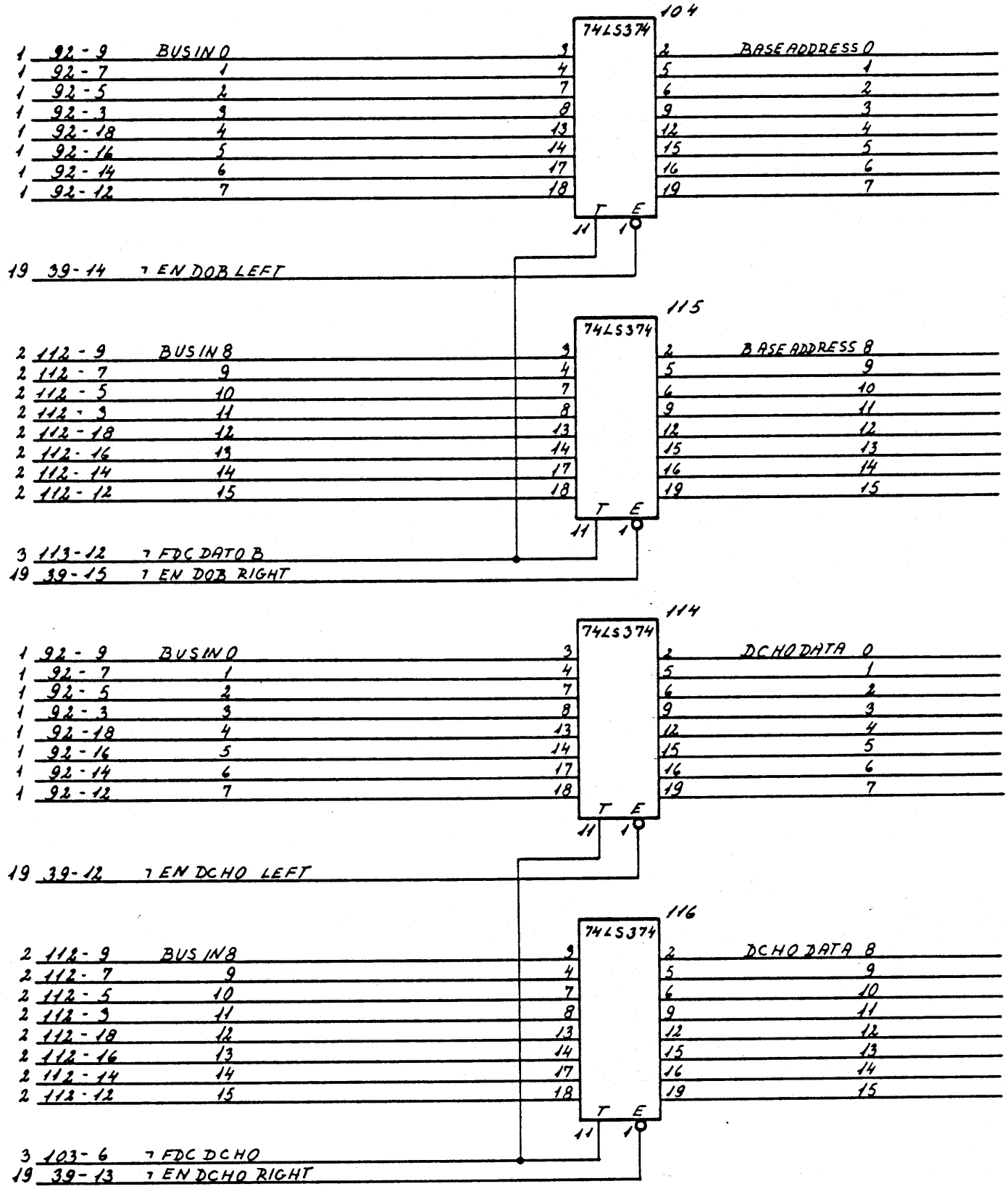
SIGNAL	DESTI-NATION	DESCRIPTION
-,STRT Ø	11	Start Flag unit Ø
-,STRT 1	12	-"- - 1
-,STRT 2	11	-"- - 2
-,STRT 3	12	-"- - 3
START	20	Start flag, current unit
STOP	30	Stop flag, current unit
FDC. DCHM	4	DCH direction



FDC 705 Start and stop Flags FDC 8

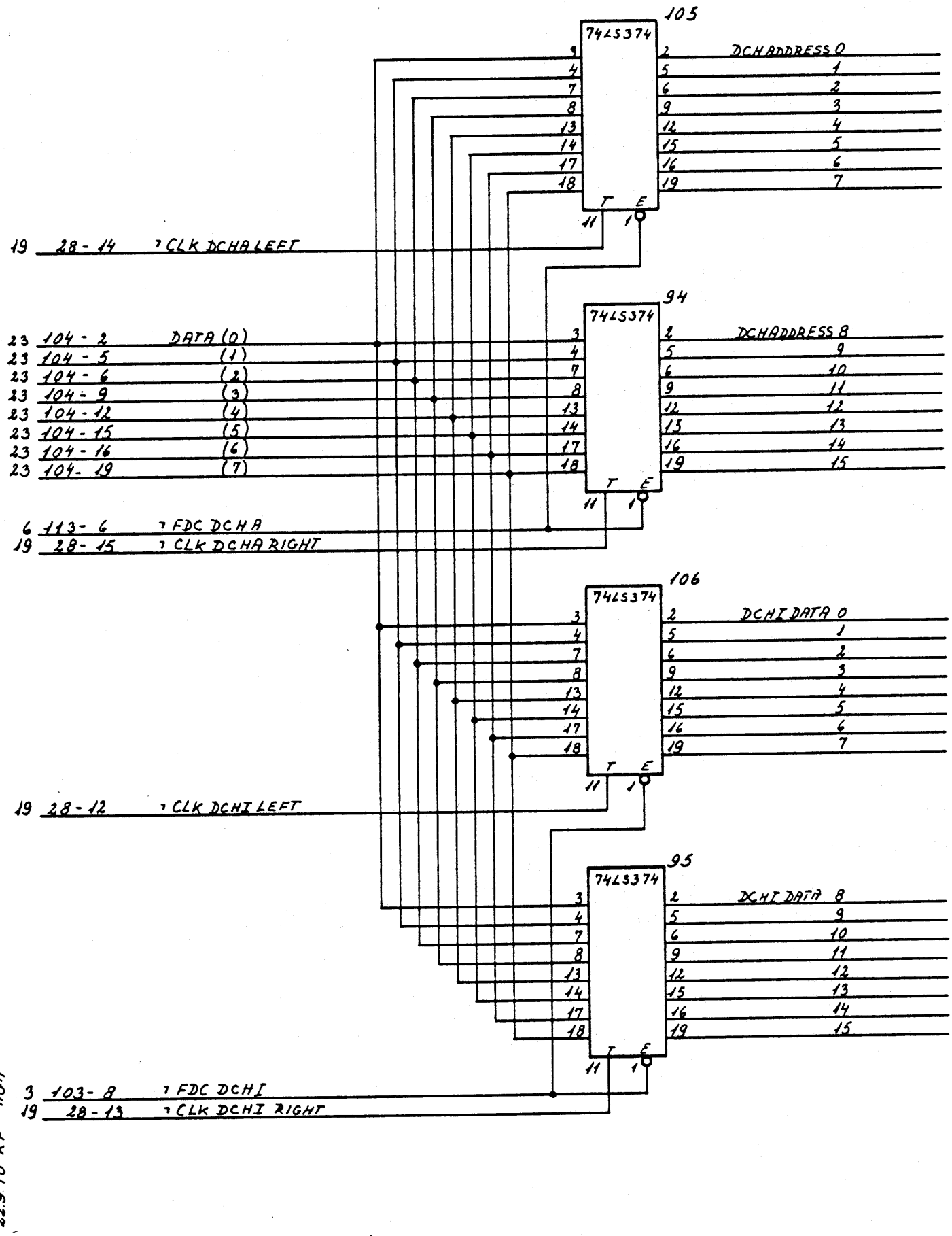
R 12530

SIGNAL	DESTI-NATION	DESCRIPTION
BASE ADDRESS (0-15)	23	MPU Data bus
DCHO DATA (0-15)	23	-"-

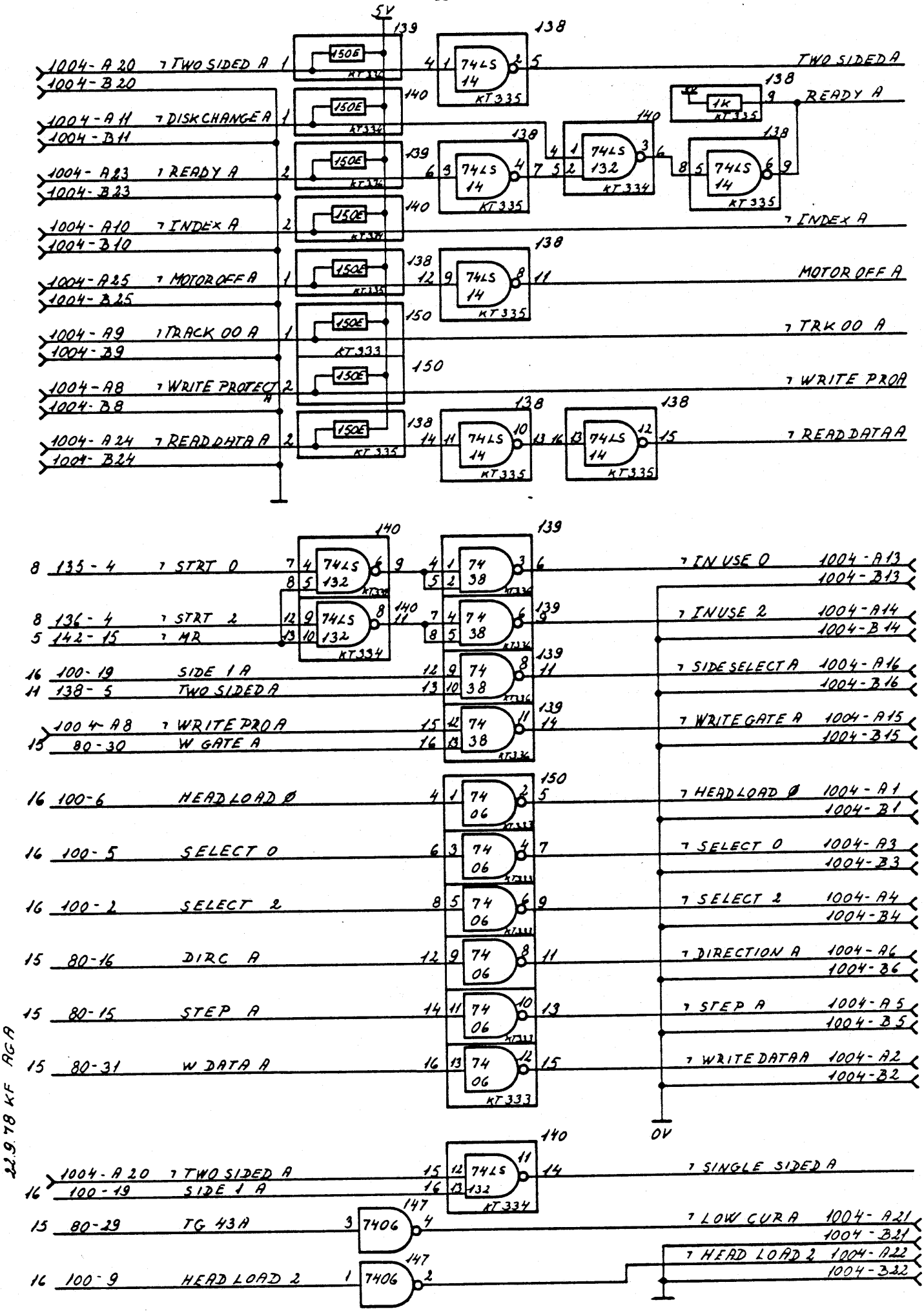

104
74LS374
1 92-9 BUS IN 0
1 92-7 1
1 92-5 2
1 92-3 3
1 92-18 4
1 92-16 5
1 92-14 6
1 92-12 7
BASE ADDRESS 0
19 39-14 ¬ EN DOB LEFT
115
74LS374
2 112-9 BUS IN 8
2 112-7 9
2 112-5 10
2 112-3 11
2 112-18 12
2 112-16 13
2 112-14 14
2 112-12 15
BASE ADDRESS 8
3 113-12 ¬ FDC DATO B
19 39-15 ¬ EN DOB RIGHT
114
74LS374
1 92-9 BUS IN 0
1 92-7 1
1 92-5 2
1 92-3 3
1 92-18 4
1 92-16 5
1 92-14 6
1 92-12 7
DCHO DATA 0
19 39-12 ¬ EN DCHO LEFT
116
74LS374
2 112-9 BUS IN 8
2 112-7 9
2 112-5 10
2 112-3 11
2 112-18 12
2 112-16 13
2 112-14 14
2 112-12 15
DCHO DATA 8
3 103-6 ¬ FDC DCHO
19 39-13 ¬ EN DCHO RIGHT

22.9.78 KF AG A

SIGNAL	DESTI-NATION	DESCRIPTION
DCH ADDRESS (0-15)	22	BUS OUT
DCHI DATA (0-15)	22	-"-


105
74LS374
DCH ADDRESS 0
DCH ADDRESS 1
DCH ADDRESS 2
DCH ADDRESS 3
DCH ADDRESS 4
DCH ADDRESS 5
DCH ADDRESS 6
DCH ADDRESS 7
19 28-14 CLK DCHA LEFT
94
74LS374
DCH ADDRESS 8
DCH ADDRESS 9
DCH ADDRESS 10
DCH ADDRESS 11
DCH ADDRESS 12
DCH ADDRESS 13
DCH ADDRESS 14
DCH ADDRESS 15
23 104-2 DATA (0)
23 104-5 (1)
23 104-6 (2)
23 104-9 (3)
23 104-12 (4)
23 104-15 (5)
23 104-16 (6)
23 104-19 (7)
6 113-6 FDC DCH A
19 28-15 CLK DCHA RIGHT
106
74LS374
DCHI DATA 0
DCHI DATA 1
DCHI DATA 2
DCHI DATA 3
DCHI DATA 4
DCHI DATA 5
DCHI DATA 6
DCHI DATA 7
19 28-12 CLK DCHI LEFT
95
74LS374
DCHI DATA 8
DCHI DATA 9
DCHI DATA 10
DCHI DATA 11
DCHI DATA 12
DCHI DATA 13
DCHI DATA 14
DCHI DATA 15
3 103-8 FDC DCHI
19 28-13 CLK DCHI RIGHT
22.978 KF AGA

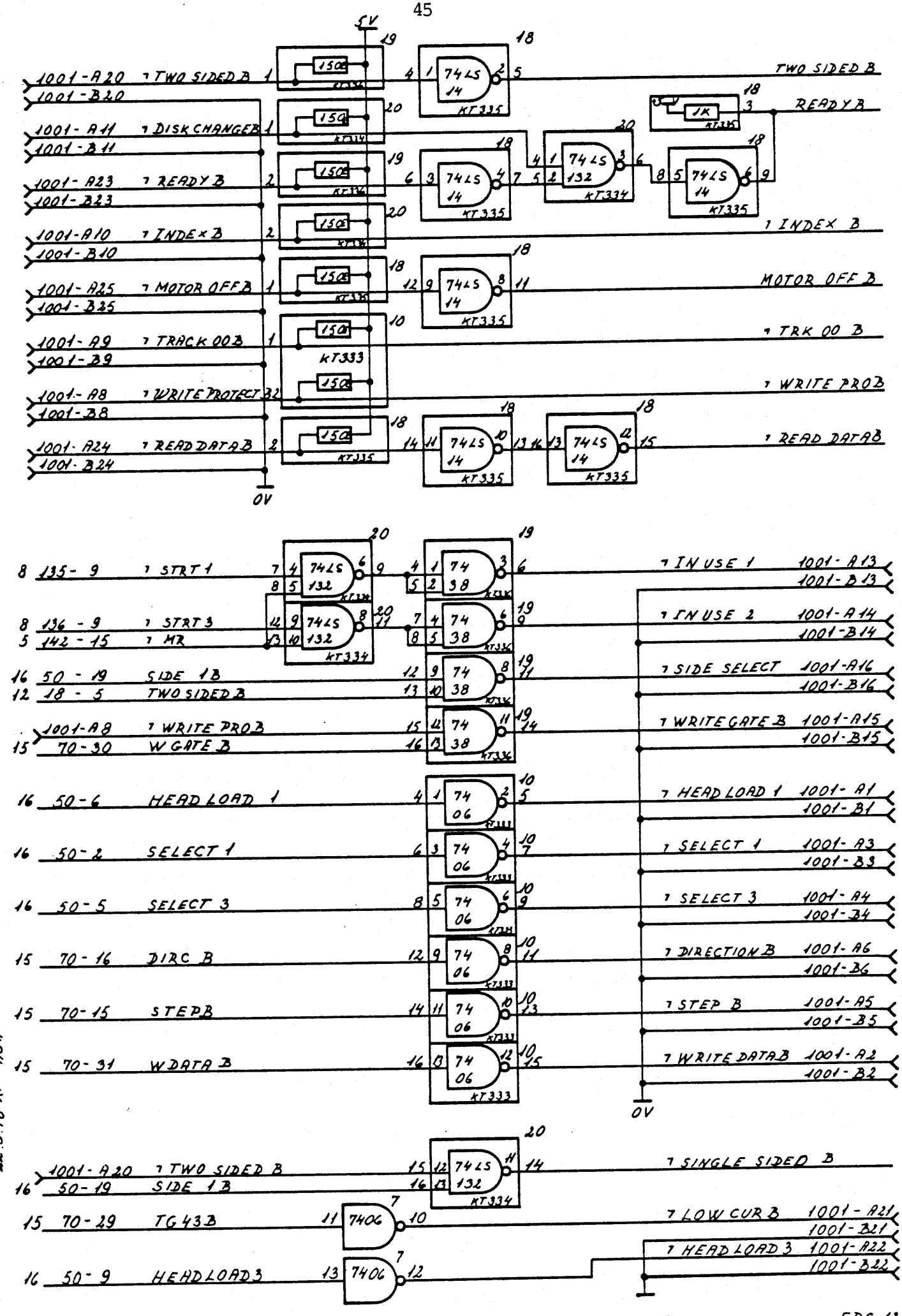
SIGNAL	DESTI-NATION	DESCRIPTION
TWO SIDED A	11	The selected drive contains a two sided diskette
-,DISK CHANGE A	1004	The selected drive has been not ready since last selected
-,READY A	1004	The selected drive is ready
READY	15,20	Online status
-,INDEX A	13,15	Index Pulse
MOTOR OFF A	20	Spindle motor not running
-,TRKOO A	15	Track Ø photosenser active
-,WRITE PRO A	11,15	The diskette is write protected
-,READ DATA A	13	Composite Read Data
-,IN USE Ø&2	1004	Run signal to the spindle motor
-,SIDE SELECT A	1004	Select side 2 of the diskette
-,WRITE GATE A	1004	Turn on write current
-,HEAD LOAD Ø	1004	Load head, unit 0
-,SELECT Ø	1004	Select unit 0
-,SELECT 2	1004	Select unit 2
-,DIRECTION A	1004	Active when stepping in
-,STEP A	1004	Step the motor
-,WRITE DATA A	1004	Composite write data
-,SINGLE SIDED A	20	Side two of a single sided diskette is selected!
-,LOW CUR A	1004	The head is positioned on a track larger than 43. Switch to low write current.
-,Head load 2	1004	load head, unit 2



FDC 705 Drive Control Signal Receivers & Driver A FDC 11

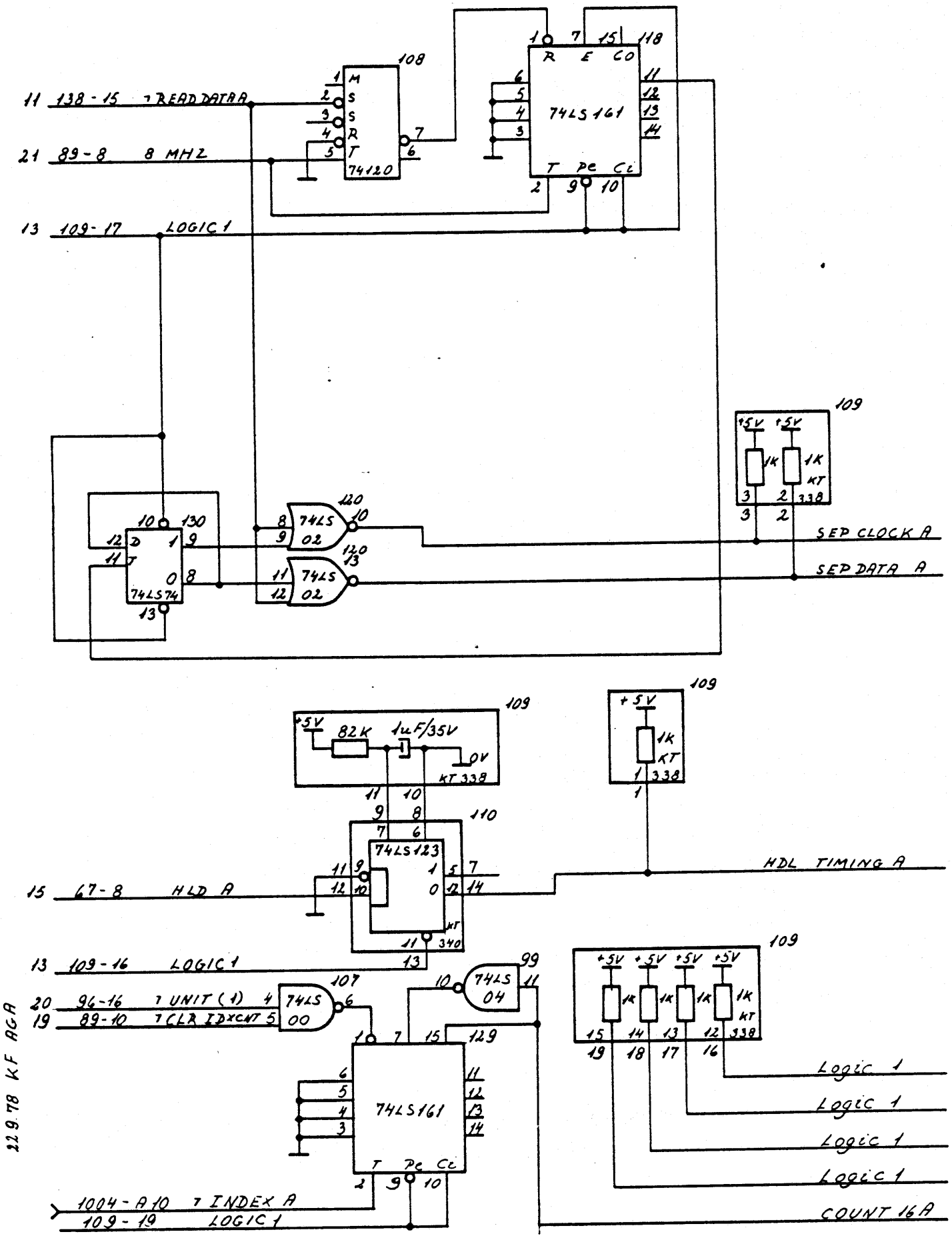
R 12533

SIGNAL	DESTI-NATION	DESCRIPTION
TWO SIDED B	12	The selected drive contains a two sided diskette
-,DISK CHANGE B	1001	The selected drive has been not ready since last selected
-,READY B	1001	The selected drive is ready
READY	15,20	Online status
-,INDEX B	14,15	Index Pulse
MOTOR OFF B	20	Spindle motor not running
-,TRKOO B	15	Track Ø photosenser active
-,WRITE PRO B	12,15	The diskette is write protected
-,READ DATA B	14	Composite Read Data
-,IN USE 1&3	1001	Run signal to the spindle motor
-,SIDE SELECT B	1002	Select side 2 of the diskette
-,WRITE GATE B	1002	Turn on write current
-,HEAD LOAD 1	1002	load head, unit 1
-,SELECT 1	1002	Select unit 1
-,SELECT 3	1002	Select unit 3
-,DIRECTION B	1002	Active when stepping in
-,STIP B	1002	Step the motor
-,WRITE DATA B	1002	Composite write data
-,SINGLE SIDED B	20	Side two of a single sided diskette is selected!
-,LOW CUR B	1002	The head is positioned on a track larger than 43. Switch to low write current
-,Head load 3	1002	load head, unit 3



FDC 705 Drive Control Signal Receivers & Drivers B FDC 12

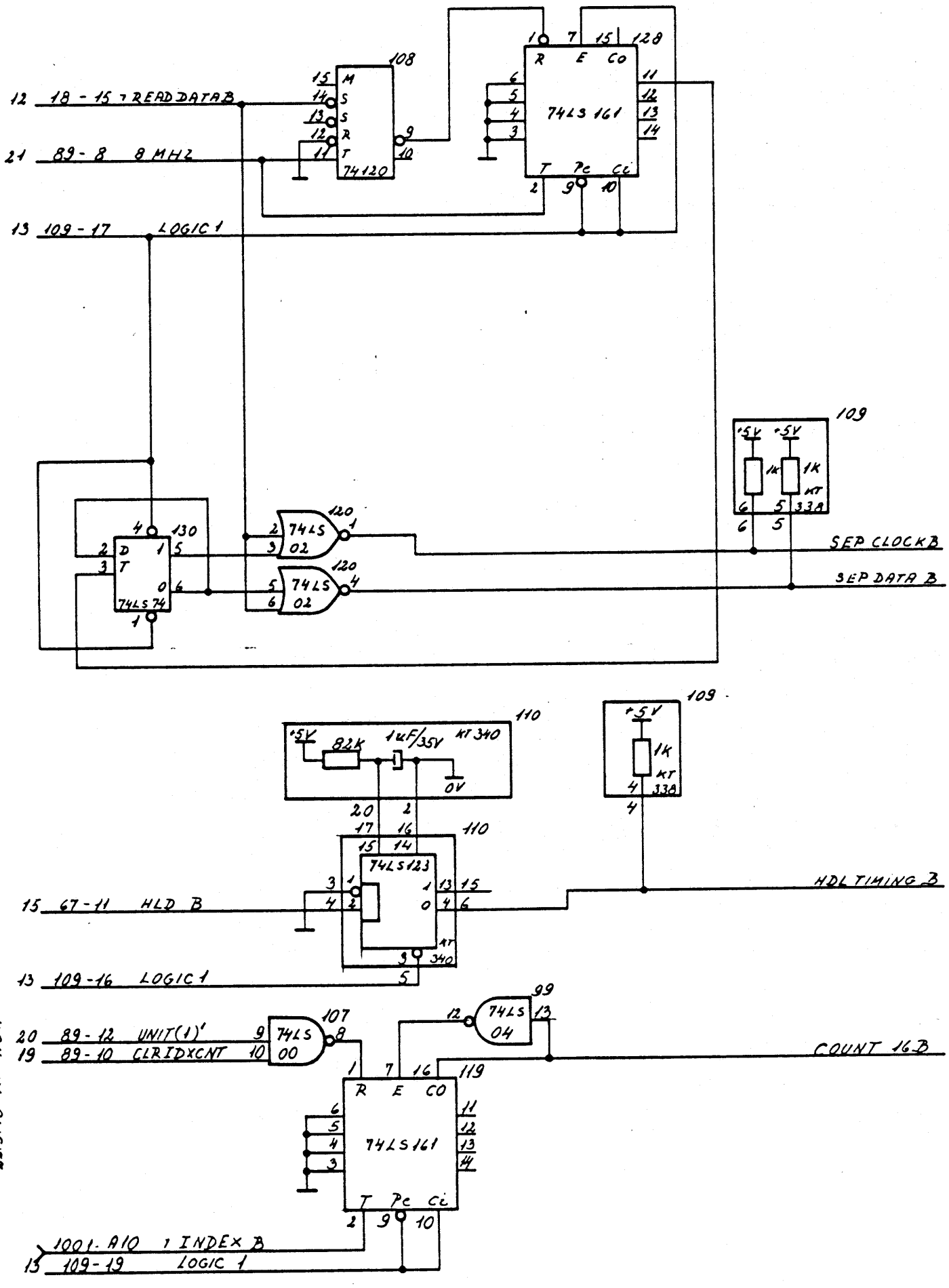
SIGNAL	DESTI-NATION	DESCRIPTION
-,SEP CLOCK A	15	The separate clock and data
-,SEP DATA A	15	The two signals may be reversed!
HDL TIMING A	15	This signal reflects the head load time (35 m sec)
LOGIC 1 (109-16)	4,6,7,13, 14	
LOGIC 1 (109-17)	13,14	
-"- (109-18)	7,20	
-"- (109-19)	13,14	
COUNT 16A		Sixteen index pulses counted. Indicates head should be unloaded for drive not selected.



FDC 705 Data/Clock separator A FDC 13

R12535

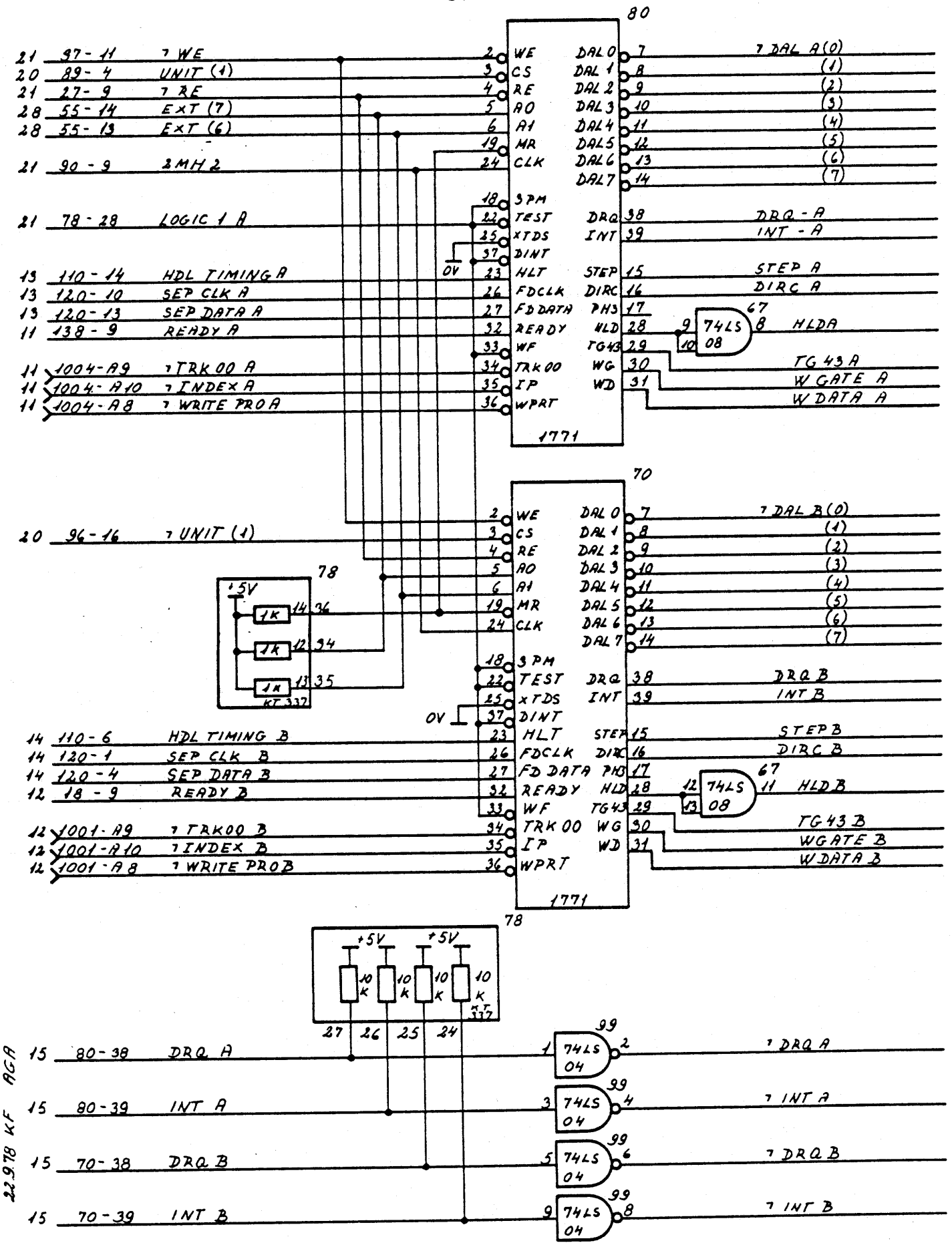
SIGNAL	DESTI-NATION	DESCRIPTION
-,SEP CLOCK B	15	The separate clock and data
-,SEP DATA B	15	The two signals may be reversed!
HDL TIMING B	15	This signal reflects the head load time (35 m sec)
COUNT 16B		Sixteen index pulses counted. Indicates head should be unloaded for drive not selected.



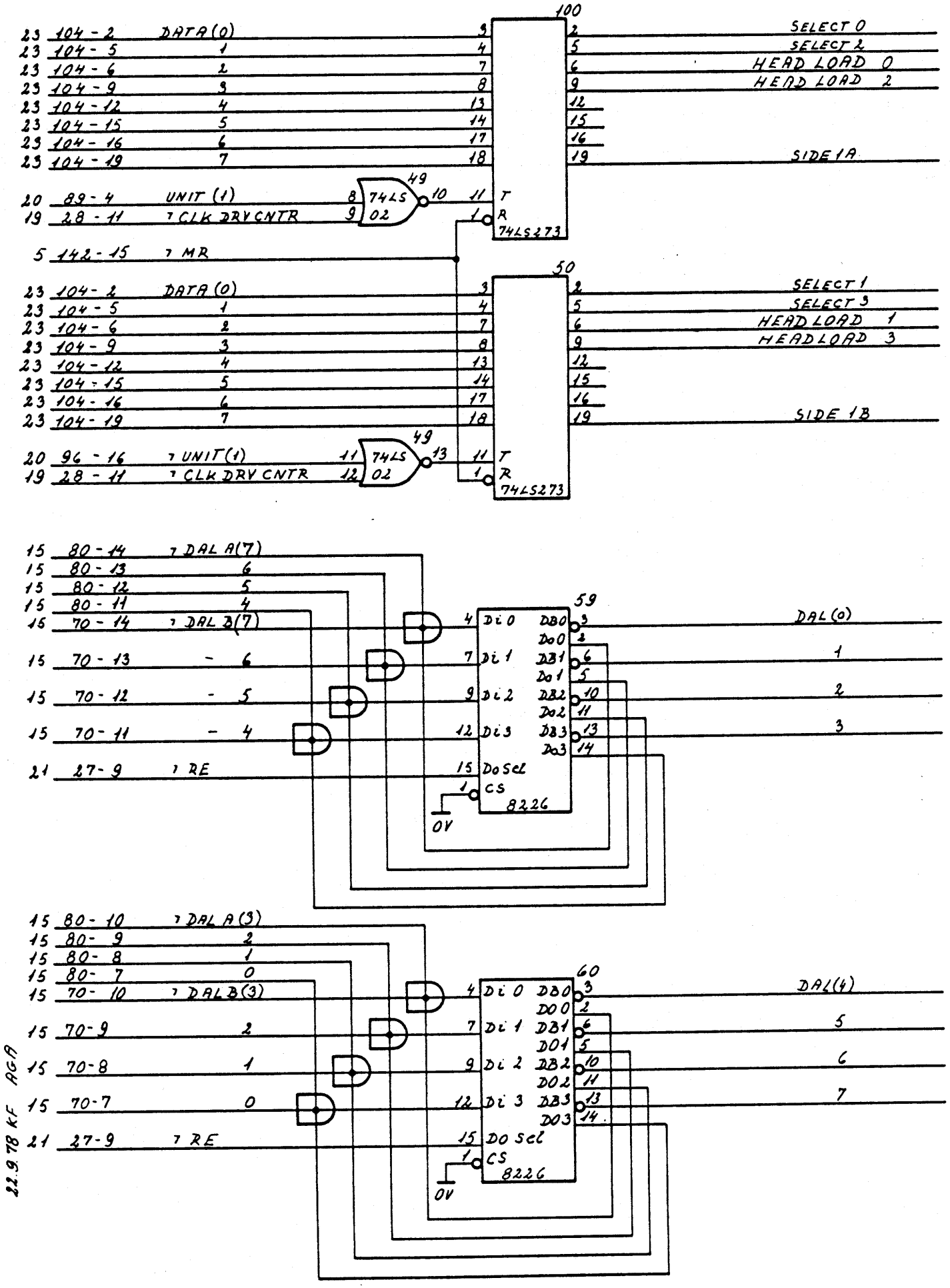
FDC 705 Data/Clock Separator B FDC 14

R 12 536

SIGNAL	DESTI-NATION	DESCRIPTION
-,DAL A(0-7)	16	Bidirectional data bus
DRQ-A	15	Formatter Data request
INT-A	15	-"- interrupt request
HLDA	13,20	Head load
TG 43 A	11	Track greater than 43
WGATE A	11	Write Gate
WDATA A	11	Write Data
-,DAL B(0-7)	16	
DRQ-B	15	
INT-B	15	
HLD B	14,20	Channel B signals
TG43B	12	
WGATE B	12	
WDATA B	12	
-,DRQA	20	
-,INTA	20	
-,DRQB	20	
-,INTB	20	


80
21 97-11 ↑WE
20 89-4 UNIT (1)
21 27-9 ↑RE
28 55-14 EXT (7)
28 55-13 EXT (6)
21 90-9 2MH2
21 78-28 LOGIC 1 A
13 110-14 HDL TIMING A
13 120-10 SEP CLK A
13 120-13 SEP DATA A
11 138-9 READY A
11 1004-A9 ↑TRK 00 A
11 1004-A10 ↑INDEX A
11 1004-A8 ↑WRITE PRO A
WE
CS
RE
A0
A1
MR
CLK
3PM
TEST
XTDS
DINT
HLT
FDCLK
FD DATA
READY
WF
TRK 00
IP
WPRT
1771
DAL 0
DAL 1
DAL 2
DAL 3
DAL 4
DAL 5
DAL 6
DAL 7
DRQ
INT
STEP
DIRC
PH3
HLD
TG43
WG
WD
↑DAL A(0)
(1)
(2)
(3)
(4)
(5)
(6)
(7)
DRQ-A
INT-A
STEP A
DIRC A
74LS 08
HLDA
TG43 A
W GATE A
W DATA A
70
20 96-16 ↑UNIT (1)
78
+5V
1K
KT 337
14 110-6 HDL TIMING B
14 120-1 SEP CLK B
14 120-4 SEP DATA B
12 18-9 READY B
12 1001-A9 ↑TRK00 B
12 1001-A10 ↑INDEX B
12 1001-A8 ↑WRITE PROB
↑DAL B(0)
DRQ B
INT B
STEP B
DIRC B
HLD B
TG43 B
WGATE B
W DATA B
78
+5V
10 K
KT 337
27 26 25 24
99
74LS 04
15 80-38 DRQ A
15 80-39 INT A
15 70-38 DRQ B
15 70-39 INT B
↑DRQ A
↑INT A
↑DRQ B
↑INT B
22978 KF AGA

SIGNAL	DESTI-NATION	DESCRIPTION
Select 0	11	Select unit 0
Select 2	11	Select unit 2
Head load 0	11	load head unit 0
Head load 2	11	load head unit 2
Side 1 A	11	Side select channel A
Select 1	12	Select unit 1
Select 3	12	Select unit 3
Head load 1	12	load head unit 1
Head load 3	12	load head unit 3
Side 1 B	12	Side select channel B
DAL (0-7)	23	MPU data bus



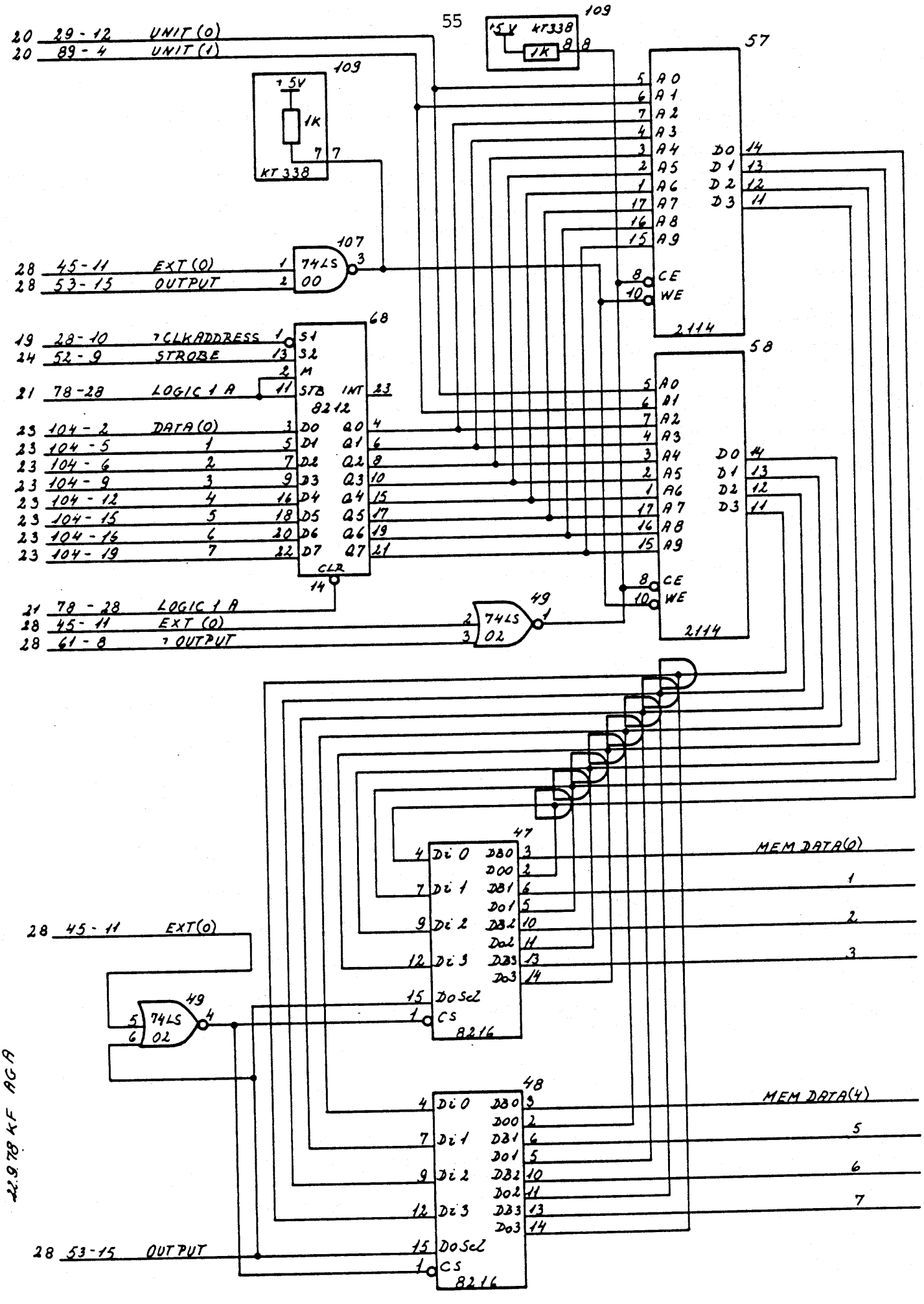
FDC 705

R 12538

Drive Control Registers & Formatter Bus Connection

FDC 16

SIGNAL	DESTI-NATION	DESCRIPTION
MEM DATA (0-7)	23	MPU data bus



22.9.78 KF AGA

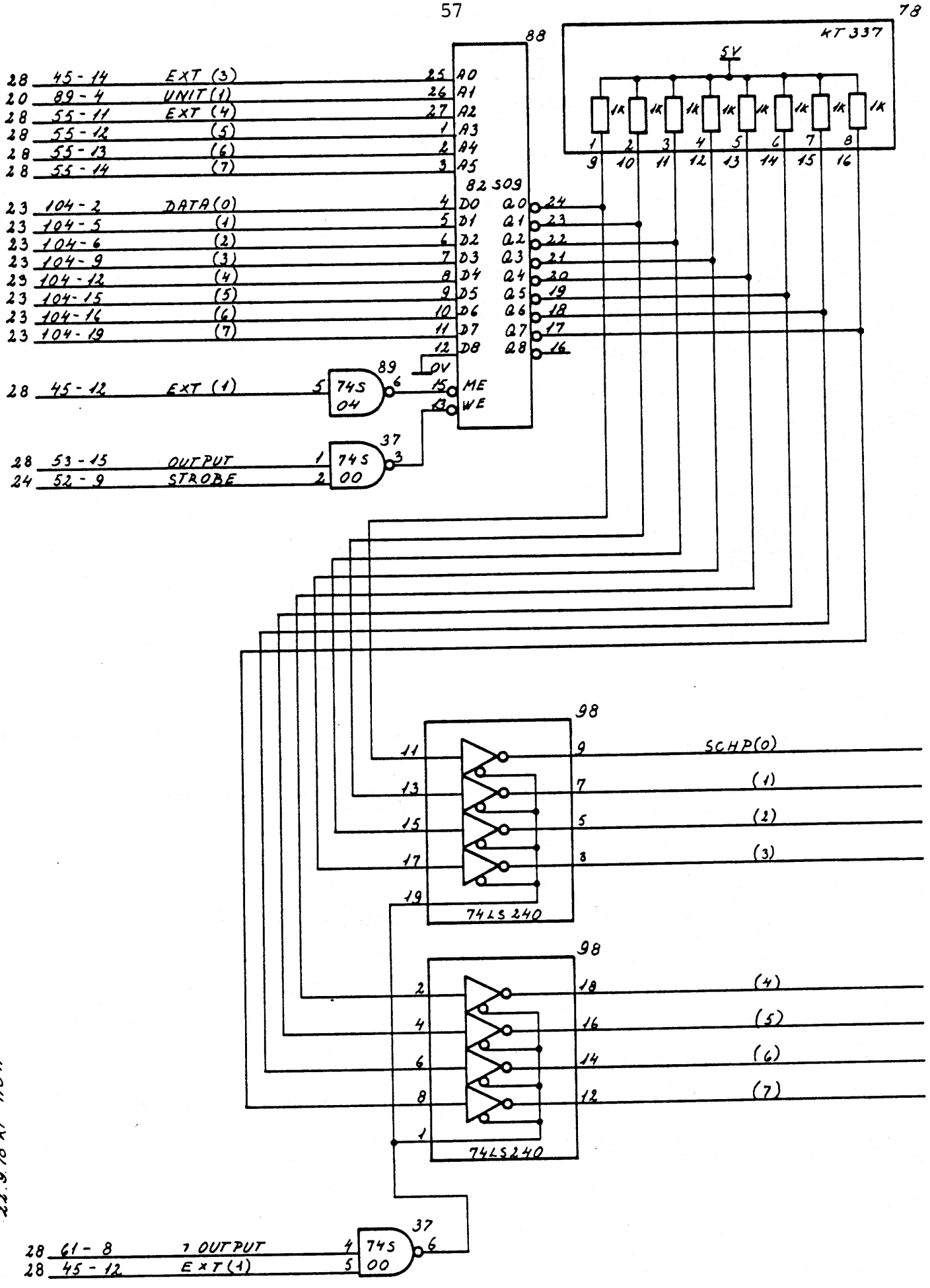
FDC 705

R 12539

Code Converter Ram's

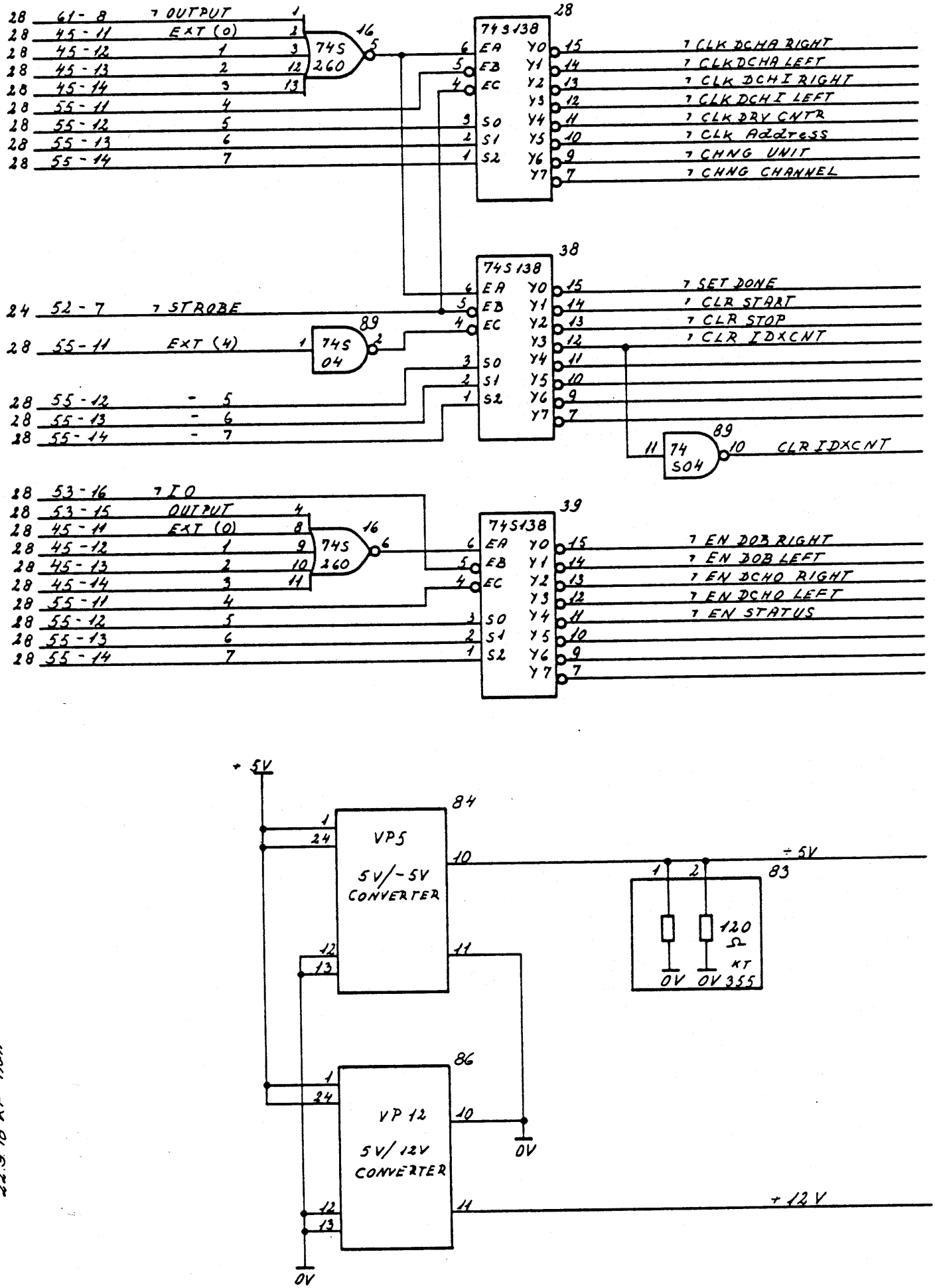
FDC 17

SIGNAL	DESTI-NATION	DESCRIPTION
SCHP (0-7)	23	MPU data bus


88
82 S09
KT 337
5V
1K
28 45 - 14 EXT (3)
20 89 - 4 UNIT (1)
28 55 - 11 EXT (4)
28 55 - 12 (5)
28 55 - 13 (6)
28 55 - 14 (7)
23 104 - 2 DATA (0)
23 104 - 5 (1)
23 104 - 6 (2)
23 104 - 9 (3)
23 104 - 12 (4)
23 104 - 15 (5)
23 104 - 16 (6)
23 104 - 19 (7)
A0 A1 A2 A3 A4 A5
D0 D1 D2 D3 D4 D5 D6 D7 D8
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
OV
ME
WE
89
74S 04
28 45 - 12 EXT (1)
37
74S 00
28 53 - 15 OUTPUT
24 52 - 9 STROBE
98
74LS 240
SCHP(0)
(1)
(2)
(3)
(4)
(5)
(6)
(7)
28 61 - 8 ↑ OUTPUT
28 45 - 12 EXT (1)

22.9 78 KF AGA

SIGNAL	DESTI-NATION	DESCRIPTION
-,CLK DCHA RIGHT	8,10	Load DCH address register LSB
-,CLK DCHA LEFT	6,8,10	-"- MSB
-,DCMI RIGHT	10	Load DCH input data register LSB
-,CLK DCHI LEFT	8,10	-"- MSB
-,CLK DRV CNTR	16	Load current channels Drive Control register
-,CLK ADDRESS	17	Load Code Converter address register
-,CHNG UNIT	20	Toggle current channels unit select FF
-,CHNG CHANNEL	20	Toggle channel select FF
-,SET DONE	7	Set current units Done Flag
-,CLR START	7	Clear current units Start Flag
-,CLR STOP	7	Clear current units Stop Flag
-,CLR IDXCNT		Reset the four bit index pulse counter for current channel
CLR IDXCNT	13,14	
-,EN DOB RIGHT	9	Base address LSB to MPU data bus
-,EN DOB LEFT	9	-"- MSB -"-
-,EN DCHO RIGHT	9	DCH output data LSB to MPU data bus
-,EN DCHO LEFT	9	-"- MSB -"-
-,EN STATUS	20	Status register to MPU data bus
- 5V	15	Formatter chip supply voltage
+ 12V	15	-"-



22.9.78 KF ACA

FDC 705

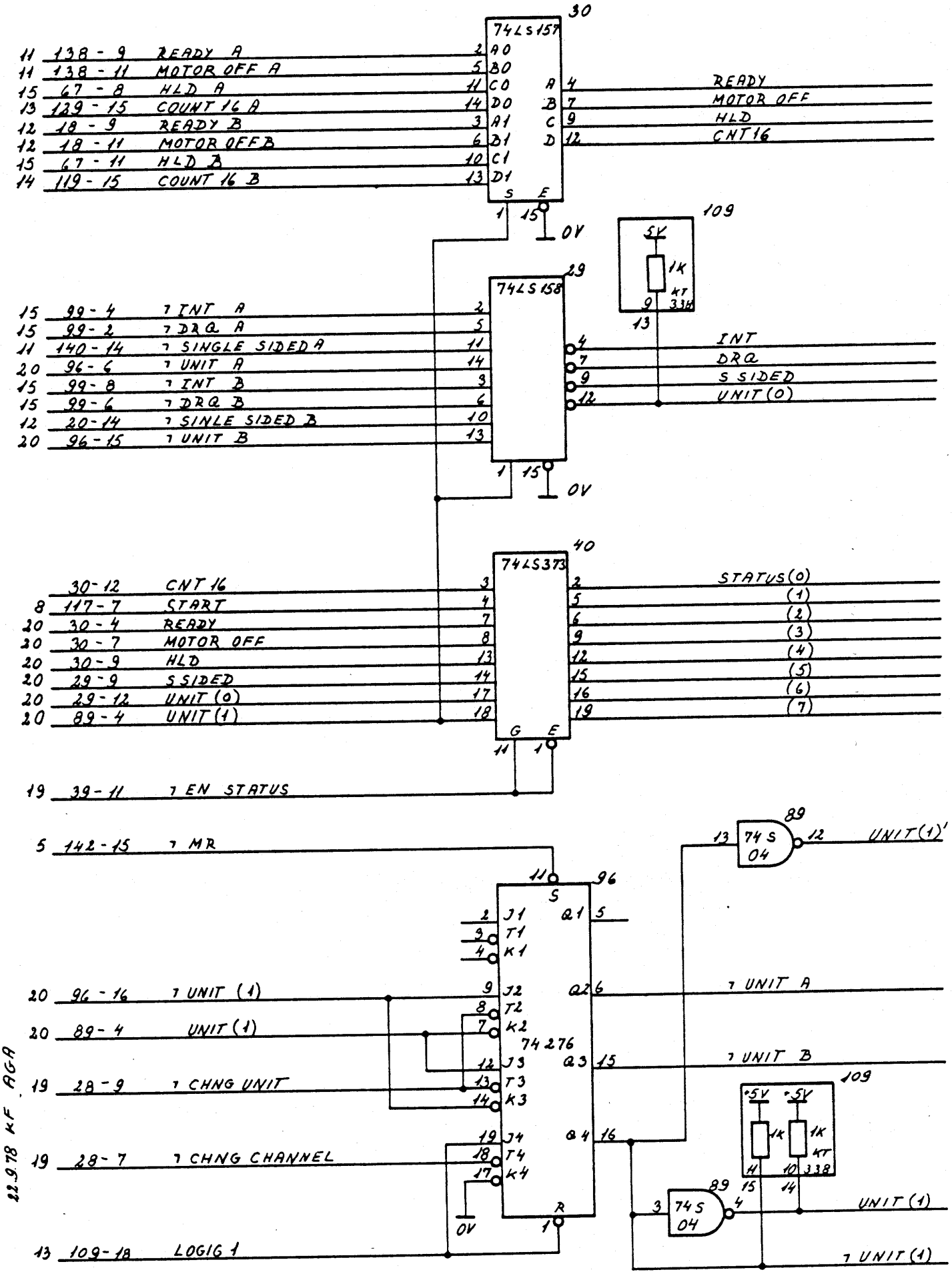
R 12 541

MPU I/O Select Logic

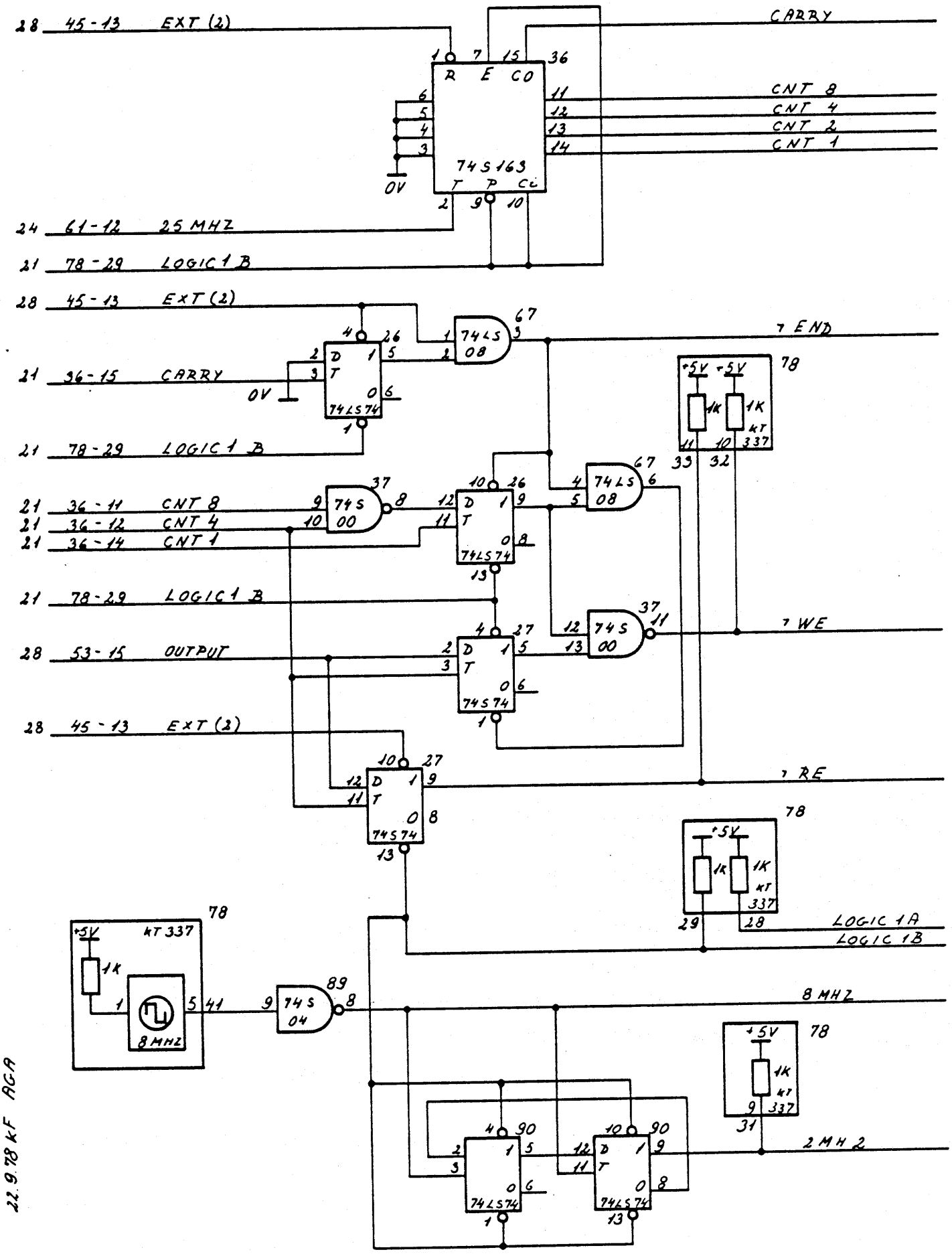
FDC 19

SIGNAL	DESTI-NATION	DESCRIPTION
READY	20	Current Unit ready
MOTOR OFF	20	Current Units AC motor stopped
HLD	20	Current channel head load
CNT16	20	Current channel index counter overflow
INT	30	Current formatter interrupt request
DRQ	30	-"- data request
S SIDED	20	Current channel side two violation
UNIT (0)	7,8,17,20	Unit select current channel
STATUS (0-7)	23	MPU data bus
UNIT (1)'	14	Channel Select Signal
UNIT (1)	7,8,15,16 17,18,20, 29	
-,UNIT (1)	13,15,16, 20	
-,UNIT A	20	Unit select, channel A
-,UNIT B	20	-"- , -"-

Unit		
FDC 705		FDC 20

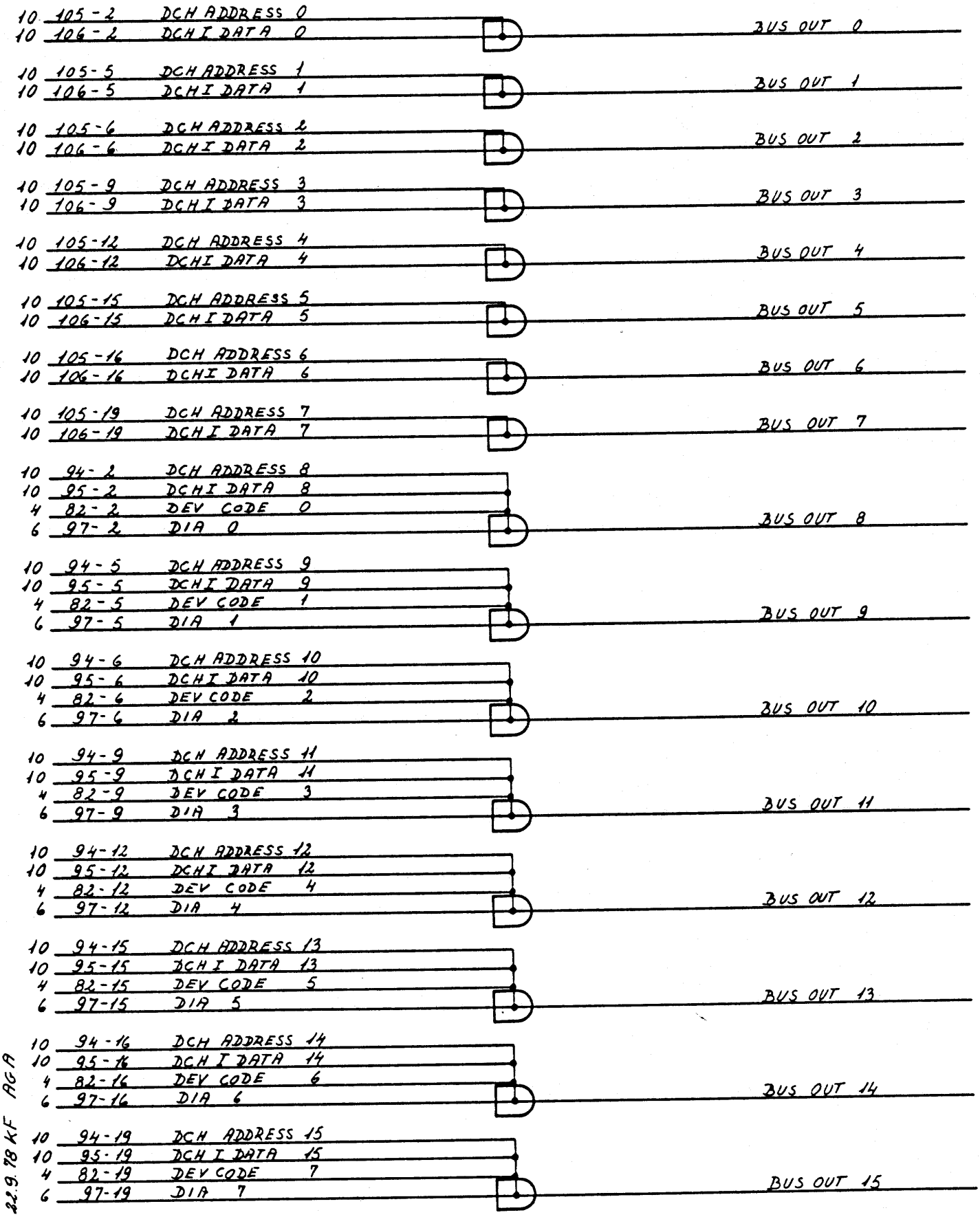

30
74LS157
11 138 - 9 READY A
11 138 - 11 MOTOR OFF A
15 67 - 8 HLD A
13 129 - 15 COUNT 16 A
12 18 - 9 READY B
12 18 - 11 MOTOR OFF B
15 67 - 11 HLD B
14 119 - 15 COUNT 16 B
READY
MOTOR OFF
HLD
CNT16
0V
109
5V
1K
4T 338
29
74LS 158
15 99 - 4 ⅂ INT A
15 99 - 2 ⅂ DRQ A
11 140 - 14 ⅂ SINGLE SIDED A
20 96 - 6 ⅂ UNIT A
15 99 - 8 ⅂ INT B
15 99 - 6 ⅂ DRQ B
12 20 - 14 ⅂ SINLE SIDED B
20 96 - 15 ⅂ UNIT B
INT
DRQ
S SIDED
UNIT (0)
40
74LS373
30 - 12 CNT 16
8 117 - 7 START
20 30 - 4 READY
20 30 - 7 MOTOR OFF
20 30 - 9 HLD
20 29 - 9 S SIDED
20 29 - 12 UNIT (0)
20 89 - 4 UNIT (1)
STATUS (0)
(1)
(2)
(3)
(4)
(5)
(6)
(7)
19 39 - 11 ⅂ EN STATUS
5 142 - 15 ⅂ MR
89
74 S 04
UNIT (1)'
96
74 276
20 96 - 16 ⅂ UNIT (1)
20 89 - 4 UNIT (1)
19 28 - 9 ⅂ CHNG UNIT
19 28 - 7 ⅂ CHNG CHANNEL
13 109 - 18 LOGIC 1
⅂ UNIT A
⅂ UNIT B
UNIT (1)
⅂ UNIT (1)
22.978 KF AGA

SIGNAL	DESTI-NATION	DESCRIPTION
CARRY	21	Refer to timing diagram
CNT 1	21	-
CNT 4	21	-
CNT 8	21	-
-,END	24	When high the MPU is stopped
-,WE	15	Write enable signal to formatters
-,RE	15	Read -"-
LOGIC 1A	15,17,21	
LOGIC 1B	21	
8 MHZ	13,21	Clock signal to Data/Clock sep.
2 MHZ	15	Clock signal to formatters

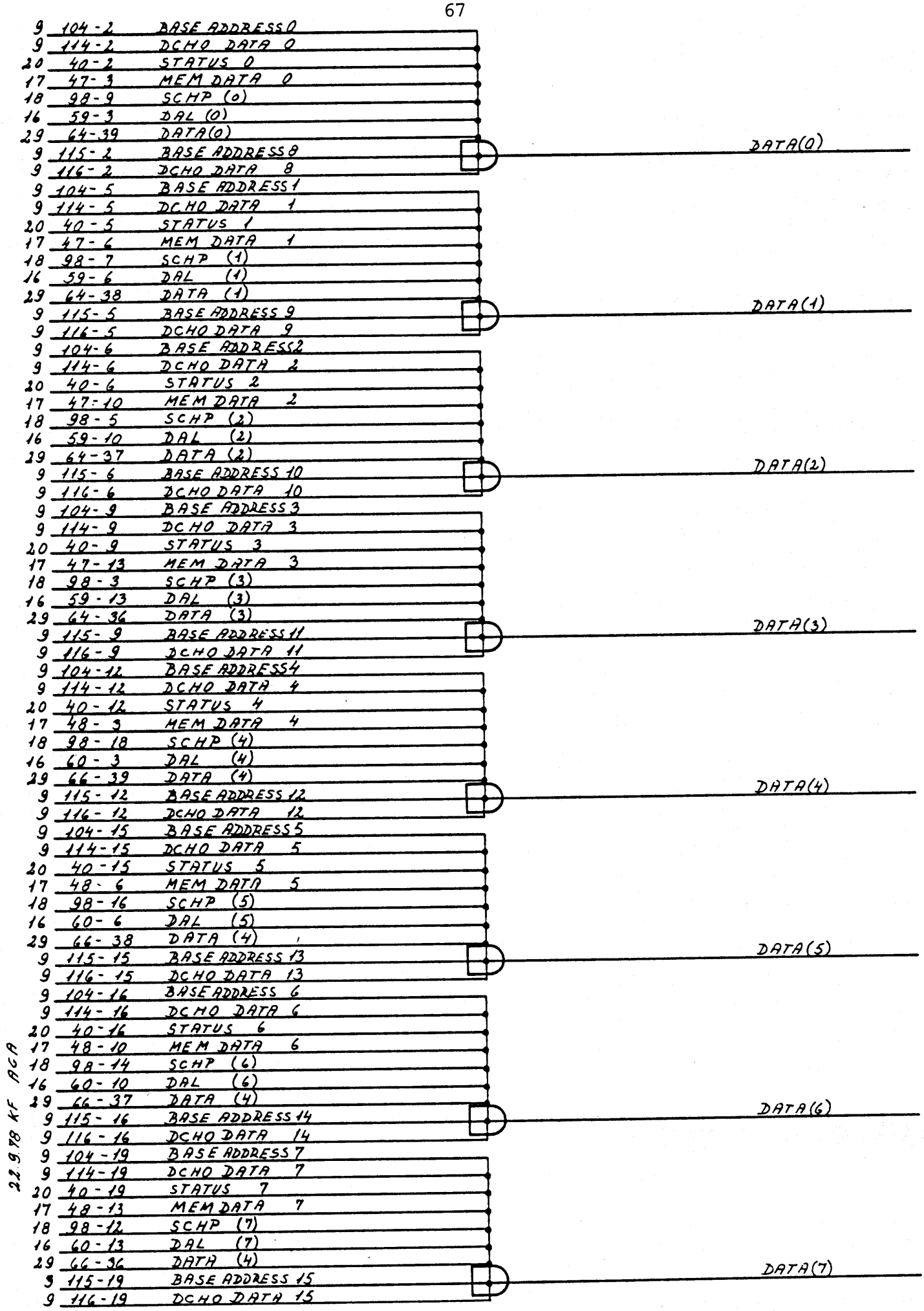


FDC 705 Formatter Timing Logic FDC 21

R 12543


10 105-2 DCH ADDRESS 0
10 106-2 DCH I DATA 0
BUS OUT 0
10 105-5 DCH ADDRESS 1
10 106-5 DCH I DATA 1
BUS OUT 1
10 105-6 DCH ADDRESS 2
10 106-6 DCH I DATA 2
BUS OUT 2
10 105-9 DCH ADDRESS 3
10 106-9 DCH I DATA 3
BUS OUT 3
10 105-12 DCH ADDRESS 4
10 106-12 DCH I DATA 4
BUS OUT 4
10 105-15 DCH ADDRESS 5
10 106-15 DCH I DATA 5
BUS OUT 5
10 105-16 DCH ADDRESS 6
10 106-16 DCH I DATA 6
BUS OUT 6
10 105-19 DCH ADDRESS 7
10 106-19 DCH I DATA 7
BUS OUT 7
10 94-2 DCH ADDRESS 8
10 95-2 DCH I DATA 8
4 82-2 DEV CODE 0
6 97-2 DIA 0
BUS OUT 8
10 94-5 DCH ADDRESS 9
10 95-5 DCH I DATA 9
4 82-5 DEV CODE 1
6 97-5 DIA 1
BUS OUT 9
10 94-6 DCH ADDRESS 10
10 95-6 DCH I DATA 10
4 82-6 DEV CODE 2
6 97-6 DIA 2
BUS OUT 10
10 94-9 DCH ADDRESS 11
10 95-9 DCH I DATA 11
4 82-9 DEV CODE 3
6 97-9 DIA 3
BUS OUT 11
10 94-12 DCH ADDRESS 12
10 95-12 DCH I DATA 12
4 82-12 DEV CODE 4
6 97-12 DIA 4
BUS OUT 12
10 94-15 DCH ADDRESS 13
10 95-15 DCH I DATA 13
4 82-15 DEV CODE 5
6 97-15 DIA 5
BUS OUT 13
10 94-16 DCH ADDRESS 14
10 95-16 DCH I DATA 14
4 82-16 DEV CODE 6
6 97-16 DIA 6
BUS OUT 14
10 94-19 DCH ADDRESS 15
10 95-19 DCH I DATA 15
4 82-19 DEV CODE 7
6 97-19 DIA 7
BUS OUT 15

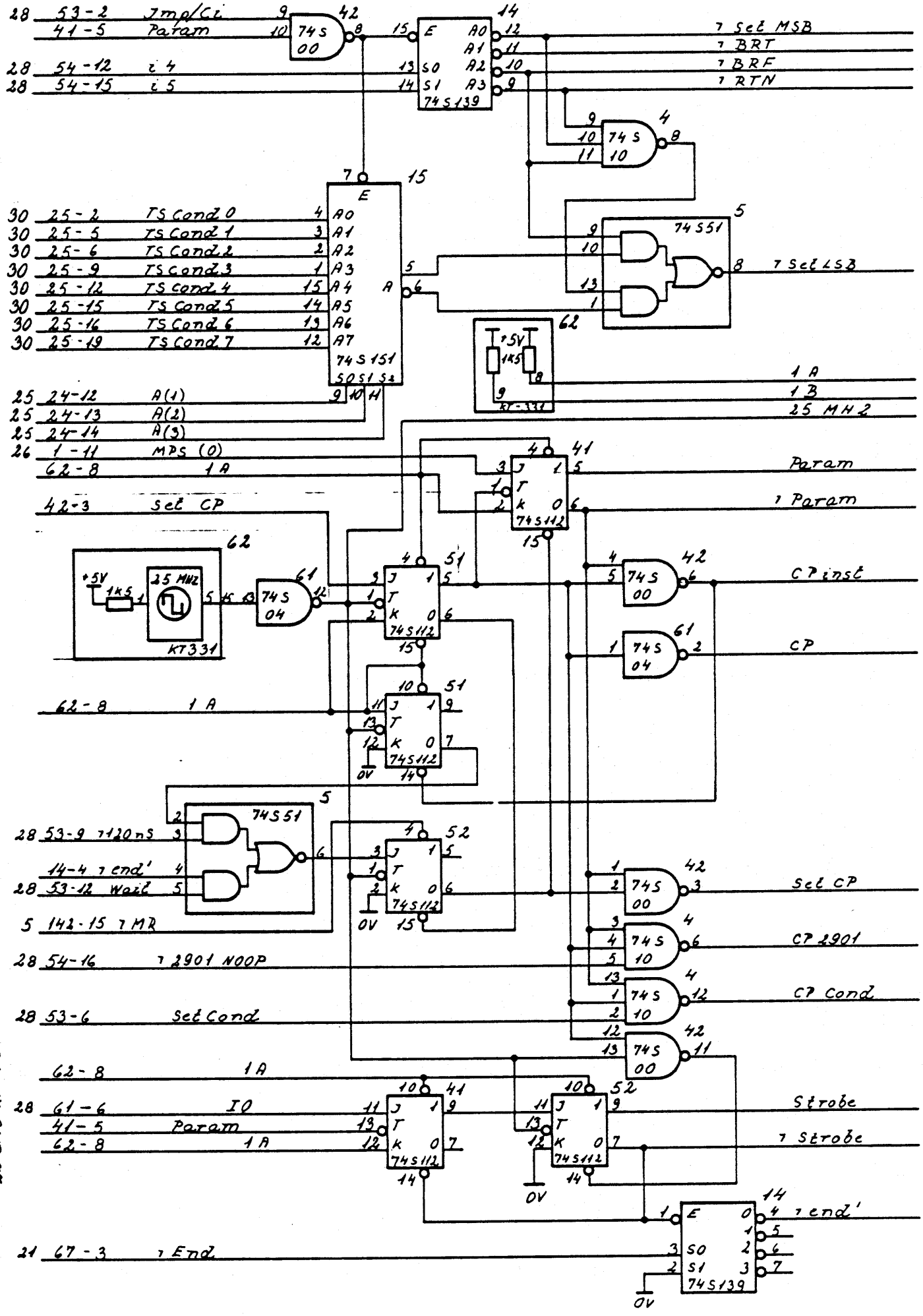
22.9.78 KF AG A



FDC 705 DATA BUS FDC 23

R 12545

SIGNAL	DESTI-NATION	DESCRIPTION
-,SET MSB	25	Parallel load MSB's of program counter
-,BRT	NC	Branch on condition true inst.
-,BRF		-"- false inst.
-,RTN	25,30	Disable ROM's and enable rtn. reg
-,SET LSB	25	Parallel load LSB's of program counter
1A	24	logic 1
1B	25,28,29, 30	-"-
Param	24,25,28	The next clock pulse is for a parameter
-,PARAM		
CP INST	28	Instruction register clock pulse
CP	24,25,28, 30	Clock Pulse
SET CP	24	Generate a Clock Pulse on next 25 MHZ period
CP 2901	29	Clock Pulse for AM 2901
CP COND	30	Condition Register Clock Pulse
STROBE	17,18	Output Strobe
-,STROBE	19	
-,END'	24	Continue execution

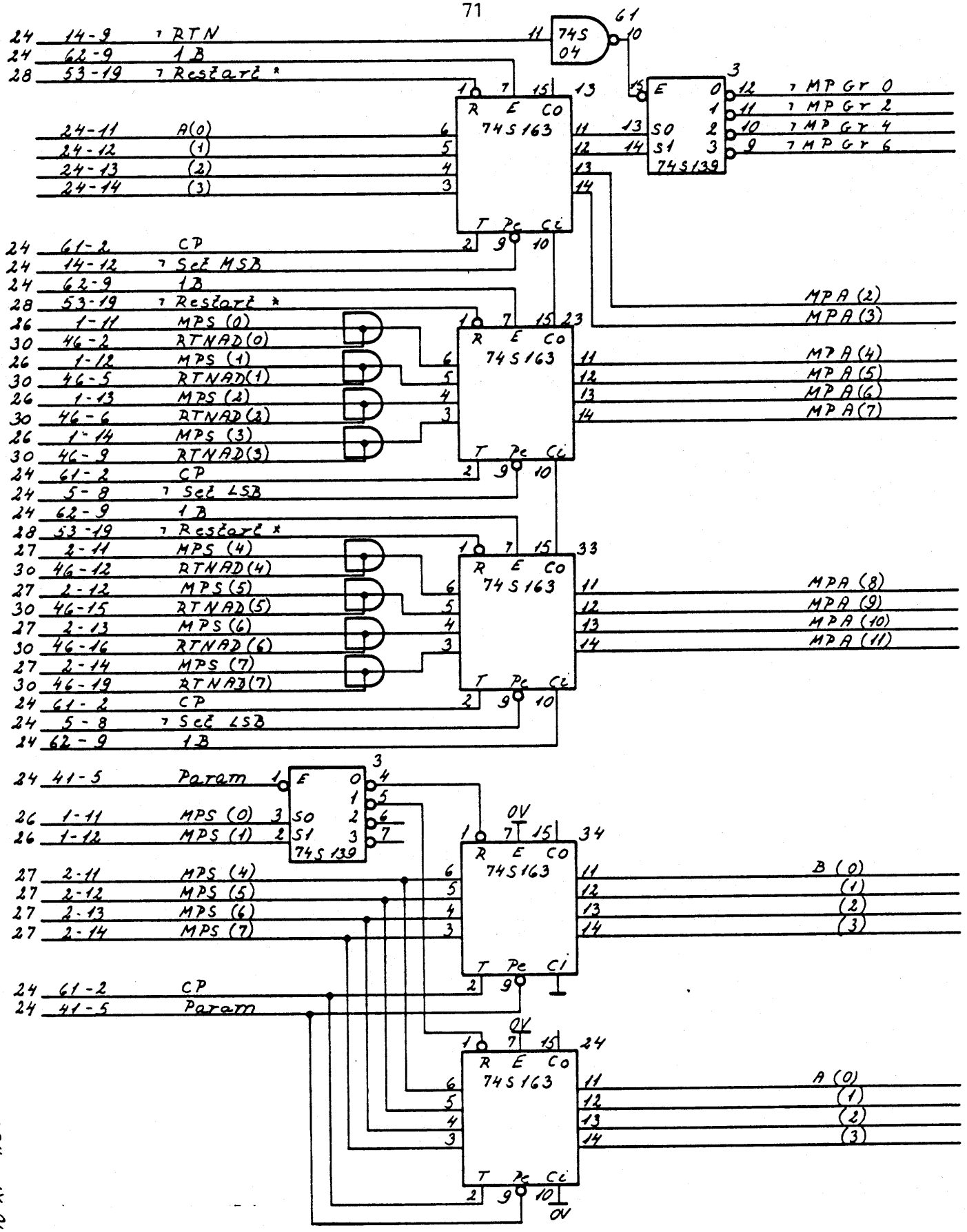


FDC 705 Clock generation and Jump Controle FDC 24

R 12546

SIGNAL	DESTI-NATION	DESCRIPTION
-,MPGR Ø	26,27	Enable ROM (address Ø-1777)
-,MPGR 2	26,27	-"- (-"- 2000-3777)
-,MPGR 4	26,27	-"- (-"- 4000-5777)
-,MPGR 6	26,27	-"- (-"- 6000-7777)
MPA (2-11)	26,27	Microprogram Address
B (0)	NC	
B(1-3)	29	2901 register "B" address
A(0)	25,30	2901 register "A" address, MSB of
A(1-3)	24,25,29	jump address and condition select

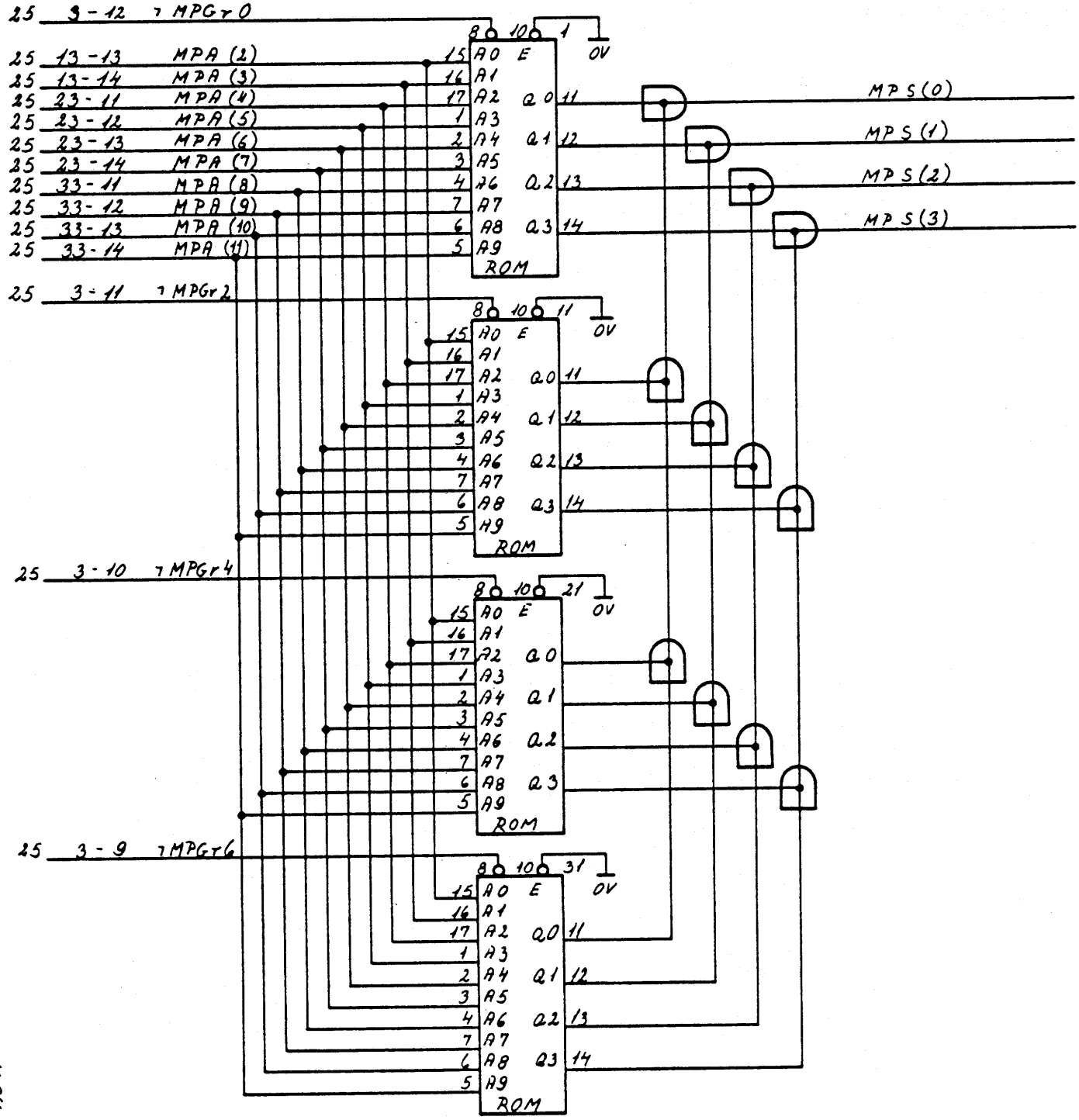
Unit		
FDC 705		FDC 25



FDC 705 Programcounter and Register Address Latches FDC 25

R 12547

SIGNAL	DESTI-NATION	DESCRIPTION
MPS (Ø)	24,25,28, 30	Microprogram memory data
MPS (1-3)	25,28,30	

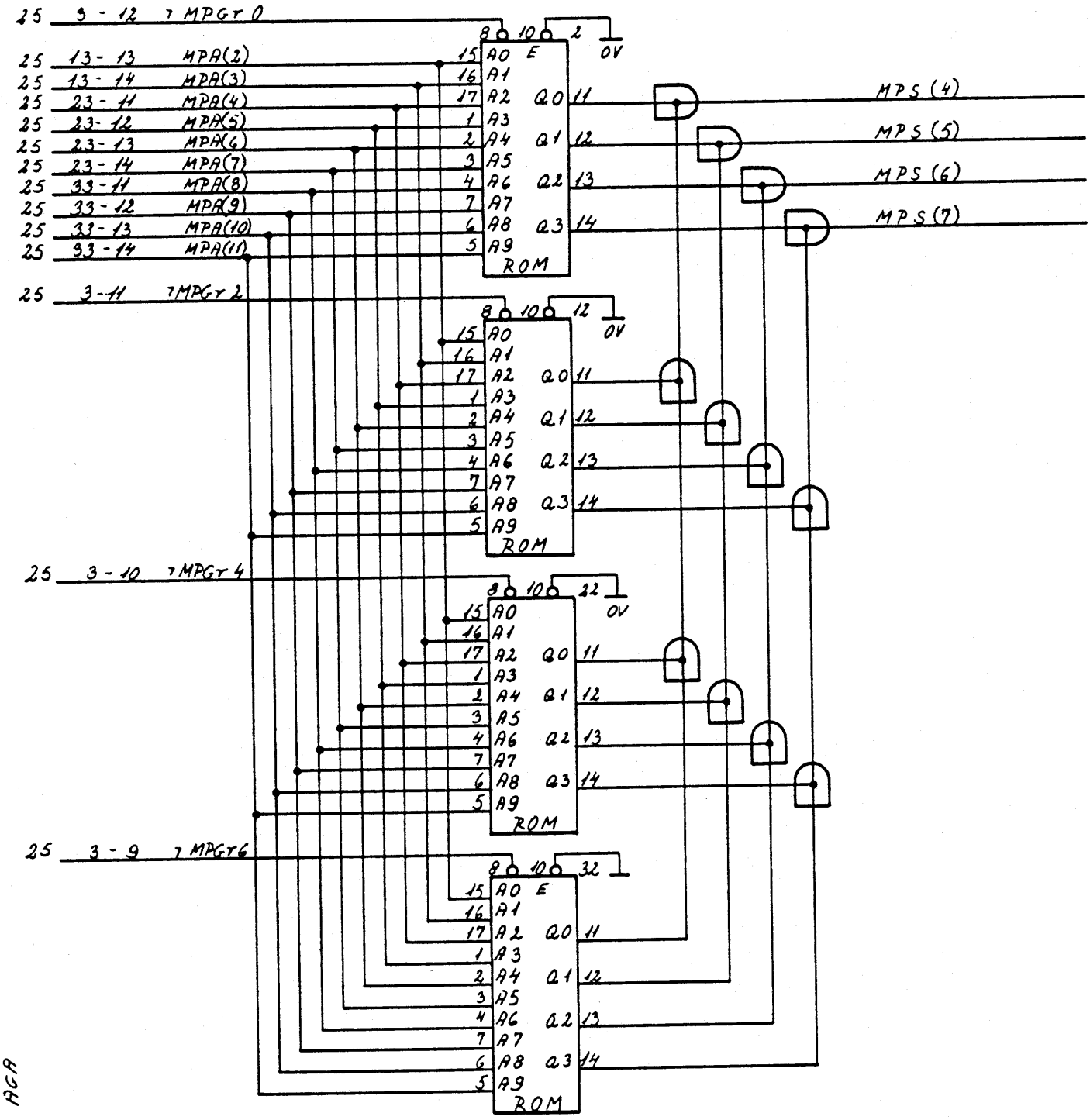


22.9.78 KF AG19

FDC 705 Microprogramstore MPS (4:7) FDC26

R12548

SIGNAL	DESTI-NATION	DESCRIPTION
MPS (4-7)	25,28,30	Microprogram memory data



22.9.78 KF AGA

FDC705

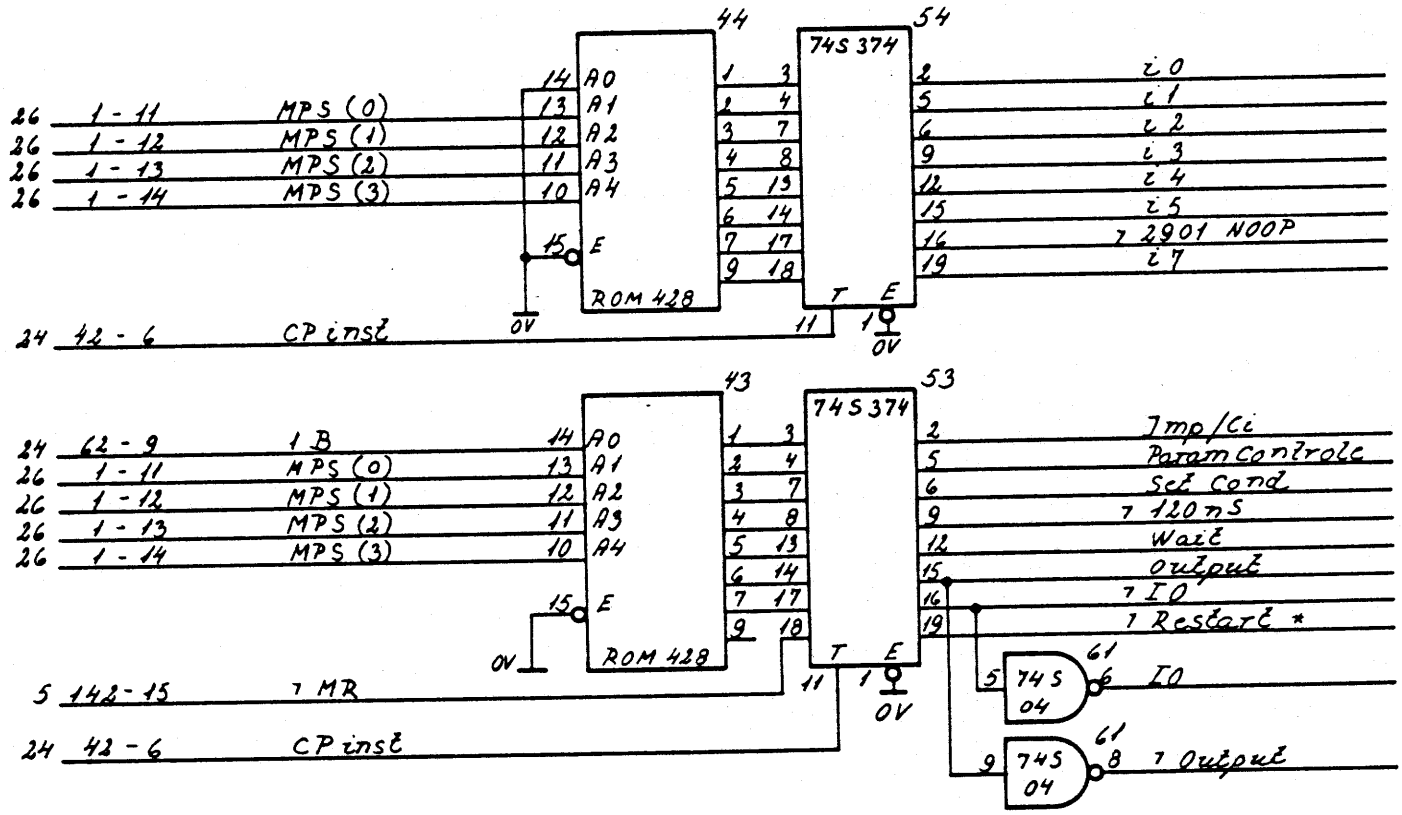
2 12549

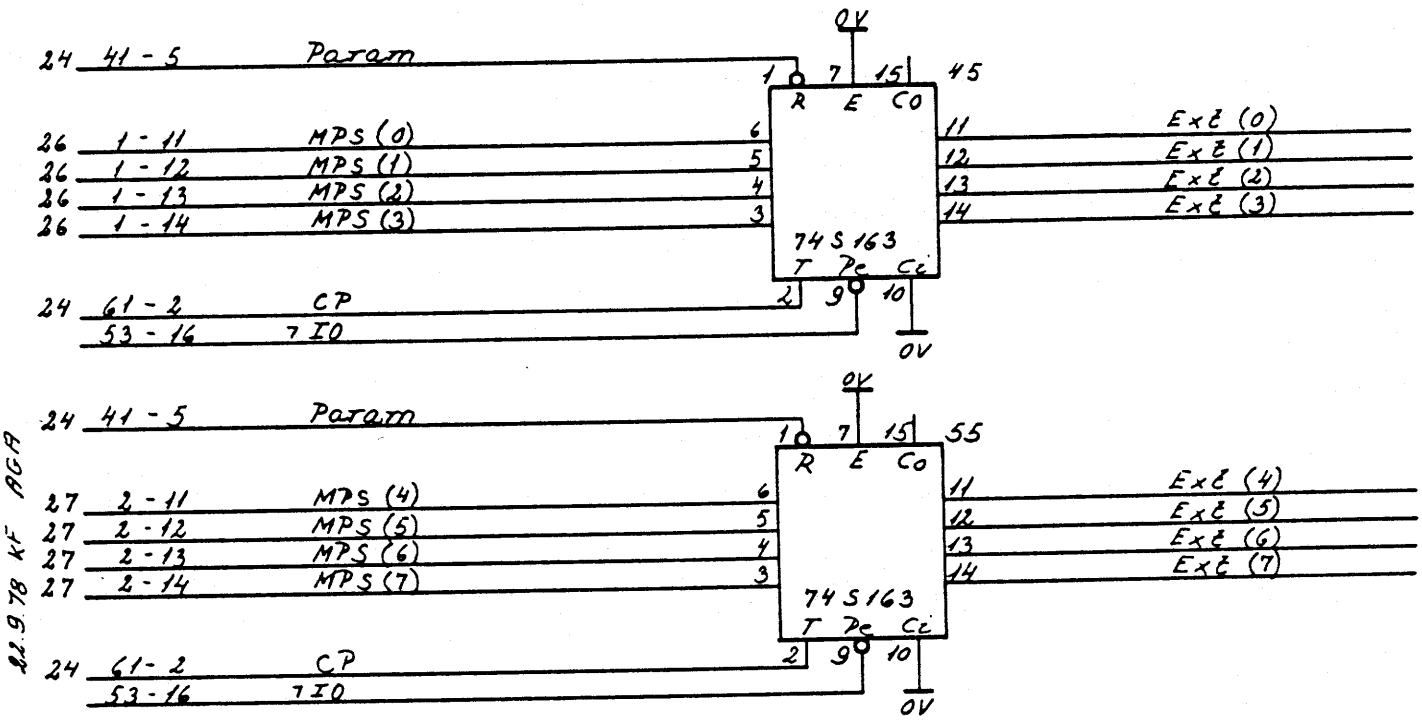
Microprogramsčore MPS (4:7)

FDC 27

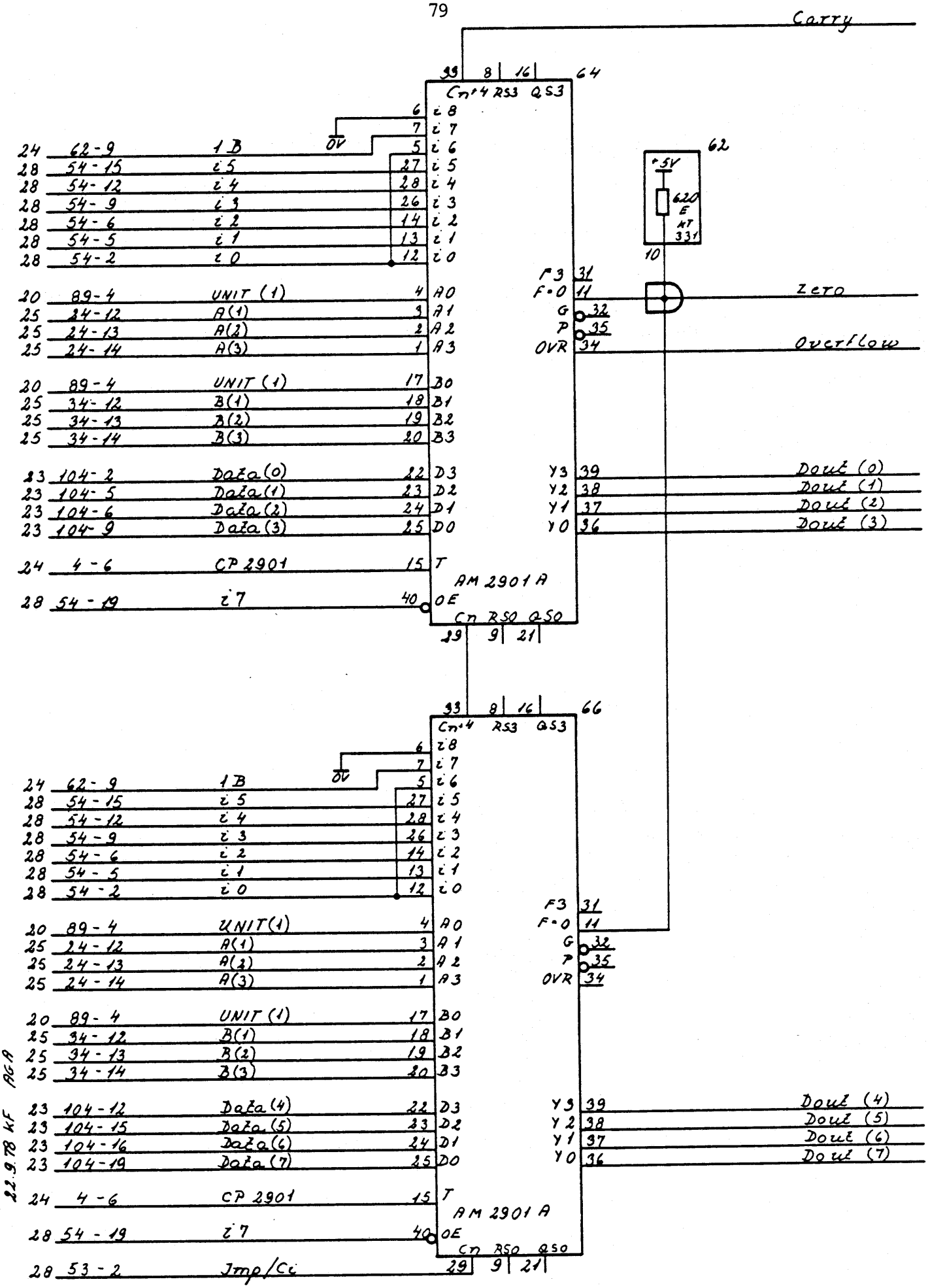
SIGNAL	DESTI-NATION	DESCRIPTION
iø	29	2901 instruction signals
i1	29	-"-
i2	29	-"-
i3	29	-"-
i4	24,29	2901 instruction and
i5	24,29	jump control signals
-,2901 NOOP	24	No clock pulse to 2901
i7	29	2901 output enable
JMP/ci	24,29	2901 carry in or jump instr.
PARAM CONTROLE	30	Gate parameter register to data bus
SET COND	24	Clock the condition register
-,120 NS	24	Fast instruction cycle
WAIT	24	I/O wait for slow device
OUTPUT	17,18,19, 21	output instruction
-,IO	19,28	I/O instruction
-,RESTART*	25	Syncronized Master Reset. Resets the program counter
IO	24	
-,OUTPUT	17,18,19	
EXT (0)	17, 19	
EXT (1)	18, 19	
EXT (2)	19,21,28	I/O address register
EXT (3-5)	18,19	
EXT (6-7)	15,18,19	

Unit		
FDC 705		FDC 28


44
54
74S374
ROM 428
MPS (0)
MPS (1)
MPS (2)
MPS (3)
CP inst
i 0
i 1
i 2
i 3
i 4
i 5
¬ 2901 NOOP
i 7
43
53
74S374
ROM 428
1 B
MPS (0)
MPS (1)
MPS (2)
MPS (3)
¬ MR
CP inst
Imp/Ci
Param controle
Sel Cond
¬ 120 nS
Wait
Ouput
¬ IO
¬ Restart *
74S 04
IO
¬ Ouput


45
74S163
Param
MPS (0)
MPS (1)
MPS (2)
MPS (3)
CP
¬ IO
Exé (0)
Exé (1)
Exé (2)
Exé (3)
55
74S163
Param
MPS (4)
MPS (5)
MPS (6)
MPS (7)
CP
¬ IO
Exé (4)
Exé (5)
Exé (6)
Exé (7)

SIGNAL	DESTI-NATION	DESCRIPTION
CARRY	30	ALU Carry out
ZERO	30	ALU Result equals zero
OVERFLOW	30	ALU overflow
DOUT (0-7)	30	MPU Data bus

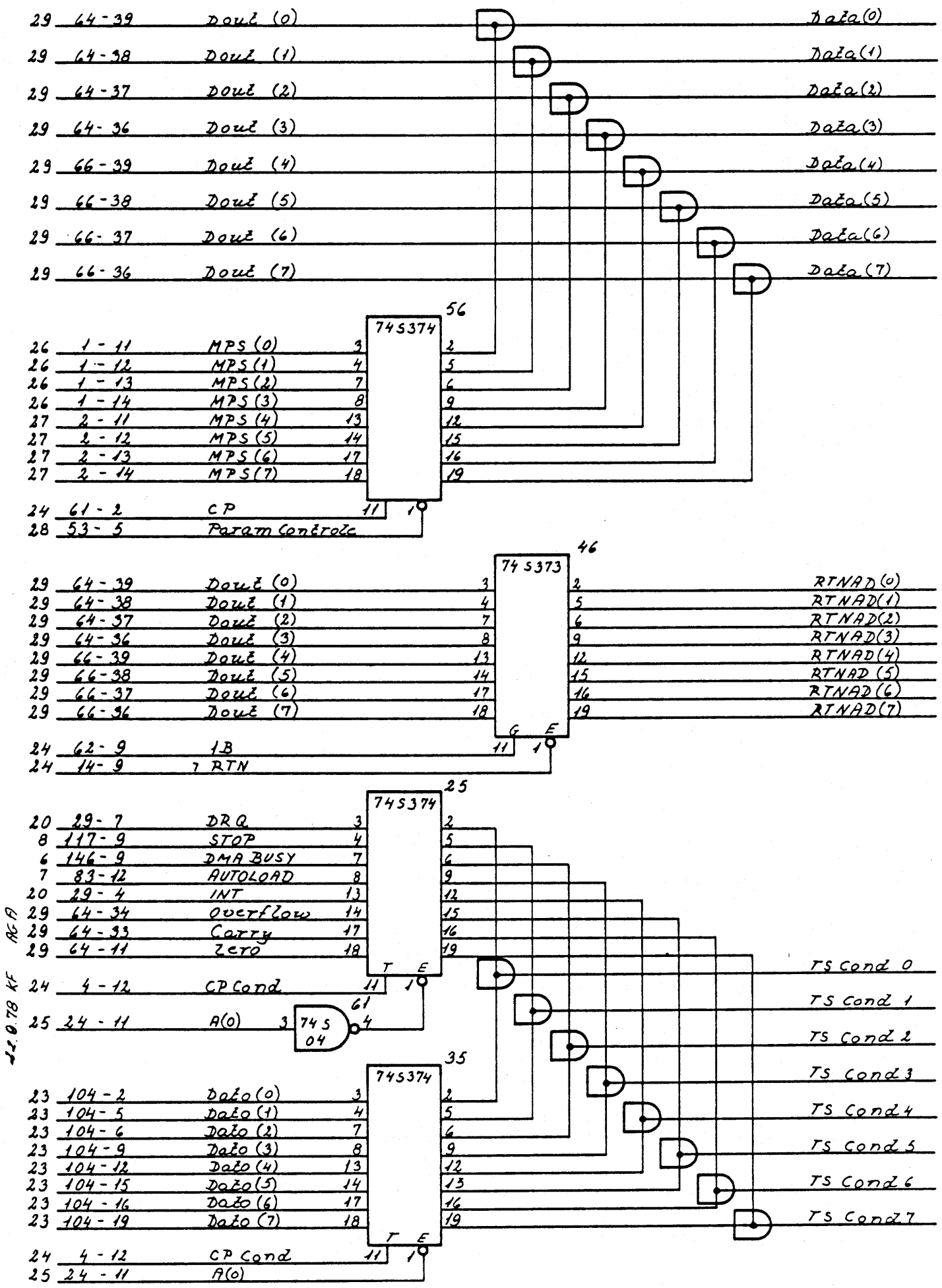


FDC 705 Register/Arithmetic/Logic Unit FDC 29

R 12 551

SIGNAL	DESTI-NATION	DESCRIPTION
DATA (0-7)	23	MPU data bus
RTNAD (0-7)	25	MPU data bus to address bus transceiver. Used during the instruction RTN
TS COND (0-7)	24	16-8 selected condition signals

Unit		
FDC 705		FDC 30

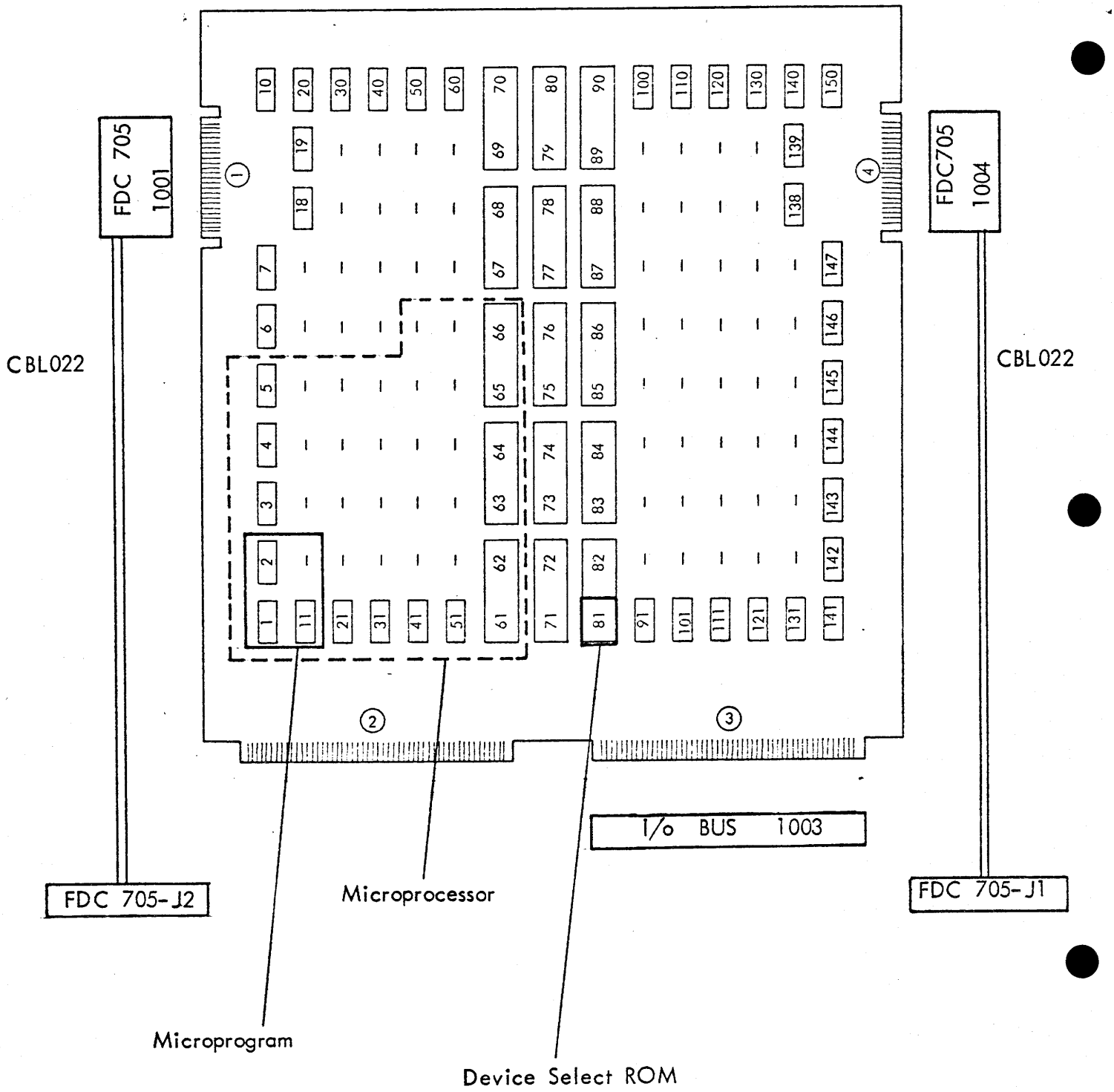


FDC 705 I/O Databus and jump Conditions registers FDC 30

R 12 552

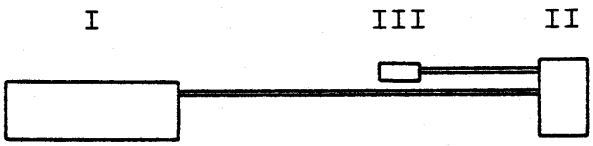
6. Assembly Drawing.

6.



7. Plug lists. 7.

7.1 Internal Cable, CBL022. 7.1



I: 2 x 25 Socket Edge Connector
II: Cannon 52 P
III: Spade point

I		II		
Ground	Signal	Ground	Signal	Description
B1	A1	2	1	-,Head load (n)
B2	A2	4	3	-,Write Data
B3	A3	6	5	-,Select (n)
B4	A4	8	7	-,Select (n+2)
B5	A5	10	9	-,Step
B6	A6	12	11	-,Direction Select
B7	A7	14	13	
B8	A8	16	15	-,Write Protect
B9	A9	35	17	-,Track ØØ
B10	A10	33	34	-,Index
B11	A11	31	32	-,Disk Change
B12	A12	29	30	
B13	A13	27	28	-,In use (n)
B14	A14	25	26	-,In use (n+2)
B15	A15	23	24	-,Write Gate
B16	A16	21	22	-,Side Select
B17	A17	19	20	
B18	A18	36	18	
B19	A19	38	37	-,Spare
B20	A20	40	39	-,Two Sided
B21	A21	42	41	-,Low Current
B22	A22	44	43	-,Head load (n+2)
B23	A23	46	45	-,Ready
B24	A24	48	47	-,Read Data
B25	A25	50	49	-,Motor off
III		52	51	Chassis Ground

CBL 022
Internal Controller Chassis
Cable for FDC 705

7.2 Back Panel I/O Bus Connector 1003.

PIN NO.	A	B
1	+5V	+5V
2	-12V	-12V
3	-24V	-24V
4	V3	V3
5	-,DS 0	POB
6	-,DS 1	0V
7	-,DS 2	0V
8	-,DS 3	0V
9	-,DS 4	0VFLO
10	-,DS 5	0V
11	-,DCHA	0V
12	DCHI	0V
13	DCHO	INTA
14	-,DATA 0	0V
15	-,DATA 1	0V
16	-,DATA 2	0V
17	-,DATA 3	-,DATA 4
18	-,DATA 5	0V
19	-,DATA 6	0V
20	-,DATA 7	0V
21	-,DATA 8	-,DATA 9
22	-,DATA 10	0V
23	-,DATA 11	0V
24	-,DATA 12	0V
25	-,DATA 13	-,DATA 14
26	-,DATA 15	0V
27	POK	0V
28	-,PINT	0V
29	-,SELB	-,SELD
30	-,INTR	0V
31	-,DCHR	0V
32	DATOA	0V
33	DATOB	IOPLS
34	DATOC	0V
35	DATIA	0V
36	DATIB	0V
37	DATIC	CLR
38	STRT	0V
39	-,RQENB	0V
40	-,MSKO	0V
41	-,INTP OUT	-,INTP IN
42	IORST	0V
43	-,DCHM 0	0V
44	-,DCHM 1	0V
45	-,DCHP OUT	-,DCHP IN
46	V2	V2
47	+24V	+24V
48	+12V	+12V
49	+5V	+5V

NOVAI/O BUS SIGNAL ALLOCATION

BACK PANEL CONNECTOR 1003

8. Component list. 8.

The following electrical components are used in the FDC 705 controller:

Qty	Description	RC part No.
1	SN7400N	35900
4	SN7406N	19308
2	SN7438N	40804
1	SN74120N	57102
1	SN74276N	63603
2	SN74S00N	55910
2	SN74S04N	43713
1	SN74S10N	56500
1	SN74S51N	54405
1	SN74S74N	43715
3	SN74S112N	56503
3	SN74S138N	57107
2	SN74S139N	58200
1	SN74S151N	57101
8	SN74S163N	58203
1	SN74S260N	58209
1	SN74S373N	58212
5	SN745374N	58213
1	SN74S412N	56717
2	SN74LS00N	52611
3	SN74LS02N	52605
1	SN74LS04N	49807
3	SN74LS08N	52606
3	SN74LSI0N	61803
2	SN74LS14N	58111
8	SN74LS74N	52608
1	SN74LS123N	61915
2	SN74LS132N	58112
1	SN74LS155N	
1	SN74LS157N	58114
1	SN74LS158N	58115
4	SN74LS161N	52609
3	SN74LS240N	61904
2	SN74LS273N	63618
3	SN74LS279N	63619
1	SN74LS352N	
3	SN74LS373N	61909
8	SN74LS374N	61910
1	SN75451P	40800
12	SN75452P	55909
2	AM25LS2539PC	
2	AM2901A	63716
1	N82S09	58218
2	8216	63715
2	8226	
2	INS1771-2	

Qty	Description	RC part No.	
2	2114-2	63809	
1	VP5	60701	
1	VP12	58811	
2	906C102 x 5VG	60014	
2	916C102 x 5PE	60015	
1	CCO-8 8MHZ	60008	
1	CCO-8 25MHZ		
1	Condenser, Tantol, JµF/35V		38301
2	-"- -"- , 22µF/15V		11118
49	-"- , Ceramic, 47nF/12V		43911
1	-"- , 5% 1nF/63V		11303
4	Resistor, metal film 330E 2% 0,4w		44018
2	-"- -"- 120E 2% 0,4w		
4	-"- -"- 390E 2% 0,4w		44019
16	-"- -"- 150E 2% 0,4w		
10	-"- , Carbon JK 5% 1/8w		10600
1	-"- , -"- 680E 5% 1/8w		15203
4	-"- , -"- 10K 5% 1/8w		10704
1	-"- , -"- 1K 5% 1/20w		57402
2	-"- , -"- 82K 5% 1/8w		10806
2	SN74S288		
1	MMI 6309-1J		
4	MMI 6353-1J		

9. Components Description and Specifications. 9.

The following pages contain the component specifications for some of the integrated circuits used in the controller.

Listnings of the PROM contents are provided for the functional PROM's. For a listning of the microprogram PROM's refer to the program listning.

ROM 428

Instruction	Address	Contents								Address								
Mnemonies	Octal	(2901A Controle)								Octal								
		iø /i6	i1	i2	i3	i4/JMP CNTRL	i5/JMP CNTRL	-,2901 NOOP	-,OE		JUMP/ci PARAM CONTROLE			SET COND -,120NS WAIT		OUTPUT -,IO		not used
ADD	0	1	0	0	0	0	0	1	0	20	0	1	1	1	0	0	1	0
SUB	1	1	0	0	1	0	0	1	0	21	0	1	1	1	0	0	1	0
AND	2	1	0	0	0	0	1	1	0	22	0	1	1	0	0	0	1	0
XOR	3	1	0	0	0	1	1	1	0	23	0	1	1	0	0	0	1	0
INC	4	1	1	0	0	0	0	1	0	24	1	1	1	1	0	0	1	0
DEC	5	1	1	0	1	0	0	1	0	25	0	1	1	1	0	0	1	0
OR	6	1	0	0	1	1	0	1	0	26	0	1	1	0	0	0	1	0
MOV	7	0	0	1	1	1	0	1	0	27	0	1	1	0	0	0	1	0
LD	10	1	1	1	1	1	0	1	1	30	0	0	0	1	0	0	1	0
IN	11	1	1	1	1	1	0	1	1	31	0	1	1	1	1	0	0	0
OUT	12	0	0	1	1	1	0	0	0	32	0	1	1	1	1	1	0	0
FUT	13	0	0	1	1	1	0	0	0	33	0	1	1	1	0	1	0	0
JMP	14	0	0	0	0	0	0	0	1	34	1	0	0	1	0	0	1	0
BRT	15	0	0	0	0	0	1	0	1	35	1	0	0	1	0	0	1	0
BRF	16	0	0	0	0	1	0	0	1	36	1	0	0	1	0	0	1	0
RTN	17	0	0	0	0	1	1	0	0	37	1	1	0	1	0	0	1	0

ROM SIZE: 32 x 8

Instruction Decode ROM's

ROM 428

ROM 491

Address Octal	Address Binary	Contents Binary	Contents Octal
	C0 C1 C2 C3 C4 C5 C6 C7	Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7	
	INTA INTR -,DSØ - 1 - 2 - 3 - 4 - 5	DEVCODE Ø /DEVSEL - 1 - 2 - 3 - 4 - 5 - 6 - 7	
0	0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1	177
15	0 0 0 0 1 1 0 1	0 1 1 1 1 1 1 1	177
16	0 0 0 0 1 1 1 0	1 1 1 1 1 1 1 1	377
17	0 0 0 0 1 1 1 1	0 1 1 1 1 1 1 1	177
115	0 1 0 0 1 1 0 1	0 1 1 1 1 1 1 1	177
116	0 1 0 0 1 1 1 0	1 1 1 1 1 1 1 1	377
117	0 1 0 0 1 1 1 1	0 1 1 1 1 1 1 1	177
277	1 0 1 1 1 1 1 1	0 1 1 1 1 1 1 1	177
300	1 1 0 0 0 0 0 0	0 0 1 1 0 0 0 1	61
377	1 1 1 1 1 1 1 1	0 0 1 1 0 0 0 1	61

ROM SIZE: 256 x 8

Device Select Decode ROM

Device code = 61

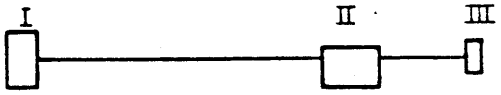
ROM 498

Address Octal	Address Binary	Contents Binary	Contents Octal
	C0 C1 C2 C3 C4 C5 C6 C7	Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7	
	INTA INTR -,DSØ - 1 - 2 - 3 - 4 - 5	DEVCODE Ø /DEVSEL - 1 - 2 - 3 - 4 - 5 - 6 - 7	
0	0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1	177
12	0 0 0 0 1 0 1 0	0 1 1 1 1 1 1 1	177
13	0 0 0 0 1 0 1 1	1 1 1 1 1 1 1 1	377
14	0 0 0 0 1 1 0 0	0 1 1 1 1 1 1 1	177
112	0 1 0 0 1 0 1 0	0 1 1 1 1 1 1 1	177
113	0 1 0 0 1 0 1 1	1 1 1 1 1 1 1 1	377
114	0 1 0 0 1 1 0 0	0 1 1 1 1 1 1 1	177
277	1 0 1 1 1 1 1 1	0 1 1 1 1 1 1 1	177
300	1 1 0 0 0 0 0 0	0 0 1 1 0 1 0 0	64
377	1 1 1 1 1 1 1 1	0 0 1 1 0 1 0 0	64

ROM SIZE: 256 x 8

Device Select Decode ROM

Device code = 64

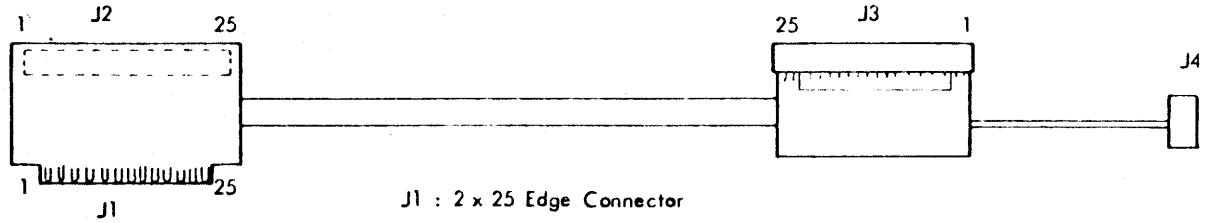


I : Cannon 52 P
II : 2x25 Socket Edge Connector
III : Berg Minilatch Housing 1 x 5 Contacts.

I		II		III		
Ground	Signal	Ground	Signal	Ground	Signal	Description
2	1	A9	B9	-	-	-, Head Load (n)
4	3	A19	B19	-	-	-, Write Data
6	5	A13	B13	-	-	-, Drive Select (n)
8	7	A14	B14	-	-	-, Drive Select (n+2)
10	9	A18	B18	-	-	-, Step
12	11	A17	B17	-	-	-, Direction Select
16	15	A22	B22	-	-	-, Write Protect
35	17	A21	B21	-	-	-, Track 0 0
33	34	A10	B10	-	-	-, Index
31	32	A6	B6	-	-	-, Disk Change
27	28	-	-	1	3	-, IN Use (n)
-	-	A16	B16	4	5	Motor off
25	26	A15	B15	-	-	-, In Use (n+2)
23	24	A20	B20	-	-	-, Write Gate
21	22	A7	B7	-	-	-, Side Select
38	37	A2	B2	-	-	-, Spare
40	39	A5	B5	-	-	-, Two Sided
42	41	A1	B1	-	-	-, Low Cur
44	43	A8	B8	-	-	-, Head Load (n+2)
46	45	A11	B11	-	-	-, Ready
48	47	A23	B23	-	-	-, Read Data
50	49	A12	B12	-	-	-, Motor off

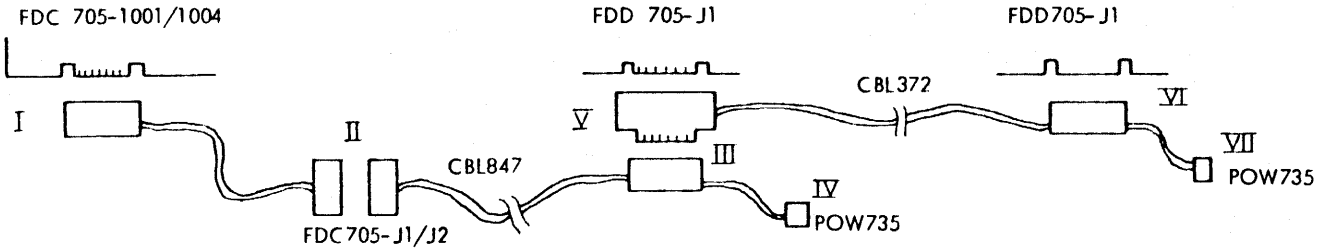
R 12565

CBL 372
Connecting FDD 705 to FDD 705
(Daisy Chain Cable)



J1 : 2 x 25 Edge Connector
J2 : 2 x 25 Socket Edge Connector
J3 : 2 x 25 Socket Edge Connector
J4 : Berg Minilatch 1 x 5 Contacts

J1		J2		J3		J4		Signal Name
Ground	Signal	Ground	Signal	Ground	Signal	Ground	Signal	
A1	B1	A 1	B1	A1	B1			7 Low Cur
A2	B2	A2	B2	A2	B2			7 Spare
A5	B5	A5	B5	A5	B5			7 Two Sided
A6	B6	A6	B6	A6	B6			7 Disk Change
A7	B7	A7	B7	A7	B7			7 Side Select
A8	B8	-	-	A9	B9			7 Head Load (n+2)
A9	B9	A9	B9	-	-			7 Head Load (n)
A10	B10	A10	B10	A10	B10			7 Index
A11	B11	A11	B11	A11	B11			7 Ready
A12	B12	A12	B12	A12	B12			7 Motor off
A13	B13	A13	B13	-	-			7 Drive Select (n)
A14	B14	-	-	A13	B13			7 Drive Select (n+2)
A15	B15	-	-	-	-	1	3	7 In use (n+2)
-	-	-	-	A16	B16	4	5	Motor off
A16	B16	A16	B16	-	-			Motor off
A17	B17	A17	B17	A17	B17			7 Direction Select
A18	B18	A18	B18	A18	B18			7 Step
A19	B19	A19	B19	A19	B19			7 Write Date
A20	B20	A20	B20	A20	B20			7 Write Gate
A21	B21	A21	B21	A21	B21			7 Track 0 0
A22	B22	A22	B22	A22	B22			7 Write Protect
A23	B23	A23	B23	A23	B23			7 Read Data



Interconnection Signal Reference Table.

I		II		III		IV		V		VI		VII		
FDC705-1004(or1001)		FDC705-J1 (or J2)		CBL847 Socket Edge Connector		POW 735 Unit 0 (or 1)		FDD705-J1 Unit 0(or 1)		FDD705-J1 Unit 2(or 3)		POW 735 Unit 2(or 3)		
Ground	Signal	Ground	Signal	Ground	Signal	Ground	Signal	Ground	Signal	Ground	Signal	Ground	Signal	Signal Description
B1	A1	2	1	A9	B9			17	18					7 Head Load (n)
B2	A2	4	3	A19	B19			37	38	37	38			7 Write Data
B3	A3	6	5	A13	B13			25	26	—	—			7 Drive Select (n)
B4	A4	8	7	A14	B14					25	26			7 Drive Select (n+2)
B5	A5	10	9	A18	B18			35	36	35	36			7 Step
B6	A6	12	11	A17	B17			33	34	33	34			7 Direction Select
B7	A7	14	13					—	—	—	—			
B8	A8	16	15	A22	B22			43	44	43	44			7 Write Protect
B9	A9	35	17	A21	B21			41	42	41	42			7 Track 0 0
B10	A10	33	34	A10	B10			19	20	19	20			7 Index
B11	A11	31	32	A6	B6			11	12	11	12			7 Dirk Change
B12	A12	29	30	—	—			—	—	—	—			
B13	A13	27	28	—	—	1	3	—	—	—	—			7 In Use (n)
—	—	—	—	A16	B16	4	5	31	32	—	—			Motor off
B14	A14	25	26	A15	B15			—	—	—	—	1	3	7 In Use (n+2)
—	—	—	—	—	—			—	—	31	32	4	5	Motor off
B15	A15	23	24	A20	B20			39	40	39	40			7 Write Gate
B16	A16	21	22	A7	B7			13	14	13	14			7 Side Select
B17	A17	19	20	—	—			—	—	—	—			
B18	A18	36	18	—	—			—	—	—	—			
B19	A19	38	37	A2	B2			3	4	3	4			7 Spare
B20	A20	40	39	A5	B5			9	10	9	10			7 Two Sided
B21	A21	42	41	A1	B1			1	2	1	2			7 Low Current
B22	A22	44	43	A8	B8			—	—	17	18			7 Head Load (n+2)
B23	A23	46	45	A11	B11			21	22	21	22			7 Ready
B24	A24	48	47	A23	B23			45	46	45	46			7 Read Data
B25	A25	50	49	A12	B12			23	24	23	24			7 Motor off