
Title:

CPU 720

MICROPROGRAM FLOWCHARTS

PRELIMINARY DOCUMENTATION

 **REGNECENTRALEN**

RC SYSTEM LIBRARY: FALKONERALLE 1 DK-2000 COPENHAGEN F

RCSL No: 44- RT 1877

Edition: 790323

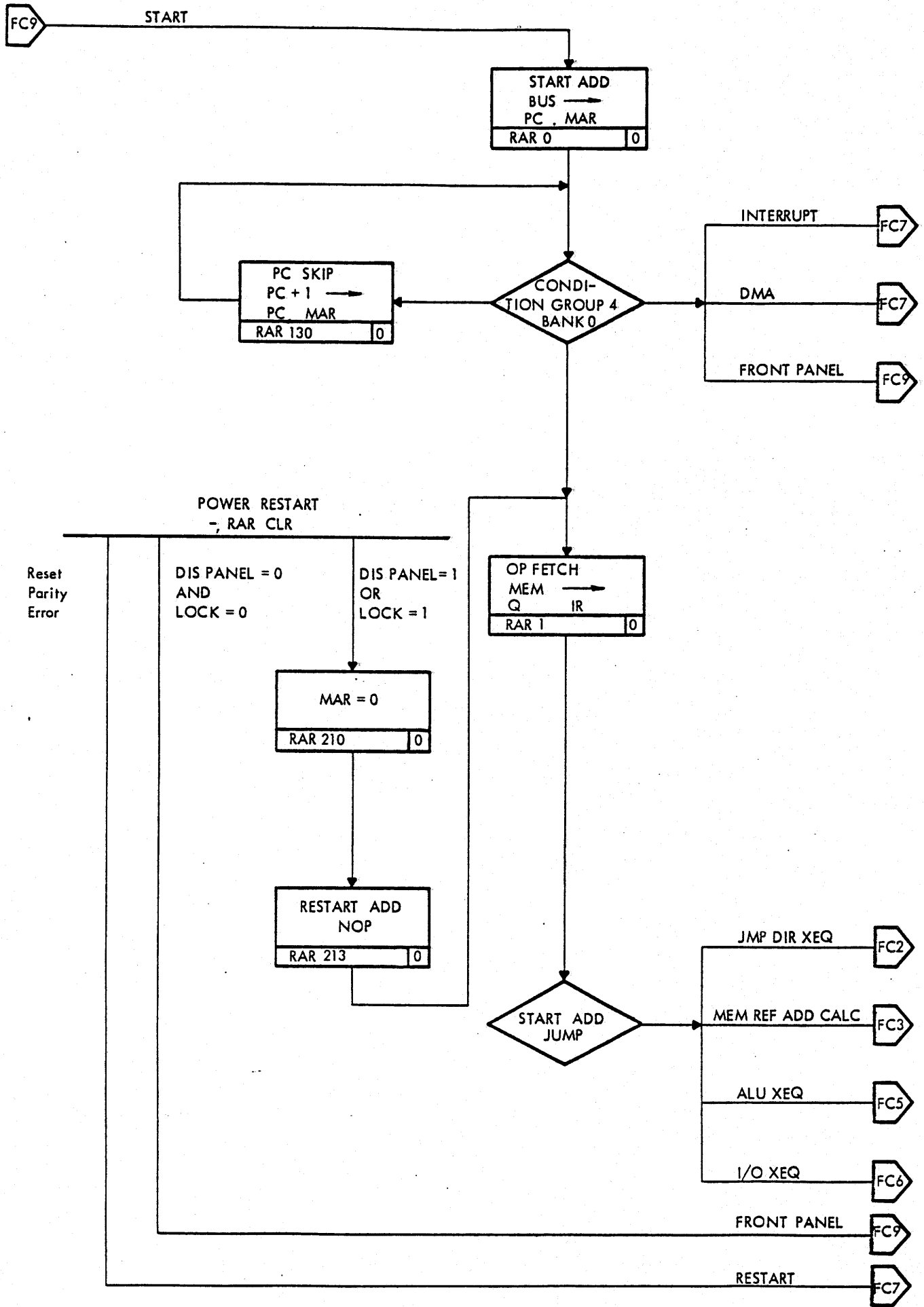
Author: BJ

Keywords:

Abstract:

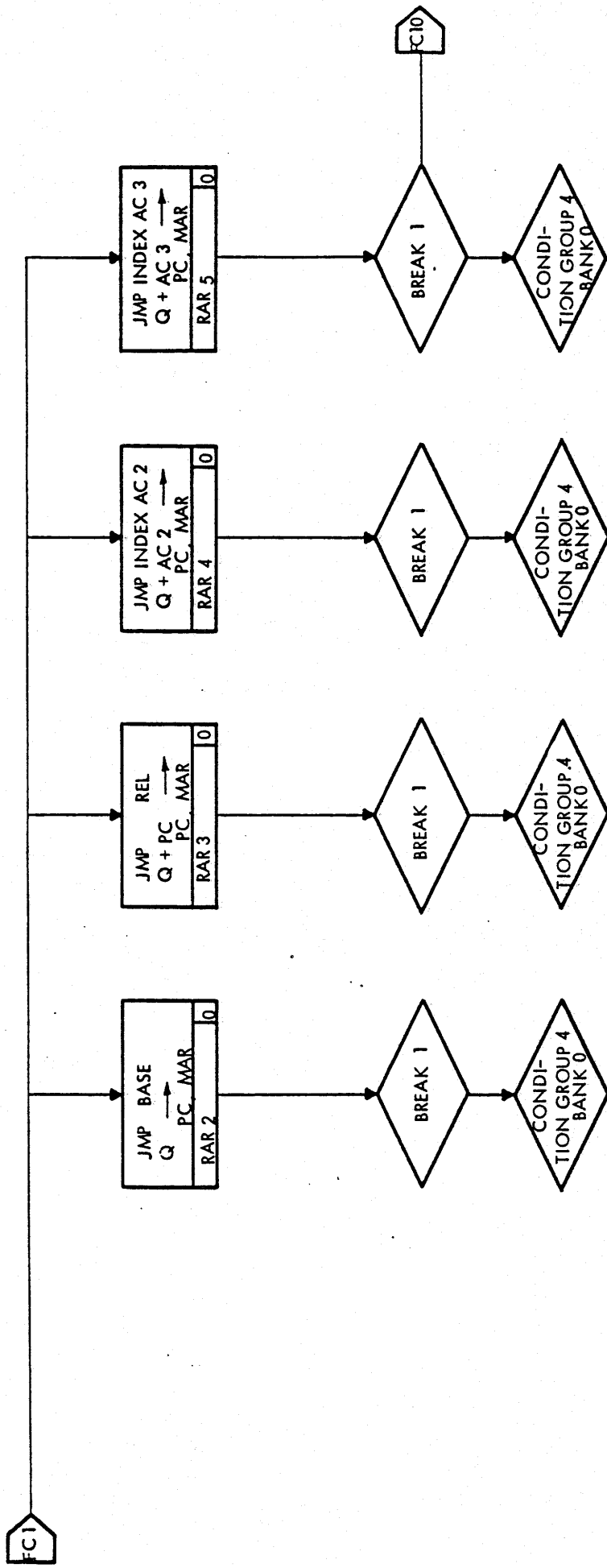


| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS | |
|------------------------|--|---|-----------------|
| 0 | CONDITION GROUP 4 BANK 0 | <ul style="list-style-type: none"> 7 RESTART ADD 7 LD DATA REG 7 LD MAR 7 CLR INTEN 7 TEST MEM | |
| 1 | JUMP TO START ADD | <ul style="list-style-type: none"> 7 LD IR 7 MEM READ 7 LD DATA REG 7 RQENBX 7 FETCH | |
| 130 | CONDITION GROUP 4 BANK 0 | <ul style="list-style-type: none"> 7 BLOCK BIT 0 7 3 STATE EN 7 LD MAR 7 CIN | |
| 210 | DIRECT | <ul style="list-style-type: none"> 7 LD MAR 7 CLR INTEN 7 3 STATE EN 7 TEST MEM | |
| 213 | DIRECT | <ul style="list-style-type: none"> 7 RESTART ADD 7 TEST MEM | |
| | | | |
| Unit CPU 720 | OP FETCH, RESTART, SKIP Signal List | | FC 1 1 of 21 |

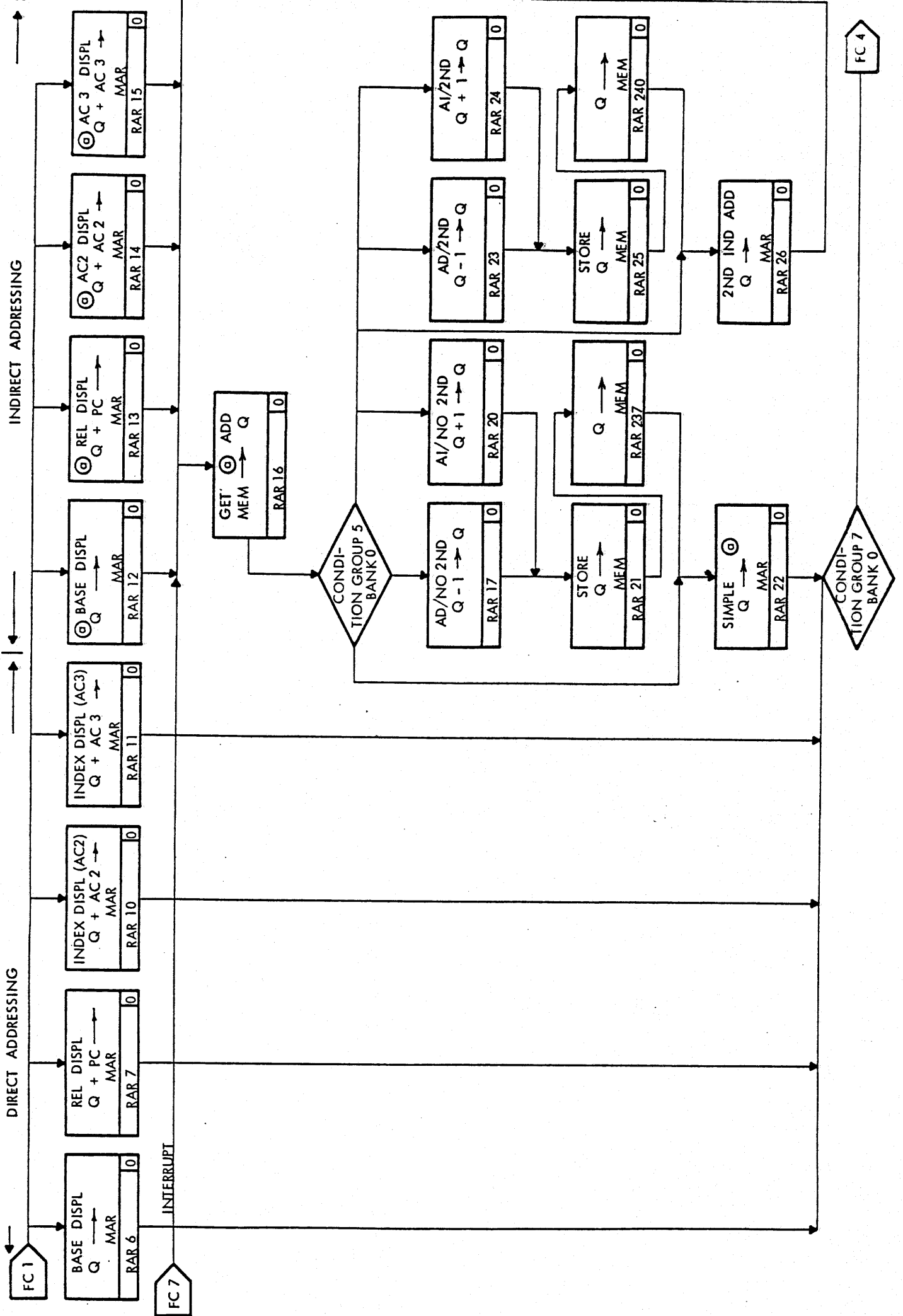


790208 B J 790208 ABP

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|--------------------------------|---|
| 2 | CONDITION GROUP 4 BANK 0 | <ul style="list-style-type: none"> 7 3 STATE EN 7 LD MAR 7 BLOCK BIT 0 |
| 3 | CONDITION GROUP 4 BANK 0 | <ul style="list-style-type: none"> 7 3 STATE EN 7 LD MAR 7 BLOCK BIT 0 |
| 4 | CONDITION GROUP 4 BANK 0 | <ul style="list-style-type: none"> 7 3 STATE EN 7 LD MAR 7 BLOCK BIT 0 |
| 5 | CONDITION GROUP 4 BANK 0 | <ul style="list-style-type: none"> 7 3 STATE EN 7 LD MAR 7 BLOCK BIT 0 |
| | | |

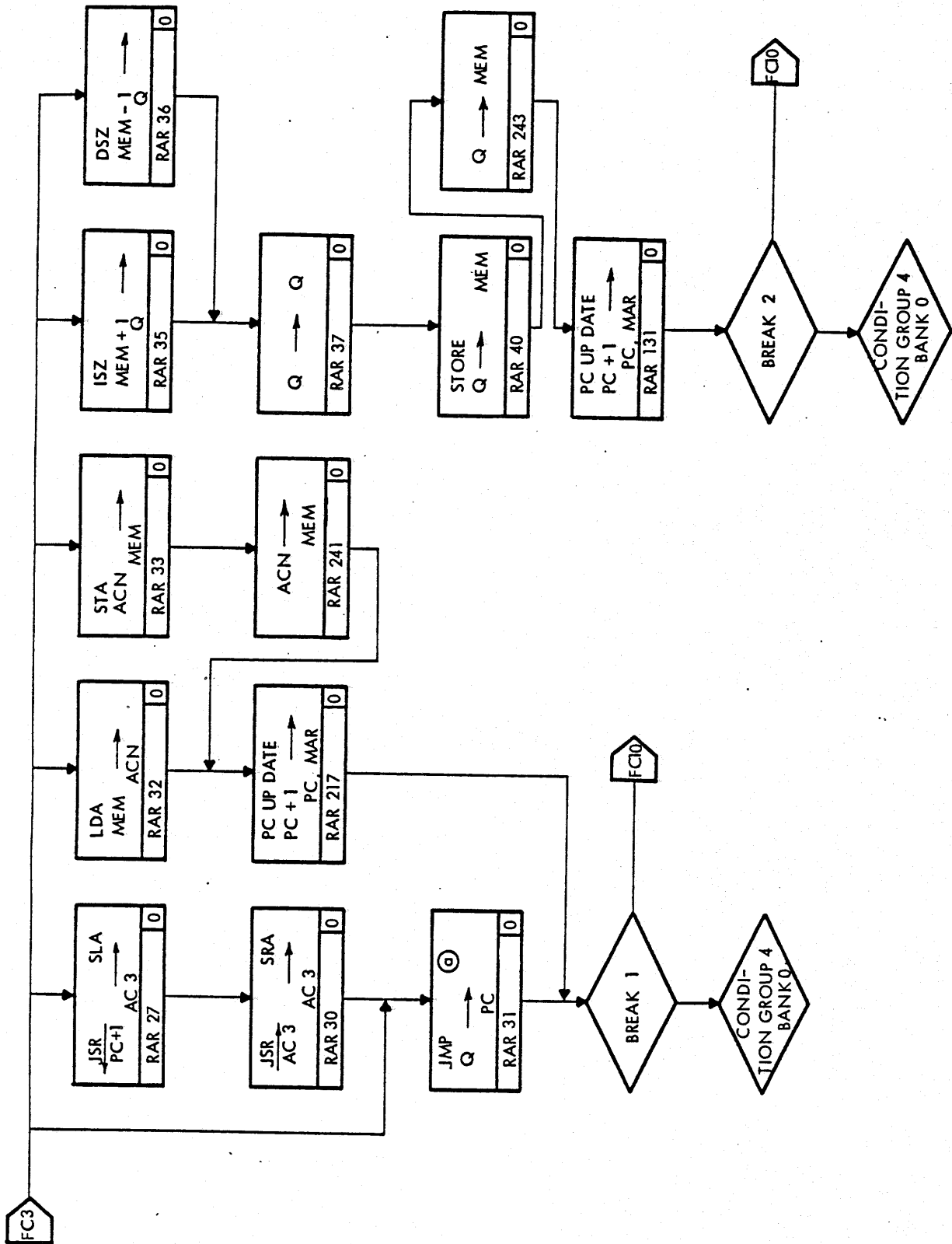


| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|--------------------------------|--|
| 6,7 | CONDITION GROUP 7 BANK 0 | -, TEST MEM -, LD MAR -, BLOCK BIT 0 |
| 10,11 | CONDITION GROUP 7 BANK 0 | -, TEST MEM -, LD MAR |
| 12,13,14,15 | DIRECT | -, LD MAR -, 3 STATE EN -, DEFER -, BLOCK BIT 0 |
| 16 | CONDITION GROUP 5 BANK 0 | -, MEM READ -, LD DATA REG |
| 17,23 | DIRECT | -, LD DATA REG -, 3 STATE EN |
| 20,24 | DIRECT | -, LD DATA REG -, CIN -, 3 STATE EN |
| 21,25, 237, 240 | DIRECT | -, MEM WRITE -, TEST MEM -, LD DATA REG |
| 22 | CONDITION GROUP 7 BANK 0 | -, LD MAR -, 3 STATE EN -, BLOCK BIT 0 |
| 26 | DIRECT | -, 3 STATE EN -, LD MAR -, DEFER -, BLOCK BIT 0 |
| | | |

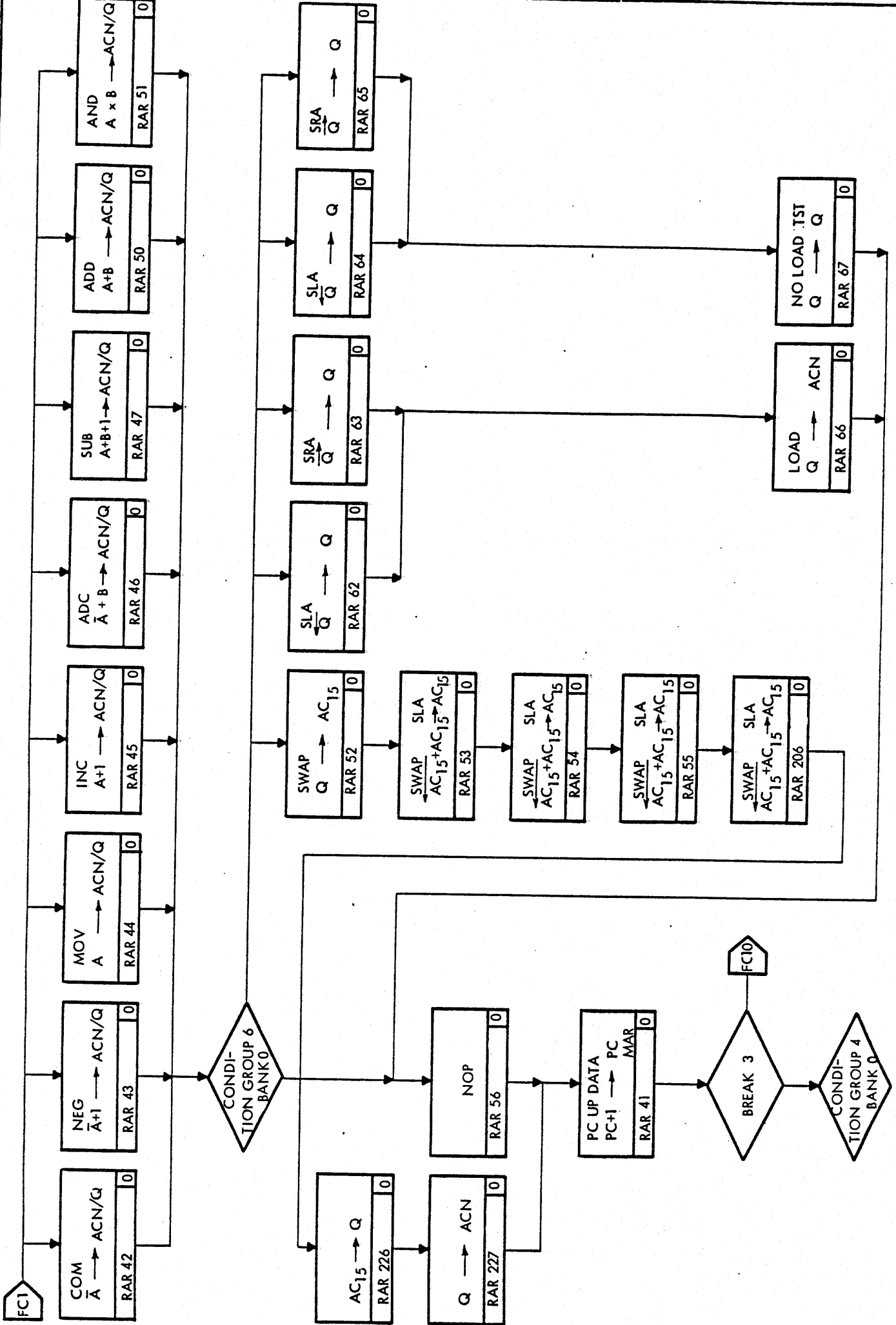


MICROPROGRAM FLOW CHART
MEMORY REFERENCE ADDRESS CALCULATION

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|--------------------------------|---|
| 27 | DIRECT | LD DATA REG CIN 3 STATE EN ALU FLAG CLK |
| 30 | DIRECT | 3 STATE EN LD DATA REG RESET BIT 0 |
| 31 | CONDITION GROUP 4 BANK 0 | LD MAR 3 STATE EN BLOCK BIT 0 |
| 32 | DIRECT | MEM READ GATE ACN LD DATA REG |
| 33, 241 | DIRECT | LD DATA REG MEM WRITE GATE ACN 3 STATE EN |
| 35 | DIRECT | MEM READ CIN ALU= 0 CLK LD DATA REG |
| 36 | DIRECT | LD DATA REG MEM READ ALU= 0 CLK |
| 37 | DIRECT | ALU= 0 CLK TEST MEM LD DATA REG |
| 40, 243 | DIRECT | LD DATA REG MEM WRITE 3 STATE EN SKIP EN |
| 131 | CONDITION GROUP 4 BANK 0 | 3 STATE EN LD MAR CIN BLOCK BIT 0 |
| 217 | CONDITION GROUP 4 BANK 0 | LD DATA REG LD MAR CIN 3 STATE EN BLOCK BIT 0 |



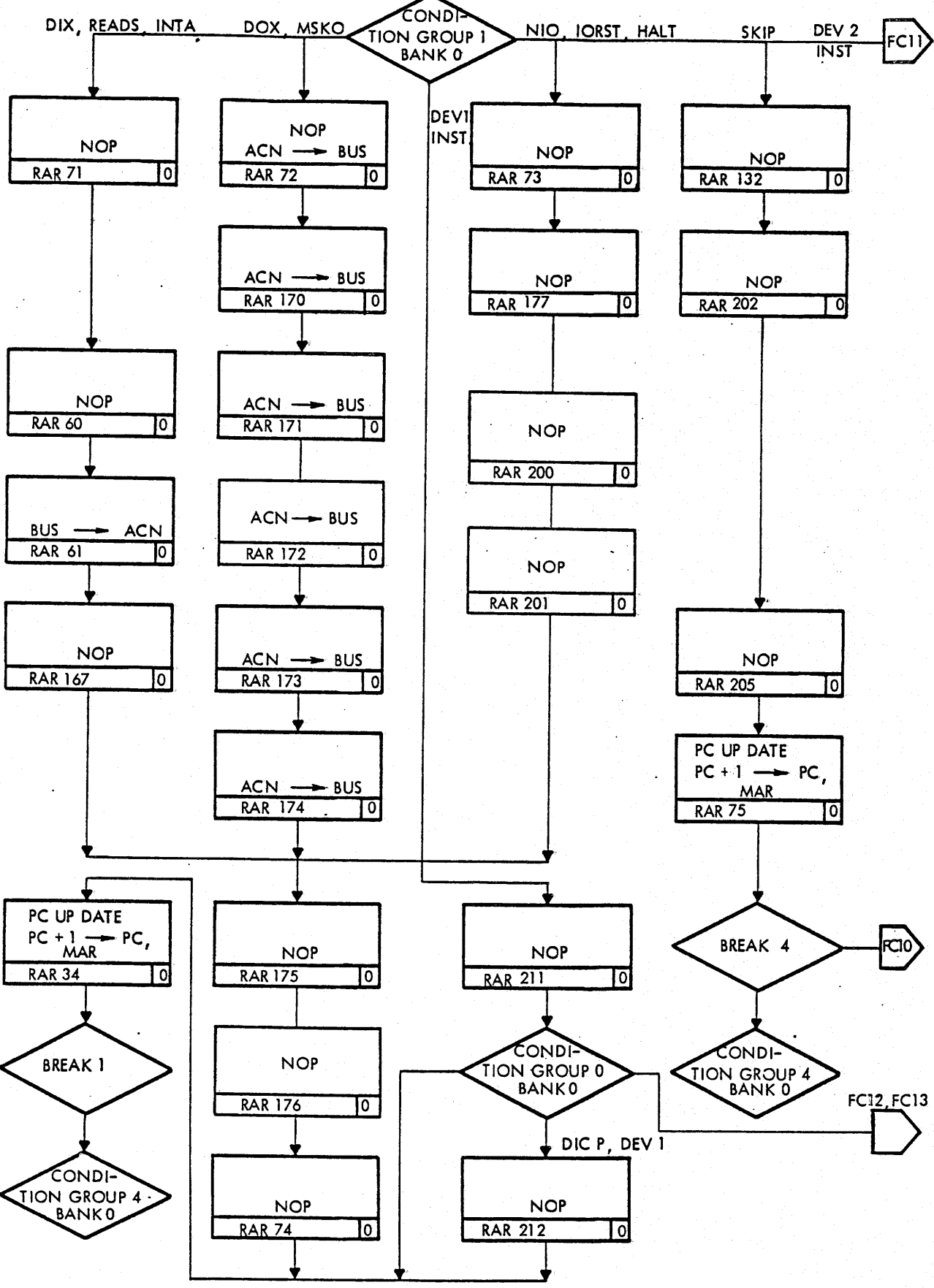
| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS | |
|------------------------|---|--|-----------------|
| 42 51 | CONDITION GROUP 6 BANK 0 | <ul style="list-style-type: none"> - 3 STATE EN - ALU = 0 CLK - ALU FLAG CLK - ALCCON - GATE ACN - LD DATA REG | |
| 43, 45, 47 | CONDITION GROUP 6 BANK 0 | <ul style="list-style-type: none"> - 3 STATE EN - ALU = 0 CLK - ALU FLAG CLK - ALCCON - GATE ACN - COUT EN - CIN - LD DATA REG | |
| 44, 46, 50 | CONDITION GROUP 6 BANK 0 | <ul style="list-style-type: none"> - 3 STATE EN - ALU = 0 CLK - ALU FLAG CLK - ALC CON - GATE ACN - COUT EN - LD DATA REG | |
| 52 | DIRECT | <ul style="list-style-type: none"> - 3 STATE EN - LD DATA REG | |
| 53, 54, 55, 206 | DIRECT | <ul style="list-style-type: none"> - SWAP EN - 3 STATE EN - LD DATA REG | |
| 56 | DIRECT | <ul style="list-style-type: none"> - 3 STATE EN - SKIP EN | |
| 62, 64 | DIRECT | <ul style="list-style-type: none"> - COUT EN - 3 STATE EN - SLA EN - LD DATA REG | |
| 63, 65 | DIRECT | <ul style="list-style-type: none"> - LD DATA REG - SRA EN - 3 STATE EN - COUT EN | |
| 66 | DIRECT | <ul style="list-style-type: none"> - LD DATA REG - GATE ACN - ALU = 0 CLK - 3 STATE EN | |
| 67 | DIRECT | <ul style="list-style-type: none"> - LD DATA REG - 3 STATE EN - ALU = 0 CLK | |
| 226 | DIRECT | <ul style="list-style-type: none"> - COUT EN | |
| 227 | DIRECT | <ul style="list-style-type: none"> - GATE ACN - COUT EN - SKIP EN | |
| 41 | CONDITION GROUP 4 BANK 0 | <ul style="list-style-type: none"> - 3 STATE EN - LD MAR - CIN - CARRY LINK CLK - BLOCK BIT 0 | |
| Unit CPU 720 | ARITHMETIC AND LOGICAL INSTRUCTION Signal List | | FC 5 5 of 21 |
| Dwg. No. A13616 | | | |



| ROM ADDRESS (CCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|------------------------------------|---|
| 34 | CONDITION GROUP 4 BANK 0 | -, I/O SLO -, LD MAR -, CIN -, 3 STATE EN -, BLOCK BIT 0 |
| 60,71 | DIRECT | -, LD DATA REG -, GEN IODT -, GATE IN -, I/O SLO |
| 61 | DIRECT | -, I/O SLO -, GATE ACN -, GEN IODT -, GATE IN -, LD DATA REG |
| 70 | CONDITION GROUP 1 BANK 0 | -, I/O SLO |
| 72 | DIRECT | -, LD DATA REG -, 3 STATE EN -, I/O SLO -, GATE ACN |
| 73 | DIRECT | -, GEN IODT -, I/O SLO |
| 74,175,176 | DIRECT | -, I/O SLO -, GEN IOP |
| 75 | CONDITION GROUP 4 BANK 0 | -, TEST MEM -, 3 STATE EN -, CIN -, LD MAR -, I/O SLO -, BLOCK BIT 0 |
| 132,167,202 | DIRECT | -, I/O SLO |
| 170,174 | DIRECT | -, 3 STATE EN -, GATE OUT -, I/O SLO -, GATE ACN |
| 171,172,173 | DIRECT | -, 3 STATE EN -, GEN IODT -, GATE OUT -, I/O SLO -, GATE ACN |
| 177,200,201 | DIRECT | -, GEN IODT -, I/O SLO |
| 205 | DIRECT | -, SKIP EN -, I/O SLO |
| 211 | CONDITION GROUP 0 BANK 0 | -, I/O SLO |
| 212 | DIRECT | -, I/O SLO -, SET EXTEND |
| | | |

FC1

BRANCH SEL
NOP
RAR 70 0



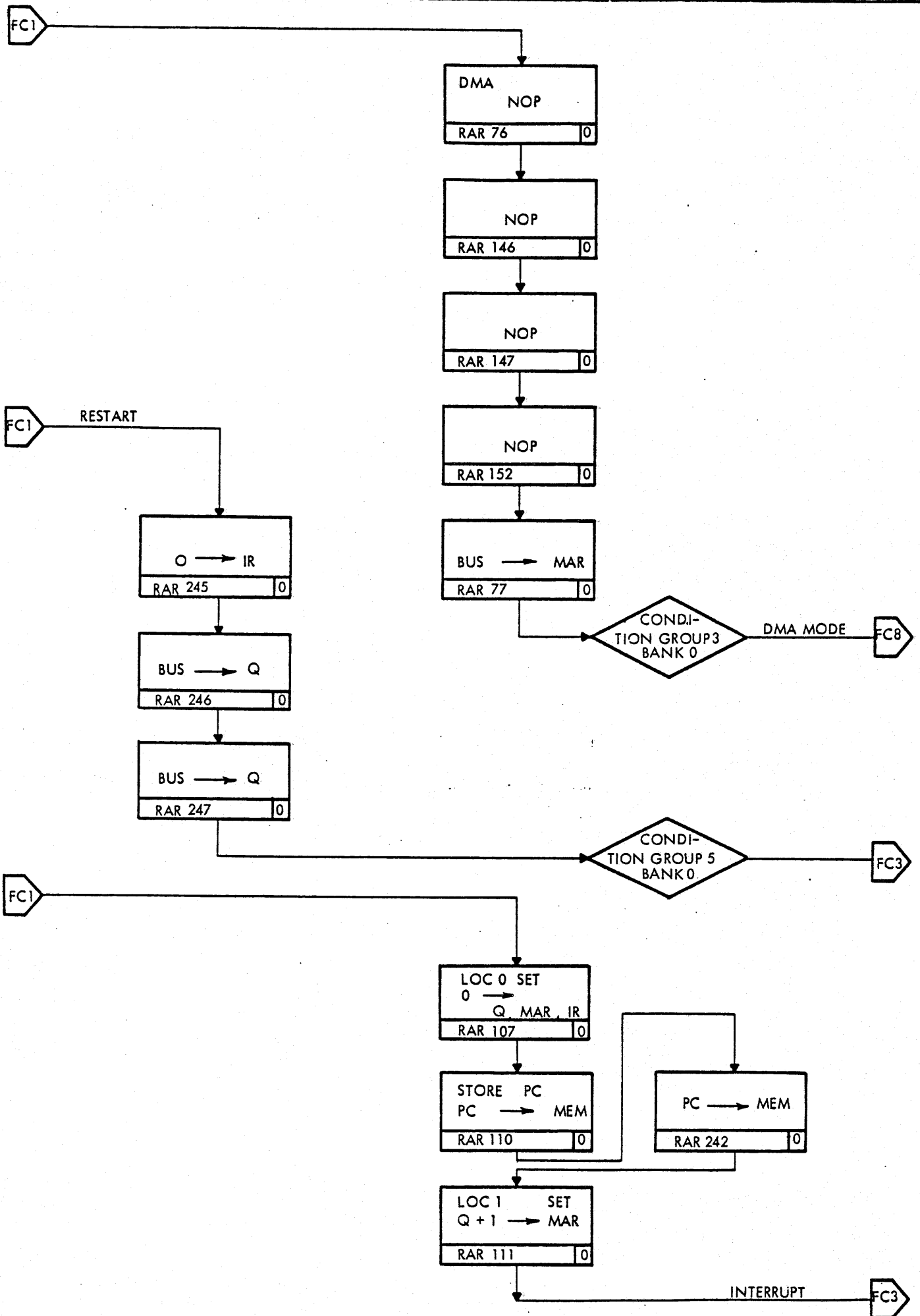
790208 BJ 790208 ABP

| | |
|----------|---------|
| Unit | CPU 720 |
| Dwg. No. | A13673 |

MICROPROGRAM FLOW CHART
 INPUT / OUTPUT INSTRUCTION EXECUTE
 INTERRUPT AND SKIP INSTRUCTION EXECUTE
 Flow Diagram

FC 6

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|------------------------------------|--|
| 76 | DIRECT | - DCHAX |
| 77 | CONDITION GROUP 3 BANK 0 | - LD MAR - DCHAX - GATE IN |
| 107 | DIRECT | - LD MAR - LD IR - CLR INTEN |
| 110, 242 | DIRECT | - LD DATA REG - MEM WRITE - CLR INTEN - 3 STATE EN - BLOCK BIT 0 |
| 111 | DIRECT | - 3 STATE EN - LD MAR - CIN - CLR INTEN |
| 146, 147, 152 | DIRECT | - DCHAX |
| 245 | DIRECT | - LDIR |
| 246 | DIRECT | - RESTART ADD |
| 247 | CONDITION GROUP 5 BANK 0 | - RESTART ADD |
| | | |



790208 BJ 790208 A8P

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| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|------------------------------------|--|
| 100,103 | DIRECT | - LD DATA REG - RQENBX - DCHI |
| 101 | DIRECT | - LD DATA REG - RQENBX - GATE OUT - MEM READ |
| 102 | DIRECT | - TEST MEM - LD DATA REG - RQENBX - MEM READ - CIN - ALU FLAG CLK |
| 104 | DIRECT | - TEST MEM - LD DATA REG - RQENBX - MEM READ - ALU FLAG CLK |
| 105 | DIRECT | - TEST MEM - LD DATA REG - 3 STATE EN - GATE OUT - MEM READ - DCH OFLO EN |
| 106 | CONDITION GROUP 4 BANK 0 | - 3 STATE EN - LD MAR - BLOCK BIT 0 |
| 153,154 164,165 | DIRECT | - DCHI - RQENBX |
| 133, 244 | DIRECT | - LD DATA REG - 3 STATE EN - MEM WRITE |
| 155 | DIRECT | - RQENBX - DCHI - GATE IN |
| 156,157 | DIRECT | - RQENBX - DCHO - GATE OUT - MEM READ |
| 160 | DIRECT | - RQENBX - GATE OUT - MEM READ |
| 161 | DIRECT | - 3 STATE EN - RQENBX - GATE OUT - MEM WRITE |
| 162 | DIRECT | - RQENBX - 3 STATE EN - DCHO - GATE OUT - MEM WRITE |
| 163 | DIRECT | - DCHO - GATE OUT - MEM WRITE - DCH OFLO EN |
| 166 | DIRECT | - TEST MEM - RQENBX - DCHI - GATE IN |
| 215 | DIRECT | - DCH OFLO EN |

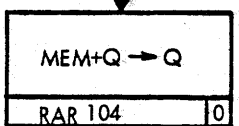
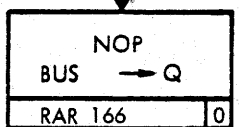
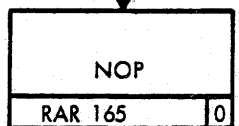
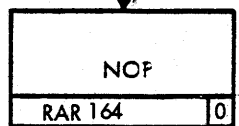
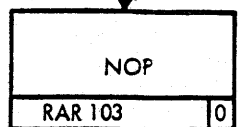
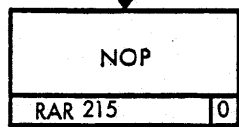
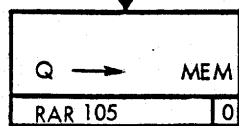
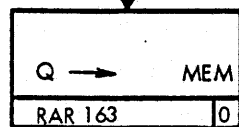
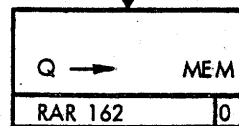
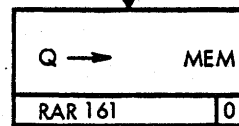
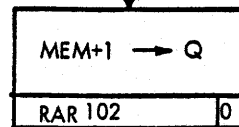
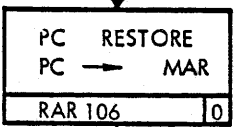
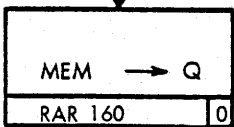
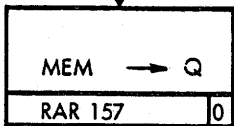
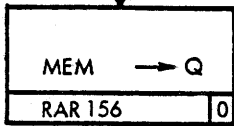
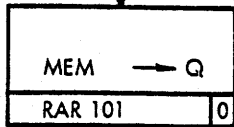
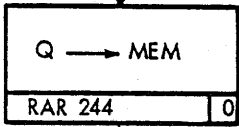
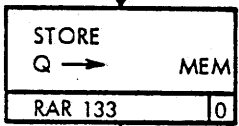
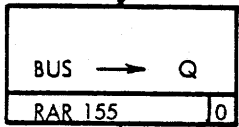
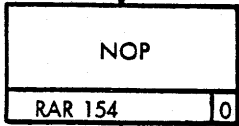
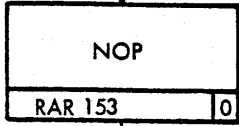
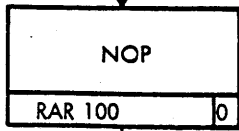
FC7

DMA IN

DMA OUT

DMA INCR

DMA ADD TO MEM



790209 BJ 790209 ASF

Unit CPU 720

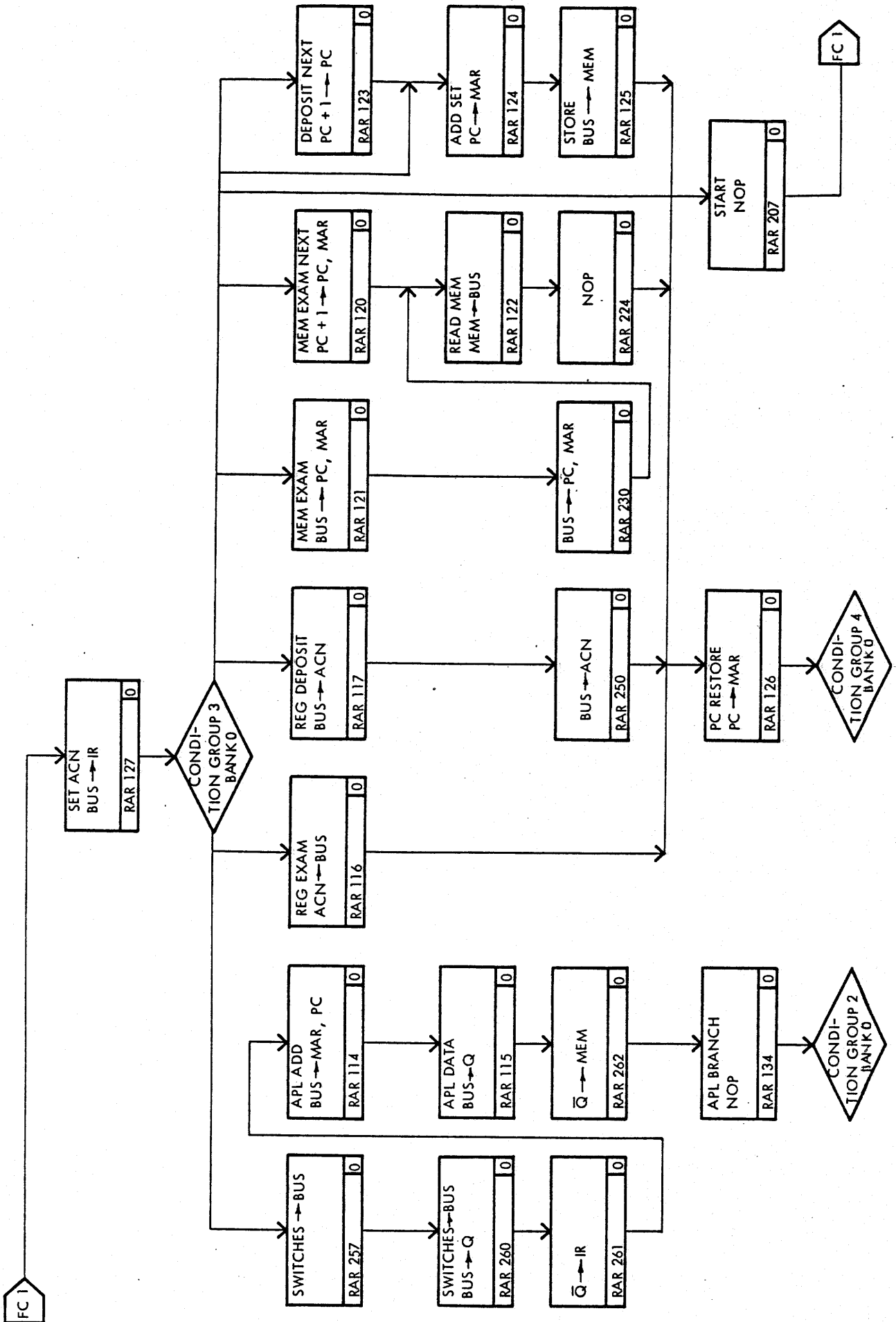
Dwa No. A13675

MICROPROGRAM FLOW DIAGRAM
DMA CHANNEL EXECUTE

Flow Diagram

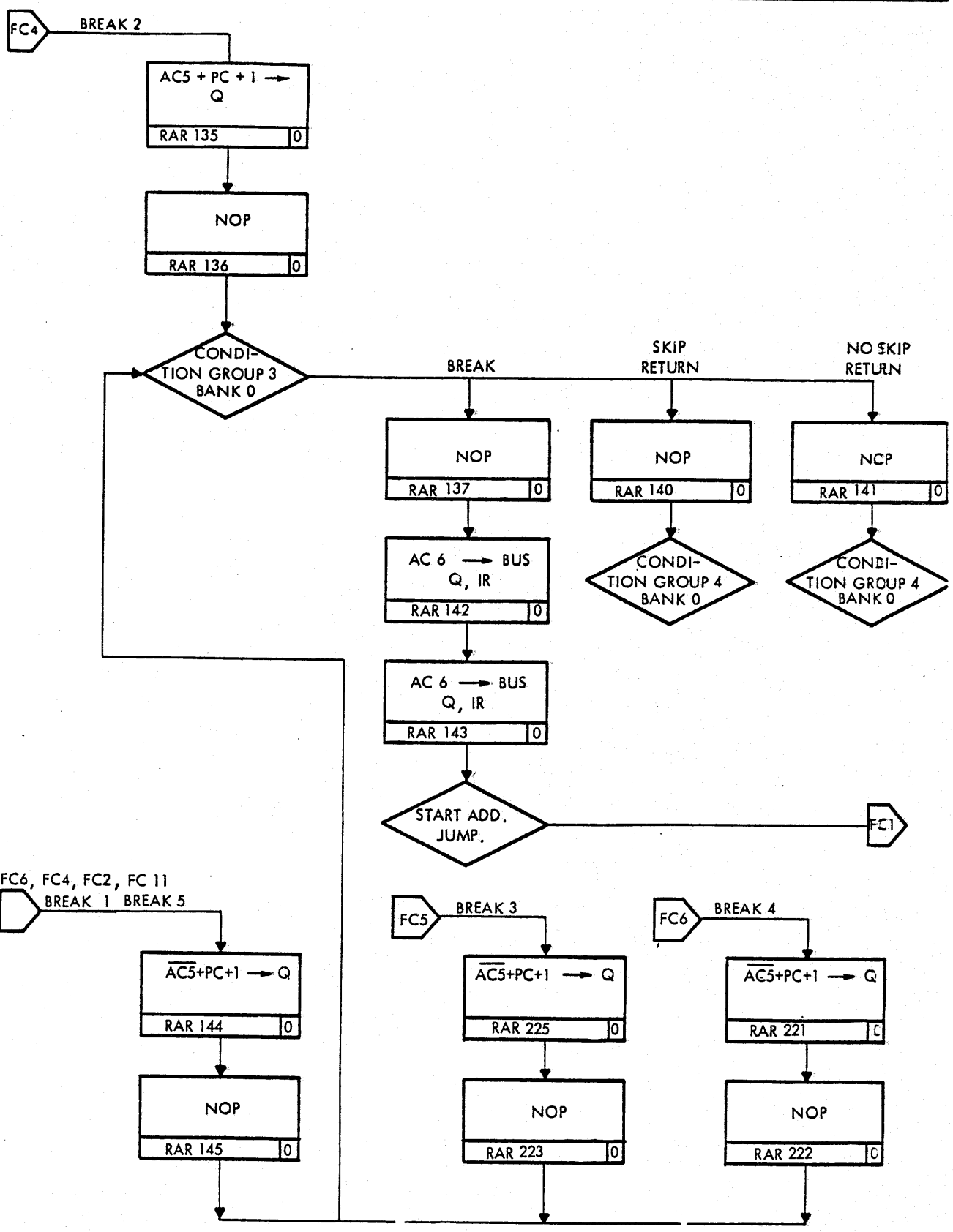
FC 8

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|--------------------------------|---|
| 114 | DIRECT | - TEST MEM - LD MAR - GATE APL ADD |
| 115 | DIRECT | - GATE APL DATA - LD DATA REG |
| 116 | DIRECT | - FPOP END - LD DATA REG - PAN ACN - GATE ACN - 3 STATE EN |
| 117, 250 | DIRECT | - PAN ACN EN - GATE ACN - GATE DATA SW - FPOP END - LD DATA REG |
| 120 | DIRECT | - TEST MEM - LD MAR - CIN - 3 STATE EN |
| 121, 230 | DIRECT | - LD MAR - TEST MEM - GATE DATA SW |
| 122 | DIRECT | - FPOP END - LD DATA REG - TEST MEM - MEM READ |
| 123 | DIRECT | - 3 STATE EN - CIN - LD DATA REG |
| 124 | DIRECT | - TEST MEM - LD MAR - 3 STATE EN - BLOCK BIT 0 |
| 125 | DIRECT | - MEM WRITE - TEST MEM - GATE DATA SW - FPOP EN - LD DATA REG |
| 126 | CONDITION GROUP 4 BANK 0 | - TEST MEM - LD MAR - 3 STATE EN |
| 127 | CONDITION GROUP 2 BANK 0 | - LD IR - GATE REG EN |
| 134 | CONDITION GROUP 2 BANK 0 | - CIN |
| 207 | DIRECT | - RESTART ADD |
| 224 | DIRECT | |
| 257, 260 | DIRECT | - GATE DATA SW |
| 261 | DIRECT | - LD IR - LD DATA REG |
| 262 | DIRECT | - TEST MEM - MEM WRITE - LD DATA REG |



MICROPROGRAM FLOW CHART
FRONT PANEL OPERATIONS
Flow Diagram

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS | |
|------------------------|-----------------------------------|---|-------------------|
| 135 | DIRECT | EN BREAK -, 3 STATE EN -, SKIP EN -, CIN | |
| 136 | CONDITION GROUP 3 BANK 0 | -, SKIP EN EN BREAK | |
| 137 | DIRECT | -, 3 STATE EN -, CIN | |
| 140 | CONDITION GROUP 4 BANK 0 | | |
| 141 | CONDITION GROUP 4 BANK 0 | | |
| 142 | DIRECT | -, 3 STATE EN -, FETCH -, LD IR -, LD DATA REG | |
| 143 | JUMP TO START ADD | -, 3 STATE EN -, FETCH -, LD IR -, LD DATA REG | |
| 144 | DIRECT | -, 3 STATE EN -, CIN EN BREAK | |
| 145 | DIRECT | EN BREAK | |
| 221 | DIRECT | EN BREAK -, 3 STATE EN -, SKIP EN -, I/O SLO -, CIN | |
| 222 | CONDITION GROUP 3 BANK 0 | -, SKIP EN -, I/O SLO EN BREAK | |
| 223 | CONDITION GROUP 3 BANK 0 | EN BREAK -, SKIP EN -, CARRY LINK CLK | |
| 225 | DIRECT | -, 3 STATE EN -, SKIP EN -, CIN -, CARRY LINK CLK | |
| | | | |
| Unit CPU 720 | BREAK TEST EXECUTE Signal List | | FC 10 10 of 21 |
| Dwg. No. A13620 | | | |



790209 BJ 790209 ABP

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| Unit | CPU 720 |
| Dwg. No. | A13677 |

MICROPROGRAM FLOWCHART
BREAK TEST EXECUTE
Flow Diagram

FC 10

A/S REGN CENTRALEN

Designed by

Drawn by

Dwg. Office Check

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|--------------------------------|---|
| 1 | DIRECT | 7 LD DATA REG 7 ENABLE CONSTANT |
| 2 | CONDITION GROUP 2 BANK 1 | 7 LD DATA REG 7 3 STATE EN 7 ALC CON |
| 3 | CONDITION GROUP 4 BANK 0 | 7 LD DATA REG 7 3 STATE EN 7 LD MAR 7 C IN |
| 256 | CONDITION GROUP 0 BANK 1 | |
| 377 | DIRECT | 7 3 STATE EN 7 LD MAR 7 C IN |
| | | |

Unit
CPU 720

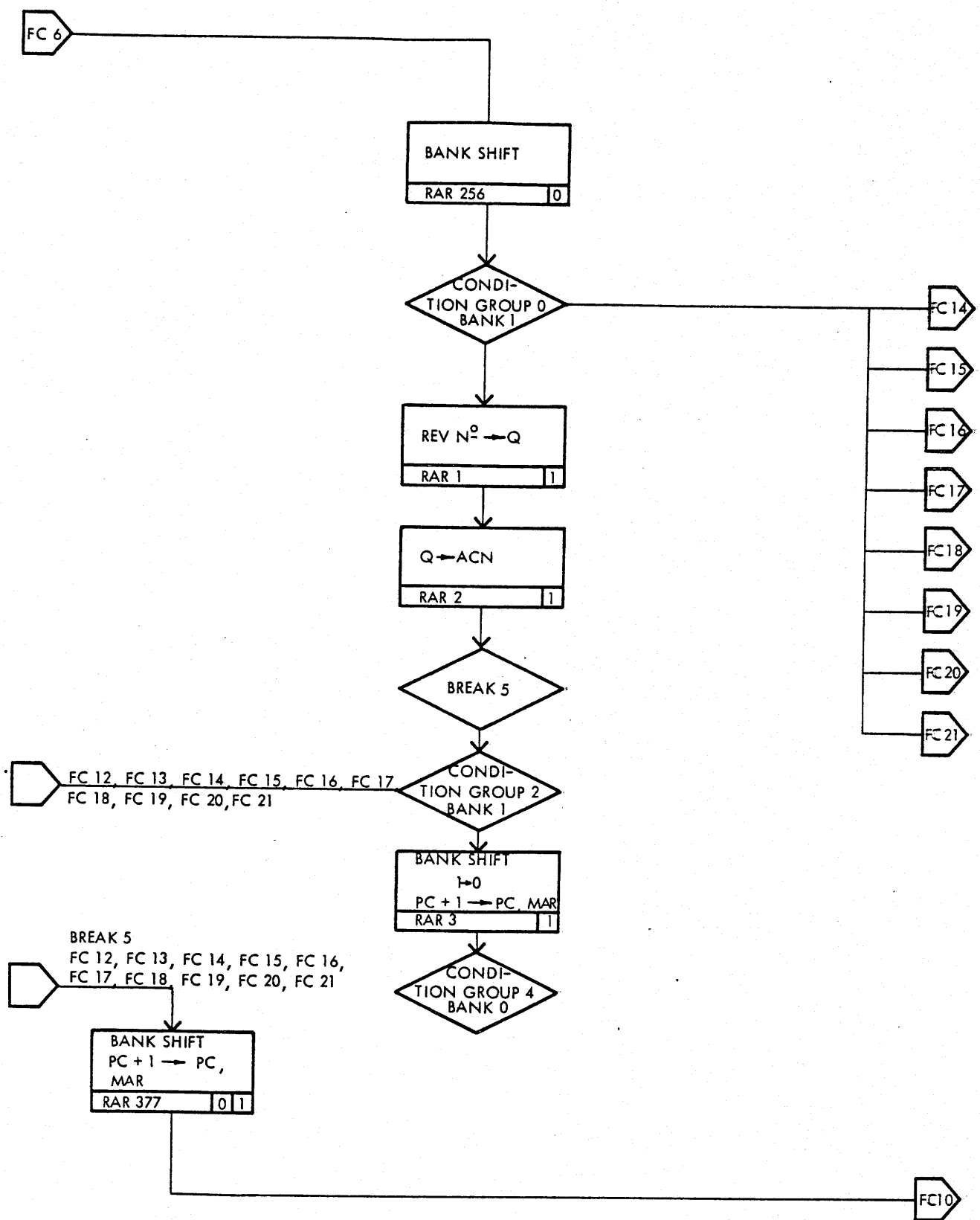
CPU IDENTIFY

FC 11

Dwg. No.
A25627

Signal List

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790202 BJ 790202 ABP

A/S REGNECENTRALEN

Designed by

Drawn by

Dwg. Office Check

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|-----------------------------------|---|
| 42 | DIRECT | ; RESET BIT 0 |
| 43, 46, 47 | DIRECT | ; ENABLE CONSTANT |
| 44 | DIRECT | ; LD DATA REG ; 3 STATE EN ; LD MAR |
| 45 | DIRECT | ; RQEN BX ; MEM READ |
| 50 | DIRECT | ; LD DATA REG COND SEL 0 COND SEL 1 ; 3 STATE EN ; LD MAR |
| 51 | DIRECT | ; LD DATA REG ; 3 STATE EN |
| 52, 53, 54 | DIRECT | ; LD DATA REG ; 3 STATE EN SWAP EN |
| 55 | DIRECT | ; LD DATA REG ; 3 STATE EN SWAP EN COND SEL 0 |
| 56, 57 | CONDITION GROUP 6, 2 BANK 1 | |
| 60 | DIRECT | ; LD DATA REG ; 3 STATE EN COND SEL 0 |
| 375 | DIRECT | ; 3 STATE EN ; ALU FLAG CLK |
| | | |

Unit
CPU 720

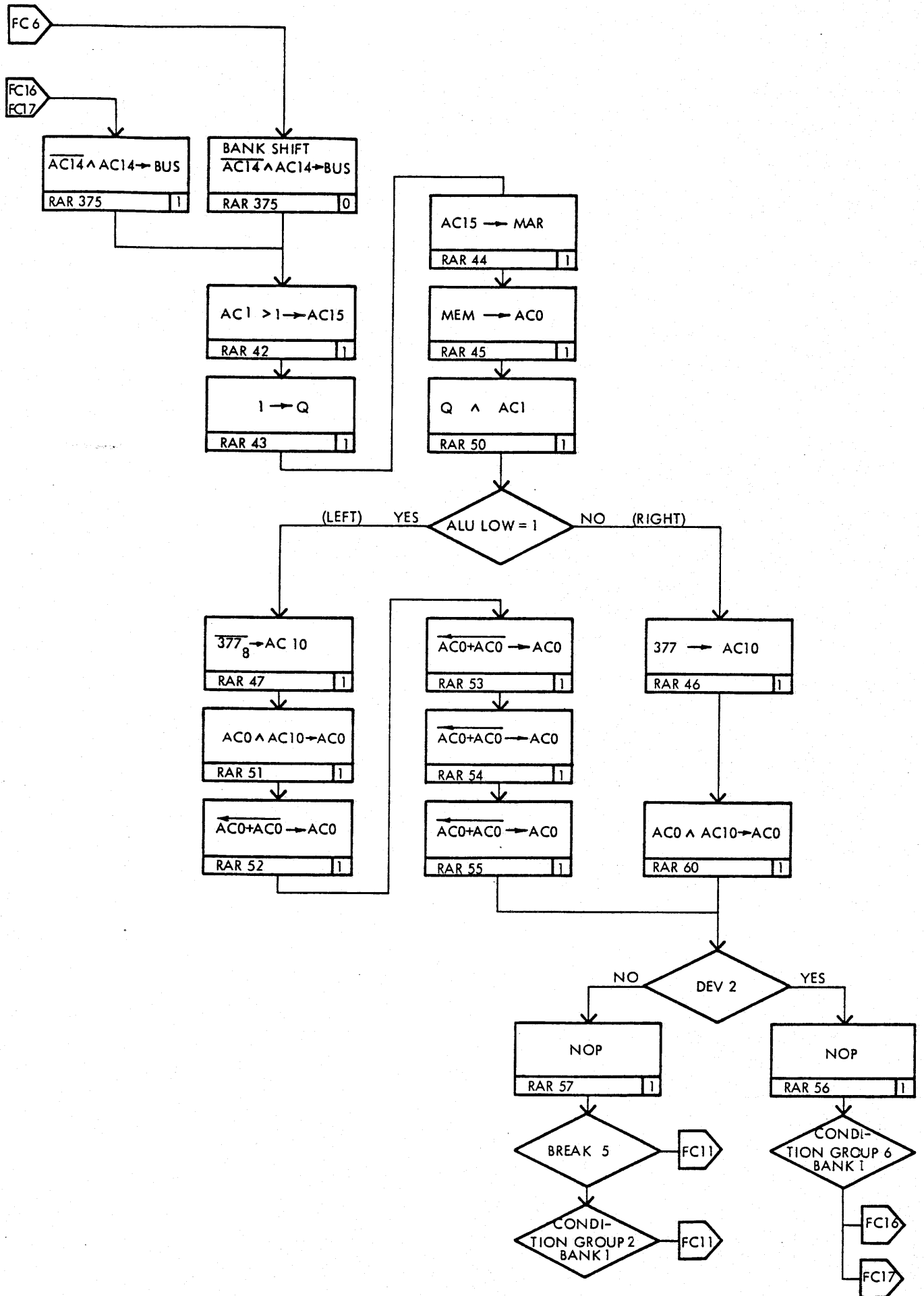
Dwg. No.
A25628

LOAD BYTE

Signal List

FC 12

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790205 ABP

790205 BJ

A/S REGNENCENTRALEN

Designed by

Drawn by

Dwg. Office Check

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|--------------------------------|---|
| 16 | DIRECT | 7 RESET BIT 0 |
| 17, 24, 25 | DIRECT | 7 ENABLE CONSTANT |
| 20 | DIRECT | 7 LD DATA REG 7 3 STATE EN 7 LD MAR |
| 21 | DIRECT | 7 LD DATA REG 7 MEM READ |
| 22 | DIRECT | 7 LD DATA REG COND SEL 0 COND SEL 1 7 3 STATE EN |
| 23 | DIRECT | 7 LD DATA REG |
| 26 | DIRECT | 7 LD DATA REG 7 3 STATE EN |
| 27, 30, 31, 32 | DIRECT | 7 LD DATA REG 7 3 STATE EN SWAP EN |
| 33, 34, 35, 363 | DIRECT | |
| 36 | DIRECT | COND SEL 1 |
| 37 | CONDITION GROUP 2 BANK 1 | |
| 41 | DIRECT | 7 LD DATA REG 7 3 STATE EN 7 RQEN BX 7 MEM WRITE COND SEL 0 7 TEST MEM |
| 376 | DIRECT | 7 3 STATE EN 7 ALU FLAG CLK |
| | | |

Unit
CPU 720

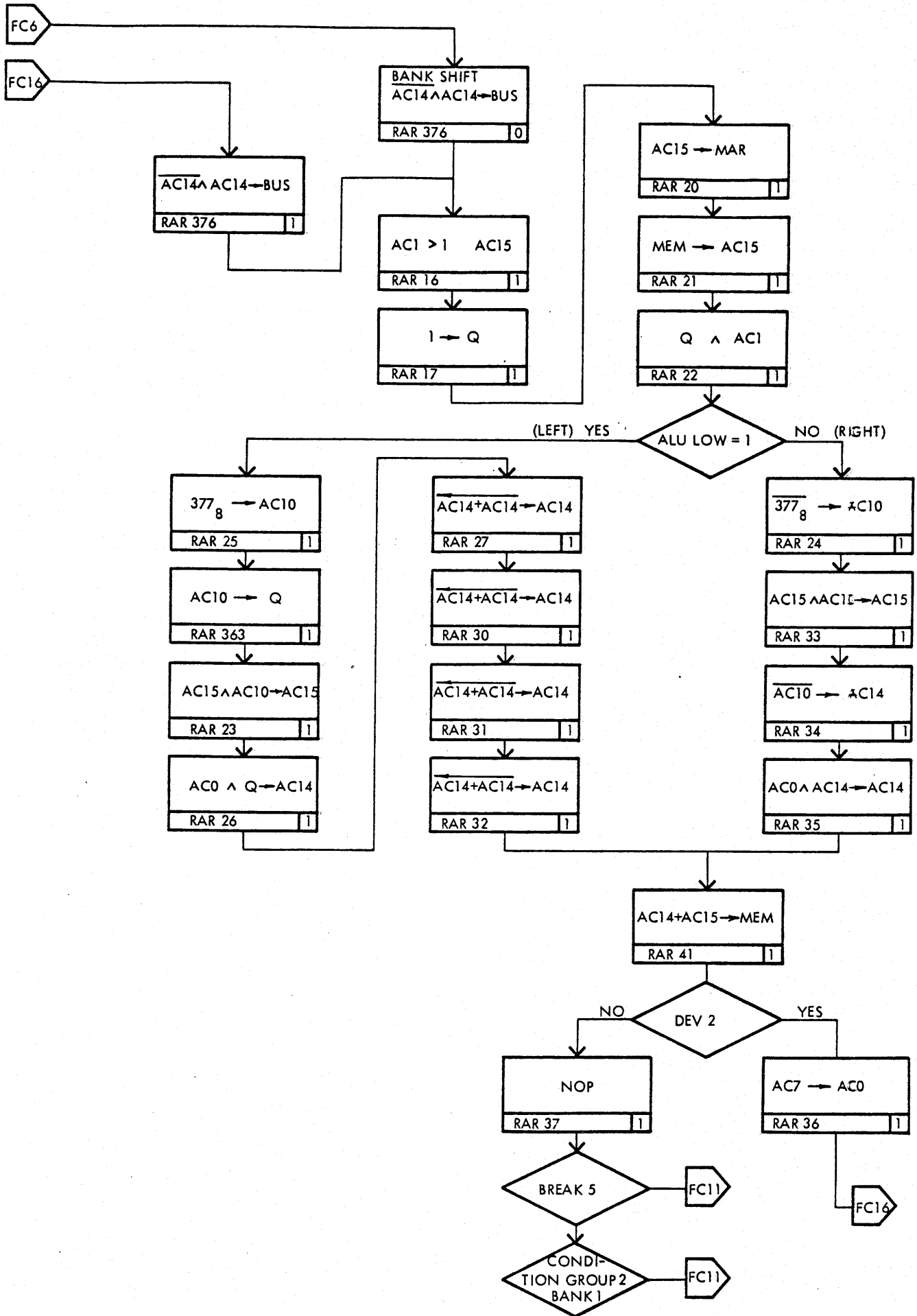
Dwg. No.
A25629

STORE BYTE

Signal List

FC 13

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790205 BJ 790205 ABP

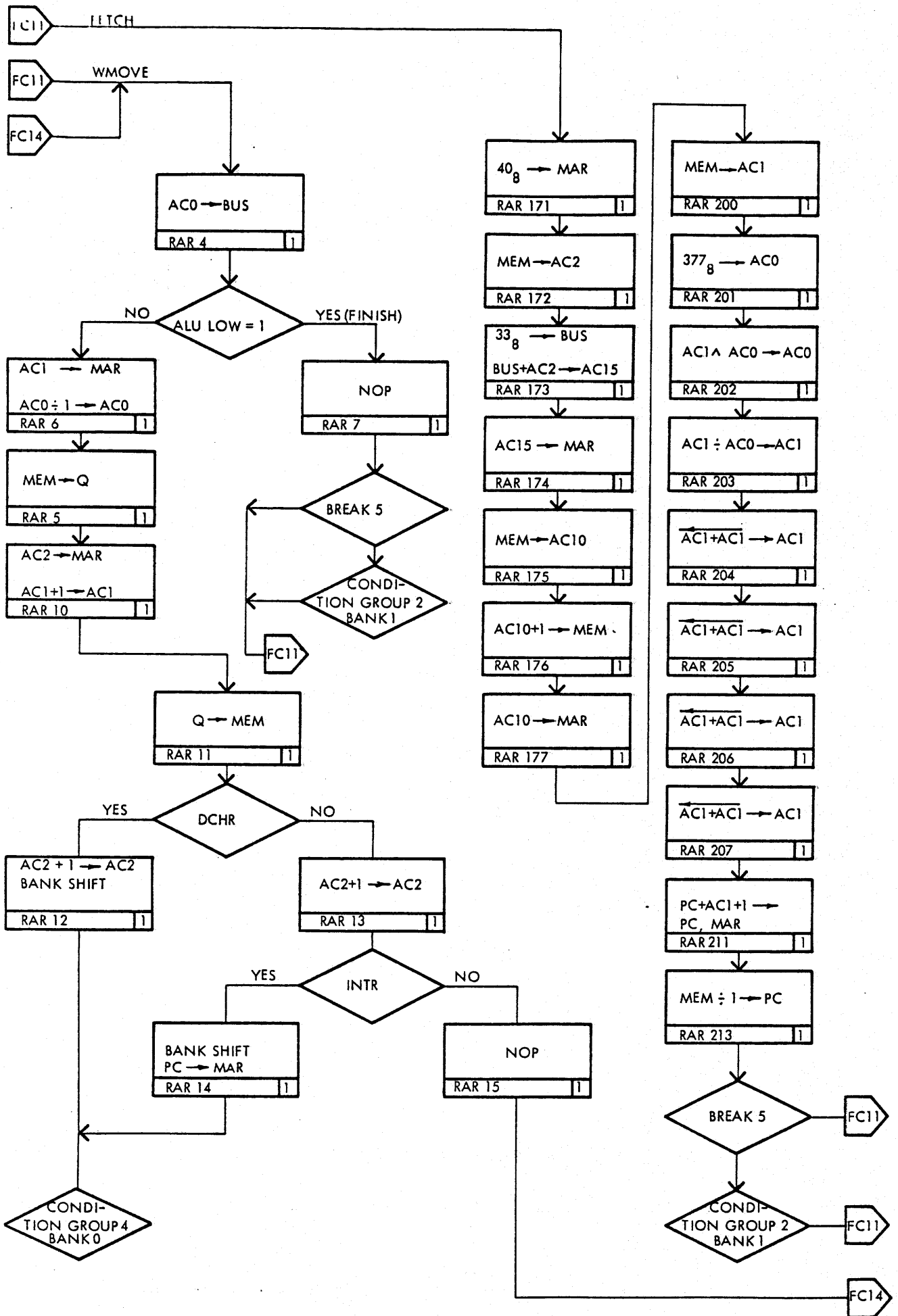
| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|--------------------------------|--|
| 4 | DIRECT | 7 LD DATA REG COND SEL 0 COND SEL 1 7 3 STATE EN 7 LD MAR |
| 5 | DIRECT | 7 MEM READ |
| 6 | DIRECT | 7 LD DATA REG 7 3 STATE EN 7 LD MAR |
| 7 | CONDITION GROUP 2 BANK 1 | |
| 10 | DIRECT | 7 LD DATA REG 7 3 STATE EN 7 RQEN BX 7 LD MAR 7 C IN |
| 11 | DIRECT | 7 LD DATA REG COND SEL 1 7 3 STATE EN 7 MEM WRITE 7 TEST MEM |
| 12 | CONDITION GROUP 4 BANK 0 | 7 C IN |
| 13 | DIRECT | COND SEL 2 7 C IN |
| 14 | CONDITION GROUP 4 BANK 0 | 7 3 STATE EN 7 LD MAR |
| 15, 202 | DIRECT | |
| 171 | DIRECT | 7 LD MAR 7 ENABLE CONSTANT |
| 172, 175, 200 | DIRECT | 7 LD DATA REG 7 MEM READ |
| 173, 201 | DIRECT | 7 ENABLE CONSTANT |
| 174, 177 | DIRECT | 7 3 STATE EN 7 LD MAR |
| 176 | DIRECT | 7 3 STATE EN 7 MEM WRITE 7 TEST MEM 7 C IN |
| 203 | DIRECT | 7 C IN |
| 204, 205, 206, 207 | DIRECT | SWAP EN |
| 211 | DIRECT | 7 3 STATE EN 7 RQEN BX 7 LD MAR 7 C IN |
| 213 | CONDITION GROUP 2 BANK 1 | 7 LD DATA REG 7 MEM READ |

A/S REGN...
 NTRALEN
 Designed by
 Drawn by
 Dwg. Office Check

Unit CPU 720
Dwg. No. A13621

WORD MOVE, MUSIL FETCH
Signal List

FC 14
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790205 ABP
790205 BJ

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|--------------------------------|---|
| 120, 122 | DIRECT | , ENABLE CONSTANT |
| 121 | DIRECT | , LD DATA REG , 3 STATE EN , LD MAR |
| 123, 147 | DIRECT | , RQEN BX , LD MAR , ENABLE CONSTANT |
| 124 | DIRECT | , LD DATA REG COND SEL 0 COND SEL 1 , MEM READ |
| 125, 127 | DIRECT | , 3 STATE EN , LD MAR |
| 126, 134, 142 | DIRECT | , LD DATA REG , MEM READ |
| 130, 136, 144 | DIRECT | , LD DATA REG , RQEN BX , MEM READ |
| 131, 137, 145 | DIRECT | , 3 STATE EN COND SEL 0 COND SEL 1 |
| 132, 140, 146 | DIRECT | , 3 STATE EN COND SEL 1 |
| 133, 135, 141, 143 | DIRECT | , 3 STATE EN , LD MAR , C IN |
| 150 | CONDITION GROUP 4 BANK 0 | |
| 151 | DIRECT | COND SEL 2 |
| 152 | CONDITION GROUP 4 BANK 0 | , 3 STATE EN , LD MAR |
| 153 | DIRECT | |
| 154 | CONDITION GROUP 2 BANK 1 | , LD DATA REG , MEM READ |
| | | |

A/S REGNENCENTRALEN

Designed by

Drawn by

Dwg. Office Check

Unit CPU 720

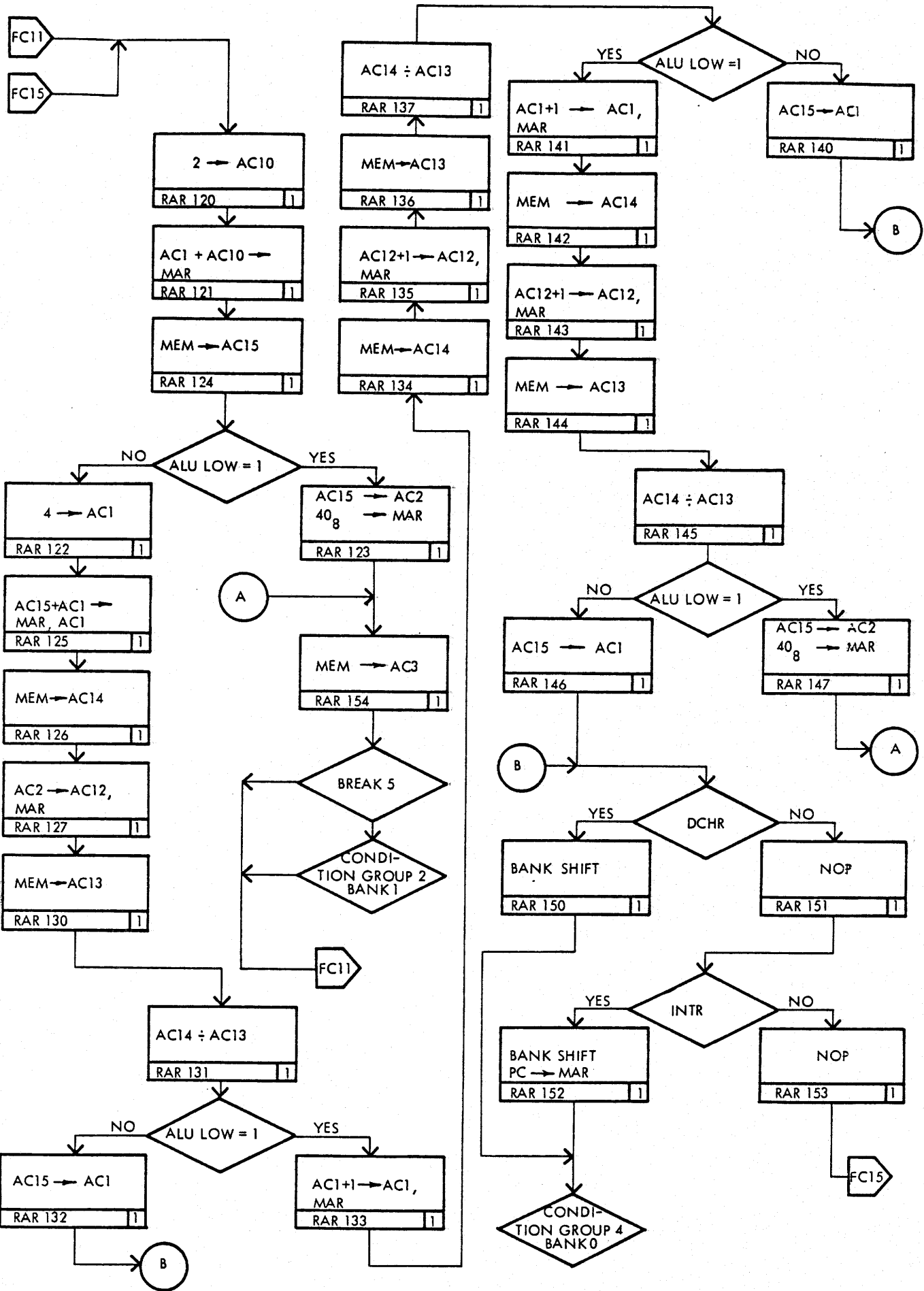
Dwg. No. A25630

SEARCH ITEM

Signal List

FC 15

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790206 ABP
790206 BJ

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|--------------------------------|---|
| 100 | DIRECT | 7 LD DATA REG COND SEL 0 COND SEL 1 7 3 STATE EN 7 RQEN BX 7 LD MAR 7 ALU = 0 CLK |
| 101, 117 | DIRECT | 7 LD DATA REG 7 3 STATE EN 7 C IN |
| 102, 111, 115, 345 | DIRECT | |
| 103 | CONDITION GROUP 2 BANK 1 | |
| 104, 110 | DIRECT | 7 LD DATA REG 7 3 STATE EN |
| 112 | CONDITION GROUP 4 BANK 0 | |
| 113 | DIRECT | COND SEL 2 |
| 114 | CONDITION GROUP 4 BANK 0 | 7 3 STATE EN 7 LD MAR |
| 116 | DIRECT | 7 3 STATE EN 7 C IN 7 ALU = 0 CLK COND SEL 1 |
| 212 | DIRECT | COND SEL 0 COND SEL 1 7 LD MAR |
| 344 | DIRECT | 7 C IN |
| 346 | CONDITION GROUP 4 BANK 0 | |
| | | |

A/S REGNECENTRALEN

Designed by

Drawn by

Dwg. Office Check

Unit
CPU 720

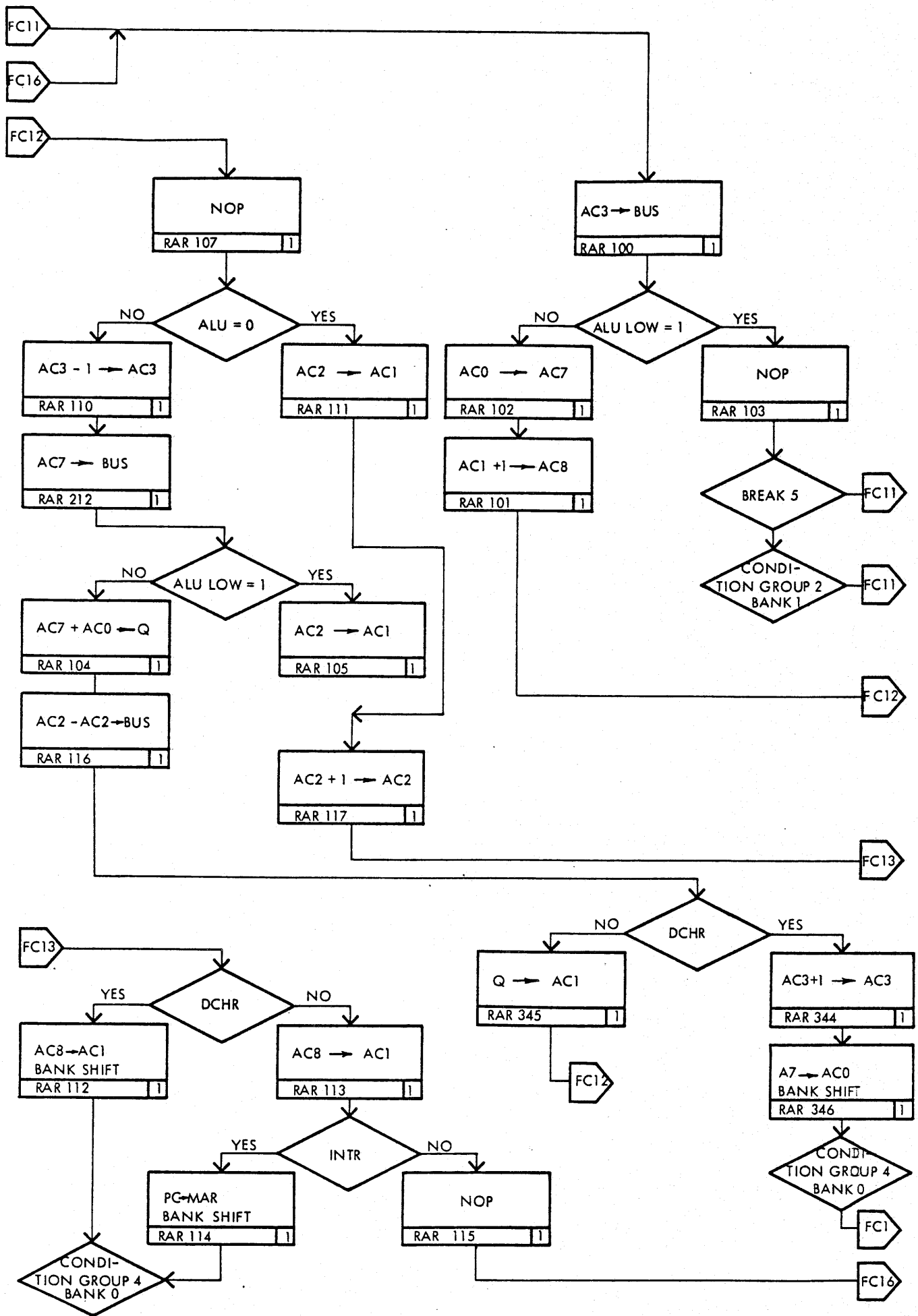
Dwg. No.
A25631

BYTE MOVE

Signal List

FC 16

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790206 ABP
790206 BJ

A/S REGCENTRALEN

Designed by

Drawn by

Dwg. Office Check

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|--------------------------------|---|
| 61 | DIRECT | 7 LD DATA REG COND SEL 0 COND SEL 1 7 3 STATE EN 7 RQEN BX 7 LD MAR 7 ALU = 0 CLK |
| 62 | DIRECT | 7 C IN |
| 63 | CONDITION GROUP 2 BANK 1 | |
| 64 | DIRECT | 7 3 STATE EN 7 C IN 7 ALU = 0 CLK |
| 65 | DIRECT | 7 LD DATA REG 7 3 STATE EN 7 C IN |
| 66, 67, 77 | DIRECT | |
| 70 | DIRECT | COND SEL 1 COND SEL 2 7 LD MAR |
| 71 | DIRECT | COND SEL 0 COND SEL 1 7 LD MAR 7 C IN |
| 72 | CONDITION GROUP 2 BANK 1 | 7 LD DATA REG 7 3 STATE EN |
| 73 | DIRECT | COND SEL 1 |
| 74 | CONDITION GROUP 4 BANK 0 | |
| 75 | DIRECT | COND SEL 2 |
| 76 | CONDITION GROUP 4 BANK 0 | 7 3 STATE EN 7 LD MAR |

Unit
CPU 720

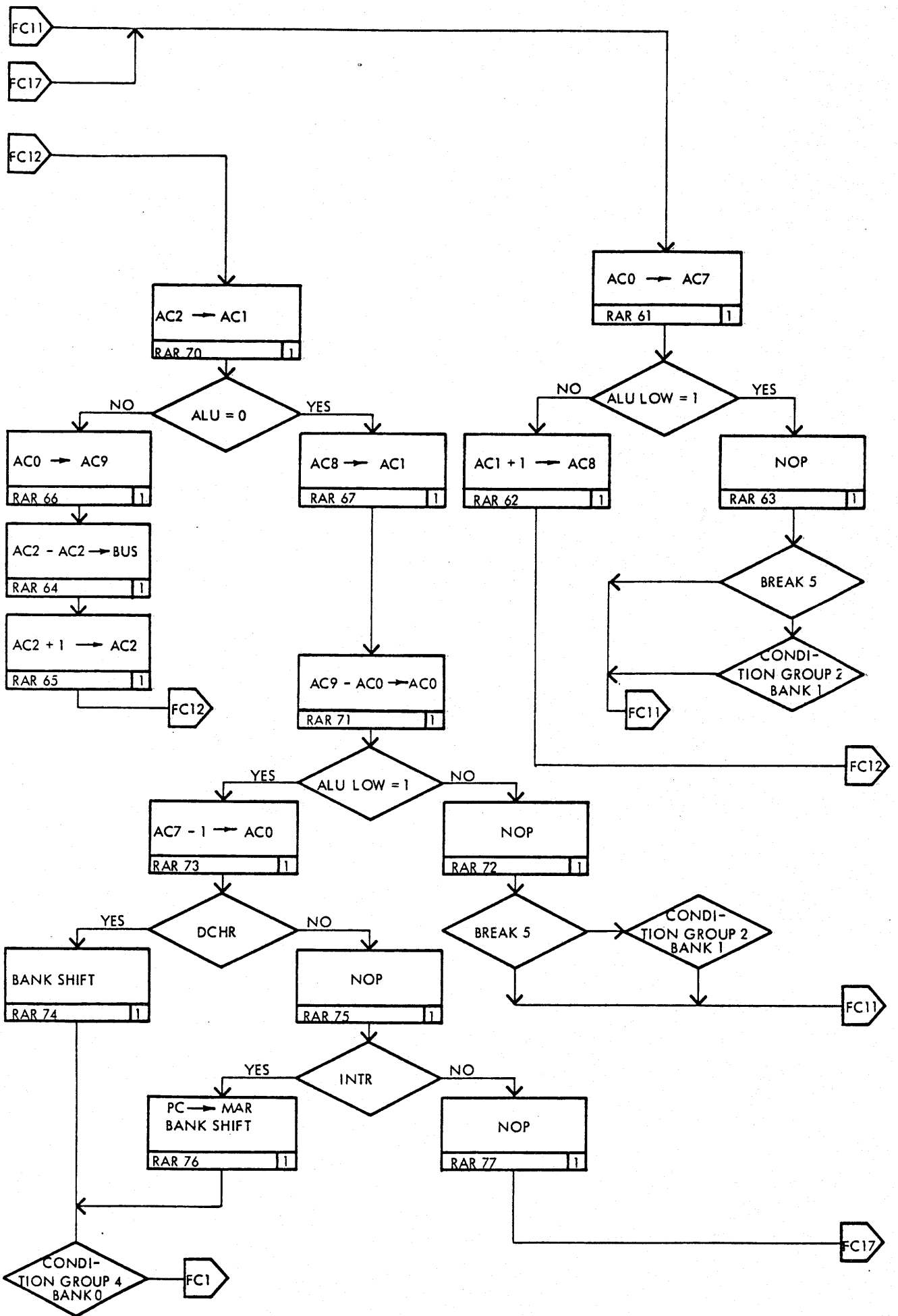
BYTE COMPARE

FC 17

Dwg. No.
A25632

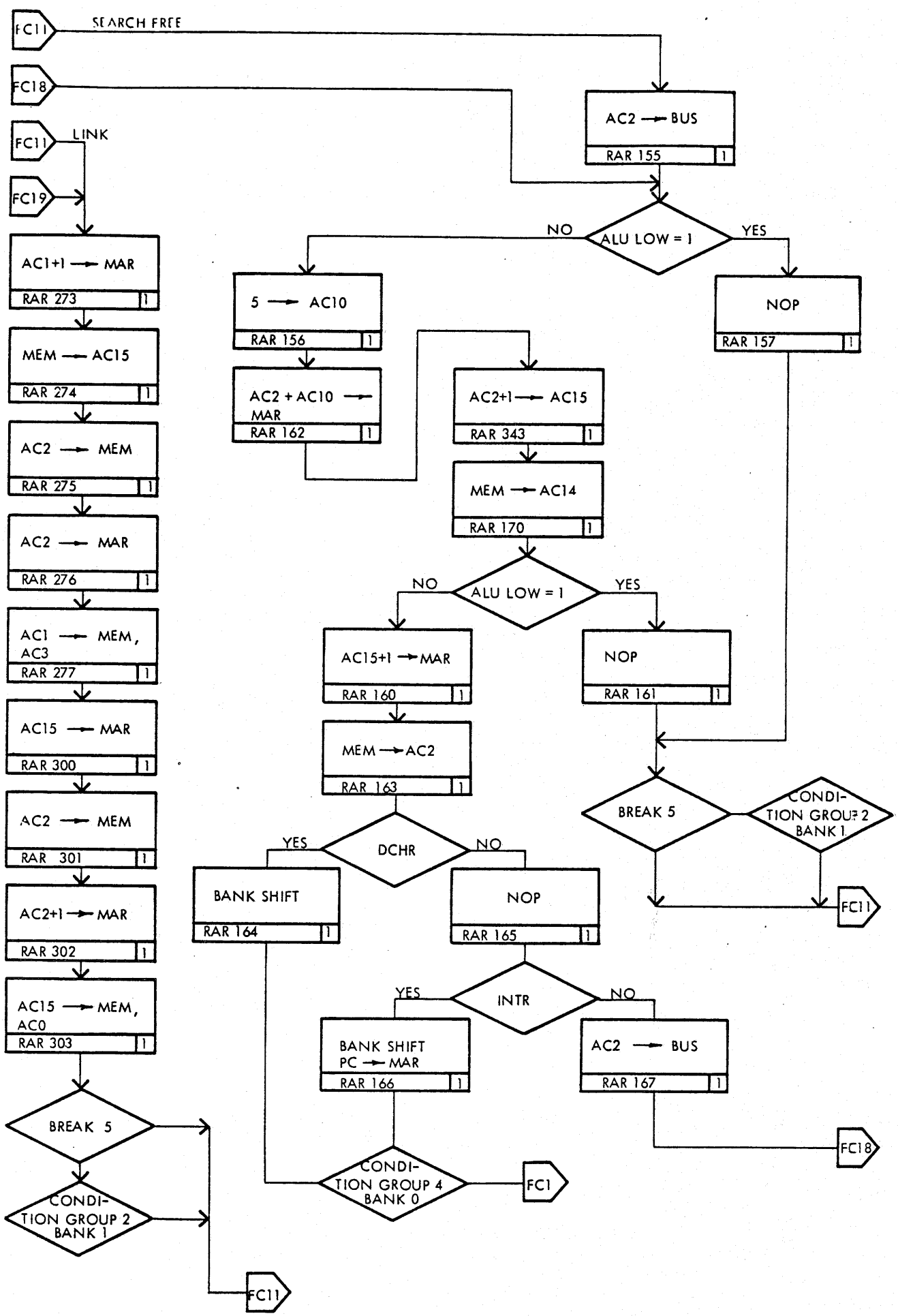
Signal List

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790206 BJ 790206 ABP

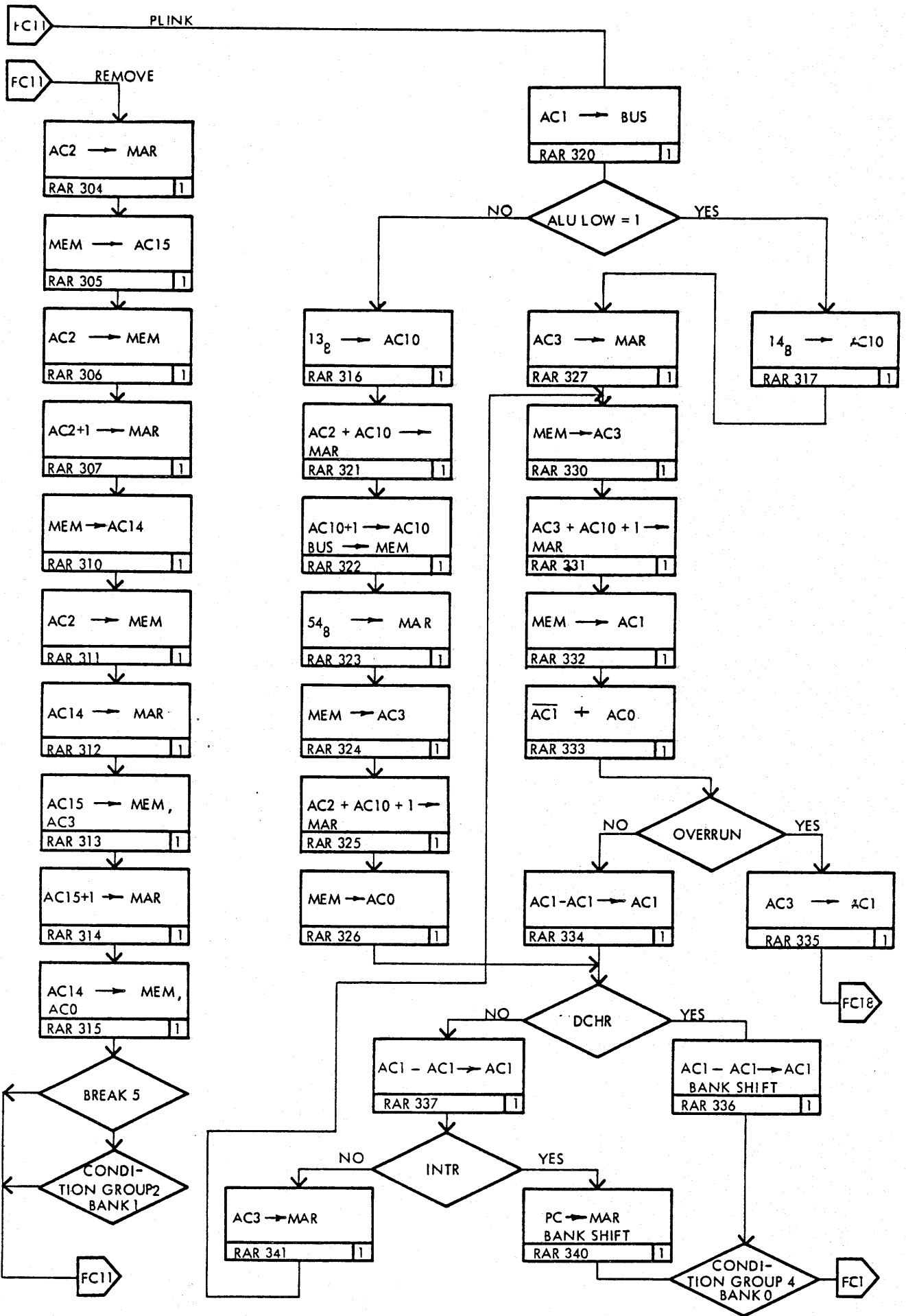
| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|--------------------------------|--|
| 155, 167 | DIRECT | <ul style="list-style-type: none"> ↳ COND SEL 0 ↳ COND SEL 1 ↳ 3 STATE EN ↳ LD MAR |
| 156 | DIRECT | ↳ ENABLE CONSTANT |
| 157 | CONDITION GROUP 2 BANK 1 | |
| 160, 302 | DIRECT | <ul style="list-style-type: none"> ↳ 3 STATE EN ↳ LD MAR ↳ C IN |
| 161, 343 | DIRECT | |
| 162, 273 | DIRECT | <ul style="list-style-type: none"> ↳ 3 STATE EN ↳ LD MAR |
| 163 | DIRECT | ↳ LD DATA REG COND SEL 1 |
| 164 | CONDITION GROUP 4 BANK 0 | |
| 165 | DIRECT | COND SEL 2 |
| 166 | CONDITION GROUP 4 BANK 0 | <ul style="list-style-type: none"> ↳ 3 STATE EN ↳ LD MAR |
| 170 | DIRECT | <ul style="list-style-type: none"> ↳ LD DATA REG COND SEL 0 COND SEL 1 ↳ RQEN BX ↳ MEM READ |
| 274 | DIRECT | ↳ LD DATA REG ↳ MEM READ |
| 275, 301 | DIRECT | <ul style="list-style-type: none"> ↳ 3 STATE EN ↳ MEM WRITE ↳ TEST MEM |
| 276, 300 | DIRECT | ↳ 3 STATE EN ↳ LD MAR |
| 277 | DIRECT | <ul style="list-style-type: none"> ↳ 3 STATE EN ↳ MEM WRITE ↳ TEST MEM ↳ RQEN BX |
| 303 | CONDITION GROUP 2 BANK 1 | ↳ 3 STATE EN ↳ MEM WRITE ↳ TEST MEM |
| | | |



790207 ABP
790207 BJ

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|-------------------------|--------------------------------|---|
| 304, 312, 321, 327, 341 | DIRECT | <ul style="list-style-type: none"> ↳ 3 STATE EN ↳ LD MAR |
| 305, 310, 324, 330 | DIRECT | <ul style="list-style-type: none"> ↳ LD DATA REG ↳ MEM READ |
| 306, 313 | DIRECT | <ul style="list-style-type: none"> ↳ LD DATA REG ↳ 3 STATE EN ↳ MEM WRITE ↳ TEST MEM |
| 307, 325, 331, 314 | DIRECT | <ul style="list-style-type: none"> ↳ 3 STATE EN ↳ LD MAR ↳ C IN |
| 311 | DIRECT | <ul style="list-style-type: none"> ↳ LD DATA REG ↳ 3 STATE EN ↳ RQEN BX ↳ MEM WRITE ↳ TEST MEM |
| 315 | CONDITION GROUP 2 BANK 1 | <ul style="list-style-type: none"> ↳ LD DATA REG ↳ 3 STATE EN ↳ MEM WRITE ↳ TEST MEM |
| 316, 317 | DIRECT | <ul style="list-style-type: none"> ↳ ENABLE CONSTANT |
| 320 | DIRECT | <ul style="list-style-type: none"> COND SEL 0 COND SEL 1 ↳ LD MAR |
| 322 | DIRECT | <ul style="list-style-type: none"> ↳ MEM WRITE ↳ TEST MEM ↳ C IN |
| 323 | DIRECT | <ul style="list-style-type: none"> ↳ RQEN BX ↳ LD MAR ↳ ENABLE CONSTANT |
| 332 | DIRECT | <ul style="list-style-type: none"> ↳ LD DATA REG ↳ RQEN BX ↳ MEM READ |
| 333 | DIRECT | <ul style="list-style-type: none"> ↳ LD DATA REG COND SEL 0 COND SEL 1 ↳ 3 STATE EN ↳ LD MAR |
| 334 | DIRECT | <ul style="list-style-type: none"> ↳ C IN COND SEL 1 |
| 326 | DIRECT | <ul style="list-style-type: none"> ↳ LD DATA REG ↳ MEM READ COND SEL 1 |
| 335 | DIRECT | |
| 336 | CONDITION GROUP 4 BANK 0 | <ul style="list-style-type: none"> ↳ C IN |
| 337 | DIRECT | <ul style="list-style-type: none"> COND SEL 2 ↳ C IN |
| 340 | CONDITION GROUP 4 BANK 0 | <ul style="list-style-type: none"> ↳ 3 STATE EN ↳ LD MAR |

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790207 ABP
790207 BJ

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|---------------------------------|--------------------------------|---|
| 214, 215, 216 | DIRECT | , ENABLE CONSTANT |
| 217, 224, 226, 232 | DIRECT | , 3 STATE EN , LD MAR |
| 220 | DIRECT | COND SEL 0 , LD MAR , ENABLE CONSTANT |
| 221, 227 | DIRECT | , 3 STATE EN , RQEN BX , LD MAR |
| 222, 223, 225, 231, 233, 234 | DIRECT | , LD DATA REG , MEM READ |
| 230 | DIRECT | , LD MAR , EN CONSTANT |
| 235 | DIRECT | , 3 STATE EN , MEM WRITE , TEST MEM , C IN |
| 236 | DIRECT | , RESET BIT 0 |
| 237 | CONDITION GROUP 2 BANK 1 | , RESET BIT 0 |
| 342 | DIRECT | , LD DATA REG COND SEL 0 COND SEL 1 |
| | | |

A/S REGNENCENTRALEN

Designed by

Drawn by

Dwg. Office Check

Unit
CPU 720

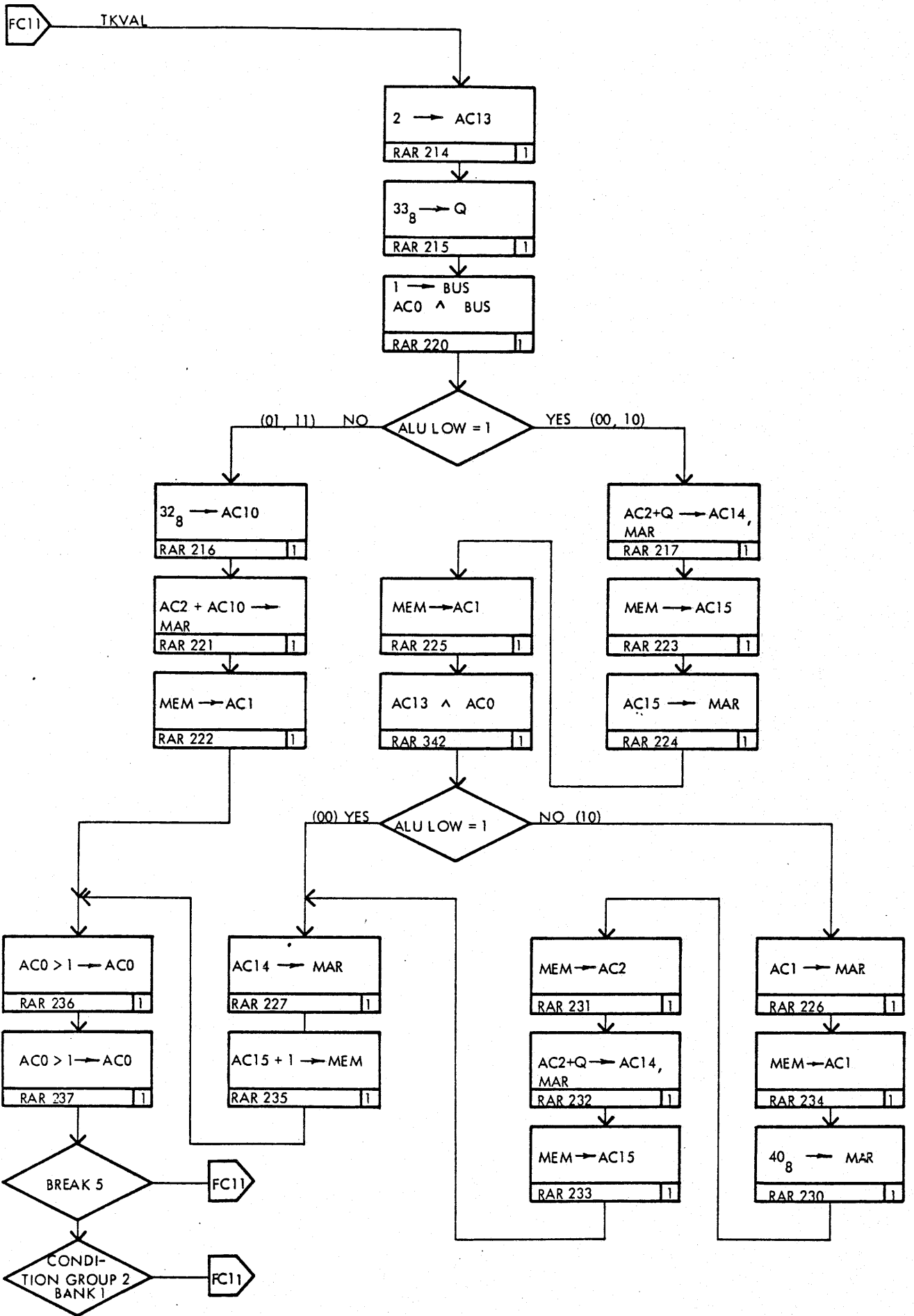
TAKE VALUE

FC 20

Dwg. No.
A25633

Signal List

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790208 BJ 790208 ABP

| ROM ADDRESS (OCTAL) | ADDRESS CALCULATION TYPE | DO - FUNCTIONS |
|------------------------|--------------------------------|--|
| 240, 252, 263, 266 | DIRECT | , ENABLE CONSTANT |
| 241, 264, 267 | DIRECT | , 3 STATE EN , LD MAR |
| 242 | DIRECT | , MEM READ |
| 243 | DIRECT | , LD DATA REG , 3 STATE EN , MEM WRITE , TEST MEM , C IN |
| 244 | DIRECT | , LD DATA REG , 3 STATE EN , RQEN BX , LD MAR |
| 246, 265, 272 | DIRECT | , LD DATA REG , MEM READ |
| 247 | DIRECT | COND SEL 0 COND SEL 1 , LD MAR , ENABLE CONSTANT |
| 250, 251 | DIRECT | , RESET BIT 0 |
| 253 | CONDITION GROUP 2 BANK 1 | , RESET BIT 0 |
| 254 | DIRECT | COND SEL 0 COND SEL 1 , LD MAR |
| 255 | DIRECT | , C IN |
| 256, 257, 260, 261 | DIRECT | SWAP EN |
| 262 | DIRECT | |
| 270 | DIRECT | , LD DATA REG , TEST MEM , MEM READ |
| 271 | DIRECT | , RQEN BX , LD MAR , ENABLE CONSTANT |
| | | |

Unit
CPU 720

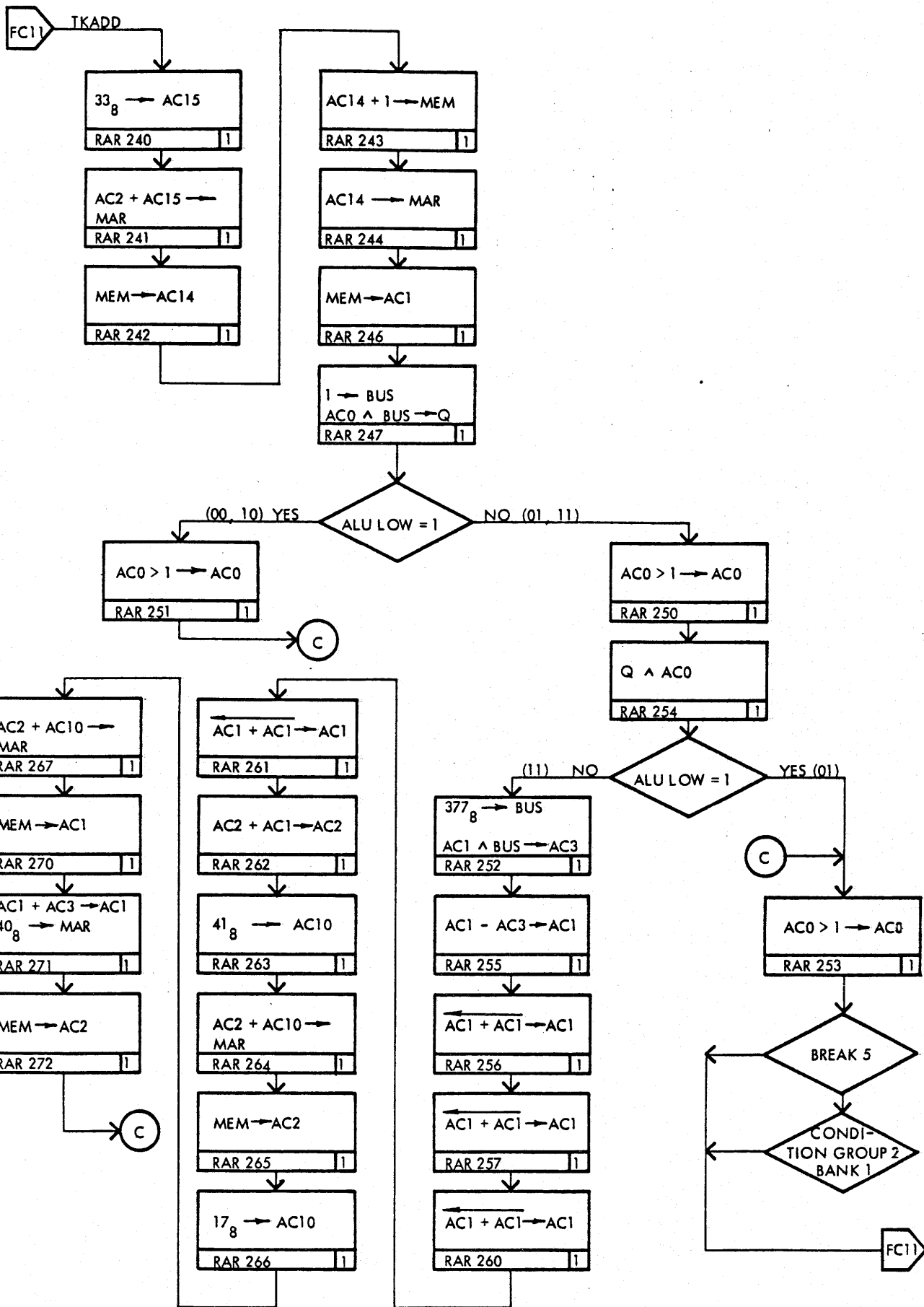
Dwg. No.
A25634

TAKE ADDRESS

Signal List

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790208 BJ 790208 ABP

