Title:

CPU 720

LOGIC DIAGRAMS

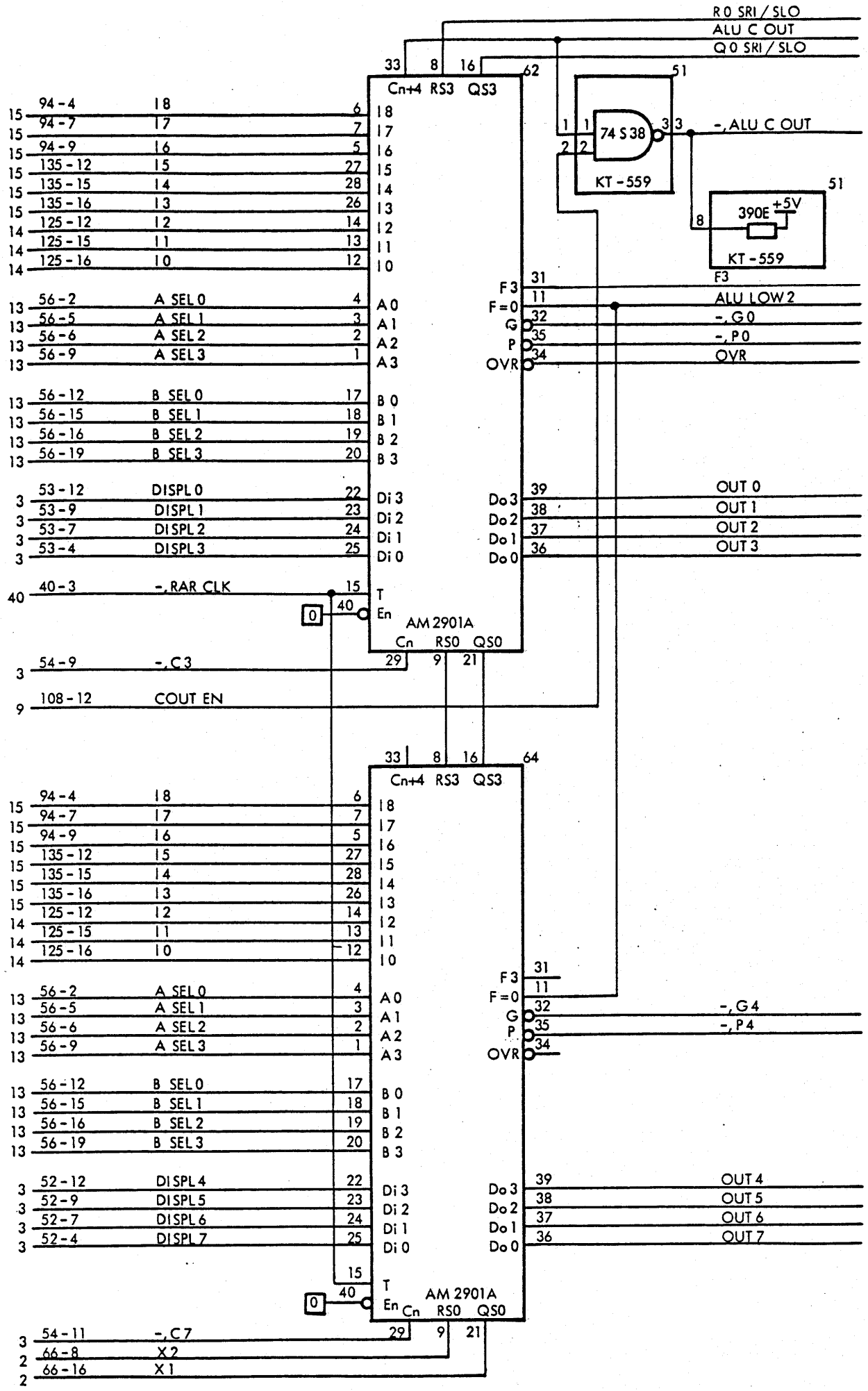
PRELIMINARY DOCUMENTATION

A/S REGNECENTRALEN

RC SYSTEM LIBRARY: FALKONERALLE 1 DK-2000 COPENHAGEN F

RCSL No: 44-RT 1878
Edition: 790323
Author: BJ

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
ALU COUT		p. 10 p. 42	ALU Carry OUTput The carry-out of the AM 2901A array.
¯; ALU COUT		p. 16	¯; ALU Carry OUTput The carry-out of the AM 2901A array gated by COUT EN.
ALU LOW 2		p. 26	ALU LOW output 2 This is an open collector output which goes high if the data on the ALU outputs bit 0-7 are all low.
¯; G0, ¯; G4		p. 3	¯; carry Generate outputs The carry generate outputs of the AM 2901A are used for carry-lookahead.
OUT 0-7		p. 5	OUTput bit 0-7 Output data contain either the outputs of the ALU or the data on the A-port of the register stack (16-8).
OVR		p. 16	OVeRflow Indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.
¯; P0, ¯; P4		p. 3	¯; carry Propagate outputs Used for carry lookahead.
Qo SRI/SLO		p. 18	Qo Shift Right Input/Shift Left Output. Q-register shift.
Ro SRI/SLO		p. 18	Ro Shift Right Input/Shift Left Output. Register stack shift.
F3		p. 42	The most significant ALU output bit (sign).



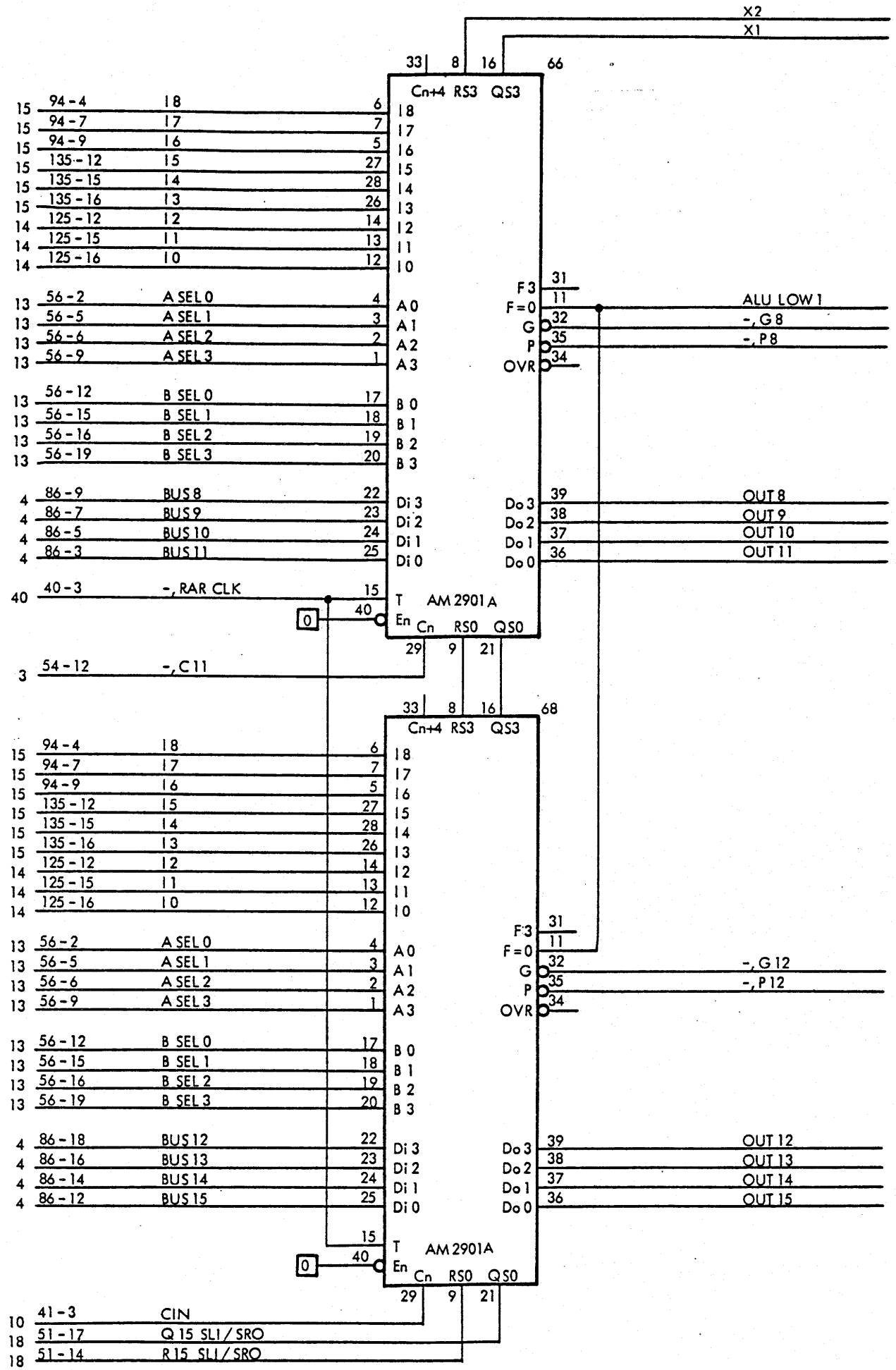
790130 BJ 790130 ABP

CPU 720
A13626

MICROPROCESSOR SLICES BIT 0-3 & 4-7
LOGIC DIAGRAM

CPU 001

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
ALU LOW 1		p. 26	ALU LOW output 1 This is an open collector output which goes high if the data on the ALU outputs, bit 8-15 are all low.
$\overline{\ }$ G8, $\overline{\ }$ G12		p. 3	$\overline{\ }$ carry Generate outputs Used for carry lookahead.
OUT 8-15		p. 5	OUTput bit 8-15 Output data contain either the outputs of the ALU or the data on the A-port of the register stack (16-8).
$\overline{\ }$ P8, $\overline{\ }$ P12		p. 3	$\overline{\ }$ carry Propagate outputs Used for carry lookahead.
x1		p. 1	Q_7 Shift Right Input/Shift Left output.
x2		p. 1	R_7 Shift Right Input/Shift Left output.



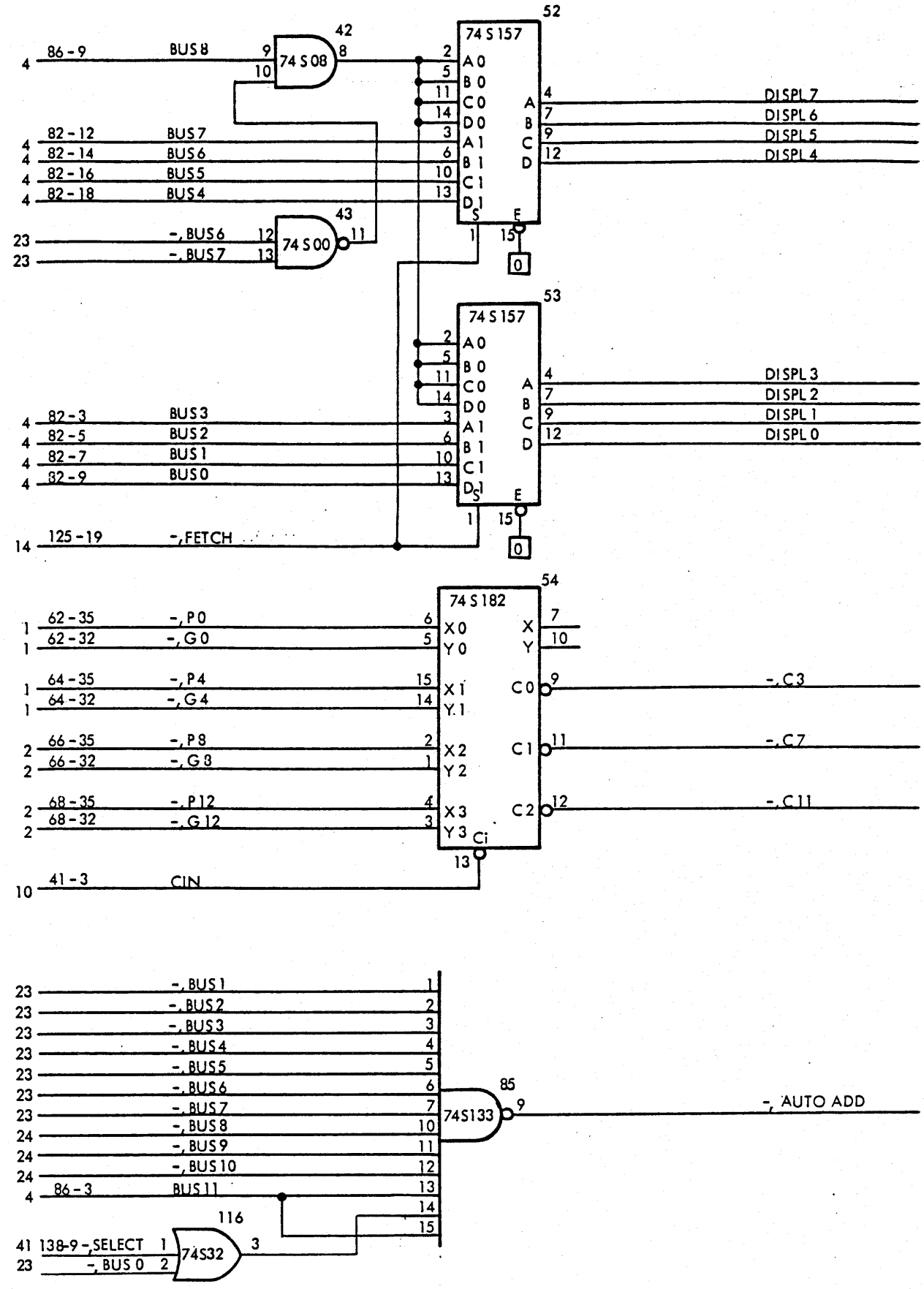
CPU 720

MICROPROCESSOR SLICES BIT 8-11 & 12-15
. LOGIC DIAGRAM

CPU 002

A13627

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
~ AUTO ADD		p. 16	AUTO increment/decrement ADDress.
~ C3		p. 1	~ Carry 3 Output from the carry look ahead generator.
~ C7		p. 1	~ Carry 7 Output from the carry look ahead generator.
~ C11		p. 2	~ Carry 11 Output from the carry look ahead generator.
DISPL 0-7		p. 1	DISPLacement bit 0-7 This data line contains either BUS 0-7 or the sign of the displacement in the instruction set extended through bit 0-7.



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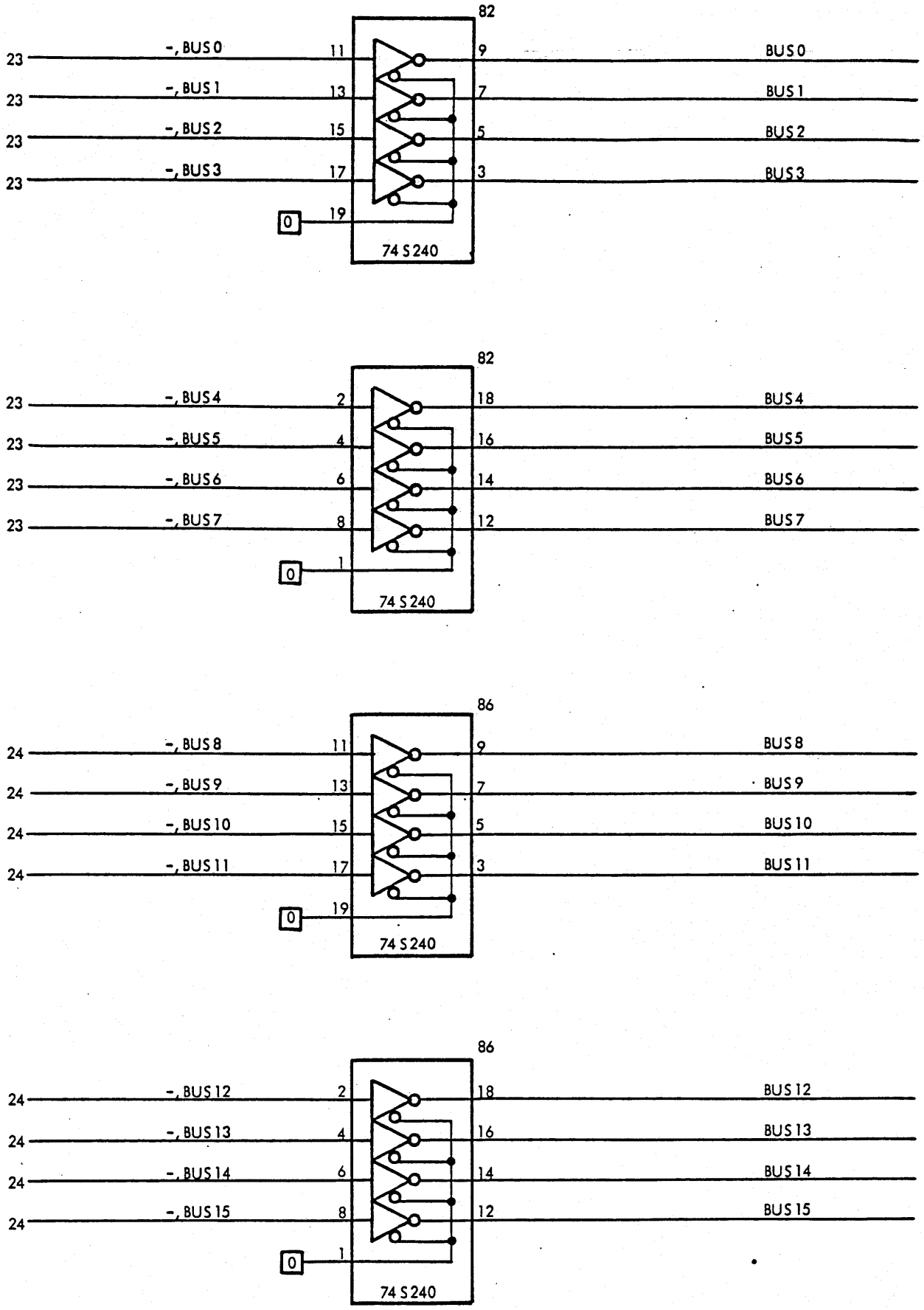
CPU 720

A13628

AUTO INCR/DECR DECODER, CARRY LOOK AHEAD
SIGN EXTEND CIRCUIT
LOGIC DIAGRAM

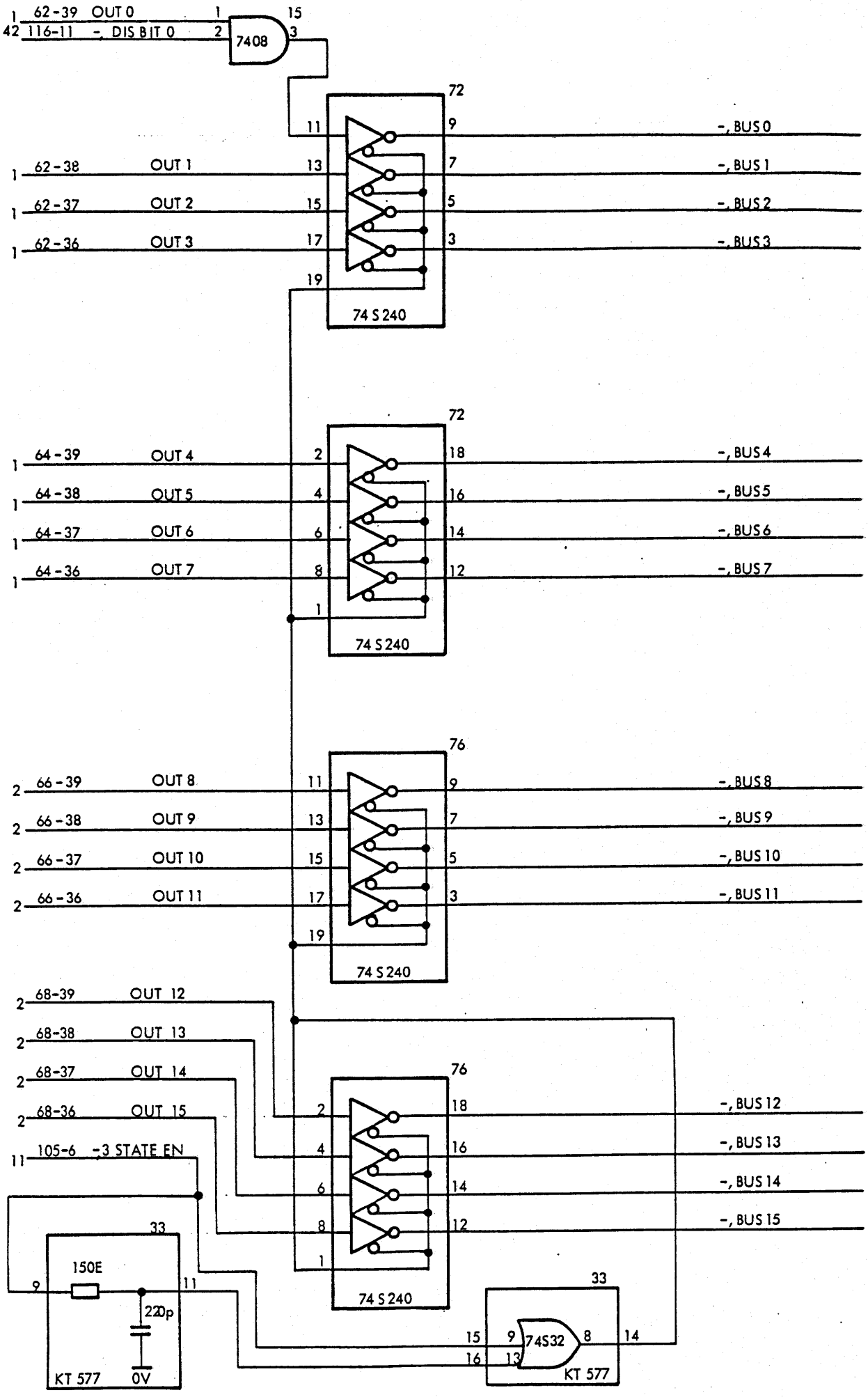
CPU 003

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
BUS 0		p. 3 p. 6 p. 8 p. 16 p. 17 p. 41	Internal BUS bit 0.
BUS 1-7		p. 3 p. 6 p. 8	Internal BUS bit 1-7.
BUS 8, 11		p. 2 p. 3 p. 6	Internal BUS bit 8, 11.
BUS 9-10, 13-14		p. 2 p. 6	Internal BUS bit 9-10, 13-14.
BUS 12, 15		p. 2 p. 6 p. 16	Internal BUS bit 12, 15.



790130 BJ 790130 ABP

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
⁻; BUS 0-7		p. 23	⁻; internal BUS bit 0-7.
⁻; BUS 8-15		p. 24	⁻; internal BUS bit 8-15.



790130 BJ 790130 ABP

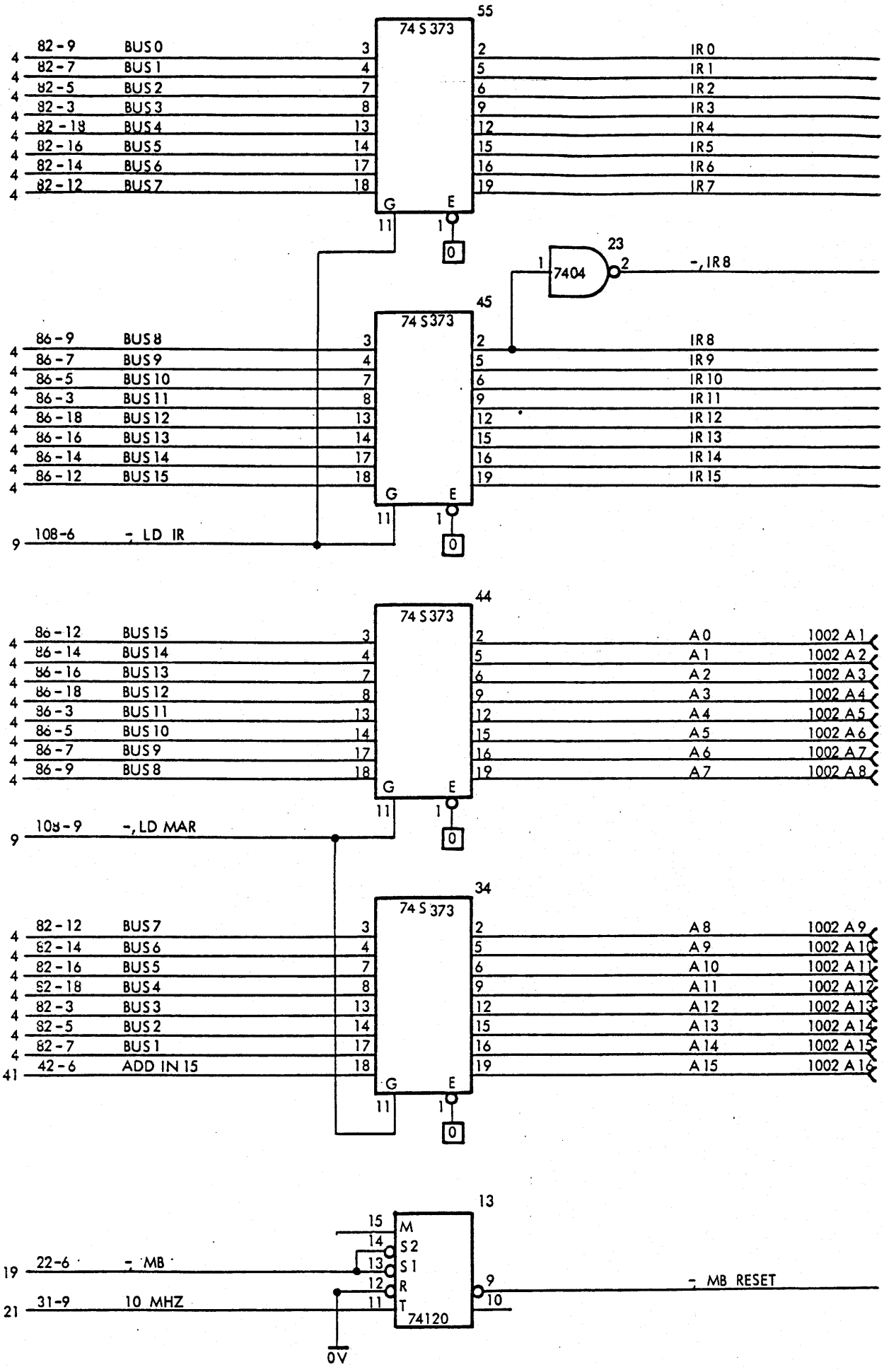
CPU 720

INVERTER FOR MICROPROCESSOR OUTPUT
LOGIC DIAGRAM

CPU 005

A13630

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
A0-A15		1002	memory Address 0-15. A0 is the least significant bit of the memory address. A15 is normal zero except when memory extension is selected.
IR 15		p. 18 p. 33 p. 22	Instruction Register bit 15.
IR 14-13		p. 17 p. 18 p. 33 p. 22	Instruction Register bit 14-13.
IR 12		p. 16 p. 17 p. 33 p. 22	Instruction Register bit 12.
IR 11-10		p. 16 p. 33 p. 22	Instruction Register bit 11-10.
IR 9		p. 16 p. 17 p. 18 p. 31 p. 33	Instruction Register bit 9.
IR 8		p. 16 p. 17 p. 31 p. 33	Instruction Register bit 8.
IR 7-5		p. 17 p. 31	Instruction Register bit 7-5.
IR 4-2		p. 17 p. 13	Instruction Register bit 4-2.
IR 1		p. 18 p. 17 p. 13	Instruction Register bit 1
IR 0		p. 18	Instruction Register bit 0.
-, IR 8		p. 33	-, Instruction Register bit 8.
-, MB RESET		p. 19	-, Memory Busy RESET. Reset pulse to the Memory Start flip-flop, generated on the Leading edge of Memory Busy.



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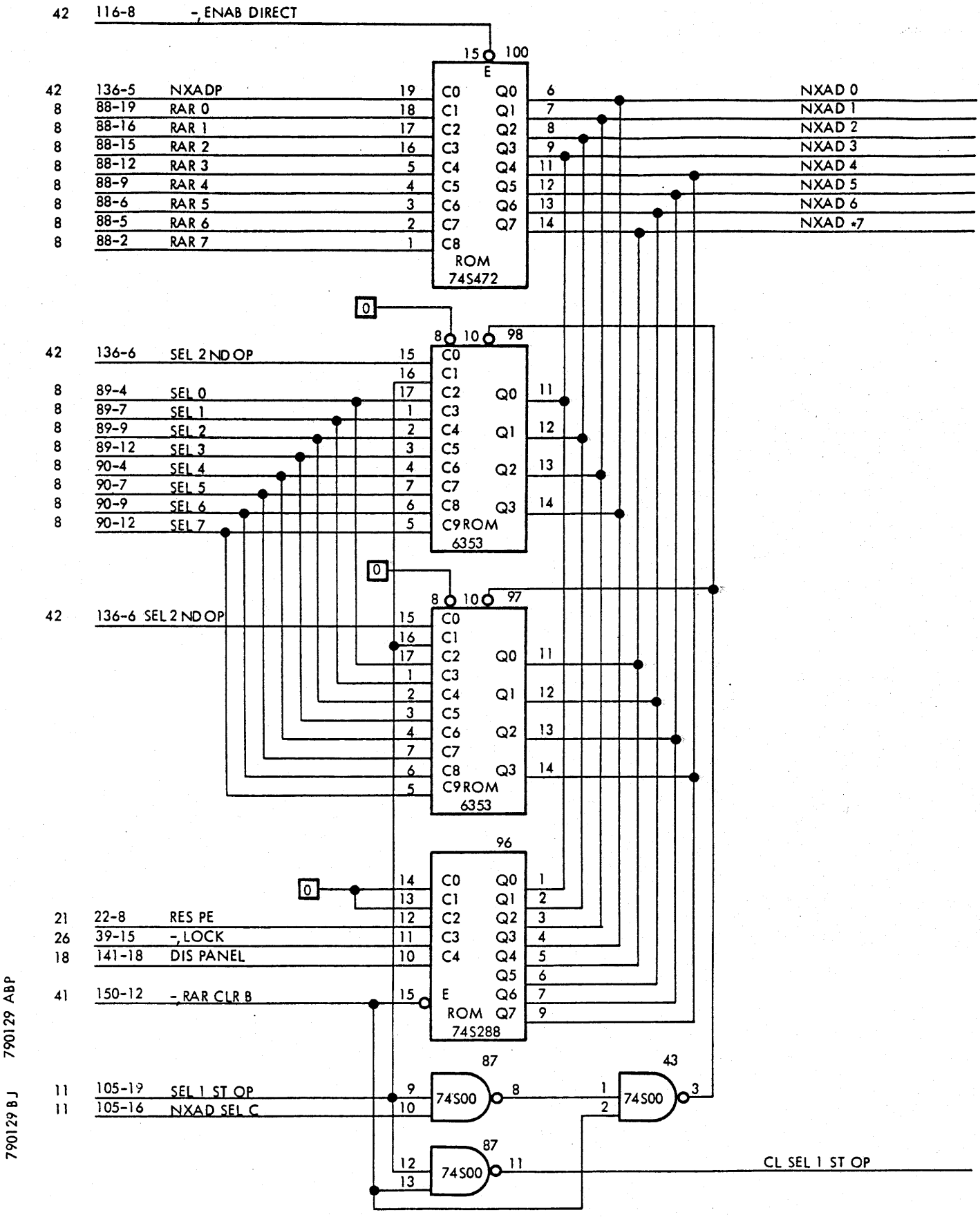
CPU 720

INSTRUCTION REGISTER - MEMORY ADDRESS REGISTER
LOGIC DIAGRAM

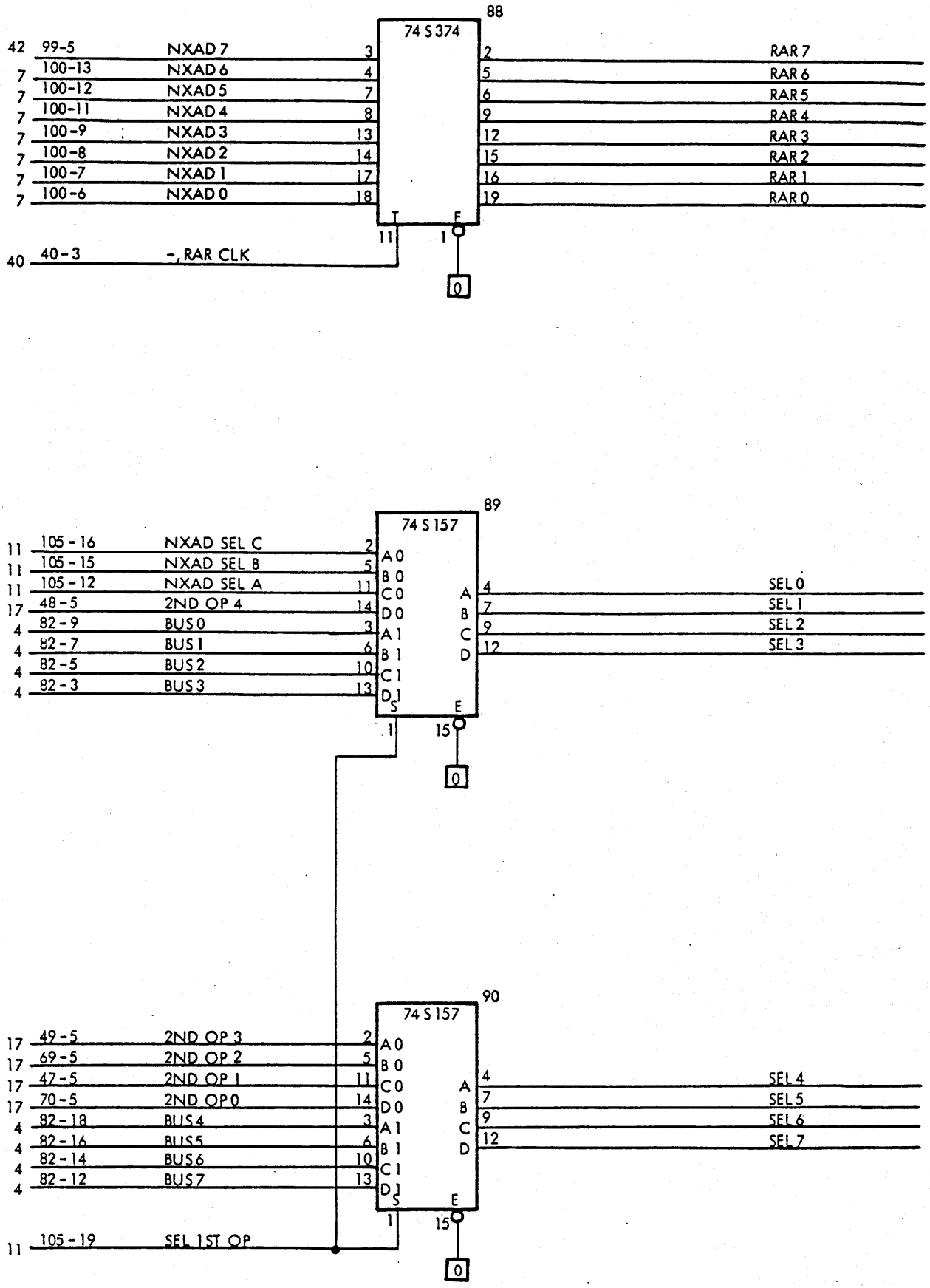
CPU 006

A13631

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
NXAD 0-6		p. 8 p. 9 p. 10 p. 11 p. 12 p. 13 p. 14 p. 15 p. 16 p. 41 p. 42	NeXt micro ADdress bit 0-7. NXAD 7 is the least significant bit of the address. During fetch or conditional jump the next address is read out from ROM Unconditional jump address is read out from ROM Start address after power up is read out from ROM
NXAD * 7		p. 42	
CL SEL 1ST OP		p. 42	CLocked SEL 1ST OP


42 116-8 -, ENAB DIRECT
15 100
E
42 136-5 NXADP 19 C0 Q0 6 NXAD 0
8 88-19 RAR 0 18 C1 Q1 7 NXAD 1
8 88-16 RAR 1 17 C2 Q2 8 NXAD 2
8 88-15 RAR 2 16 C3 Q3 9 NXAD 3
8 88-12 RAR 3 5 C4 Q4 11 NXAD 4
8 88-9 RAR 4 4 C5 Q5 12 NXAD 5
8 88-6 RAR 5 3 C6 Q6 13 NXAD 6
8 88-5 RAR 6 2 C7 Q7 14 NXAD *7
8 88-2 RAR 7 1 C8
ROM
74S472
0
8 10 98
42 136-6 SEL 2ND OP 15 C0
16 C1
8 89-4 SEL 0 17 C2 Q0 11
8 89-7 SEL 1 1 C3
8 89-9 SEL 2 2 C4 Q1 12
8 89-12 SEL 3 3 C5
8 90-4 SEL 4 4 C6 Q2 13
8 90-7 SEL 5 7 C7
8 90-9 SEL 6 6 C8 Q3 14
8 90-12 SEL 7 5 C9ROM
6353
0
8 10 97
42 136-6 SEL 2ND OP 15 C0
16 C1
17 C2 Q0 11
1 C3
2 C4 Q1 12
3 C5
4 C6 Q2 13
7 C7
6 C8 Q3 14
5 C9ROM
6353
96
0
14 C0 Q0 1
13 C1 Q1 2
21 22-8 RES PE 12 C2 Q2 3
26 39-15 -, LOCK 11 C3 Q3 4
18 141-18 DIS PANEL 10 C4 Q4 5
Q5 6
41 150-12 -, RAR CLR B 15 E Q6 7
ROM Q7 9
74S288
87
43
11 105-19 SEL 1 ST OP 9 74S00 8 1 74S00 3
11 105-16 NXAD SEL C 10 2
87
12 74S00 11 CL SEL 1 ST OP
13
790129 ABP
790129 BJ

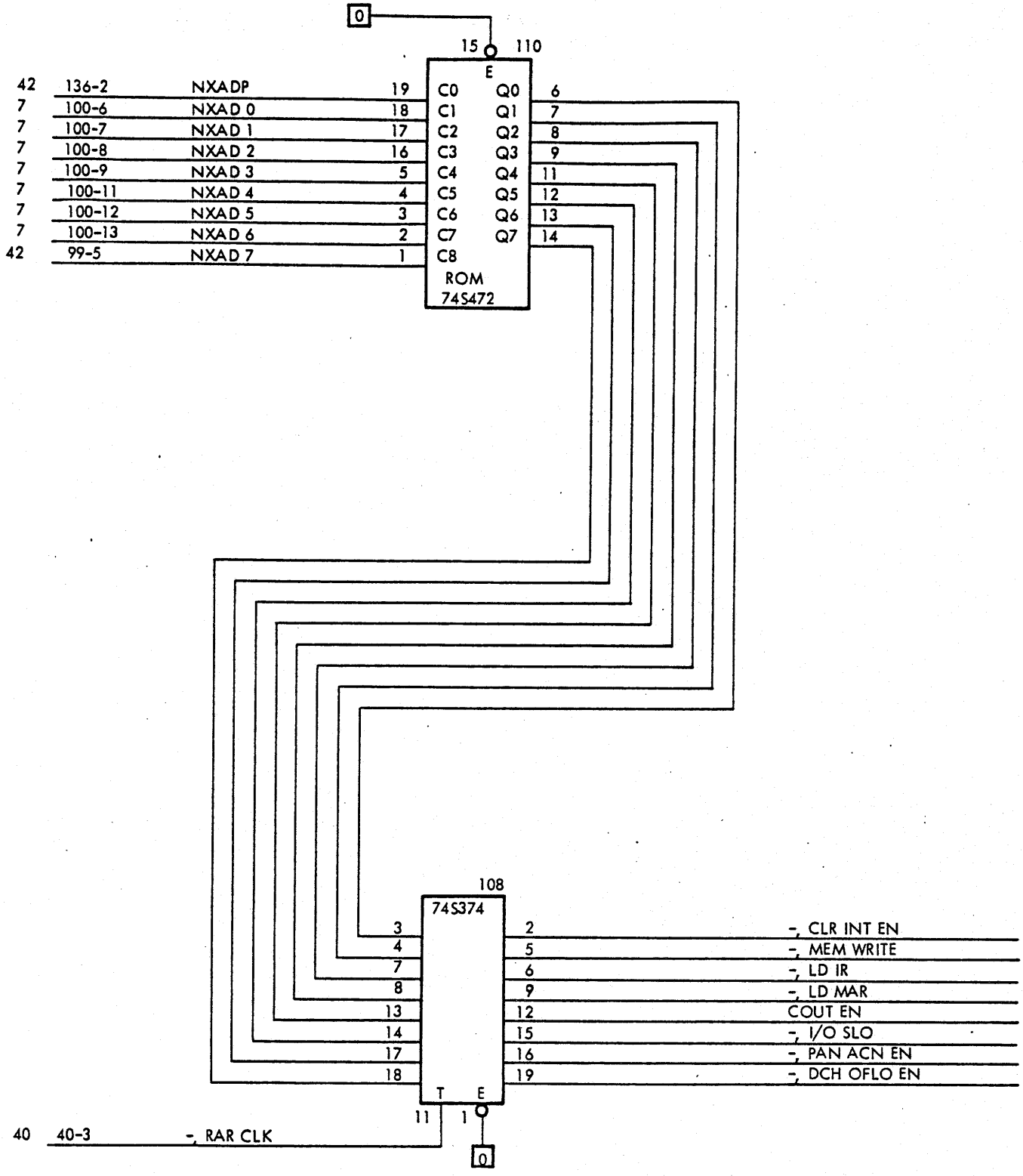
SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
RAR 0-7		p. 7 p. 38	Rom Address Register bit 0-7.
SEL 0-7		p. 7	SELect bit 0-7 These signals contain an eight bits address to the NEXT ADDRESS table. During the Fetch cycle (SEL 1ST OP = 1) these signals simply are BUS 0-7. During conditional jump (SEL 1ST OP = 0) these signals are the outputs from the condition selector extended to an eight bits address by help of NXAD SEL C-A (condition selection).



790130 ABP

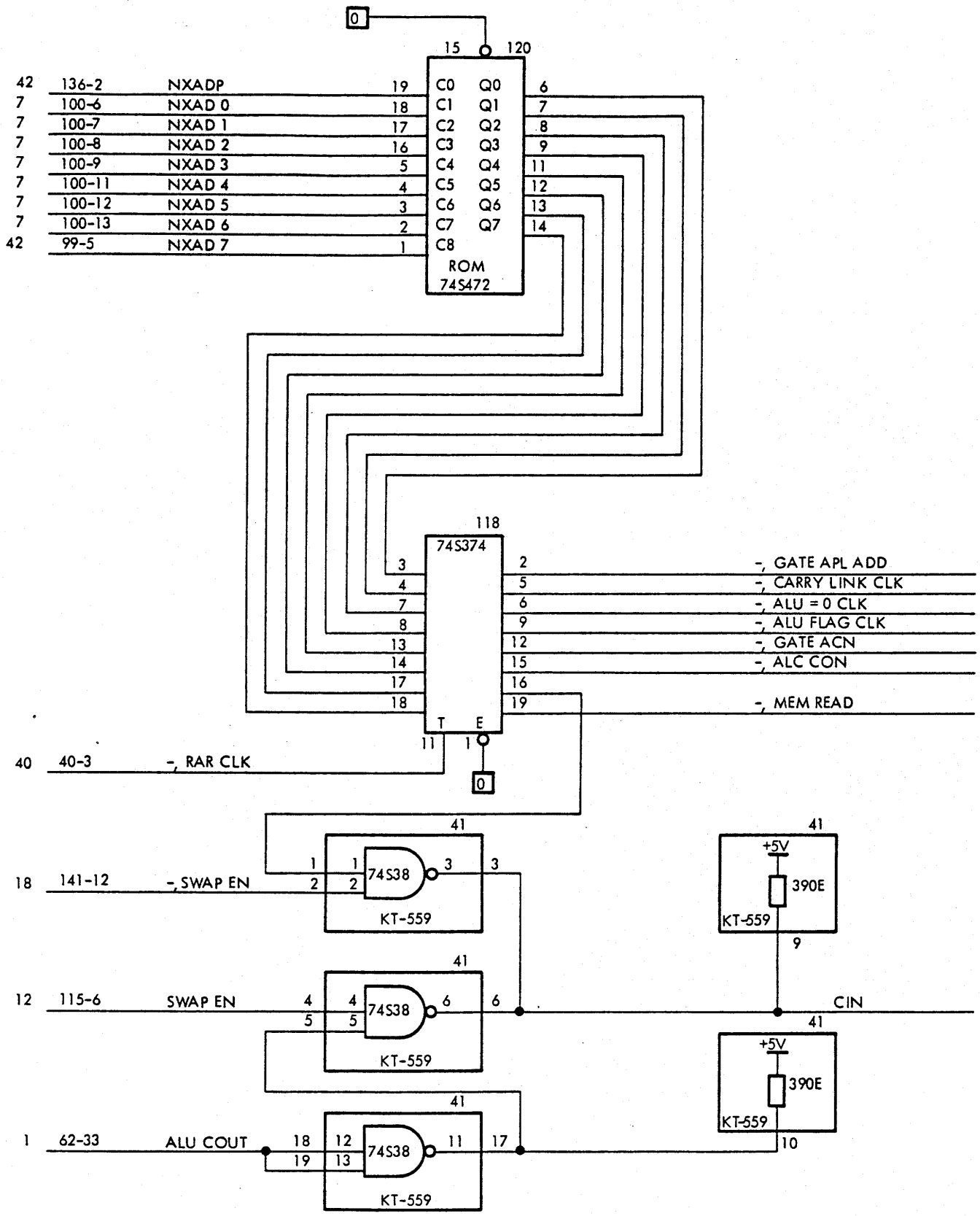
790130 BJ

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
~ CLR INT EN		p. 31	~ CLeaR INTerrupt ENable Clear Interrupt ON to prevent the processor from responding to further interrupt requests.
COUT EN		p. 1	Carry OUT ENable Used to enable carry out from the AM 2901A array.
~ DCH OFLO EN		p. 33	~ Data CHannel OverFLOw ENable Used to strobe the Overflow status out on the Data Channel control line OVFLO.
~ I/O SLO		p. 33	~ Input/Output device SeLect Out Places instruction register bit 10-15 on the Device Selection lines (DS 0-5).
~ LD IR		p. 6	~ LoaD Instruction Register Loads the contents on the data bus into the instruction register.
~ LD MAR		p. 6 p. 21	~ LoaD Memory Address Register Loads the contents on the data bus into the memory address register.
~ MEM WRITE		p. 19 p. 20	~ MEMory WRITE Starts the memory up with a write cycle.
~ PAN ACN EN		p. 13	~ PANel ACcumulator ENable Enables decoding of ASEL 0-3 and BSEL 0-3 from the state of the AC Sel switches on the Diagnostic Panel TCP 701.



790129 BJ 790129 ABP

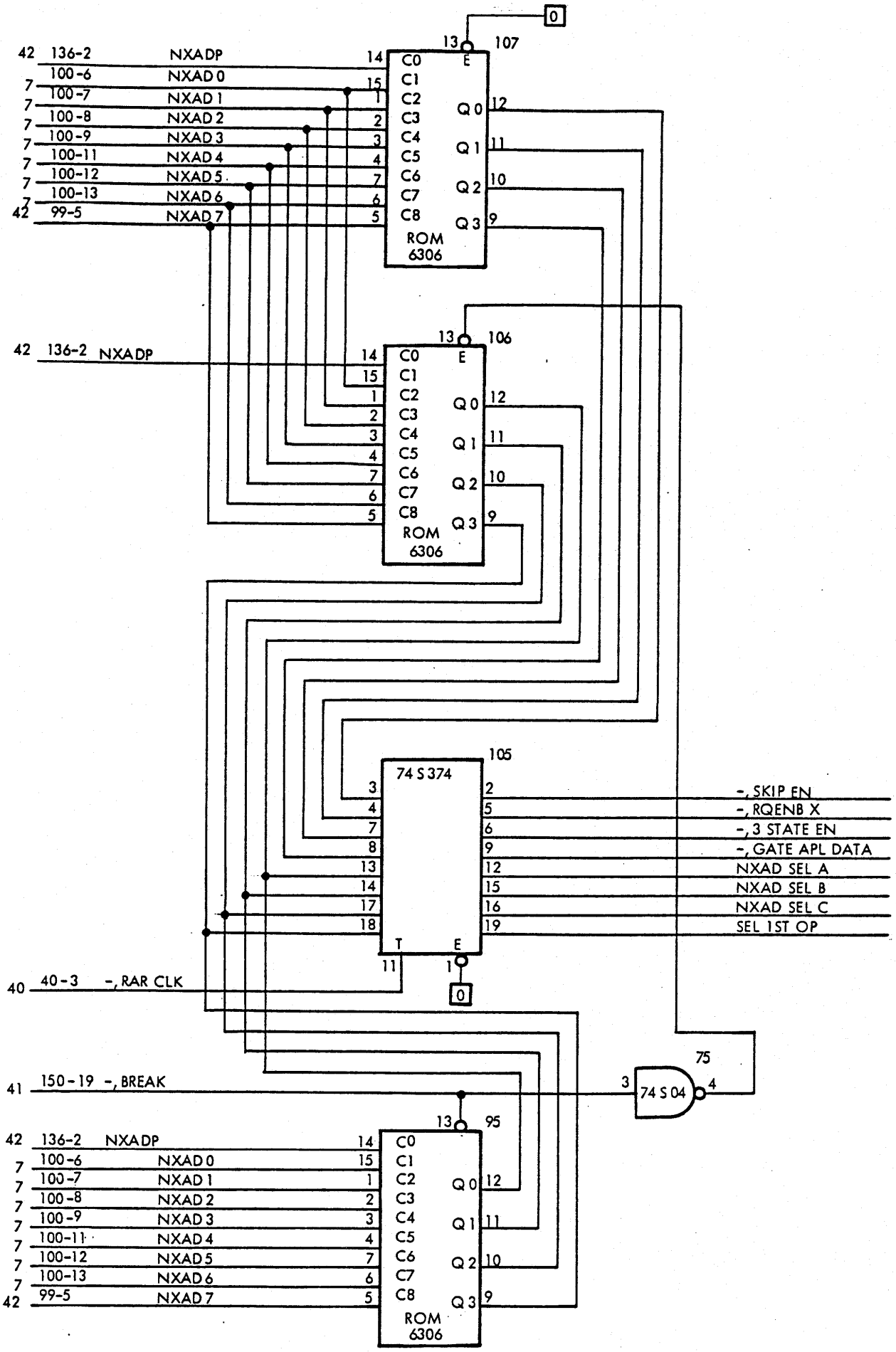
SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
~ ALC CON		p. 15	~ ALu Condition CONtrol Enables a decoder on IR 8-15 to determine if the result from the arithmetic operation should be loaded into Q or the specified distination accumulator.
~ ALU = 0 CLK		p. 18	~ ALU = 0 CLocK Loads the state of the zero decoder output from AM 2901A into the ALU = 0 status register.
~ ALU FLAG CLK		p. 16	~ ALU FLAG CLocK Updates the ALU status register.
~ CARRY LINK CLK		p. 18	~ CARRY LINK CLocK Loads the new carry from the Carry Generator into the Carry Register.
CIN		p. 2 p. 3	Carry INput Carry Input to the AM 2901 array.
~ GATE ACN		p. 13	~ GATE ACcumulator eNable Enables decoding of ASEL 0-3 and BSEL 0-3 from IR 1-4.
~ GATE APL ADD		p. 22 p. 37	~ GATE Automatic Program Load ADDress Gates the contents of the APL address counter out on the data bus.
~ MEM READ		p. 19 p. 20	~ MEMory READ Starts the memory up in a READ cycle.



790129 ABP

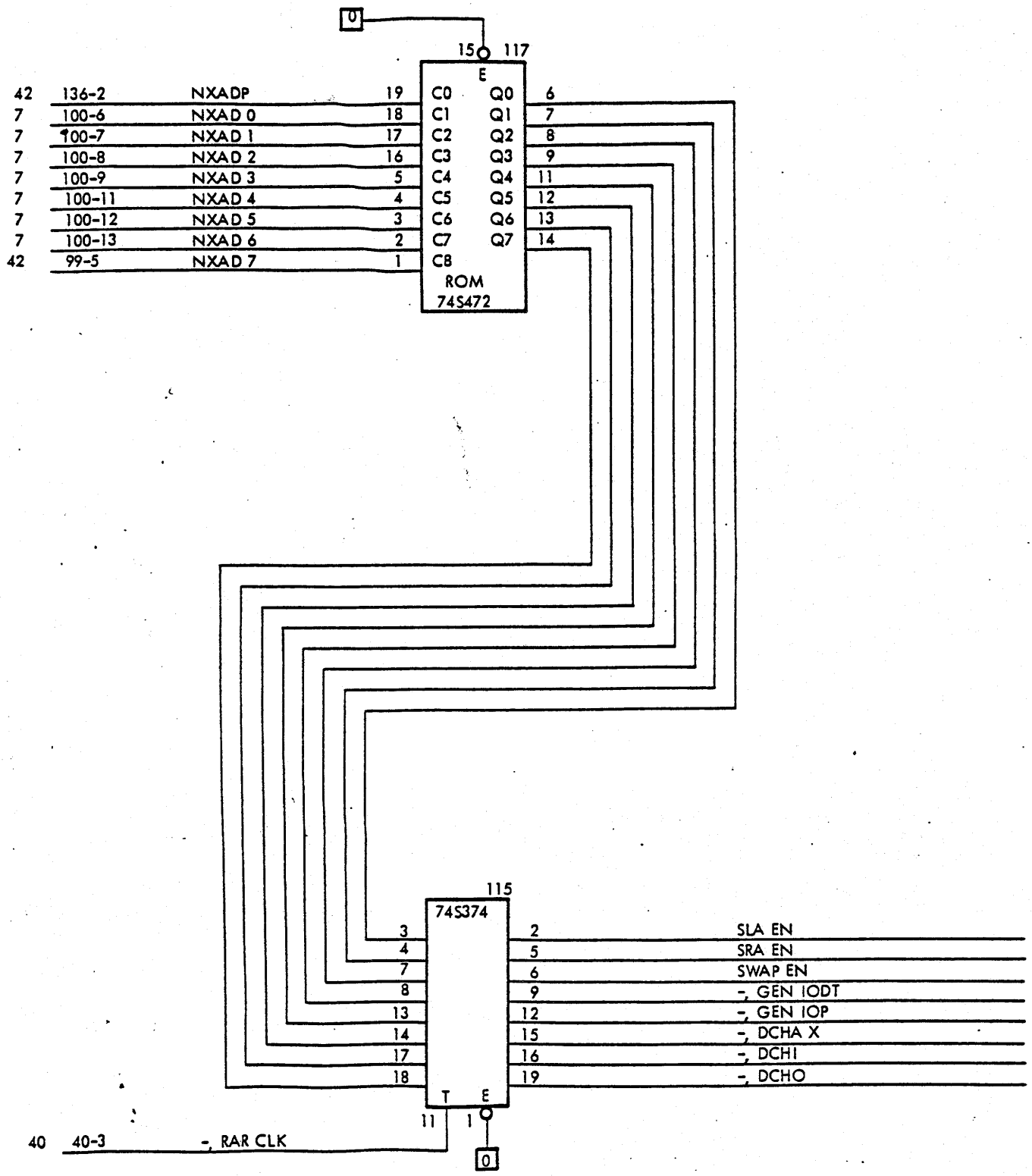
790129 BJ

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
~ GATE APL DATA		p. 18 p. 22	~ GATE Automatic Program Load DATA The contents of the addressed location of the autoload PROM is gated out on the data bus.
NXAD SEL A NXAD SEL B NXAD SEL C		p. 8 p. 17 p. 42 p. 8 p. 17 p. 7 p. 8 p. 17	NeXt ADdress SEL A-C Determines whether the next address calculation is conditional, unconditional or jumps from fetch cycle to the start-address of the microsequence to execute the current instruction.
~ RQEN B x		p. 32	~ ReQuest ENaBle x Allows all devices on the I/O BUS to request program interrupts or data channel requests.
SEL 1ST OP		p. 7 p. 8 p. 21	SELect 1ST OPerand MSB address input to the next address table.
~ SKIP EN		p. 18	~ SKIP ENable Enables SKIP condition GENerator.
~ 3 STATE EN		p. 5	~ 3 STATE ENable Gates data from AM 2901 out on the internal data bus.



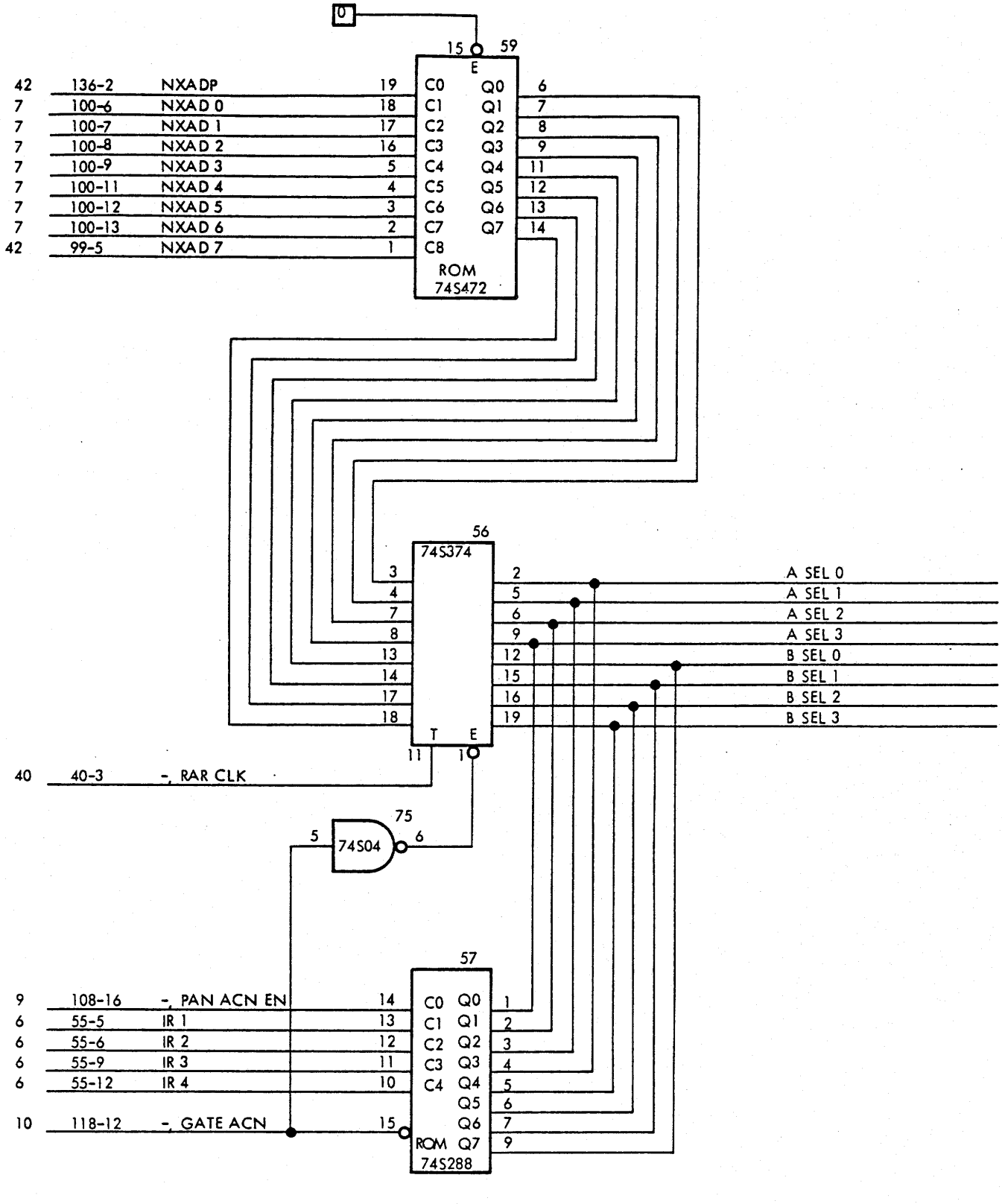
790131 BJ 790131 ABP

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
-, DCHA x		p. 32	-, Data CHannel Acknowledge x Strobes the memory address from current device out on the I/O BUS.
-, DCH I		p. 32	-, Data CHannel Input.
-, DCH O		p. 32	-, Data CHannel Output.
-, GEN IODT		p. 31	-, GENerate Input Output DaTa pulse Used to generate the I/O BUS signals DATO A-B, DATI A-B, INTA, MSKO and IORST.
-, GEN IOP		p. 31	-, GENerate Input Output Pulse Used to generate STRT, CLR and IOPL.
SLA EN		p. 18	Shift Left Accumulator ENable Connets SHIFT GENERATOR to Q_{15} SLI/SRO.
SRA EN		p. 18	Shift Right Accumulator ENable Connects SHIFT GENERATOR to Qo SRI/SLO.
SWAP EN		p. 10 p. 18	SWAP ENable Connects Ro SRI/SLO to R_{15} SLI/SRO, and ALU COUT to CIN.

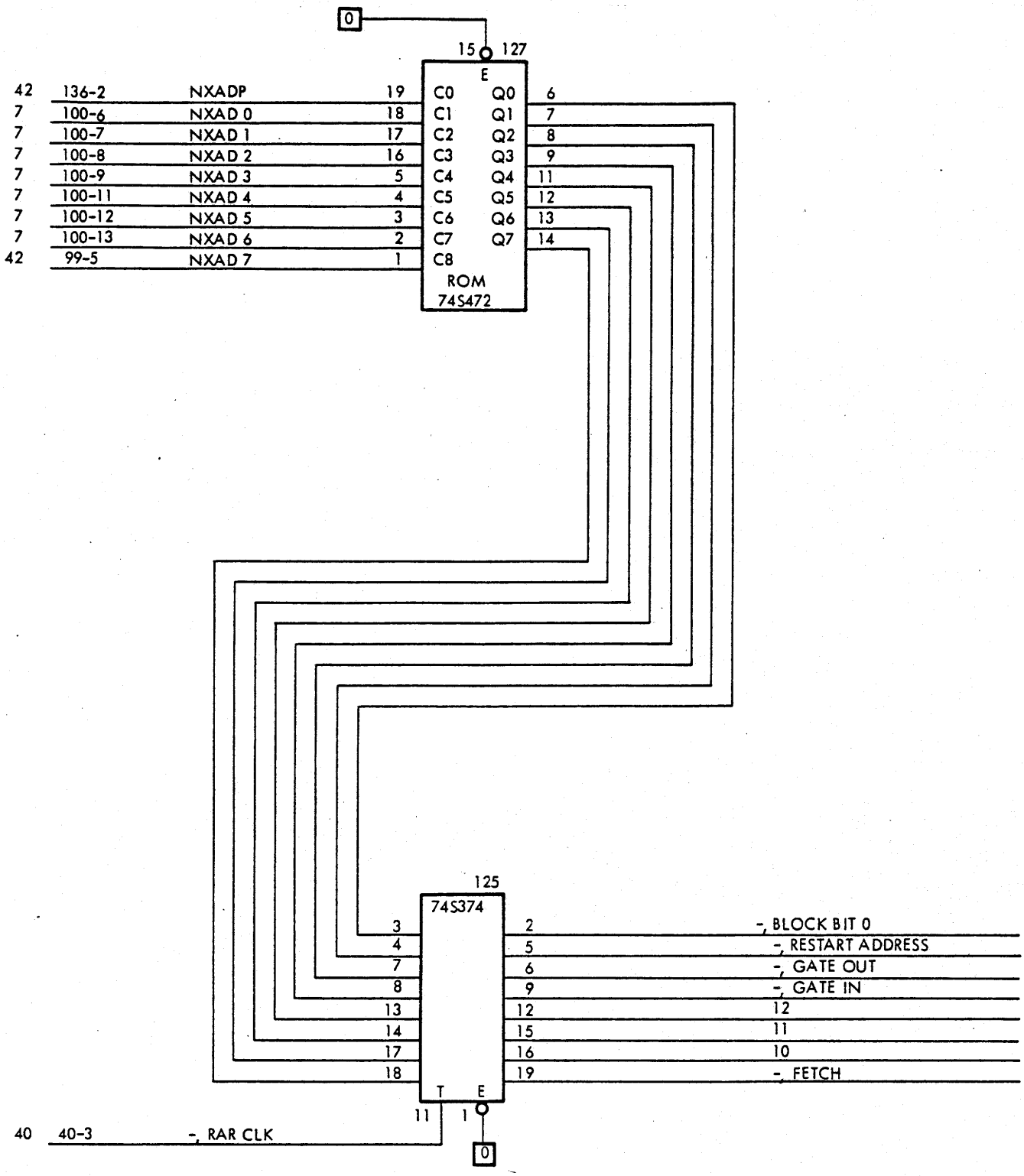


79 01 29 BJ 79 01 29 ABP

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
A SEL 0-3		p. 1 p. 2	A register SELect 0-3 Read only register address input to AM 2901 array.
B SEL 0-3		p. 1 p. 2	B register SELect 0-3 read-write register address input to the AM 2901 array.


0
15
59
E
42 136-2 NXADP 19 C0 Q0 6
7 100-6 NXAD 0 18 C1 Q1 7
7 100-7 NXAD 1 17 C2 Q2 8
7 100-8 NXAD 2 16 C3 Q3 9
7 100-9 NXAD 3 5 C4 Q4 11
7 100-11 NXAD 4 4 C5 Q5 12
7 100-12 NXAD 5 3 C6 Q6 13
7 100-13 NXAD 6 2 C7 Q7 14
42 99-5 NXAD 7 1 C8
ROM
74S472
56
74S374
3
4
7
8
13
14
17
18
2
5
6
9
12
15
16
19
A SEL 0
A SEL 1
A SEL 2
A SEL 3
B SEL 0
B SEL 1
B SEL 2
B SEL 3
T
E
11
10
40 40-3 -, RAR CLK
75
5
74S04
6
57
9 108-16 -, PAN ACN EN 14 C0 Q0 1
6 55-5 IR 1 13 C1 Q1 2
6 55-6 IR 2 12 C2 Q2 3
6 55-9 IR 3 11 C3 Q3 4
6 55-12 IR 4 10 C4 Q4 5
Q5 6
10 118-12 -, GATE ACN 15 Q6 7
ROM Q7 9
74S288
790129 ABP
790129 BJ

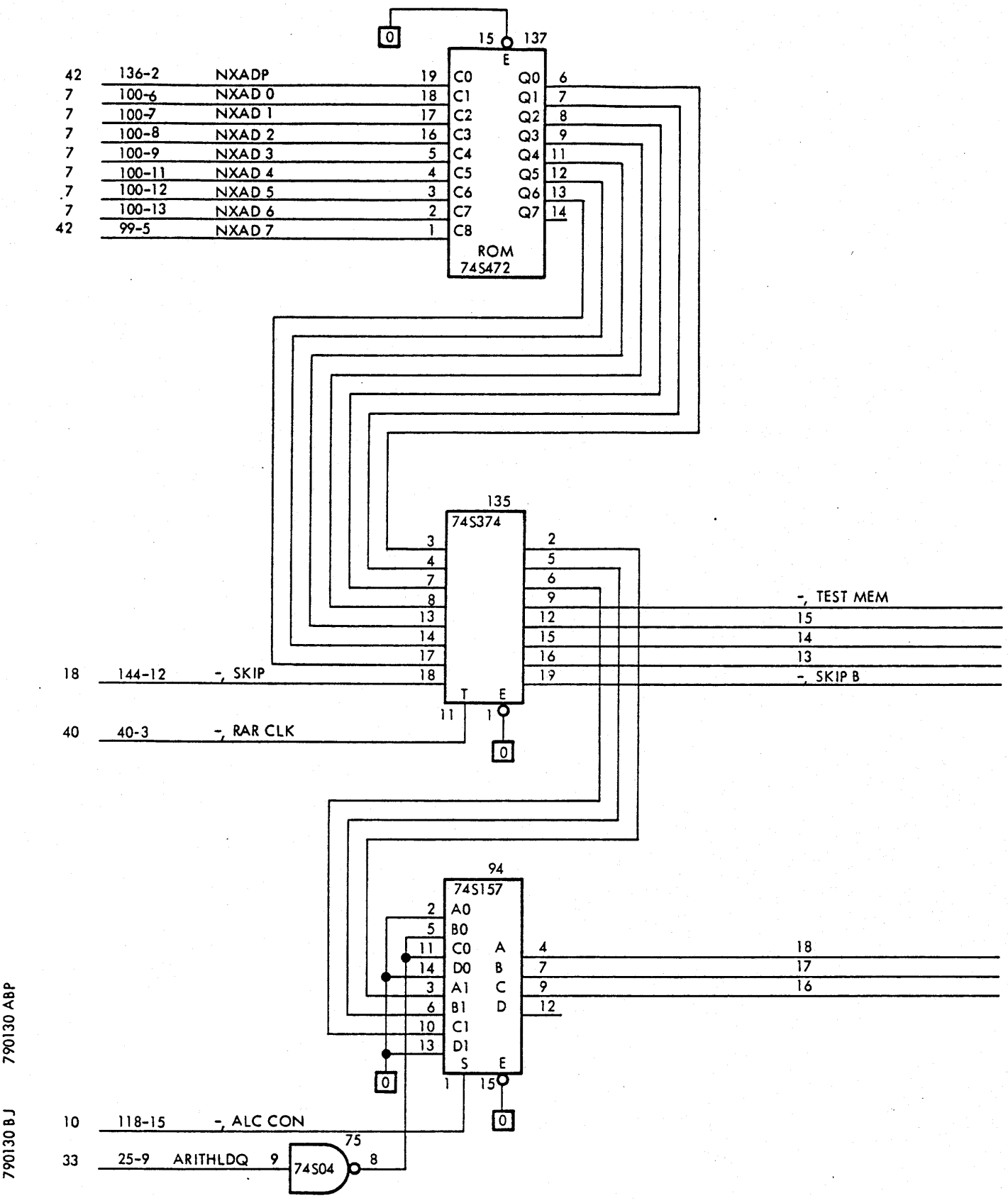
SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
-, BLOCK BIT 0		p. 42	-, BLOCK BIT 0 Forces a logical zero on bit 0 from the AM2901 array.
-, FETCH		p. 3 p. 37 p. 40 p. 31	-, FETCH Indicates that the CPU is reading an instruction from memory.
-, GATE IN		p. 30	-, GATE INput Gates the contents on the I/O Data BUS out on the internal bus.
-, GATE OUT		p. 40	-, GATE OUTput Gates the contents on the internal bus out on the I/O Data BUS.
I 0-2		p. 1 p. 2	micro Instruction bit 0-2 ALU source operand controls.
-, RESTART ADDRESS		p. 34 p. 37	-, RESTART ADDRESS Gates the contents of the Data Switches (TCP 701) out on the internal data bus and sets the CPU into the RUN state.



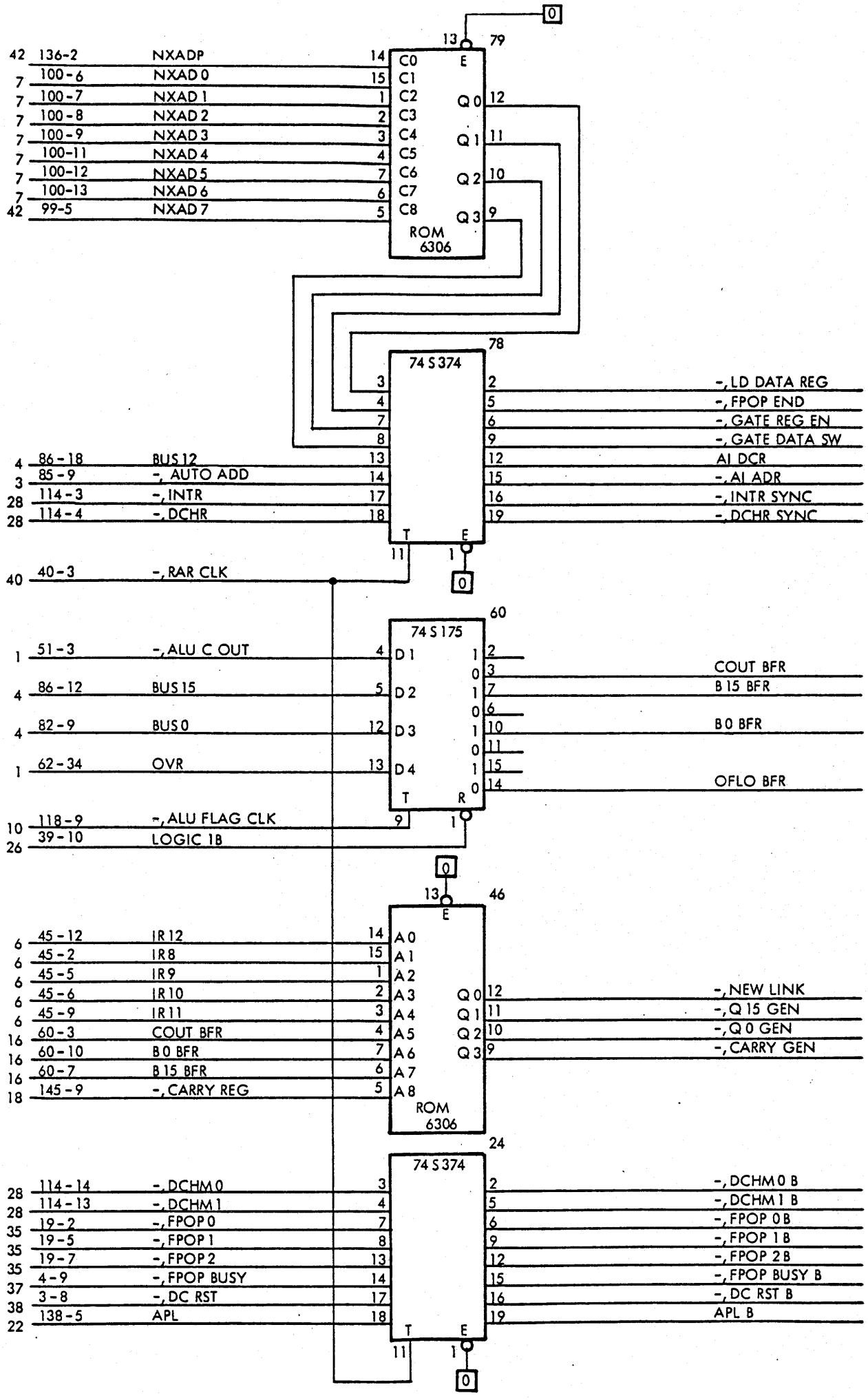
790129 ABP

790129 BJ

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
I 3-4		p. 1 p. 2	micro Instruction bit 3-4 ALU function control.
I 6-8		p. 1 p. 2	micro Instruction bit 6-8 ALU result destination control.
⁻; SKIP B		p. 17	⁻; SKIP Buffer Output from the SKIP condition Generator synchronized with the microprogram.
⁻; TEST MEM		p. 19	⁻; TEST MEMory Used to test the state of the Memory Busy status.


0
15
137
E
42 136-2 NXADP 19 C0 Q0 6
7 100-6 NXAD 0 18 C1 Q1 7
7 100-7 NXAD 1 17 C2 Q2 8
7 100-8 NXAD 2 16 C3 Q3 9
7 100-9 NXAD 3 5 C4 Q4 11
7 100-11 NXAD 4 4 C5 Q5 12
7 100-12 NXAD 5 3 C6 Q6 13
7 100-13 NXAD 6 2 C7 Q7 14
42 99-5 NXAD 7 1 C8
ROM
74S472
135
74S374
3 2
4 5
7 6
8 9 -, TEST MEM
13 12 15
14 15 14
17 16 13
18 144-12 -, SKIP 18 19 -, SKIP B
T E
11 1
40 40-3 -, RAR CLK
0
94
74S157
2 A0
5 B0
11 C0 A 4 18
14 D0 B 7 17
3 A1 C 9 16
6 B1 D 12
10 C1
13 D1
S E
1 15
0
0
790130 ABP
790130 BJ
10 118-15 -, ALC CON
75
33 25-9 ARITHLDQ 9 74S04 8

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
~ AIADR		p. 17	~ Automatic Indexing ADdRess
AIDCR		p. 17	Automatic Indexing DeCRement
APL B		p. 17	Automatic Program Load Buffered
B0 BFR		p. 16 p. 18	Bus bit 0 BuFfeRed
B15 BFR		p. 16	Bus bit 15 BuFfeRed
COUT BFR		p. 16	Carry OUTput BuFfeRed
~ CARRY GEN		p. 18	~ CARRY GENerator
~ DCHM 0-1 B		p. 17	~ Data CHannel Mode bit 0-1 Buffered
~ DC RST B		p. 17	~ DC ReSeT Buffered
~ DCHR SYNC		p. 17 p. 42	~ Data CHannel Requests SYNChronized
~ FPOP 0-2 B		p. 17	~ Front Panel OPeration bit 0-2 Buffered
~ FPOP BUSY B		p. 17	~ Front Panel OPeration BUSY Buffered
~ FPOP END		p. 37	~ Front Panel OPeration END
~ GATE DATA SW		p. 34	~ GATE DATA SWitches
~ GATE REG EN		p. 35	~ GATE REGister ENable
~ INTR SYNC		p. 17 p. 42	~ INTerrupt Requests SYNChronized
~ LD DATA REG		p. 36	~ LoaD DATA REGister
~ NEW LINK		p. 18	~ NEW LINK
OFLO BFR		p. 33	OverFLOw status BuFfeRed
~ Qo GEN		p. 18	~ Qo shift GENerator
~ Q_{15} GEN		p. 18	~ Q_{15} shift GENerator



790131 ABP

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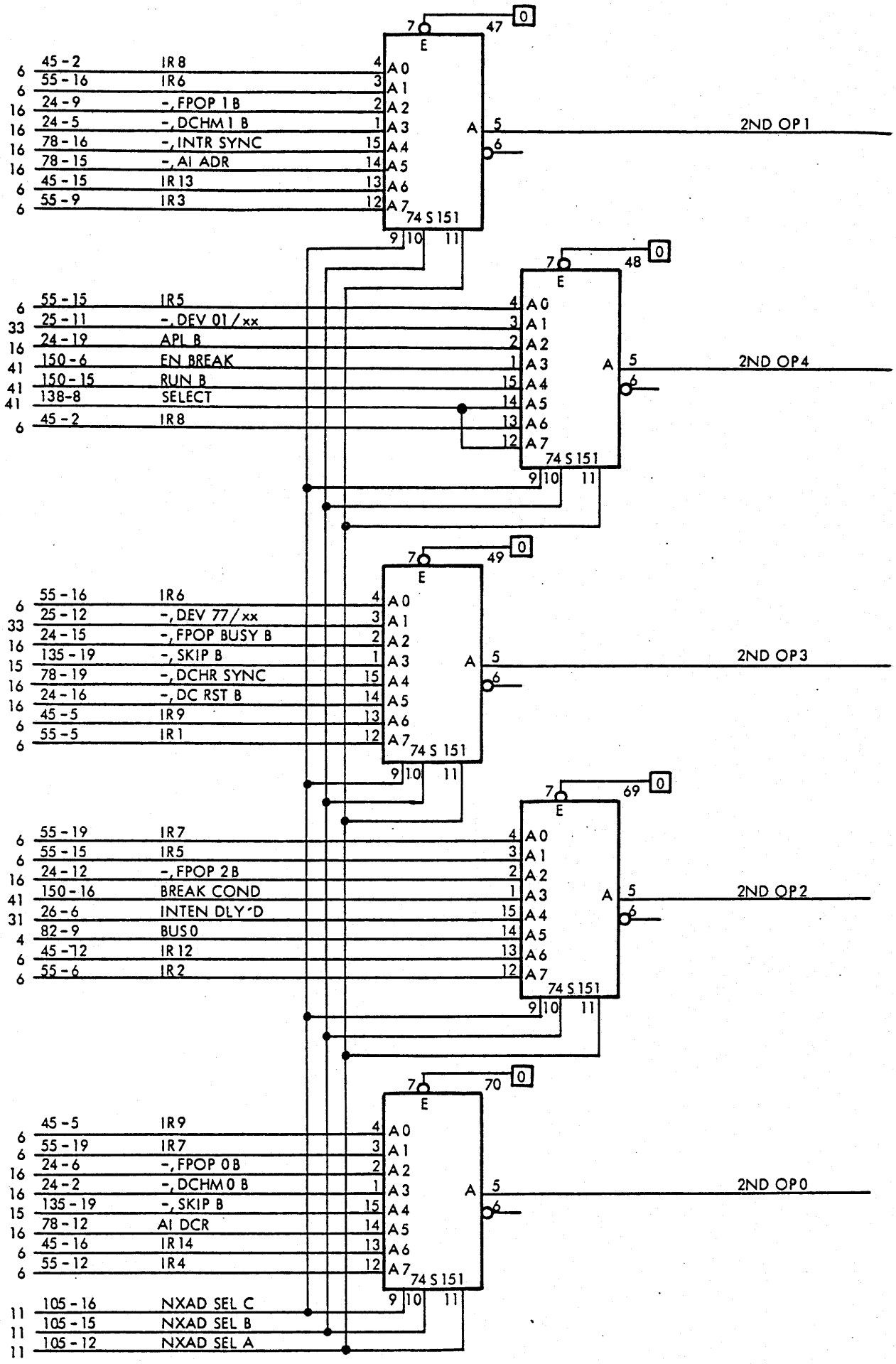
CPU 720

A13641

MICROPROGRAM STORE
CONTOL SIGNAL BUFFERS
CARRY DECODER
LOGIC DIAGRAM

CPU 016

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
2ND OP 0-4		p. 8	2ND OPerand bit 0-4 Outputs from the condition selector; used as the five least significant address inputs to the conditional next address table.



790131 BJ 790131 ABP

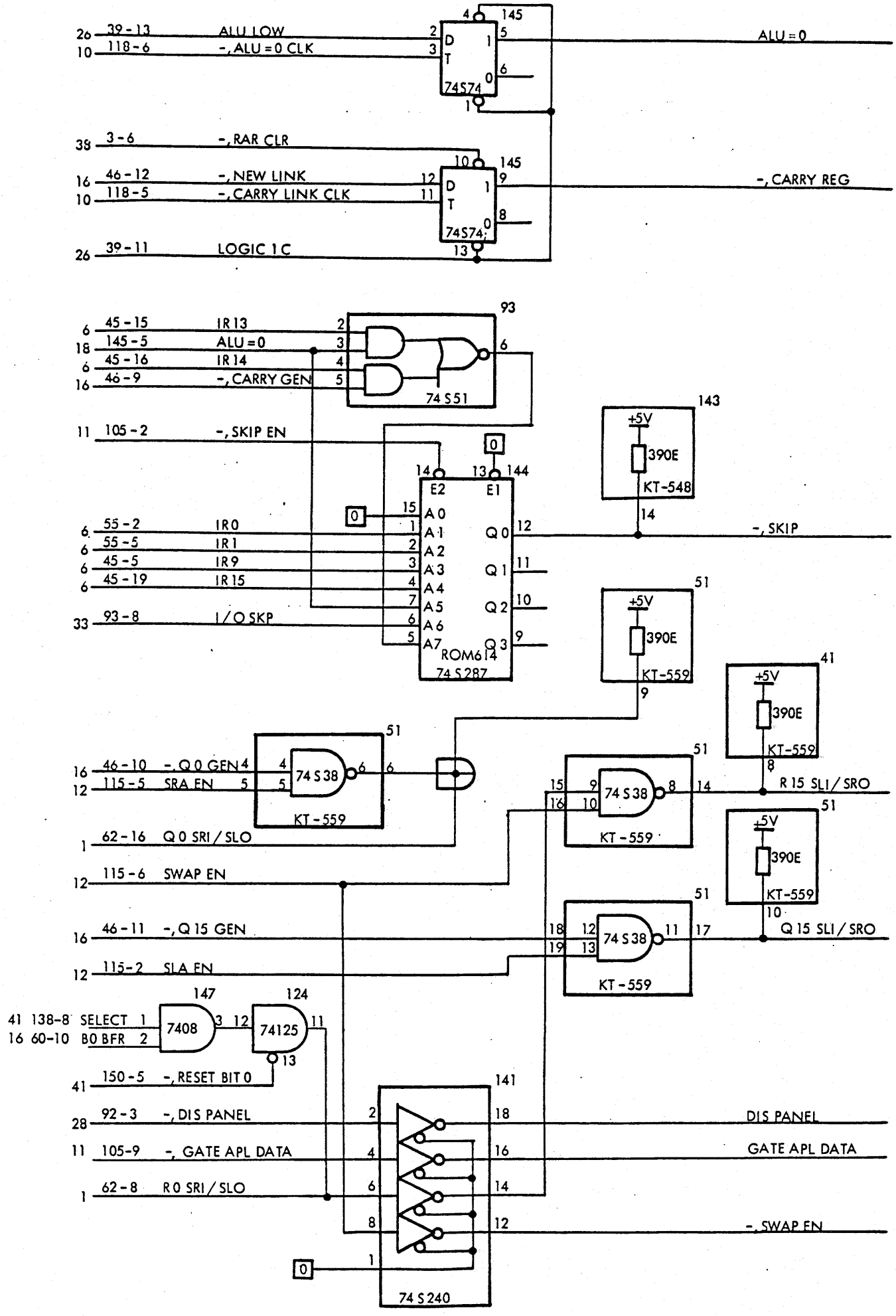
CPU 720

CONDITION SELECTOR
LOGIC DIAGRAM

CPU 017

A13642

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
ALU = 0		p. 18 p. 42	ALU = 0 Zero status from the ALU.
⁻; CARRY REG		p. 16 p. 40	⁻; CARRY REGister The Carry Out status register.
DIS PANEL		p. 34 p. 35 p. 38 p. 7	DISable PANEL Indicates the state of the ENABLE TCP switch.
Q_{15} SLI/SRO		p. 2	Q15 Shift Left Input/Shift Right Output Input to Q-shifter.
R_{15} SLI/SRO		p. 2	R15 Shift Left Input/Shift Right Output Input to Register-shifter.
⁻; SKIP		p. 15	⁻; SKIP Output from the SKIP condition decoder.
⁻; SWAP EN		p. 10	⁻; SWAP ENable Connects Ro SRI/SLO to R_{15} SLI/SRO, and ALU COUT to CIN.
GATE APL DATA		p. 22	GATE Automatic Program Load DATA



790131 BJ 790131 ABP

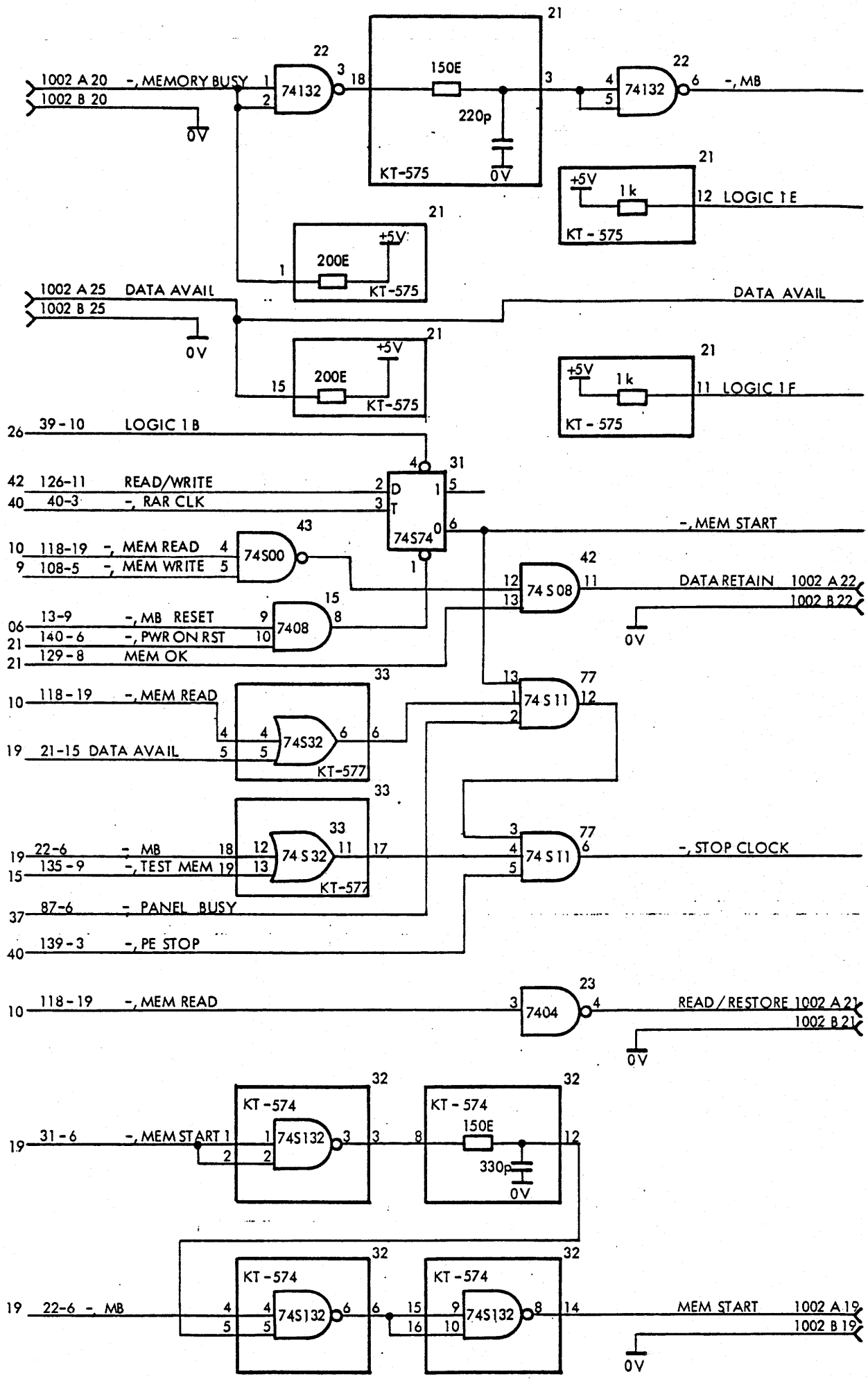
CPU 720

A13643

ALU = 0 F/F AND CARRY LINK F/F
SKIP DECODER
SHIFT LEFT/RIGHT SERIAL INPUT
LOGIC DIAGRAM

CPU 018

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
DATA AVAIL		p. 19	DATA AVAILable Indicates that data is ready from memory during a read cycle.
DATA RETAIN		1002	DATA RETAIN Used to disable memory start when not in use.
LOGIC 1E		p. 22 p. 31 p. 37	LOGIC 1E
LOGIC 1F		p. 37 p. 40	LOGIC 1F
⁻; MB		p. 19 p. 6	⁻; Memory Busy Indicates that memory is not ready to accept a new memory start.
MEM START		1002	MEMory START Starts the memory with a Read or Write cycle.
READ/RESTORE		1002	READ/RESTORE Indicates to memory that the requested cycle should be a Read.
⁻; STOP CLOCK		p. 21	⁻; STOP CLOCK Used to stop the microprogram if: Parity Error stop occurs, Memory not ready, or panel busy.



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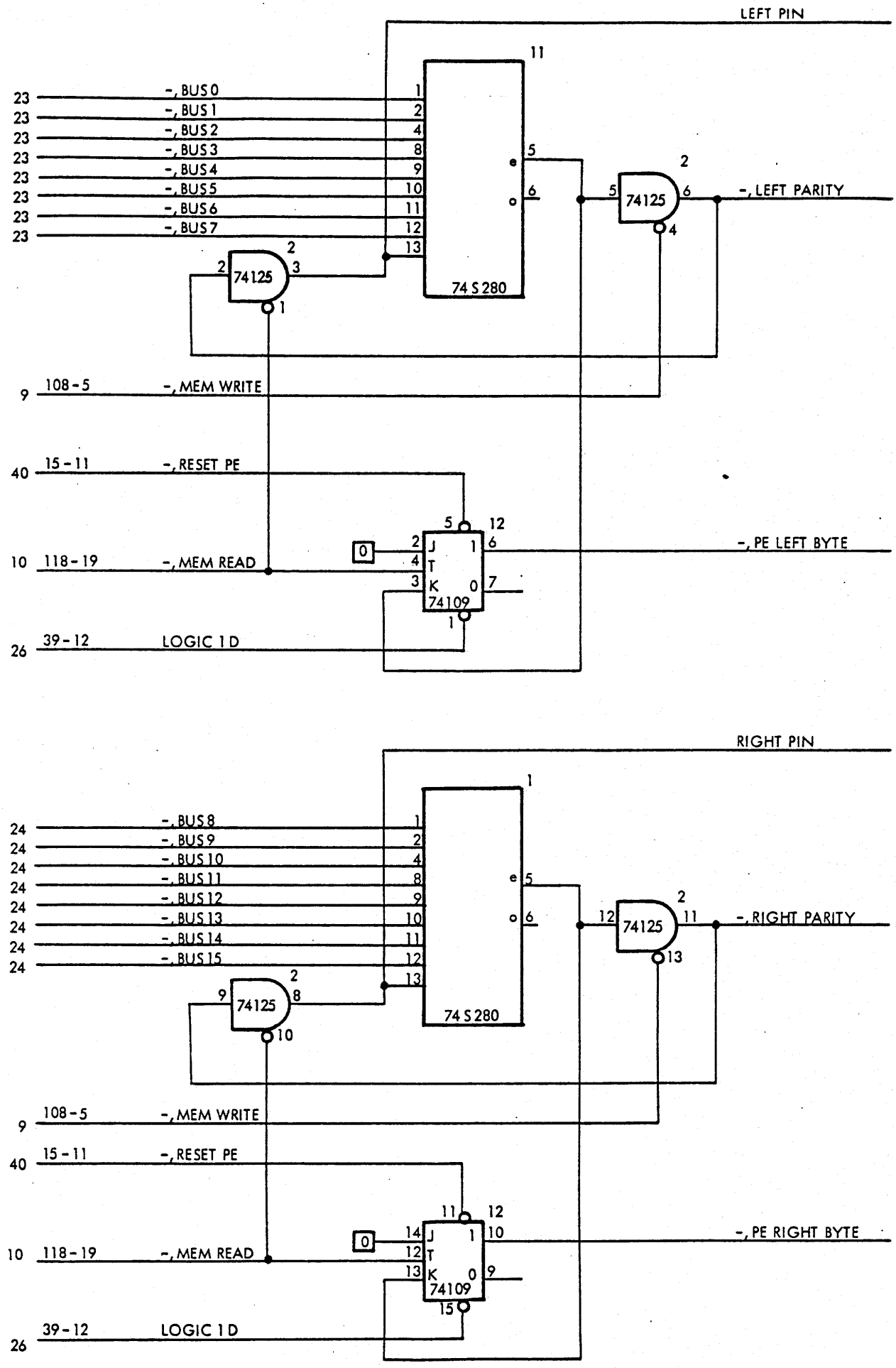
CPU 720

A13644

MEMORY INTERFACE
CONTROL LOGIC
LOGIC DIAGRAM

CPU 019

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
~; LEFT PARITY		p. 26	~; LEFT PARITY bit Left parity bus to or from memory.
LEFT PIN		p. 26	LEFT Parity INput Received left parity bit during a Read cycle.
~; PE LEFT BYTE		p. 40	~; Parity Error LEFT BYTE LEFT BYTE Parity Error Buffer.
~; PE RIGHT BYTE		p. 40	~; Parity ERROR RIGHT BYTE RIGHT BYTE Parity Error Buffer.
~; RIGHT PARITY		p. 26	~; RIGHT PARITY bit Right parity bus to or from memory.
RIGHT PIN		p. 26	RIGHT Parity INput Received right parity bit during a Read cycle.



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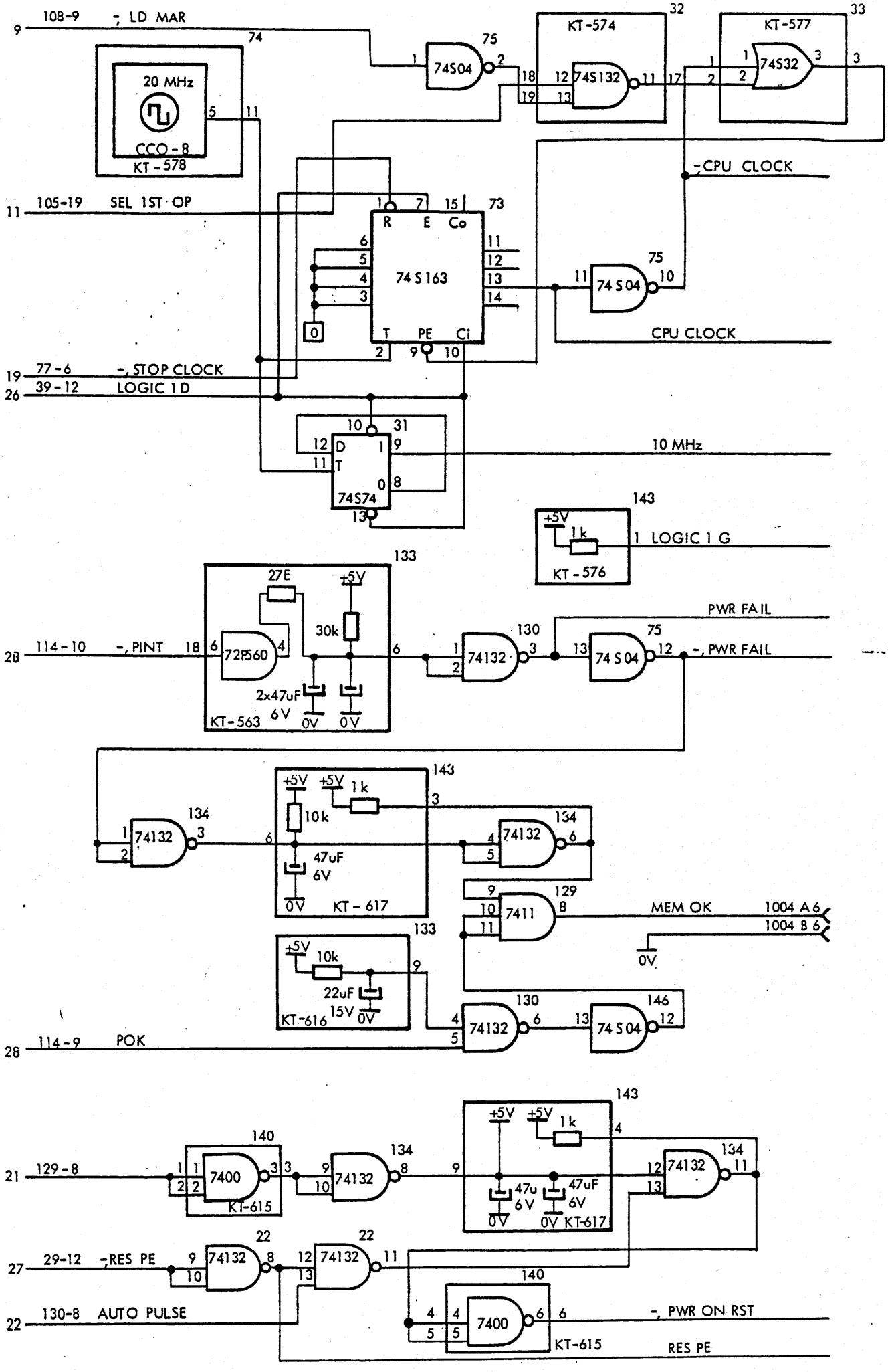
CPU 720

A13645

MEMORY INTERFACE
PARITY GENERATOR/CHECKER
LOGIC DIAGRAM

CPU 020

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
CPU CLOCK		p. 37	CPU CLOCK (frequency 6.6 MHz).
-; CPU CLOCK		p. 40	-; CPU CLOCK. Same as above.
LOGIC 1G		p. 33 p. 38	LOGIC 1 G.
MEM OK		p. 19 1004	MEMory power OK.
-; PWR FAIL		p. 33	-; PoWeR FAILure This signal will be the first to go low in the event of a power failure, approximately 1 to 2 msec. before MEM OK.
PWR FAIL		p. 33	
-; PWR ON RST		p. 19 p. 22 p. 35 p. 37 p. 38 p. 40	-; PoWeR ON ReSeT Used to reset the logic circuits after power is turned on.
10 MHZ		p. 35 p. 38 p. 6	10 MHZ clock.
RES PE		p.7	RESet Parity Error. Generates an restart address to the microprogram when the AUTO switch is activated while the Reset Parity Error switch is standing in the reset state.



CPU 720

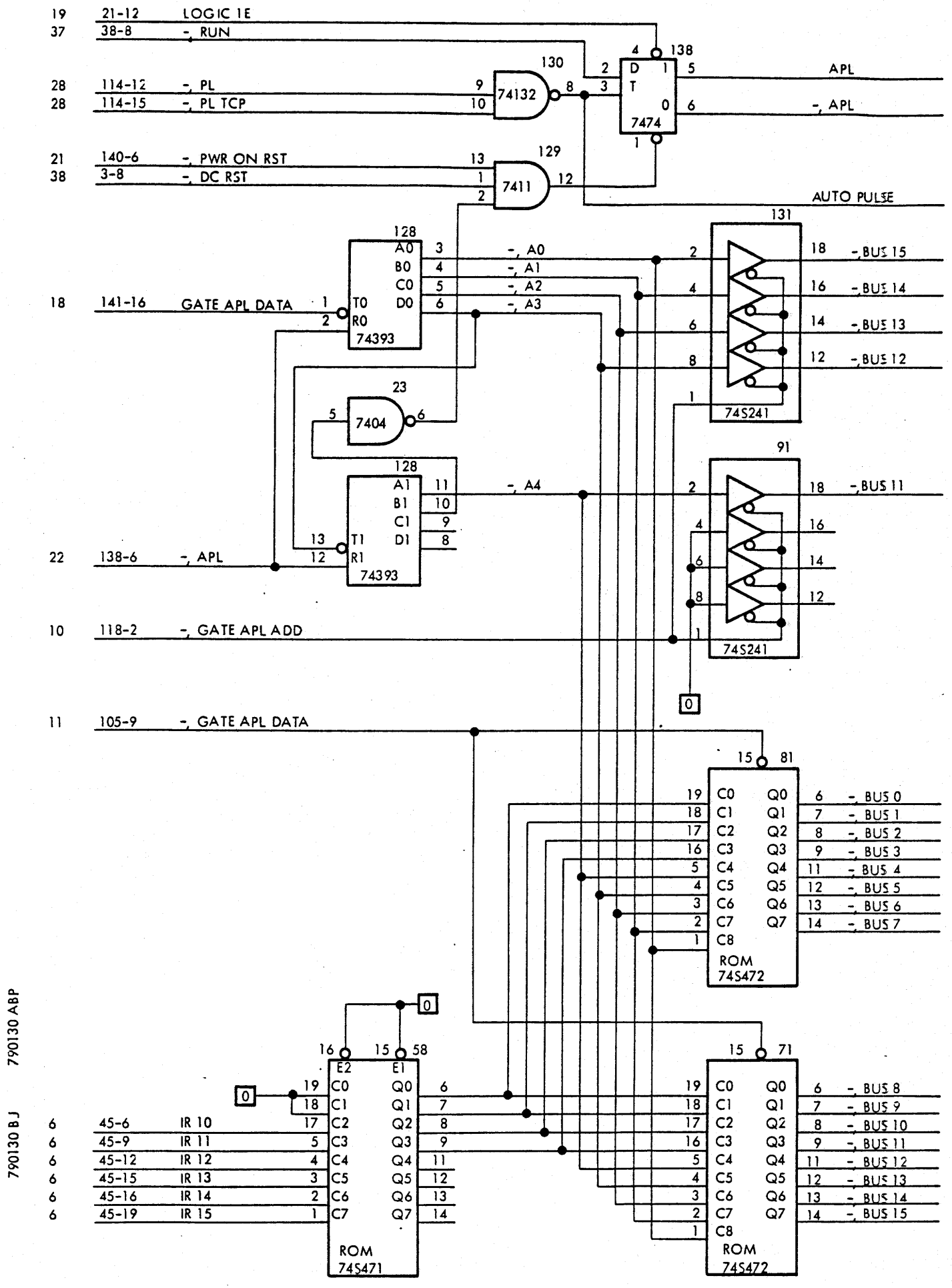
CLOCK GENERATOR AND POWER ON RESET
LOGIC DIAGRAM

CPU 021

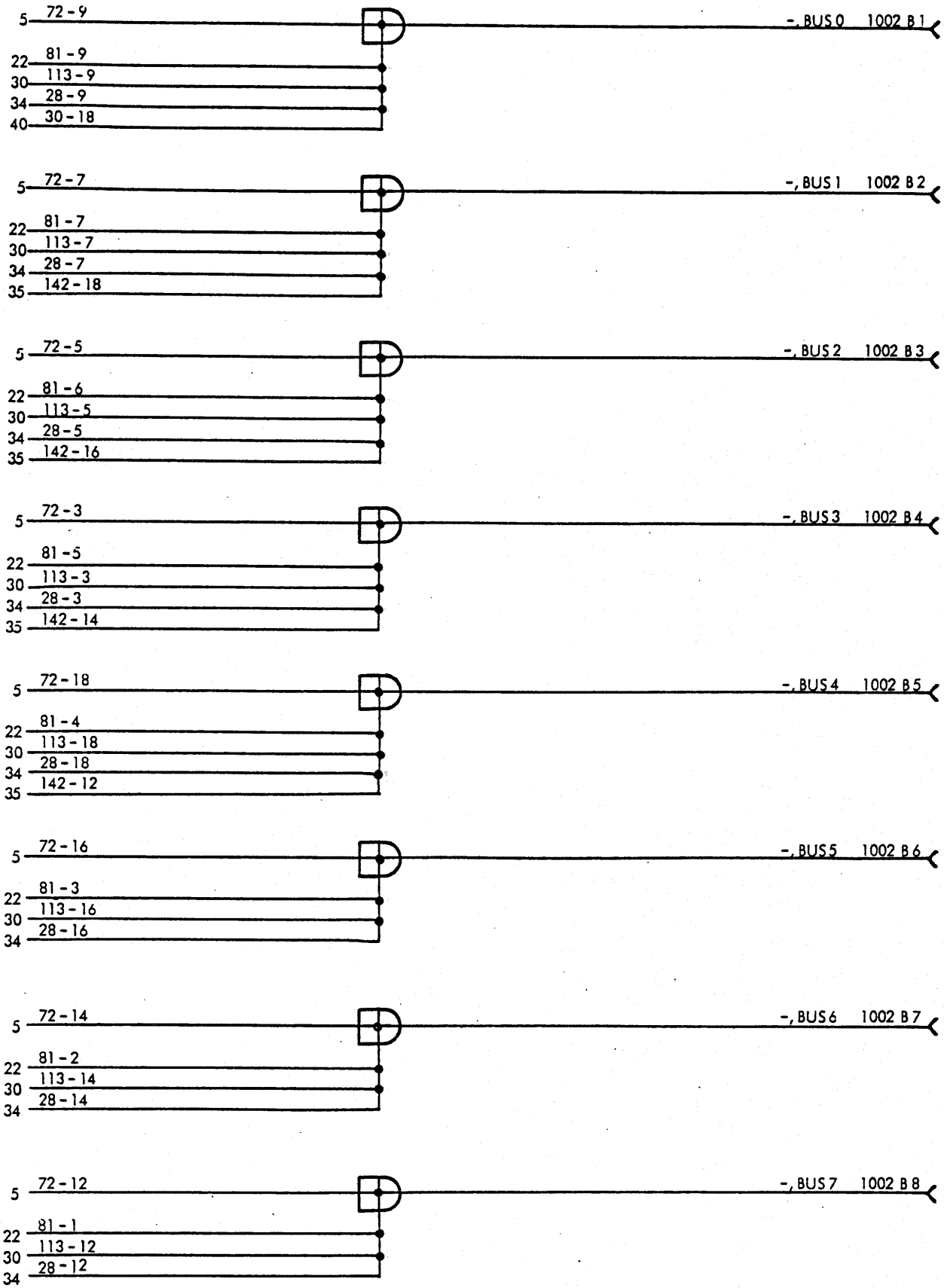
A13646

790131 BJ 790131 ABP

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
APL		p. 16	Automatic Program Load This signal is true the period taken to move the contents of the Auto-load Program proms into main memory location 0-37.
⁻; BUS 8-15		p. 24	⁻; internal BUS bit 8-15 On this logic Diagram is shown two sources on the internal data bus: 1. The autoload address counter. 2. The output from the Autoload Program memory (Right Byte).
⁻; BUS 0-7		p. 23	⁻; internal BUS bit 0-7 Output from the Autoload Program memory (Left Byte).
AUTO PULSE		p. 21	AUTO PULSE


19 21-12 LOGIC 1E
37 38-8 -, RUN
28 114-12 -, PL
28 114-15 -, PL TCP
130
74132
4 138
D 1
T
0
7474
APL
-, APL
21 140-6 -, PWR ON RST
38 3-8 -, DC RST
129
7411
AUTO PULSE
128
74393
18 141-16 GATE APL DATA
-, A0
-, A1
-, A2
-, A3
131
74S241
-, BUS 15
-, BUS 14
-, BUS 13
-, BUS 12
23
7404
128
74393
22 138-6 -, APL
-, A4
91
74S241
-, BUS 11
10 118-2 -, GATE APL ADD
11 105-9 -, GATE APL DATA
15 81
ROM
74S472
-, BUS 0
-, BUS 1
-, BUS 2
-, BUS 3
-, BUS 4
-, BUS 5
-, BUS 6
-, BUS 7
16 15 58
E2 E1
ROM
74S471
6 45-6 IR 10
6 45-9 IR 11
6 45-12 IR 12
6 45-15 IR 13
6 45-16 IR 14
6 45-19 IR 15
15 71
ROM
74S472
-, BUS 8
-, BUS 9
-, BUS 10
-, BUS 11
-, BUS 12
-, BUS 13
-, BUS 14
-, BUS 15
790130 ABP
790130 BJ

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
⁻, BUS 0-7		p. 3 p. 4 p. 20 p. 25 p. 30 p. 36 1002	⁻, internal BUS bit 0-7 The destination for the internal data bus is the ⁻, (BUS 1-10) = 0 Decoder, BUS inverter, parity checker/generator, I/O Data Bus drivers, and the Diagnostic Panel data bus.



790131 BJ 790131 ABP

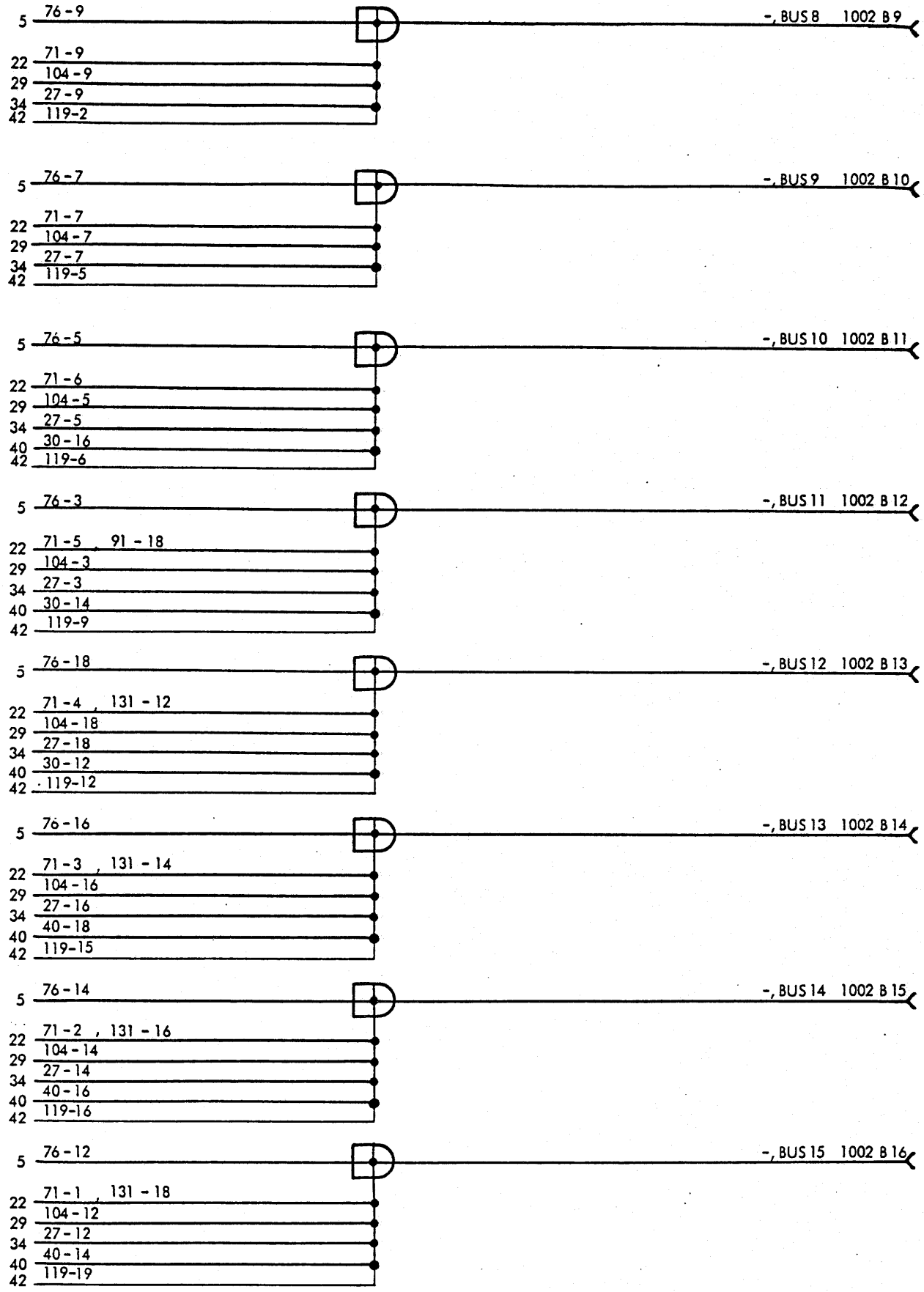
CPU 720

A13648

BUS WIRE OR BIT 0-7
LOGIC DIAGRAM

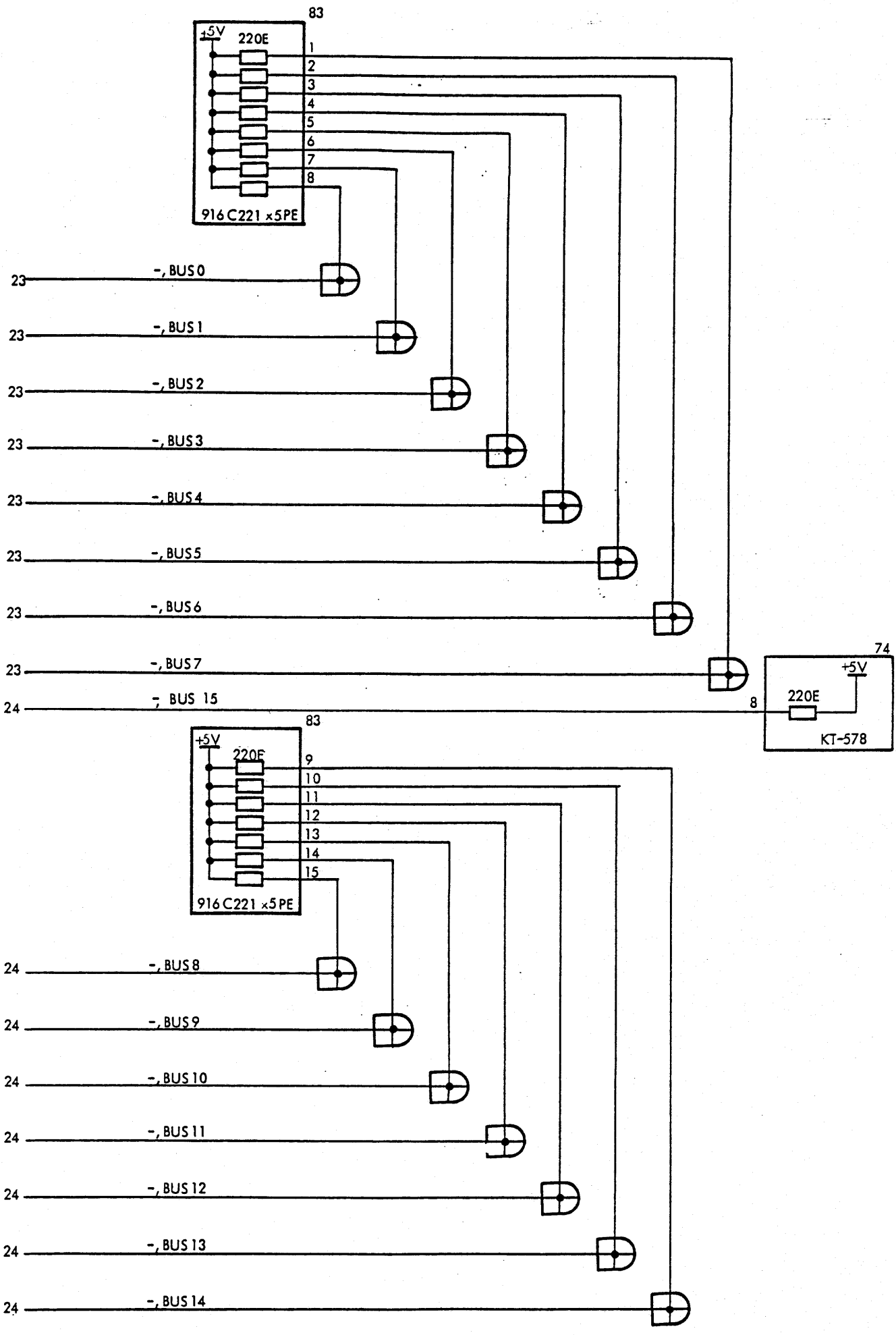
CPU 023

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
⁻, BUS 8-10		p. 3 p. 4 p. 20 p. 25 p. 29 p. 36 1002	⁻, Internal BUS bit 8-15 The destination for the internal data bus is the ⁻, (BUS 1-10) = 0 Decoder, BUS inverter, parity checker/generator, I/O Data Bus drivers and the Diagnostic Panel data bus.
⁻, BUS 11-15		p. 4 p. 20 p. 25 p. 29 p. 36 1002	



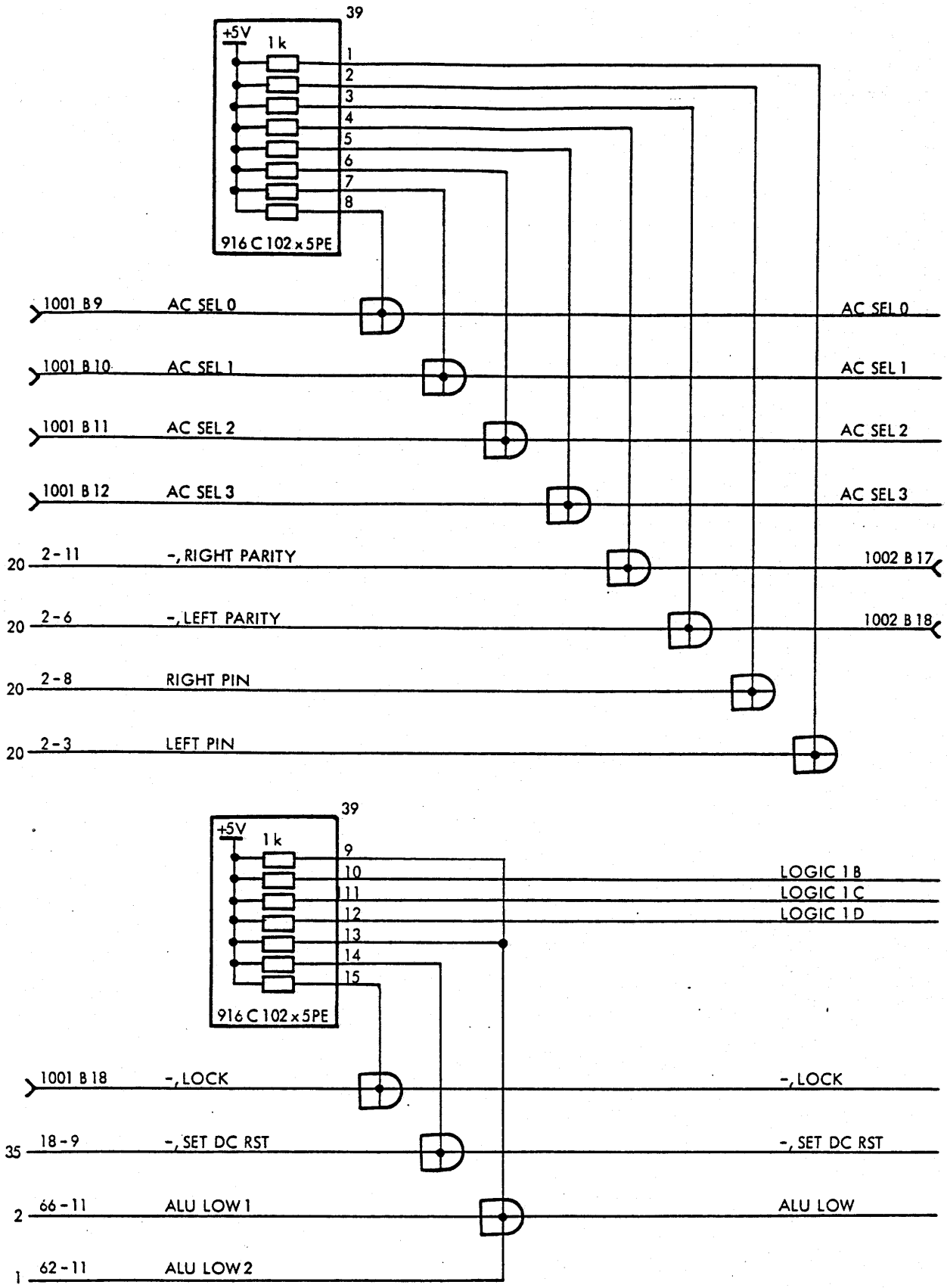
790131 BJ 790131 ABP

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION



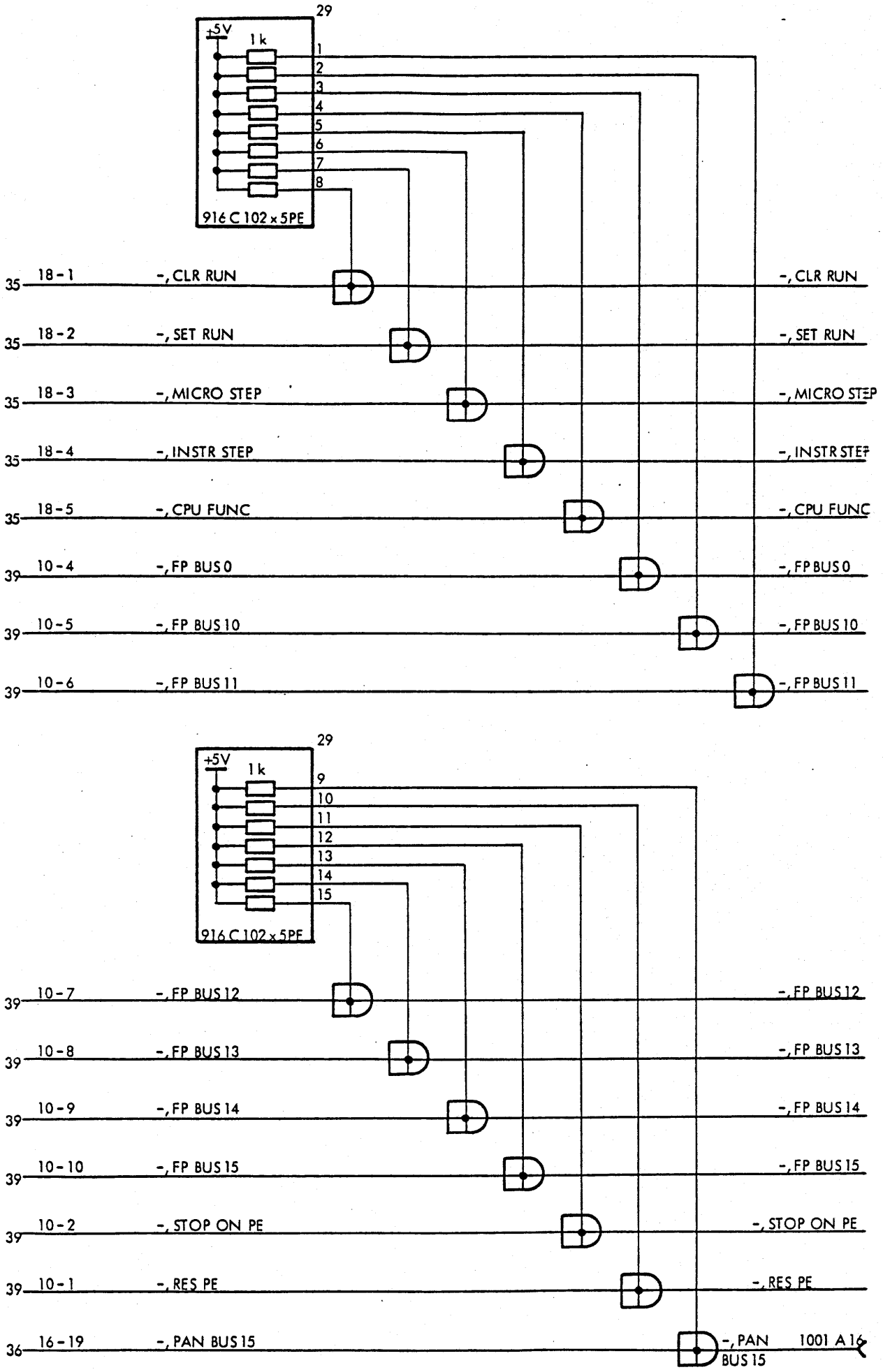
790131 BJ 790131 ABP

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
AC SEL 0-3		p. 35 1001	ACcumulator SELect bit 0-3 Register stack address from the Diagnostic Panel TCP 701.
ALU LOW		p. 18 p. 41 p. 42	ALU LOW Indicates that the output from the ALU contains all zeroes.
⁻, LEFT PARITY		1002	⁻, LEFT PARITY bit Left parity bus to or from memory.
⁻, LOCK		p. 7	⁻, LOCK The state of the POWER ON/LOCK switch on the Diagnostic Panel. If this switch is not mounted, the ⁻, LOCK signal is always logic high.
LOGIC 1 B		p. 16 p. 19 p. 31 p. 32	LOGIC 1 B.
LOGIC 1 C		p. 18	LOGIC 1 C.
LOGIC 1 D		p. 20 p. 21	LOGIC 1 D.
⁻, RIGHT PARITY		1002	⁻, RIGHT PARITY bit Right parity to or from memory.
⁻, SET DC RST		p. 38	⁻, SET DC ReSeT Used to generate IORST.
⁻, PAN BUS 15		p. 27	⁻, PANel BUS bit 15



790131 BJ 790131 ABP

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
⁻; CLR RUN		p. 37	⁻; CLeaR RUN Used to reset the RUN flip flop.
⁻; CPU FUNC		p. 37	⁻; CPU FUNCtion Indicates that the started Diagnostic Panel operation requires microprogram execution.
⁻; FP BUS 0, 10-15		p. 40 p. 39	⁻; Front Panel BUS bit 0, 10-15 Autoload information used when Diagnostic Panel is not connected or not enabled.
⁻; INSTR STEP		p. 37	⁻; INSTRuction STEP.
⁻; MICRO STEP		p. 37	⁻; MICROprogram STEP.
⁻; PAN BUS 15		1001	⁻; PANel data BUS 15.
⁻; RES PE		p. 40 p. 39 p. 21	⁻; RESet Parity Error Used to clear the Parity Error indicator register.
⁻; SET RUN		p. 37	⁻; SET RUN Sets the RUN flip flop.
⁻; STOP ON PE		p. 40 p. 39	⁻; STOP ON Parity Error Switches input from the CPU 708 Front Panel, determining whether the CPU should both indicate parity error and stop the microprogram execution, or the CPU should only indicate parity errors.



790131 BJ 790131 ABP

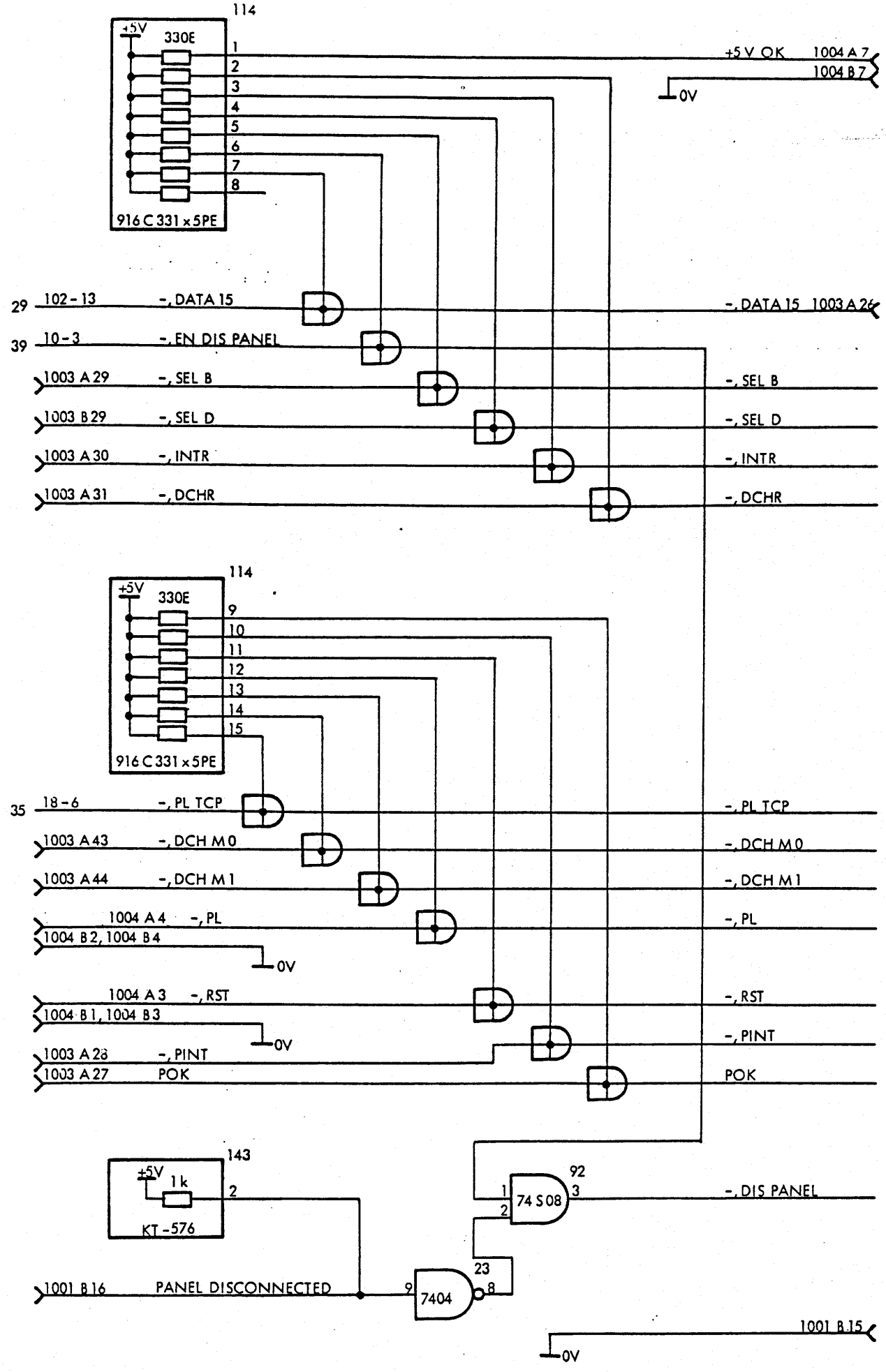
CPU 720

A13652

1k PULL UP CIRCUITS

CPU 027

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
⁻, DATA 15		1003	⁻, I/O DATA bus bit 15.
⁻, DCHM 0-1		p. 16	⁻, Data CHannel Mode bit 0-1.
⁻, DCHR		p. 16	⁻, Data CHannel Request.
⁻, DIS PANEL		p. 18 p. 34 p. 35 p. 37 p. 40 p. 41	⁻, DISable diagnostic PANEL.
⁻, INTR		p. 16 p. 33	⁻, INTerrupt Request.
⁻, PINT		p. 21	⁻, Power INTerrupt.
⁻, PL		p. 22	⁻, set Program Load.
⁻, PL TCP		p. 22	⁻, set Program Load from TCP.
POK		p. 21	Power OK.
⁻, RST		p. 35	⁻, ReSeT External signal to simulate the RESET button on the Diagnostic Panel.
⁻, SEL D		p. 33 p. 41	⁻, SELect Done The state of the DONE flip flop in the addressed I/O Device.
⁻, SEL B		p. 33	⁻, SELect Busy The state of the BUSY flip flop in the addressed I/O Device.



790131 BJ 790131 ABP

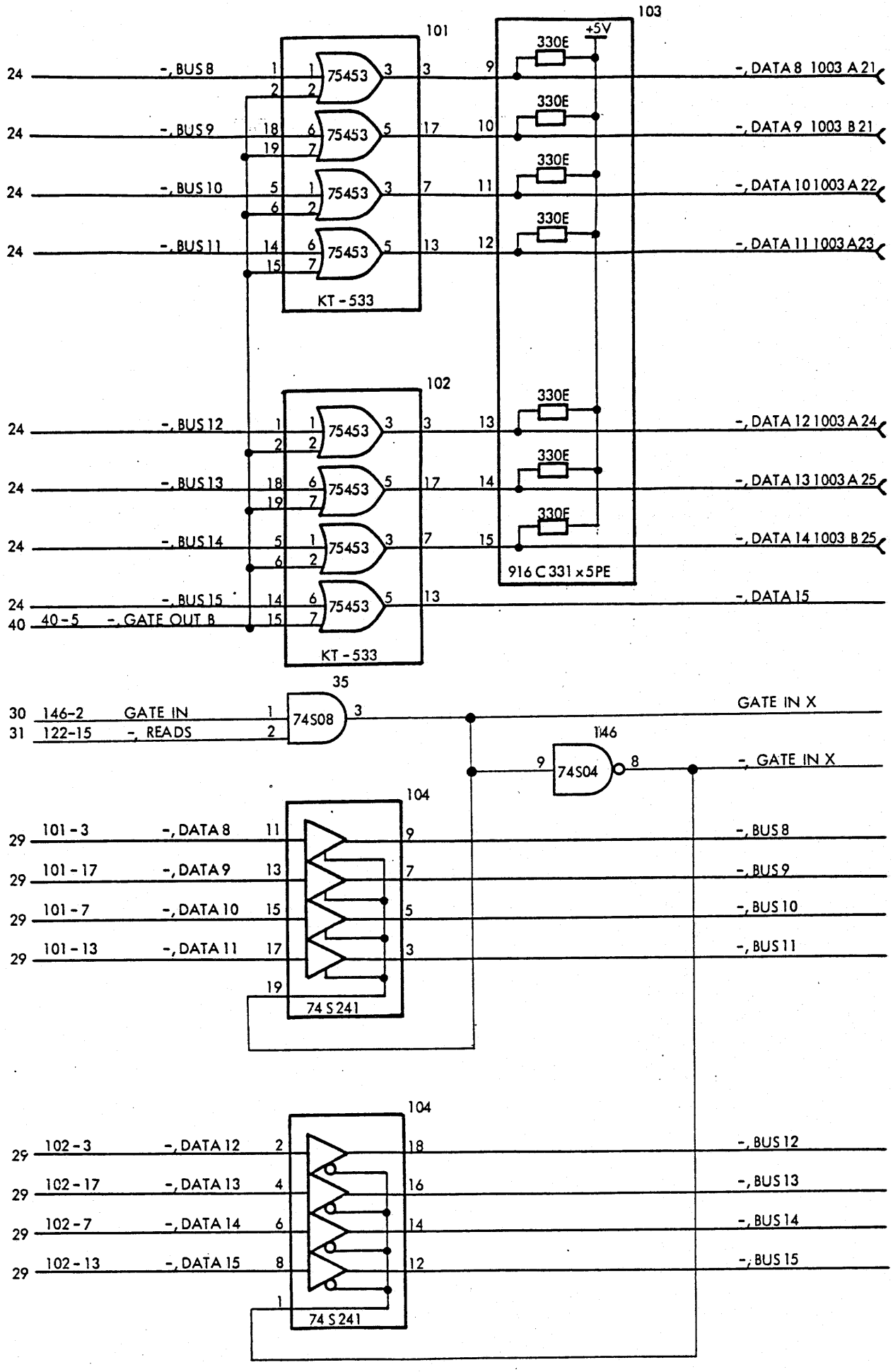
CPU 720

A13653

330E PULL UP CIRCUITS
LOGIC DIAGRAM

CPU 028

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
⁻; BUS 8-15		p. 24	⁻; internal BUS bit 8-15 The shown source on the internal BUS is the I/O Data Bus receivers.
⁻; DATA 8-14		1003	⁻; I/O DATA BUS bit 8-14.
⁻; DATA 15		p. 28	⁻; I/O DATA BUS bit 15.
GATE INX		p. 30	GATE INput Gates the contents on the I/O Data Bus out on the internal bus.
⁻; GATE INX		p. 30	



790131 BJ 790131 ABP

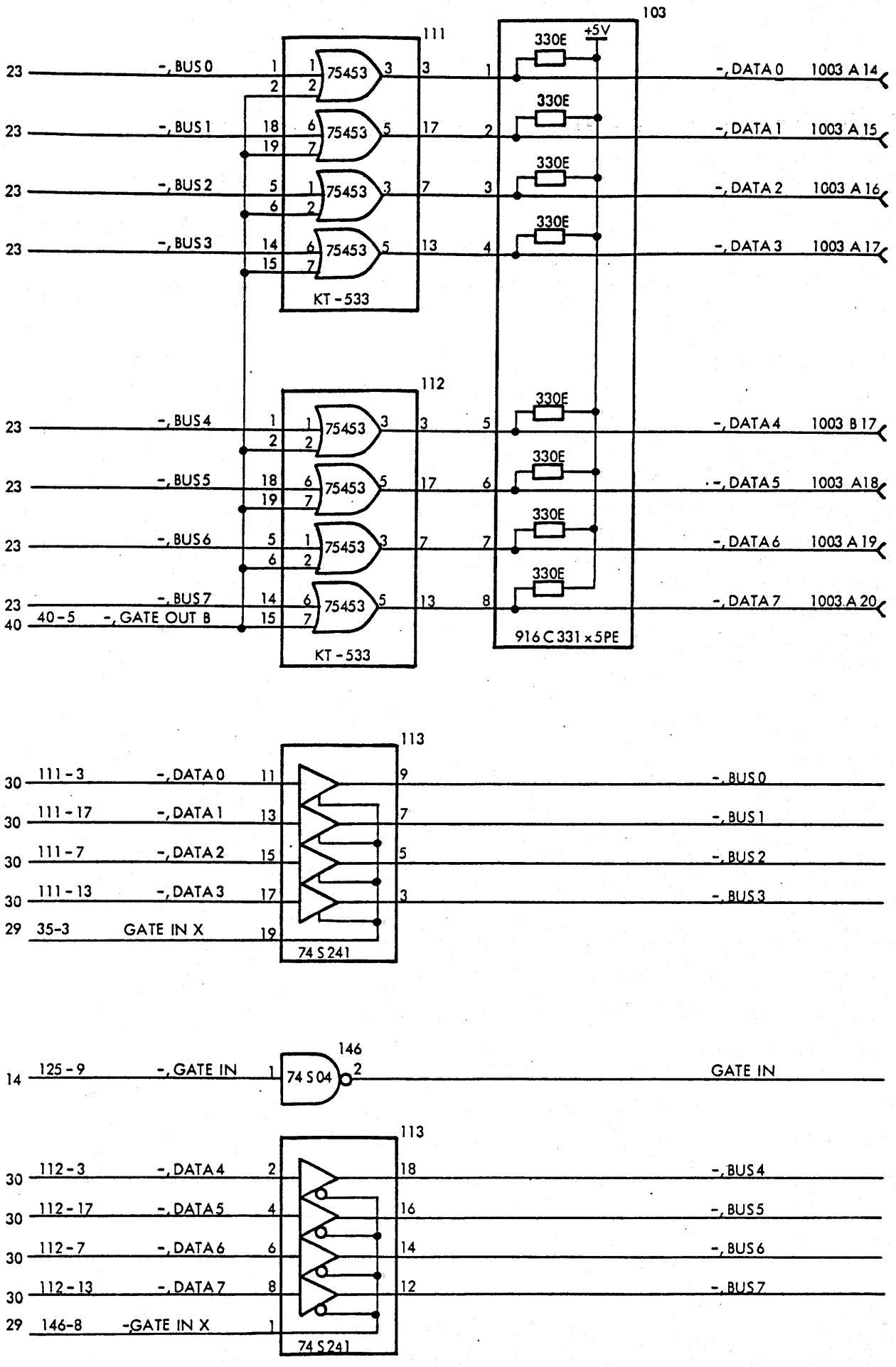
CPU 720

A13654

DATA BUS DRIVERS AND RECEIVERS
BIT 8-15
LOGIC DIAGRAM

CPU 029

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
⁻; BUS 0-7		p. 23	⁻; internal BUS bit 0-7 The shown source on the internal BUS is the I/O Data Bus Receivers.
⁻; DATA 0-7		1003	⁻; I/O DATA bus bit 0-7.
GATE IN		p. 29	GATE INput Gates the contents on the I/O Data Bus out on the internal bus.



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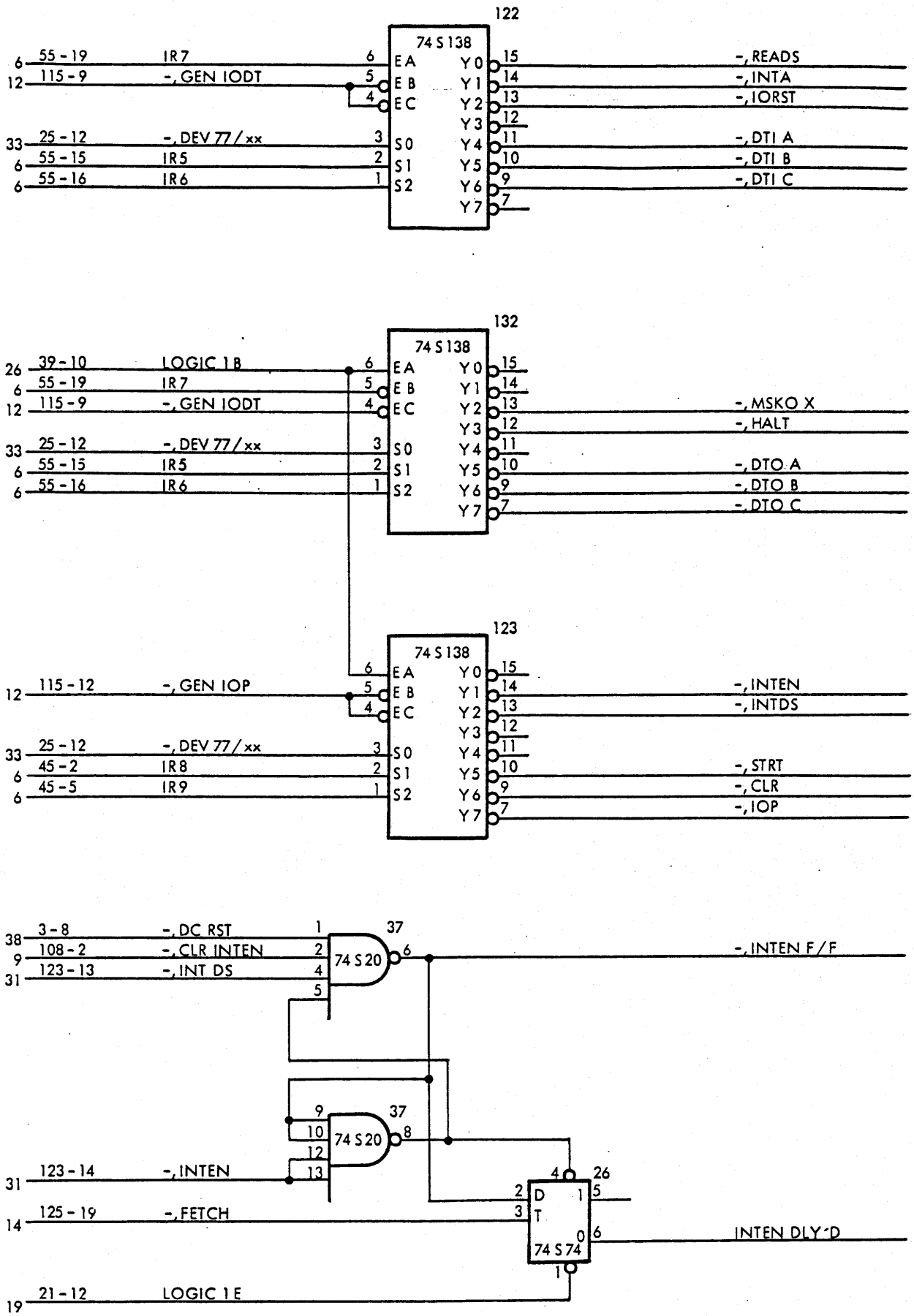
CPU 720

A13655

DATA BUS DRIVERS AND RECEIVERS
BIT 0 - 7
LOGIC DIAGRAM

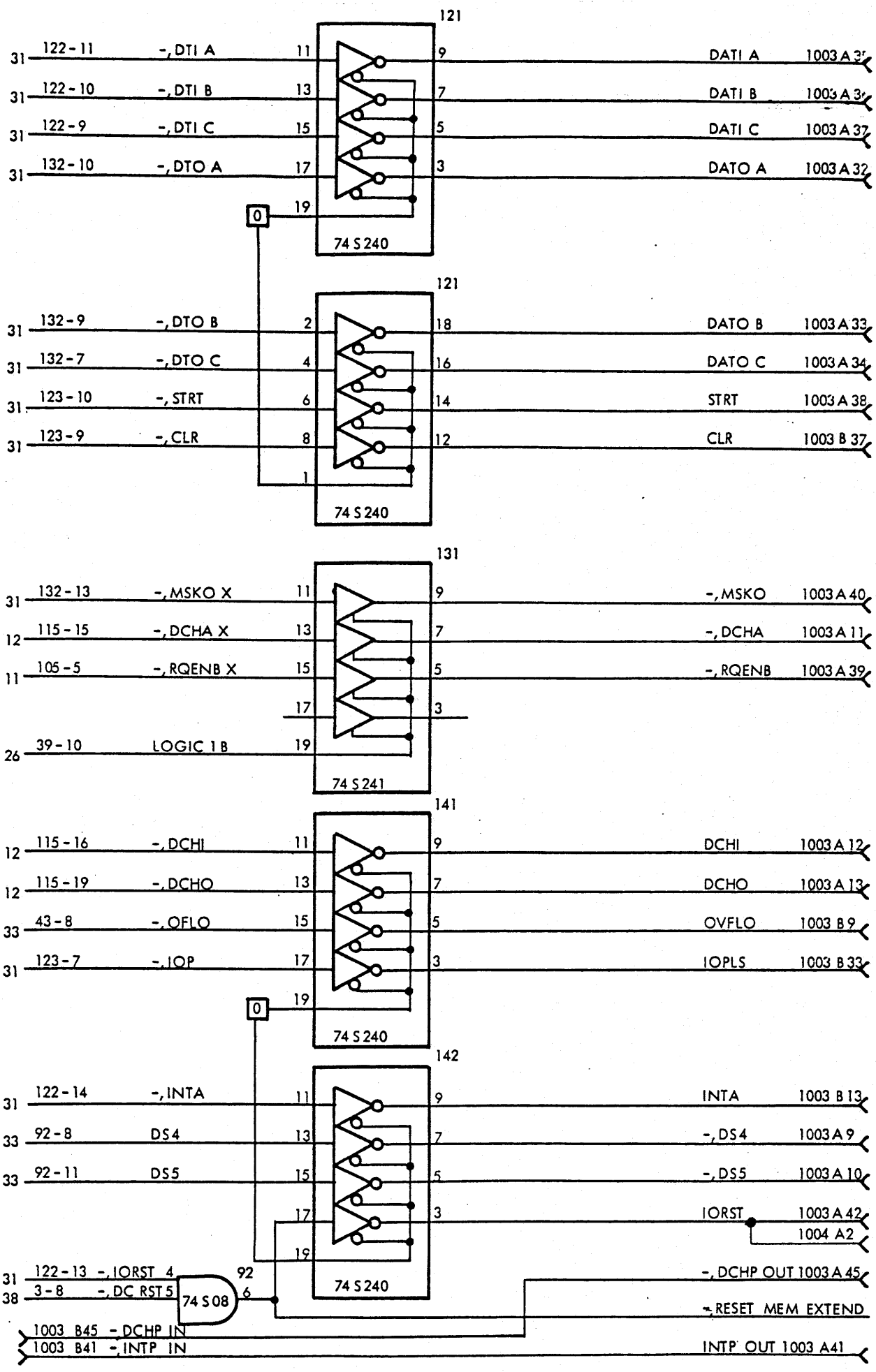
CPU 030

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
~, CLR		p. 32	~, CLeaR I/O control signal.
~, DTI A-C		p. 32	~, DaTa Input A-C I/O data input strobes.
~, DTO A-C		p. 32	~, DaTa Output A-C I/O Data output strobes.
~, HALT		p. 37	~, HALT Resets the RUN flip flop.
~, INTA		p. 32	~, INTerrupt Acknowledge Device address strobe.
INTEN DLY'D		p. 17	INTerrupt ENable DeLaY'D.
~, INTEN F/F		p. 40 p. 33	~, INTerrupt ENable Flip/Flop.
~, INTEN		p. 31	~, INTerrupt ENable Sets the INT. ENable flip flop.
~, INTDS		p. 31	~, INTerrupt DiSable Resets the INT. ENable flip flop.
~, IOP		p. 32	~, Input/Output Pulse I/O Control Signal.
~, IORST		p. 32	~, Input/Output ReSeT I/O control signal.
~, MSKO x		p. 32	~, MaSK Output x Strobes priority mask out on the I/O Data BUS.
~, READ S		p. 34 p. 29	~, READ Switches BUS:= Data Switches.
~, STRT		p. 32	~, STaRT I/O control signal.



790131 BJ 790131 ABP

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
CLR		1003	CLeaR.
DATI A-C		1003	DATa Input A-C.
DATAO A-C		1003	DATa Output A-C.
~ DCHA		1003	~ Data CHannel Acknowledge.
DCHI		1003	Data CHannel Input.
DCHO		1003	Data CHannel Output.
~ DCHP OUT		1003	~ Data CHannel Priority OUT.
~ DS 4-5		1003	~ Device Select bit 4-5.
INTA		1003	INTerrupt Acknowledge.
~ INTP OUT		1003	~ INTerrupt Priority OUT.
IOPLS		1003	Input/Output PuLSe.
IORST		1003	Input/Output ReSeT.
~ MSKO		1003	~ MaSK Output.
OVFLO		1003	OVerFLOw.
~ RESET MEM EXTEND		p. 41	~ RESET MEMory EXTEND flip flop.
~ RQENB		1003	~ ReQuest ENaBle.
STRT		1003	STaRT.



790131 BJ 790131 ABP

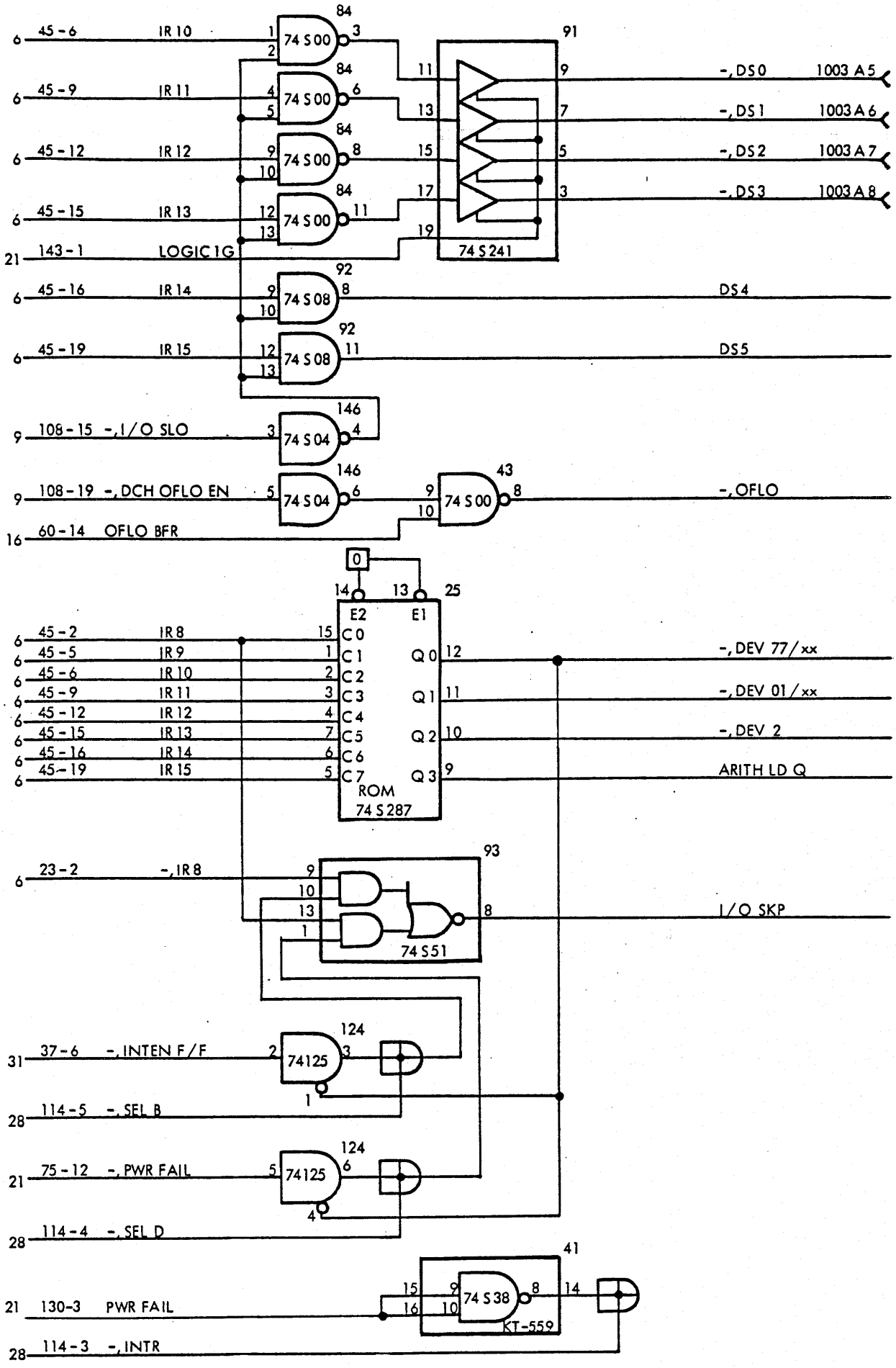
CPU 720

BUS CONTROL SIGNAL DRIVERS
LOGIC DIAGRAM

CPU 032

A13657

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
ARITH LD Q		p. 15	ARITHmetic LoaD Q Determines whether the ALU result is loaded into Q or the Destination Accumulator.
-, DEV 01/xx		p. 17 p. 41	-, DEVice 01/xx.
-, DEV 77/xx		p. 17 p. 31 p. 33	-, DEVice 77/xx.
-, DEV 2		p. 42	-, DEVice 2.
DS 5-4		p. 32	Device Select 5-4, see below.
-, DS 3-0		1003	-, Device Select bit 3-0 Device address out on the I/O Bus.
INTPO		p. 32	INTerrupt Priority Out.
I/O SKP		p. 18	Input/Output SKiP condition Tests the state of DONE or BUSY depending upon IR 8.
-, OFLO		p. 32	-, OverFLOw Overflow status to the Data Channel.



790131 BJ 790131 ABP

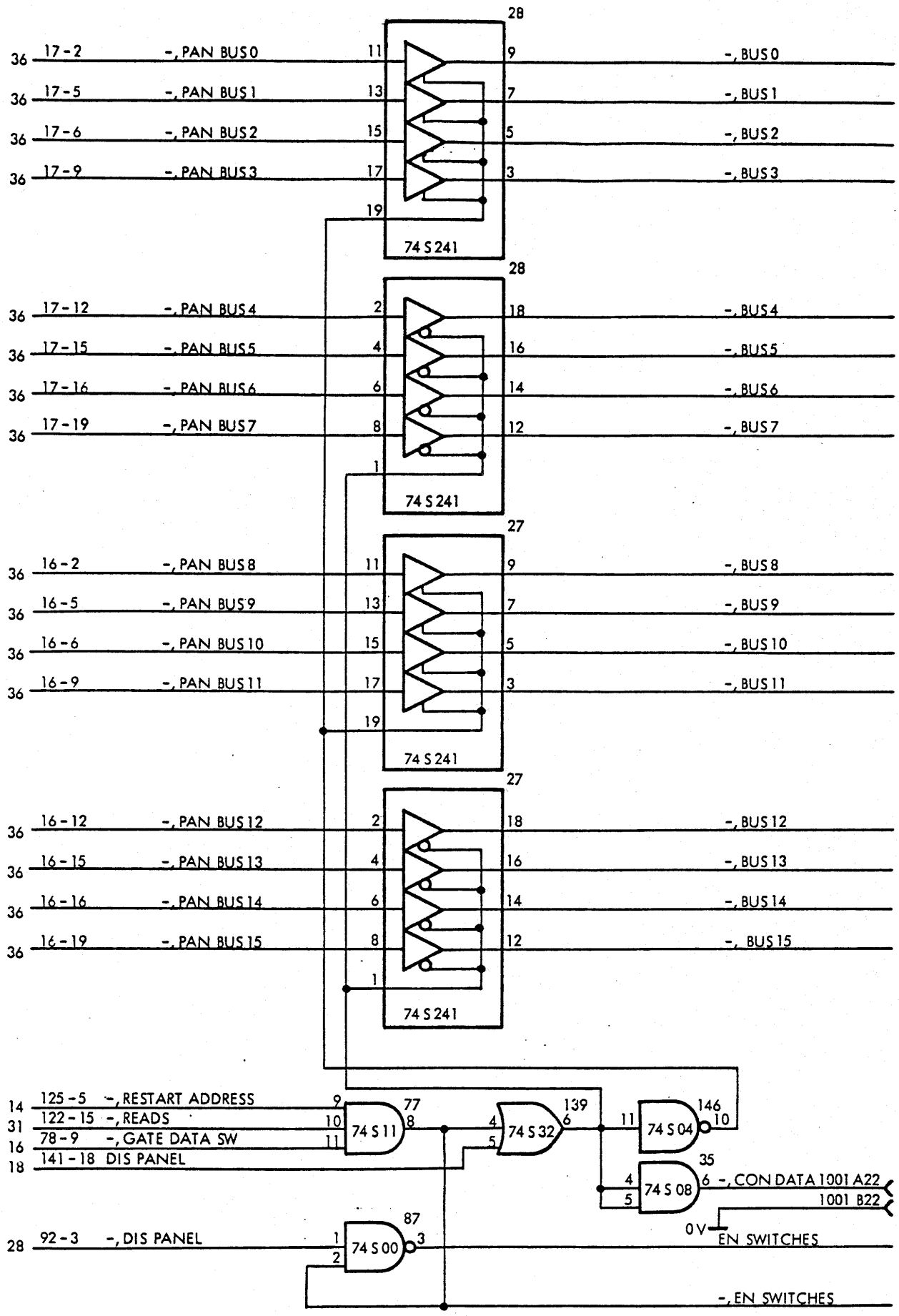
CPU 720

A13658

BUS ADDRESS LINE DRIVERS
POWER FAIL INTERRUPT CIRCUIT
LOGIC DIAGRAM

CPU 033

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
⁻, BUS 0-7		p. 23	⁻, internal BUS bit 0-7 The shown source on the Bus is the Diagnostic Panel Bus Receivers.
⁻, BUS 8-15		p. 24	⁻, internal BUS bit 8-15 See above.
⁻, CON DATA		1001	⁻, CONtrol DATA Used to disable the data switches in the Diagnostic Panel from the ⁻, PAN BUS.
EN SWITCHES		p. 36	ENable SWITCHES Disables the Data Register from the ⁻, PAN BUS, during read switches.
⁻, EN SWITCHES		p. 40	⁻, ENable SWITCHES Same as above.



790131 ABP

790131 BJ

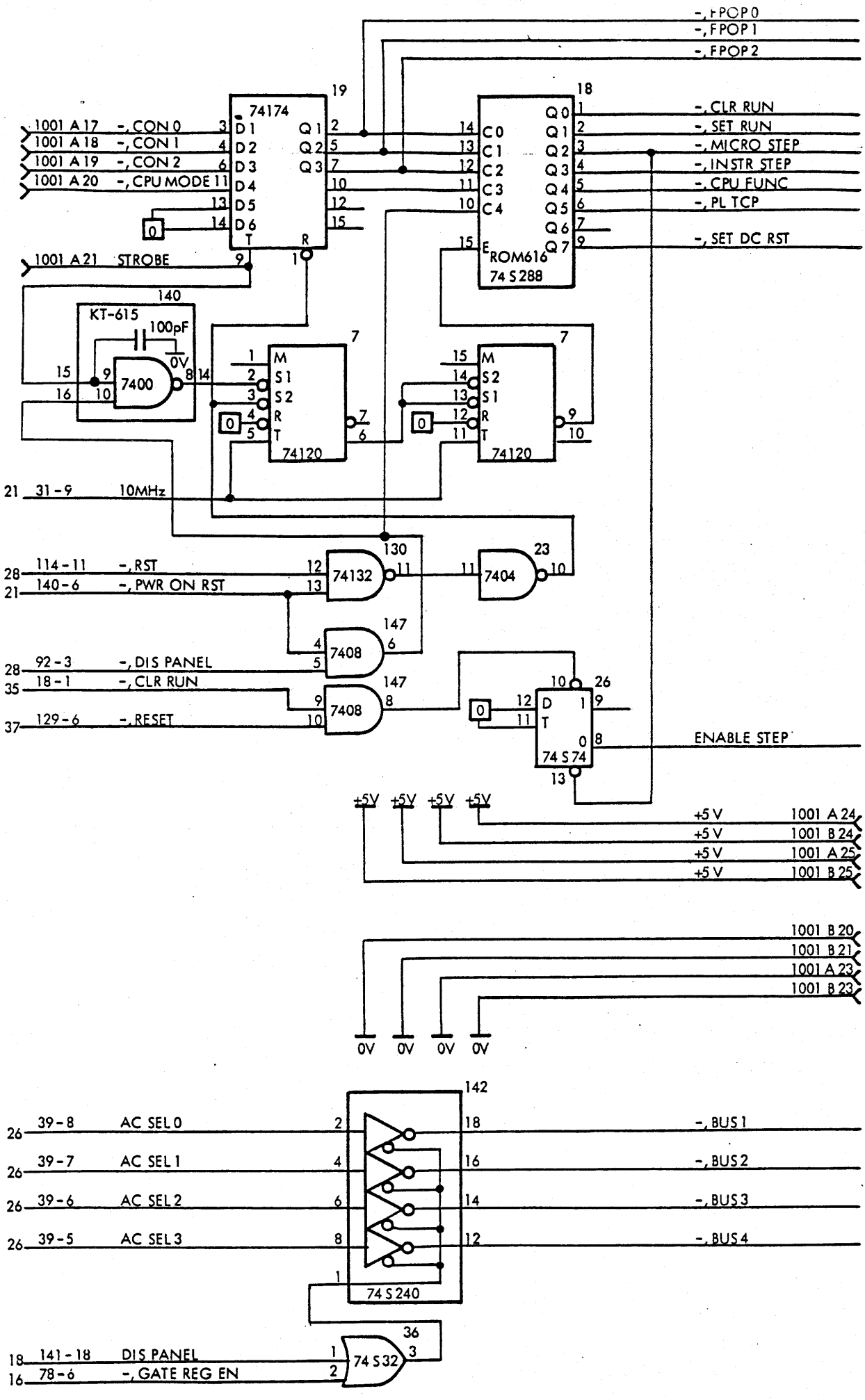
CPU 720

A13669

SERVICE PANEL DATA BUS RECEIVERS
LOGIC DIAGRAM

CPU 034

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
~ BUS 1-4		p. 23	~ internal BUS bit 1-4 This source on the internal bus is the AC SEL switches on the Diagnostic Panel.
~ CLR RUN		p. 27 p. 37	~ CLeaR RUN.
~ CPU FUNC		p. 27 p. 37	~ CPU FUNCtion Diagnostic Panel operation which requires microprogram execution.
ENABLE STEP		p. 37	ENABLE STEP.
~ FPOP 0-2		p. 16	~ Front Panel OPeration bit 0-2 The value on these lines determines the operation requested from the Diagnostic Panel.
~ INSTR STEP		p. 27 p. 37	~ INSTRuction STEP.
~ MICRO STEP		p. 27 p. 37	~ MICROinstruction STEP.
~ PL TCP		p. 28	~ set Program Load from TCP.
~ SET DC RST		p. 26 p. 38	~ SET DC ReSeT Used to generate IORST.
~ SET RUN		p. 27 p. 37	~ SET RUN Sets the RUN flip flop.



790131 BJ 790131 ABP

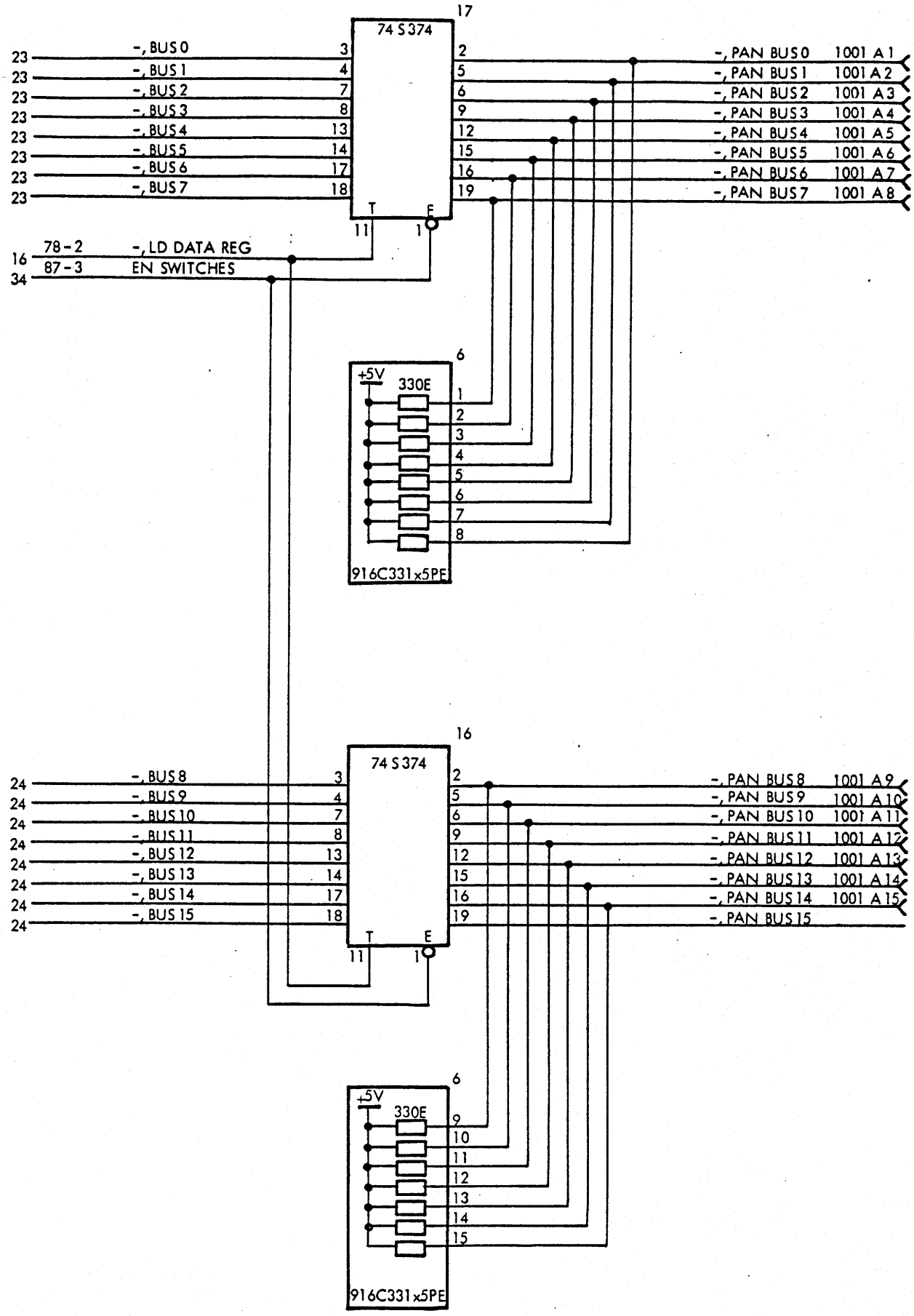
CPU 720

A13660

FRONT PANEL CONTROL DECODER
ACCUMULATOR SELECT RECEIVERS AND GATES
LOGIC DIAGRAM

CPU 035

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
⁻₇ PAN BUS 0-14		1001 p. 34	⁻₇ PANel BUS bit 0-14 Bidirectional data bus between the CPU and Diagnostic Panel. Transfers the information on the internal Data Bus out on the indicators in the Diagnostic Panel, TCP 701. Transfers the information on Diagnostic Panel data switches to the internal CPU Data Bus.
⁻₇ PAN BUS 15		p. 27 p. 34	⁻₇ PANel BUS bit 15 Same as above.



790131 BJ 790131 ABP

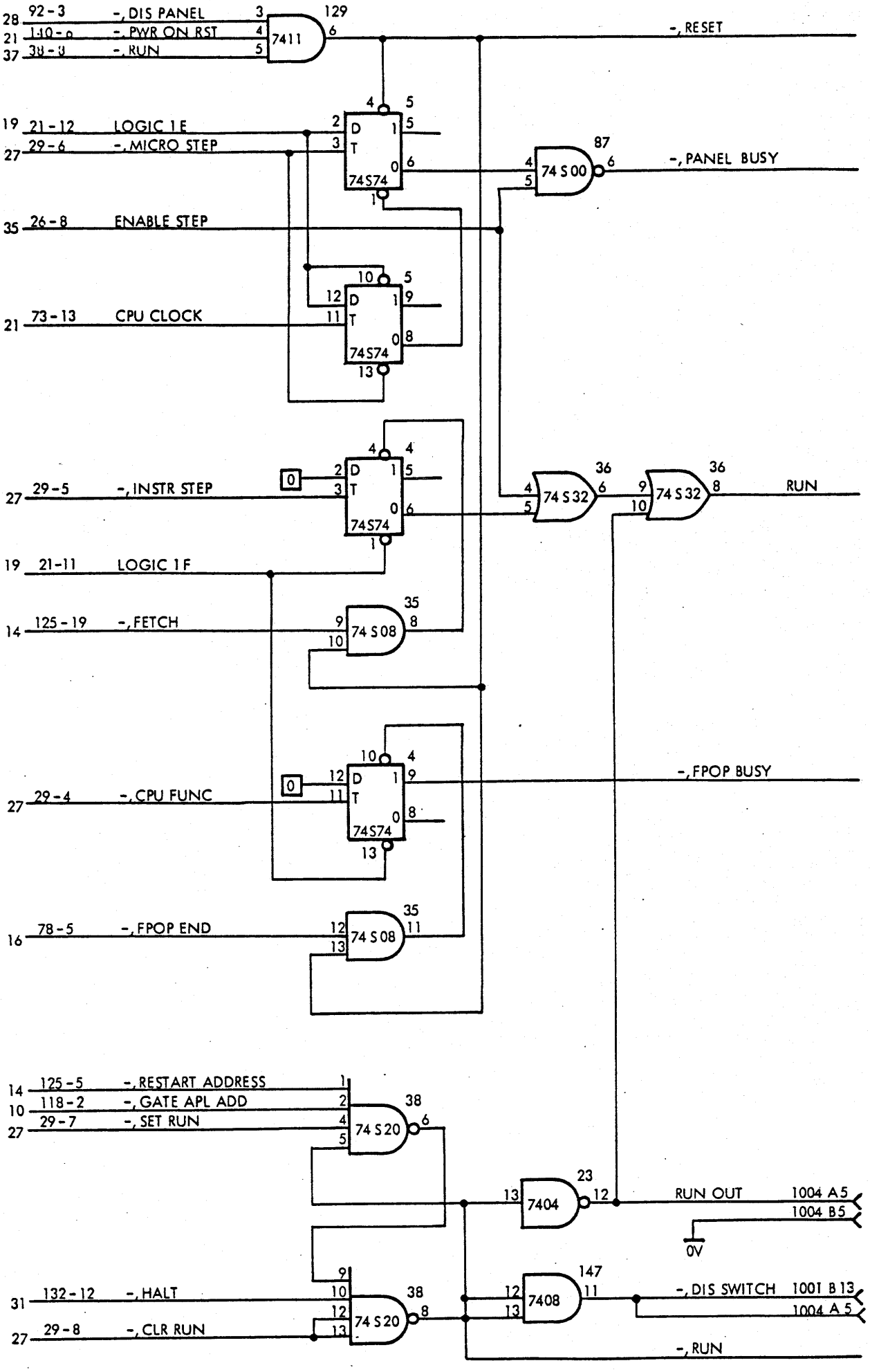
CPU 720

DATA BUS LATCH AND DRIVERS TO SERVICE PANEL
LOGIC DIAGRAM

CPU 036

A13661

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
-, DIS SWITCH		1001	-, DISable SWITCHes Used to disable the function switches on the Diagnostic Panel (not RESET, STOP) when the CPU is in the RUN state.
-, FPOP BUSY		p. 16	-, Front Panel OPeration BUSY Indicates that the Diagnostic Panel has requested an operation Reset by the microprogram when the current operation is terminated.
-, PANEL BUSY		p. 19	-, PANEL BUSY Indicates that an INSTR STEP or MICRO STEP is in progress.
-, RESET		p. 35	-, RESET
RUN		p. 41	RUN The RUN state of the CPU.
RUN OUT		1004	RUN OUTput.
-, RUN		p. 22	-, RUN.



790131 BJ 790131 ABP

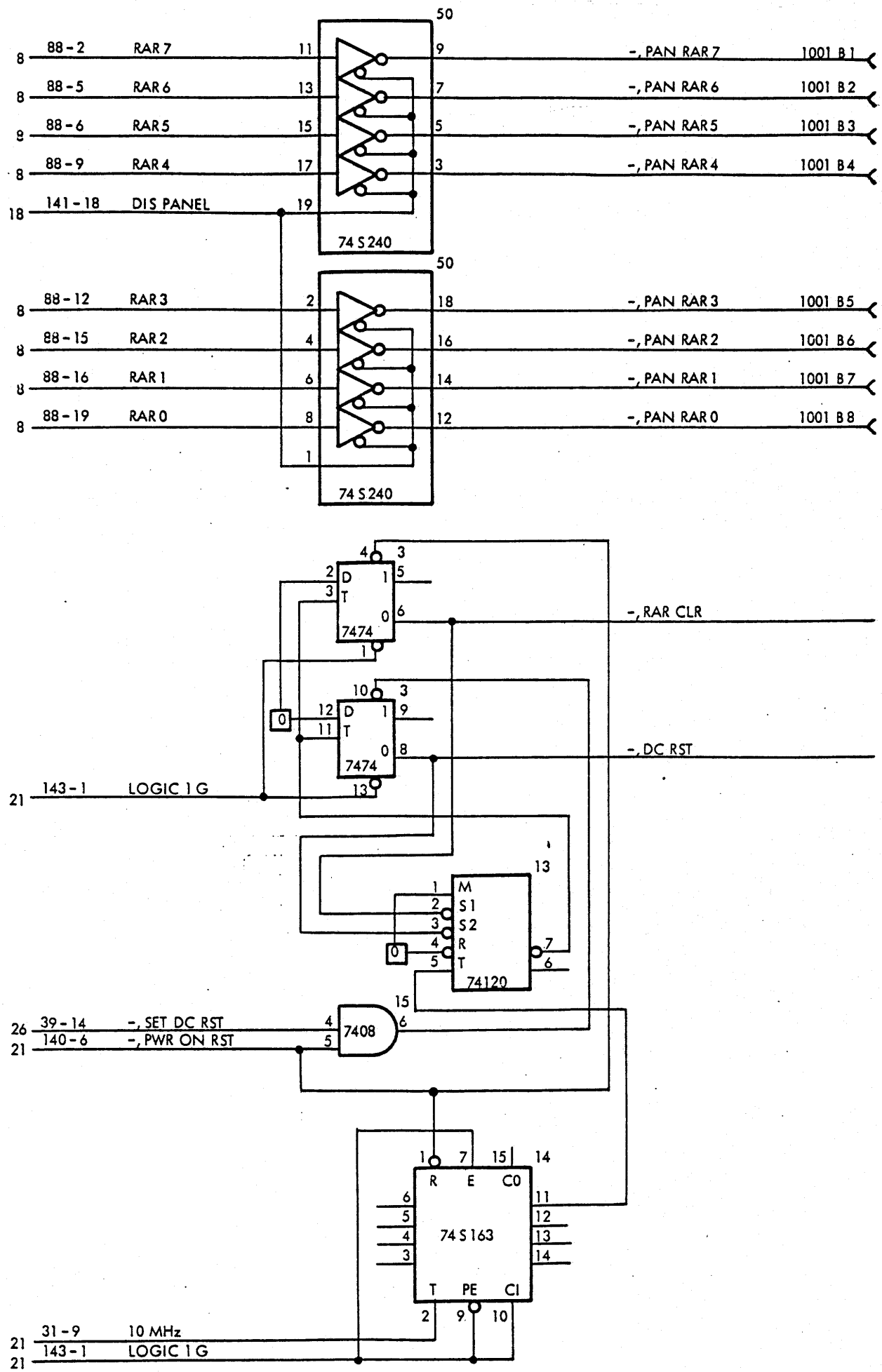
CPU 720

MICROSTEP - INSTRUCTIONSTEP - CPU PANEL FUNCTION
RUN/STOP F/F
LOGIC DIAGRAM

CPU 037

A13662

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
⁻; DC RST		p. 16 p. 22 p. 32 p. 31	⁻; DC ReSeT Clears the CPU and generates IORST.
⁻; PAN RAR 0-7		1001	⁻; PANel Rom Address Register bit 0-7 Output to drive indicators on the Diagnostic Panel.
⁻; RAR CLR		p. 41 p. 18	⁻; Rom Address Register CLeaR Generated after power on reset to determine the start address of the microprogram.



790131 BJ 790131 ABP

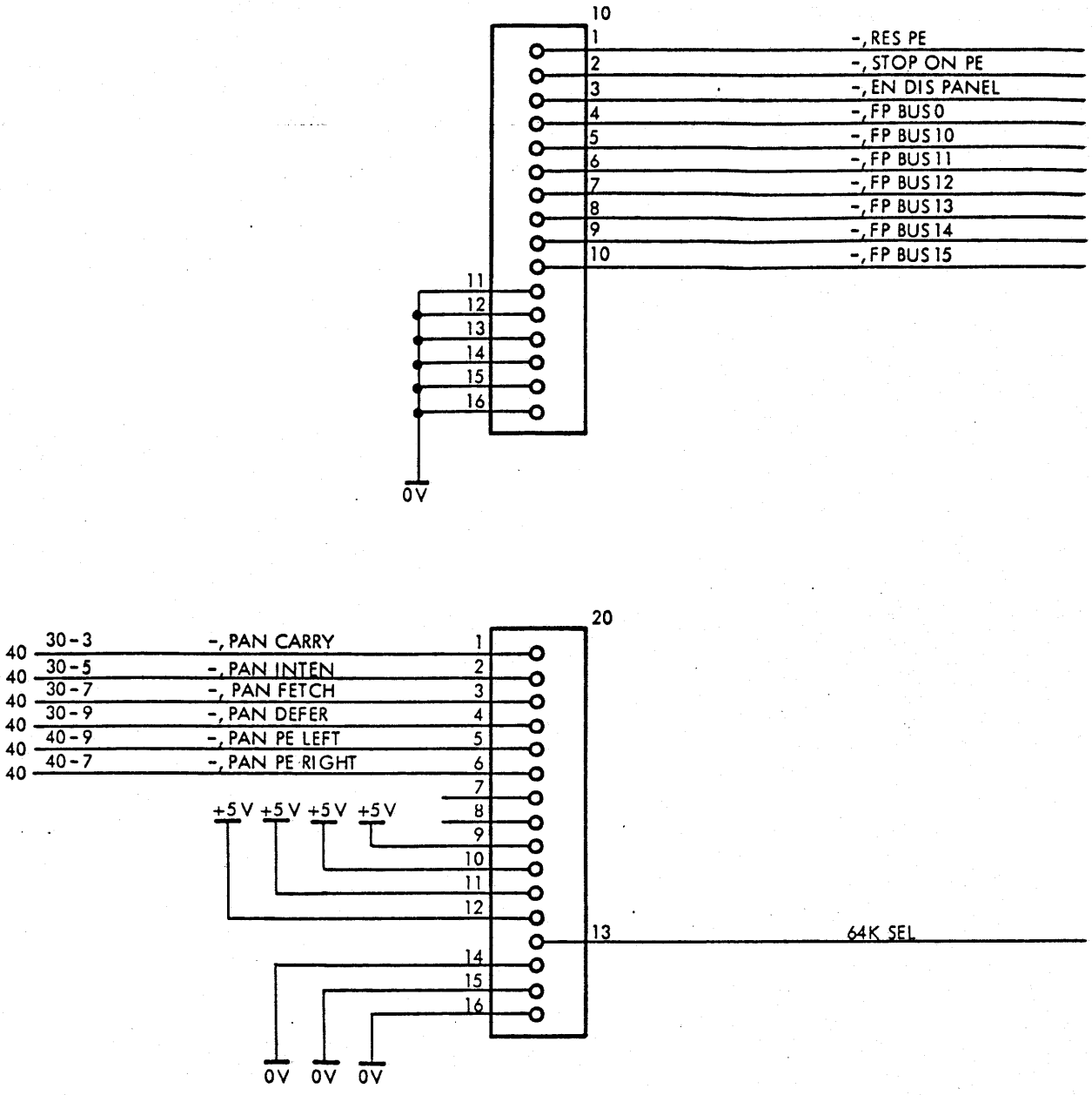
CPU 720

A13663

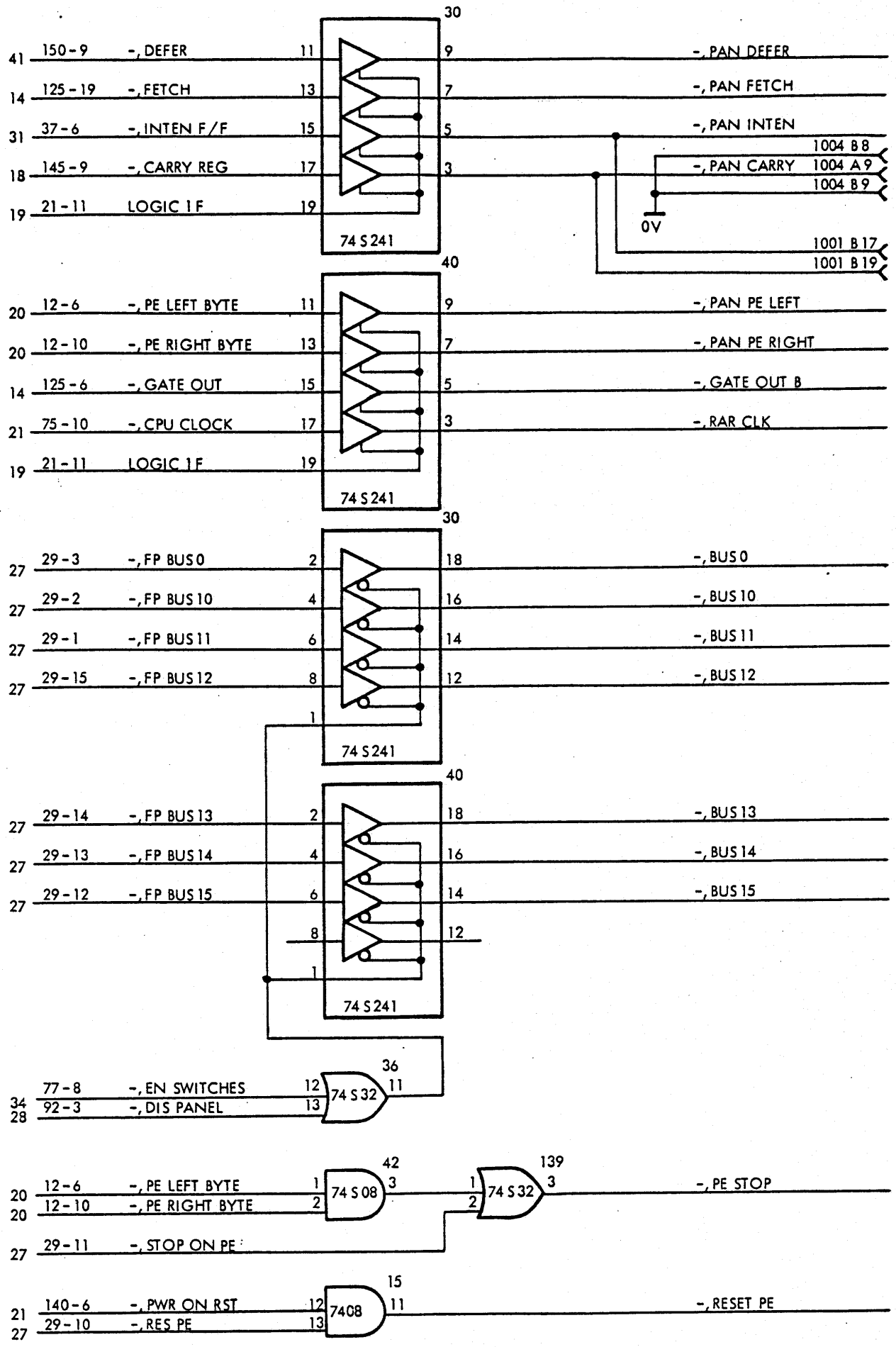
MICROADDRESS DRIVERS
POWER ON RESTART CIRCUIT
LOGIC DIAGRAM

CPU 038

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
⁻; EN DIS PAN		p. 28	⁻; ENable DISable PANel
⁻; FP BUS 0, 10-15		p. 27	⁻; Front Panel BUS bit 0, 10-15 Autoload information used when the Diagnostic Panel is not connected or not enabled.
⁻; RES PE		p. 27	⁻; RESet Parity Error Clears the Parity Error indicator register.
⁻; STOP ON PE		p. 27	⁻; STOP ON Parity Error Switches input from the CPU 708 Front Panel, determining whether the CPU should both indicate parity error and stop the micro-program execution or the CPU should only indicate parity errors.
64 K SEL		p. 41	64 K SELect Enables program setting of the memory extension flip flop.


10
1
2
3
4
5
6
7
8
9
10
-, RES PE
-, STOP ON PE
-, EN DIS PANEL
-, FP BUS 0
-, FP BUS 10
-, FP BUS 11
-, FP BUS 12
-, FP BUS 13
-, FP BUS 14
-, FP BUS 15
11
12
13
14
15
16
0V
20
40 30-3 -, PAN CARRY 1
40 30-5 -, PAN INTEN 2
40 30-7 -, PAN FETCH 3
40 30-9 -, PAN DEFER 4
40 40-9 -, PAN PE LEFT 5
40 40-7 -, PAN PE RIGHT 6
7
+5V +5V +5V +5V 8
9
10
11
12
13
64K SEL
14
15
16
0V 0V 0V

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
~ BUS 0		p. 23	~ internal BUS 0
~ BUS 10-15		p. 24	~ internal BUS 10-15 The data switches on the Front Panel gated out on the internal bus.
~ GATE OUT B		p. 29 p. 30	~ GATE OUTput Buffer Gates the contents on the internal bus out on the I/O Data Bus.
~ PAN CARRY		p. 39 1004 1001	~ PANel CARRY indicator.
~ PAN DEFER		p. 39	~ PANel DEFER indicator.
~ PAN FETCH		p. 39	~ PANel FETCH indicator.
~ PAN INTEN		p. 39 1001	~ PANel INTerrupt ENable indicator.
~ PAN PE LEFT		p. 39	~ PANel Parity Error LEFT byte indicator.
~ PAN PE RIGHT		p. 39	~ PANel Parity Error RIGHT byte indicator.
~ PE STOP		p. 19	~ Parity Error STOP.
~ RAR CLK		p. 1 p. 2 p. 8 p. 9 p. 10 p. 11 p. 12 p. 13 p. 14 p. 15 p. 16 p. 41 p. 42	~ Rom Address Register CLocK.
~ RESET PE		p. 20	~ RESET Parity Error indicator register.



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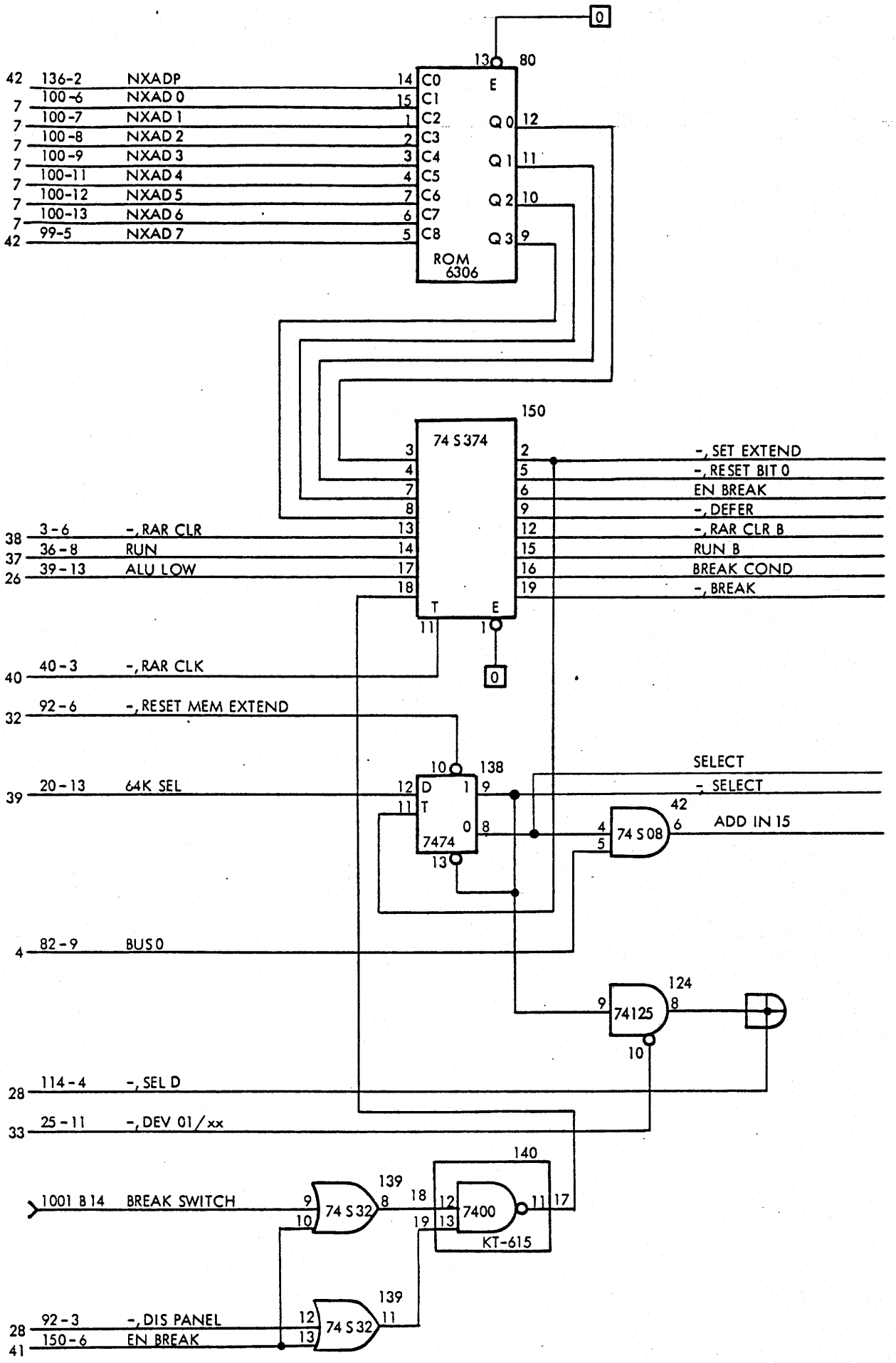
CPU 720

CPU FRONT PANEL DRIVERS AND RECEIVERS
LOGIC DIAGRAM

CPU 040

A13665

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
ADD IN 15		p. 6	ADDress INput bit 15 Logic zero if memory extension is not selected, else Bus 0.
BREAK COND		p. 17	BREAK CONDition Indicates that PC is equal to AC5.
-; BREAK		p. 11	-; BREAK switch.
-; DEFER		p. 40	-; DEFER Indicates that the next microcycle will be used to follow an indirection chain.
EN BREAK		p. 17	ENable BREAK Indicates that the microprogram is in the BREAK loop.
-; RAR CLR B		p. 7	-; Rom Address Register CLeaR Buffer Generated after power on reset to determine the start address of the microprogram.
-; RESET BIT 0		p. 18	-; RESET BIT 0 Places a zero as input to the MSB end of the register shifter (Qo SRI/SLO).
RUN B		p. 17	RUN Buffer Indicates that the CPU is in the RUN state.
-; SET MEM EXTEND		p. 41	
SELECT		p. 17 p. 18 p. 42	Memory extension SELECTed.
-; SELECT		p. 3	



790131 BJ 790131 ABP

SIGNAL	DESTINATION	DESCRIPTION
-, BUS 8-15	p. 24	Internal BUS 8-15
-, DIS BIT 0	p. 5	DISable BIT 0 Forces a logical zero on bit 0 from the AM 2901A array in 64K mode.
-, ENAB DIRECT	p. 7	ENABle next microaddress DIRECT
NX AD 7	p. 8 p. 9 p. 10 p. 11 p. 12 p. 13 p. 14 p. 15 p. 16 p. 41 p. 42	NeXt micro ADdress bit 7 The least significant bit in the address.
NX ADP	p. 9 p. 10 p. 11 p. 12 p. 13 p. 14 p. 15 p. 16 p. 41 p. 42	NeXt ADdress Page Used to separate BANK 0 and BANK 1 in the micro program.
SEL 2ND OP	p. 7	SELect 2ND OPerand Used to separate NEXT address map in BANK 0 and BANK 1.
READ/WRITE	p. 19	READ or WRITE cycle in memory.

Designed by

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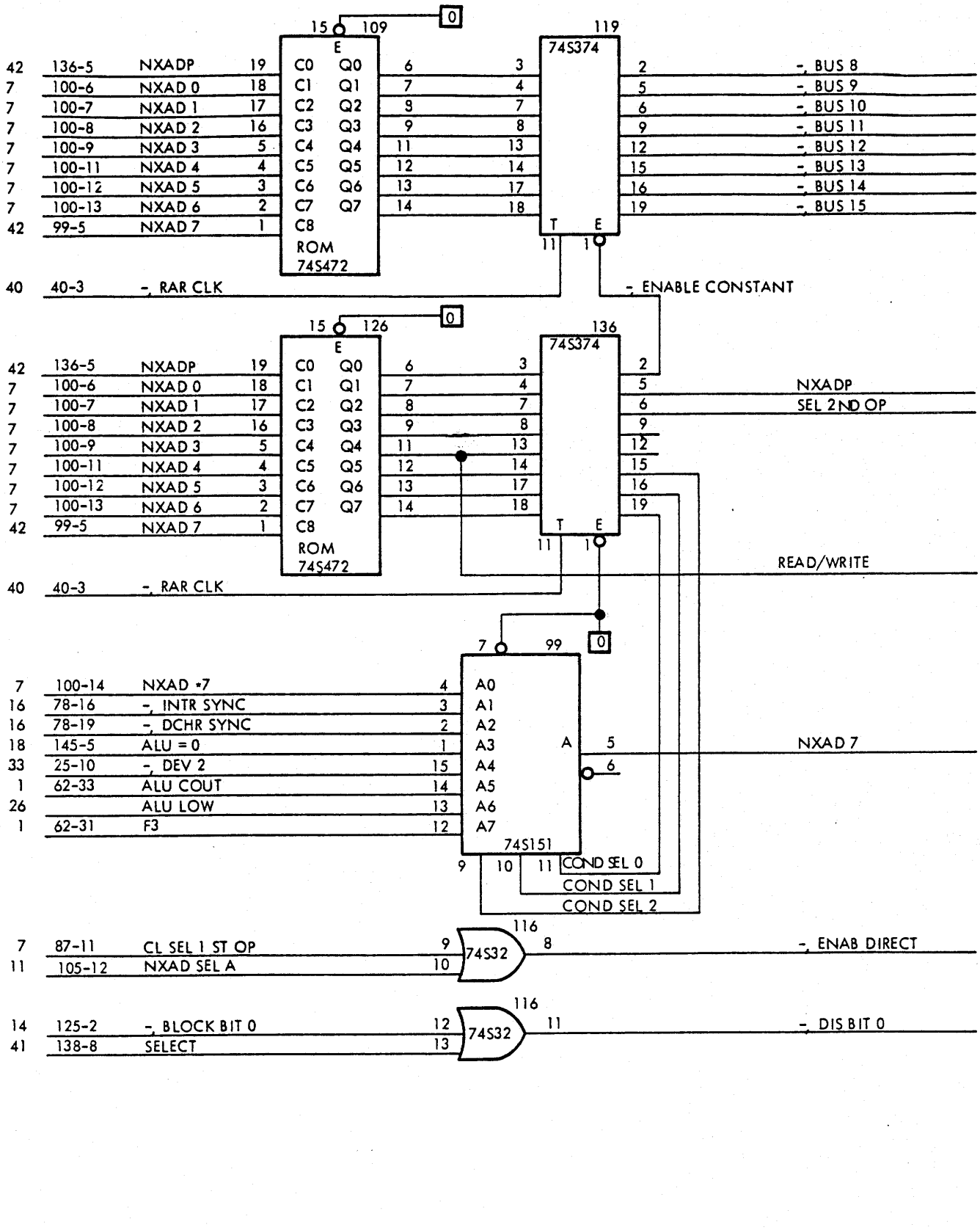
Office Check

Unit		
CPU 720	MICROPROGRAM STORE EXTENSION	CPU 042
Dwg. No. A25676	Signal List	of 42



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