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Author: Niels Toft

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Title:

Technical Manual for Chassis CHS 706 - 710 and 716-717-719

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**Keywords:**

Chassis, RC3600

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**Abstract:**

This manual contains the technical descriptions and diagrams of the internal wiring in the chassis.

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## CONTENTS

## PAGE

CONTENTS	PAGE
Chassis Description	1
Chassis Drawing CHS 706 (CPU + 1 MEM)	2
Chassis Drawing CHS 707 (CPU + 2 MEM) = 719	3
Chassis Drawing CHS 708 (CPU + 4 MEM) = 716	4
Chassis Drawing CHS 709 (Controller, 7") = 717	5
Chassis Drawing CHS 710 (Controller, 8 3/4")	6
Busmother board/Cable CBL 315 (CHS 706-707-708) (1)	7
Busmother board/Cable CBL 315 (CHS 706-707-708) (2)	8
Busmother board/Cable CBL 018 (CHS 709) (1)	9
Busmother board/Cable CBL 018 (CHS 709) (2)	10
Busmother board/Cable CBL 376 (CHS 710) (1)	11
Busmother board/Cable CBL 376 (CHS 710) (2)	12
Memory Bus f. CHS 706, MBU 706	13
Memory Bus f. CHS 707, MBU 707	14
Memory Bus f. CHS 708, MBU 708	15
Power Chassis Mother board, R12358	16
Control Module POW 728	17
+5V Power Module POW 716, V13773	18
+12V Power Module POW 717, V13774	19
-12V Power Module POW 718, V13775	20
-18V Power Module POW 721, R12152	21
Connections f. Power Chassis CHS 706	22
Connections f. Power Chassis CHS 707	23
Connections f. Power Chassis CHS 708	24
Connections f. Power Chassis CHS 709	25
Connections f. Power Chassis CHS 710	26

For information on powersupplies in CHS 716-717 and 719 you are referred to manual RCSL 44-RT 1912

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CHASSIS DESCRIPTIONS.1. MATERIALS.

1.

Cold-rolled steelplate, zincplated Frontplate, anodized aluminium profiles.

2. MAIN COMPONENTS.

2.

The Chassis is made up of 3 main parts. The main chassis for the controller boards, the power chassis for the power modules and the bottom chassis for the internal cables.

The power chassis is fixed to the main chassis with hinges, and can be turned up to a horizontal position. The chassis is held in its working position by 3 screws. The bottom plate in the bottom chassis can be pilled out, when the 2 screws in the front-plate are removed.

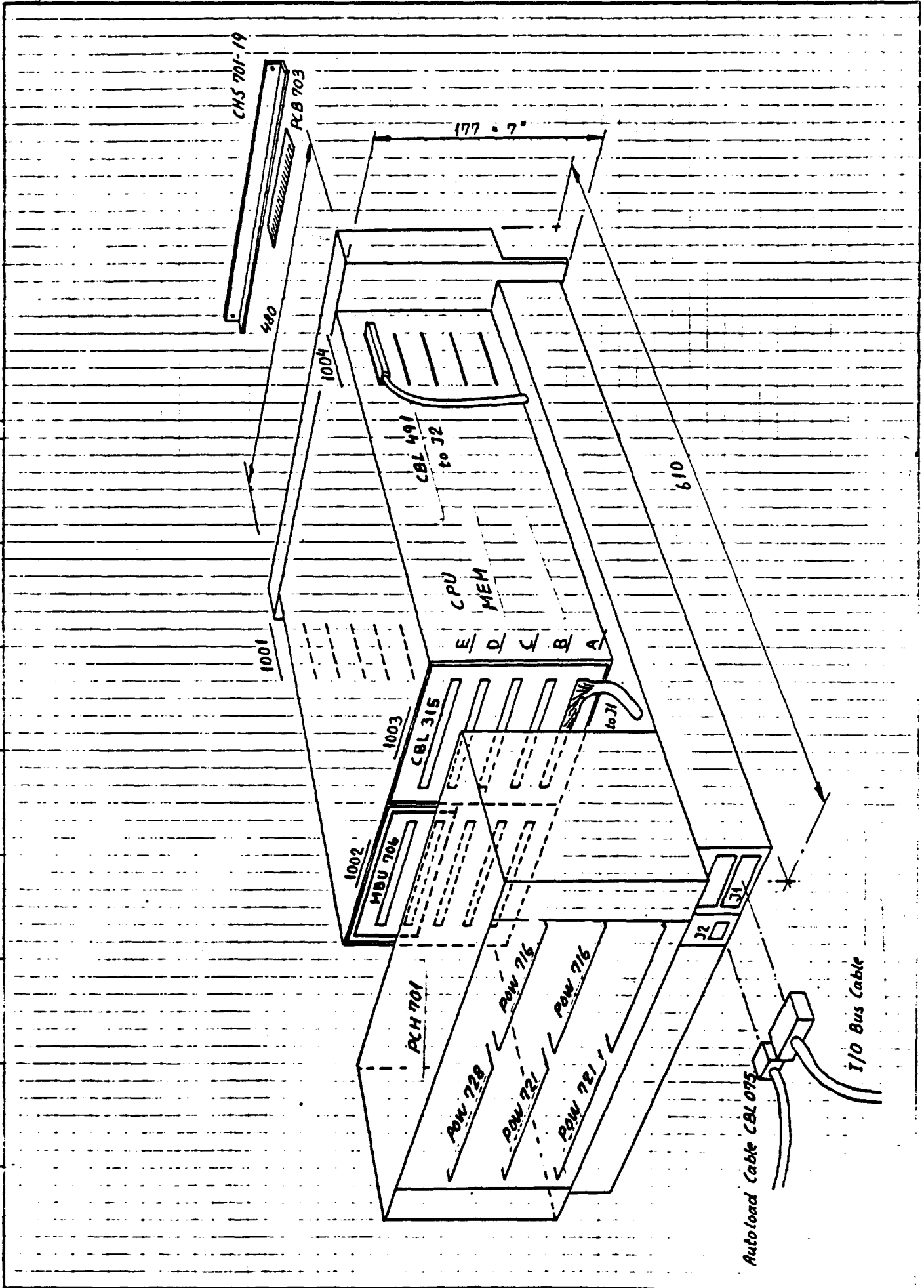
3. FANS.

3.

The main chassis is cooled by 2 axial fans delivering about 80 m<sup>3</sup>/h each. The power chassis is cooled by 1 fan, delivering about 80 m<sup>3</sup>/h. (NOTE: The power chassis should not be left running with the rear-cover removed, as this will cause overheating of the power modules.

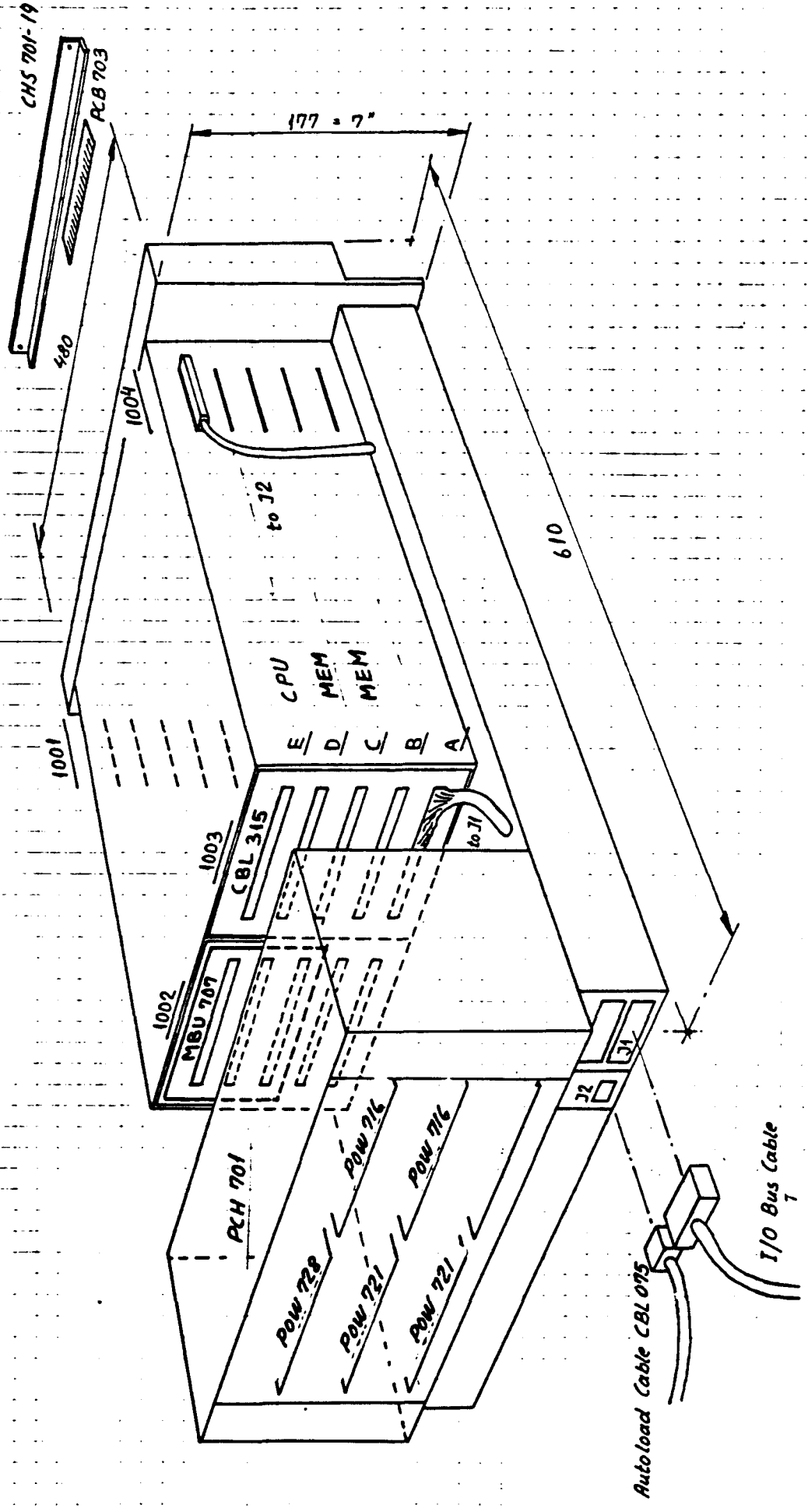
The fans have ball-bearings and are lubricated for life.

A/S MEGNENCENTRALEN  
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 NT 990780  
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 Design Check  
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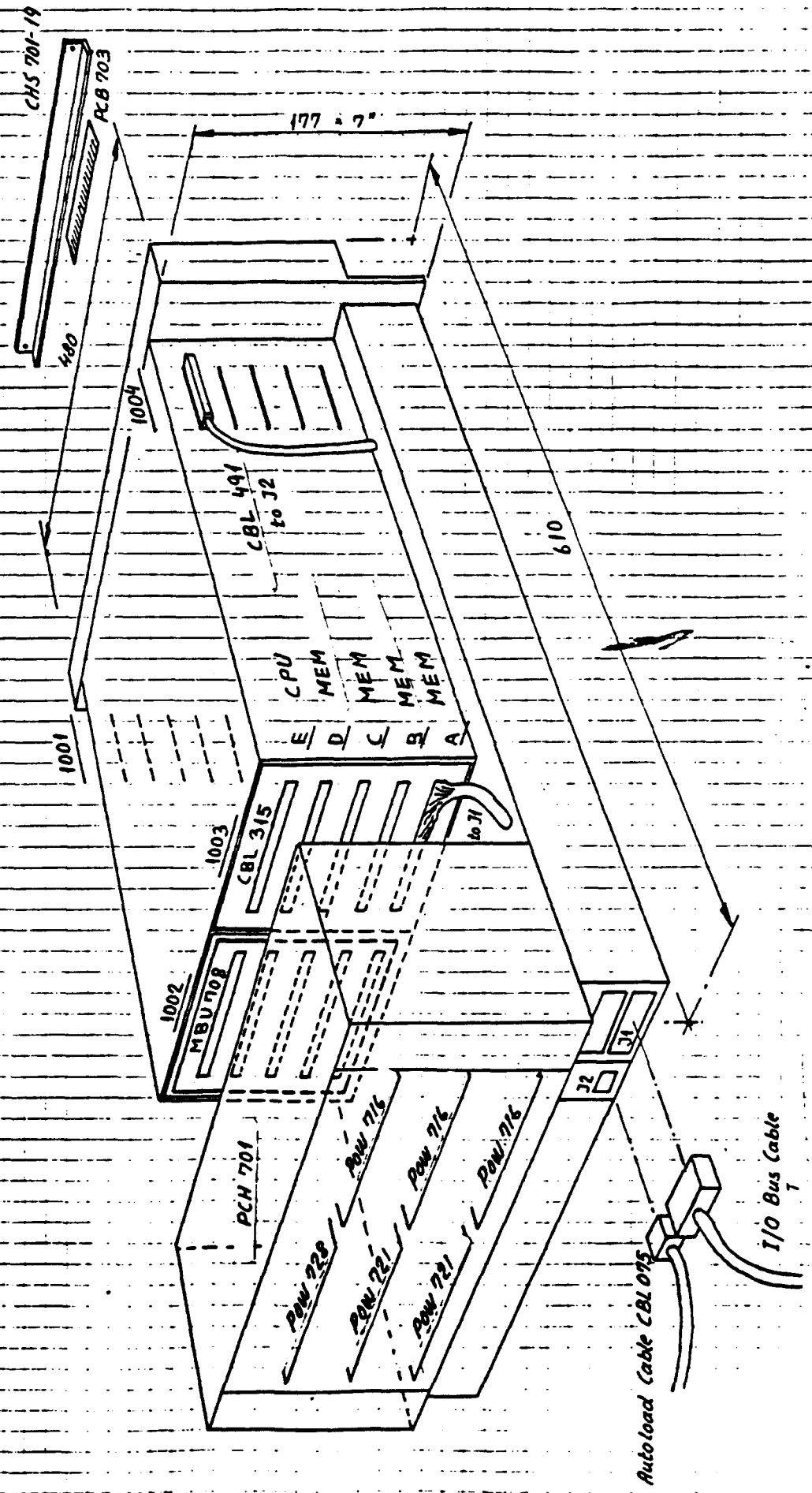
CPU-CHASSIS CHS 706

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CPU - CHASSIS CHS 707 / 719

A/S REGNECENTRALN  
 Designed by  
 Drawn by  
 NT 910720  
 (Draw) Office Check  
 (Verify) Check  
 Replaces Lowy 740  
 (See) to 4-111  
 Replaced by Long 740



CPU - CHASSIS CHS 708 / 716



CONTROL UNIT  
Designed by  
NT 99020

Optional backpanels w. 98 busins; CBL 064  
2x49-pin edge conn.

CBL 063

CBL 062

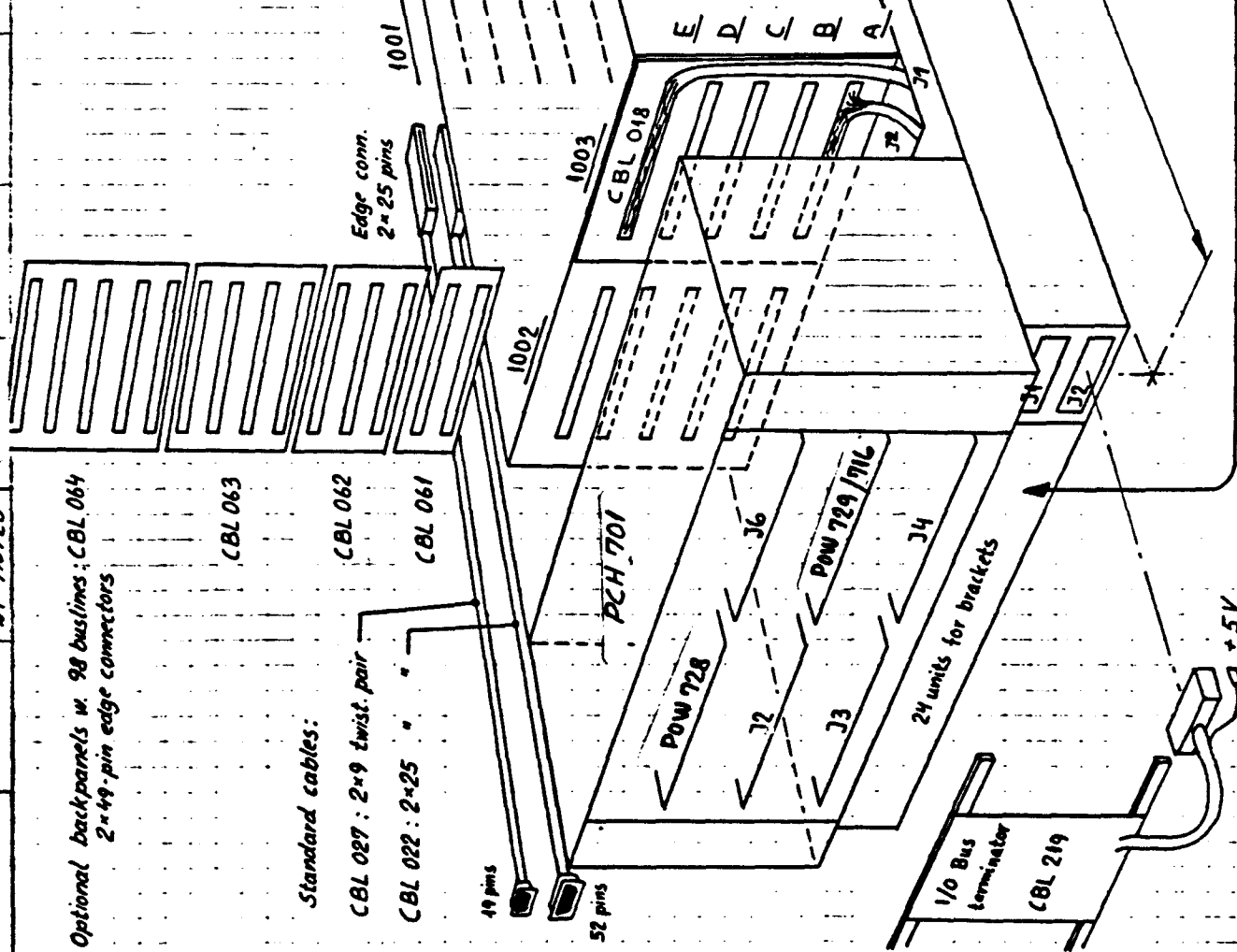
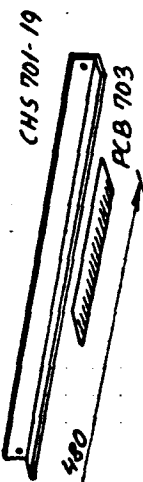
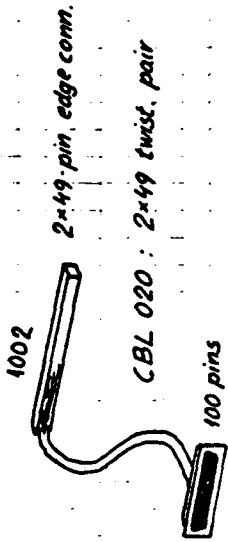
CBL 061

Standard cables:

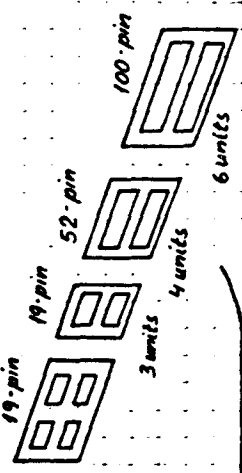
CBL 027: 2x9 twist pair

CBL 022: 2x25 "

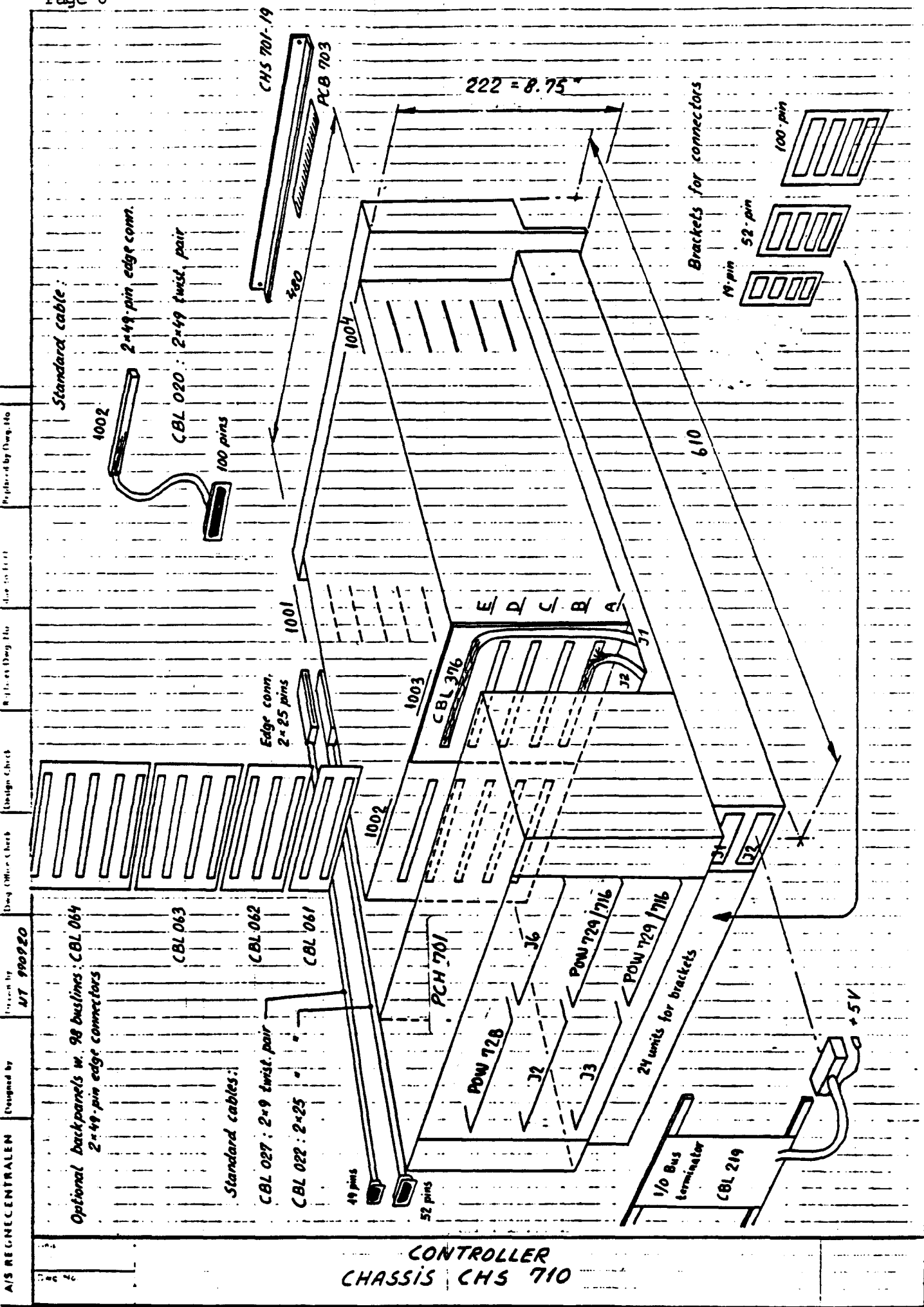
Standard cable:



Brackets for connectors



CONTROLLER  
CHASSIS CHS 709/717

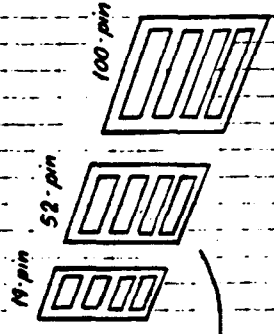


Designed by **UT 990220**  
 Drawn by **UT 990220**  
 Design Check  
 Checked by  
 Approved by

**Optional backpanels w. 98 buslines: CBL 064**  
**2x49-pin edge connectors**  
**CBL 063**  
**CBL 062**  
**CBL 061**  
**Standard cables:**  
**CBL 027: 2x9 twist pair**  
**CBL 022: 2x25**

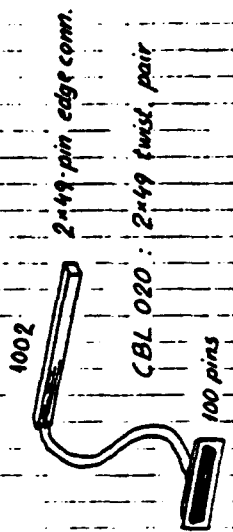
**CONTROLLER CHASSIS CHS 710**

Brackets for connectors



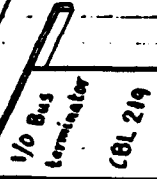
610

222 = 8.75"



Edge conn. 2x25 pins

24 units for brackets



+5V

Connecto I : 1003 A (2x49 pin conn.)



















































Connecto II : J1 (100-pin conn.)

CONN. B-C-D-E MOTHERBOARD		I PIN	WIRE	II PIN	SIGNAL NAME	CONN. B-C-D-E MOTHERBOARD		I PIN	WIRE	II PIN	SIGNAL NAME
Voltage Bus	A1	B1			+ 5V	A15	B15			5	DATA1
	B1									6	0V
	A2	B2			- 12V	A16	B16			7	DATA2
	B2									8	0V
A3	B3				A17	B18			9	DATA3	
B3									10	0V	
A4	B4				A18	B17			11	DATA4	
B4									12	0V	
I/O Bus	A5	B6	⊗	61	DS0	A18	B19	⊗	13	DATA5	
	B6			62	0V				14	0V	
	B5	B6	⊗	81	POB	A19	B19	⊗	15	DATA6	
	B6			80	0V				16	0V	
	A6	B7	⊗	63	DS1	A20	B20	⊗	17	DATA7	
	B7			64	0V				18	0V	
	A7	B7	⊗	65	DS2	A21	B22	⊗	19	DATA8	
	B7			66	0V				20	0V	
	A8	B8	⊗	67	DS3	B21	B22	⊗	21	DATA9	
	B8			68	0V				22	0V	
	B9	B10	⊗	91	OVFLO	A22	B23	⊗	23	DATA10	
	B10			90	0V				24	0V	
	A9	B10	⊗	69	DS4	A23	B23	⊗	25	DATA11	
	B10			70	0V				26	0V	
	A10	B11	⊗	71	DS5	A24	B24	⊗	51	DATA12	
B11	72			0V	50				0V		
A11	B11	⊗	31	DCHA	A25	B26	⊗	49	DATA13		
B11			30	0V				48	0V		
A12	B12	⊗	29	DCHI	B25	B26	⊗	47	DATA14		
B12			28	0V				46	0V		
A13	B14	⊗	55	DCHO	A26	B27	⊗	45	DATA15		
B14			56	0V				44	0V		
B13	B14	⊗	73	INTA	A27	B27	⊗	79	POK		
B14			74	0V				78	0V		
A14	B15	⊗	3	DATA0	A28	B28	⊗	77	PINT		
B15			4	0V				76	0V		

cont'd.

NT  
770721

Connector I : 1003 A (2x49 pin edge conn.)  
 Connector II : J1 (100 - pin conn.)  
 Cable :  
 Length :

CONN. B-C-D-E MOTHERBOARD	I PIN	WIRE	II PIN	SIGNAL NAME	CONN. B-C-D-E MOTHERBOARD	I PIN	WIRE	II PIN	SIGNAL NAME
↑ I/O Bus ↓	A29		87	SELB	↑ I/O Bus ↓	A42		95	IORST
	B30		86	0V		B43		94	0V
	B29		85	SELD		A43		27	DCHMO
	B30		84	0V		B43		52	0V
	A30		99	INTR		A44		53	DCHMI
	B31		98	0V		B44		54	0V
	A31		59	DCHR		A45		57	DCHP OUT
	B31		60	0V		B44		58	0V
	A32		37	DATO A		B45			DCHP IN
	B32		36	0V					
	A33		35	DATO B					
	B34		34	0V					
	B33		97	IOPLS		A46			}
	B34		96	0V		B46			
	A34		33	DATO C		A47			}
	B35		32	0V		B47			
	A35		43	DATO A		A48			} + 12V
	B35		42	0V		B48			
	A36		41	DATO B		A49			} + 5V
	B36		40	0V		B49			
	A37		39	DATO C					
	B38		38	0V					
	B37		1	CLR					
	B38		2	0V					
	A38		83	STR T					
	B39		82	0V					
	A39		89	RQENB					
	B39		88	0V					
	A40		93	MSKO					
	B40		92	0V					
	A41		75	INTP OUT					
	B42		100	0V					
	B41			INTP IN					

Connector I : 1003 A and 1003 E (2x49 pin edge conn.)  
 Connector II : J 1 and J 2 (100-pin conn.)  
 Cable :  
 Length :

CONN. B-C-D-MOTHERBOARD	I PIN	WIRE	II PIN	SIGNAL NAME	CONN. B-C-D-MOTHERBOARD	I PIN	WIRE	II PIN	SIGNAL NAME
Voltage Bus	A 1	⊗		} + 5 V	I/O Bus	A 15	⊗	5	DATA1
	B 1					B 15		6	0V
	A 2	⊗		} - 12V		A 16	⊗	7	DATA2
	B 2					B 16		8	0V
	A 3	⊗		} - 24V		A 17	⊗	9	DATA3
	B 3					B 18		10	0V
	A 4	⊗		} Voltage Bus not used		B 17	⊗	11	DATA4
	B 4					B 18		12	0V
	A 5	⊗	61	DS0	A 18	⊗	13	DATA5	
	B 6		62	0V	B 19		14	0V	
	B 5	⊗	81	POB	A 19	⊗	15	DATA6	
	B 6		80	0V	B 19		16	0V	
	A 6	⊗	63	DS1	A 20	⊗	17	DATA7	
	B 7		64	0V	B 20		18	0V	
	A 7	⊗	65	DS2	A 21	⊗	19	DATA8	
	B 7		66	0V	B 22		20	0V	
	A 8	⊗	67	DS3	B 21	⊗	21	DATA9	
	B 8		68	0V	B 22		22	0V	
	B 9	⊗	91	OVFLO	A 22	⊗	23	DATA10	
	B10		90		B 23		24	0V	
	A 9	⊗	69	DS4	A 23	⊗	25	DATA11	
	B10		70	0V	B 23		26	0V	
	A10	⊗	71	DS5	A 24	⊗	51	DATA12	
	B11		72	0V	B 24		50	0V	
	A11	⊗	31	DCHA	A 25	⊗	49	DATA13	
	B11		30	0V	B 26		48	0V	
	A12	⊗	29	DCHI	B 25	⊗	47	DATA14	
	B12		28	0V	B 26		46	0V	
	A13	⊗	55	DCHO	A 26	⊗	45	DATA15	
	B14		56	0V	B 27		44	0V	
	B13	⊗	73	INTA	A 27	⊗	79	POK	
	B14		74	0V	B 27		78	0V	
	A14	⊗	3	DATA0	A 28	⊗	77	PINT	
	B15		4	0V	B 28		76	0V	

cont'd.

NT  
770721

Connector I : 1003 A and 1003 E (2 x 49 pin edge conn.)  
 Connector II : J1 and J2 (100-pin conn.)  
 Cable :  
 Length :

CONN. B-C-D-MOTHERBOARD	I PIN	WIRE	II PIN	SIGNAL NAME	CONN. B-C-D-MOTHERBOARD	I PIN	WIRE	II PIN	SIGNAL NAME
↑ I/O Bus ↓	A29	⊗	87	SELB	↑ I/O Bus ↓	A42	⊗	95	IORST
	B 30	⊗	86	0V		B 43	⊗	94	0V
	B 29	⊗	85	SELD		A43	⊗	27	DCHMO
	B 30	⊗	84	0V		B 43	⊗	52	0V
	A30	⊗	99	INTR		A44	⊗	53	DCHMI
	B 31	⊗	98	0V		B 44	⊗	54	0V
	B 31	⊗	59	DCHR		A45	⊗	57	DCHP OUT
	B 31	⊗	60	0V		B 44	⊗	58	0V
	A32	⊗	37	DATOA		B 45	⊗		DCHP IN
	B 32	⊗	36	0V					
	A33	⊗	35	DATOB	↑ Voltage Bus ↓	A46	⊗		} Voltage Bus not used
	B 34	⊗	34	0V		B 46	⊗		
	B 33	⊗	97	IOPLS		A47	⊗		} + 24V
	B 34	⊗	96	0V		B 47	⊗		
	A34	⊗	33	DATOC		A48	⊗		} + 12V
	B 35	⊗	32	0V		B 48	⊗		
	A35	⊗	43	DATIA		A49	⊗		} + 5V
	B 35	⊗	42	0V		B 49	⊗		
	A36	⊗	41	DATIB					
	B 36	⊗	40	0V					
	A37	⊗	39	DATIC					
B 38	⊗	38	0V						
B 37	⊗	1	CLR						
B 38	⊗	2	0V						
A38	⊗	83	STRT						
B 39	⊗	82	0V						
A39	⊗	89	RQENB						
B 39	⊗	88	0V						
A40	⊗	93	MSKO						
B 40	⊗	92	0V						
A41	⊗	75	INTP OUT						
B 42	⊗	100	0V						
B 41			INTP IN						

Connector I : 1003 A and 1003 E (2x49 pin edge conn.)  
 Connector II : J 1 and J 2 (100-pin conn.)  
 Cable :  
 Length :

NT  
70721

CONN. B-C-D-MOTHERBOARD	I PIN	WIRE	II PIN	SIGNAL NAME	CONN. B-C-D-MOTHERBOARD	I PIN	WIRE	II PIN	SIGNAL NAME
Voltage Bus	A 1	⊗		} + 5 V	I/O Bus	A 15	⊗	5	DATA1
	B 1					B 15		6	0V
	A 2	⊗		} - 12V		A 16	⊗	7	DATA2
	B 2					B 16		8	0V
	A 3	⊗		} - 24V		A 17	⊗	9	DATA3
	B 3					B 18		10	0V
	A 4	⊗		} Voltage Bus not used		B 17	⊗	11	DATA4
	B 4					B 18		12	0V
A 5	⊗	61	DS0	A 18	⊗	13	DATA5		
B 6		62	0V	B 19		14	0V		
B 5	⊗	81	POB	A 19	⊗	15	DATA6		
B 6		80	0V	B 19		16	0V		
A 6	⊗	63	DS1	A 20	⊗	17	DATA7		
B 7		64	0V	B 20		18	0V		
A 7	⊗	65	DS2	A 21	⊗	19	DATA8		
B 7		66	0V	B 22		20	0V		
A 8	⊗	67	DS3	B 21	⊗	21	DATA9		
B 8		68	0V	B 22		22	0V		
B 9	⊗	91	OVFLO	A 22	⊗	23	DATA10		
B10		90		B 23		24	0V		
A 9	⊗	69	DS4	A 23	⊗	25	DATA11		
B10		70	0V	B 23		26	0V		
A10	⊗	71	DS5	A 24	⊗	51	DATA12		
B11		72	0V	B 24		50	0V		
A11	⊗	31	DCHA	A 25	⊗	49	DATA13		
B11		30	0V	B 26		48	0V		
A12	⊗	29	DCHI	B 25	⊗	47	DATA14		
B12		28	0V	B 26		46	0V		
A13	⊗	55	DCHO	A 26	⊗	45	DATA15		
B14		56	0V	B 27		44	0V		
B13	⊗	73	INTA	A 27	⊗	79	POK		
B14		74	0V	B 27		78	0V		
A14	⊗	3	DATA0	A 28	⊗	77	PINT		
B15		4	0V	B 28		76	0V		

cont'd.

Connector I : 1003 A and 1003 E (2 x 49 pin edge conn.)  
 Connector II : J1 and J2 (100-pin conn.)  
 Cable :  
 Length :

CONN. B-C-D-MOTHERBOARD	I PIN	WIRE	II PIN	SIGNAL NAME	CONN. B-C-D-MOTHERBOARD	I PIN	WIRE	II PIN	SIGNAL NAME
↑ I/O Bus ↓	A29	⊗	87	SELB	↑ I/O Bus ↓ Priority Line	A42	⊗	95	IORST
	B30	⊗	86	0V		B43	⊗	94	0V
	B29	⊗	85	SELD		A43	⊗	27	DCHMO
	B30	⊗	84	0V		B43	⊗	52	0V
	A30	⊗	99	INTR		A44	⊗	53	DCHMI
	B31	⊗	98	0V		B44	⊗	54	0V
	B31	⊗	59	DCHR		A45	⊗	57	DCHP OUT
	B31	⊗	60	0V		B44	⊗	58	0V
	A32	⊗	37	DATOA		B45	⊗		DCHP IN
	B32	⊗	36	0V					
	A33	⊗	35	DATOB	↑ Voltage Bus ↓	A46	⊗		} Voltage Bus not used
	B34	⊗	34	0V		B46	⊗		
	B33	⊗	97	IOPLS		A47	⊗		} + 24V
	B34	⊗	96	0V		B47	⊗		
	A34	⊗	33	DATOC		A48	⊗		} + 12V
	B35	⊗	32	0V		B48	⊗		
	A35	⊗	43	DATIA		A49	⊗		} + 5V
	B35	⊗	42	0V		B49	⊗		
	A36	⊗	41	DATIB					
	B36	⊗	40	0V					
A37	⊗	39	DATIC						
B38	⊗	38	0V						
B37	⊗	1	CLR						
B38	⊗	2	0V						
A38	⊗	83	STRT						
B39	⊗	82	0V						
A39	⊗	89	RQENB						
B39	⊗	88	0V						
A40	⊗	93	MSKO						
B40	⊗	92	0V						
A41	⊗	75	INTP OUT						
B42	⊗	100	0V						
B41									
				INTP IN					



CPU  
CONNECTOR E

MEM

D

PIN	A	B
1	A0	-.BUS 0
2	A1	-.BUS 1
3	A2	-.BUS 2
4	A3	-.BUS 3
5	A4	-.BUS 4
6	A5	-.BUS 5
7	A6	-.BUS 6
8	A7	-.BUS 7
9	A8	-.BUS 8
10	A9	-.BUS 9
11	A10	-.BUS 10
12	A11	-.BUS 11
13	A12	-.BUS 12
14	A13	-.BUS 13
15	A14	-.BUS 14
16	A15	-.BUS 15
17		-. RIGHT PARITY
18		-. LEFT PARITY
19	MEM START	0V
20	MEMORY BUSY	0V
21	READ/RESTORE	0V
22	DATA RETAIN	0V
23		
24		
25	DATA AVAIL	0V
26		
27		
28		
29		
30		
31	- 18V	- 18V
32	- 18V	- 18V
33	- 18V	- 18V
34	- 18V	- 18V
35	- 18V	- 18V
36		
37		
38	0V	0V
39	0V	0V
40	0V	0V
41	0V	0V
42	0V	0V
43		
44		
45		
46		
47		
48		
49		

A B



TOP

18V

0V

GND.

Repl. ( ) Dwg. No. ( )  
 Replaces Dwg. No. ( ) due to ECN ( )  
 Design Check ( )  
 Dwg. Office ( )  
 Drawn by NT 770721  
 Designed by  
**ENTRALEN**

Unit	CHS 706	MEMORY BUS MBU 706
Dwg. No.		CHS 706 pos. 1002

CPU MEM MEM  
CONNECTOR E D C

PIN	A	B	A B	A B
1	A0	--BUS 0		
2	A1	--BUS 1		
3	A2	--BUS 2		
4	A3	--BUS 3		
5	A4	--BUS 4		
6	A5	--BUS 5		
7	A6	--BUS 6		
8	A7	--BUS 7		
9	A8	--BUS 8		
10	A9	--BUS 9		
11	A10	--BUS 10		
12	A11	--BUS 11		
13	A12	--BUS 12		
14	A13	--BUS 13		
15	A14	--BUS 14		
16	A15	--BUS 15		
17		-- RIGHT PARITY		
18		-- LEFT PARITY		
19	MEM START	0V		
20	MEM BUSY	0V		
21	READ/RESTORE	0V		
22	DATA RETAIN	0V		
23				
24				
25	DATA AVAIL	0V		
26				
27				
28				
29				
30				
31	-18V	-18V		
32	-18V	-18V		
33	-18V	-18V		
34	-18V	-18V		
35	-18V	-18V		
36				
37				
38	0V	0V		
39	0V	0V		
40	0V	0V		
41	0V	0V		
42	0V	0V		
43				
44				
45				
46				
47				
48	GND.			
49				

TOP

-18V

0V

GND.

Replaces by Dwg. No.

due to ECN

Replaces Dwg. No.

Design Check

Dwg. Office Check

Drawn by NT 700781

Designed by

A/S REGNENCENTRALEN

Unit CHS 707

MEMORY BUS MBU 707

Dwg. No.

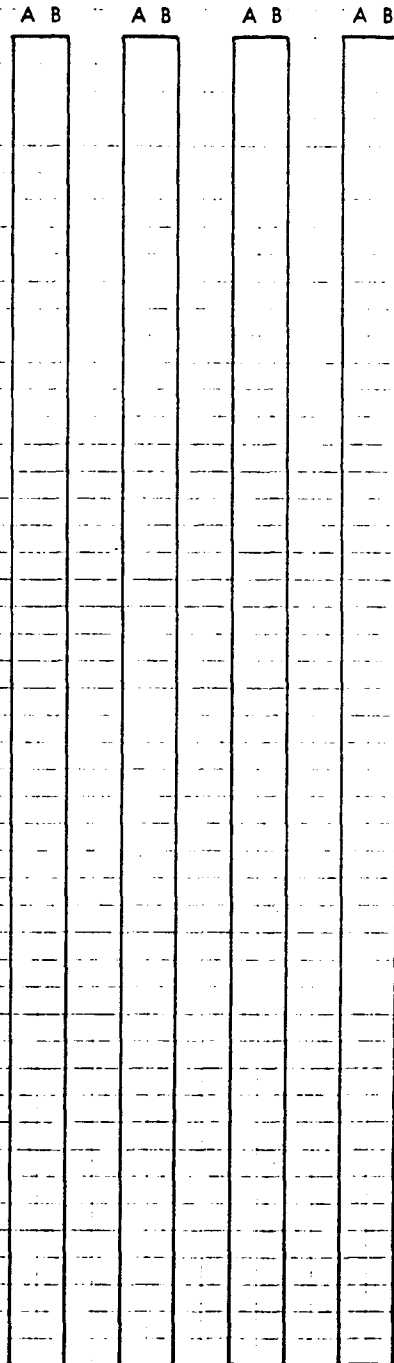
CHS 707 pos. 1002

CPU  
CONNECTOR E

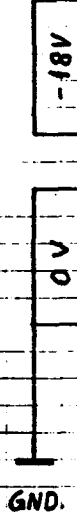
MEM MEM MEM MEM

D C B A

PIN	A	B
1	A0	-.BUS 0
2	A1	-.BUS 1
3	A2	-.BUS 2
4	A3	-.BUS 3
5	A4	-.BUS 4
6	A5	-.BUS 5
7	A6	-.BUS 6
8	A7	-.BUS 7
9	A8	-.BUS 8
10	A9	-.BUS 9
11	A10	-.BUS 10
12	A11	-.BUS 11
13	A12	-.BUS 12
14	A13	-.BUS 13
15	A14	-.BUS 14
16	A15	-.BUS 15
17		-. RIGHT PARITY
18		-. LEFT PARITY
19	MEM START	0V
20	MEMORY BUSY	0V
21	READ/RESTORE	0V
22	DATA RETAIN	0V
23		
24		
25	DATA AVAIL	0V
26		
27		
28		
29		
30		
31	- 18V	- 18V
32	- 18V	- 18V
33	- 18V	- 18V
34	- 18V	- 18V
35	- 18V	- 18V
36		
37		
38	0V	0V
39	0V	0V
40	0V	0V
41	0V	0V
42	0V	0V
43		
44		
45		
46		
47		
48		
49		

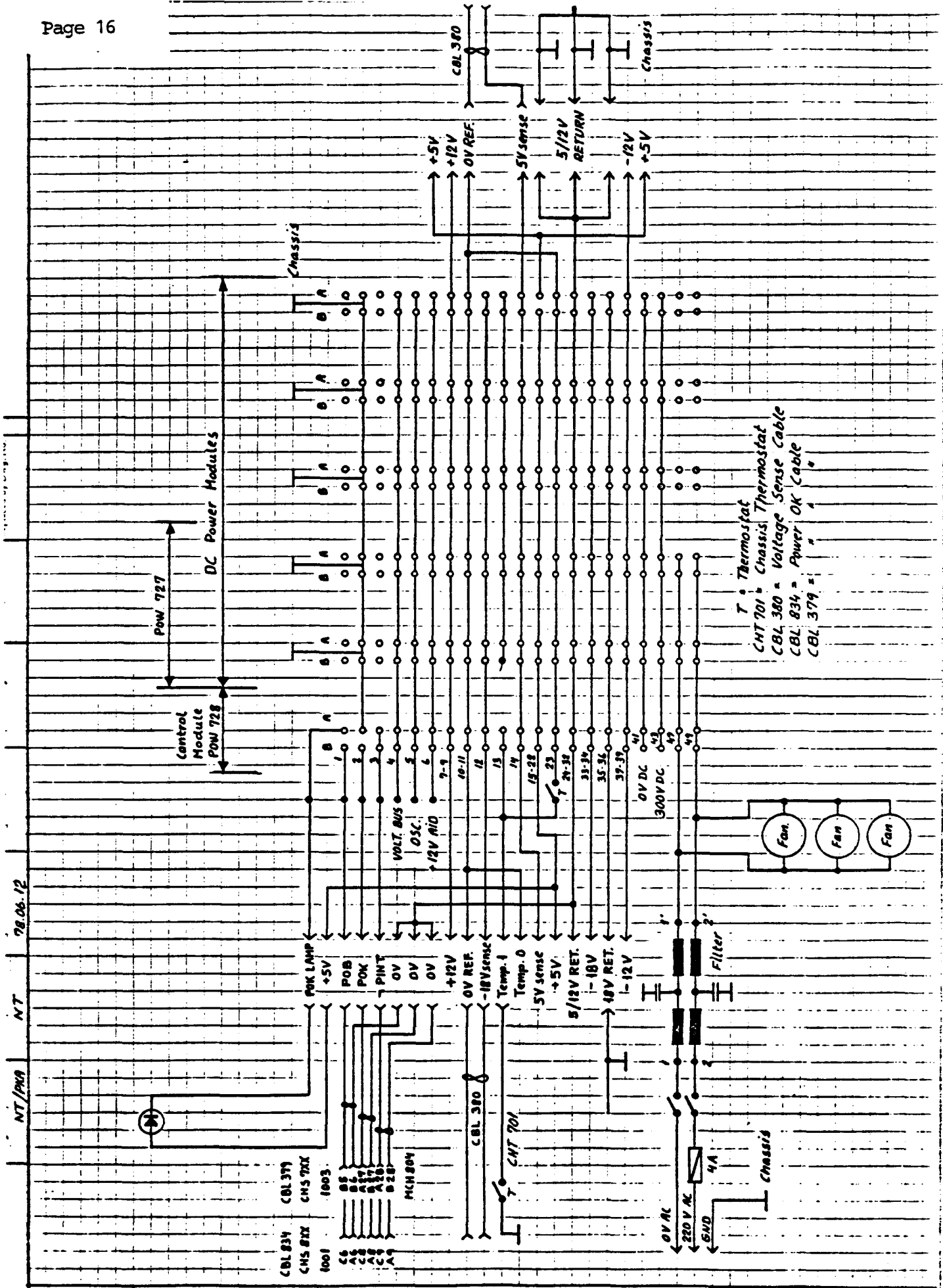


TOP



Dwg. No. \_\_\_\_\_  
 Repl. ( ) \_\_\_\_\_  
 due to ECN \_\_\_\_\_  
 Replaces Dwg. No. \_\_\_\_\_  
 Design Check \_\_\_\_\_  
 Dwg. Office \_\_\_\_\_  
 Drawn by NT 770721  
 Designed by CENTRALEN

Unit	CHS 708	MEMORY BUS MBU 708
Dwg. No.		CHS 708 pos. 1002



T = Thermosstat  
 CHT 701 = Chassis Thermostat  
 CBL 380 = Voltage Sense Cable  
 CBL 834 = Power OK Cable  
 CBL 379 = " " " " " "

NT/PWA NT 78.06.12

Wh PCH 701  
 Dwg. No R 12 358

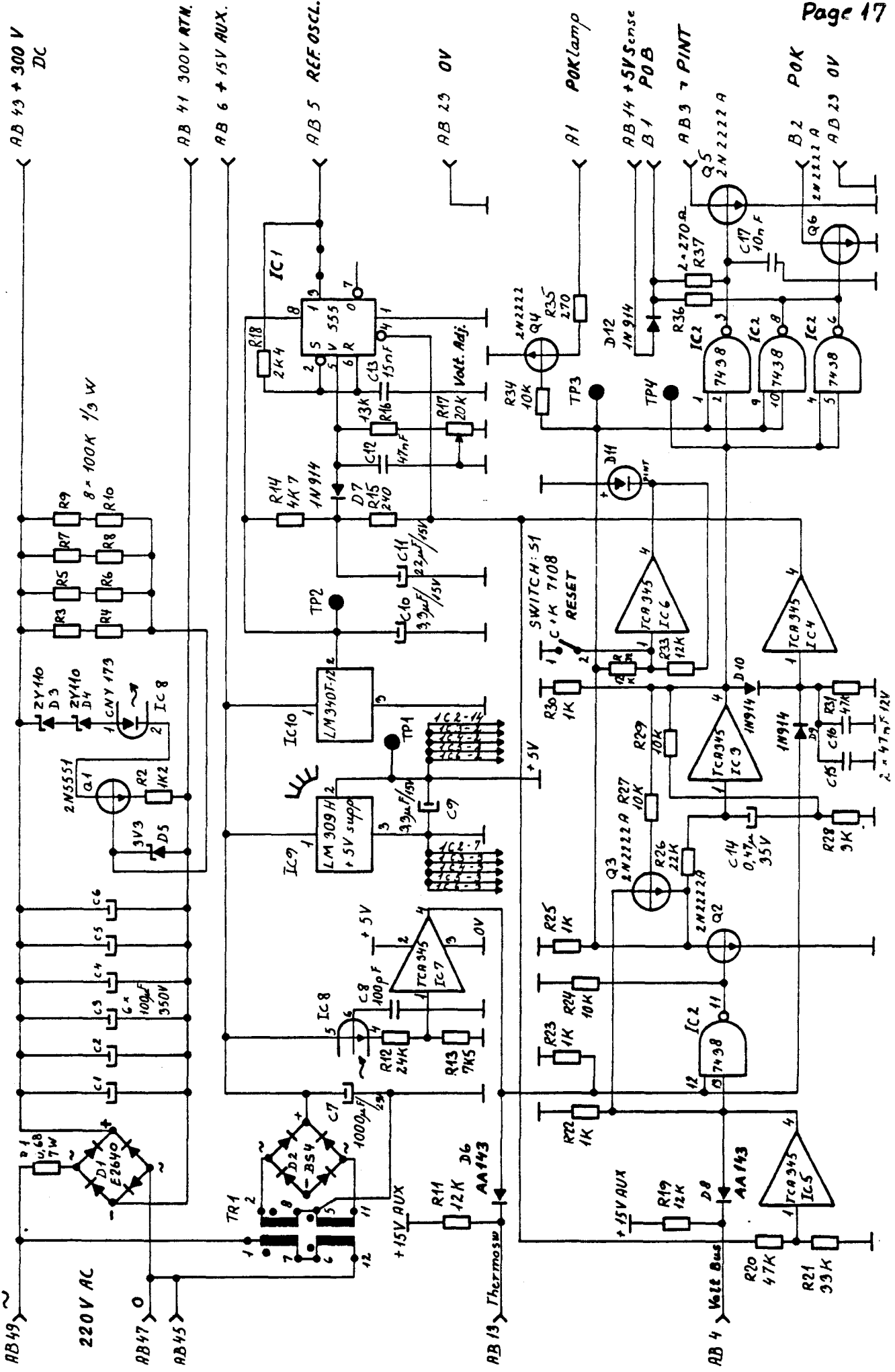
POWER CHASSIS MOTHERBOARD

R 12688

KF 790828

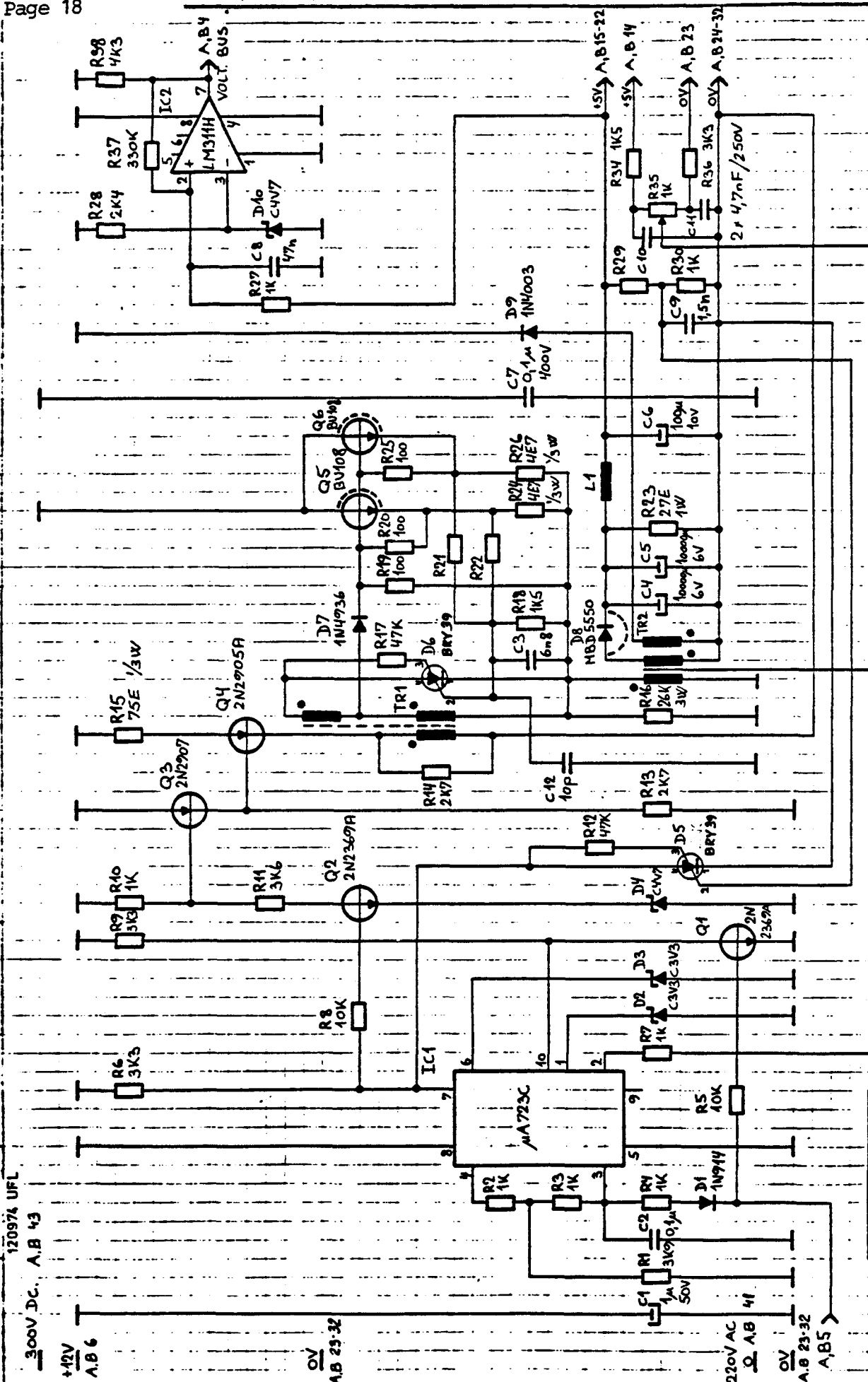
POW 728

R12742



CONTROL MODULE  
POW 728

120974 UFL  
300V DC, A, B 43  
+12V A, B 6  
0V A, B 23-32  
220V AC A, B 41  
0V A, B 23-32  
A, B 5  
A, B 15-22  
+5V A, B 14  
0V A, B 23  
0V A, B 24-32  
A2  
DANGER HIGH VOLTAGE



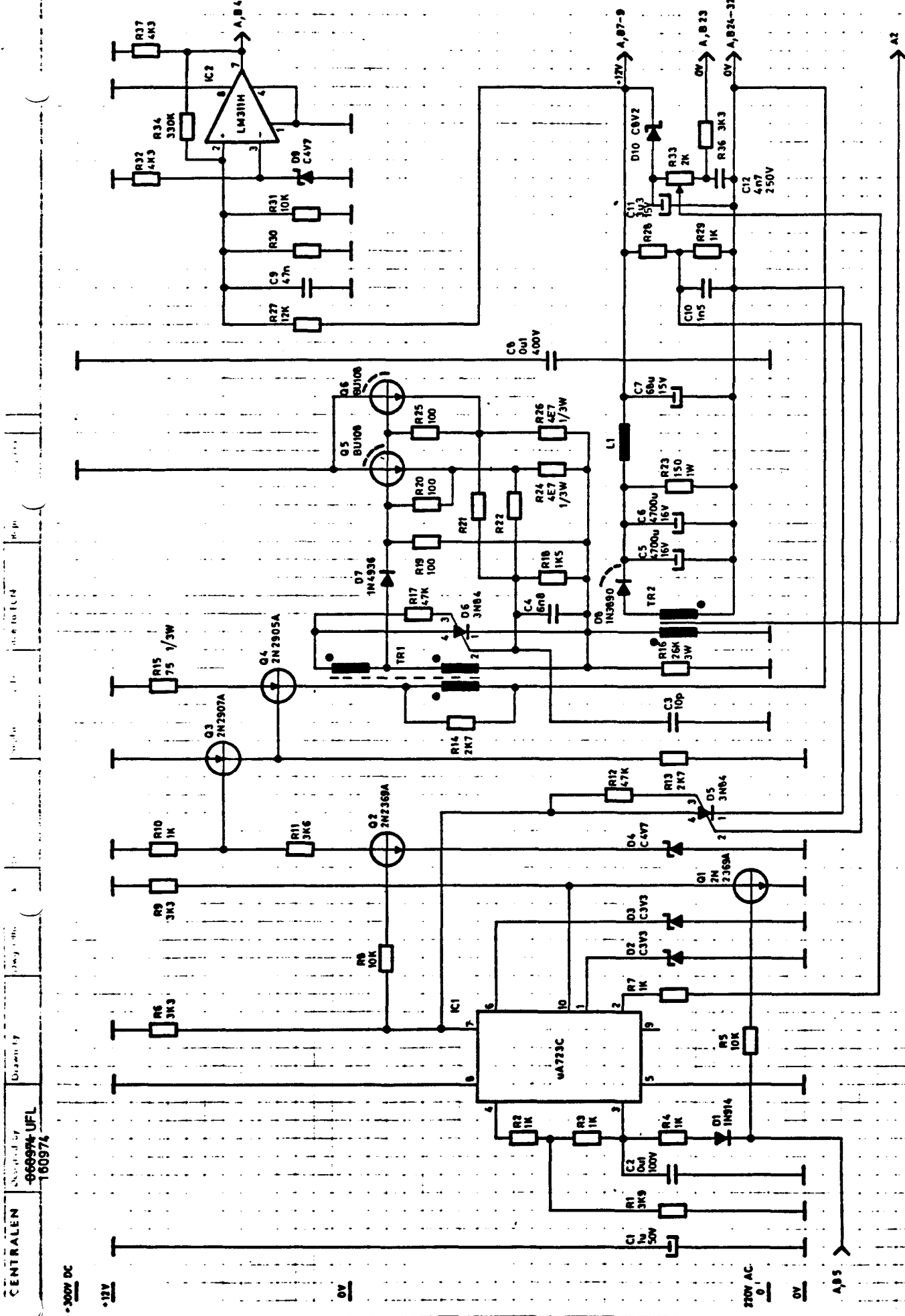
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220V AC, A, B 41  
+12V, A, B 6

DANGER HIGH VOLTAGE

POW 716

+5V POWER MODULE

V13773

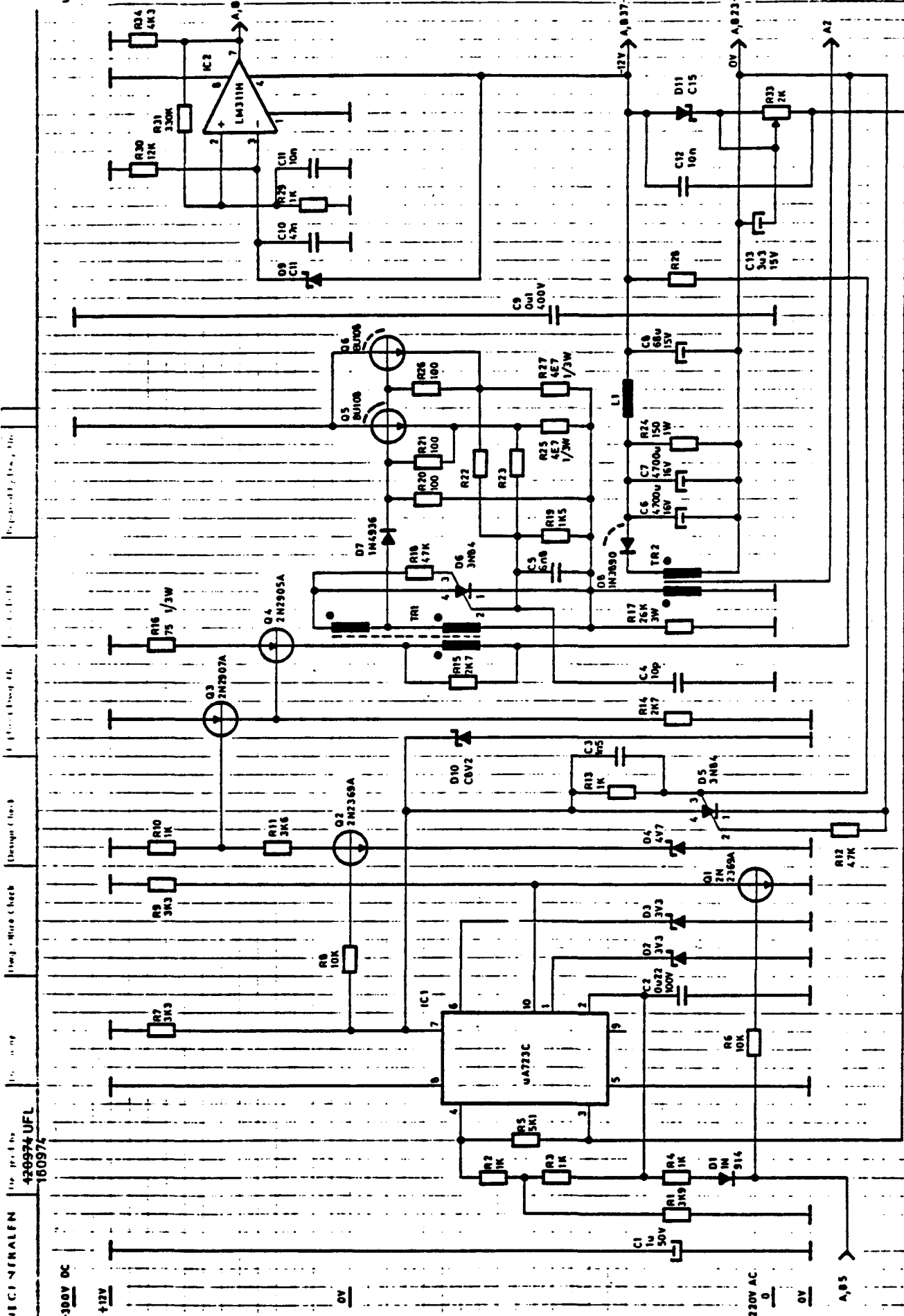


DANGER HIGH VOLTAGE

+300V DC  
 +12V  
 0V

A/S RE  
 CENTRALEN  
 Drawn by  
 86699% UFL  
 160974  
 Part No  
 POW717  
 V13774

•12V POWER MODULE



DANGER HIGH VOLTAGE

A/S REGNIGI NENALFN  
 420974 UFL  
 180974

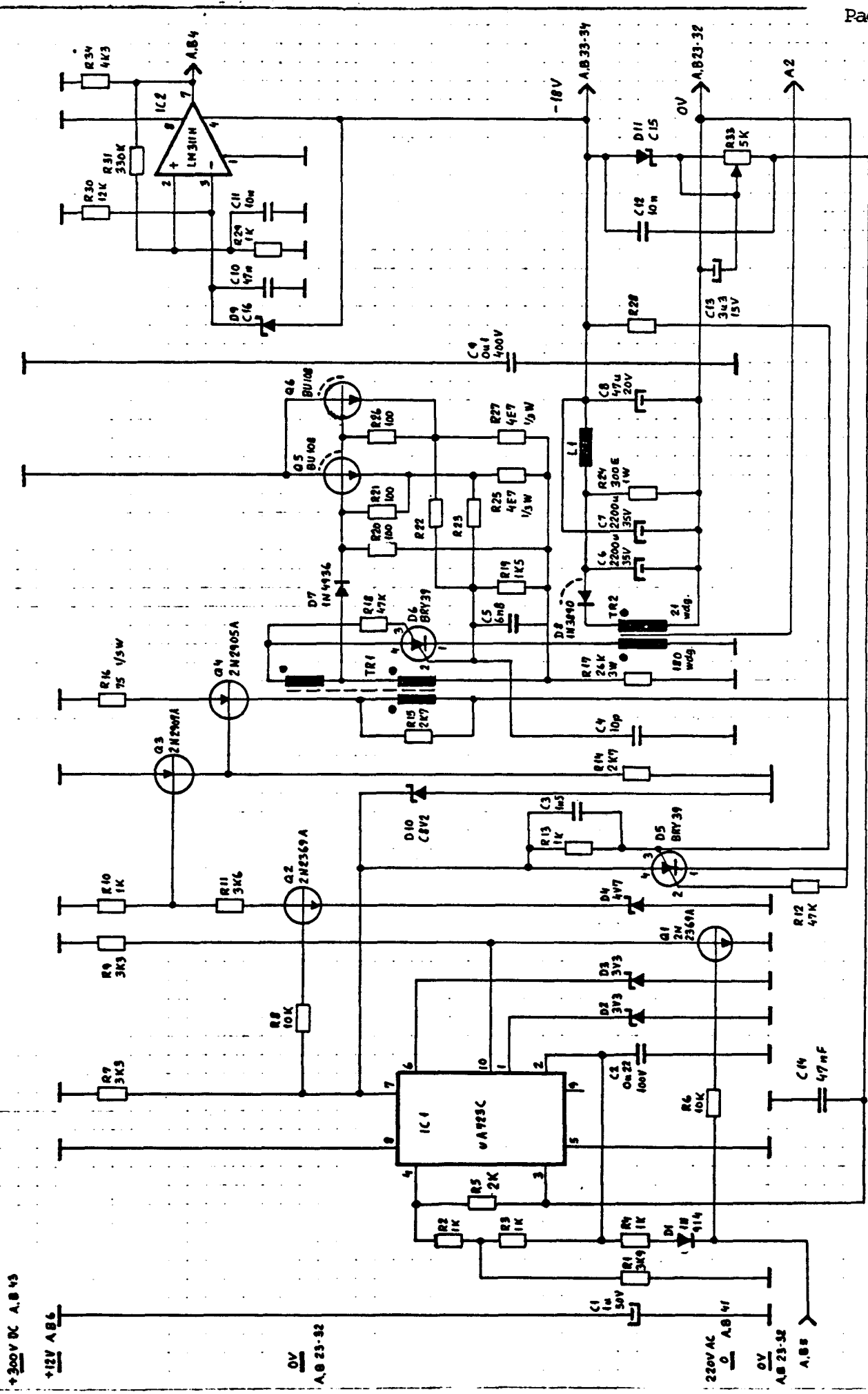
POW 718  
 V13775

-12V POWER MODULE

Design Check  
 Design Drawn  
 Prepared by Des. Div.



POW721  
R12 152  
35 76 1102 NT 770722

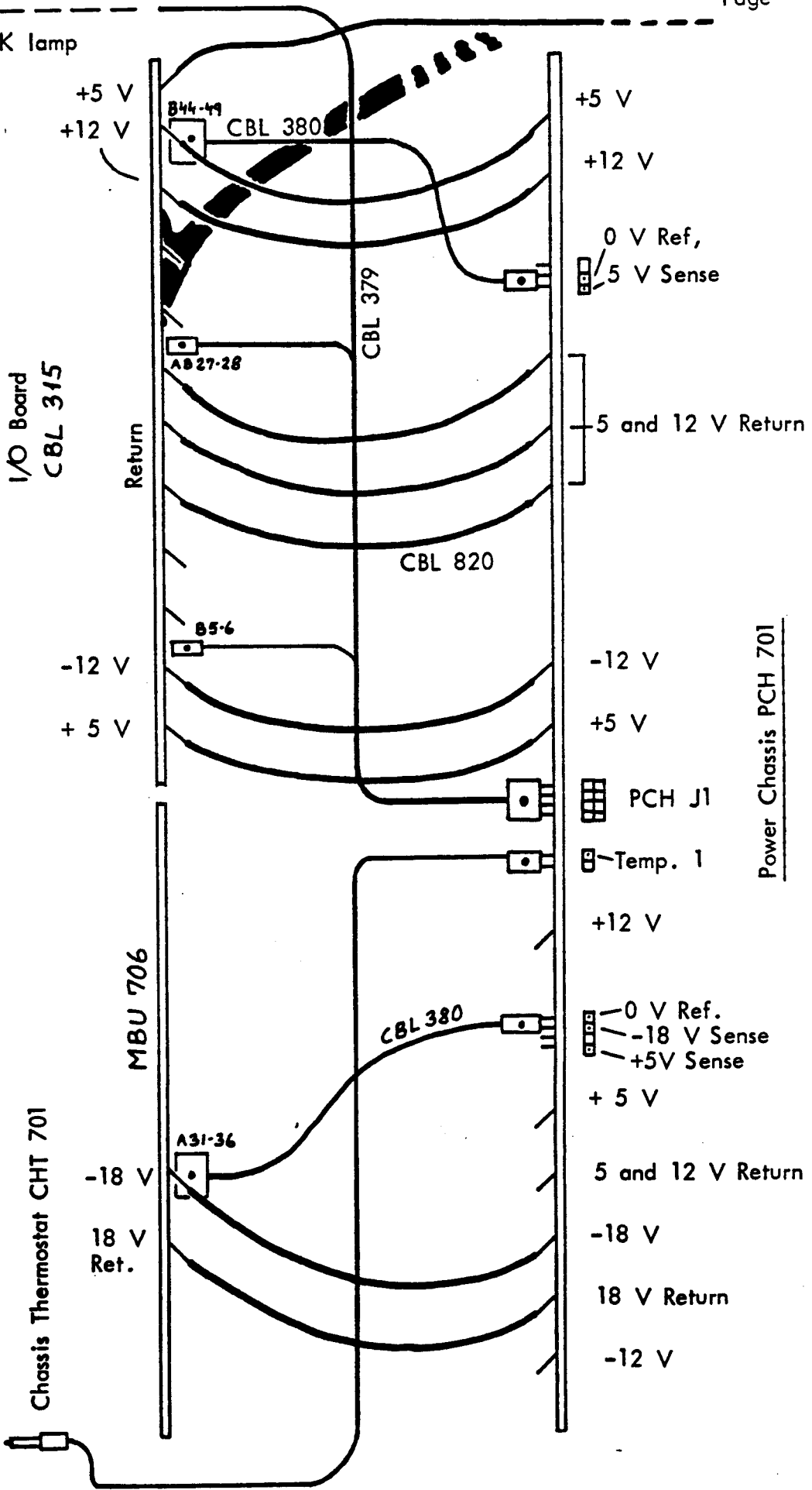


+300V DC A.B.43  
 +12V A.B.6  
 0V A.B.23-32  
 220V AC 0 A.B.41  
 0V A.B.23-32  
 A.B.5

POW721  
 -18V POWER MODULE 3.5 A  
 R12 152

Power OK lamp

Main Chassis

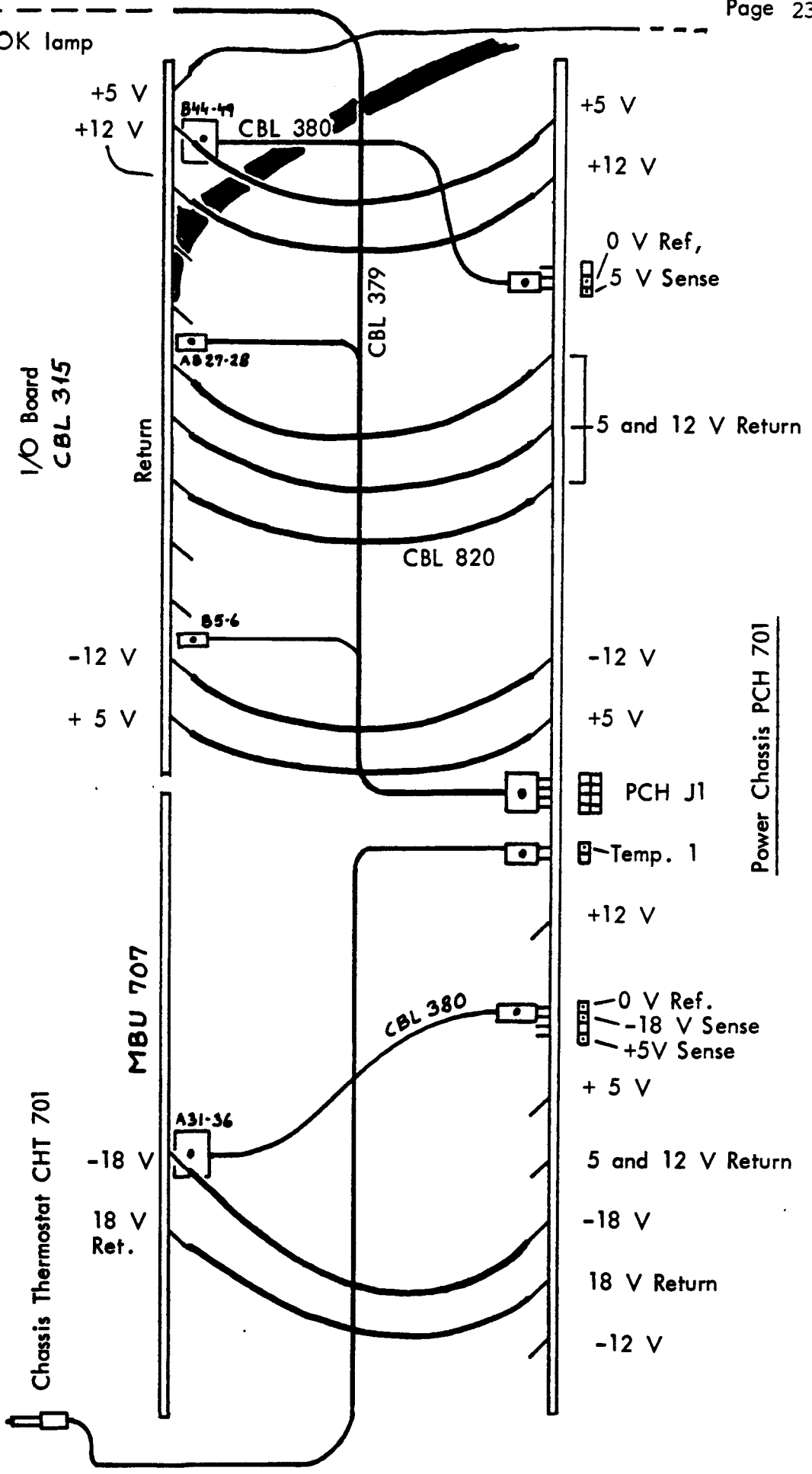


78.07.20  
NT

CABLE CONNECTIONS FOR POWER CHASSIS  
CHS 706

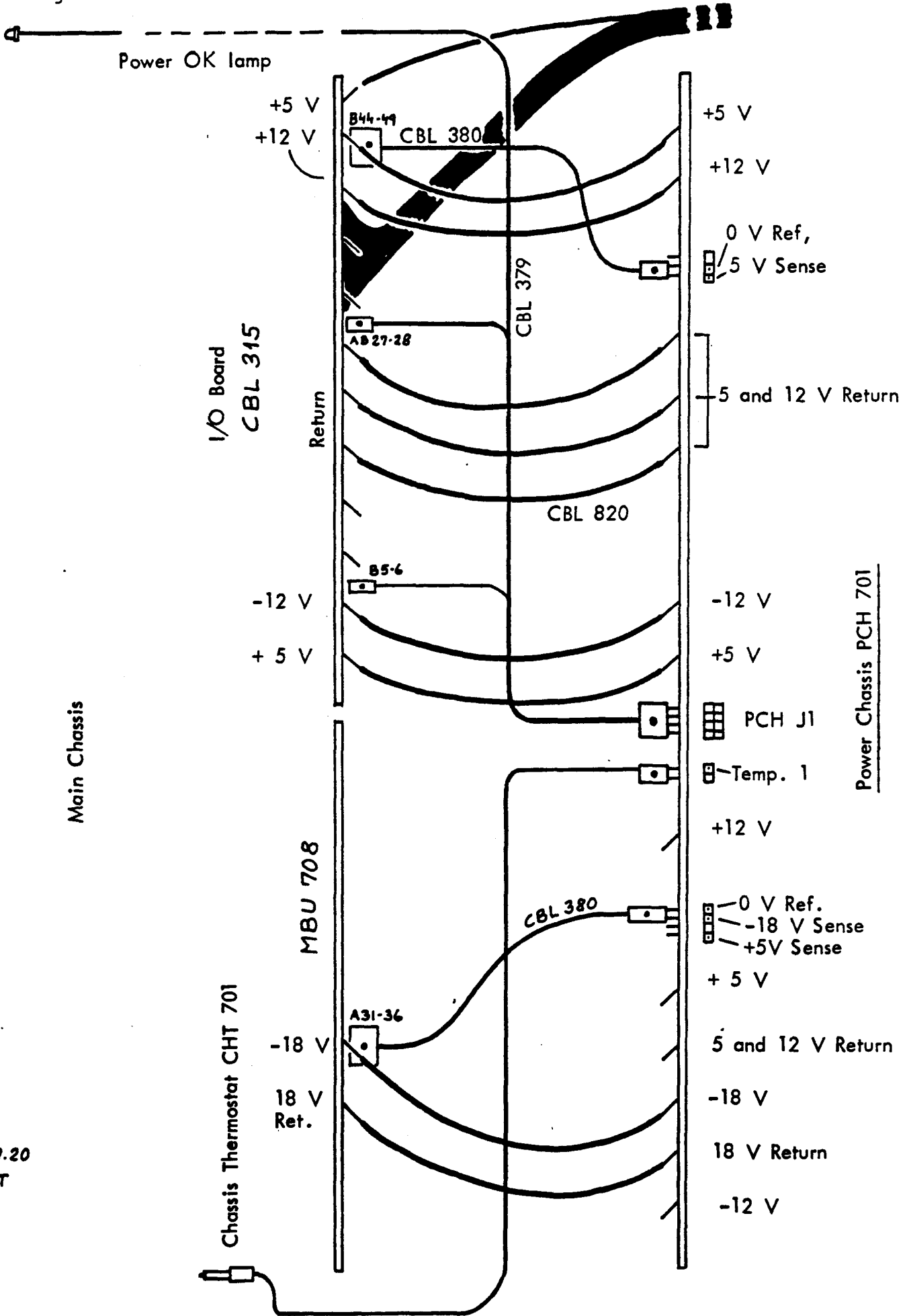
Power OK lamp

Main Chassis



CABLE CONNECTIONS FOR POWER CHASSIS  
CHS 707

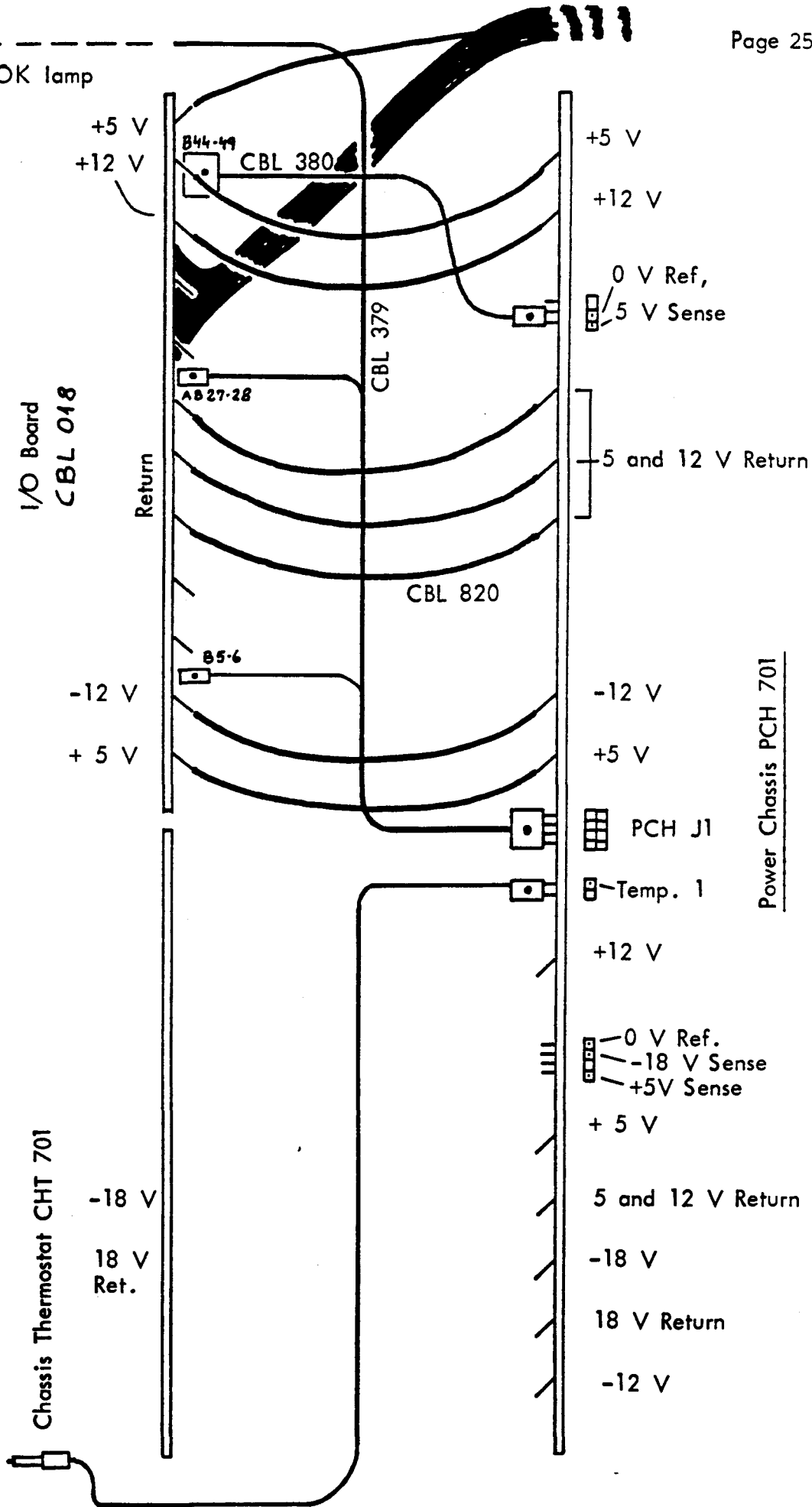
18.07.20  
NT



78.07.20  
NT

CABLE CONNECTIONS FOR POWER CHASSIS  
CHS 708

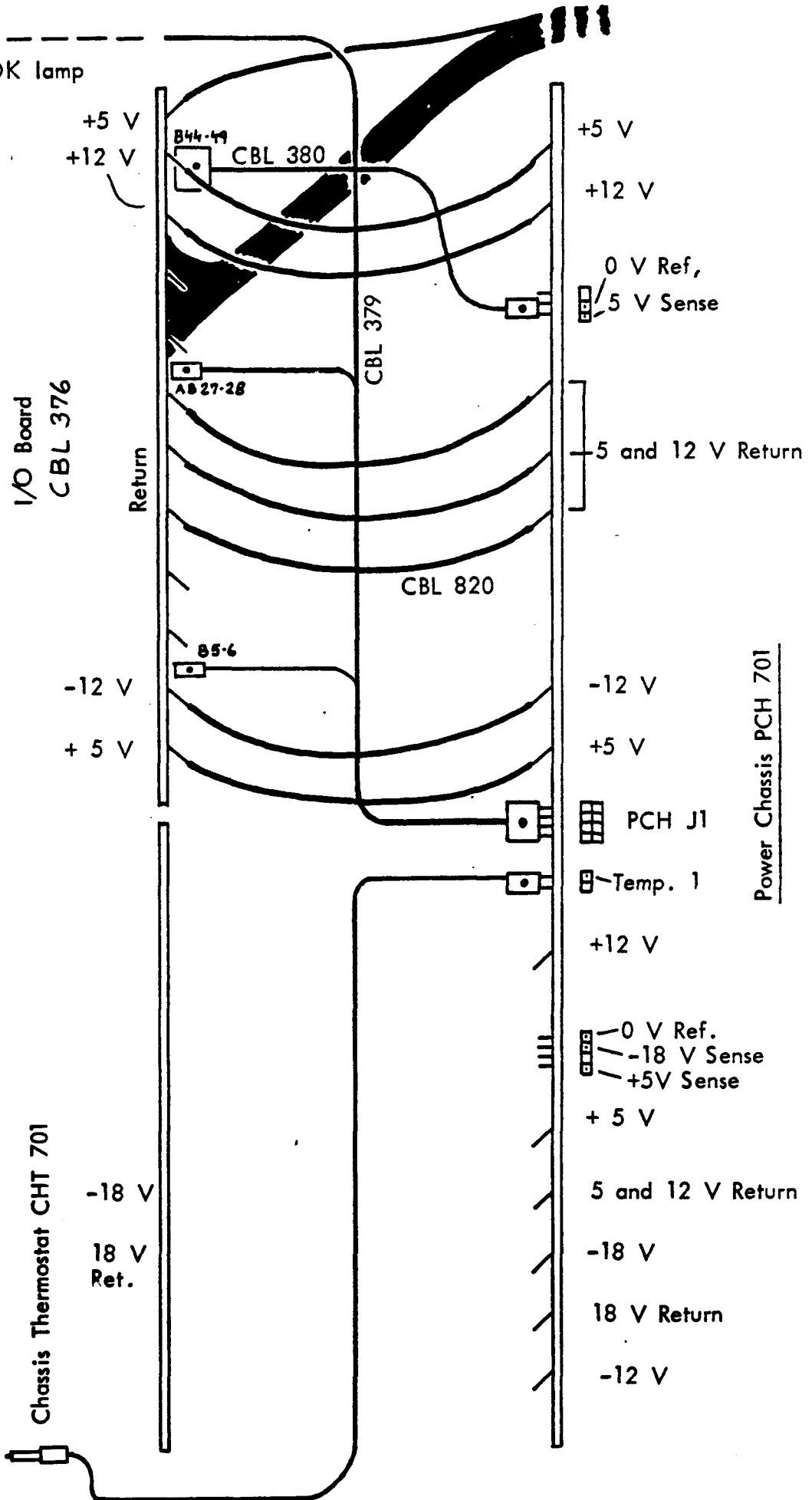
Main Chassis



78.07.20  
NT

CABLE CONNECTIONS FOR POWER CHASSIS  
CHS 709

Main Chassis



78.07.20  
NT

CABLE CONNECTIONS FOR POWER CHASSIS  
CHS 710

1

2

3

4

1

2

3

4