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Technical Manual for MEM720.

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Semiconductormemory, I/O controller.

Abstract:

This manual contains technical information on the MEM720 semiconductor-memory and I/O controller.

(76 printed pages)

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CONTENTS PAGE.

1. DESCRIPTION. 1

MEM720 is a multilayer printed circuit board, which contains two basic system modules intended for use in the RC3600 computer family.

The two main devices are:

1. 128 k bytes dynamic semiconductor memory.

2. An input/output controller containing:
   Two teletype controllers
   Paper Tape Reader controller
   Paper Tape punch controller
   Real Time Clock.

The MEM720 is designed to be mounted in the RC3600 CPU-chassis which provides connections between the CPU board and the MEM720 board by means of the two backplane motherboards: the memory bus motherboard, and the I/O-bus motherboard.

1.1 Memory. 1.1

The memory part of MEM720 contains 64 K words by 18 bit dynamic semiconductor memory. The 18 data bit are made up by 16 bit of information and two parity bits, one for each octet.

A memory module selection switch makes it possible to disable the whole or half of the memory array. If only 32 K words are enabled, these can be addressed in the address space from either 0 to 32 K or from 32 K to 64 K.

The memory is plug compatible with existing core memories (plug 1002), and it is possible to connect both types of memories to the memory bus, provided that only 32 K words of address space is enabled on the MEM720.

1.2 Input/Output Controllers 1.2

The I/O controllers are plug and interface compatible with the corresponding controllers on the existing IOC707 printed circuit board. The I/O controllers connects to the I/O Bus via plug 1003. The devices connects to the controllers via an internal chassis cable and plug 1004.

The device codes for the different controllers contained on the MEM720 are selected as one out of 16 combinations by means of a four bit switch.

2. SWITCH SETTINGS. 2.

The MEM720 contains several DIP-switches controlling memory address space, negative supply voltage source, I/O device codes and Baud-rates. Below, the function of each of these switches as well as the front panel toggle switch is described.

2.1 Memory Select Switch. 2.1

The memory select switch is located at position 112. It controles the memory size and the address space as illustrated in fig. 2.1.

Red dot visible ~"0"

Memory Size	Address Space	1 2 3 4
0	x	0 0 x x
32 K words	0-32 K	1 0 1 0
32 K words	32-64 K	0 1 1 0
64 K words	0-64 K	1 1 0 1

Fig. 2.1 Memory Select Switch.

2.2 Negative Voltage Source Switch. 2.2

The various integrated circuits on the MEM720 board presents the following combined demand for supply voltages: -12V, -5V, 0V, +5V and +12V.

The -5V is generated on the board from the -12V. The -12V, again is either supplied directly from the chassis power supply, or it can be generated on board from -18V. This feature facilitates installation of MEM720 in system previously equipped with core memory.

The DIP change over switch in position 1 is used to select either -12V or -18V as the primary negative supply voltage according to fig. 2.2.

Red dot visible ~"0"

1 2	Supply Voltage
0 0	N/A
0 1	-18V
1 0	-12V
1 1	N/A

Fig. 2.2.

2.3 Device Select Switch. 2.3

By means of the DIP-switch in location 132 the device code for the different I/O controllers can be selected according to the scheme in fig. 2.3.

Red dot visible ~ "0"

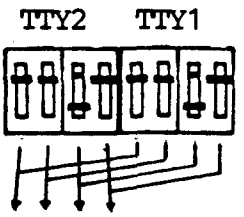
1 2 3 4	RTC	TRC	PUC	TTI1	TTO1	TTI2	TTO2
0 0 0 0	14	12	13	10	11	50	51
0 0 0 1	14	x	13	10	11	50	51
0 0 1 0	14	12	x	10	11	50	51
0 0 1 1	14	12	13	10	11	x	x
0 1 0 0	x	23	31	32	33	34	35
0 1 0 1	x	x	x	32	33	34	35
0 1 1 0	x	23	31	x	x	x	x
0 1 1 1	x	23	x	x	x	x	x
1 0 0 0	x	23	13	32	33	34	35
1 0 0 1	x	x	13	32	33	34	35
1 0 1 0	x	23	13	x	x	34	35
1 0 1 1	x	x	x	x	x	x	x
1 1 0 0	x	12	13	50	51	32	33
1 1 0 1	x	x	13	50	51	32	33
1 1 1 0	x	12	x	50	51	32	33
1 1 1 1	x	12	13	50	51	x	x

x: Disabled

Fig.2.3. Device Select Switch.

2.4 Baud-Rate Select Switches. 2.4

The baud-rates of the two teletypecontrollers are selected using the DIP switches in position 136. (Refer to fig. 2.4).



Red dot visible ~ "0"

A	B	C	D	Baud Rate (bps)
0	0	0	0	Off
0	0	0	1	50
0	0	1	0	75
0	0	1	1	110
0	1	0	0	134.5
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	900
1	0	0	1	1200
1	0	1	0	1800
1	0	1	1	2400
1	1	0	0	3600
1	1	0	1	4800
1	1	1	0	7200
1	1	1	1	9600

Fig. 2.4 Baud Rate Switches.

2.5 Memory Initialization Inhibit Switch. 2.5

Following a power up condition the MEM720 initialize the memory by writing all ones into the array thereby providing each byte with correct parity.

The power low condition is recognized by the MEM720 as a low level on the POK (Power OK) signal from the I/O bus. In order

to make it possible to switch off power from other chassis in the system without destroying the loaded program, a memory reset inhibit switch is supplied on the front panel.

The reset inhibit switch is momentary activ, and once activated the inhibit mode is selected, indicated by the front panel light emitting diode. In this mode the POK signal will have no effect on the memory.

The reset inhibit condition will last until power is removed from the MEM720 board.

3. BLOCK DIAGRAM

3.

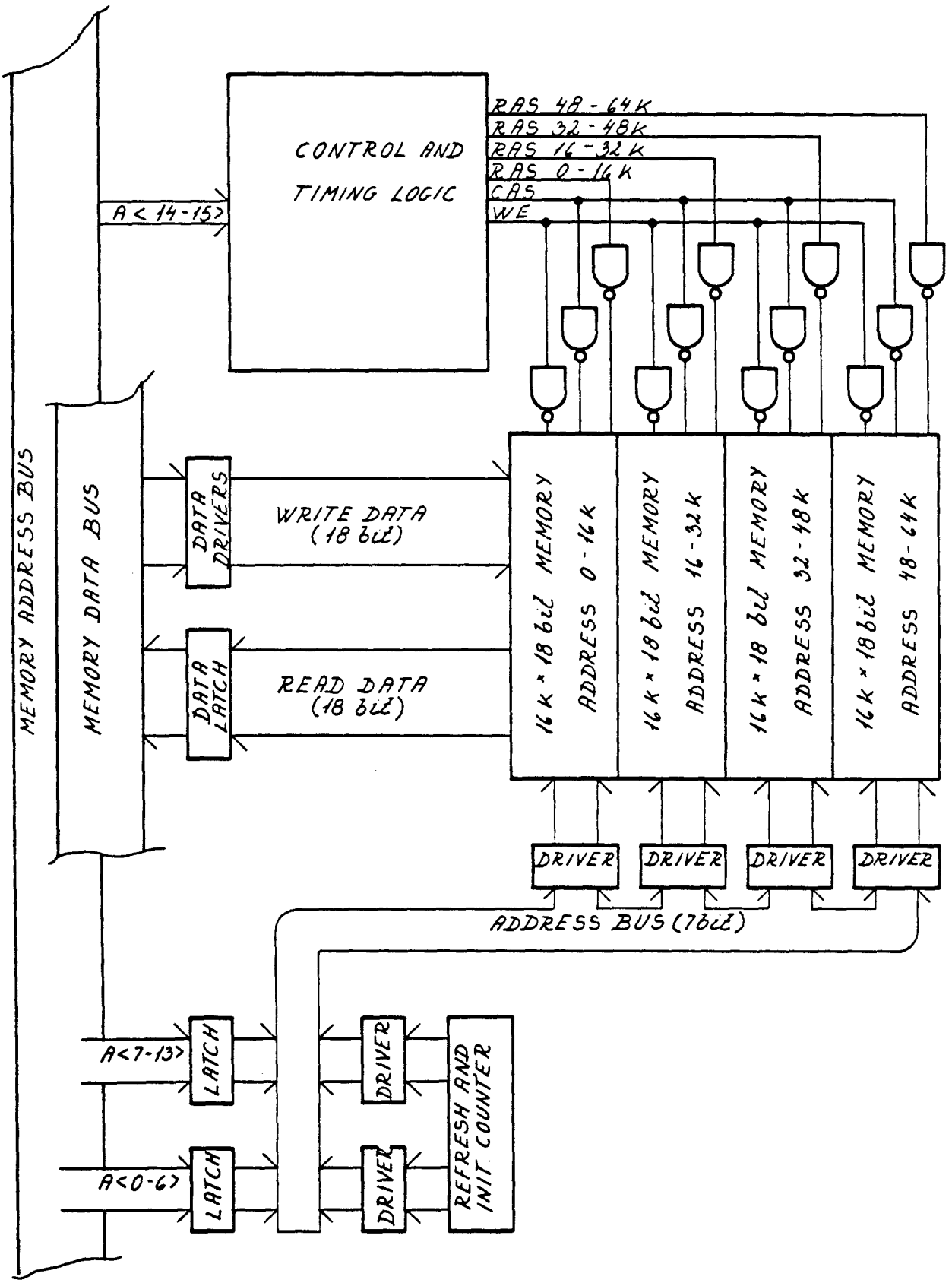
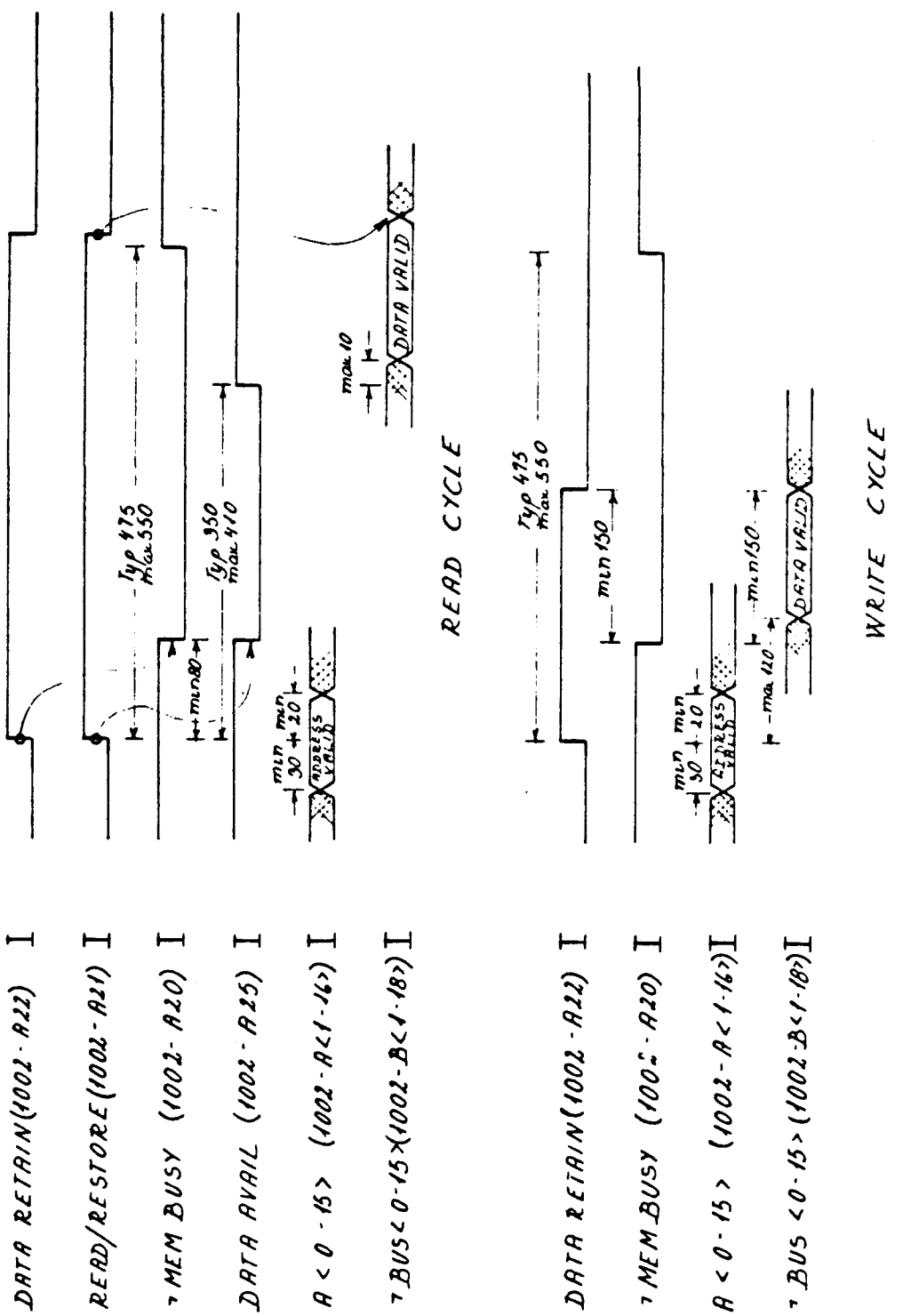


Fig. 3.1. Block Diagram of Memory.

4. TIMING DIAGRAMS. 4.



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MEM 720

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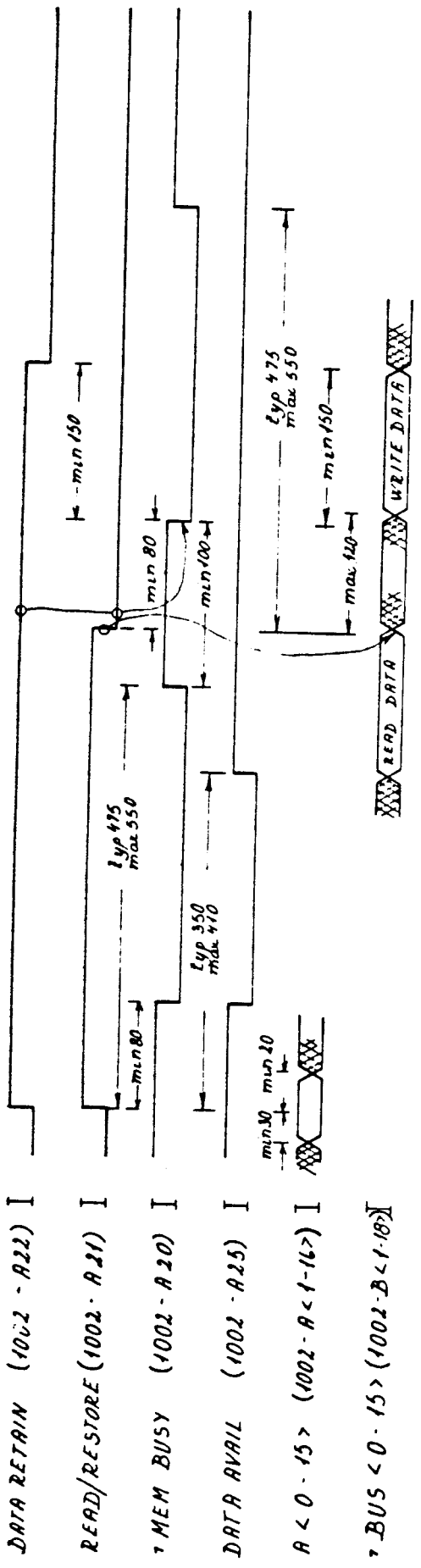
READ / WRITE CYCLE TIMING DIAGRAM

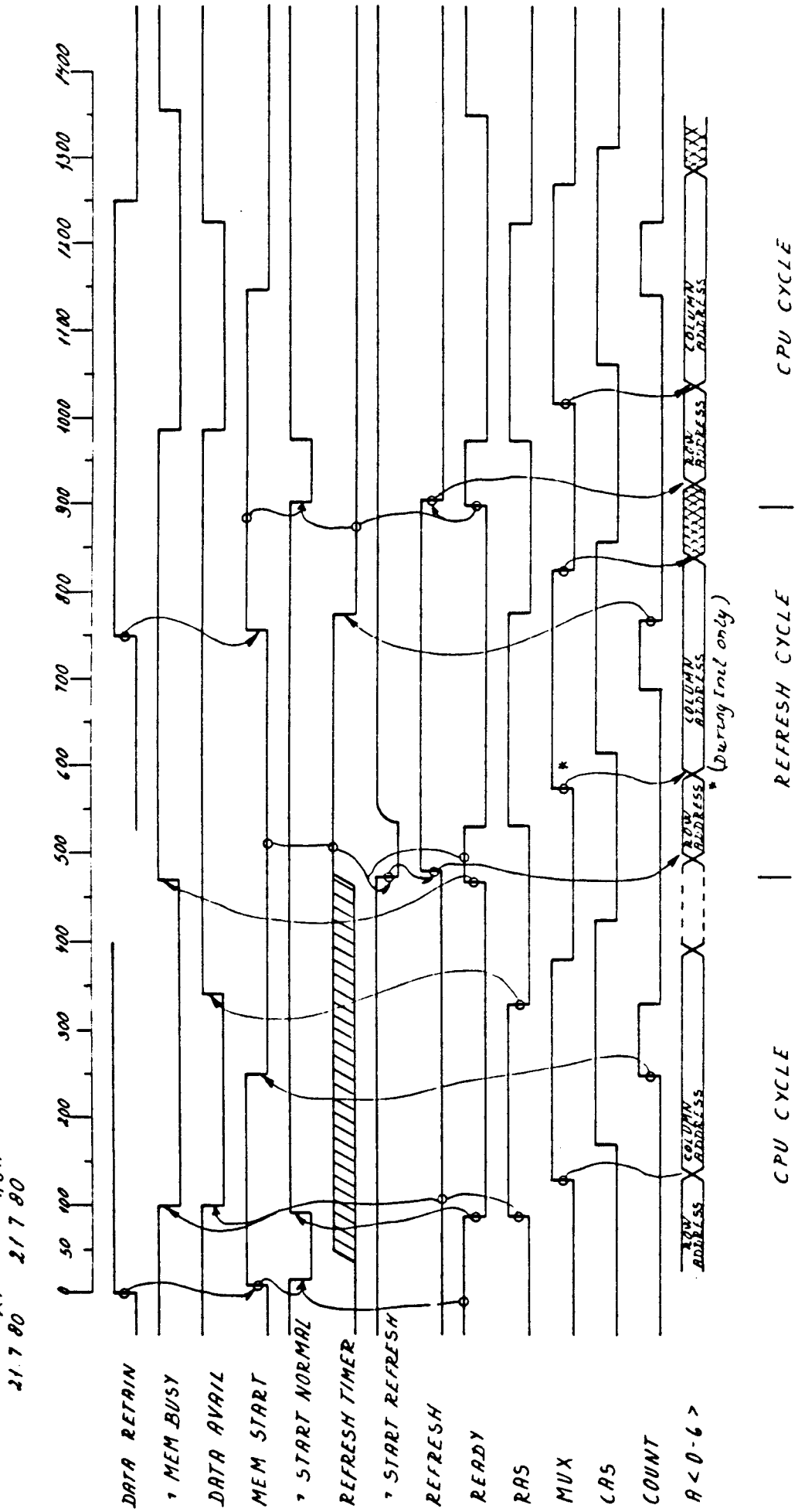


Read - Modify - Write Cycle

Read - Modify - Write Cycle
Timing Diagram

MEM 720

R 12919



MEM 720

R 12918

REFRESH CYCLE
TIMING DIAGRAM

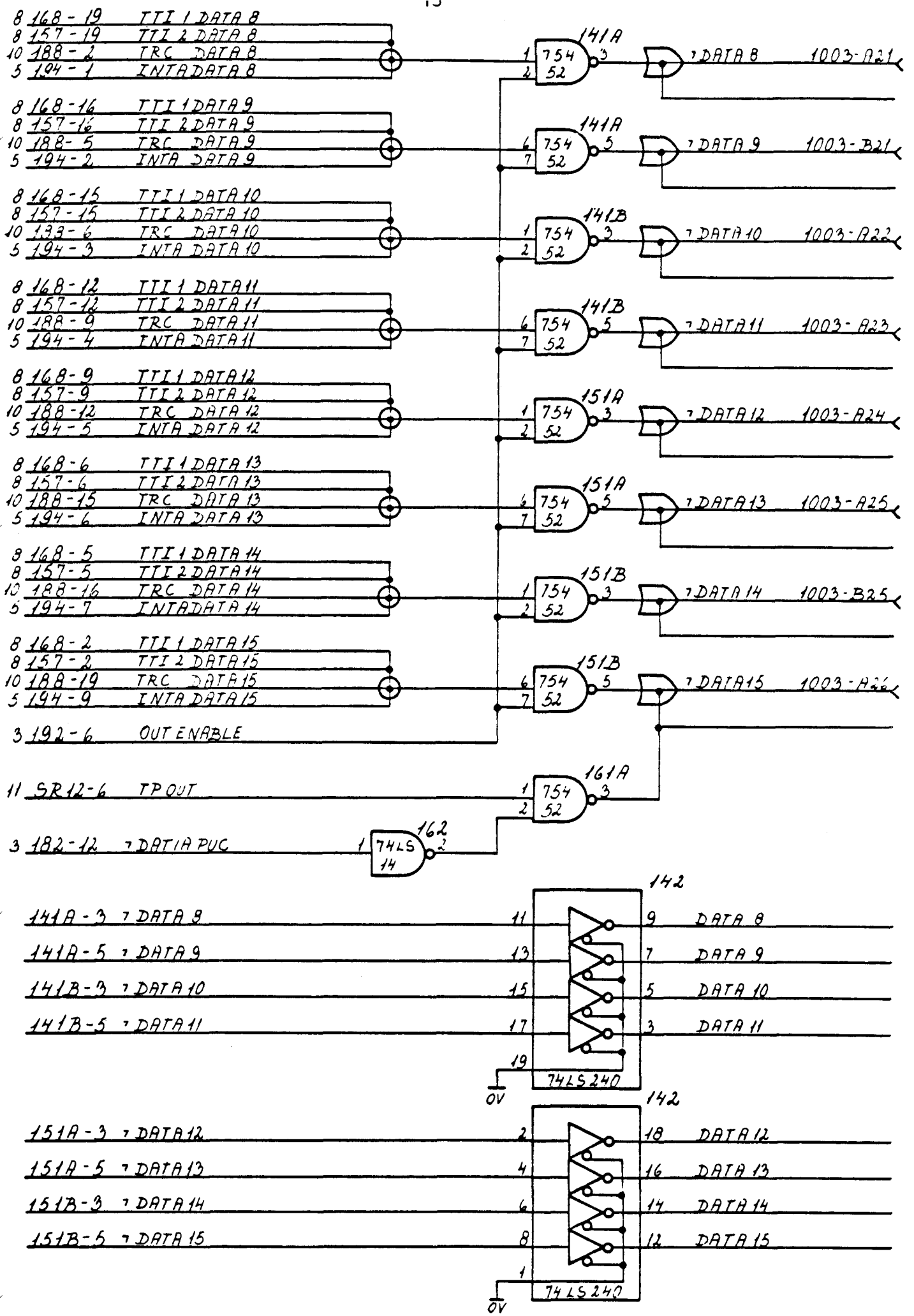
5. LOGIC DIAGRAMS AND FUNCTIONAL DESCRIPTION. 5.

The following right hand pages contain logic diagrams for MEM720. A functional description for every sheet of diagram is found on the corresponding left hand page.

The functional description consists of a schematic listing of all signals generated on the page. A short description and a listing of the diagrams to which the signal is transferred is given for each signal.

NOTE: All references between individual diagrams make use of diagram numbers (lower right corner) and not page numbers (upper right corner).

SIGNAL	DESTI-NATION	DESCRIPTION
→ DATA <8-15>	1003	The I/O Data bus
DATA 8	IOC 8 IOC11	Output data bus
DATA 9	IOC 8 IOC 11	
DATA 10	IOC 8 IOC 11	
DATA 11	IOC 5 IOC 8 IOC 11	
DATA 12	IOC 8 IOC 11	
DATA 13	IOC 5 IOC 8 IOC 11	
DATA 14	IOC 5 IOC 6 IOC 8 IOC 11	
DATA 15	IOC 5 IOC 6 IOC 8 IOC 11	



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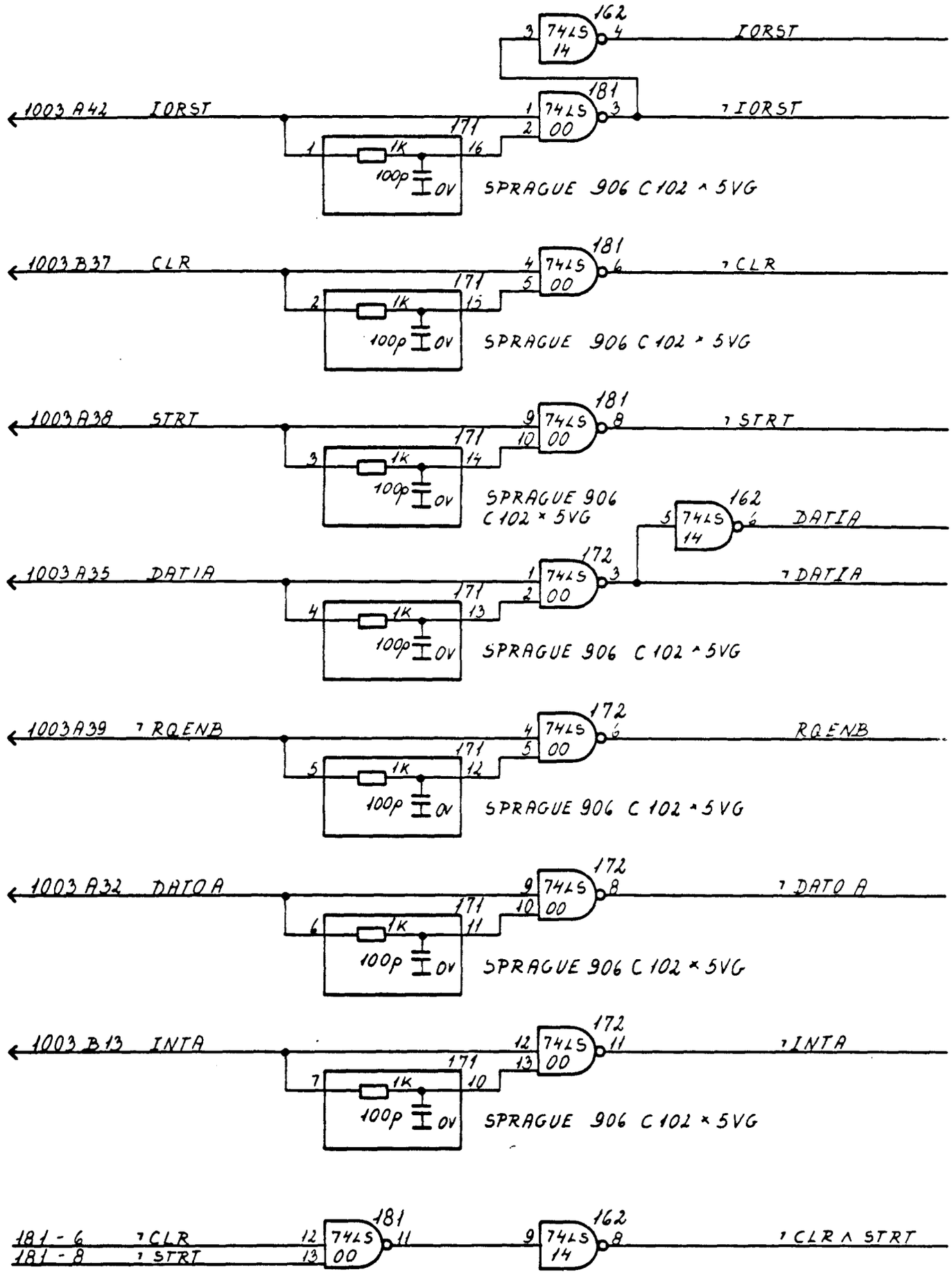
MEM 720

I/O BUS DRIVERS & RECEIVERS

IOC 1

2 12893

SIGNAL	DESTI-NATION	DESCRIPTION
IORST	IOC 6	Received I/O Reset Signal
⊃IORST	IOC 4 IOC 5 IOC 6 IOC 11	
⊃ CLR	IOC 4 IOC 5	Received Clear Pulse
⊃ STRT	IOC 4	Received Start Pulse
DATIA		Received Data Input A Signal
⊃DATIA	IOC 3	
RQENB	IOC 5	Received Request Enable Signal
⊃DATOA	IOC 3	Received Data Output A Signal
⊃INTA	IOC 3 IOC 5	Received Interrupt Acknowledge Signal
⊃CLR ∧STRT	IOC 4	A Clear or a Start pulse received



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I/O CONTROL SIGNAL RECEIVERS

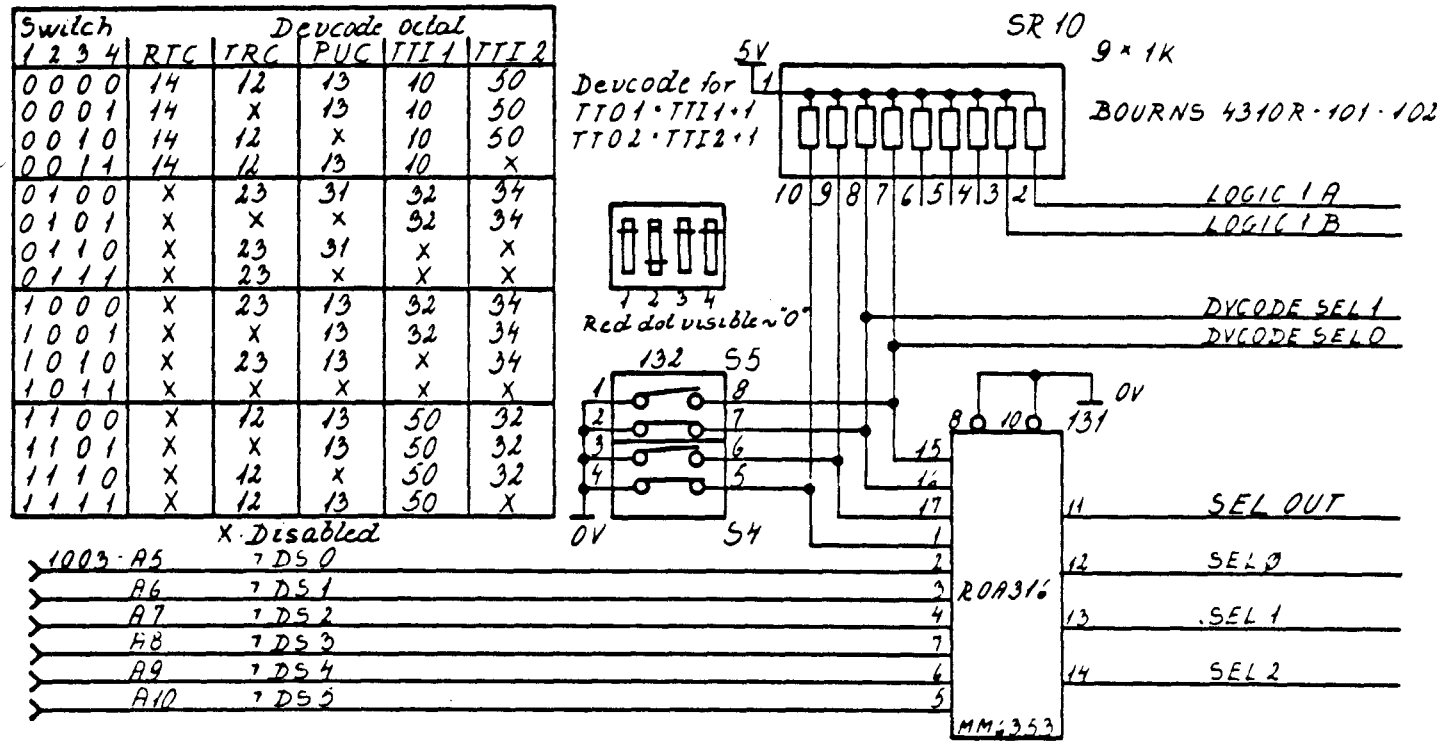
IOC 2

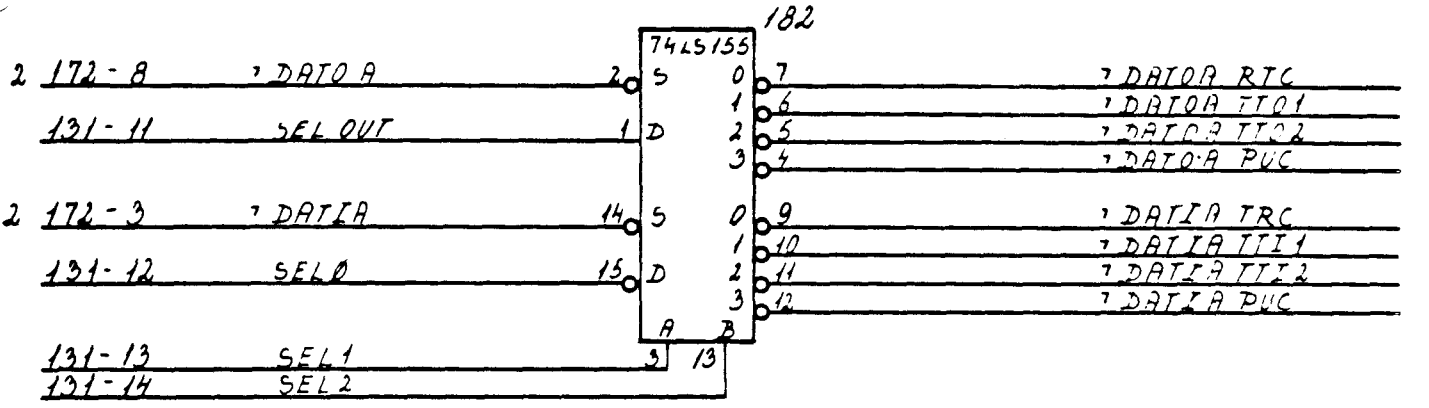
R 12894

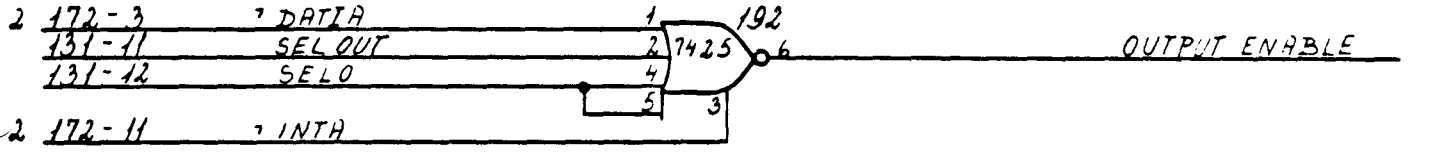
SIGNAL	DESTI-NATION	DESCRIPTION
LOGIC 1 A	IOC 4 IOC 5 IOC 6	1 K ohm pull up.
LOGIC 1 B	IOC 6	Pull up for IORST delay
DVCODE SEL 1	IOC 5	Selects one out of four
DVCODE SEL 2	IOC 6	Groups of device codes
SEL OUT	IOC 3	An output device is selected
SEL ⟨0-2⟩	IOC 3 IOC 4	Selects one out seven devices. The code 4 (octal) is dummy
⁄DATOA RTC	IOC 6	Selected Data output Strobe
⁄DATOA TTO1	IOC 8	- " -
⁄DATOA TTO2	IOC 8	- " -
⁄DATOA PUC	IOC 11	- " -
⁄DATIA TRC	IOC 10	Selected Data input Strobe
⁄DATIA TTI1	IOC 8	- " -
⁄DATIA TTI2	IOC 8	- " -
⁄DATIA PUC	IOC 1	- " -

Switch 1 2 3 4	RTC	TRC	PUC	TTI 1	TTI 2
0 0 0 0	14	12	13	10	50
0 0 0 1	14	X	13	10	50
0 0 1 0	14	12	X	10	50
0 0 1 1	14	12	13	10	X
0 1 0 0	X	23	31	32	34
0 1 0 1	X	X	X	32	34
0 1 1 0	X	23	31	X	X
0 1 1 1	X	23	X	X	X
1 0 0 0	X	23	13	32	34
1 0 0 1	X	X	13	32	34
1 0 1 0	X	23	13	X	34
1 0 1 1	X	X	X	X	X
1 1 0 0	X	12	13	50	32
1 1 0 1	X	X	13	50	32
1 1 1 0	X	12	X	50	32
1 1 1 1	X	12	13	50	X

X · Disabled







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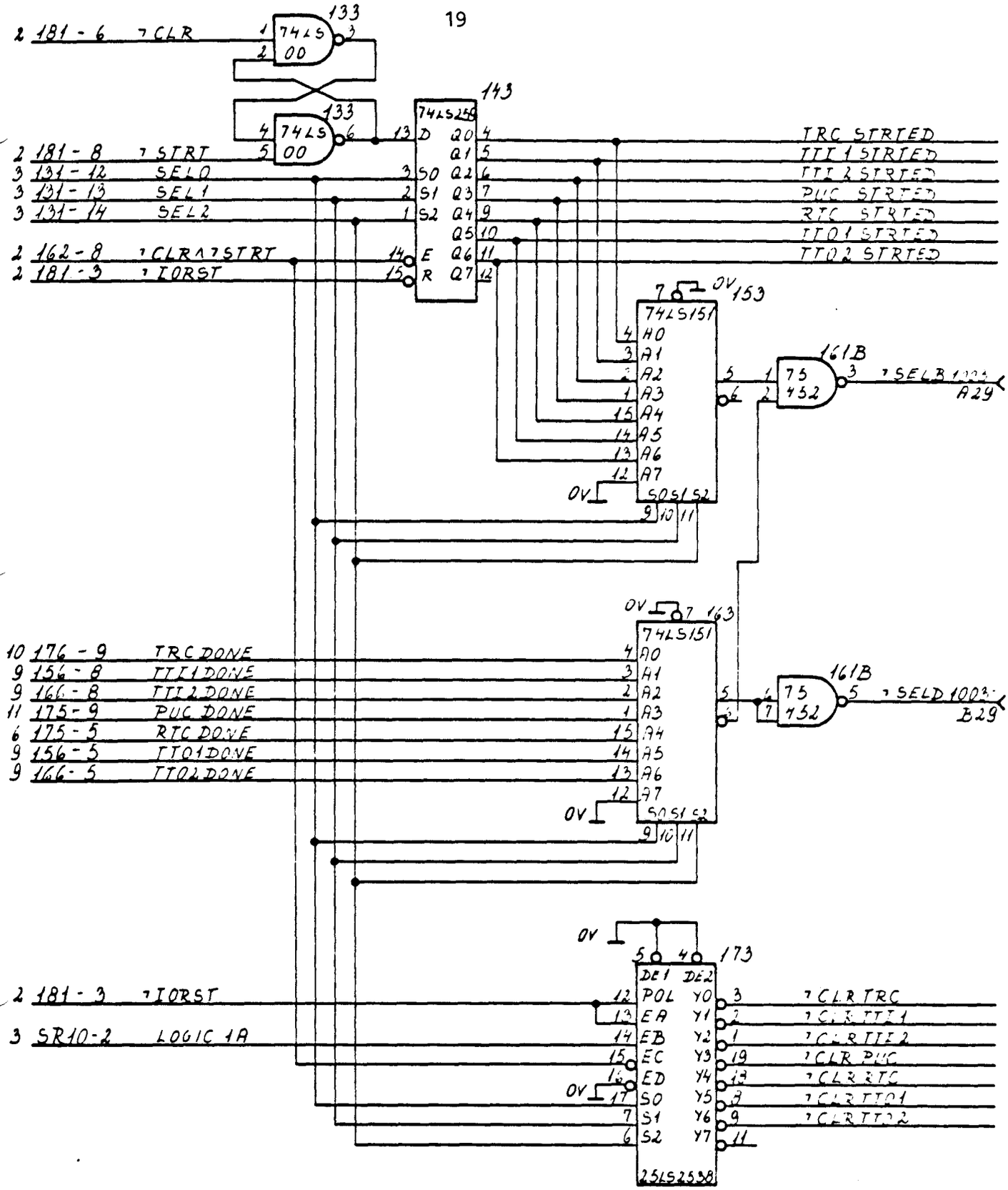
MEM 720

DEVICE SELECT LOGIC

IOC 3

R 12895

SIGNAL	DESTI-NATION	DESCRIPTION
TRC STRTED	IOC 10	Selected and latched start pulse
TTI1 STRTED		- " -
TTI2 STRTED		- " -
PUC STRTED	IOC 11	- " -
RTC STRTED	IOC 6	- " -
TTO1 STRTED	IOC 9	- " -
TTO2 STRTED	IOC 9	- " -
⁊SELB	1003	Selected Busy Signal
⁊SELD	1003	Selected Done Signal
⁊CLR TRC	IOC 10	Selected Start or Clear, or I/O Reset pulse
⁊CLR TTI1	IOC 8	- " -
⁊CLR TTI2	IOC 8	- " -
⁊CLR PUC	IOC 11	- " -
⁊CLR RTC	IOC 6	- " -
⁊CLR TTO1	IOC 9	- " -
⁊CLR TTO2	IOC 9	- " -



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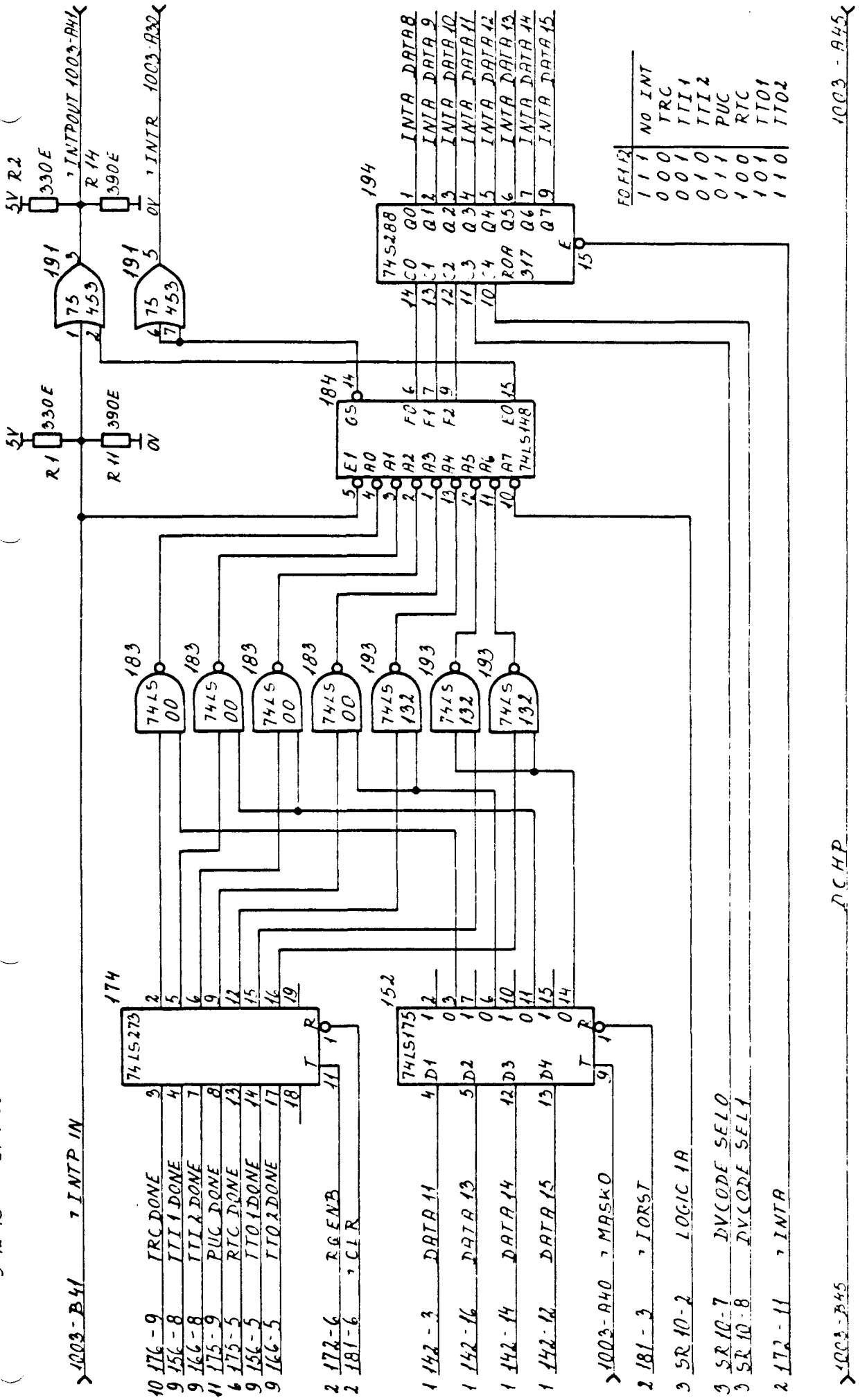
BUSY/DONE CONTROL LOGIC

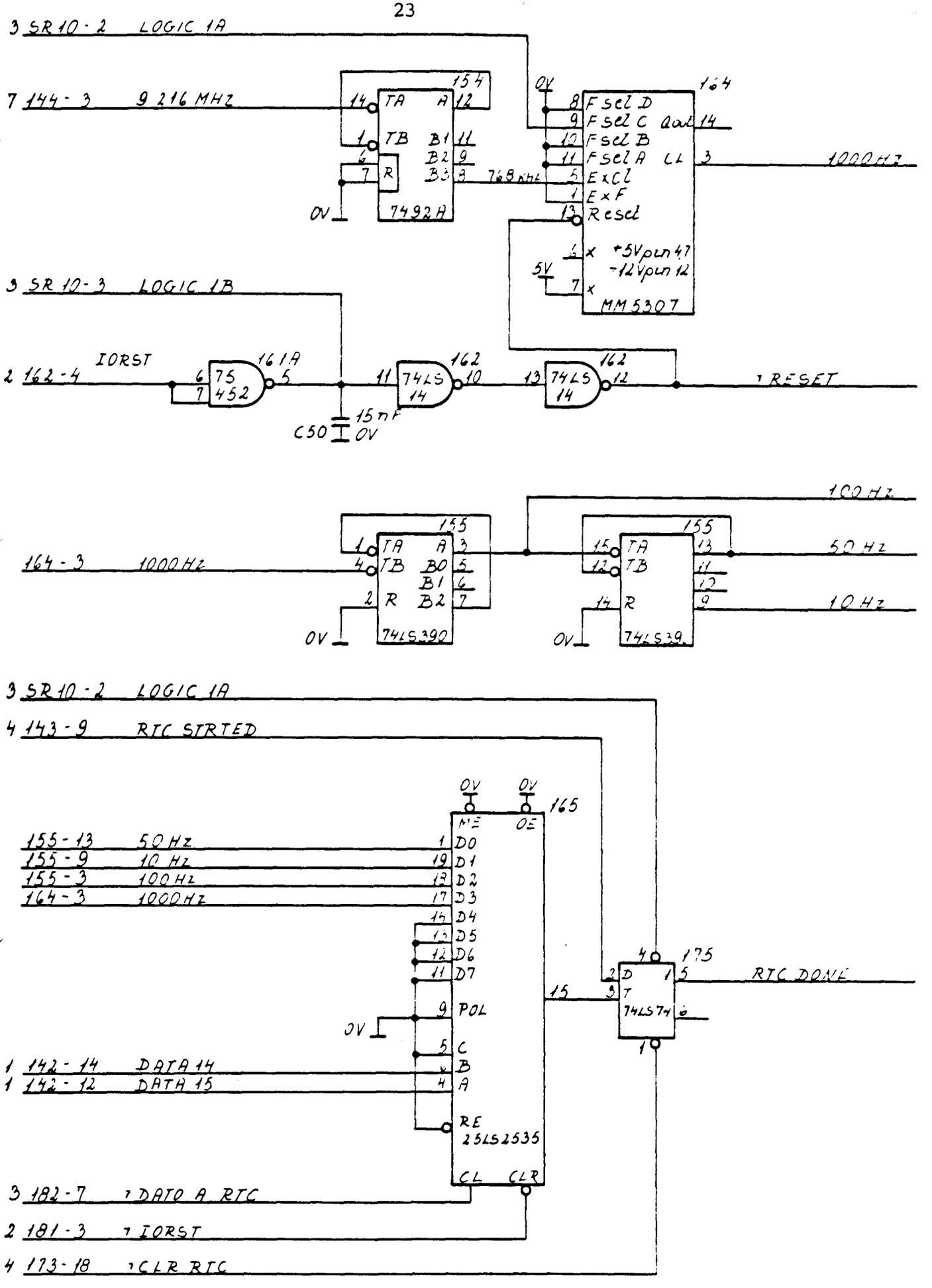
IOC 4

R 12896

SIGNAL	DESTI-NATION	DESCRIPTION
⁊INTPOUT	1003	Serial Interrupt Priority output signal
⁊INTR	1003	Interrupt Request
INTA DATA ‹8-15›	IOC 1	Contains the device-code of the interrupting controller during interrupt acknowledge.
DCHP	1003	Data Channel Priority signal


5V R2
330E
R 14
390E
0V
~INTPOUT 1003-B41
~INTR 1003-A32
191
75 453
5V
330E
R 1
390E
R 11
0V
184
74LS148
194
74S288
INTA DATA8
INTA DATA 9
INTA DATA 10
INTA DATA 11
INTA DATA 12
INTA DATA 13
INTA DATA 14
INTA DATA 15
FQFI/2
NO INT
TRC
TTI1
TTI2
PUC
RTC
TTO1
TTO2
183
7415 00
193
7415 132
174
74LS273
152
74LS175
TRC DONE
TTI1 DONE
TTI2 DONE
PUC DONE
RTC DONE
TTO1 DONE
TTO2 DONE
R GENB
~CLR
DATA 11
DATA 13
DATA 14
DATA 15
1003-A40 ~MASKO
~IORST
LOGIC 1A
DVCODE SEL0
DVCODE SEL1
~INTA
~INTP IN
1003-B41
1003-A45
DCHP

SIGNAL	DESTI-NATION	DESCRIPTION
>RESET	IOC 6 IOC 7	Stretched I/O Reset signal
1000 Hz	IOC 6	
100 Hz	IOC 6	
50 Hz	IOC 6	
10 Hz	IOC 6	
RTC DONE	IOC 4 IOC 5	



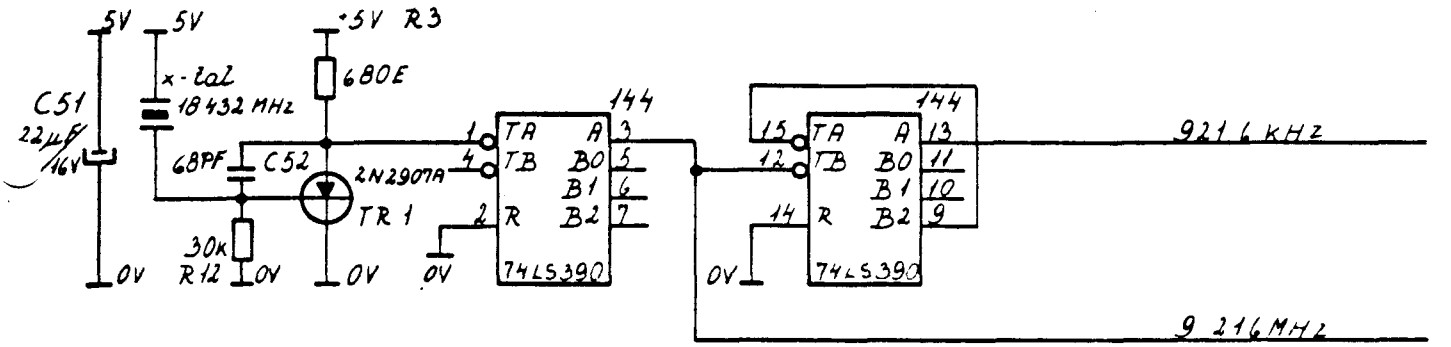
MEM 720

REAL TIME CLOCK

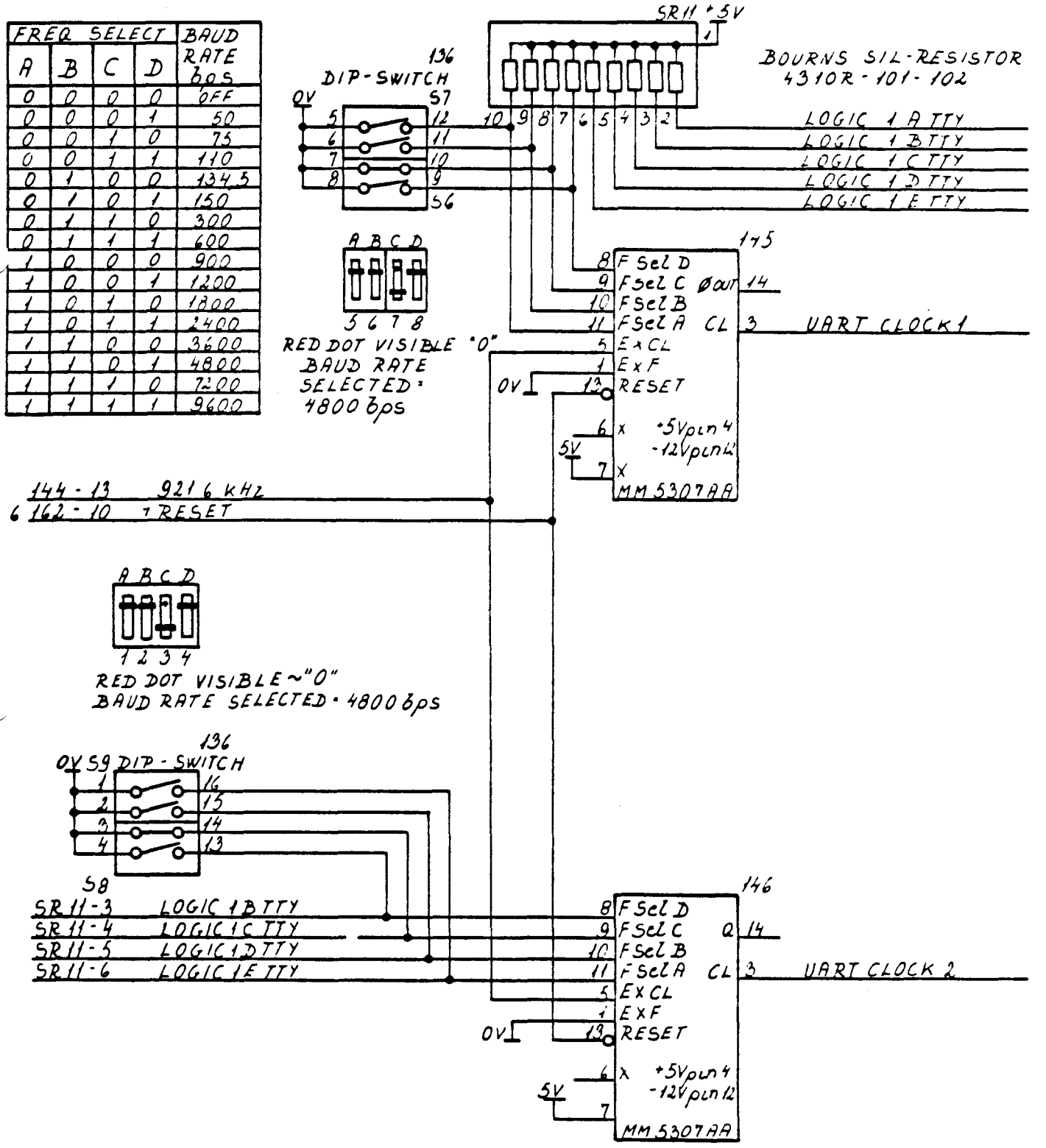
IOC 6

R 12898

SIGNAL	DESTI-NATION	DESCRIPTION
921.6 KHz	IOC 7	
9.216 MHz	IOC 6	RTC clock.
LOGIC 1 ‹A-E› TTY	IOC 7	Pull up for UART no. 2 frequency select
UART CLOCK 1	IOC 8	Clock for the asynchronous transmitter and receiver
UART CLOCK 2	IOC 8	- " -



FREQ SELECT				BAUD RATE bps
A	B	C	D	
0	0	0	0	OFF
0	0	0	1	50
0	0	1	0	75
0	0	1	1	110
0	1	0	0	134.5
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	900
1	0	0	1	1200
1	0	1	0	1800
1	0	1	1	2400
1	1	0	0	3600
1	1	0	1	4800
1	1	1	0	7200
1	1	1	1	9600



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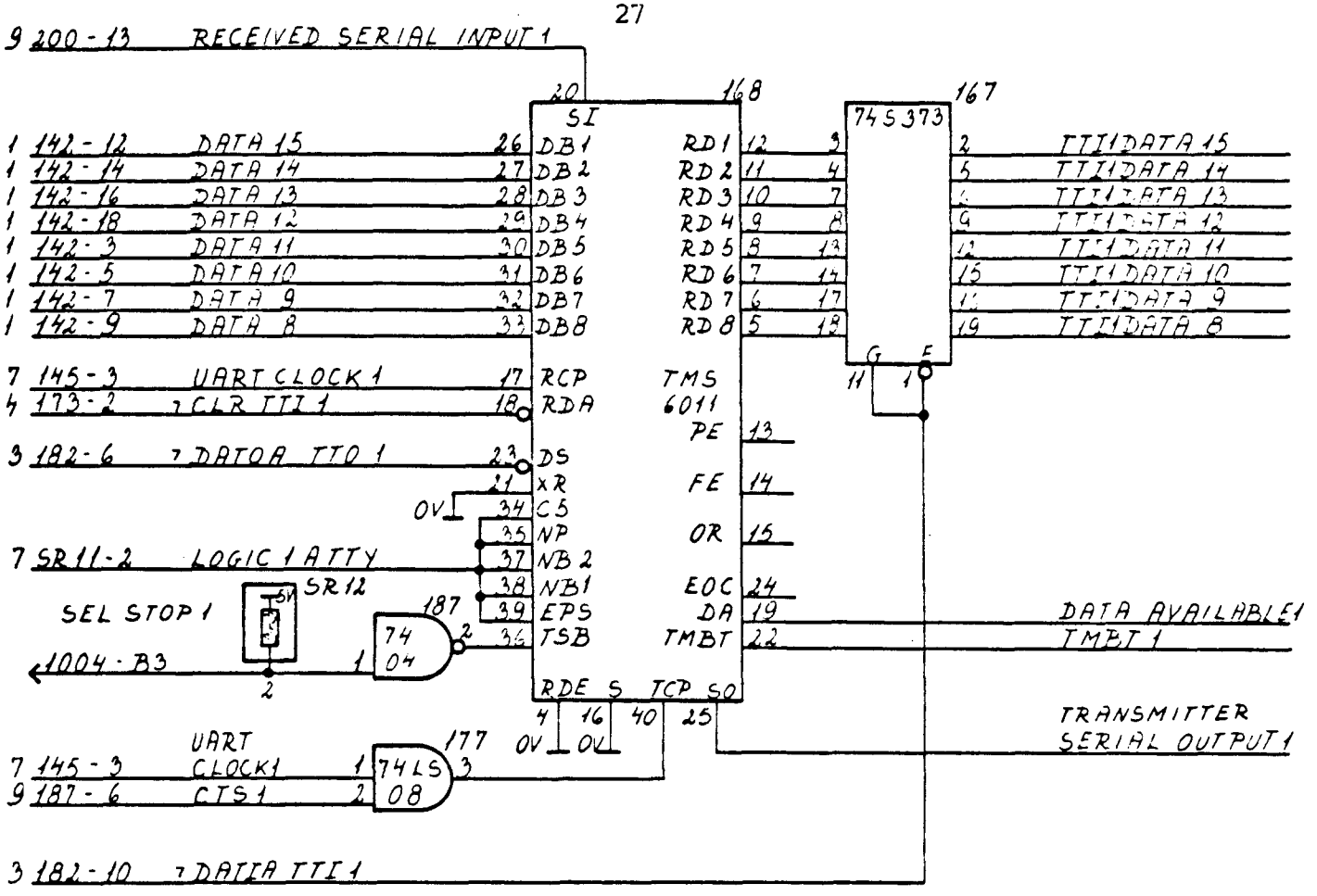
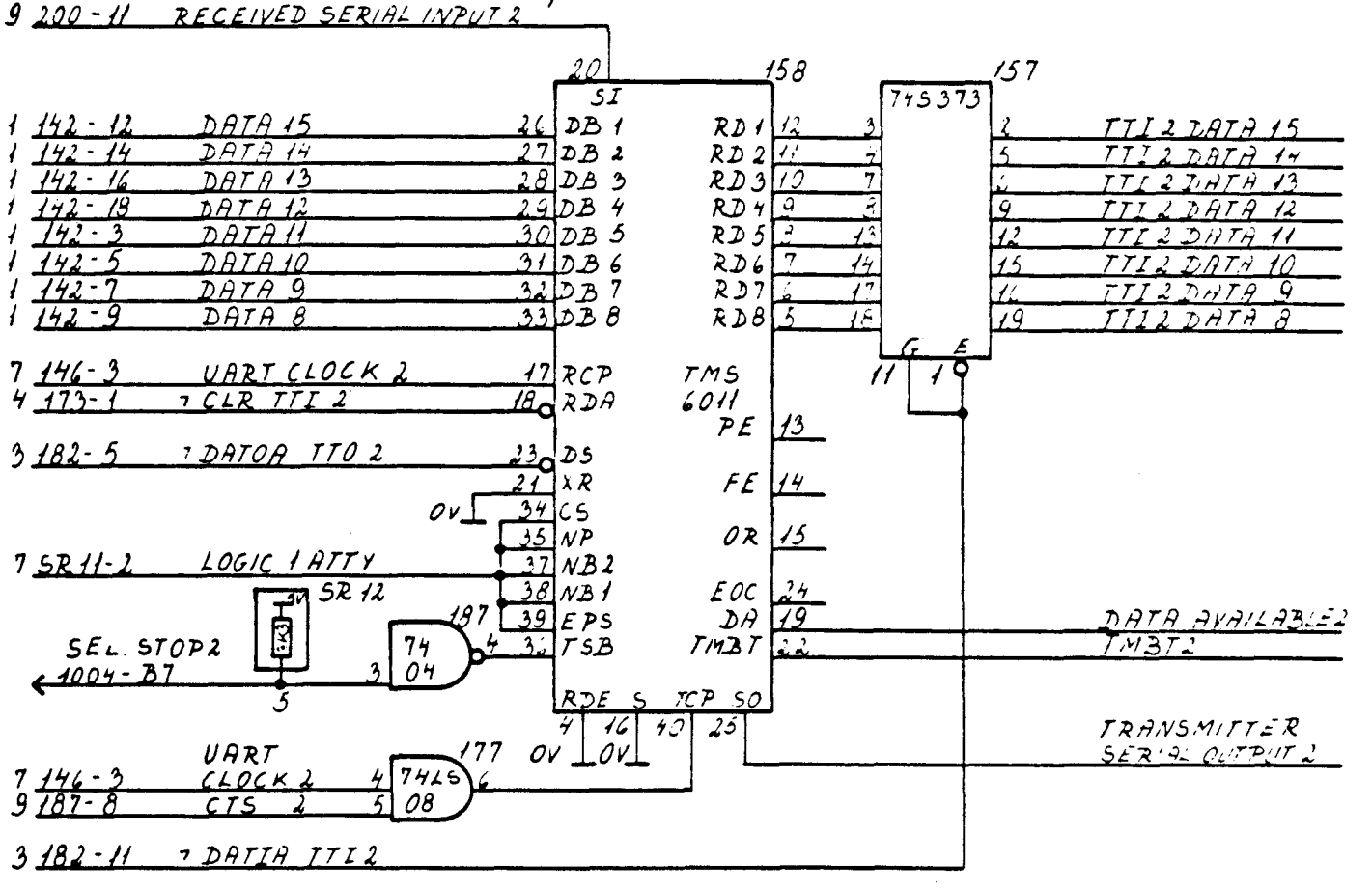
SIGNAL	DESTI-NATION	DESCRIPTION
TTI1 DATA <8-15>	IOC 1	Input Data bus
DATA AVAILABLE 1	IOC 9	Set TTI1 Done flag
TMBT 1	IOC 9	Set TTO1 Done flag
TTI2 DATA <8-15>	IOC 1	Intput Data bus
DATA AVAILABLE 2	IOC 9	Set TTI1 Done flag
TMBT 2	IOC 9	Set TTO1 Done flag
SERIAL OUTPUT 2	IOC 9	

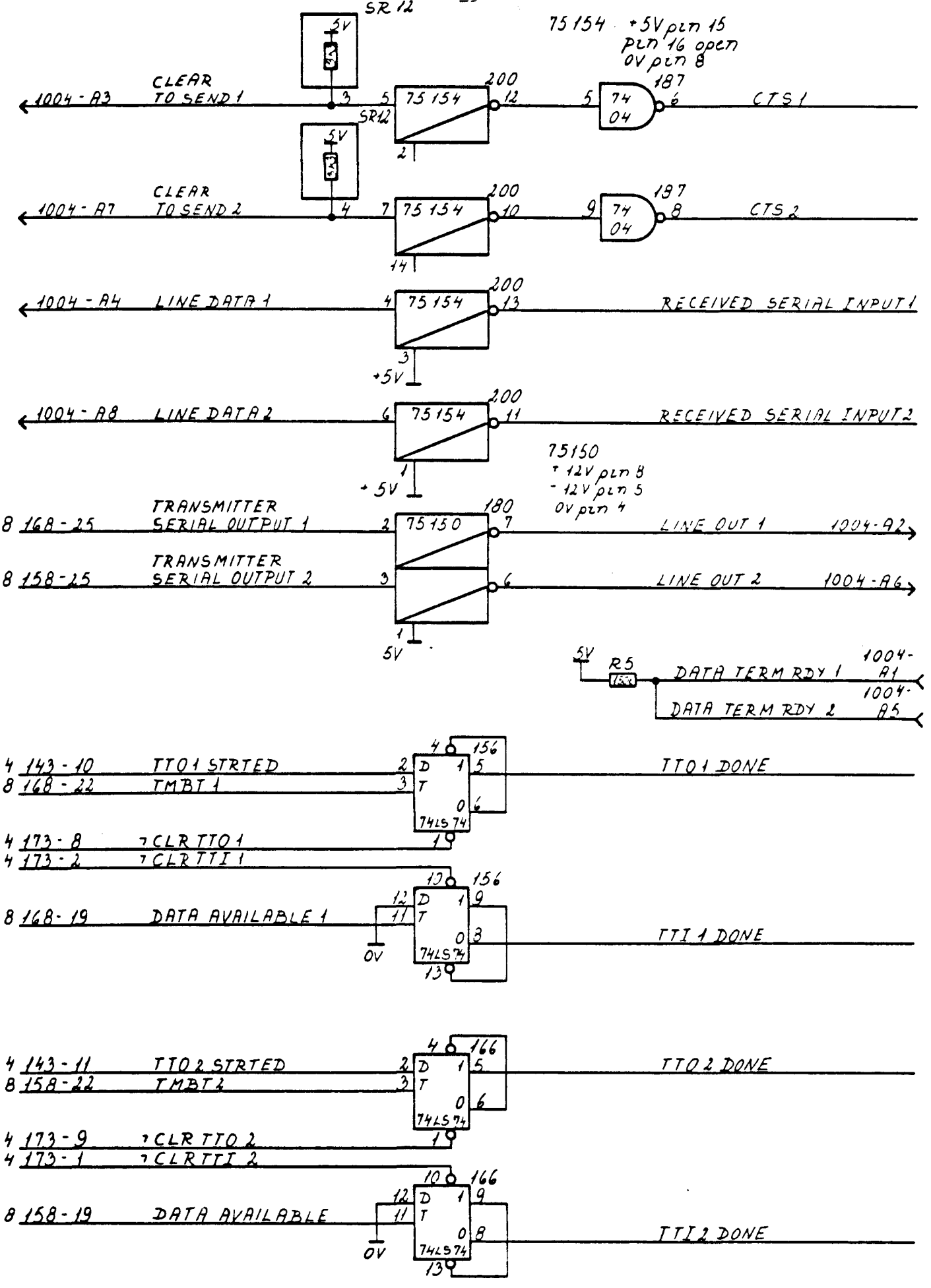


TMS 6011
pin 1 +5V
pin 2 -12V
pin 3 0V

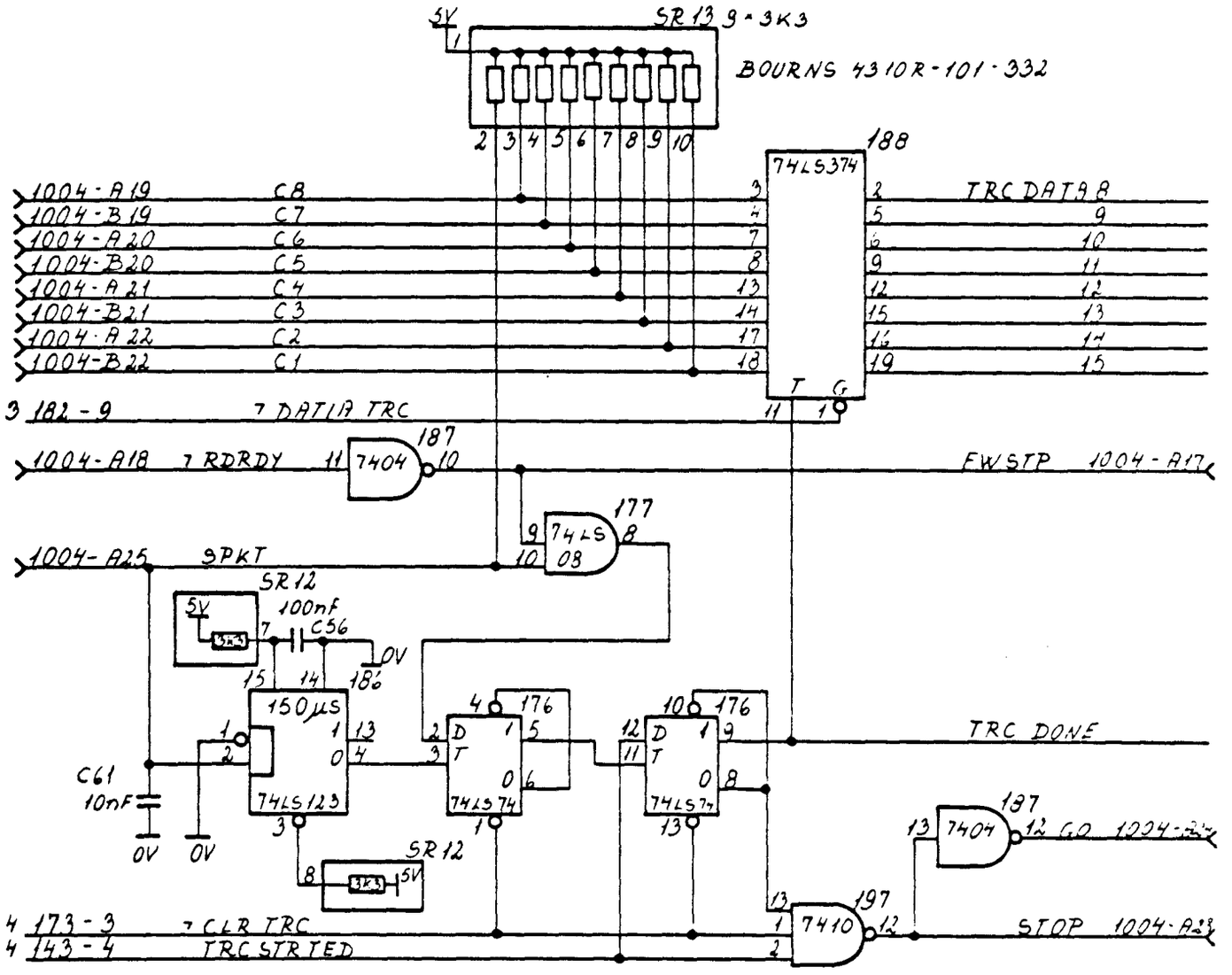


KF 21780 AGA 5 12 79

SIGNAL	DESTI-NATION	DESCRIPTION
CTS 1	IOC 8	Received Clear to Send Signal
CTS 2	IOC 8	- " -
SERIAL INPUT 1	IOC 8	Received serial data
SERIAL INPUT 2	IOC 8	- " -
LINE OUT 1	1004	Serial data output
LINE OUT 2	1004	- " -
DATA TERM RDY 1	1004	
DATA TERM RDY 2	1004	
TTO 1 DONE	IOC 4 IOC 5	Done flags
TTI 1 DONE	IOC 4 IOC 5	
TTO 2 DONE	IOC 4 IOC 5	
TTI 1 DONE	IOC 4 IOC 5	

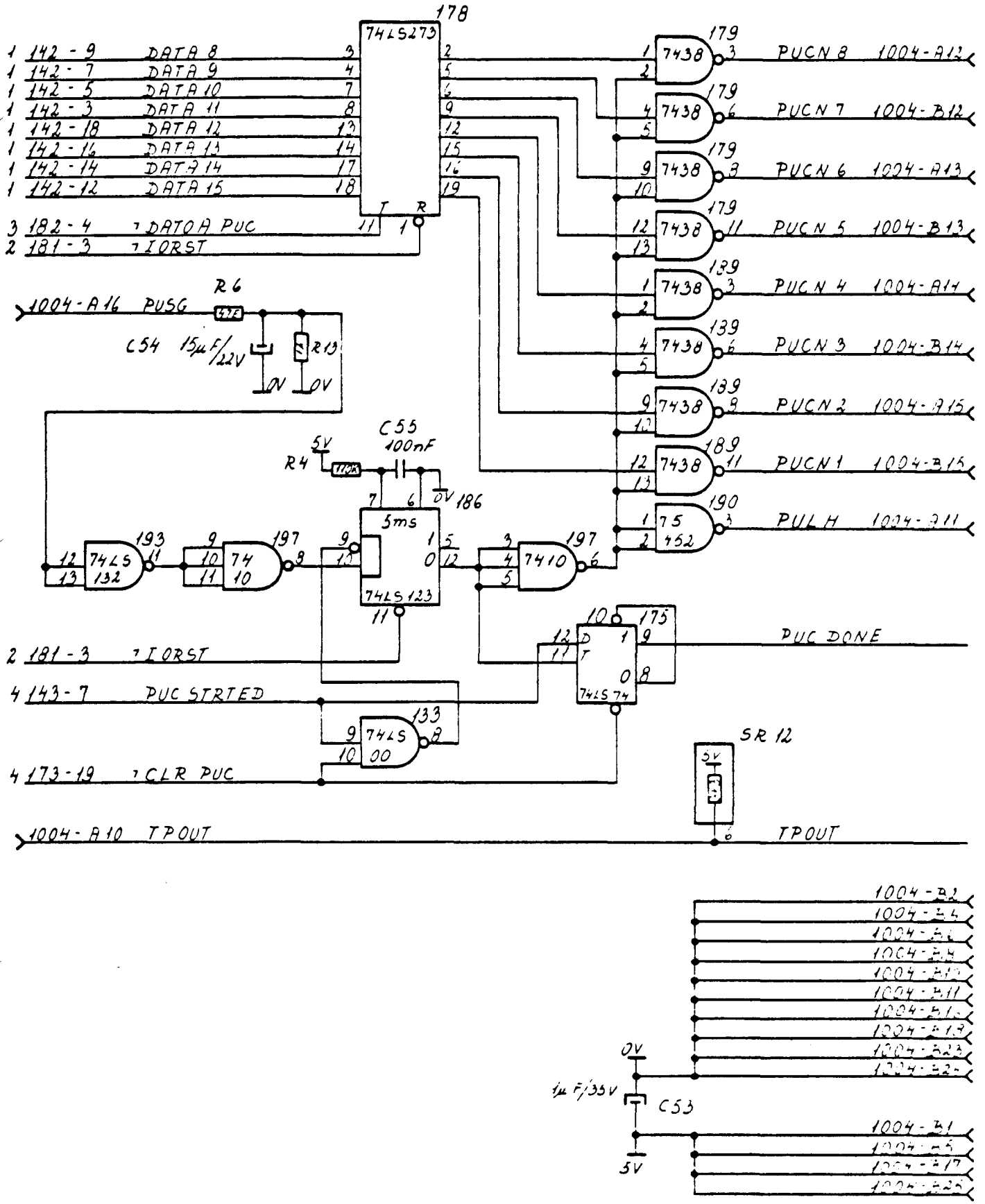

SR 12
5V
75154 +5V pin 15
pin 16 open
0V pin 8
1004-A3
CLEAR TO SEND 1
75154
200
74 04
187
CTS 1
SR12
1004-A7
CLEAR TO SEND 2
CTS 2
1004-A4
LINE DATA 1
RECEIVED SERIAL INPUT 1
+5V
1004-A8
LINE DATA 2
RECEIVED SERIAL INPUT 2
75150
+12V pin 8
-12V pin 5
0V pin 4
180
8 168-25
TRANSMITTER SERIAL OUTPUT 1
LINE OUT 1
1004-A2
8 158-25
TRANSMITTER SERIAL OUTPUT 2
LINE OUT 2
1004-A6
R5
DATA TERM RDY 1
1004-A1
DATA TERM RDY 2
1004-A5
4 143-10
TTO 1 STRTED
8 168-22
TMBT 1
TTO 1 DONE
156
74LS74
4 173-8
CLR TTO 1
4 173-2
CLR TTI 1
8 168-19
DATA AVAILABLE 1
TTI 1 DONE
0V
4 143-11
TTO 2 STRTED
8 158-22
TMBT 2
TTO 2 DONE
166
4 173-9
CLR TTO 2
4 173-1
CLR TTI 2
8 158-19
DATA AVAILABLE
TTI 2 DONE
KF 5 12 79 AGA 11 7 80

SIGNAL	DESTI-NATION	DESCRIPTION
TRC DATA <8-15>	IOC 1	Input Data Bus
FWSTP	1004	Forward Step
TRC DONE	IOC 4 IOC 5	Done flag
GO	1004	Character Request
STOP	1004	



KF 21 7 80 AGA
5 12 79

SIGNAL	DESTI-NATION	DESCRIPTION
PUCN ‹1-8›	1004	Data output channel 1 to 8
PULH	1004	Data output strobe
PUC DONE	IOC 4 IOC 5	Done flag
TP OUT	IOC 1	Tape Low status signal



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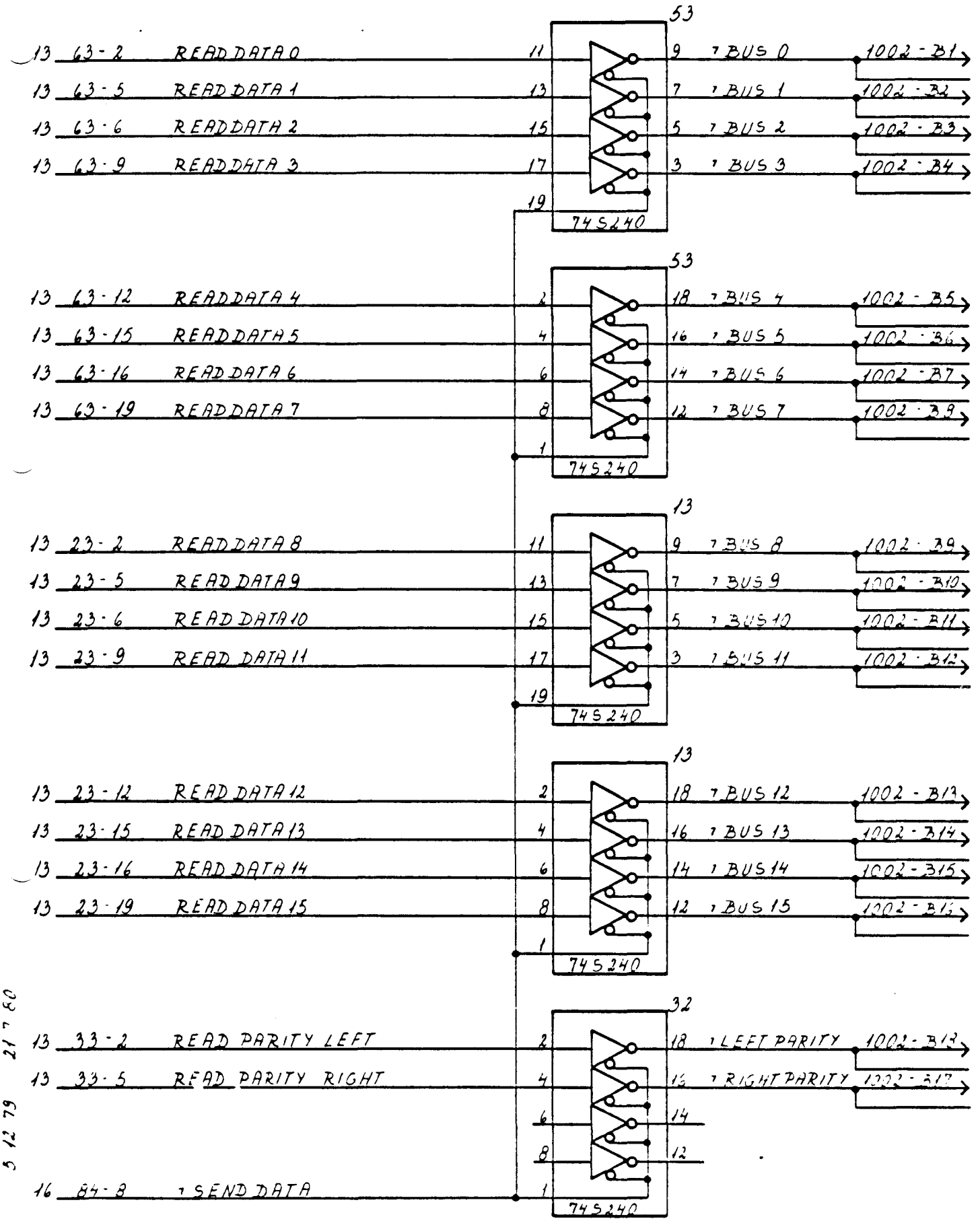
PAPER TAPE PUNCH CONTROLLER

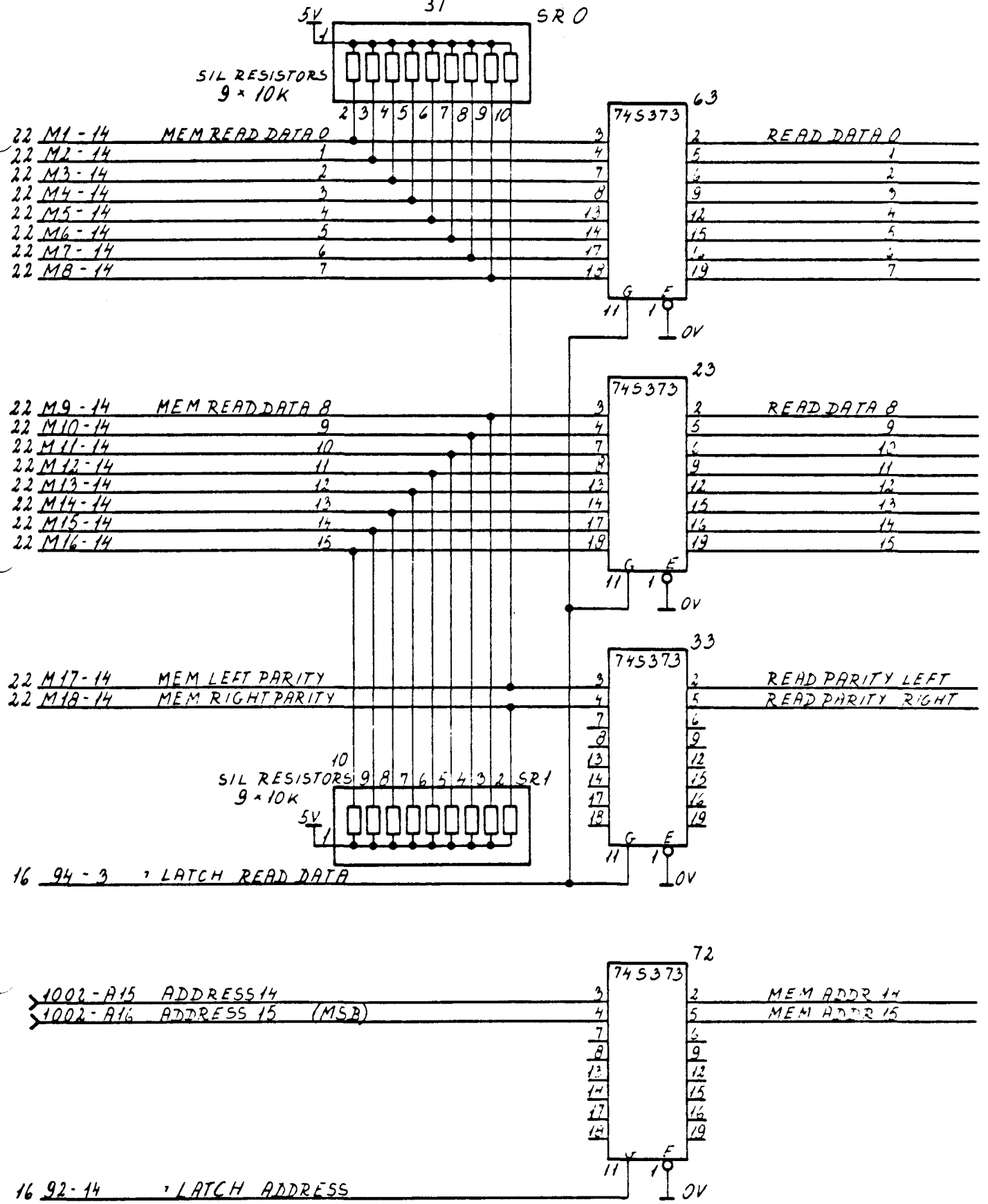
IOC 11

R 12903

SIGNAL	DESTI-NATION	DESCRIPTION
⇁BUS ‹0-15›	1002 MEM 14	CPU / Memory Data Bus
⇁LEFT PARITY	1002 MEM 14	- " -
⇁RIGHT PARITY	1002 MEM 14	- " -

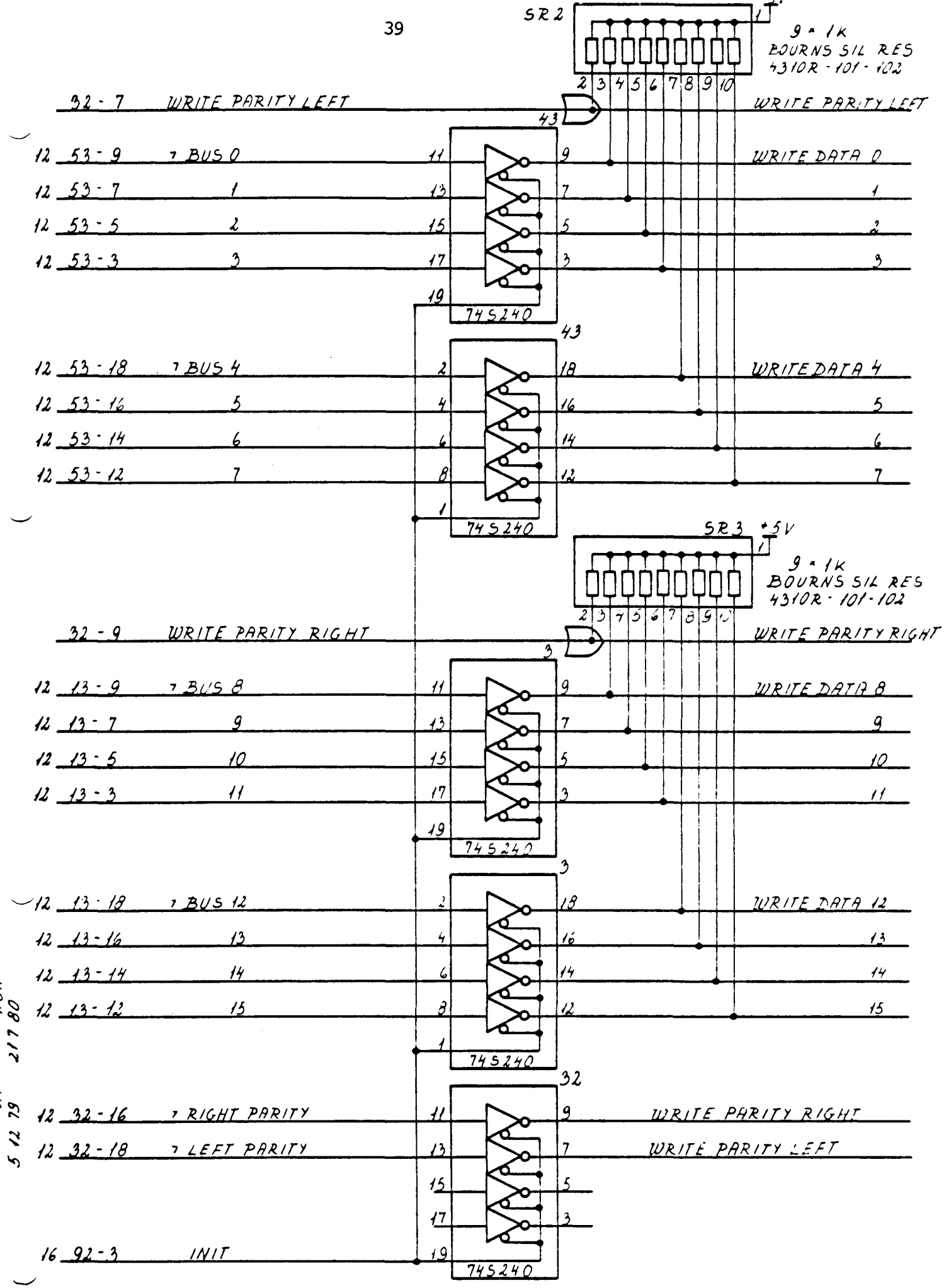

53
13 63-2 READ DATA 0
13 63-5 READ DATA 1
13 63-6 READ DATA 2
13 63-9 READ DATA 3
11
13
15
17
19
9 ↑BUS 0
7 ↑BUS 1
5 ↑BUS 2
3 ↑BUS 3
1002-B1
1002-B2
1002-B3
1002-B4
74S240
53
13 63-12 READ DATA 4
13 63-15 READ DATA 5
13 63-16 READ DATA 6
13 63-19 READ DATA 7
2
4
6
8
1
18 ↑BUS 4
16 ↑BUS 5
14 ↑BUS 6
12 ↑BUS 7
1002-B5
1002-B6
1002-B7
1002-B8
74S240
13
13 23-2 READ DATA 8
13 23-5 READ DATA 9
13 23-6 READ DATA 10
13 23-9 READ DATA 11
11
13
15
17
19
9 ↑BUS 8
7 ↑BUS 9
5 ↑BUS 10
3 ↑BUS 11
1002-B9
1002-B10
1002-B11
1002-B12
74S240
13
13 23-12 READ DATA 12
13 23-15 READ DATA 13
13 23-16 READ DATA 14
13 23-19 READ DATA 15
2
4
6
8
1
18 ↑BUS 12
16 ↑BUS 13
14 ↑BUS 14
12 ↑BUS 15
1002-B13
1002-B14
1002-B15
1002-B16
74S240
32
13 33-2 READ PARITY LEFT
13 33-5 READ PARITY RIGHT
2
4
6
8
1
18 ↑LEFT PARITY
16 ↑RIGHT PARITY
14
12
1002-B17
1002-B18
74S240
16 84-8 ↑SEND DATA
FGA 21 7 60
KF 5 12 79

SIGNAL	DESTI-NATION	DESCRIPTION
READ DATA ‹0-15›	MEM 12	Latched Memory Read Data
READ PARITY LEFT	MEM 12	- " -
READ PARITY RIGHT	MEM 12	- " -
MEM ADDR 14	MEM 15	Latched address bit 14 and 15, used
MEM ADDR 15	MEM 15	for module select.



KF 21 7 80 AGA
5 12 79

SIGNAL	DESTI-NATION	DESCRIPTION
WRITE DATA ‹0-15›	MEM 22	Memory Write data.
WRITE PARITY LEFT	MEM 22	Odd parity for bit ‹0-7›
WRITE PARITY RIGHT	MEM 22	Odd parity for bit ‹8-15›



AGA 21780 KF 5 12 79

MEM 720

MEMORY DATA BUS RECEIVERS

MEM 14

R 12906

SIGNAL	DESTI-NATION	DESCRIPTION
LOGIC 1A MEM	MEM 16 MEM 17	1 K ohm pull up for unused TTL inputs.
PULL UP <A-C>	MEM 23	Pull up for open collector gates
MEM SEL	MEM 16	Memory Select
SEL 0-16	MEM 20	Select signal for the 0-16 K memory array
SEL 16-32	MEM 20	- " - 16-32 K - " -
SEL 32-48	MEM 21	- " - 32-48 K - " -
SEL 48-64	MEM 21	- " - 48-64 K - " -
MEM ADDR <0-13>	MEM 19	Latched address (Tri-state Bus).

VALID SWITCH SETTINGS

MEMORY SIZE	ADDRESS SPACE	SW NO 1 2 3 4
MEM DISABLED	X	0 0 X X
32 k	0-32 k	1 0 1 0
	32-64K	0 1 1 0
64K		1 1 0 1

Red dot visible ~ "0"

1 2 3 4

Switches shown with:
MEM SIZE = 32 K
ADDRESS SPACE = 0-32K

9 x 1k SR 4

5V

LOGIC 1A MEM
PULL UP A
PULL UP B
PULL UP C

S 3 112 S2

113 74S157

13 72-5 MEM ADD 15
16 92-3 INIT

104 74S158

MEM SEL
SEL 0-16
SEL 16-32
SEL 32-48
SEL 48-64

13 72-2 MEM ADD 14
17 82A-11 REFRESH

91 74S373

1002-A1 A0 (LSB) → MEM ADDR 0
A2 A1 → 1
A3 A2 → 2
A4 A3 → 3
A5 A4 → 4
A6 A5 → 5
A7 A6 → 6

16 92-12 ↑LATCH ADDRESS
17 74-3 ↑REFRESH

74 74S00

81 74S373

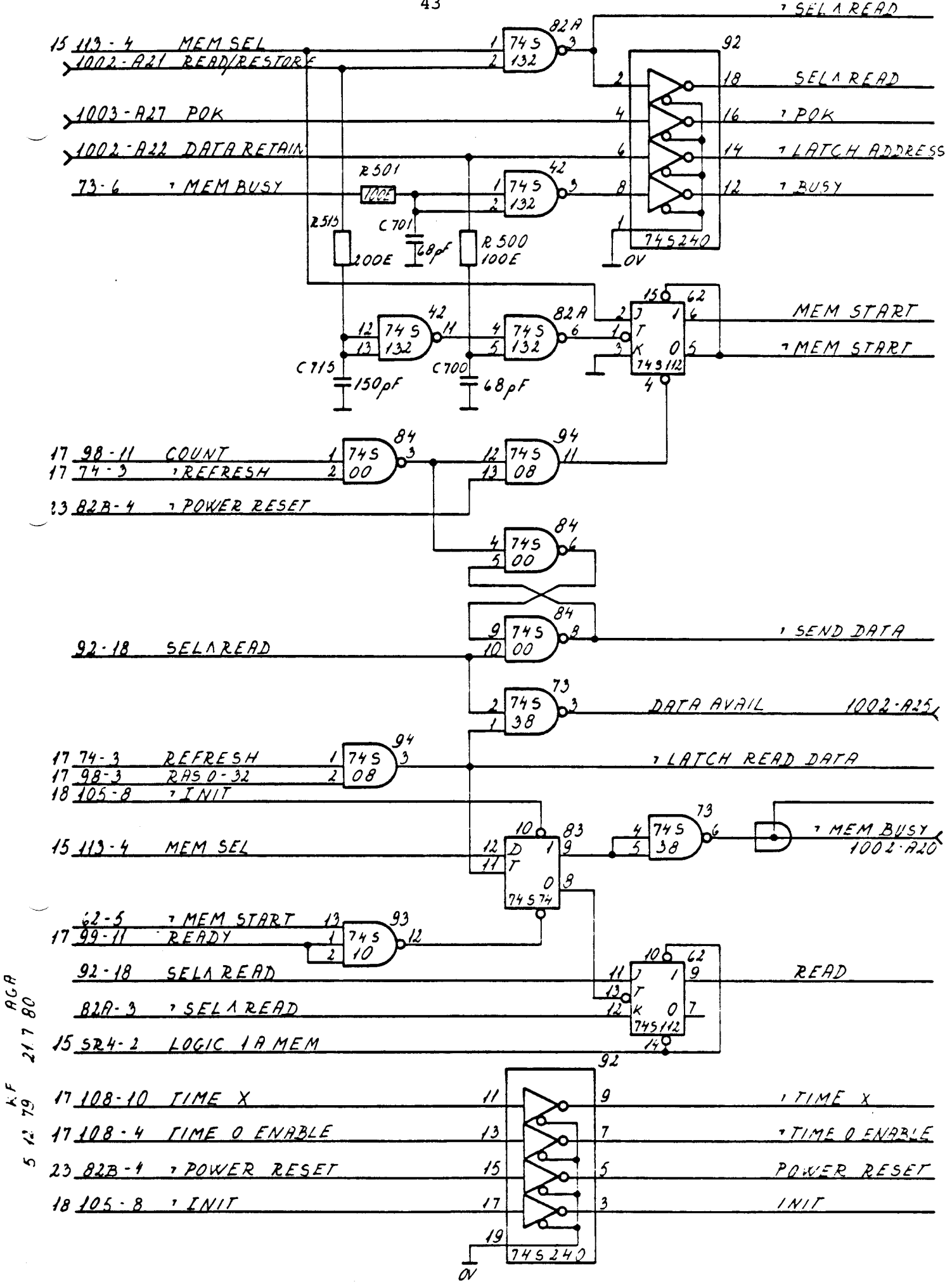
1002-A8 A7 → MEM ADDR 7
A9 A8 → 8
A10 A9 → 9
A11 A10 → 10
A12 A11 → 11
A13 A12 → 12
A14 A13 → 13

17 98-6 MUX 0-32
17 74-3 ↑REFRESH

74 74S00

AGA 21 7 80
KF 5 12 79

SIGNAL	DESTI-NATION	DESCRIPTION
~SEL∧READ	MEM 16	Selected Read Command
SEL∧READ	MEM 16	
~POK	MEM 23	Received Power OK from I/O-bus
~LATCH ADDRESS	MEM 13 MEM 15	Received Data Retain Signal
~BUSY	MEM 16 MEM 17	Received Memory Busy Signal from Memory Bus.
MEM START	MEM 17	A start condition has been detected
~MEM START	MEM 16	
~SEND DATA	MEM 12	Read data output enable
DATA AVAIL	1002	Valid read data on the bus
~LATCH READ DATA	MEM 13	
~MEM BUSY	1002 MEM 16	Memory bus busy
READ	MEM 18	Memory Cycle is a Read Cycle
~TIME X	MEM 17	40 ns after TIME 0
~TIME 0 ENABLE	MEM 17	280 ns after TIME 0
POWER RESET	MEM 18	Start initialization of memory contents
INIT	MEM 14 MEM 15 MEM 18	The memory is been initialized



AGA 21 7 80
K.F 5 12 79

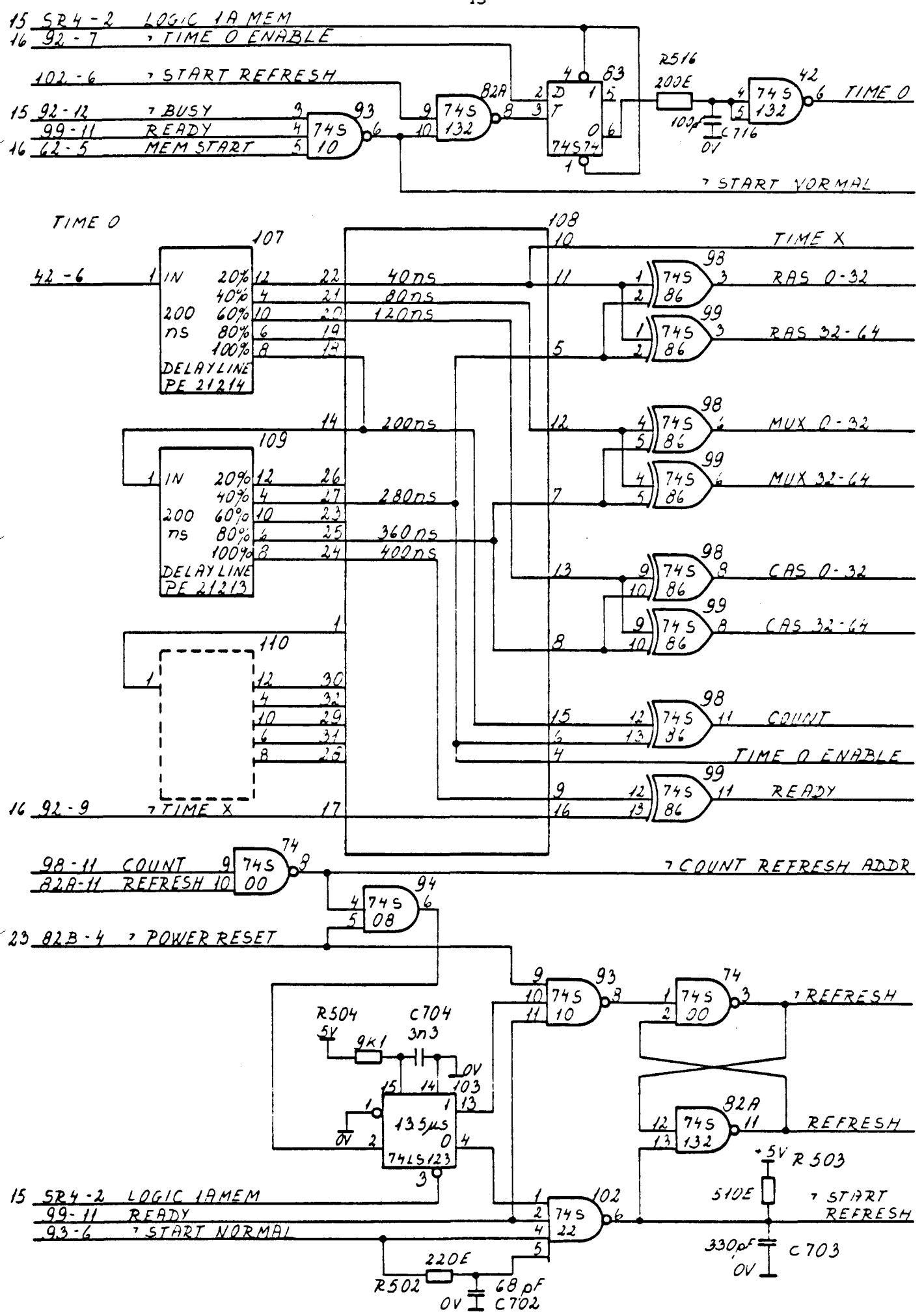
MEM 720

MEMORY CONTROL LOGIC 1

MEM 16

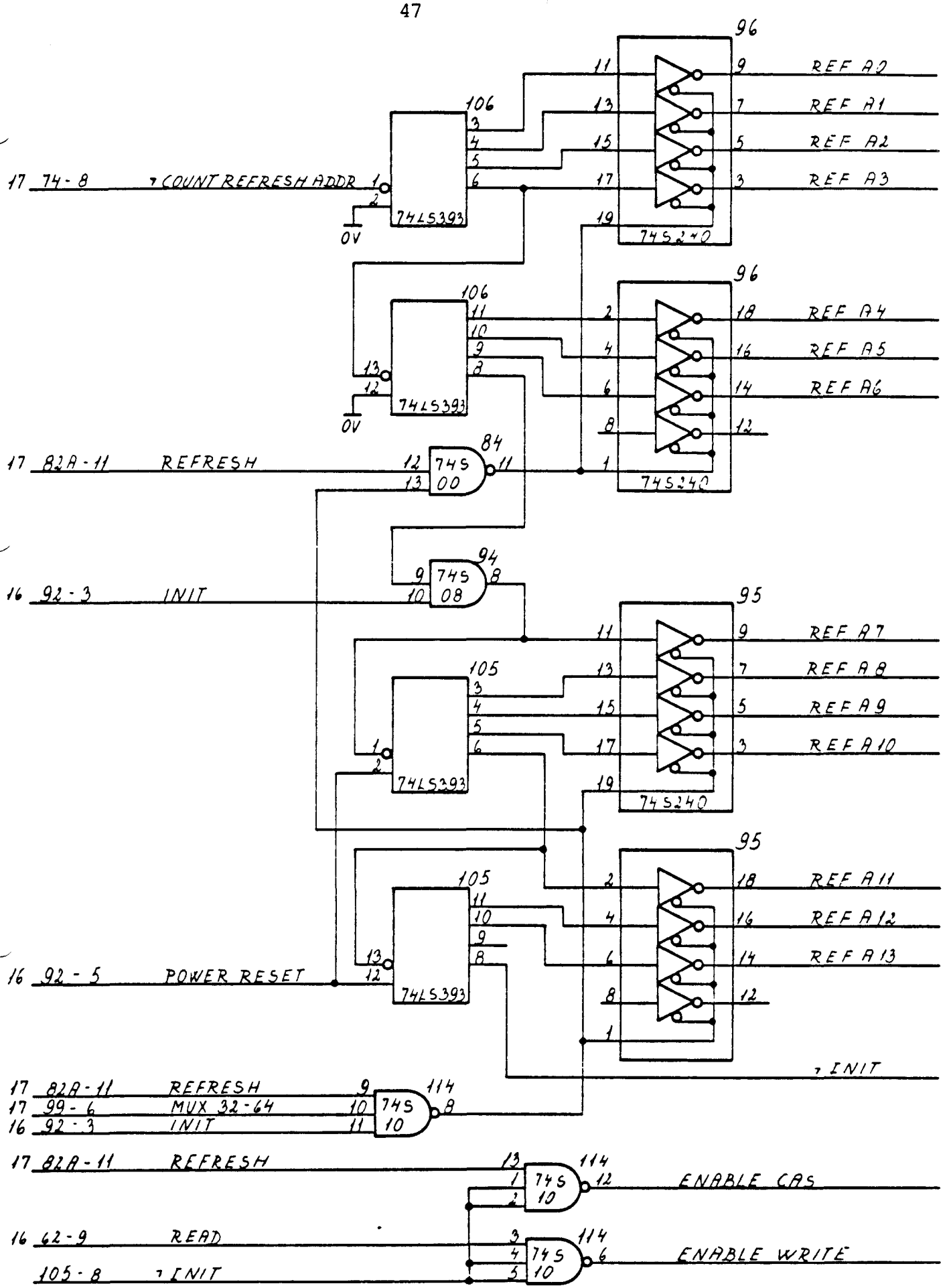
R 12908

SIGNAL	DESTI-NATION	DESCRIPTION
TIME 0	MEM 17	Intput to delay lines
⁊START NORMAL	MEM 17	CPU Read/Write cycle request
TIME X	MEM 16	40 ns after TIME 0
RAS 0-32	MEM 16 MEM 20	Row Address Strobe
RAS 32-64	MEM 21	
MUX 0-32	MEM 15 MEM 20	Select Column Address
MUX 32-64	MEM 18 MEM 21	
CAS 0-32	MEM 20	Column Address Strobe
CAS 32-64	MEM 21	
COUNT	MEM 16 MEM 17	Clear Start flag (MEM START or Refresh Timer). Increment Refresh Address.
TIME 0 ENABLE	MEM 16	280 ns after TIME 0
READY	MEM 16 MEM 17	The memory is idle
⁊COUNT REFRESH ADDR	MEM 18	
⁊REFRESH	MEM 15 MEM 16	The current cycle is a Refresh Cycle
REFRESH	MEM 15 MEM 17 MEM 18	
⁊START REFRESH	MEM 17	Refresh cycle request



AGA 21780 5.12.79 AF

SIGNAL	DESTI-NATION	DESCRIPTION
REF A ‹0-6›	MEM 19	Refresh address (only Row address)
REF A ‹7-13›	MEM 19	Column address for initialization
⁊INIT	MEM 16 MEM 18	Initialization command
ENABLE CAS	MEM 20 MEM 21	Column Address Strobe is disabled during refresh cycles
ENABLE WRITE	MEM 20 MEM 21	WE is only disabled during CPU Read cycles



AGA 21 7 80

KF 5 12 79

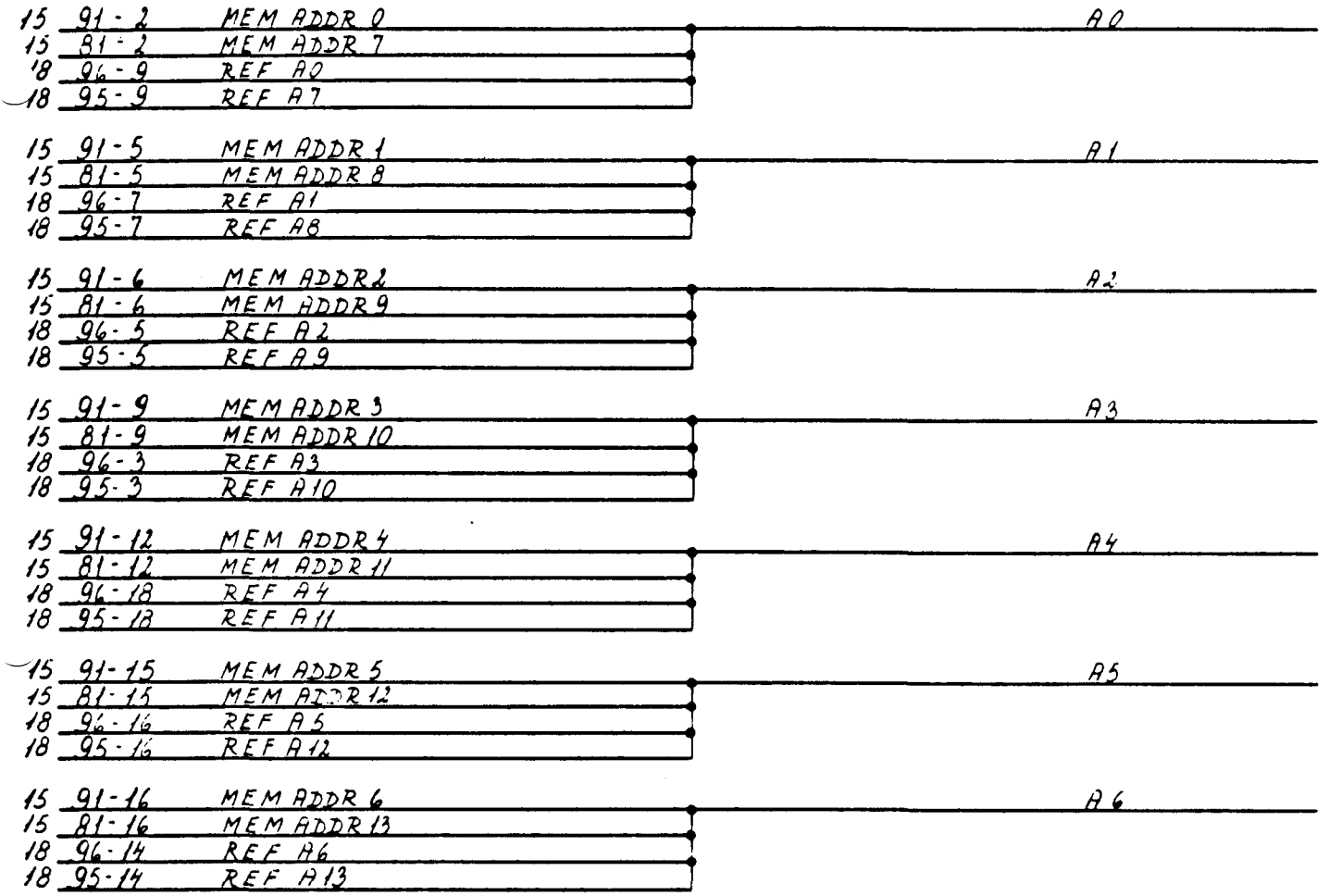
MEM 720

REFRESH ADDRESS COUNTER

MEM 18

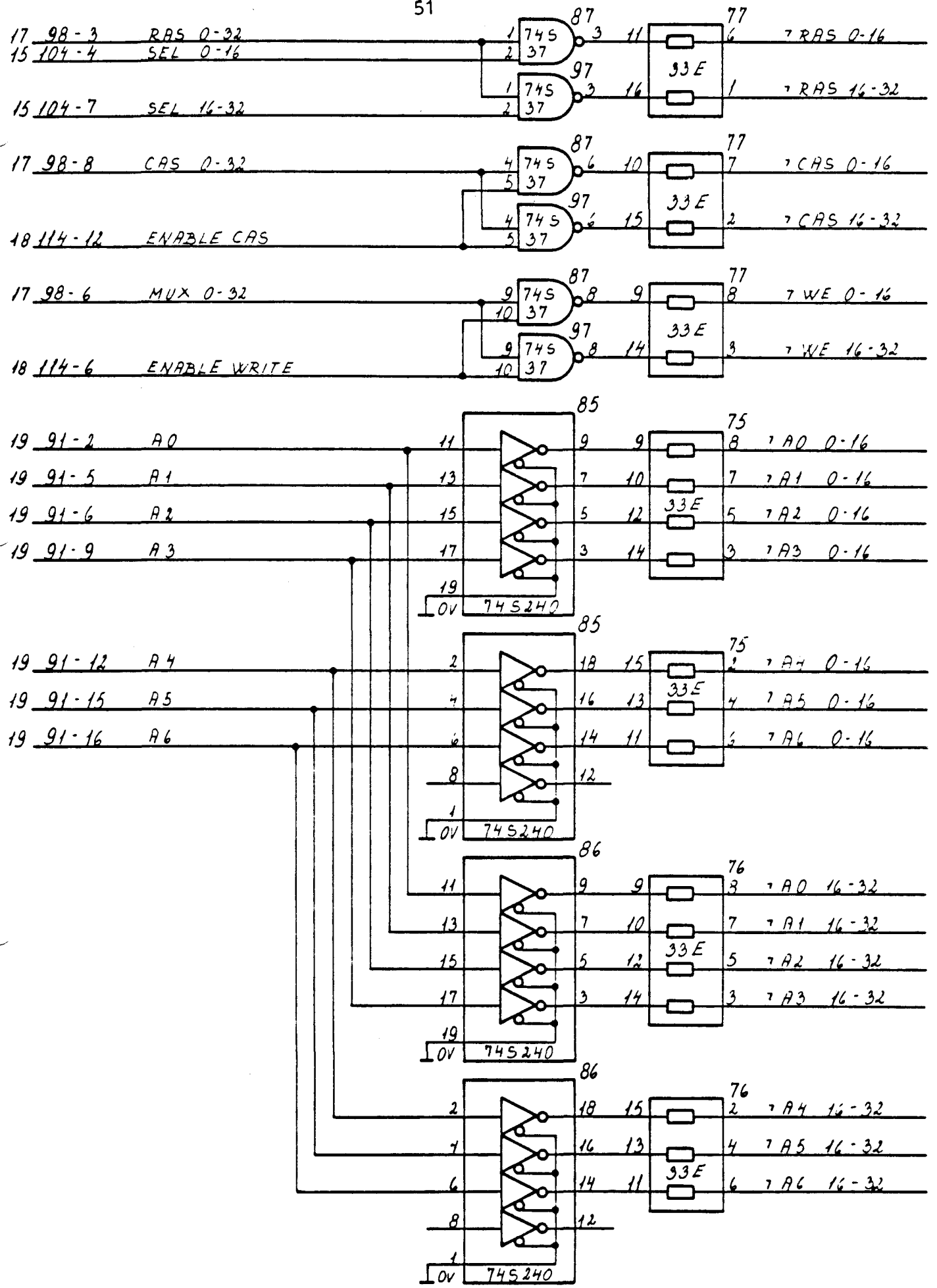
R 12.9 10

SIGNAL	DESTI-NATION	DESCRIPTION
A ‹0-6›	MEM 20 MEM 21	A tri-state bus used to multiplex row/column address from the CPU or the refresh (initialization) counter.



5 12 79 KF 21 7 80 AGA

SIGNAL	DESTI-NATION	DESCRIPTION
>RAS 0-16	MEM 22	Row Address Strobe
>RAS 16-32	MEM 22	
>CAS 0-16	MEM 22	Column address strobe
>CAS 16-32	MEM 22	
>WE 0-16	MEM 22	Write enable
>WE 16-32	MEM 22	
>A <0-6> 0-16	MEM 22	Address
>A <0-6> 16-32	MEM 22	



5.12 79 KF 217 80 AGA

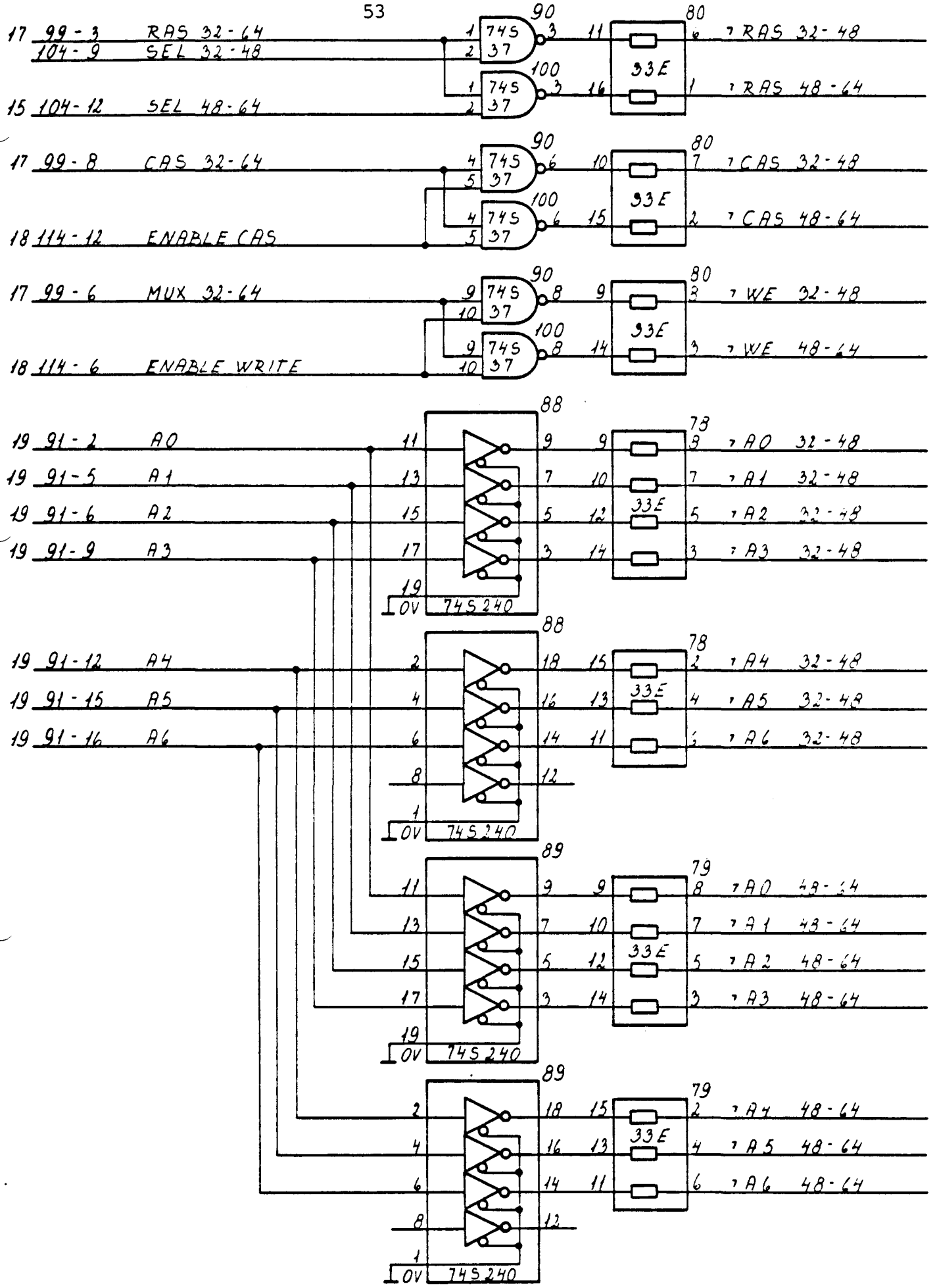
MEM 720

MEMORY ARRAY 0-16K AND 16-32K SIGNAL DRIVERS

MEM 20

R 12912

SIGNAL	DESTI-NATION	DESCRIPTION
~RAS 32-48	MEM 22	Row Address Strobe
~RAS 48-64	MEM 22	
~CAS 32-48	MEM 22	Column Address Strobe
~CAS 48-64	MEM 22	
~WE 32-48	MEM 22	Write Enable
~WE 48-64	MEM 22	
~A 0-6 32-48	MEM 22	Address
~A 0-6 48-64	MEM 22	



AGA 21 180 KF 5 12 79

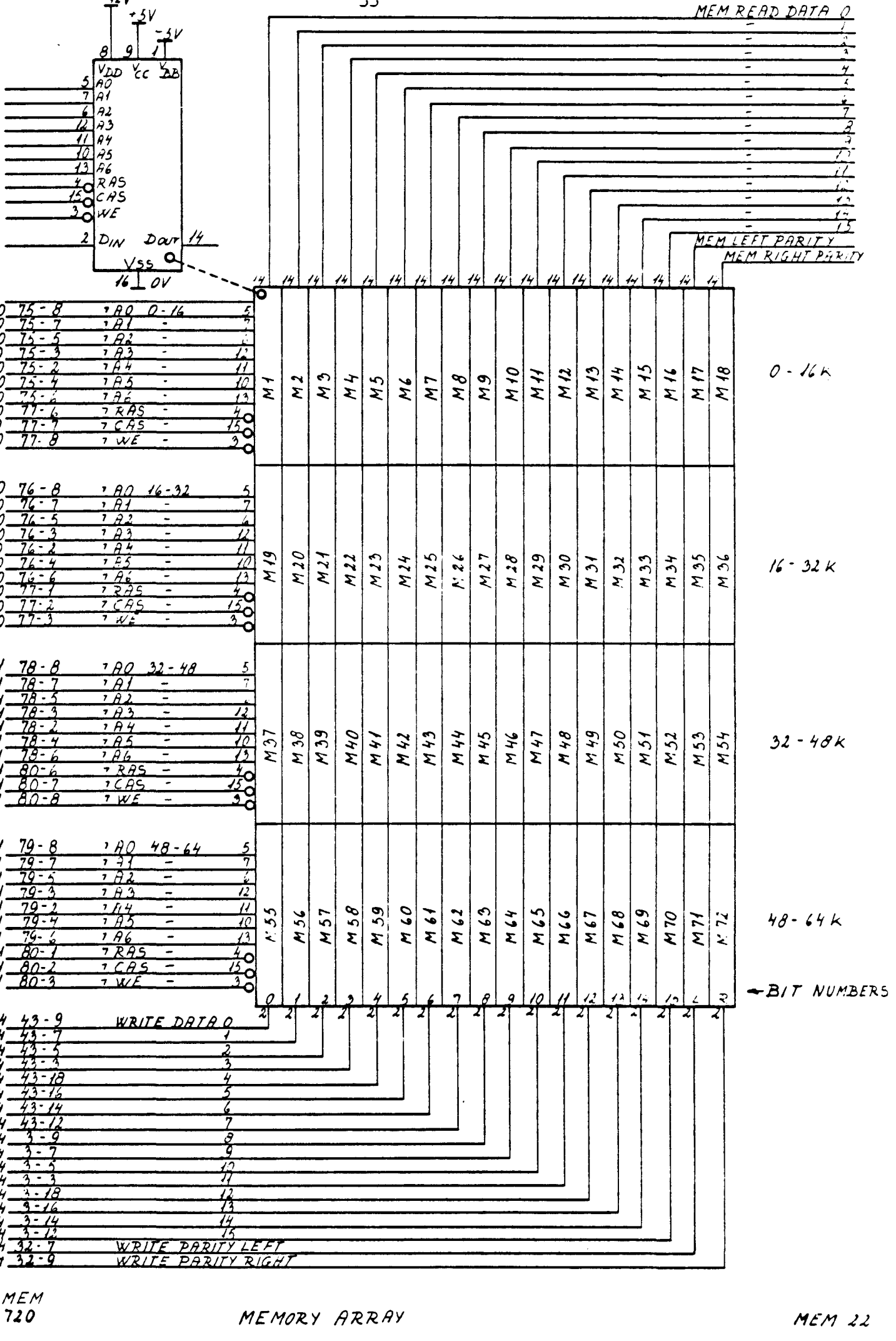
MEM 720

R 12 913

MEMORY ARRAY 32-48K AND 48-64K
SIGNAL DRIVERS

MEM 21

SIGNAL	DESTI-NATION	DESCRIPTION
MEM READ DATA 0-15	MEM 13	Data output from array
MEM LEFT PARITY	MEM 13	
MEM RIGHT PARITY	MEM 13	



KF 5.12.79 21 7 80 AGA

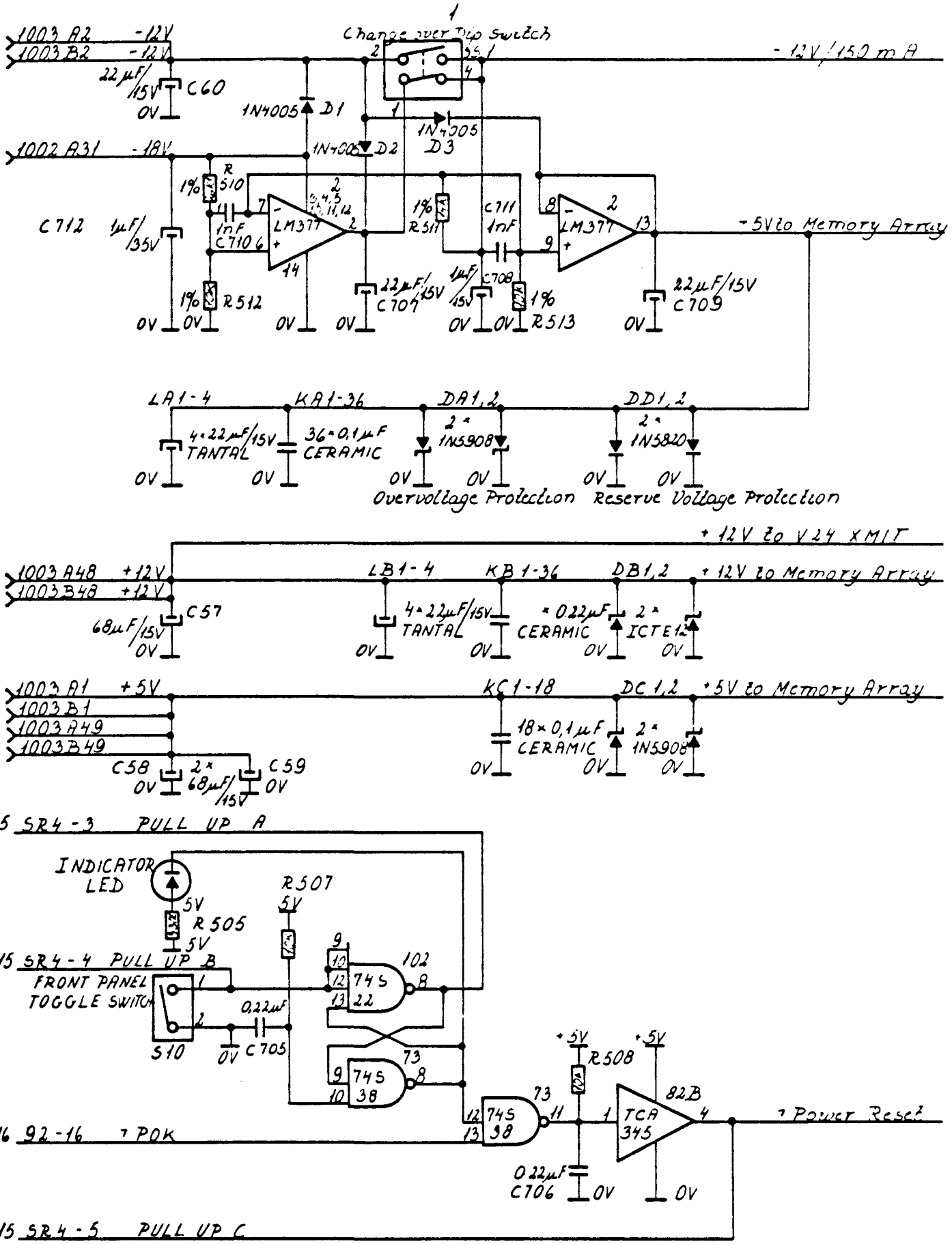
MEM 720

MEMORY ARRAY

MEM 22

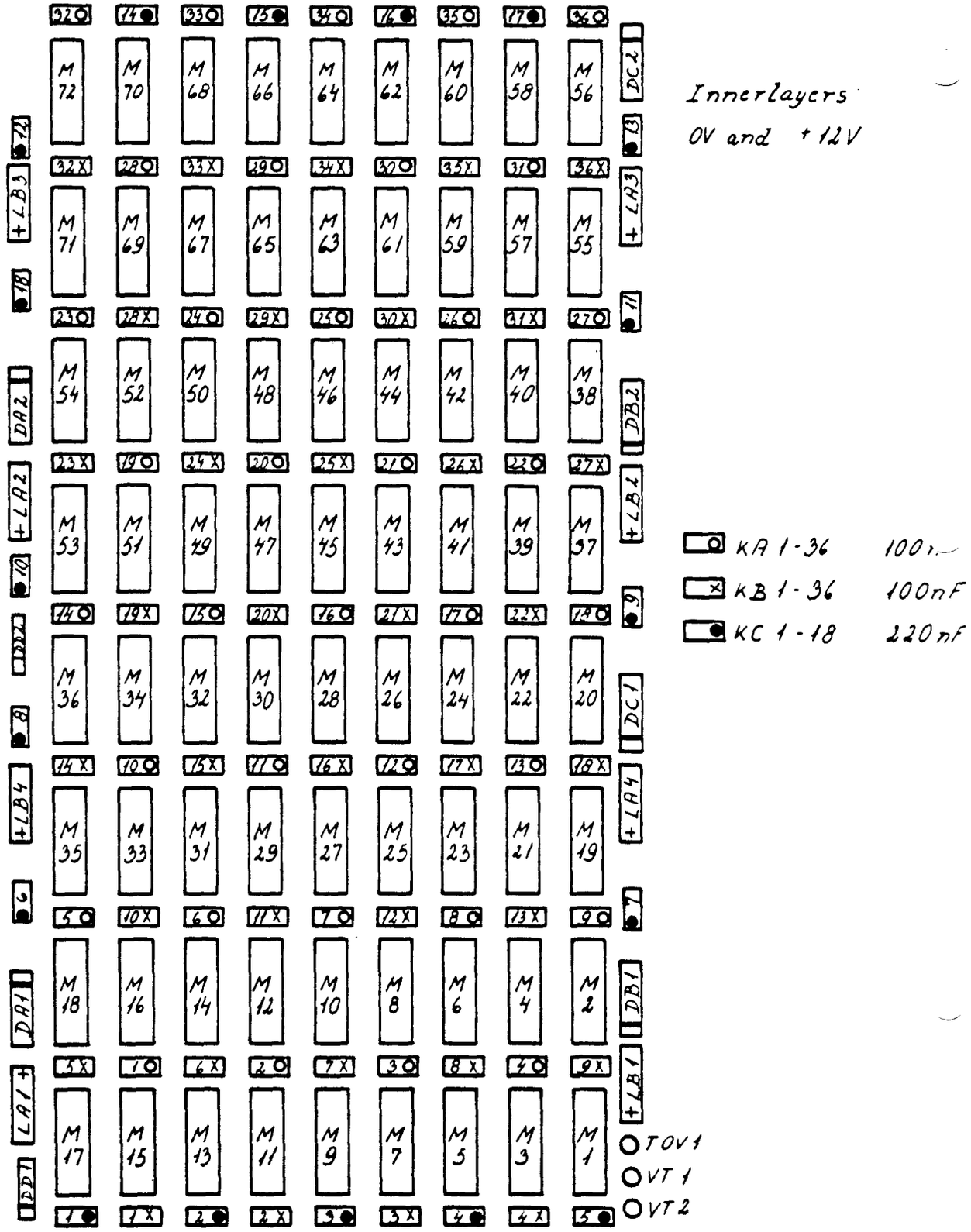
R 12914

SIGNAL	DESTI-NATION	DESCRIPTION
-12V/150 m A	IOC 6 IOC 7 IOC 8 IOC 9	-12 Volt for the teletype controllers
-5V	MEM 22	Negative memory supply voltage
+12V TO V24 XMIT	IOC 9	The Line output drivers of the teletype controllers are supplied +12V
+12V TO MEMORY ARRAY	MEM 22	The two inner layers of the PCB are converted to 0V and +12V in the memory array - area.
+5V TO MEMORY ARRAY	MEM 22	On the rert of the board the inner layers supplies 0V and +5V.
-POWER RESET	MEM 16 MEM 17	The memory must be initialized due to a power low condition.



AGA 21.7.80

KF 5.12.79



KF 5 12 79 AGA 21 7 80

MEM 720

MEMORY ARRAY LAYOUT

MEM 24

R 12916

6. PROM LISTINGS.

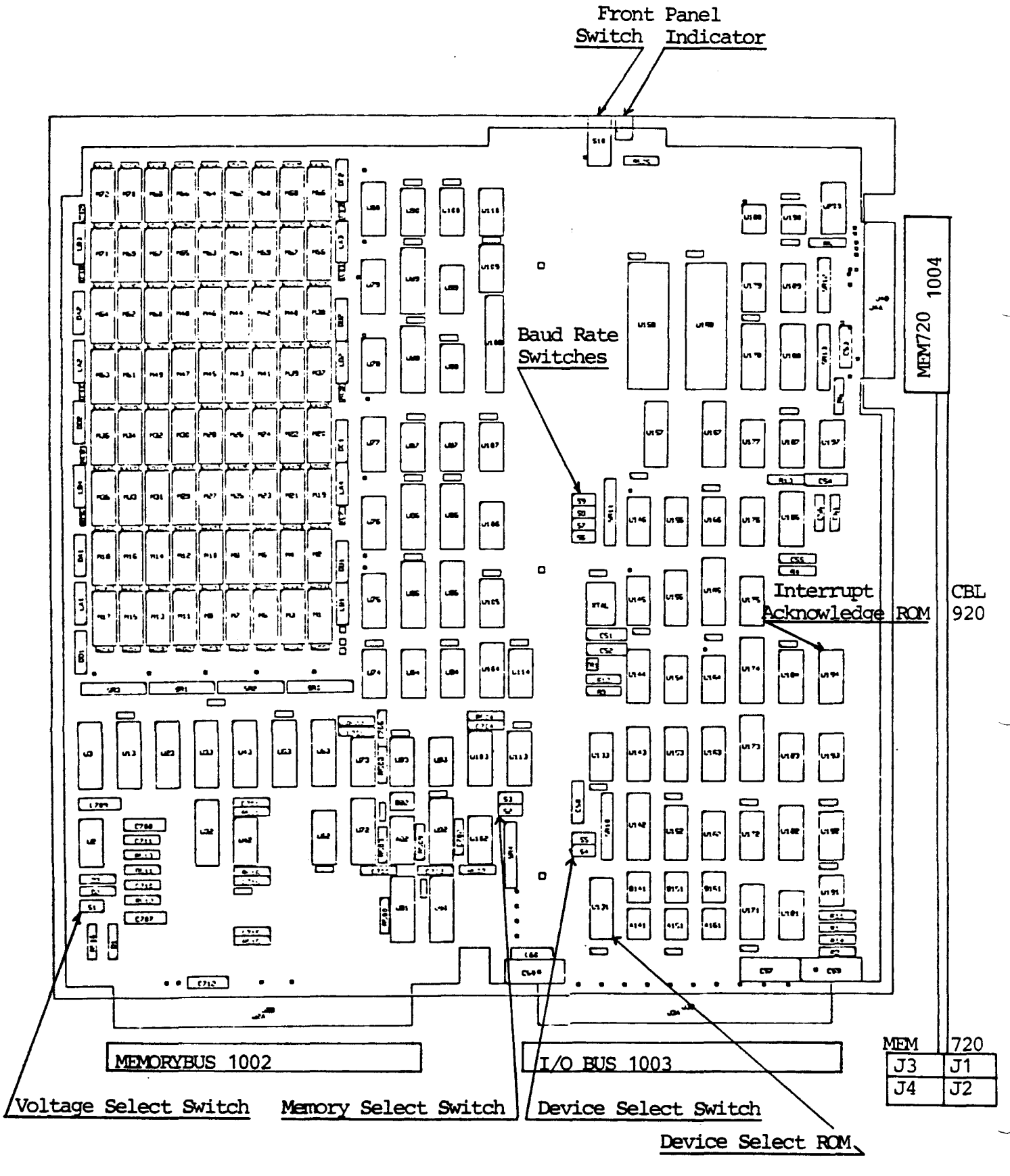

```
0001 RA316 DOMUS MACRO ASSEMBLER REV 01.06
                        .TITL RA316     ;ROA 316
02                      ;       DEVICE SELECT DECODE ROM FOR MEM720.
03                      ;
04                      ;       THE CONTENTS OF THE ADDRESSES NOT LISTED
05                      ;       EQUALS 07(OCTAL).
06                      ;
07                      ;       ROM-TYPE:       MMI6353
08                      ;
09
10                              .MACRO .FLOC    ;SET LOCATION COUNTER AND
11                      **      .DO ^1-.        ;FILL UP WITH 07(OCTAL)
12                      **      07
13                      **      .ENDC
14                      %
15
16
17                      .FLOC 0026
18 00026 000016                 16
19 00027 000002                 02
20                      .FLOC 0063
21 00063 000014                 14
22 00064 000013                 13
23 00065 000000                 00
24 00066 000015                 15
25 00067 000001                 01
26                      .FLOC 0126
27 00126 000016                 16
28 00127 000002                 02
29                      .FLOC 0163
30 00163 000014                 14
31 00164 000013                 13
32 00165 000007                 07
33 00166 000015                 15
34 00167 000001                 01
35                      .FLOC 0226
36 00226 000016                 16
37 00227 000002                 02
38                      .FLOC 0263
39 00263 000014                 14
40 00264 000007                 07
41 00265 000000                 00
42 00266 000015                 15
43 00267 000001                 01
44                      .FLOC 363
45 00363 000014                 14
46 00364 000013                 13
47 00365 000000                 00
48 00366 000015                 15
49 00367 000001                 01
50                      .FLOC 0442
51 00442 000016                 16
52 00443 000002                 02
53 00444 000015                 15
54 00445 000001                 01
55 00446 000013                 13
56                      .FLOC 454
57 00454 000000                 00
58                      .FLOC 0542
59 00542 000016                 16
60 00543 000002                 02
61 00544 000015                 15
62 00545 000001                 01
```

```
 0002 RA316
01                      .FLOC 0646
02 00646 000013                 13
03                      .FLOC 654
04 00654 000000                 00
05                      .FLOC 0754
06 00754 000000                 00
07                      .FLOC 1042
08 01042 000016                 16
09 01043 000002                 02
10 01044 000015                 15
11 01045 000001                 01
12                      .FLOC 1054
13 01054 000000                 00
14                      .FLOC 1064
15 01064 000013                 13
16                      .FLOC 1142
17 01142 000016                 16
18 01143 000002                 02
19 01144 000015                 15
20 01145 000001                 01
21                      .FLOC 1164
22 01164 000013                 13
23                      .FLOC 1242
24 01242 000016                 16
25 01243 000002                 02
26                      .FLOC 1254
27 01254 000000                 00
28                      .FLOC 1264
29 01264 000013                 13
30                      .FLOC 1426
31 01426 000015                 15
32 01427 000001                 01
33                      .FLOC 1444
34 01444 000016                 16
35 01445 000002                 02
36                      .FLOC 1464
37 01464 000013                 13
38 01465 000000                 00
39                      .FLOC 1526
40 01526 000015                 15
41 01527 000001                 01
42                      .FLOC 1544
43 01544 000016                 16
44 01545 000002                 02
45                      .FLOC 1564
46 01564 000013                 13
47                      .FLOC 1626
48 01626 000015                 15
49 01627 000001                 01
50                      .FLOC 1644
51 01644 000016                 16
52 01645 000002                 02
53                      .FLOC 1665
54 01665 000000                 00
55                      .FLOC 1726
56 01726 000015                 15
57 01727 000001                 01
58                      .FLOC 1764
59 01764 000013                 13
60 01765 000000                 00
61                      .FLOC 2000
62                      .END
```

```
 0001 RA317 DOMUS MACRO ASSEMBLER REV 01.06
                    .TITL RA317     ;ROA 317
02                  ;
03                  ;       INTERRUPT ACKNOWLEDGE ROM FOR MEM720
04                  ;
05                  ;       ROM-TYPE:       74S288
06          000000  .LOC 0
07  00000  000120  120
08  00001  000310  310
09  00002  000310  310
10  00003  000120  120
11  00004  000020  020
12  00005  000130  130
13  00006  000130  130
14  00007  000024  024
15  00010  000024  024
16  00011  000070  070
17  00012  000070  070
18  00013  000130  130
19  00014  000320  320
20  00015  000230  230
21  00016  000320  320
22  00017  000320  320
23
24  00020  000060  060
25  00021  000000  000
26  00022  000000  000
27  00023  000000  000
28  00024  000220  220
29  00025  000330  330
30  00026  000330  330
31  00027  000224  224
32  00030  000224  224
33  00031  000270  270
34  00032  000070  070
35  00033  000330  330
36  00034  000000  000
37  00035  000000  000
38  00036  000000  000
39  00037  000000  000
40
41                  .END

0000 SOURCE LINES IN ERROR
```

7. ASSEMBLY DRAWING. 7.



8. INTERNAL CABLES AND PLUG LISTS. 8.

8.1 Back Panel I/O-Bus Connector 1003. 8.1

BACK PANEL CONNECTOR 1003		
	A	B
1	+5V	+5V
2	-12V	-12V
3		
4		
5	-, DS0	POB
6	-, DS1	0V
7	-, DS2	0V
8	-, DS3	0V
9	-, DS4	0V FLO
10	-, DS5	0V
11	-, DCH A	0V
12	DCHI	0V
13	DCHO	INTA
14	-,DATA0	0V
15	-,DATA1	0V
16	-,DATA2	0V
17	-,DATA3	-,DATA4
18	-,DATA5	0V
19	-,DATA6	0V
20	-,DATA7	0V
21	-,DATA8	-,DATA9
22	-,DATA10	0V
23	-,DATA11	0V
24	-,DATA12	0V
25	-,DATA13	-,DATA14
26	-,DATA15	0V
27	POK	0V
28	-,PINT	0V
29	-,SEL B	-,SEL D
30	-,INTR	0V
31	-,DCHR	0V
32	DAT O A	0V
33	DAT O B	IOPLS
34	DAT O C	0V
35	DAT I A	0V
36	DAT I B	0V
37	DAT I C	CLR
38	STRT	0V
39	-,RQEN B	0V
40	-,MSK O	0V
41	-,INTP OUT	-,INTP IN
42	IORST	0V
43	-,DCHM 0	0V
44	-,DCHM 1	0V
45	-,DCHP OUT	-,DCHP IN
46		
47		
48	+12V	+12V
49	+5V	+5V

NOVA I/O BUS SIGNAL ALLOCATION

Back panel connector 1003

8.2 Back Panel Memory Bus Connector 1002. 8.2

BACK PANEL CONNECTOR 1002		
	A	B
1	A0	-,BUS0
2	A1	-,BUS1
3	A2	-,BUS2
4	A3	-,BUS3
5	A4	-,BUS4
6	A5	-,BUS5
7	A6	-,BUS6
8	A7	-,BUS7
9	A8	-,BUS8
10	A9	-,BUS9
11	A10	-,BUS10
12	A11	-,BUS11
13	A12	-,BUS12
14	A13	-,BUS13
15	A14	-,BUS14
16	A15	-,BUS15
17		-,RIGHT PARITY
18		-,LEFT PARITY
19		0V
20	-,MEMORY BUSY	0V
21	READ/RESTORE	0V
22	DATA RETAIN	0V
23		0V
24		0V
25	DATA AVAIL	0V
26		
27		0V
28		
29		
30		
31	-18V	
32		
33		
34		
35		
36		
37		
38	0V	0V
39	0V	0V
40	0V	0V
41	0V	0V
42	0V	0V
43		
44		
45		
46		
47		
48		
49		

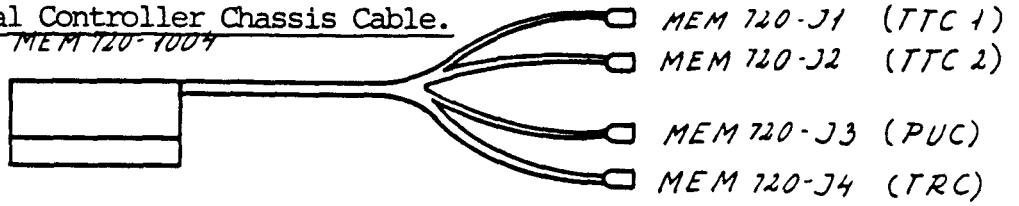
Signal list for connector 1002

8.3 Edge Connector 1004. 8.3

EDGE CONNECTOR 1004		
	A	B
1		5V
2	XMIT DATA 1	0V
3	CTS 1	SEL STOP 1
4	REC DATA 1	
5		5V
6	XMIT DATA 2	0V
7	CTS 2	SEL STOP 2
8	REC DATA 2	
9		
10	TP OUT	
11	PUC H	0V
12	PUCN8	PUCN7
13	PUCN6	PUCN5
14	PUCN4	PUCN3
15	PUCN2	PUCN1
16	PUSG	0V
17	FWSTP	5V
18	-READY	0V
19	C8	C7
20	C6	C5
21	C4	C3
22	C2	C1
23	STOP	0V
24	GO	
25	SPKT	5V

Signal list for connector 1004

8.4 Internal Controller Chassis Cable.



MEM 720-1004: 2 × 25 Socket Edge Connector

MEM 720-J1&J2: Cannon DEC 9S

MEM 720-J3&J4: Cannon 2DE 19S

I		J1			
1A					
1B	5V	1			
2A	XMIT DATA	6			Teletype 1
2B	0V	9			
3A	CTS	5			
3B	SEL STOP	8			
4A	REC DATA	3			
4B			J2		
5A					
5B	5V		1		
6A	XMIT DATA		6		Teletype 2
6B	0V		9		
7A	CTS		5		
7B	SEL STOP		8		
8A	REC DATA		3		
8B				J3	
9A					
9B					
10A	TP OUT			15	
10B					
11A	PUL H			9	
11B	0V			12	
12A	PUC N8			7	Paper Tape Punch
12B	PUC N7			6	
13A	PUC N6			5	
13B	PUC N5			4	
14A	PUC N4			3	
14B	PUC N3			2	
15A	PUC N2			1	
15B	PUC N1			8	
16A	PUS G			18	
16B	0V			13	J4
17A	FWSTP				13
17B	5V				16
18A	~ READY				11
18B	0V				18
19A	C8				8
19B	C7				7
20A	C6				6
20B	C5				5
21A	C4				4 Paper Tape Reader
21B	C3				3
22A	C2				2
22B	C1				1
23A	STOP				12
23B	0V				14
24A	GO				10
24B					
25A	SPKT				9
25B	5V				17

21 7 80 KF 21 7 80 AGA

9. COMPONENT LIST. 9.

The following electrical components are used in the MEM720.

Qty.	Description	RC Part No.
1	IC SN7404N	29711
1	IC SN7410N	35902
1	IC SN7425N	43710
1	IC SN7492AN	28312
1	IC SN7438N	40804
2	IC SN74S00N	43712
1	IC SN74S08N	50018
2	IC SN74S10N	56500
1	IC SN74S22N	03706
4	IC SN74S37N	56501
1	IC SN74S38N	56502
1	IC SN74S74N	43715
2	IC SN74S86N	54409
1	IC SN74S112N	56503
2	IC SN74S132N	56504
1	IC SN74S157N	57108
1	IC SN74S158N	58202
13	IC SN74S240N	60106
8	IC SN74S373N	58212
4	IC SN74LS00N	52611
1	IC SN74LS08N	52606
1	IC SN74LS14N	58111
4	IC SN74LS74N	52608
2	IC SN74LS123N	61915
1	IC SN74LS132N	58112
1	IC SN74LS148N	(001-28-092)
2	IC SN74LS151N	61817
1	IC SN74LS155N	(0015-28-084)
1	IC SN74LS175N	61901
1	IC SN74LS240N	61904
1	IC SN74LS259N	(0011-28-073)

Qty.	Description	RC Part No.
2	IC SN74LS273N	63618
1	IC SN74LS374N	61910
2	IC SN74LS390N	(0013-28-082)
2	IC SN74LS393N	(0012-28-088)
1	IC SN75150P	43817
1	IC SN75154N	43819
8	IC SN75452BP	55909
1	IC SN75453P	49810
1	IC SM25LS2535	63709
1	IC AM25LS2538	(0012-36-019)
3	IC MM5307AA	(0010-05-042)
2	IC TMS6011NC	58900
1	IC LM377N	(0014-05-060)
1	IC TCA345A	63815
72	IC uPD416-2	(0015-43-001)
2	IC PE21213	(0016-38-004)
3	DIODE 1N4005	21710
2	SCHOTKY DIODE 1N5820	(0030-02-064)
4	ZENER DIODE 1N5908	(0045-01-112)
2	ZENER DIODE ICTE12	(003-02-061)
1	TRANSISTOR 2N2907A	34114
1	CRYSTAL 18.432 MHz	(0272-01-029)
6	DIP RESISTOR 4116R-001-330	(0110-44-017)
5	SIL RESISTOR 4310R-101-102	64502
2	SIL RESISTOR 4310R-101-332	(0113-44-020)
1	SIL RESISTOR 4310R-101-103	(0111-44-004)
1	SIL RESISTOR 4308R-001-332	63606
1	DIL FILTER 906C102XSVG	60014
4	CONDENSOR 5% 63V 68pF	
1	" " " 100pF	
1	" " " 150pF	
1	" " " 330pF	
1	" " " 3n3F	
1	" 10% 250V 10nF	
1	" " " 15nF	

Qty.	Description	RC Part No.
47	CONDENSOR, CERAMIC 12V 47nF	43911
103	" " 25V 220nF	(0081-55-002)
3	" TANTAL 35V 1nF	(0103-01-010)
1	" " 20V 15nF	11116
8	" " 15V 22nF	11118
3	" " 15V 68nF	11119
1	RESISTOR 5% 1/8W 47E	15016
3	" " " 100E	15104
1	" " " 150E	15108
4	" " " 220E	15112
1	" " " 510E	15201
1	" " " 680E	15204
3	" " " 1K	10600
1	" " " 9K1	10703
2	" " " 10K	10704
1	" " " 30K	10715
1	" " " 110K	
3	" 2% 1/4W 330E	44018
2	" " " 390E	44019
2	" 1% 1/8W 10K	(0110-19-188)
1	" " " 14K	(0111-19-189)
1	" " " 26K1	(0116-19-187)

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