Title:

GENERAL INFORMATION
RC3803S
REVISION 1

Keywords:

RC3803S, GENERAL INFORMATION, Revision 1.

Abstract:

This paper contains general information of the central processor
unit, RC3803S.

(22 printed pages)

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1. GENERAL DESCRIPTION

The RC3803 Central Unit consists of a CPU720/CPU721 Central
Processing Unit and a MEM720 Semiconductor Memory and I/O con-
troller, housed in a CHS718 chassis. The CHS718 includes DC
power and free slots for 3 additional controller boards.

2.   SPECIFICATIONS   2.

2.1   Performance Specifications   2.1

Word Length:	16 bits.
Hardware Acculators:	4.
Index Registers:	2 hardware.
Address Modes:	Direct addressing of 1024 words, absolute, relative, and indexed modes; index addressing of up to 64K words;
Memory Cycle Time:	500 us.
Memory Access Time:	350 us.
Memory Capacity:	128 K bytes.
Memory type:	Dynamic Semiconductor Memory.
Max. DMA Transfer Rate:	1.25M words per second.
Input/Output System:	16-bit word length, 16 priority interrupt levels, 62 devices addressable.
I/O BUS Levels:	Ground and + 3 volts.
Standard Features:	Power Monitor

Standard Features (continued):

Real Time Clock
2 Teletype Controllers
Paper Tape Reader Controller
Paper Tape Punch Controller
3 Free slots for additional Controllers
Parity check on memory
Automatic Program Load from:
9-track magnetic tape,
8-channel paper tape,

80-column punched cards,
Flexible Disc Drive, or
Disc Drive

Optional Features: F09 additional controller chassis
containing separate power supply and five
slots for controller boards and an I/O
bus cable connecting it to the processing
unit.
Diagnostic panel TCP701.

2.2   Electrical Specifications

DC Power Consumption:
   CPU720/CPU721:   + 5V $\pm$ 5% 13A
   MEM720:   + 5V $\pm$ 5% 4A
                    +12V $\pm$ 5% 0.5A
                    -12V $\pm$ 5% 0.2A

DC Power for additional
controllers in CHS718:   -12V   3.5A
                       +12V   3A
                       + 5V   3A
                     2x100W of optional DC power

AC Power Consumption: 220V, 5 cps., 4A max.

Heat Dissipation: 700W max., 435 Kcal/h, 3000 BTU/h.

2.3   Environmental Specifications

Ambient Temperature: 10-40°C (50-104°F).

Relative Humidity: 20-80% (no condensation).

2.4   Physical Specifications   2.4

Dimensions:

Height:	31.1 cm (12 1/4 inches)
Width:	For cabinet mounting
Depth:	For cabinet mounting

Weight: 35 kg (77 lbs.)

Mounting:

Low Cabinet	(F90)
Desk Top Cabinet	(F91)
Midi Cabinet	(F92)
High Cabinet	(F93)

3.   IDENTIFICATION OF ITEMS   3.

Item	Reference No.	Description
1	CPU720/CPU721	Central Processor
2	CHS718	CPU Chassis
3	MEM720	128K bytes memory and I/O controllers
4	PDP711	Power Panel
5	CBL491	Internal Chassis Cable
6	CBL920	Internal Chassis Cable
7	CBL061	Memory Bus
8	CBL065	Power Cable
9	CBL879	Power Cable
10	SSB301	Logo
11	AFH057	Accessories for Chassis
12	ROM789	Autoload A
13	ROM790	Autoload B
14	ROM791	Autoload C
15	DDM139	RC3803S Documentation
16	DAT511	Seperate Documentation Items for RC3803S

4.   INSTALLATION   4.

This section describes where the different circuit boards
physically are located and how the RC3803S is connected to the
operators Control Panel, additional controller chassis,
peripheral units and main supply. The installation of the
autoload ROM's is described as well.

4.1   Installation of CPU720/CPU721 and MEM720 in CHS718 Chassis.   4.1

The CPU720/CPU721 and MEM720 must be mounted in the two topmost
positions in the chassis. In the following the installation of
the internal cables CBL491 and CBL920 as well as the memory
motherboard CBL061 is described.

a. Remove the RC2236 PCB from the two upper positions.

b. Remove the bottom of the CHS718 by loosening the two screws on
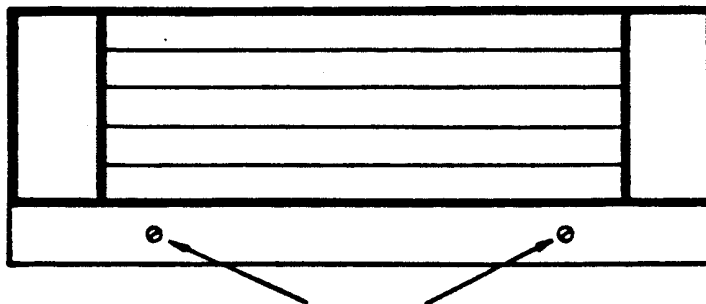the front and pull it free of the slides.

Figure 1: Front view of CHS718.

c. Mount the CBL491 internal controller cable in the following
order:

1. Mount the bracket with the 19-pin connector at the back of
the chassis (A) and connect the chassis terminal.

2. Lead the free end of the CBL491 through the hole (B) in the
chassis.

d. Mount the CBL920 in a similar manner.

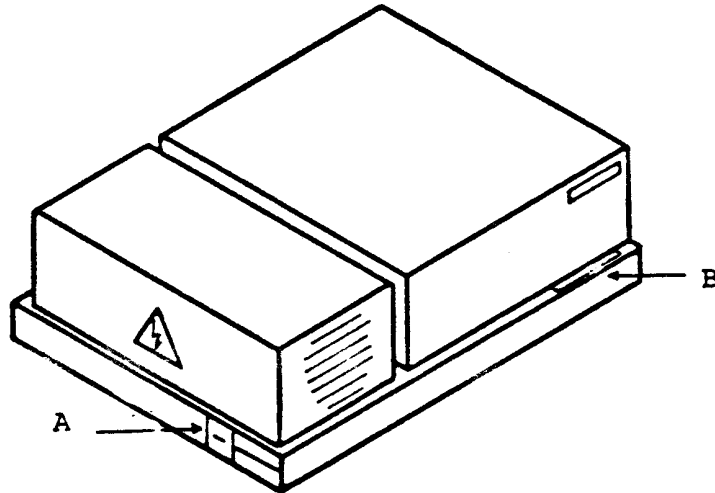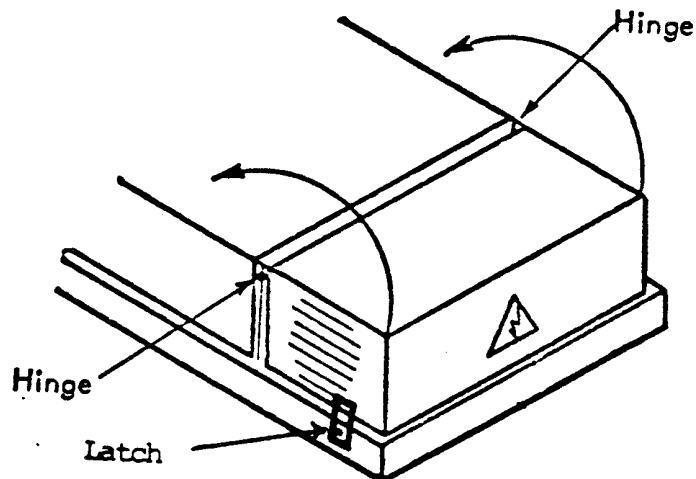e. Slide in the bottom of the chassis and tighten screws.

Figure 2: Rear and side view of CHS718.

f. Loosen the latches on both sides of the power supply, and turn the power supply over the hinges to lay upon the controller board case.

g. Mount the CBL061 two slot motherboard in the topmost position 1002.

h. Mount the power supply.

i. Install the autolod ROM's on the CPU (section 4.5) and set the DIP switches on the MEM720 (refer to RCSL No. 44-RT1954 'Technical Manual for MEM720', section 2): Then slide in the two boards and mount the edge connectors of CBL491 and CBL920 on the 1004 connector on the CPU720/CPU721 and the MEM720 respectively.

4.2 Internal Physical Organisation

Fig. 4 illustrates the mechanical configuration of the RC3803 cassette.

The CPU720/CPU721 is placed in the upper position, and MEM720 is placed just below. The last three slots can be used for various controller boards.
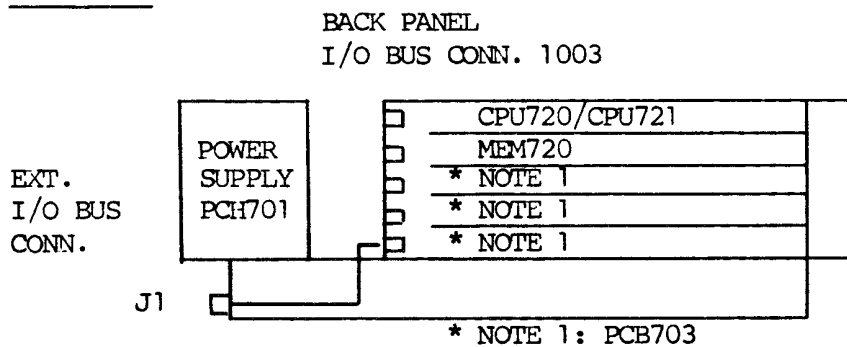
In the power supply two free slots may be used for additional power modules of 100W each.
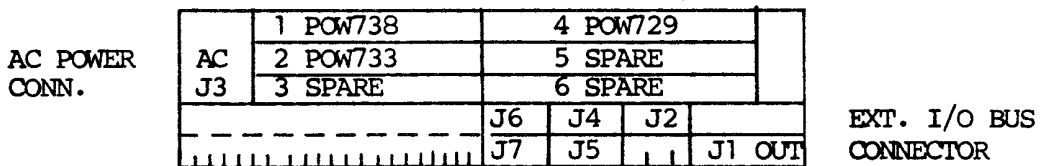
4.3 Jack/Plugs

Seven connectors are located at the back of the CPU cassette. (Refer to fig. 3).

SIDE VIEW

BACK PANEL
I/O BUS CONN. 1003

	POWER SUPPLY PCH701		CPU720/CPU721
EXT. I/O BUS CONN.			MEM720
			* NOTE 1
			* NOTE 1
			* NOTE 1

J1

* NOTE 1: PCB703

REAR VIEW

		1 POW738	4 POW729		
AC POWER CONN.	AC J3	2 POW733	5 SPARE		
		3 SPARE	6 SPARE		

	J6	J4	J2		
	J7	J5		J1 OUT	EXT. I/O BUS CONNECTOR

J2: Connection to external autoload panel.
J4: MEM720-J1 (TTC1)
J5: MEM720-J2 (TTC2)
J6: MEM720-J4 (TRC)
J7: MEM720-J3 (PUC)

Figure 3: MECHANICAL OUTLINE.

J1: External I/O-Bus connector, 100-pins Cannon connector

J2: Plug for Operators Control Panel, 2x2DE 19-pins Cannon Connector.

J3: 220V AC power Connector.

J4: Connector for first teletype (Consol), 9-pins Cannon Connector.

J5: Connector for second teletype.

J6: Connector for Paper tape Reader, 2x2De 19-pins Cannon Connector.

J7: Connector for Paper Tape Punch, 2x2DE 19-pins Cannon Connector.

For further information on the individual jacks/plugs, refer to the Technical manuals for the CPU720, CPU721 and MEM720.

4.4   Interconnection of Units   4.4

In fig. 4, a schematic diagram illustrates the interconnection between the different units.

Note that not all units need to be present, and that some units and cables may be replaced by similar variants.

CBL216

TTY 1
RC832

CBL308

CBL312

TTY 2
RC835

CBL308

J4

J5

J6 CBL268

PTR500
PTI500

RC3803S

J1

J7 CBL245

PUN701

CBL142

J2

J3

CBL075

CBL065

J1

OCP703

P1 J2

CBL126

POWER CABLES

J2 J3 J4 J4 J4 J4 J4

PDP711

J1

CBL879

220VAC MAINS

CHS701

Additional
Controller
Chassis

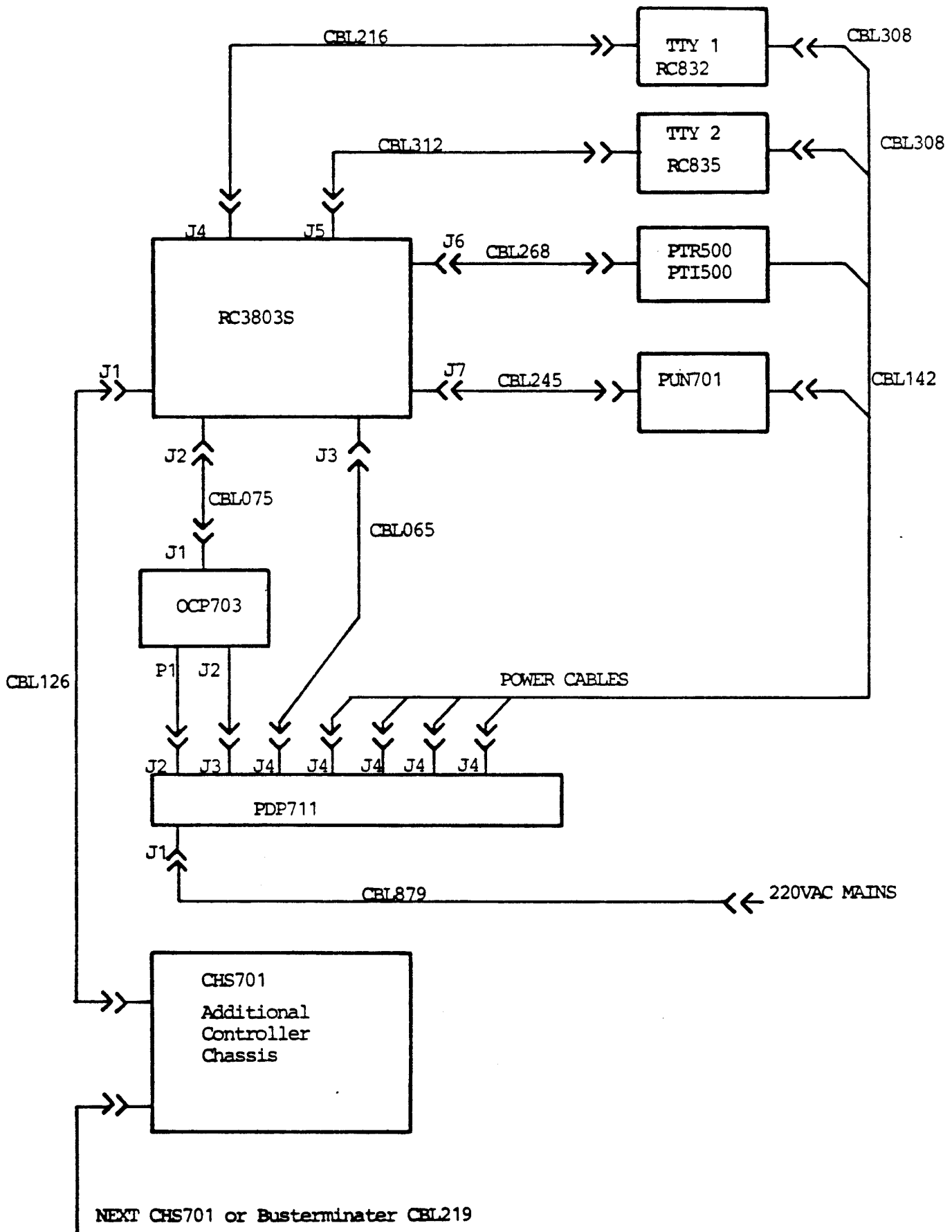NEXT CHS701 or Busterminater CBL219

Fig. 4 Interconnection Diagram.

4.5   Installation of Program Load PROM's   4.5

For Automatic program load, 3 PROM's must be installed on the CPU720/CPU721 board:

CPU720 board	CPU721 board
IC position 58: ROM789	IC position 73: ROM789
IC position 71: ROM791	IC position 82: ROM791
IC position 81: ROM790	IC position 71: ROM790

DIP-sockets are provided in the three positions, so installation is carried out without using soldering tool.

For details on the autoload PROM's refer to RCSL No 52-AA894: Hardwired Testprograms and Program Load to RC3803.

4.6   Configuration of Memory Interface   4.6

The Strapping option S1 in CPU720/CPU721 provides the user to configure the RC3803S with other memory boards than MEM720. When using the MEM720 the Strap S1 should be in the closed position. Otherwise this connection should be disconnected.

The locations of S1:
            * CPU720: position 21
               CPU721: position STI

*Note: The FCO-list should be checked.

5.   CHECK-OUT PROCEDURE   5.

Upon installation the following check out procedure should be carried out.

a. Visually inspect the cabling to insure correct interconnections.

b. Set the Parity Error Reset switch on the CPU front panel in position UP. The Stop switch should be set in position DOWN. Turn on the power and check the DC voltages +5V, +12V and -12V at the top of the CHS718 chassis. The voltages should be within ± 2% of their nominal values.
   Adjust if necessary (Rear side of chassis).

c. Verify that the indicators are lit according to the following list:

Indicator Name	Location	State
POK	Front of CHS718	ON
PINT	Rear side of CHS718	ON
FETCH	Front of CPU720/CPU721	ON
DEFER	Front of CPU720/CPU721	OFF
PARITY ERROR	Front of CPU720/CPU721	OFF
POK	Operators Control Panel	ON
RUN	Operators Control Panel	ON
AUTOLOAD	Operators Control Panel	OFF
MEM.INIT. DISABLE	Front of MEM720	OFF

Active the PINT RESET switch on the rear side of the chassis and check that the PINT indicator turns off.

Activate the MEM.INIT.DISABLE switch on the front panel of MEM720 and check that the indicator turns on.

d. Set the Autoload Device Select switches on the CPU720/CPU721 (octal). This causes the build in memory test program to be selected.
   Press the AUTOLOAD push-button on the OCP703 and observe that the RUN and AUTOLOAD indicators changes state i.e. RUN is turned off and AUTOLOAD is turned on. The FETCH indicator on the CPU720/CPU721 should remain lit, and the PARITY ERROR indicator should remain off.

e. Then change the state of the Autoload Device Select switches to 02 (octal), bit 0 set, and press autoload. Now the CPU should run a character generating program, outputting 80 characters per line on the console.

A character echo program is selected if bit 0 is reset (dev. no. unchanged) and autoload is activated. The program transmits on the teletype output each character received on the teletype input.

f. Load the CPU720 extended instructions set testprogram, 52-AA900 or latest revision, and run the program successfully for at least 3 passes (approx. 20 minuttes).

g. Load the RC3600 extended memory test, 44-RT1648 or latest revision, and run the program successfully for at least 2 passes (appr. 40 minuttes). The program should be initialized using the following parameters:

    Startaddress: 400
    First Memory Location: 11614
    Last Memory Location: 177777
    Memory Type:
The message: "Miserable Timing" should be ignored.

h. If a paper tape punch is installed, run the Paper Tape Punch Reliability program. The hereby produced paper tape should be used during the execution of the Paper Tape Reader Reliability program.

If errors are detected during the above listed procedure, one or more diagnostic program may be needed in the subsequent faultfindings. In the following, applicable test program are listed:

ABS.BIN.

paper tape	Document	Text.
44-RT1715	44-RT1714	RC3600 CPU Logic Test
44-RT985	44-RT983	RC3600 Checkerboard III
44-RT1625	44-RT1623	RC3600 Checkerboard IV
44-RT974	44-RT972	RC3600 Checkerboard V
44-RT1349	44-RT1353	RC3603 Exerciser
44-RT1807	44-RT1806	Testprogram for RTC702
44-RT1003	44-RT1001	Test for TTC705/TTC706
44-RT1558	44-RT1557	RC3600 Instruction timer test
44-RT1346	44-RT1350	Rc3603 Address Test

Note that most of the programs listed requires a TCP701
Diagnostic Panel to be mounted on the 1001 edge connector of the
CPU720/CPU721. Refer to RCSL No 52-AA542: "Programmers Reference
Manual for TCP701".

RETURN LETTER

Title: General Information RC3803S Revision 1 RCSL No.: 44-RT 2071

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