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Technical Manual for Disc File Controller RC 4818C.

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RC 4818D/RC 4819D MAGNETIC DISC
and
RC 4818C DISC FILE CONTROLLER
REFERENCE MANUAL

Keywords : RC 4000, Peripheral Device, RC 4818, RC 4819 Disc Store, Logical Structure, Reference Manual.

Abstract : This paper describes the logical structure of the RC 4818D and RC 4819D magnetic disc and the RC 4818C disc file controller (DFC 403) when used in connection with the RC 4000 computer.

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1. MAIN CHARACTERISTICS

The disc file controller DFC 403 is designed to control 1 to 8 disc stores of the type RC 4818D or RC 4819D.

RC 4818D and RC 4819D may be mixed at the same controller.

The RC 4818D disc has a capacity of 9.354.240 words each of 24 bits.

Physically the disc is organized as follows:

Segments	:	36540 segments each of 256 words
Cylinders	:	203 cylinders, i.e. possible head positions, each of 180 segments
Heads	:	20 heads, each having access to one track with 9 segments

The RC 4819D disc has a capacity of 18.708.480 words each of 24 bits.

The total capacity per controller with 8 RC 4819D discs is therefore 149.667.840 words. Physically the disc is organized as follows:

Segments	:	73080 segments each of 256 words
Cylinders	:	406 cylinders, i.e. possible head positions, each of 180 segments
Heads	:	20 heads, each having access to one track with 9 segments

A transfer of a data block to or from the disc is separated in two operations, - namely a cylinder selection followed by the actual data transfer.

The cylinder selection can be executed on several discs simultaneously. This is possible because the discs are connected to the controller via a party line system and because neither the controller nor the party line system is busy during the cylinder selection, only during the initiation.

The cylinder selection time varies from 7 to 70 milliseconds depending on the number of cylinder displacements. Nominal disc speed is 2400 revolutions per minute and nominal bit rate is 2.5 megabits per second.

The data transfer is done via the RC 4000 high-speed data channel, i.e. a data block is transferred directly to or from the internal store. The data block is composed of a variable number of consecutive segments.

The data transfer times are specified as follows:

1. Average transfer rate:
   92000 words per second
2. Transfer rate within a segment:
   104000 words per second
3. Average transfer time for transport inside a selected and positioned cylinder:
   (13 + 2.8 * number of segments) milliseconds
4. Average transfer time for transports including cylinder shifts:
   (48 + 2.8 * number of segments+8.3 * number of cylinder shifts) milliseconds

The data transfer operation can only by executed on one disc at a time, and the controller will be busy in the transfer period. Therefore new cylinder selections cannot be initiated during the data transfer operation.

Two interrupt channels are associated with the disc controller, one indicates, that a data operation is completed, the other indicates, that at least one head movement is completed.

Cylinder selections and data transfers are initiated via the RC 4000 low-speed data channel by means of control commands as described in the following sections.

2. I/O COMMANDS

2.1 Control Commands

2.1.1 Control Command Modifications

The control commands are used to specify and initiate cylinder selections and data block transfers. The disc controller accepts 12 modifications of the control command:

5 transfer first	<cyl,head,sector>
9 transfer size	<number of segments>
13 input data	<first storage address>
17 output data	<first storage address>
21 input address	<first storage address>
25 output address	<first storage address>
29 select disc	<disc number>
33 return to zero	<irrelevant>
37 transfer forward	<abs (cylinder difference)>
41 transfer reverse	<abs (cylinder difference)>
45 set mode	<mode>
61 master clear	<irrelevant>

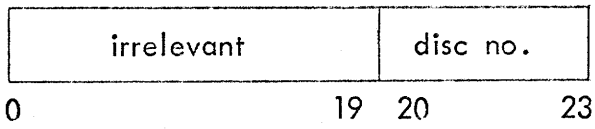
The integers denote the values of bits 18-23 in the effective address of the input/output instruction. The parameters in the brackets < and > denote the contents of the working register selected by the input/output instruction.

The parameters are interpreted as follows:

< disc number >	modulo 16
< abs (cylinder difference) >	modulo 512
< cylinder, head, sector >	modulo 512, 32, 16
< number of segments >	modulo 512
< first storage address >	modulo 262144
< mode >	modulo 16

2.1.2 Select Disc

While the disc controller is addressed by means of the device address of the input/output command, the disc itself must be selected by the control command select disc. The discs are numbered 0 to 7. In the disc select command a disc address word with the following format is transferred:



The effect of the select disc command is that all succeeding commands operate on the disc defined in the disc number word.

The disc and the controller are available immediately after the execution of the select disc command.

2.1.3 Return to Zero

The control command return to zero moves the read/write heads to cylinder 0. The command is normally used when the head position is unknown. This is the case after pack unsafe, intervention, synchronization error or data overrun. The reason for this is that the data operation is terminated as soon as the error is recognized, and that a possible cylinder shift may or may not have taken place.

The controller is busy approximately 10 μs after the return to zero command is issued. Then the controller becomes available for operations on other units connected to the controller.

While the movement of the heads is in progress, bit 11 in the status 0 word (heads moving) is set, if the disc unit in question is selected.

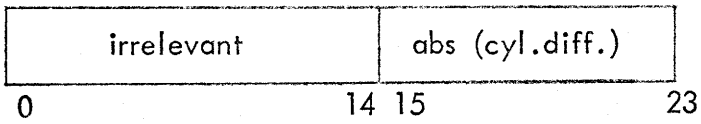
When the transfer of the heads to cylinder 0 has been completed (approx. xx to yy ms depending of initial distance from cylinder 0), the heads moving bit belonging to the disc unit in question will be cleared and a head interrupt will be generated. If an input/output address or data operation is in progress on another disc, when the head transfer is completed, the head interrupt will be delayed until the end of this operation.

Seen from the programmers point of view the data interrupt will then appear simultaneously with the head interrupt.

For this reason the head interrupt must be connected to an itr-channel with higher priority (lower number) than the itr-channel of the data transfer interrupt.

2.1.4 Transfer Forward and Transfer Reverse

These control commands initiate the cylinder selections, i.e. the positioning of read/write heads. In the transfer forward command the cylinder address is increased with abs (cylinder adifference) as specified in the transferred parameter word. The format of this is



In the transfer reverse command the cylinder address is decreased with abs (cylinder difference).

The controller is busy approximately 10 us after a transfer forward or a transfer reverse command is issued. Then the controller becomes available for operations on other units connected to the controller.

While the movement of the heads is in progress, bit 11 in the status 0 word (heads moving) is set, if the disc unit in question is selected. When the transfer of the heads has been completed (7 to 70 ms depending of the cylinder difference, average 35 ms), the heads moving status bit belonging to the disc unit in question will be cleared and a head interrupt generated. If an input/output address or data operation is in progress on another disc, when the head transfer is completed, the head interrupt will be delayed until the end of this operation.

It is possible to initiate a data transfer operation on a disc even if the cylinder selection has not been completed. In this case the controller will delay the data transfer until the heads are positioned. The head interrupt will then come at the end of the data operation and simultaneously with the interrupt from this.

The transfer forward/reverse command can be omitted if the segment address corresponds to the previous cylinder address.

A transfer first command (see 2.1.5) with the absolute value of the new cylinder address (bits 3:11) must be executed prior to the execution of the transfer forward/reverse command, because some of the bits in the absolute cylinder address are used in the disc unit for checking the head movement. The cylinder address is buffered in the selected disc drive during the head movement, so new transfer first commands may follow after the transfer forward/reverse command, with the purpose of specifying a head positioning on another disc drive or specifying a first segment address in a data transfer.

The transfer forward/reverse command must be executed before the transfer size command because the size register is used as a temporary buffer for the cylinder difference.

Positioning of heads to a non existing cylinder will be terminated with seek error and synchronization error status bits set.

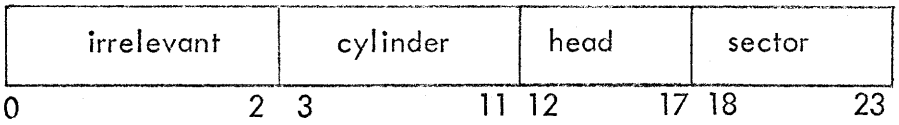
Cylinder shifts will take place automatically during a data transfer operation, if the specified data block is (or is to be) placed on more than one cylinder. This must be considered during the calculation of the next cylinder difference.

2.1.5 Transfer First and Transfer Size

A data transfer operation requires specification of a set of consecutive segments on the disc and a storage location. This specification must be presented for the disc controller in the mentioned order:

The control commands transfer first and transfer size are used to specify the set of consecutive segments. The first command transfers the address of the first segment and the second command the number of segments.

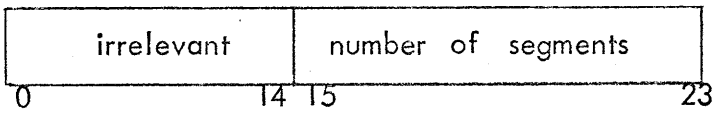
The segment address word is interpreted as follows:



where $0 \leq$ cylinder $\leq 405, 0 \leq$ head ≤ 19, and $0 \leq$ sector ≤ 8. The relation between a segment number and the segment address constituents is:

segment number = 180 * cylinder + 9 * head + sector

In the transfer size command the parameter word has the following format:

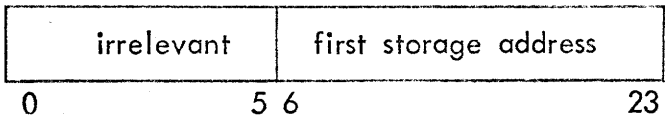


The contents of the size register is destroyed by the transfer forward/reverse commands.

The disc controller is available immediately after the execution of the transfer first and transfer size commands.

2.1.6 Input Data and Output Data

These control commands define a storage location and initiate a block transfer. The storage location is given by the first storage address word, transferred and interpreted as follows:



The data block will be transferred with the first word in the storage location specified by first storage address. The rightmost bit of this parameter (bit 23) is ignored. Thus it is irrelevant whether the parameter refers to the left or right half of the storage word.

The input data command initiates a transfer from disc to internal store. The output data command initiates a transfer from internal store to disc. After initiation of a data transfer, the disc controller is busy until the data operation is either completed successfully or terminated by an error condition. The disc delivers a data interrupt signal when it after a data transfer becomes available.

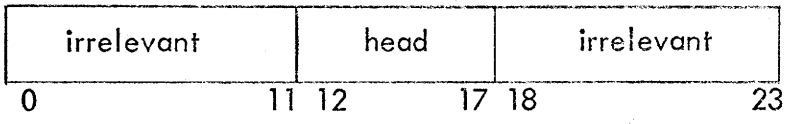
2.1.7 Input Address and Output Address

The disc surface is physically divided into sectors separated from each other by sector gaps. Each sector contains preamble bits (zeros), address marker word, address word, parity word for address (longitudinal odd parity), gap, preamble bits (zeros), marker bit (one), 256 data words, parity words for data (longitudinal odd parity), and tolerance gap. The address marker word is used to detect a sector start. The segment address word identifies the segment. A new disc pack must be supplied with address marker words and segment addresses before use.

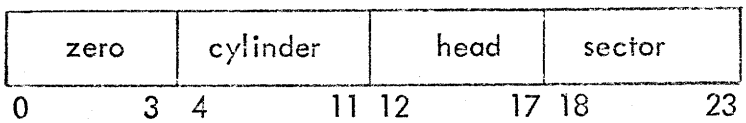
The segment addresses may afterwards be input for checking. The input and output of segment addresses follow a similar scheme as given for input data and output data.

In details, writing of segment addresses is done in 3 steps:

1) Positioning of heads to actual cylinder by means of the commands transfer first, return to zero, transfer forward, and transfer reverse.
2) Head selection by means of the transfer first command. The parameter word is interpreted as follows:



3) Writing of segment address words on the now selected track by means of output address. This command initiates writing of 9 segment address words in the sectors 0 to 8. The first storage address in the command refers to a buffer area of 9 words, the contents of which must be 9 consecutive segment address words. The format of each word should be:



The address marker words and parity words are generated automatically by the disc controller during the executing of the segment address writing.
The disc controller is busy during writing of segment addresses, and when it afterwards becomes available an interrupt signal is generated.

Use of the command transfer size is irrelevant (will be ignored) because the controller always writes 9 segment addresses per operation.

The sequence of the segment addresses should be shifted 3 per cylinder to enable cylinder shifts in 1/3 revolution (8.3 msec.).

All segment addresses must be written before checking is relevant. The checking is carried out in 3 steps:

1) Equivalent to step 1 of segment address writing.
2) Equivalent to step 2 of segment address writing.
3) Reading of segment addresses by means of input address.
   This command initiates reading of 9 segment address words in the sectors 0 to 8. First storage address of the command refers to a buffer area to which the 9 segment address words are transferred.

The format of the segment address word for the commands input and output address are identical.

The disc controller is busy during reading of segment addresses, and when it afterwards becomes available an interrupt signal is generated.

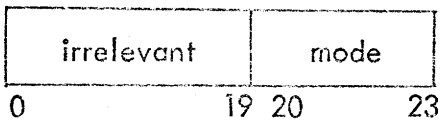
When the address markers have been written it is a good practice to initiate the data area by overwriting all segments with zeros. This will avoid status errors in case of superfluos reading later.

Notice, that this initiation always should be done. This means that if the address markers on an old diskit need a "shine up" the relevant data areas must be dumped at first.

2.1.8 Set Mode

This command is for diagnostic purposes only.

In the set mode command the parameter word has the following format:



The 4 bits in the mode register is thus under control of the set mode command. Each bit in the mode register has certain effects on the status generation when set, and may be used for checking the status generation. The meaning and effect of the mode register bits is as follows:

mode (20): Inhibit index. When set, the index pulse from the disc drive is removed. This causes input address or output address operations executed with mode (20) set, to be terminated with the timer status bit set. CR(3) in the sense 32 status word (see section 2.2.3) should be set.

The inhibit index will not have any effect on other operations.

mode (21): Inhibit CYS Requests. When set, cycle stealing requests to the RC 4000 core store are inhibited. This causes data or address transfer operations to be terminated with data overrun status bit set.

mode (22): Modify preamble. When set during an output address operation the address marker words will be slightly modified.

When the segments in question later are operated on with either input address, input data or output data, the operation will be terminated with status bits sync error and wrong 2nd index set.

mode (23): Inhibit parity. When set during write address operations, the address parity word will be written as zero.

When the segments in question later are operated on with input address, input data or output data the parity error status will be set. For input data and output data further more sync error and wrong 2nd index will be set. If mode (23) is set during write data operations, the data parity word will be written as zero.

When the segments in question later are operated on with read data operations, the parity error status bit will be set provided that the longitudinal parity of the written data is different from all ones (-1).

2.1.9 Master Clear

The control command master clear brings all important bistables in the disc file controller in a well defined initial state. The master clear signal may also be generated by the master clear switch at the controller or during a power up sequence.

The master clear command has no effect on the bistables in the disc drive (e.g. pack unsafe, pack change). The command has effect even when the controller is busy. The parameter word associated with the command is irrelevant.

2.2 Sense Commands

2.2.1 Sense Command Modifications

The sense commands are used to inform the programs about the state of the controller and the result of previous operations. The disc controller accepts 2 modifications of the sense command:

0 sense status 0	<status 0>
32 sense status 32	<status 32>

The leftmost integers denote the values of bits 18-23 in the effective address of the input/output instruction.

Bits 0-11 in status 0 word can be considered as the main status, which is required for normal operation in the RC 4000 system. Bits 12-23 in status 0 word and bits 0-23 in status 32 word are status bits, which are generated for technical diagnostic purposes only.

The status bits can be divided in two groups:

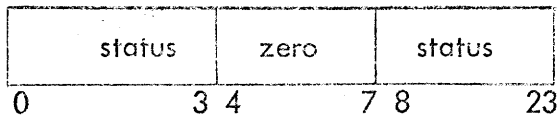
Type 1: Bits, which logically belong to the controller, and which are common to all disc units. They specify the result of the latest performed data or address operation and are independent of the contents of the unit register. They will normally be cleared by the next input/output data or input/output address operation.

Type 2: Bits, which logically belong to each disc unit, and which are selected by means of select disc command. They thus indicate the state of the currently selected disc unit. These bits are only affected by actions applied to a specific disc unit (manual or program).

The sense 0 command can only be executed when the controller is ready and connected, whereas the sense 32 command only requires the controller to be connected, because the controller always signals ready to the CPU, when this specific command is issued. The status 32 information is thus available even when the controller is busy.

2.2.2 Sense 0

When the disc controller is available, (i.e. ready and connected), a status 0 word can be transferred to a working register by means of a sense 0 command. The format of the status word is:



The status bits have the following meaning:

Bit No.	Meaning	Type
0	intervention	2
1	parity	1
2	timer	1
3	data overrun	1
8	disc in local	2
9	pack unsafe	2
10	synchronization error	1,2
11	heads moving	2
12:15	command register	1
16:23	unit selected	2

The synchronization error status bit represents error status bits both of type 1 and type 2.

2.2.2.1 Intervention

Intervention indicates that the selected disc is in local mode or has been in local mode since the most recent data transfer operation.

The intervention bit is set when the disc goes from remote to local state. The bit is reset by the first input/output data or input address command to the selected disc, but only if the disc is returned to remote state.

Setting of intervention implies a termination of a possible current operation on the disc.

The intervention bit will also be set when no disc is connected to the controller corresponding to the unit number selected.

2.2.2.2 Parity Error

This status bit indicates a parity error in one or more segments transferred in the most recent data input operation.

The parity error status is set when recognized by the controller. Recognization of the error will not terminate the operation. The status bit is reset by the first input/output data or input/output address command.

or data (se diagram) / HJ

2.2.2.3 Timer

This status bit indicates, that the controller has been busy for longer then 3 seconds and has failed to complete the required operation.

Only operations, during which the controller is busy is supervised in this way.

Head movements are thus not supervised by the controller, but each disc has a local timer to supervise the head movements. Time out in this case indicated by seek error and synchronization error status bits.

time is cleared by in/output data/address
(see diagram 1F028) / Hj

2.2.2.4 Data Overrun

Data overrun indicates overloading of the high-speed data channel. Further data transfers are suppressed and the operation terminates. The status bit is reset by the first input/output address command.

2.2.2.5 Disc in Local

Disc in local indicates that the selected disc cannot be controlled by the disc controller due to one or more of the following situations:

- cable between controller and disc is removed.
- power to the disc electronics is switched off.
- disc motor not at the proper speed.
- disc number plug has been removed.
- operator has interfered by means of the maintenance panel switches.

The transition to local sets the status bit and terminates a possible current operation. When the disc returns to the remote state, the status bit disc in local is reset.

Operations initiated in local state are not buffered but terminated immediately.

2.2.2.6 Pack Unsafe

Pack unsafe may be set due to several hardware malfunctions or irregular control of the selected disc.

The setting of this status bit terminates any operation in progress immediately.

When it is set, the FAULT indicator on the disc unit in question is illuminated and any operations on this unit will be terminated immediately. The status bit can only be cleared by manually depressing the FAULT switch. (see section 5).

2.2.2.7 Synchronization Error

This status bit indicates one or more of the following errors:

Wrong 2nd index (type 1),
Address error (type 1),
Drop out (type 1),
Seek error on selected disc (type 2).

These error bits are described in detail in later sections.

All the above mentioned errors terminates the current operation immediately. The status bit is reset by the first input/output data or input/output address command if it is set due to one or more of the three first mentioned errors.

If the bit is one due to the last mentioned reason, the bit will be cleared by the first return to zero command to the selected disc or by selecting another disc number.

2.2.2.8 Heads Moving

Heads moving indicates that a head positioning on the selected disc takes place. The status bit is set by a transfer forward/reverse or return to zero command, and is reset when the head positioning has been completed.

2.2.2.9 Command Register

Status bits 12:15 contains the 4 modifier bits of the latest control command issued to the disc controller (i.e. bits 18:21 in the address part of the input/output instruction).

2.2.2.10 Unit Selected

These 8 status bits indicates the select status of the 8 possible discs, which can be connected to the controller, one bit for each disc. A one in a bit position indicates, that the disc connected to the B cable position associated with the bit position is selected. This means, that the disc in question has a logic number plug corresponding to the current contents of the unit register.

Not more than one bit in the unit selected register should be set at a time, i.e. not more than one disc should have a given unit number.

Note that there is no certain relation between bit positions in the unit selected register and unit number, because logic number plugs may be installed and interchanged independent of the physical installation of the cables.

2.2.3 Sense 32.

When the disc controller is connected, a status 32 word can be transferred to a working register by means of a sense 32 command. Note, that the transfer is independent of the ready/busy state. The controller simulates ready with regard to this command even when it is busy. The status bits have the following meaning:

Bit No.	Meaning	Type
0:14	CR(0:14), control register	1
15	Wrong 2nd index	1
16	Address error	1
17	Drop out	1
18	Seek error	2
19	Pack unsafe	2
20:23	Unit register	2

2.2.3.1 Control Register

The control register is a 16 bit register, which specifies the state of the controller when performing a data or address operation.

One and only one of the 16 bits should be set at a time. The position of the bit set in the register specifies the state. A short description of the operation performed in each state follows:

CR(0): Ready state. No data operation in progress.

CR(1): Waiting for head movements to be completed. If already completed, only 0.4 μs in this state.

CR(2): Transfer head address to head register in selected disc drive. Duration 3.2 μs.

CR(3): Input/output address operations: Wait for index pulse. Duration up to 25 ms.

Input/output data operations: Decrement "number of segments" (size) counter. Duration 0.4 μs.

CR(4): Reset readdetector. Set word counter. Duration 0.4 μs.

CR(5): Output address operation: Dummy. Duration 0.4 μs.

Other operations: Unlock readdetector. Search for 8 consecutive zeroes to be sure, that the readdetector is synchronized to a zero pattern. Duration: min. 0.4 μs, max. depending on track information.

The state may be entered several times during the search for a proper segment address record.

CR(6): Output address: Write a segment address record. Duration 285 words * 9.6 μs = 2.73 ms.

Input address: Lock readdetector to recorded pattern. Synchronize word frame on first coming 1. Check address marker word, transfer address word to core, and check parity word. In case of mismatch in address marker word go to CR(4).

Input/output data: Lock readdetector to recorded pattern. Synchronize word frame on first coming 1. Check address marker word, check address word and check parity word. In case of any mismatch go to CR(4).

CR(7): Output/input address: Decrement "segment counter". (Special 9 to 0 counter for address operations).

Output/input data: Set wordcounter for 3 words delay. Duration 0.4 μs.

Last state in input address operations.

CR(8): Output address operation: Check the correct timing of the 2nd index pulse following the end of the 9th segment address record. Duration: 77 words * 9.6 μs = 739.2 μs. The nominal position of the 2nd index pulse is in the middle of this period.

Last state for output address operations.

Input/output data operations: 2 word delay, duration 28.8 μs. Reset readdetector.

CR(9): Output data: Set wordcounter. Duration 0.4 μs.

Input data: Unlock readdetector and search for 8 consecutive zeros. Duration approximate 4 μs.

CR(10): Output data: Write data record. Duration: 261 words * 9.6 μs = 2.51 ms.

Input data: Lock readdetector. Synchronize word frame on the 1, which is recorded before the first data bit. Read and transfer the data record. Check parity. Duration 257 words * 9.6 μs = 2.47 ms. + a short synchronize time.

CR(11): If number of segments counter equals zero go to CR(0). Otherwise go to CR(12). Duration 0.4 μs.

CR(12): Increment the concatenated cylinder, head, and sector counters. In case of a count up in cylinder counter go to CR(13), else go to CR(2). Duration 0.4 μs.

CR(13): Transfer cylinder difference = 1 to selected disc drive. Duration 3.2 μs.

CR(14): Transfer absolute cylinder address to selected disc drive. Duration 3.2 μs.

CR(15): Transfer a forward move command to selected disc drive. Duration 3.2 μs. Go to CR(2).

Only the first 15 bits of the control register (CR(0:14)) can be sensed by the sense 32 command.

To avoid false sense results due to changes in the control register during sense operation, the contents of the control register is transferred through a buffer, which contents is continously updated with the 2.5 Mhz clock of the control register, except in the following two cases, where transfer is inhibited:

1) During the execution of the sense 32 command.

2) While the timer status bit is set (see 2.2.2.3). The buffer will in this case store the contents of the control register at the time, where the timer run out.

2.2.3.2 Wrong 2nd Index

The meaning of this status bit depends of the type of operation.

Output address: The status bit is set, if the position of the 2nd index pulse was either too early or too late during the writing of a track. The required speed tolerance of the disc pack during the output address operation is tighter than normal, namely $\pm$ 1.5%. If there are no severe hardware error, this status bit indicates, that the speed tolerance was exceeded.

Input address: The status bit is set, if a 2nd index occurs before 9 segment address records are found after 1st index.

Input/output data: The status bit is set, if 2 index pulses occur before the segment address record matching the specified first segment address is found.

The status bit is cleared by the first coming input/output address or data operation.

The setting of this status bit implies, that the synchronization error also will be set. (See 2.2.2.7).

The wrong 2nd index status bit terminates the operation immediately.

2.2.3.3 Address Error

Can only be set during input or output data operations and when more than 1 segment is transferred from one cylinder.

The status bit is set, if the address word belonging to the first found address marker word following a just transferred segment on the same cylinder is not matching.

The status bit is cleared by the first coming input/output address or data operation.

The setting of this status bit implies, that the status bit sync error also will be set. (See 2.2.2.7).

The address error status bit terminates the operation immediately.

2.2.3.4 Drop Out

This status bit can be set during input address and input/output data operations.

It is set, if the readdetector, when supposed to be synchronized, detects than an expected flux change is missing.

The status bit is cleared by the first coming input/output address or data operation.

The setting of this status bit implies, that the status bit synchronization error also will be set. (See 2.2.2.7).

The drop out status bit terminates the operation immediately.

2.2.3.5 Seek Error

This status bit indicates when set, that the selected disc unit was unable to complete a head positioning initiated by a transfer forward/reverse command due to one of the following reasons:

1. The heads have gone beyond the outer limits of the recording area.
2. The selected disc unit was unable to complete the desired move in a predetermined time.

A return to zero command sent to the unit, that indicates a seek error, will clear the seek error status bit and return the heads to cylinder zero. A seek error status bit implies, that the heads moving status bit of the unit is cleared and synchronization error is set.

2.2.3.6 Pack Unsafe

Pack unsafe may be set due to several hardware malfunctions or irregular control of the selected disc.

The setting of this status bit terminates any operation in progress immediately.

When it is set, the FAULT indicator on the disc unit in question is illuminated, and any operations on this unit will be terminated immediately. The status bit can only be cleared by manually depressing the FAULT switch. (See section 5).

2.2.3.7 Unit Register

The unit register is a 4 bit register, which specifies the currently selected disc unit, i.e. the value modulo 16 of the parameter word in the latest executed select disc command. The unit register is cleared by the master clear command.

3. INTERRUPT

Two interrupt channels are associated with the disc controller, a data interrupt channel and a head interrupt channel.

3.1 Data Interrupt

When an input address, output address, input data, or output data control command is issued, the disc controller is busy until the operation is either completed succesfully or terminated by an error condition. When it then becomes available, a data interrupt is delivered.

3.2 Head Interrupt

A head movement may be initiated by means of a return to zero, transfer forward or transfer reverse control command. The controller is busy in approx. 10 μs after any of these 3 commands. However, no interrupt is generated when it becomes available again. When the controller is available, a head movement may be initiated on any disc unit, which not already has a head movement in progress.

In this way several head movements may take place simultanously. When any head movement is completed a head interrupt is generated.

If two or more disc units completes their head movements simultanously, only a single interrupt is generated.

If a head interrupt is generated before a previous interrupt has been serviced, only a single interrupt will be received. Head interrupts are not generated while the controller is busy, they are delayed until the controller becomes available. If two or more head movements are completed or terminated while the controller is busy, only a single head interrupt is generated, when the controller becomes available again.

In any case the unit or the units, which have caused the head interrupt, may be identified by selecting the disc units, from which head interrupts may be expected, one after another, and examining the heads moving status bit.

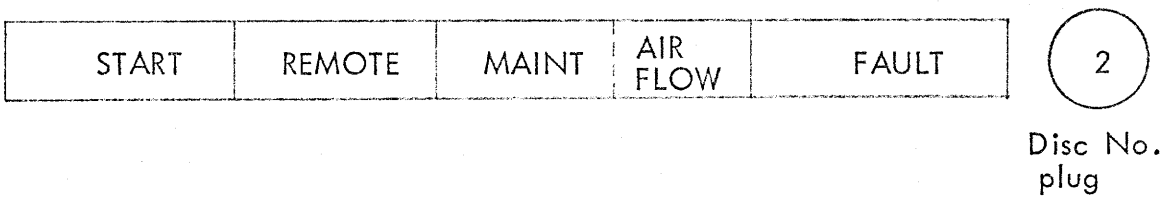
4. INDICATOR ON THE RC 4000 OPERATOR PANEL

Even if a disc controller can have up to 8 discs connected, there is just one indicator on the RC 4000 operator panel. This indicator is lit (green), when the disc controller itself is connected to RC 4000.

The status of the single disc must be observed by looking at the disc indicator panel or at the console messages.

5. DISC CONTROL SWITCHES AND INDICATORS

The disc is equipped with an operator control panel, which has the following switches and indicators:



START — is a combined switch and indicator. When the switch is depressed once, it will energize the spindle drive motor and begin the first seek sequence, provided the following conditions are satisfied:

1) The disc pack is in place
2) All covers are closed
3) Power and circuit breakers are on and maintenance control switches are in the right positions.

Depressing the START switch once more the spindle drive motor will be stopped again.

The START indicator illuminates when the START switch is in the on condition, even if a condition exists, which prevents the spindle drive motor to start.

REMOTE — is an indicator illuminated when the disc can be controlled by the computer, i.e. when the local bit in the status word is zero.

MAINT — is an indicator illuminated when the disc is in maintenance mode caused by use of different switches on the maintenance control panel.

AIR FLOW — The AIR FLOW lamp, when illuminated, indicates proper air flow rate.

FAULT — This is a combined switch and indicator.
FAULT is illuminated in consequence of different hardware malfunctions or irregular control of the disc.

The FAULT switch, when depressed, clears the FAULT memory element and extinguishes the indicator if no errors are present.

Disc No. plug:

This is an interchangeable plug with indicator. The plug defines the disc address on the party line system. The plug is equipped with a digit indicating the disc address (0 to 7). The plug indicator is illuminated when the disc in question has been selected by the select disc command.

6. LOAD METER

A load meter may be connected to the disc controller. This contains three 0 to 100% meters labelled HEAD ACCESS, ROTATIONAL ACCESS AND DATA TRANSFER.

6.1 Head Access

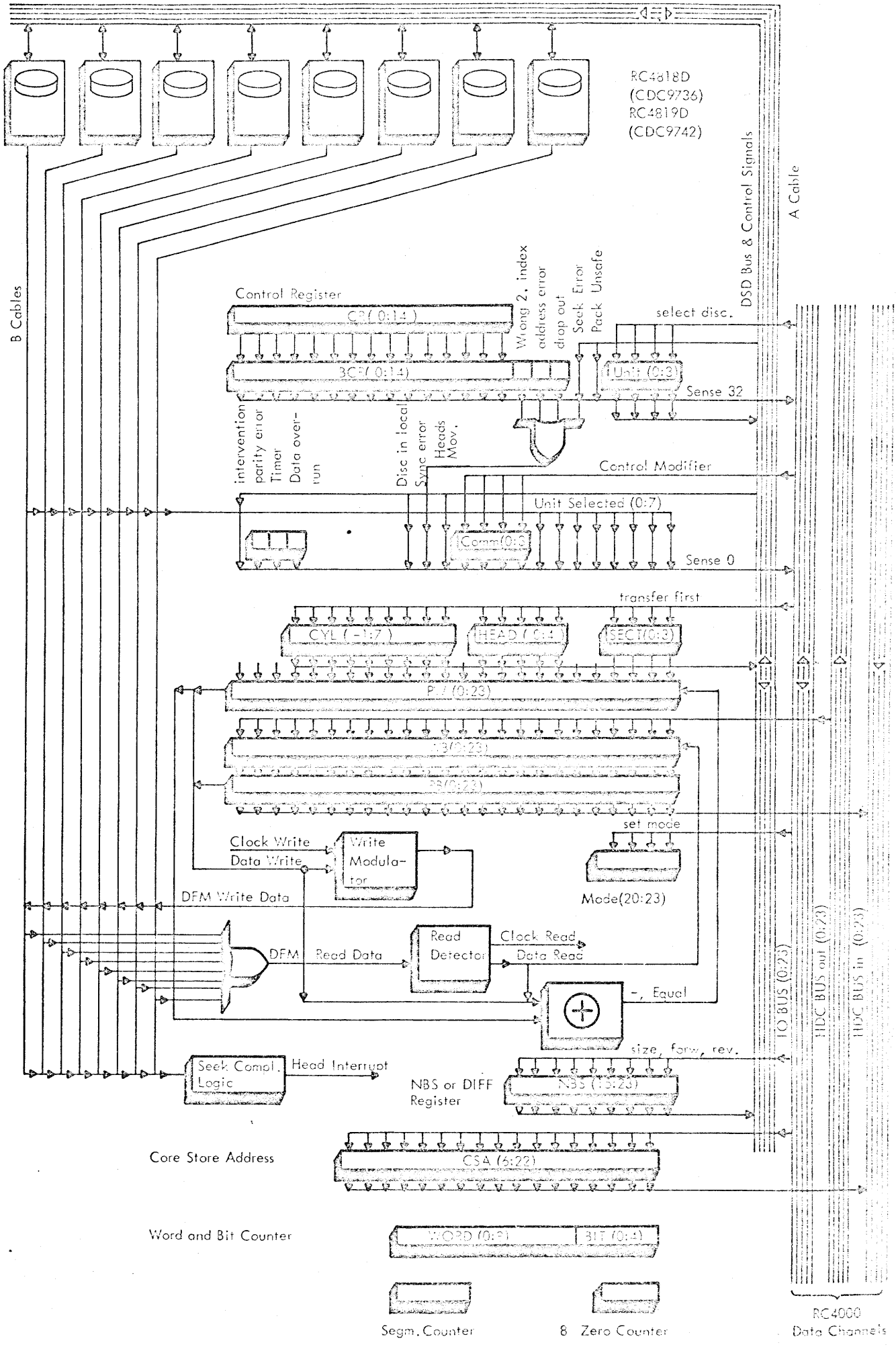
This meter indicates the relative amount of time in per cent, during which a selected disc has its heads moving.

6.2 Rotational Access

This meter indicates the relative amount of time in per cent, during which the controller is busy, has completed the head movement on the selected disc, and is waiting for the start of a segment.

6.3 Data Transfer

This meter indicates the relative amount of time in per cent, during which the controller is transferring data with the full rate of 104 kword per second.

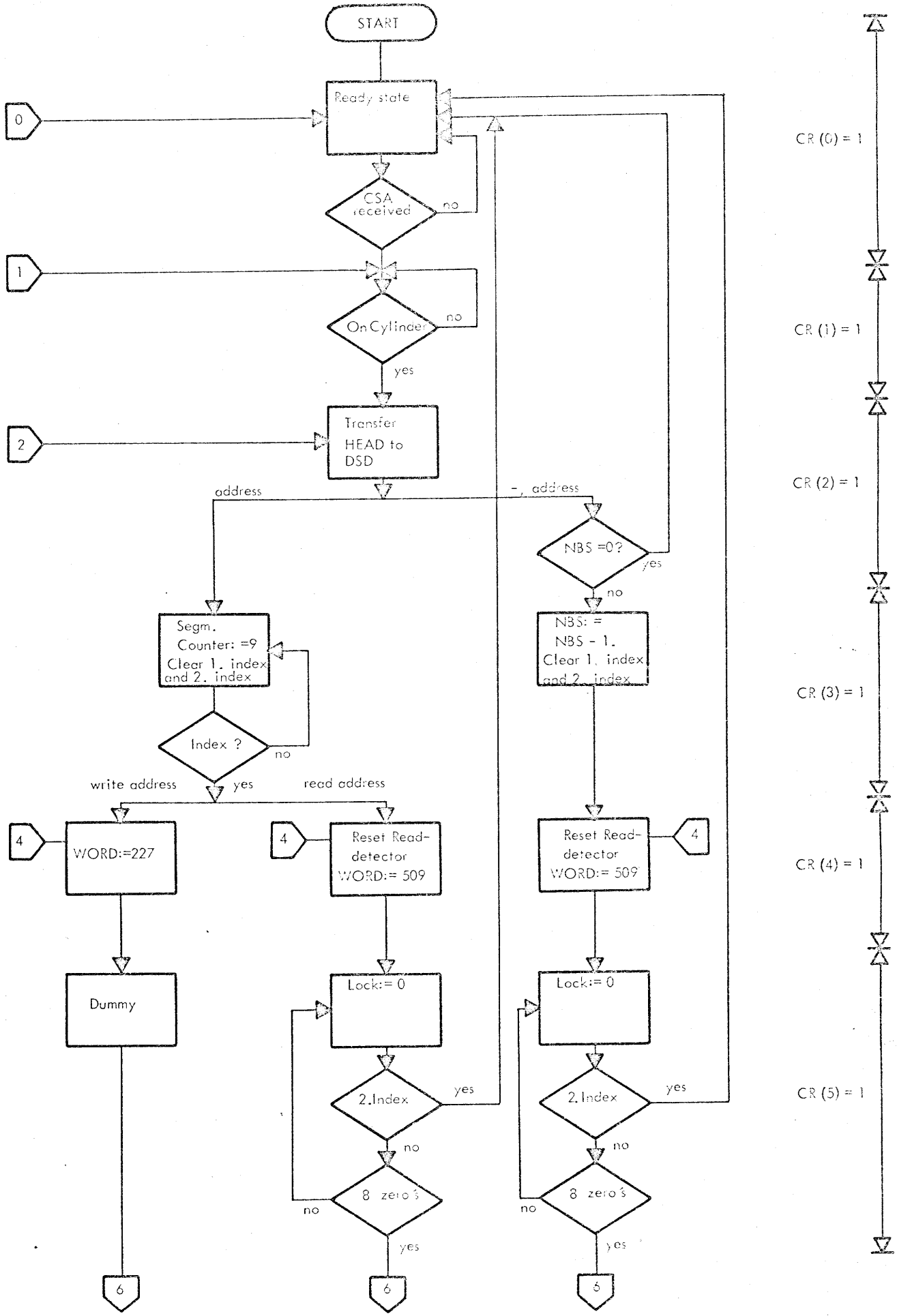


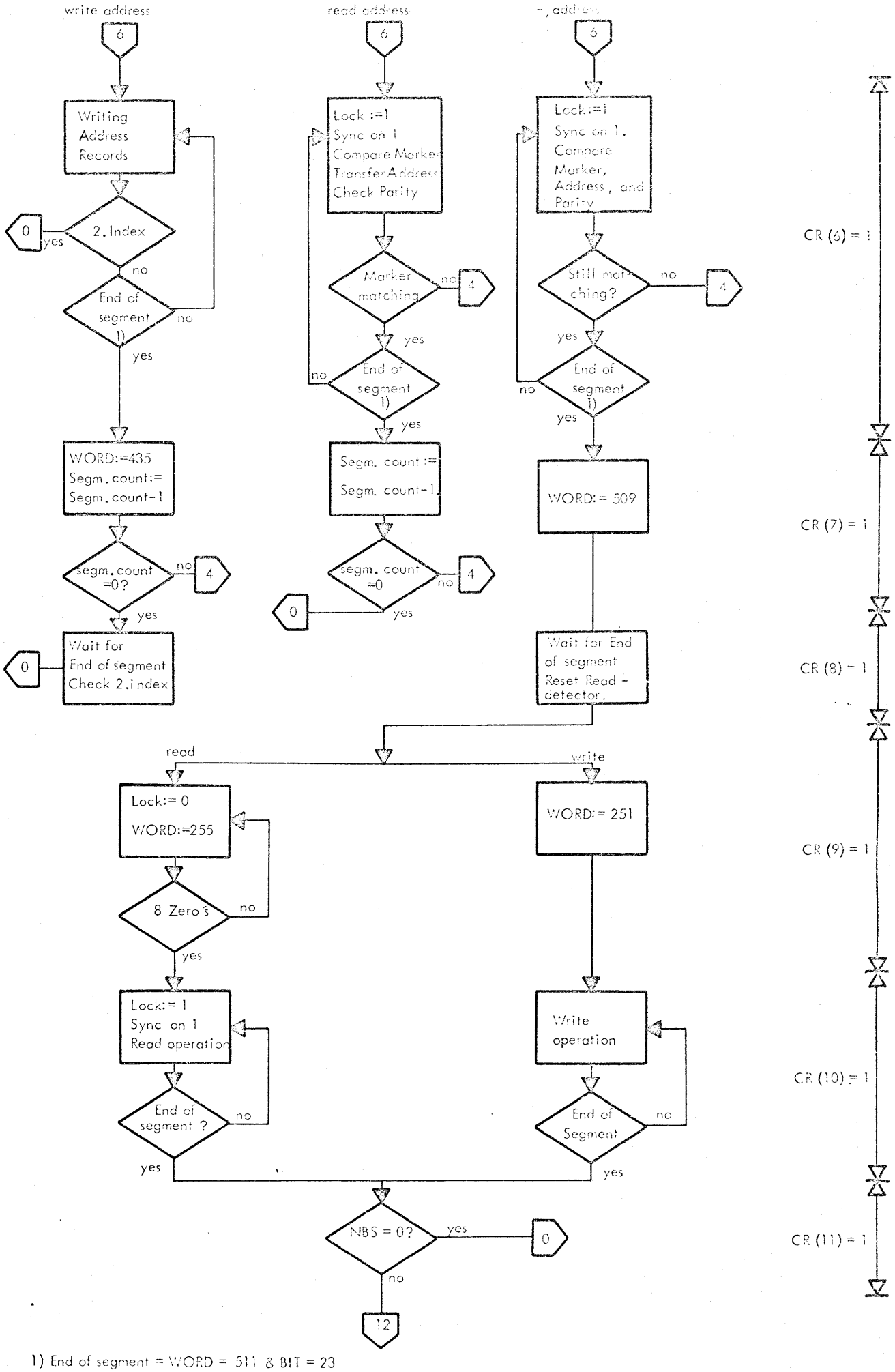
DISC FILE CONTROLLER DFC403
Register Structure

DFC403

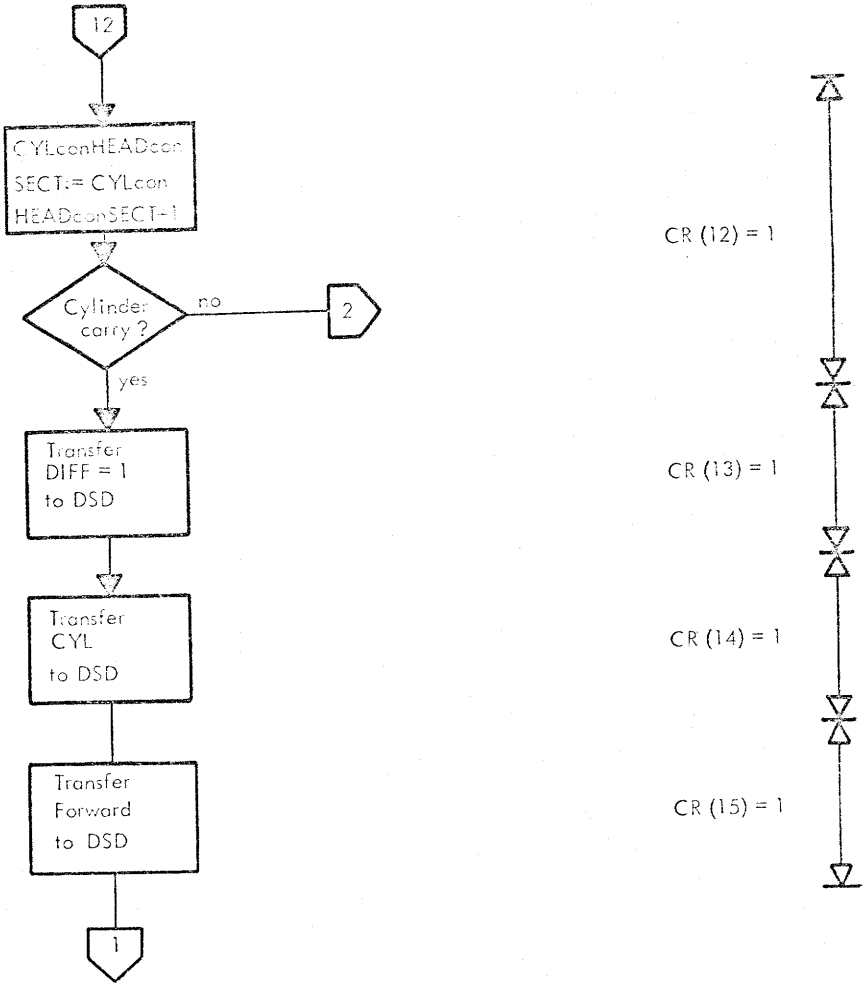
)0

13471

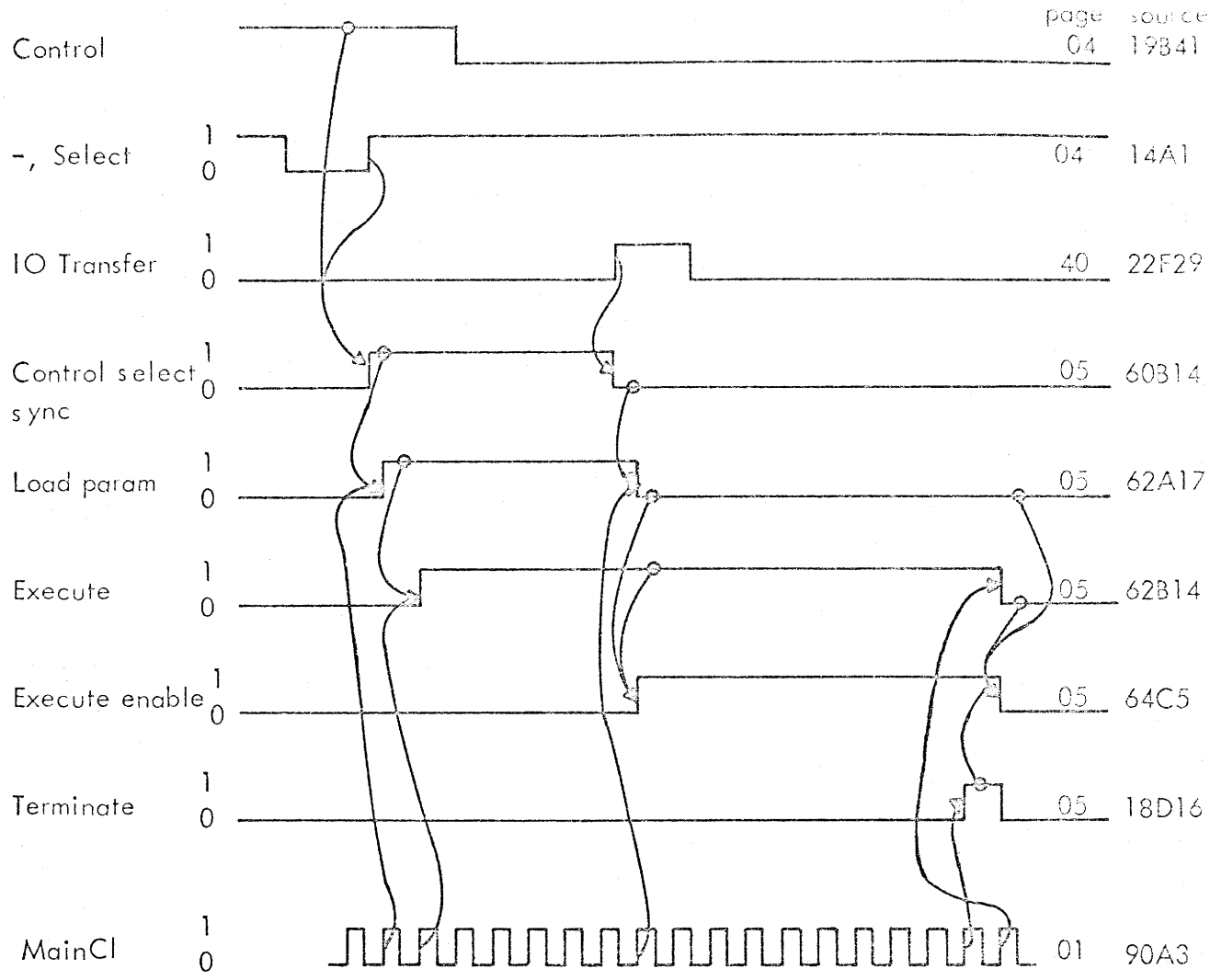

START
Ready state
0
CSA received
no
1
On Cylinder
no
yes
Transfer HEAD to DSD
2
address
-, address
NBS =0?
yes
no
Segm. Counter: =9
Clear 1. index and 2. index
NBS: = NBS - 1.
Clear 1. index and 2. index
Index ?
no
write address
yes
read address
4
WORD:=227
4
Reset Read-detector WORD:= 509
Reset Read-detector WORD:= 509
4
Dummy
Lock:= 0
Lock:= 0
2.Index
yes
no
2.Index
yes
no
8 zero's
no
yes
8 zero's
no
yes
6
6
6
CR (0) = 1
CR (1) = 1
CR (2) = 1
CR (3) = 1
CR (4) = 1
CR (5) = 1

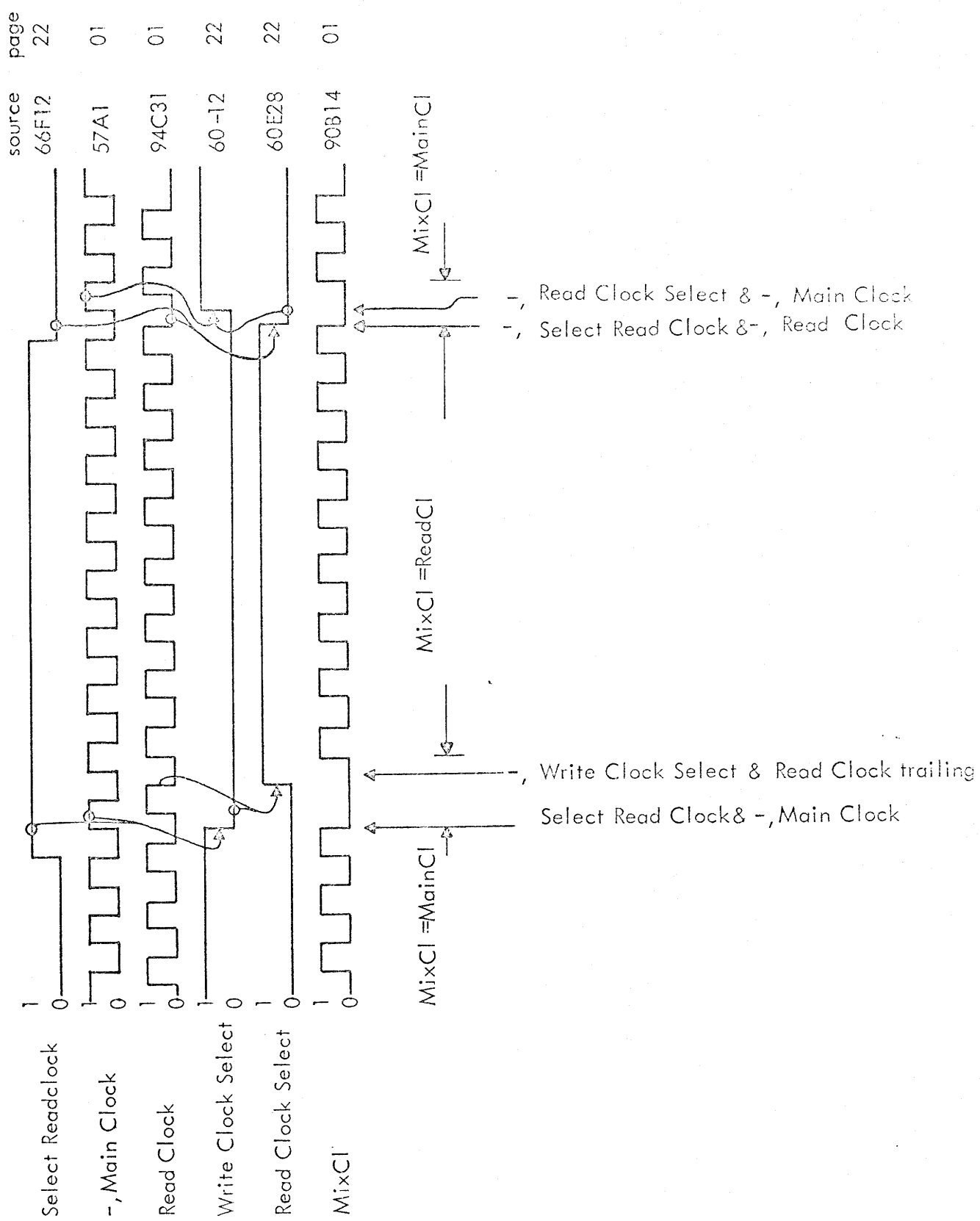


1) End of segment = WORD = 511 & BIT = 23



In all states: If-, Unit Ready! Seek Error! Data overrun! Pack Unsafe then go to Ready state
In reading state: If drop out then go to Ready state.


page source
Control
04 19841
-, Select
1
0
04 14A1
IO Transfer
1
0
40 22F29
Control select
sync
1
0
05 60B14
Load param
1
0
05 62A17
Execute
1
0
05 62B14
Execute enable
1
0
05 64C5
Terminate
1
0
05 18D16
MainCl
1
0
01 90A3



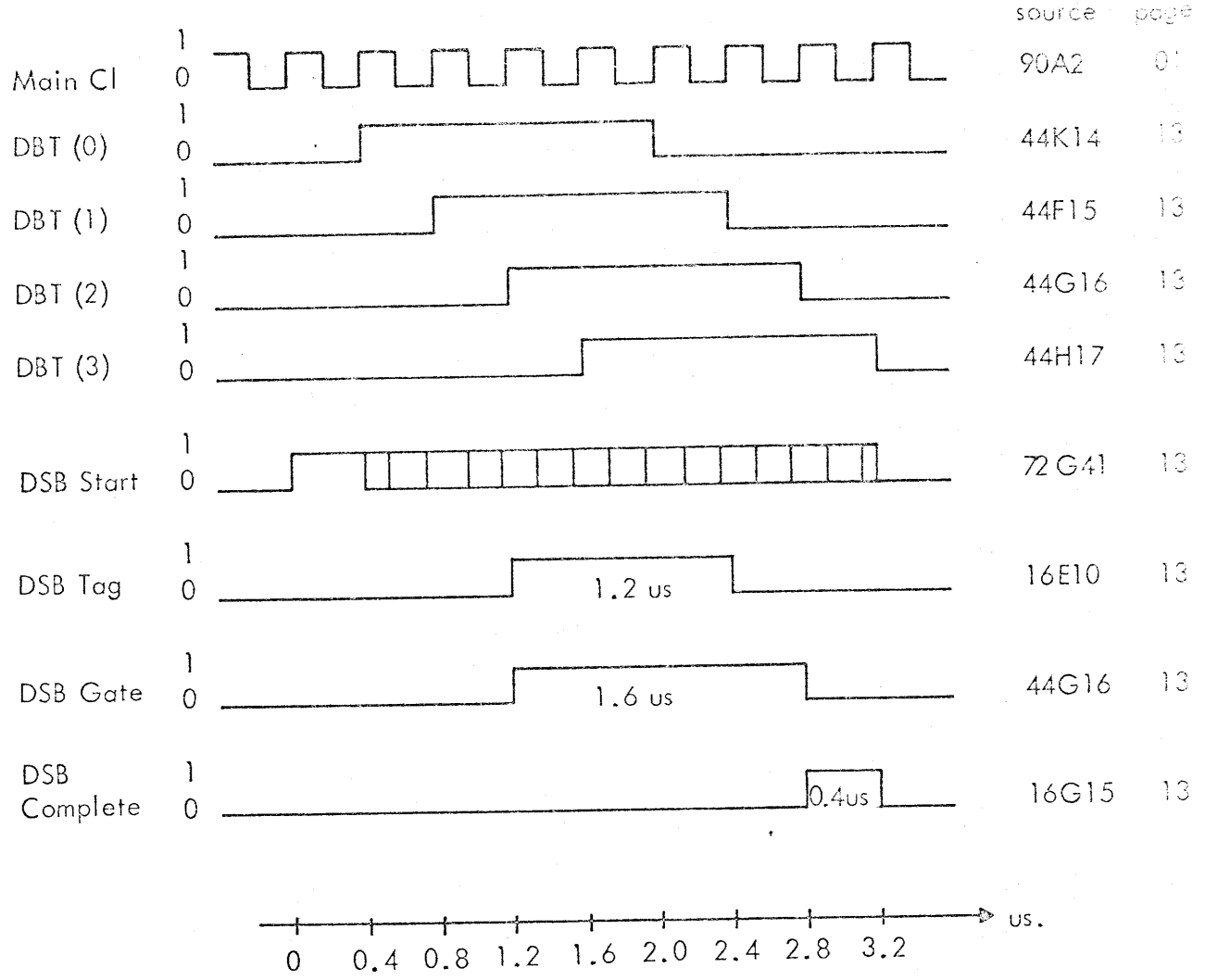
RC4000

MixCl Control Logic

DFC 403

V23255

Timing Diagram

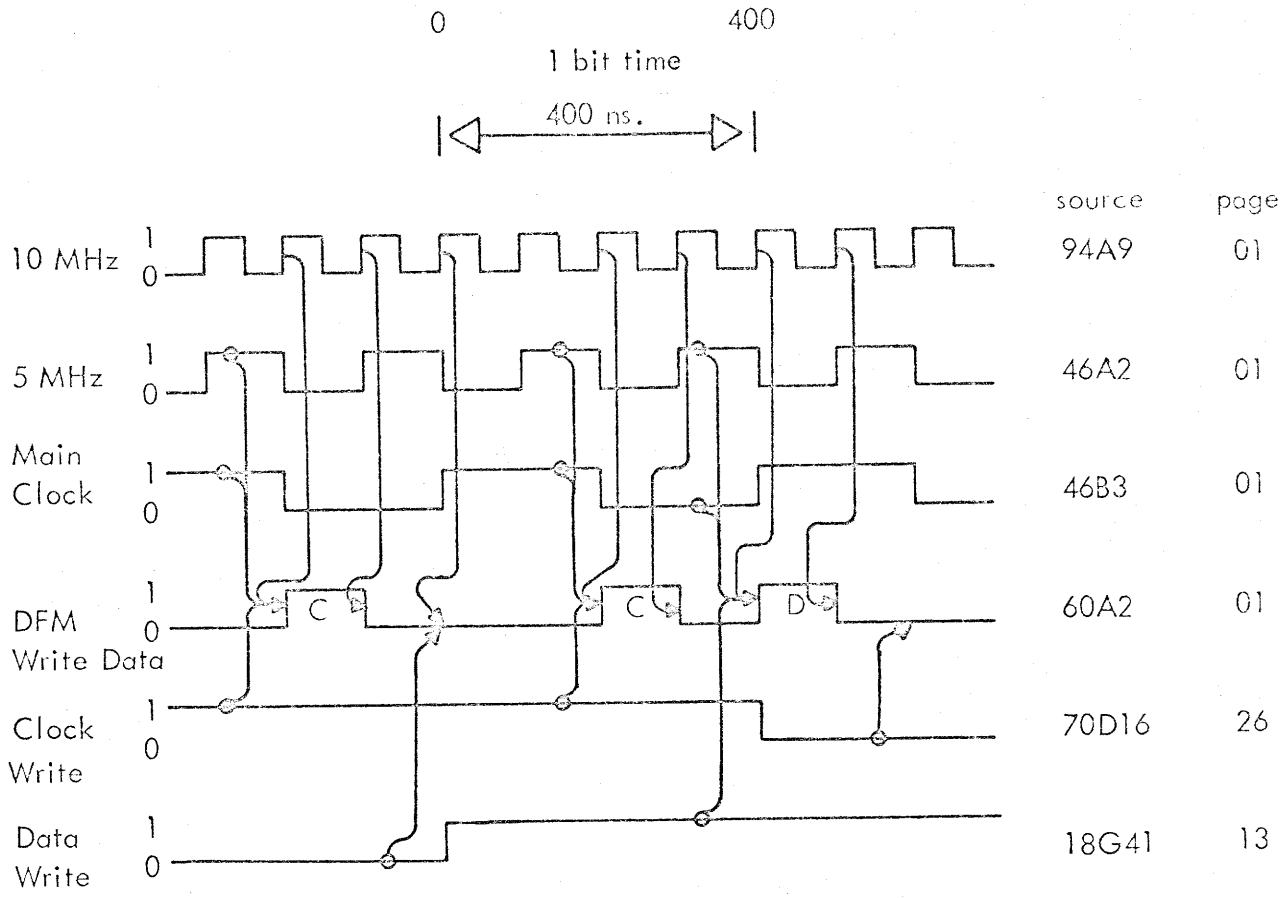


RC4000

DISC STORAGE BUS TIMER
Timing Diagram

DFC403

V23256



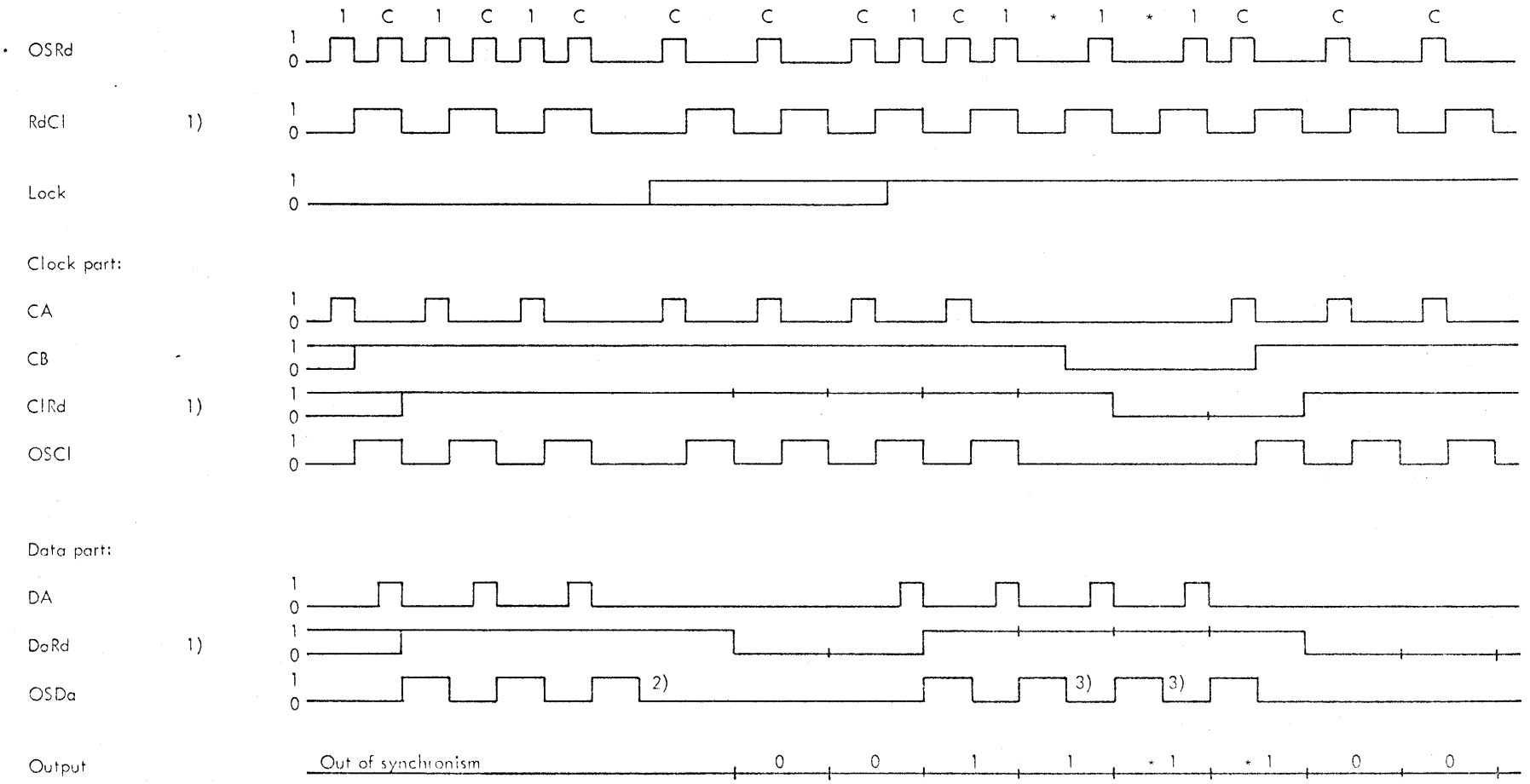
RC4000

WRITE MODULATOR
Timing Diagram

DFC403

V23257

READ DETECTOR (DFC 403)
Timing Diagram

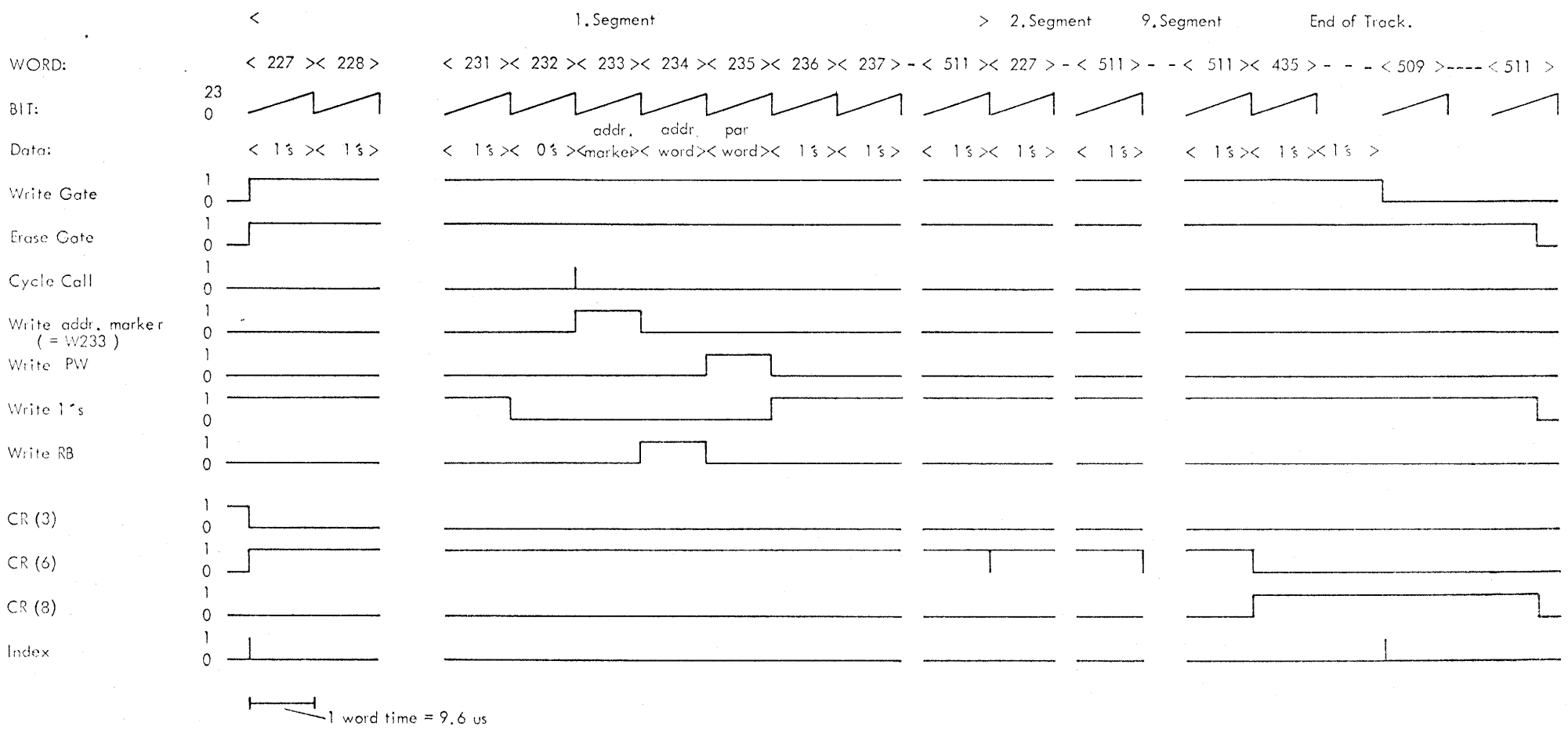


1) RdCl, ClRd, DaRd are output of the Readdetector

2) This trailing edge of OSDa does not set RdCl FF due to Lock = 0

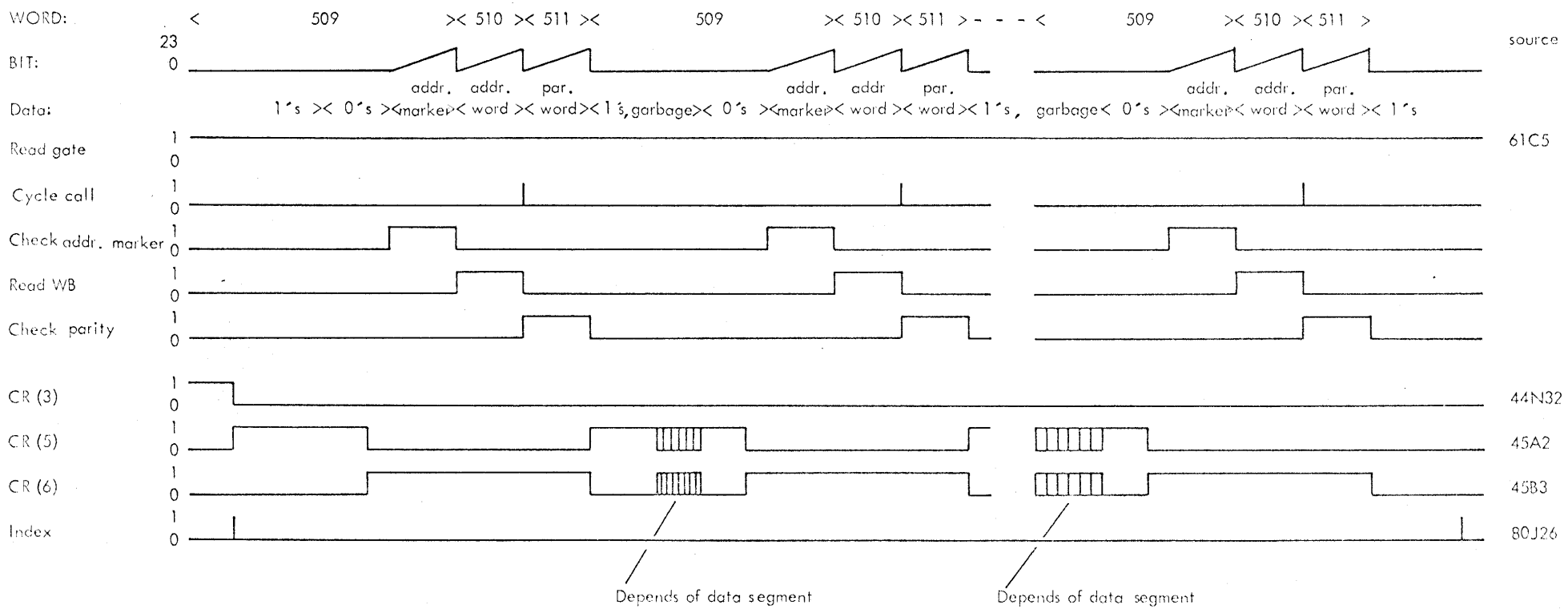
3) - - - - - sets RdCl FF due to Lock = 1.

1. Write Segment Addresses.



WRITE SEGMENT ADDRESSES
Timing Diagram

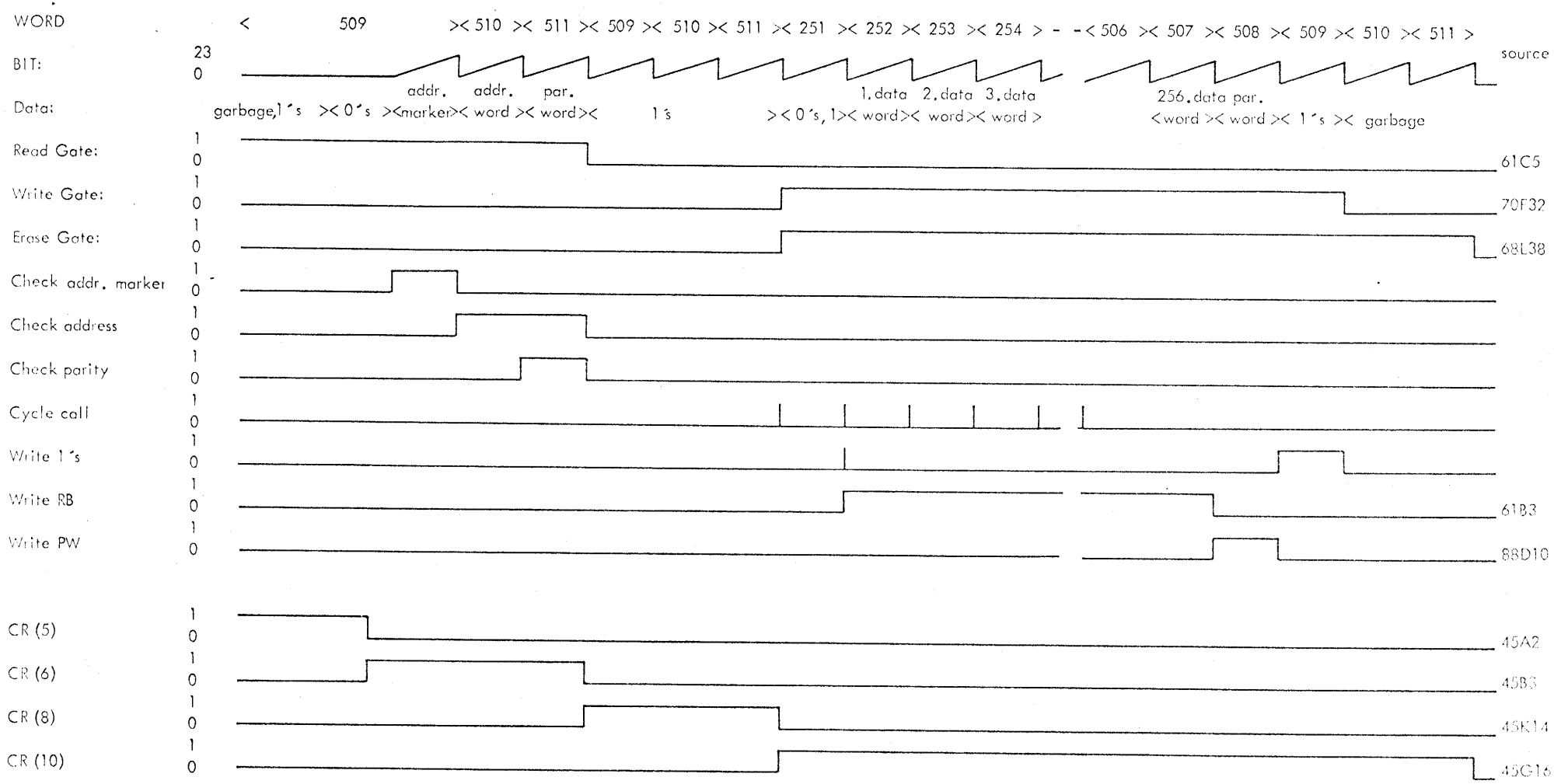
2. Read Segment Addresses.



READ SEGMENT ADDRESSES
Timming Diagram

RC4000
V13475

3. Write data



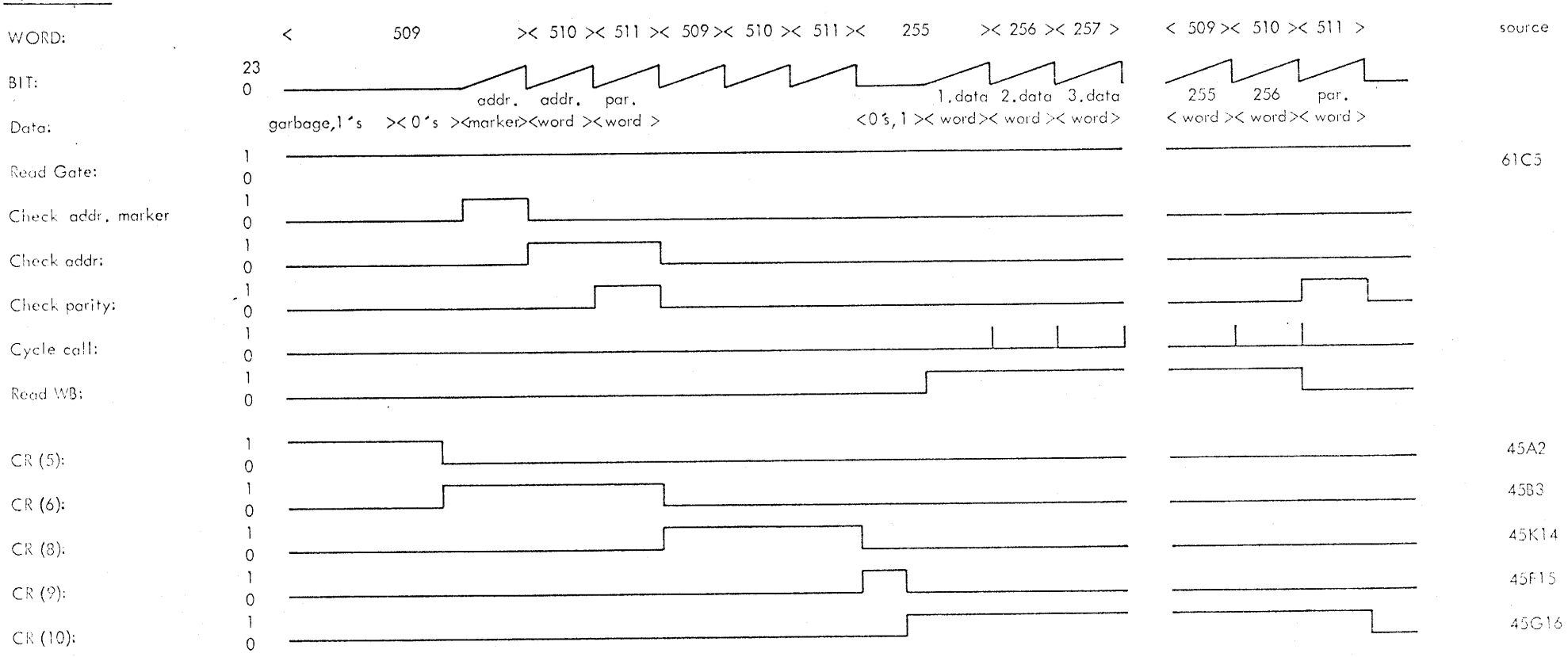
WRITE DATA
Timing Diagram

DFC403

RC4000

V1347G

4. Read data



READ DATA
Timing Diagram

DEC403

DFC403

PCBA Positionlist

Position	PCBA
DFC005	RC2059-1
DFC010	RC0956-1
DFC011	RC0935-3
DFC012	RC0935-3
DFC013	RC3032-1
DFC014	RC0834-1
DFC015	RC0834-1
DFC016	RC0956-1
DFC017	RC0834-1
DFC018	RC0839-1
DFC019	RC0901-1
DFC020	RC0897-1
DFC021	RC0897-1
DFC022	RC0897-1
DFC023	RC0897-1
DFC024	RC0897-1
DFC025	RC3032-1
DFC026	RC0839-1
DFC027	RC0838-1
DFC028	RC0847-1
DFC029	RC0839-1
DFC030	RC0935-3
DFC031	RC0935-3
DFC032	RC0898-1
DFC033	RC0898-1
DFC034	RC0898-1
DFC035	RC0898-1
DFC036	RC0898-1
DFC037	RC0898-1
DFC038	RC0935-3
DFC039	RC0935-3
DFC040	RC0935-3
DFC041	RC0935-3
DFC042	RC0935-3
DFC043	RC0935-3
DFC044	RC0935-3
DFC045	RC0935-3
DFC046	RC0935-1

V23273

150373 Rev1, 080972MOGK

Position	PCBA
DFC047	RC0935-1
DFC048	RC0935-1
DFC049	RC0935-1
DFC050	RC0935-1
DFC051	RC0935-1
DFC052	RC0935-1
DFC053	RC0839-1
DFC054	RC0839-1
DFC055	RC0834-1
DFC056	RC0956-1
DFC057	RC0834-1
DFC058	RC0838-1
DFC059	RC2060-1
DFC060	RC0835-1
DFC061	RC0956-1
DFC062	RC2060-1
DFC063	RC0847-1
DFC064	RC0956-1
DFC065	RC0858-1
DFC066	RC0956-1
DFC067	RC0834-1
DFC068	RC0834-1
DFC069	RC2060-1
DFC070	RC0839-1
DFC071	RC0956-1
DFC072	RC0839-1
DFC073	RC3032-1
DFC074	RC3032-1
DFC075	RC0834-1
DFC076	RC0835-1
DFC077	RC0957-1
DFC078	RC0995-1
DFC079	RC2056-1
DFC080	RC2056-1
DFC081	RC2056-1
DFC082	RC2057-1
DFC083	RC2057-1
DFC084	RC2057-1
DFC087	RC0888-1/1
DFC088	RC3032-1
DFC089	RC0847-1
DFC090	RC0836-1

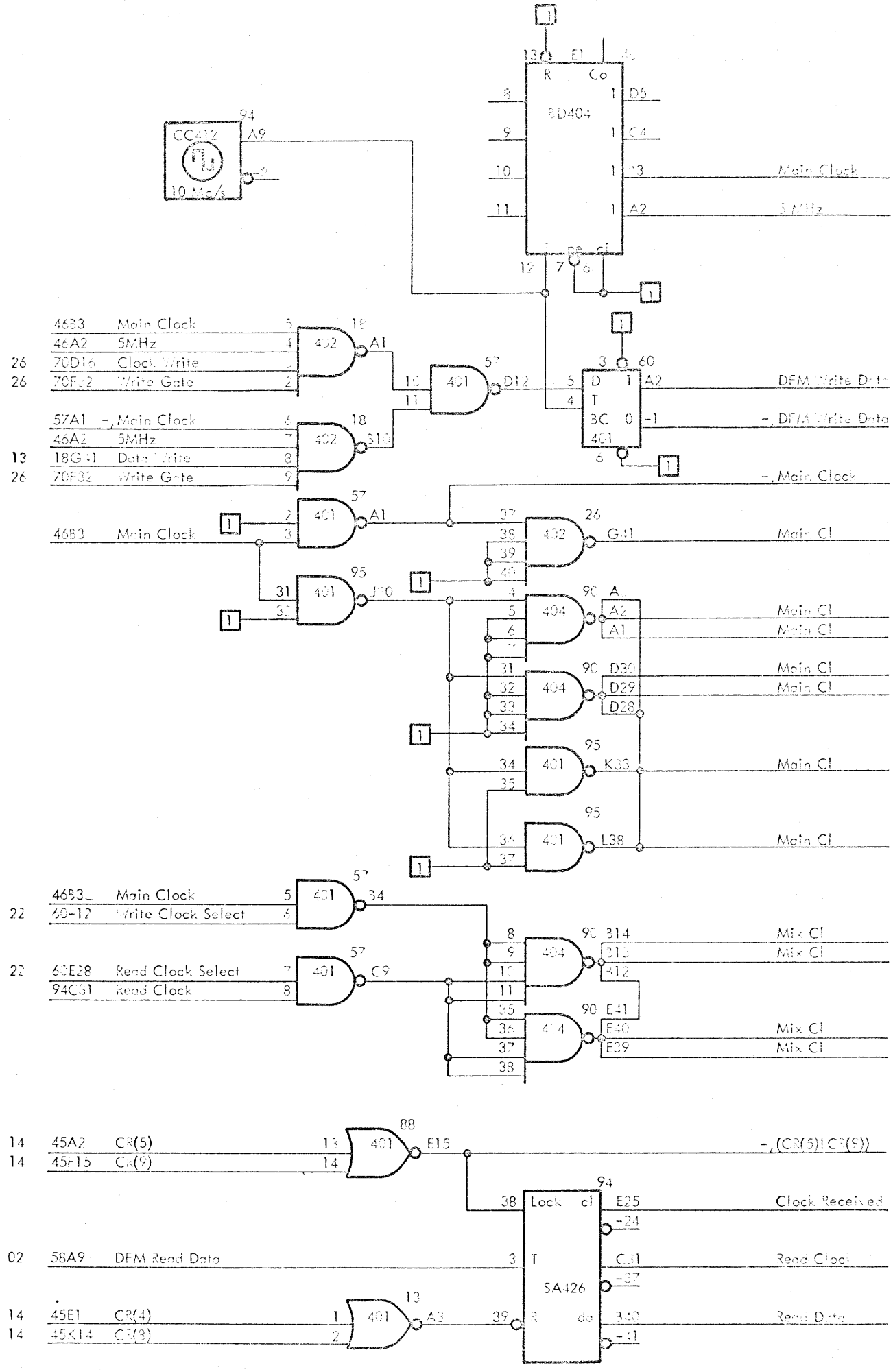
V23294

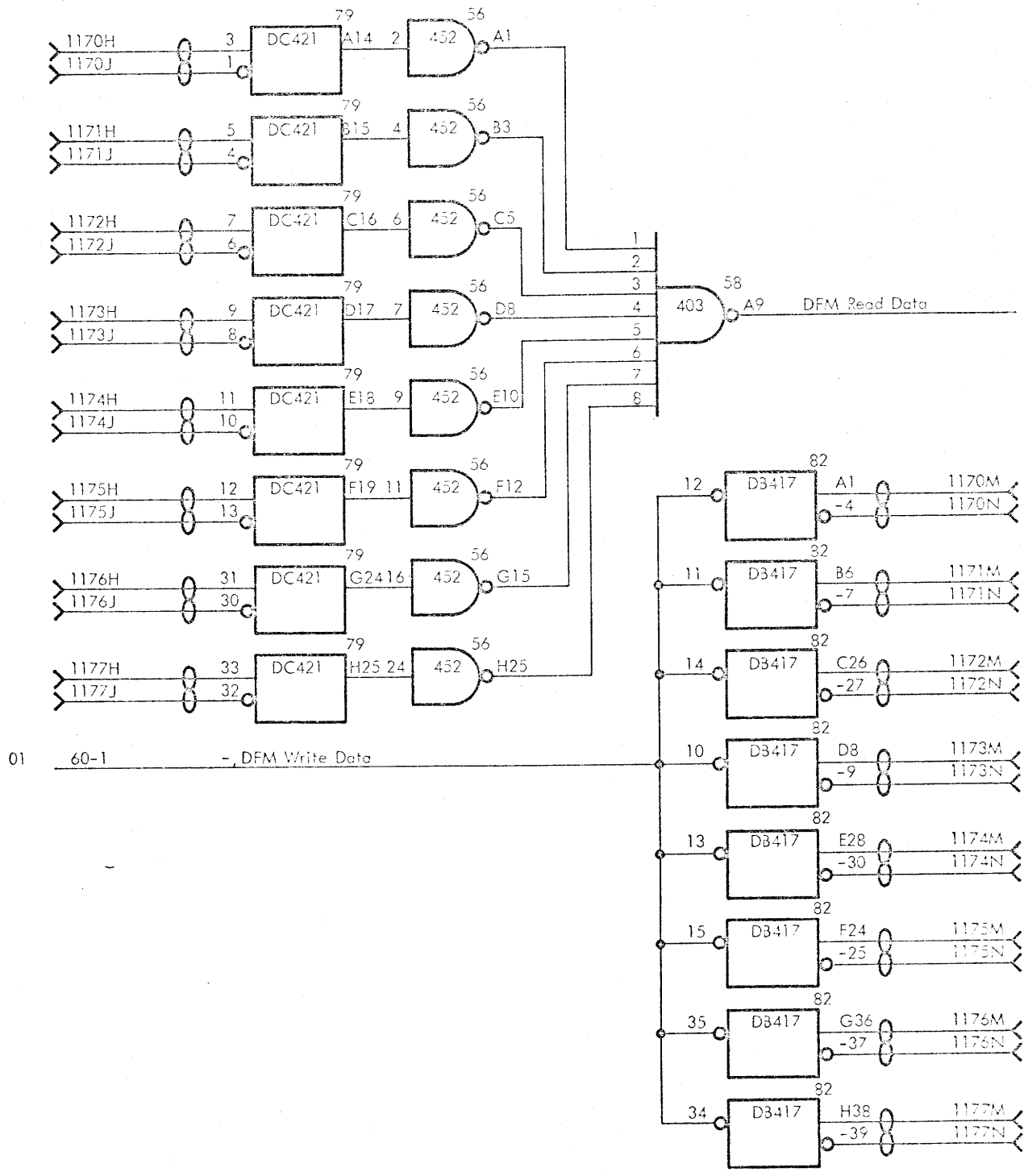
150373 Mat 080972MOGK

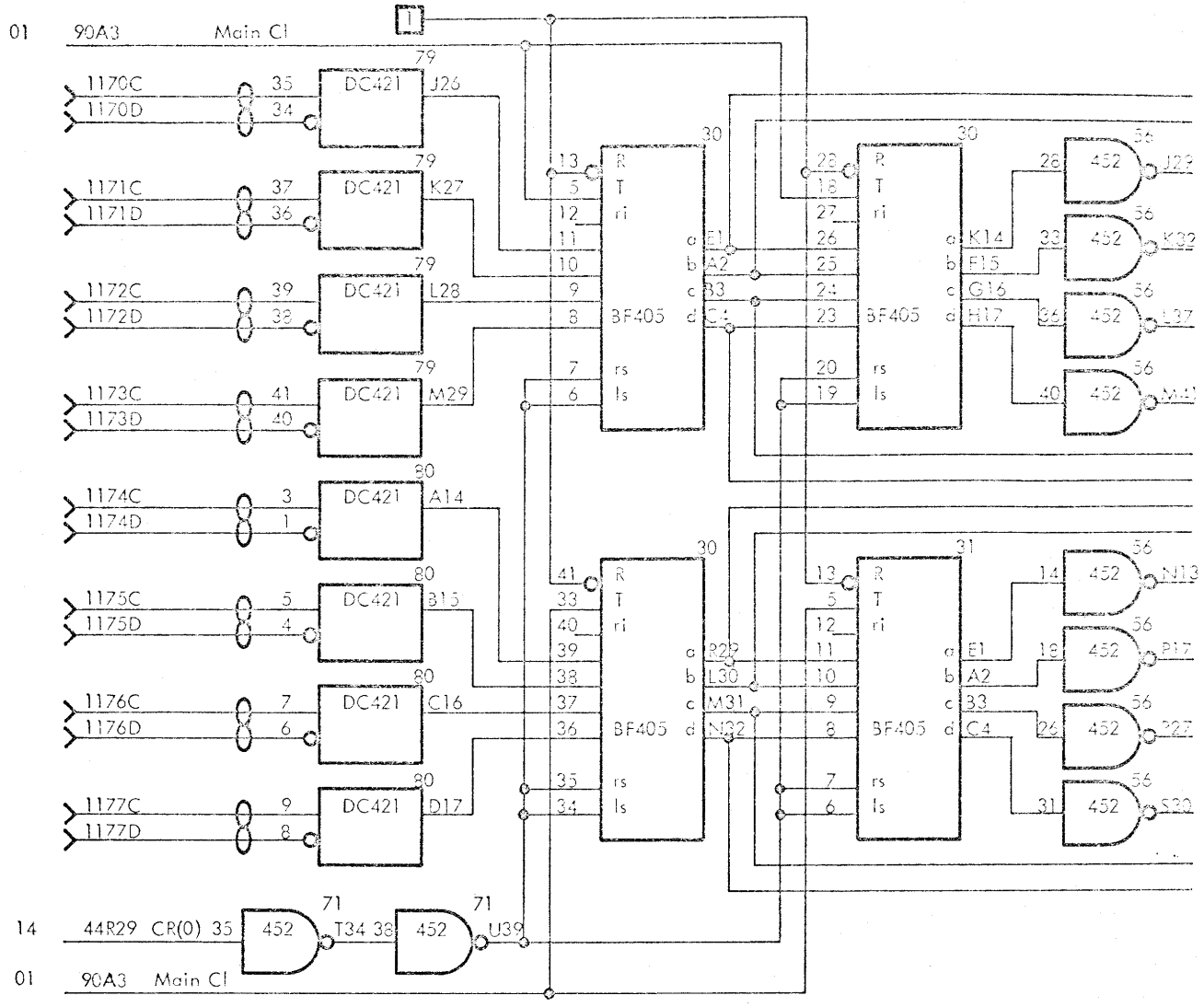
Position	PCBA
DFC091	RC0890-1
DFC092	RC2060-1
DFC093	RC0894-1
DFC094	RC2074-1
DFC095	RC0834-1
DFC096	RC0835-1
DFC097	RC0834-1
DFC099	RC0957-1
DFC100	RC0858-1

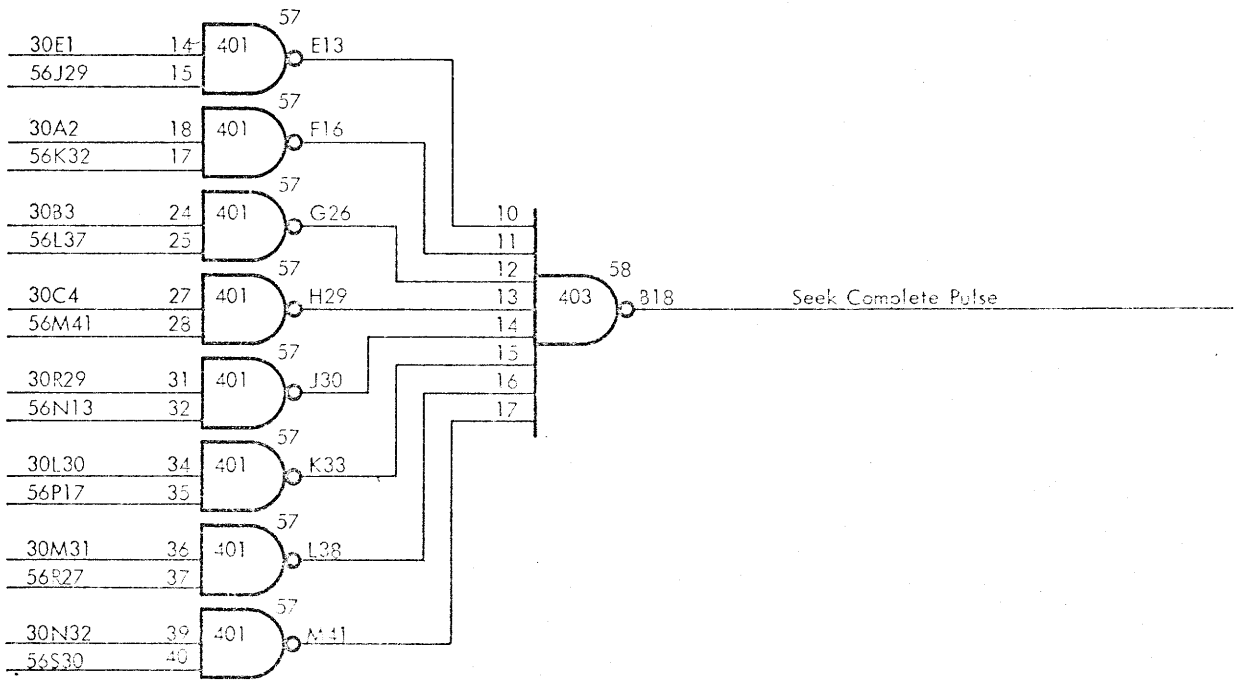
V23421

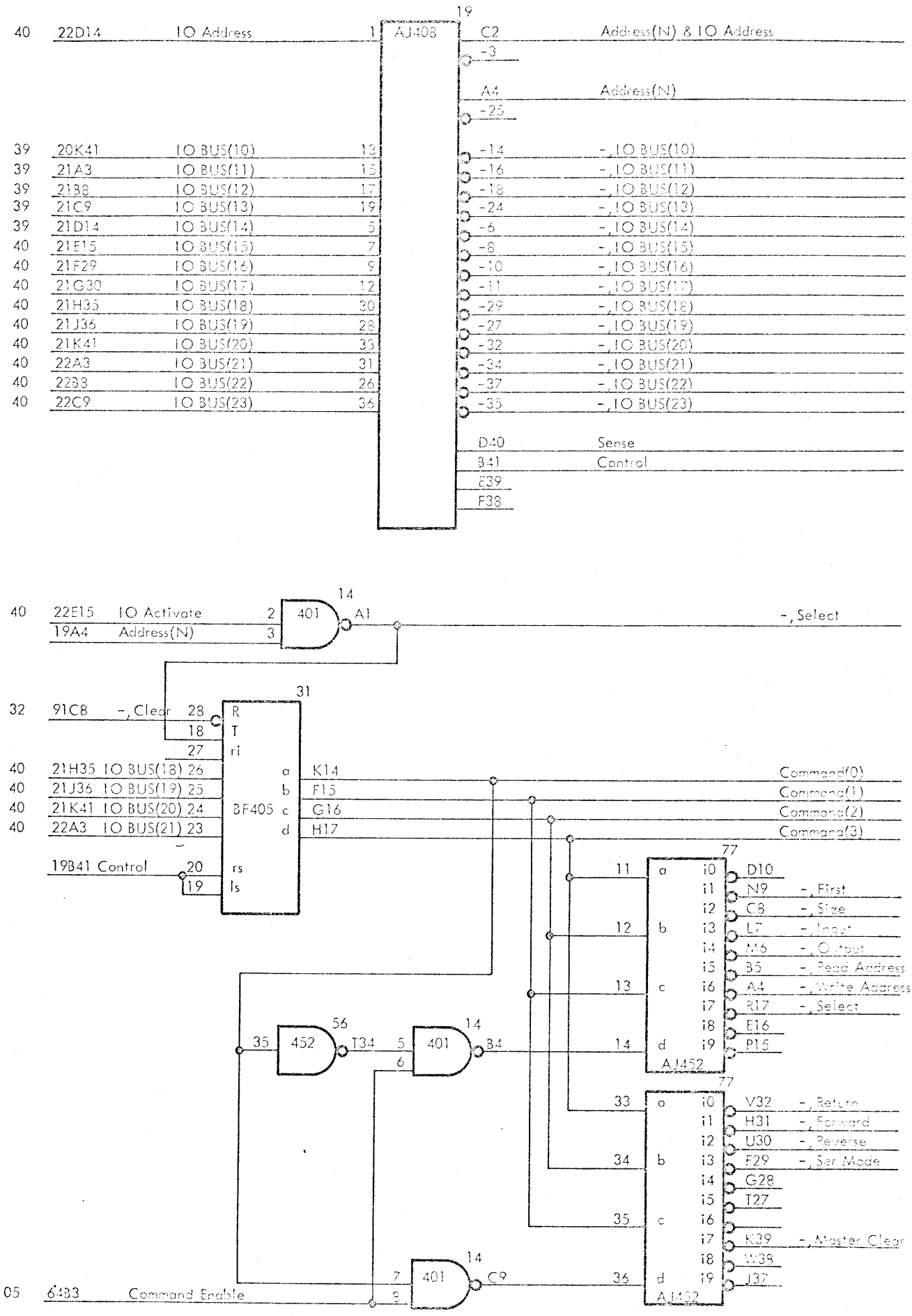
040573 MOJ 080972MOGK

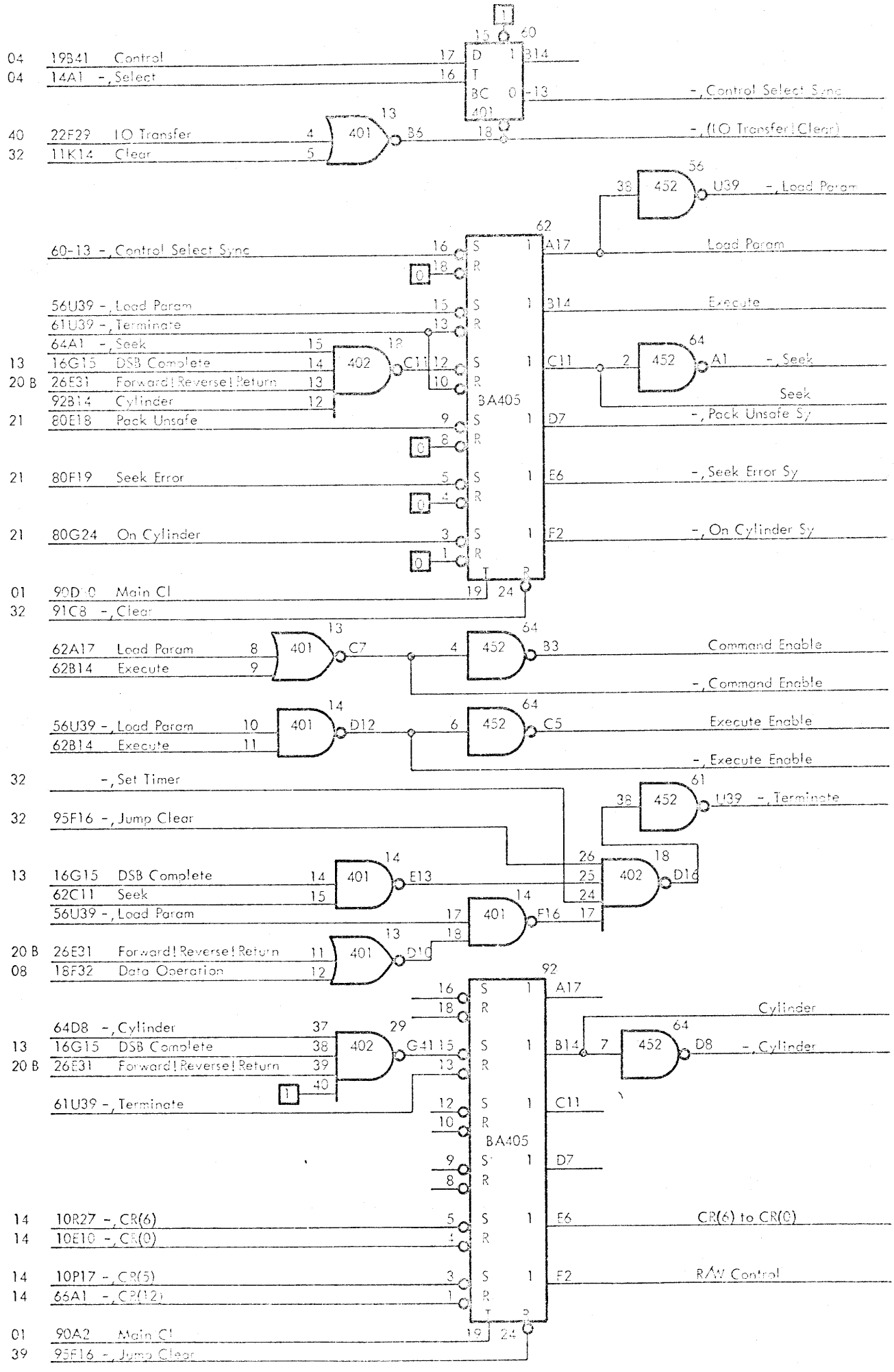

CC412
10 Mc/s
94
A9
8D404
Main Clock
5MHz
4683 Main Clock
46A2 5MHz
26 70D16 Clock Write
26 70F32 Write Gate
402
401
D12
DFM Write Data
57A1 -, Main Clock
46A2 5MHz
13 18G41 Data Write
26 70F32 Write Gate
-, DFM Write Data
-, Main Clock
4683 Main Clock
Main Cl
404
A2
A1
D30
D29
D28
95
K38
L38
4683_ Main Clock
22 60-17 Write Clock Select
22 60E28 Read Clock Select
94C31 Read Clock
C9
B14
B13
B12
E41
E40
E39
Mix Cl
14 45A2 CR(5)
14 45F15 CR(9)
88
E15
-,(CR(5)!CR(9))
Lock
SA426
E25
Clock Received
02 58A9 DFM Read Data
C31
Read Clock
14 45E1 CR(4)
14 45K14 CR(3)
A3
B30
Read Data


1170H
1170J
3
1
DC421
79
A14 2
452
56
A1
1171H
1171J
5
4
DC421
79
B15 4
452
56
B3
1172H
1172J
7
6
DC421
79
C16 6
452
56
C5
1173H
1173J
9
8
DC421
79
D17 7
452
56
D8
1174H
1174J
11
10
DC421
79
E18 9
452
56
E10
1175H
1175J
12
13
DC421
79
F19 11
452
56
F12
1176H
1176J
31
30
DC421
79
G2416
452
56
G15
1177H
1177J
33
32
DC421
79
H25 24
452
56
H25
1
2
3
4
5
6
7
8
403
58
A9
DFM Read Data
01
60-1
-, DFM Write Data
12
11
14
10
13
15
35
34
D3417
82
A1
-4
1170M
1170N
B6
-7
1171M
1171N
C26
-27
1172M
1172N
D8
-9
1173M
1173N
E28
-30
1174M
1174N
F24
-25
1175M
1175N
G36
-37
1176M
1176N
H38
-39
1177M
1177N


01 90A3 Main CI
1170C
1170D
1171C
1171D
1172C
1172D
1173C
1173D
1174C
1174D
1175C
1175D
1176C
1176D
1177C
1177D
DC421
J26
K27
L28
M29
A14
B15
C16
D17
BF405
452
J29
K32
L37
M41
N13
P17
R27
S30
44R29 CR(0)
T34
U39
14
01 90A3 Main CI


30E1
56J29
30A2
56K32
30B3
56L37
30C4
56M41
30R29
56N13
30L30
56P17
30M31
56R27
30N32
56S30
401
E13
F16
G26
H29
J30
K33
L38
M41
403
B18
Seek Complete Pulse


40 22D14 IO Address 1
AJ408 19
C2 Address(N) & IO Address
-3
A4 Address(N)
-25
39 20K41 IO BUS(10) 13 -14 -,IO BUS(10)
39 21A3 IO BUS(11) 15 -16 -,IO BUS(11)
39 21B8 IO BUS(12) 17 -18 -,IO BUS(12)
39 21C9 IO BUS(13) 19 -24 -,IO BUS(13)
39 21D14 IO BUS(14) 5 -6 -,IO BUS(14)
40 21E15 IO BUS(15) 7 -8 -,IO BUS(15)
40 21F29 IO BUS(16) 9 -10 -,IO BUS(16)
40 21G30 IO BUS(17) 12 -11 -,IO BUS(17)
40 21H35 IO BUS(18) 30 -29 -,IO BUS(18)
40 21J36 IO BUS(19) 28 -27 -,IO BUS(19)
40 21K41 IO BUS(20) 33 -32 -,IO BUS(20)
40 22A3 IO BUS(21) 31 -34 -,IO BUS(21)
40 22B8 IO BUS(22) 26 -37 -,IO BUS(22)
40 22C9 IO BUS(23) 36 -35 -,IO BUS(23)
D40 Sense
B41 Control
E39
F38
40 22E15 IO Activate 2
19A4 Address(N) 3
401 14 A1
-,Select
32 91C8 -,Clear 28
18
27
31
R
T
ri
40 21H35 IO BUS(18) 26 a K14 Command(0)
40 21J36 IO BUS(19) 25 b F15 Command(1)
40 21K41 IO BUS(20) 24 BF405 c G16 Command(2)
40 22A3 IO BUS(21) 23 d H17 Command(3)
19B41 Control 20 rs
19 ls
77
11 a i0 D10
i1 N9 -,First
i2 C8 -,Size
12 b i3 L7 -,Input
i4 M6 -,Output
i5 B5 -,Read Address
13 c i6 A4 -,Write Address
i7 R17 -,Select
i8 E16
14 d i9 P15
AJ452
56 452 35 T34 5 6
401 14 B4
77
33 a i0 V32 -,Return
i1 H31 -,Forward
i2 U30 -,Reverse
34 b i3 F29 -,Ser Mode
i4 G28
i5 T27
35 c i6
i7 K39 -,Master Clear
i8 W38
36 d i9 J37
AJ452
401 14 C9
7
9
05 6483 Command Enable



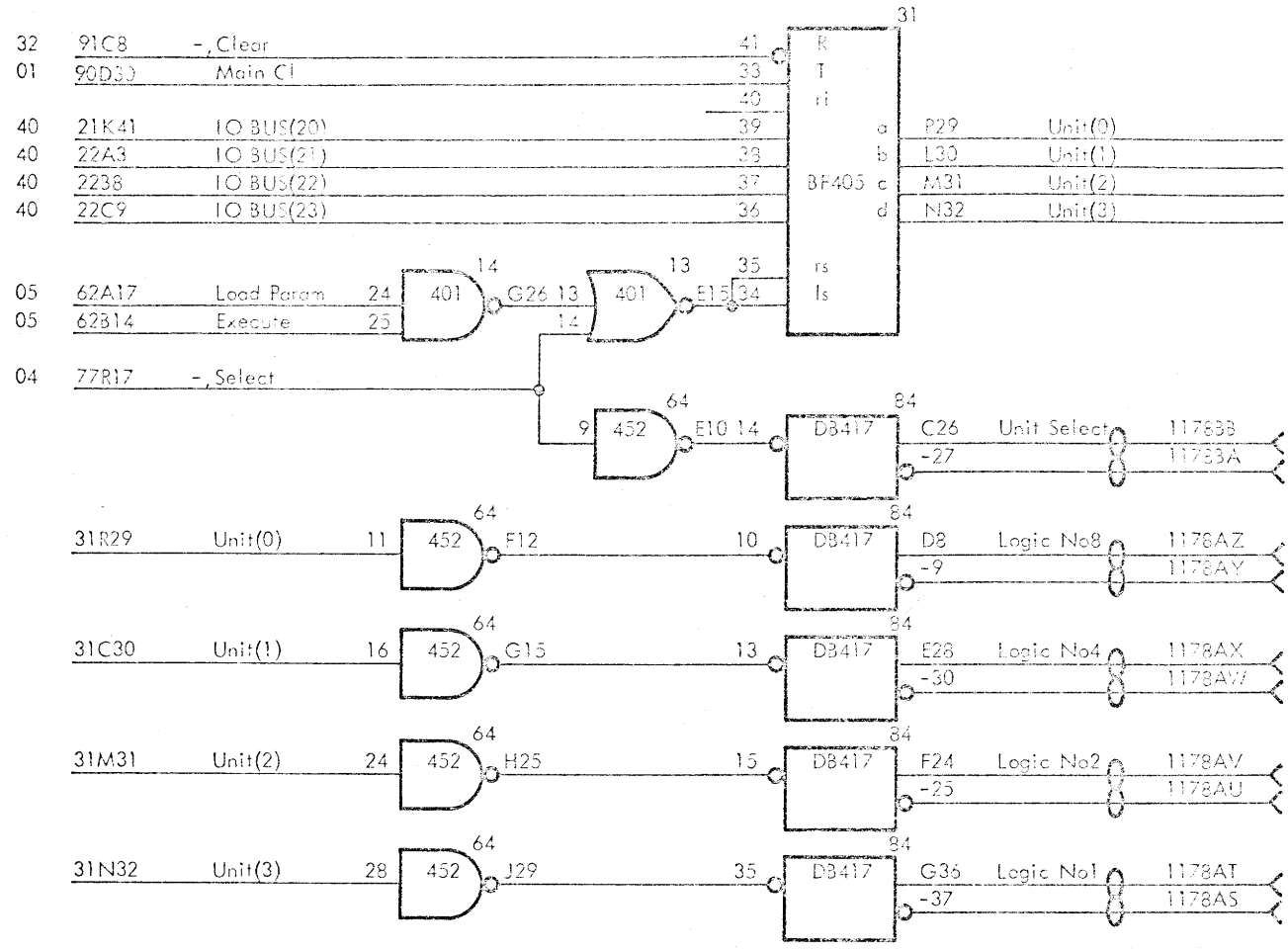
DFC403
RC4000

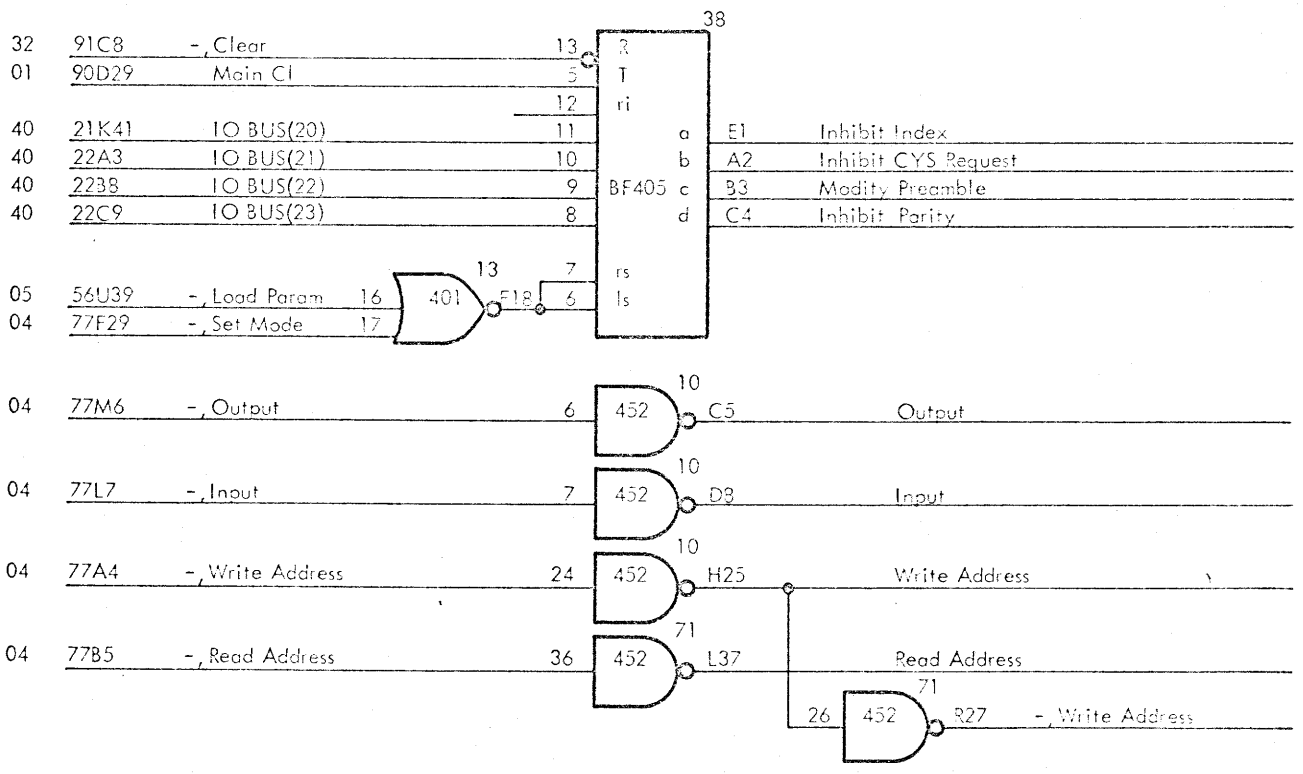
LOAD AND EXECUTE CONTROL

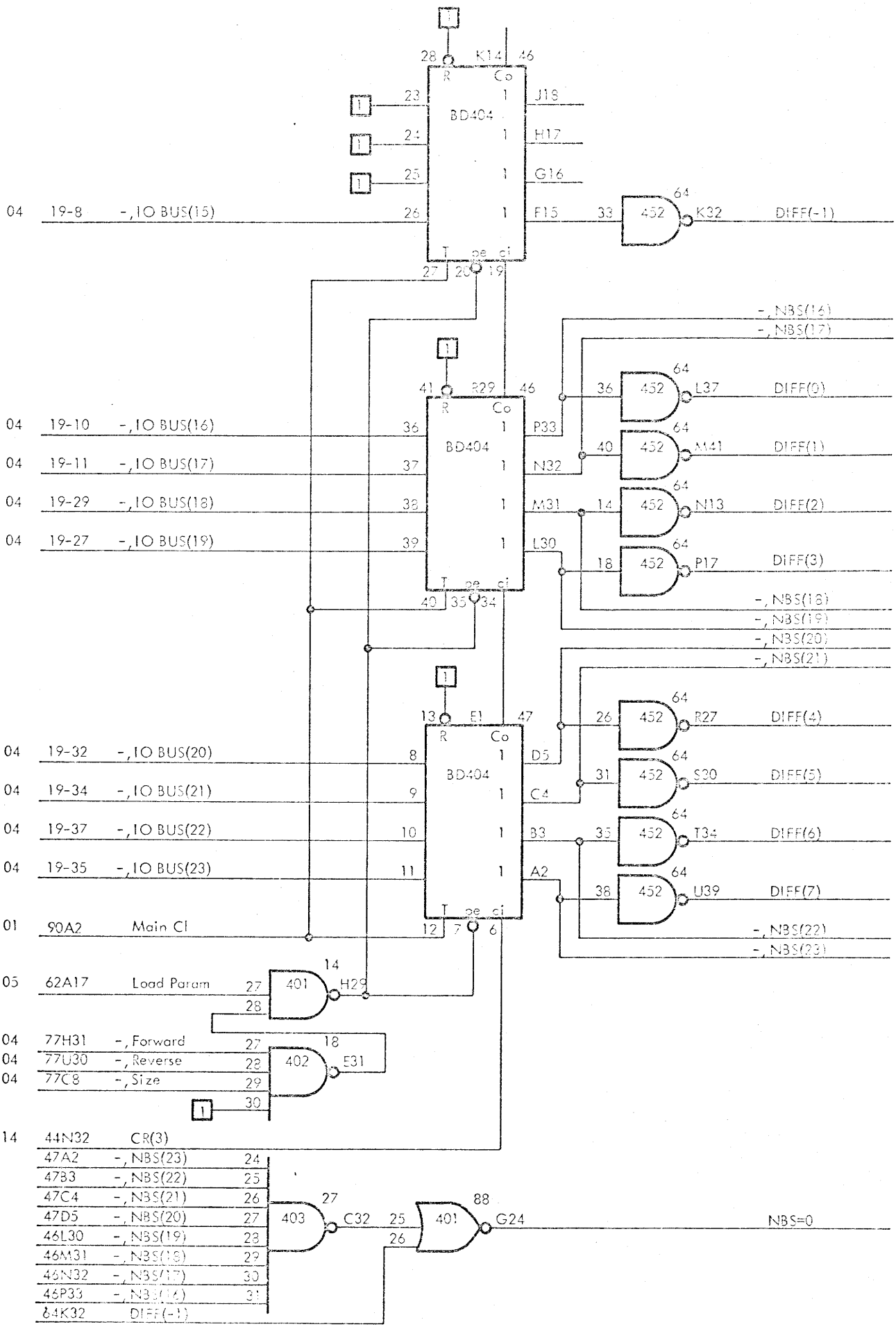
DFC05

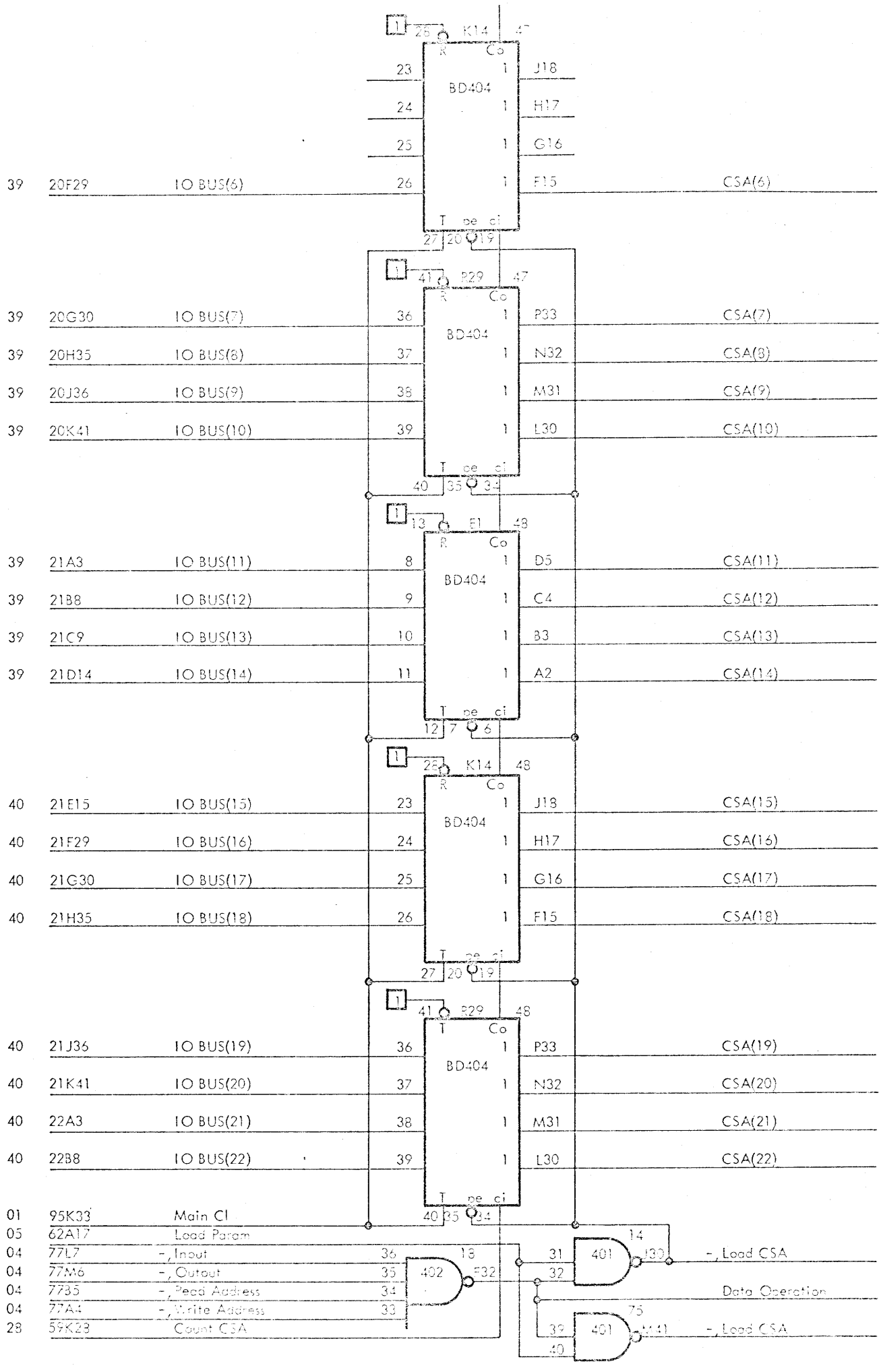
R 10533

Logic Diagram


32 91C8 -,Clear
01 90D30 Main CI
40 21K41 IO BUS(20)
40 22A3 IO BUS(21)
40 2238 IO BUS(22)
40 22C9 IO BUS(23)
05 62A17 Load Param
05 62B14 Execute
04 77R17 -,Select
31R29 Unit(0)
31C30 Unit(1)
31M31 Unit(2)
31N32 Unit(3)
BF405
401
452
D8417
P29 Unit(0)
L30 Unit(1)
M31 Unit(2)
N32 Unit(3)
C26 Unit Select
D8 Logic No8
E28 Logic No4
F24 Logic No2
G36 Logic No1
1178BB
1178BA
1178AZ
1178AY
1178AX
1178AW
1178AV
1178AU
1178AT
1178AS


32 91C8 -,Clear
01 90D29 Main CI
40 21K41 IO BUS(20)
40 22A3 IO BUS(21)
40 2238 IO BUS(22)
40 22C9 IO BUS(23)
05 56U39 -,Load Param
04 77F29 -,Set Mode
04 77M6 -,Output
04 77L7 -,Input
04 77A4 -,Write Address
04 77B5 -,Read Address
BF405
401
452
E1 Inhibit Index
A2 Inhibit CYS Request
B3 Modify Preamble
C4 Inhibit Parity
C5 Output
D8 Input
H25 Write Address
L37 Read Address
R27 -,Write Address


BD404
K14
J18
H17
G16
F15
452
K32
DIFF(-1)
L37
DIFF(0)
M41
DIFF(1)
N13
DIFF(2)
P17
DIFF(3)
R27
DIFF(4)
S30
DIFF(5)
T34
DIFF(6)
U39
DIFF(7)
04 19-8 -,IO BUS(15)
04 19-10 -,IO BUS(16)
04 19-11 -,IO BUS(17)
04 19-29 -,IO BUS(18)
04 19-27 -,IO BUS(19)
04 19-32 -,IO BUS(20)
04 19-34 -,IO BUS(21)
04 19-37 -,IO BUS(22)
04 19-35 -,IO BUS(23)
01 90A2 Main CI
05 62A17 Load Param
401
H29
04 77H31 -,Forward
04 77U30 -,Reverse
04 77C8 -,Size
402
E31
14 44N32 CR(3)
47A2 -,NBS(23)
47B3 -,NBS(22)
47C4 -,NBS(21)
47D5 -,NBS(20)
46L30 -,NBS(19)
46M31 -,NBS(18)
46N32 -,NBS(17)
46P33 -,NBS(16)
84K32 DIFF(-1)
403
C32
401
G24
NBS=0
-,NBS(16)
-,NBS(17)
-,NBS(18)
-,NBS(19)
-,NBS(20)
-,NBS(21)
-,NBS(22)
-,NBS(23)



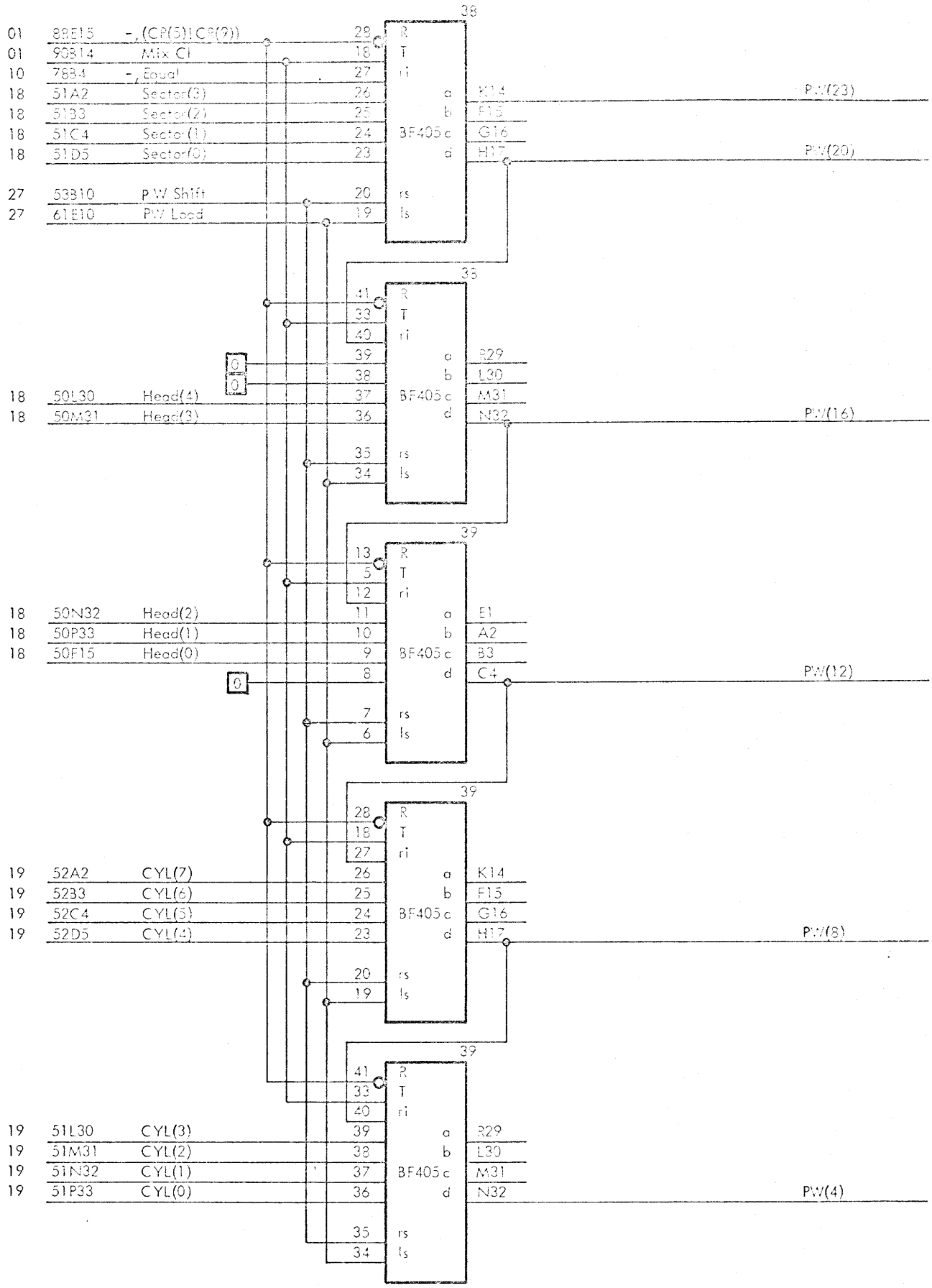
DFC403
RC4000

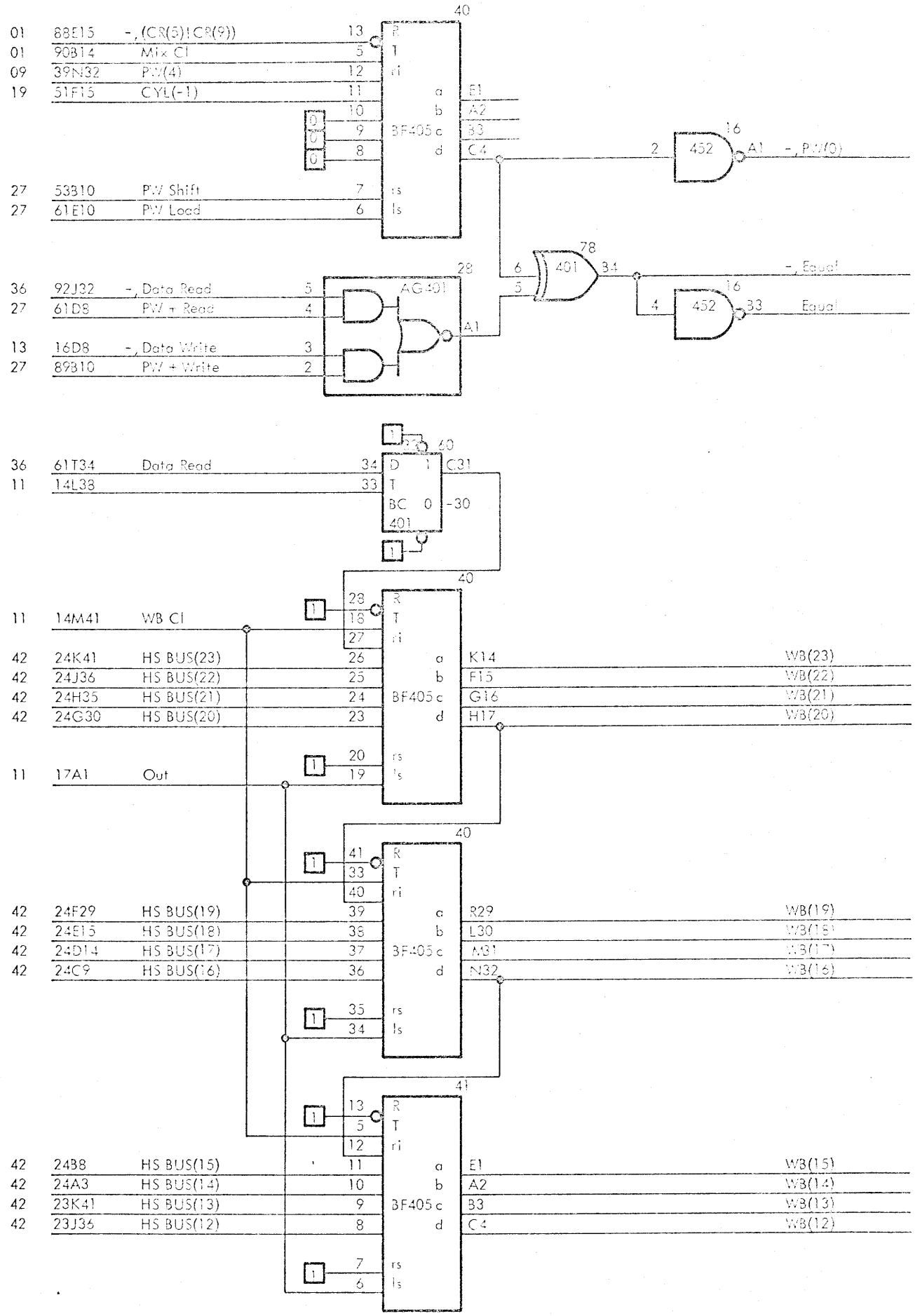
CORE STORAGE ADDRESS, CSA(4:22)

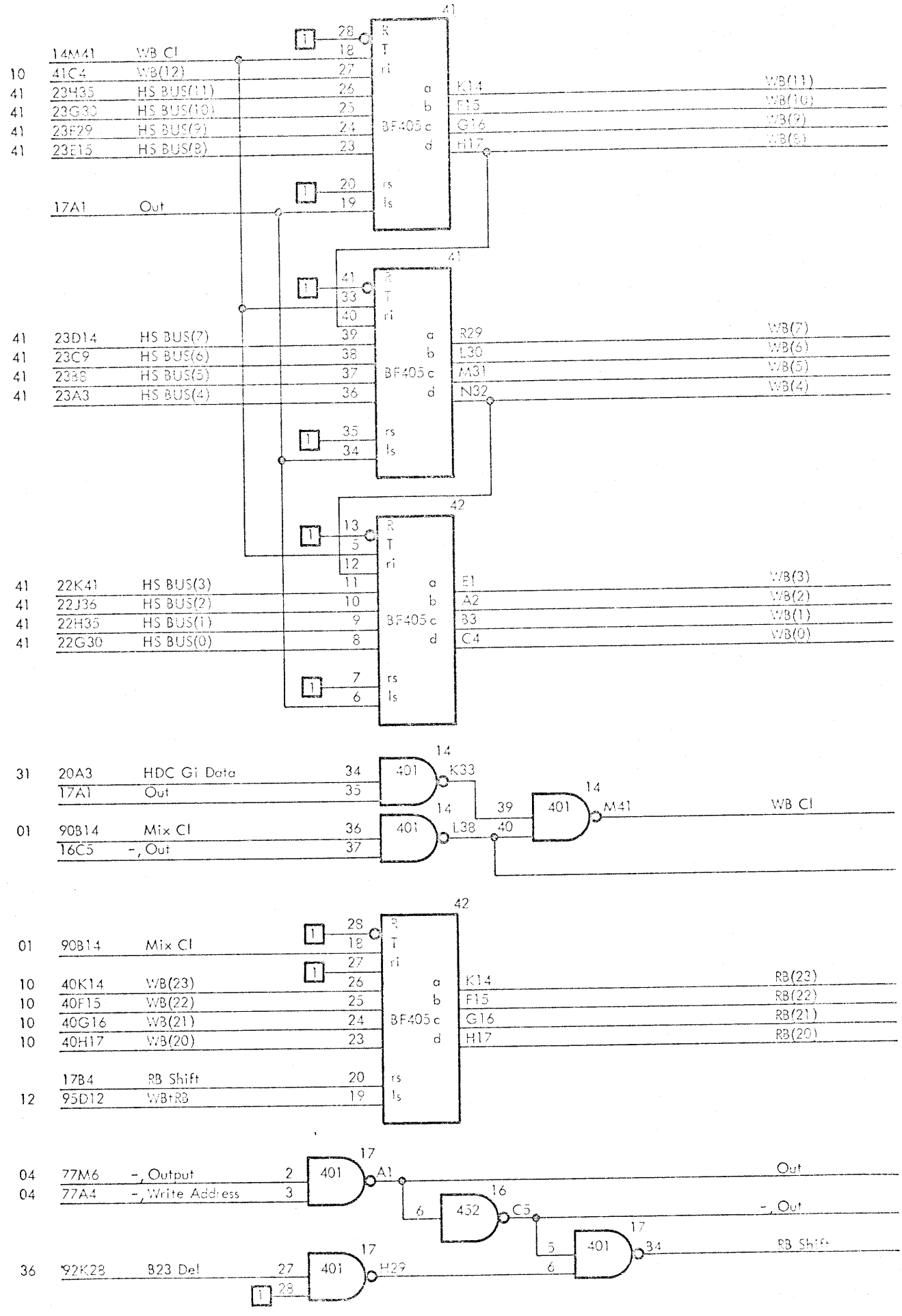
DFC08

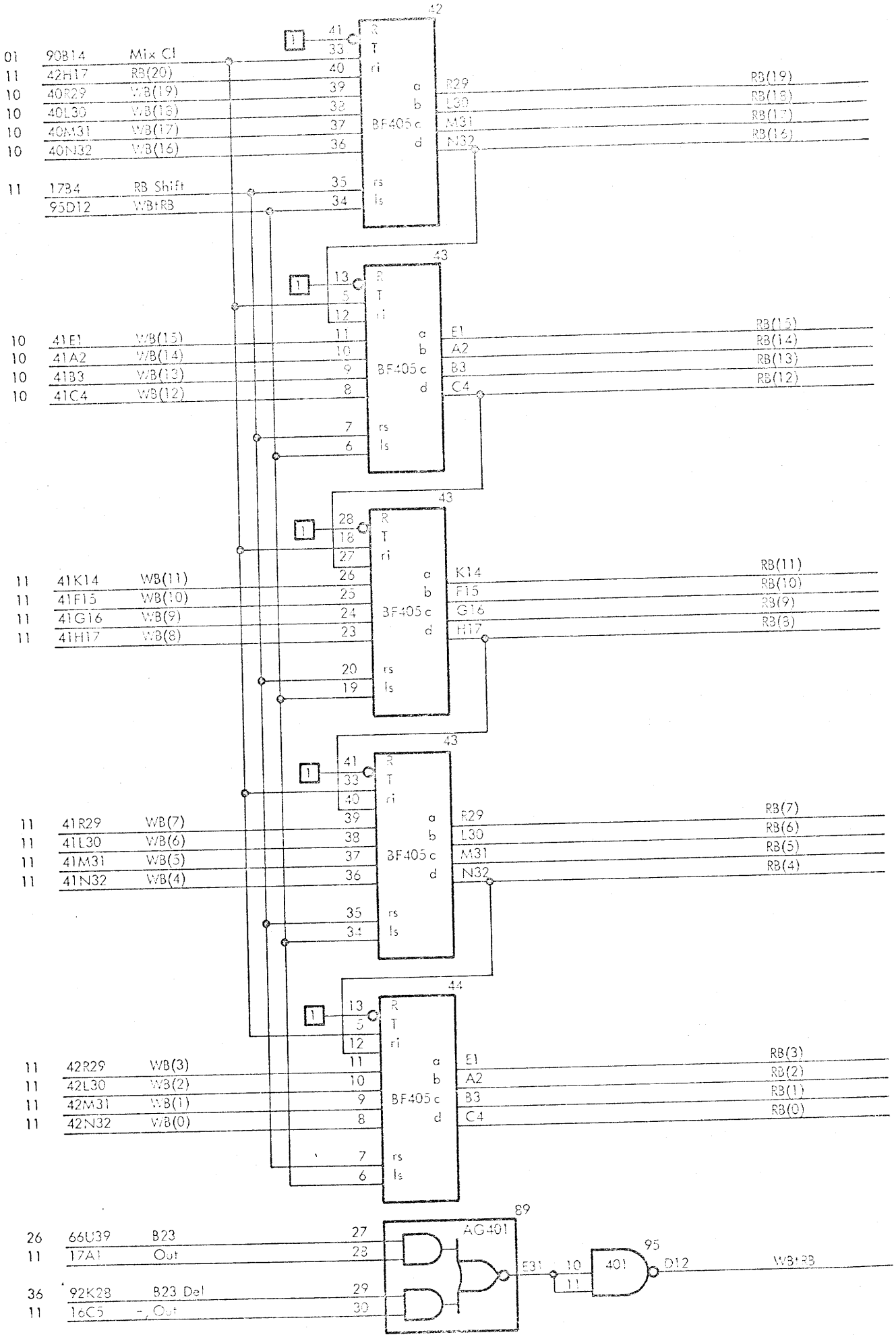
R 10536

Logic Diagram


38
01 88E15 -,(CP(5)!CP(9))
01 90B14 Mix CI
10 76B4 -,Equal
18 51A2 Sector(3)
18 51B3 Sector(2)
18 51C4 Sector(1)
18 51D5 Sector(0)
27 53B10 P.W Shift
27 61E10 PW Load
28 18 27 26 25 24 23 20 19
R T ri a b BF405 c d rs ls
K14 F15 G16 H17
PW(23)
PW(20)
35
41 33 40 39 38 37 36 35 34
R29 L30 M31 N32
0 0
18 50L30 Head(4)
18 50M31 Head(3)
PW(16)
39
13 5 12 11 10 9 8 7 6
E1 A2 B3 C4
18 50N32 Head(2)
18 50P33 Head(1)
18 50F15 Head(0)
0
PW(12)
39
28 18 27 26 25 24 23 20 19
19 52A2 CYL(7)
19 52B3 CYL(6)
19 52C4 CYL(5)
19 52D5 CYL(4)
PW(8)
39
41 33 40 39 38 37 36 35 34
19 51L30 CYL(3)
19 51M31 CYL(2)
19 51N32 CYL(1)
19 51P33 CYL(0)
PW(4)


01 88E15 -,(CR(5)!CR(9))
01 90B14 Mix CI
09 39N32 PW(4)
19 51F15 CYL(-1)
27 53B10 PW Shift
27 61E10 PW Load
36 92J32 -, Data Read
27 61D8 PW + Read
13 16D8 -, Data Write
27 89B10 PW + Write
36 61T34 Data Read
11 14L38
11 14M41 WB CI
11 17A1 Out
42 24K41 HS BUS(23)
42 24J36 HS BUS(22)
42 24H35 HS BUS(21)
42 24G30 HS BUS(20)
42 24F29 HS BUS(19)
42 24E15 HS BUS(18)
42 24D14 HS BUS(17)
42 24C9 HS BUS(16)
42 24B8 HS BUS(15)
42 24A3 HS BUS(14)
42 23K41 HS BUS(13)
42 23J36 HS BUS(12)
BF405
AG401
401
452
-30
-, PW(0)
-, Equal
Equal
WB(23)
WB(22)
WB(21)
WB(20)
WB(19)
WB(18)
WB(17)
WB(16)
WB(15)
WB(14)
WB(13)
WB(12)


14M41 WB CI
41C4 WB(12)
23H35 HS BUS(11)
23G30 HS BUS(10)
23F29 HS BUS(9)
23E15 HS BUS(8)
17A1 Out
BF405
K14 WB(11)
F15 WB(10)
G16 WB(9)
H17 WB(8)
23D14 HS BUS(7)
23C9 HS BUS(6)
23B8 HS BUS(5)
23A3 HS BUS(4)
R29 WB(7)
L30 WB(6)
M31 WB(5)
N32 WB(4)
22K41 HS BUS(3)
22J36 HS BUS(2)
22H35 HS BUS(1)
22G30 HS BUS(0)
E1 WB(3)
A2 WB(2)
B3 WB(1)
C4 WB(0)
20A3 HDC Gi Data
17A1 Out
401
K33
M41 WB CI
90B14 Mix CI
16C5 -, Out
L38
90B14 Mix CI
40K14 WB(23)
40F15 WB(22)
40G16 WB(21)
40H17 WB(20)
17B4 RB Shift
95D12 WB+RB
K14 RB(23)
F15 RB(22)
G16 RB(21)
H17 RB(20)
77M6 -, Output
77A4 -, Write Address
452
A1
C5
Out
-, Out
92K28 B23 Del
H29
RB Shift



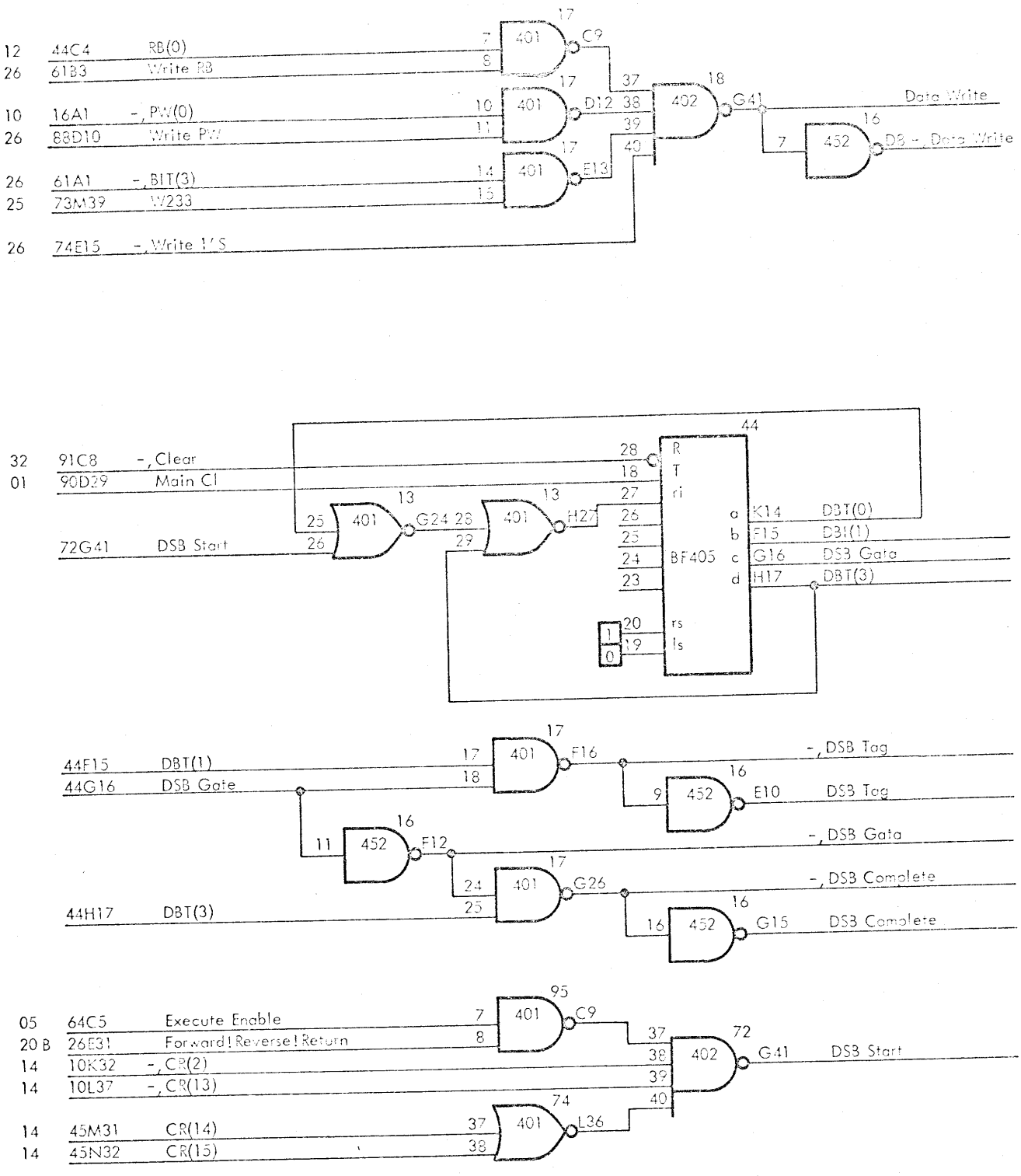
DFC 403
RC4000

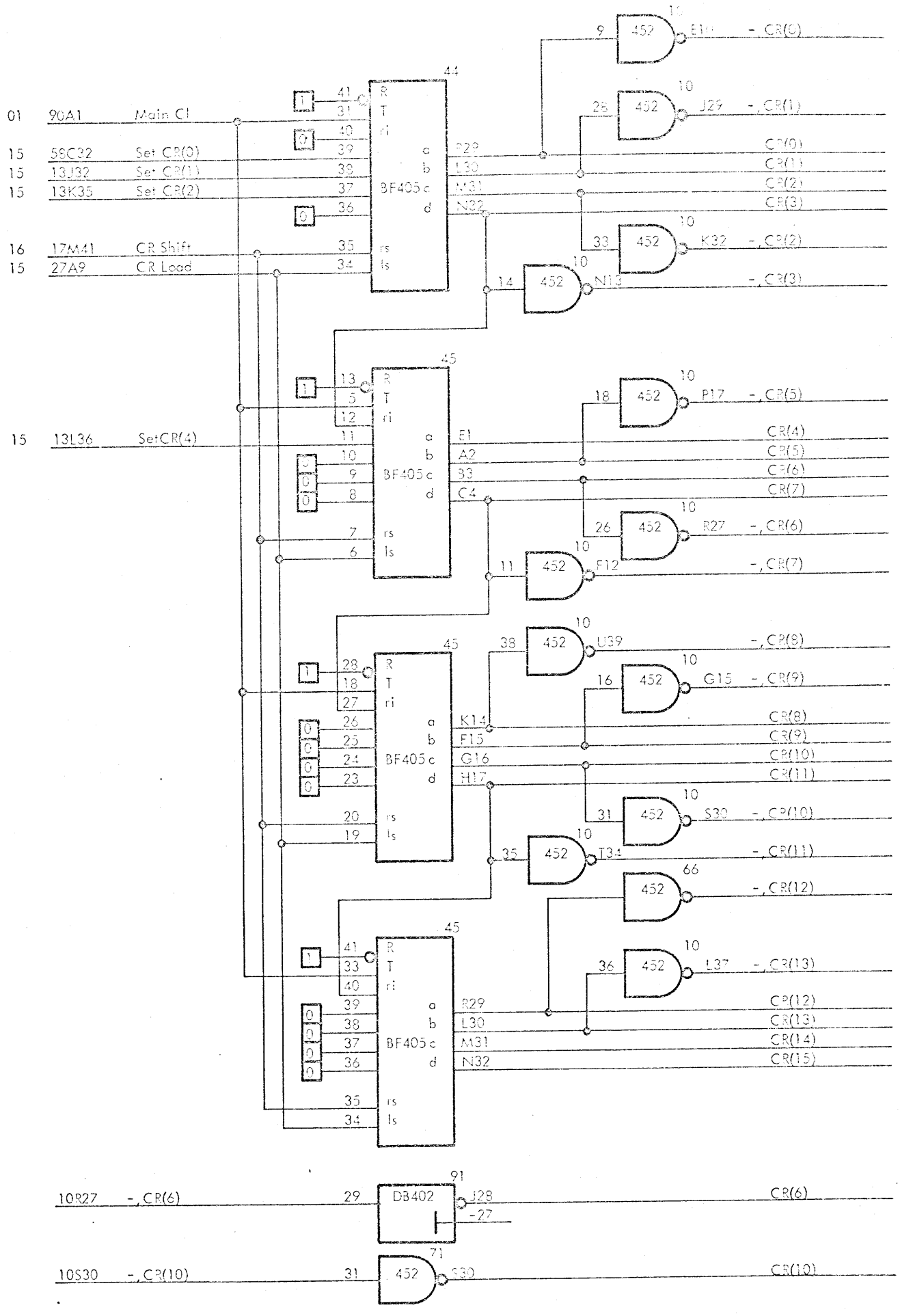
READ BUFFER, RB(0:19)

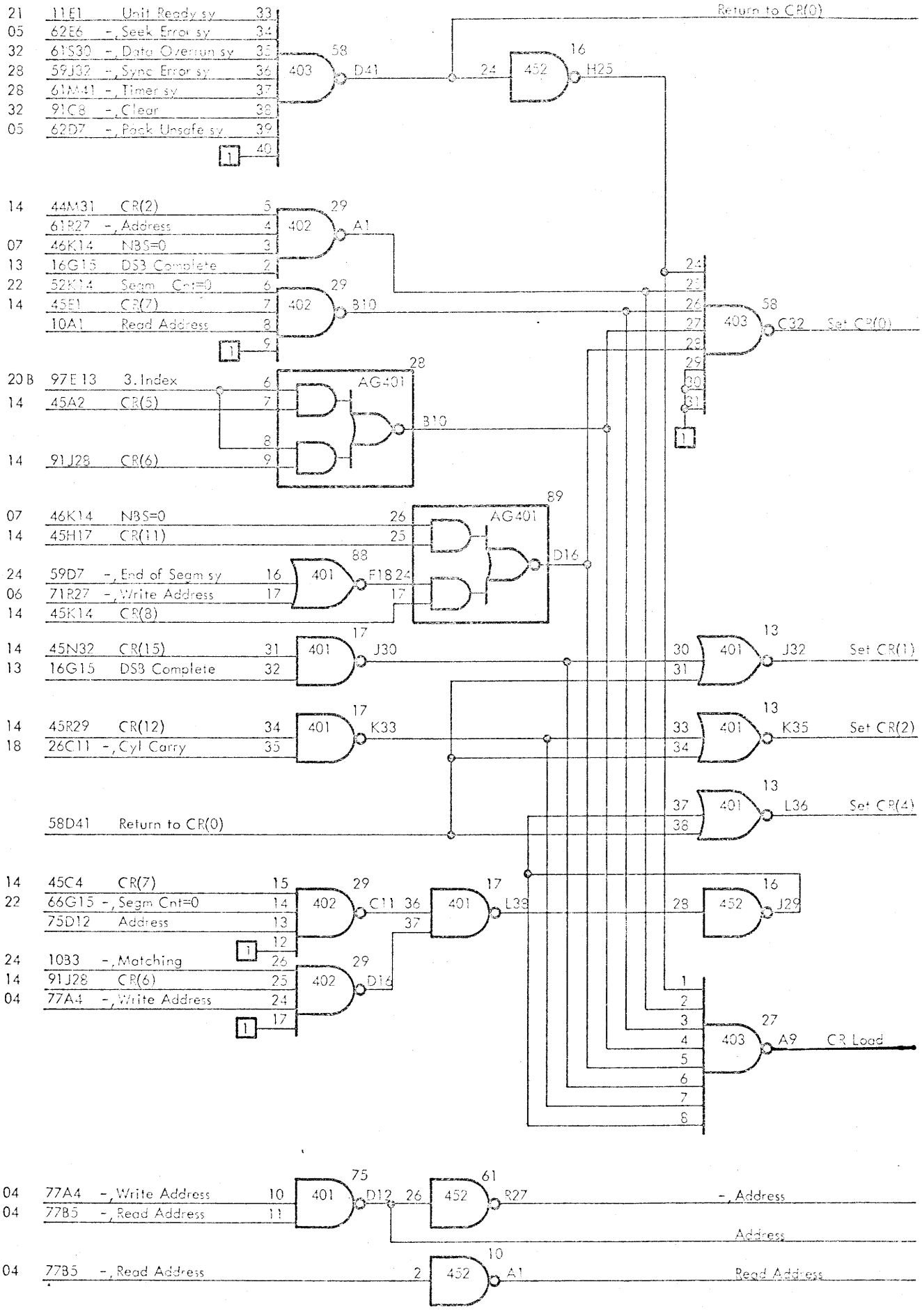
DFC12

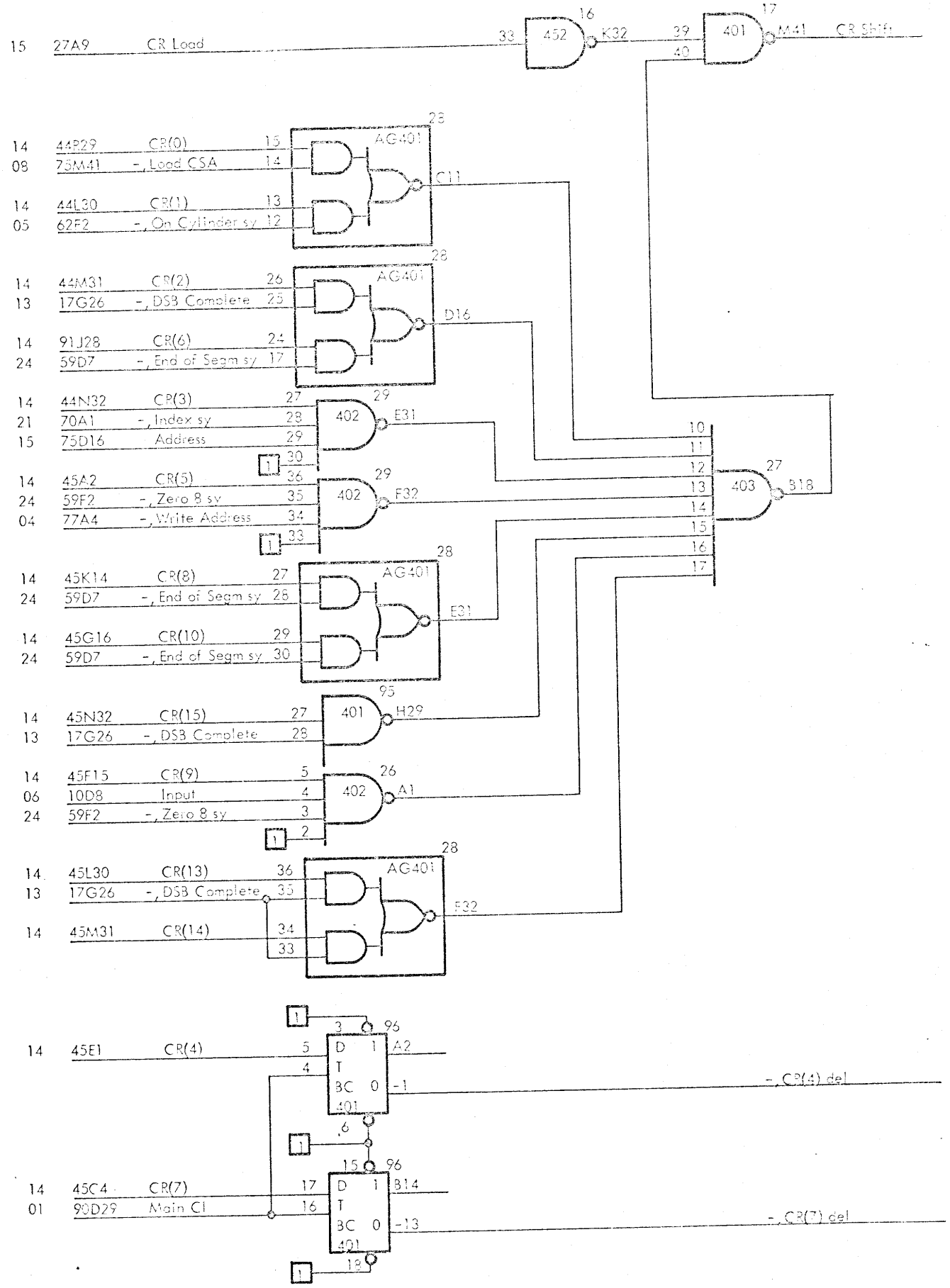
R 10540

Logic Diagram


12 44C4 RB(0)
26 61B3 Write RB
10 16A1 -, PW(0)
26 88D10 Write PW
26 61A1 -, BIT(3)
25 73M39 W233
26 74E15 -, Write 1's
401
C9
D12
E13
402
G41
Data Write
452
D8 - Data Write
32 91C8 -, Clear
01 90D29 Main CI
72G41 DSB Start
G24
H27
BF405
R
T
ri
rs
ls
K14 DBT(0)
F15 DBT(1)
G16 DSB Gate
H17 DBT(3)
44F15 DBT(1)
44G16 DSB Gate
44H17 DBT(3)
F16
E10
F12
G26
G15
-, DSB Tag
DSB Tag
-, DSB Gate
-, DSB Complete
DSB Complete
05 64C5 Execute Enable
20 B 26E31 Forward! Reverse! Return
14 10K32 -, CR(2)
14 10L37 -, CR(13)
14 45M31 CR(14)
14 45N32 CR(15)
L36
G41 DSB Start


01 90A1 Main Cl
15 58C32 Set CR(0)
15 13J32 Set CR(1)
15 13K35 Set CR(2)
16 17M41 CR Shift
15 27A9 CR Load
15 13L36 SetCR(4)
44
45
45
45
BF405
452
DB402
91
71
CR(0)
CR(1)
CR(2)
CR(3)
CR(4)
CR(5)
CR(6)
CR(7)
CR(8)
CR(9)
CR(10)
CR(11)
CR(12)
CR(13)
CR(14)
CR(15)
10R27 -,CR(6)
10S30 -,CR(10)


21 11E1 Unit Ready sy 33
05 62E6 -, Seek Error sy 34
32 61S30 -, Data Overrun sy 35
28 59J32 -, Sync Error sy 36
28 61M41 -, Timer sy 37
32 91C8 -, Clear 38
05 62D7 -, Pack Unsafe sy 39
40
58 403 D41
Return to CR(0)
24 452 16 H25
14 44M31 CR(2) 5
61R27 -, Address 4
07 46K14 NBS=0 3
13 16G15 DS3 Complete 2
22 52K14 Segm Cnt=0 6
14 45E1 CR(7) 7
10A1 Read Address 8
9
402 29 A1
402 29 B10
20B 97E13 3. Index 6
14 45A2 CR(5) 7
8
14 91J28 CR(6) 9
AG401 28 B10
24
25
26
27
28
29
30
31
58 403 C32 Set CR(0)
07 46K14 NBS=0 26
14 45H17 CR(11) 25
AG401 89 D16
24 59D7 -, End of Segm sy 16
06 71R27 -, Write Address 17
14 45K14 CR(8)
401 88 F18 24 17
14 45N32 CR(15) 31
13 16G15 DS3 Complete 32
401 17 J30
30
31
401 13 J32 Set CR(1)
14 45R29 CR(12) 34
18 26C11 -, Cyl Carry 35
401 17 K33
33
34
401 13 K35 Set CR(2)
37
38
401 13 L36 Set CR(4)
58D41 Return to CR(0)
14 45C4 CR(7) 15
22 66G15 -, Segm Cnt=0 14
75D12 Address 13
12
402 29 C11 36
37
401 17 L39
28
452 16 J29
24 1033 -, Matching 26
14 91J28 CR(6) 25
04 77A4 -, Write Address 24
17
402 29 D16
1
2
3
4
5
6
7
8
403 27 A9 CR Load
04 77A4 -, Write Address 10
04 77B5 -, Read Address 11
401 75 D12
26
452 61 R27
-, Address
Address
04 77B5 -, Read Address 2
452 10 A1
Read Address



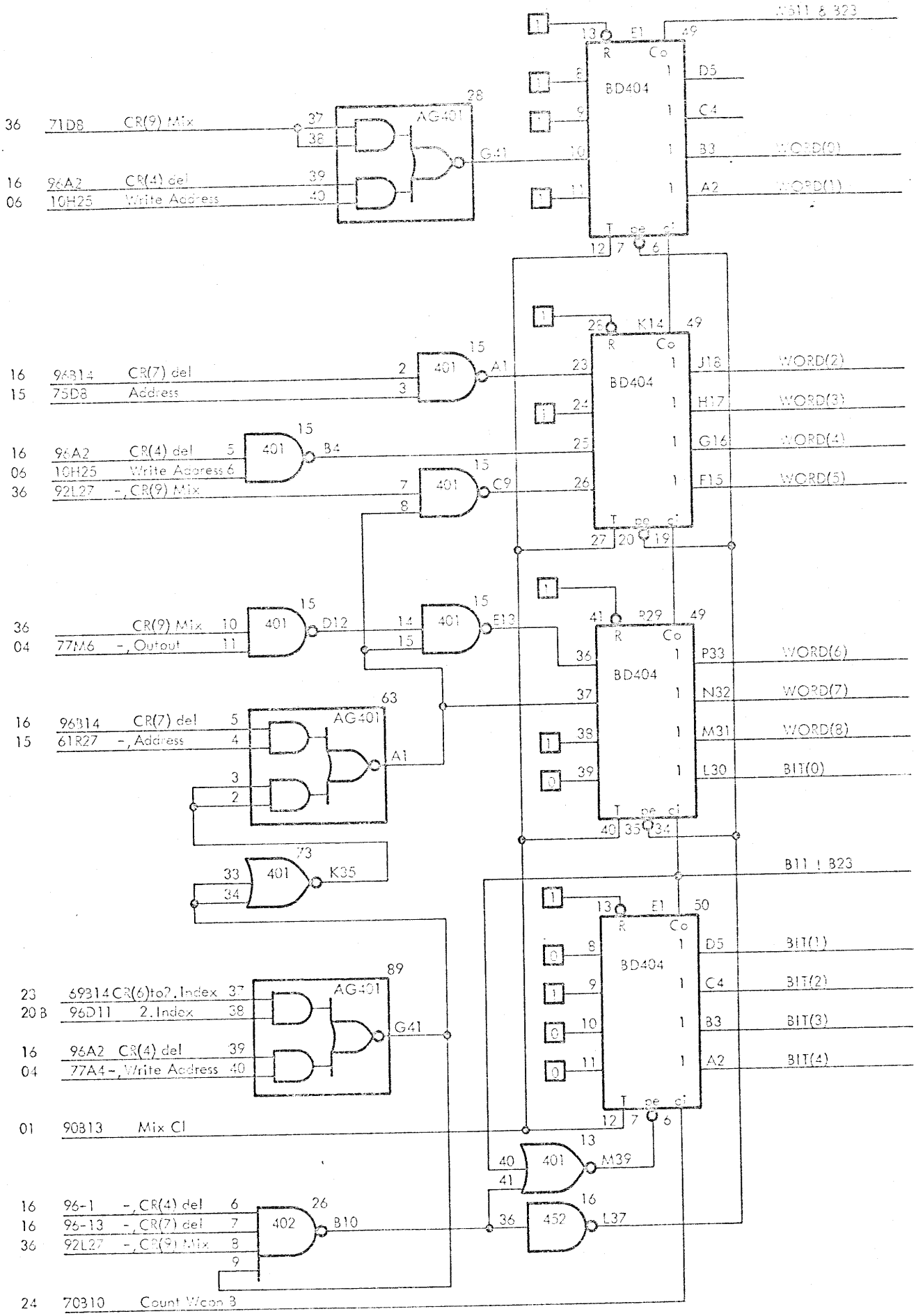
DFC403
RC4000

WAITING CONTROL

Logic Diagram

DFC16

R 10344



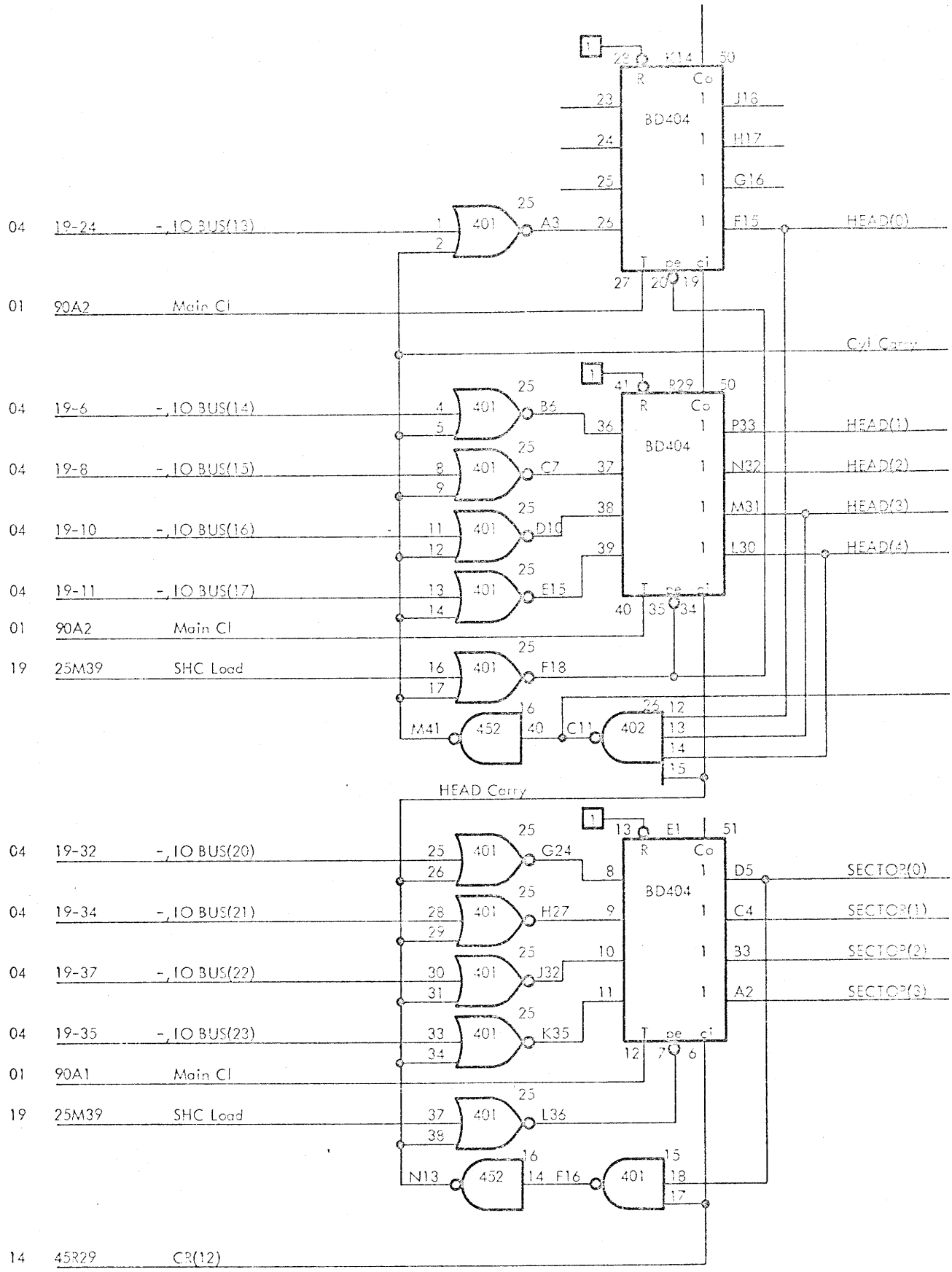
DFC 403
RC4000

WORD AND BIT COUNTER, WORD(0:8), BIT(0:4)

DFC17

R 10545

Logic Diagram



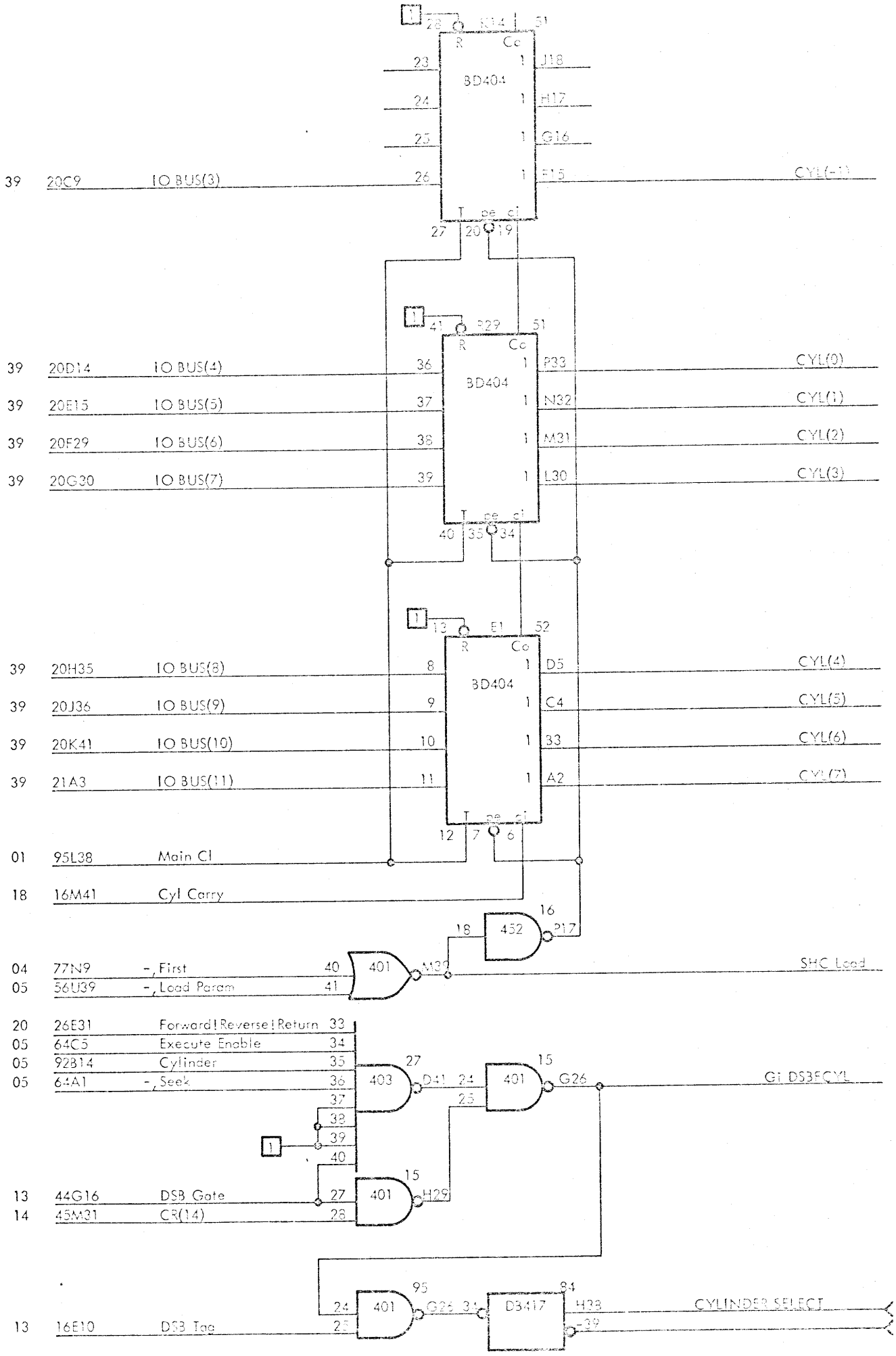
DFC 403
RC4000

SECTOR AND HEAD COUNTERS, SECTOR(0:3), HEAD(0:4)

DFC18

R 10546

Logic Diagram



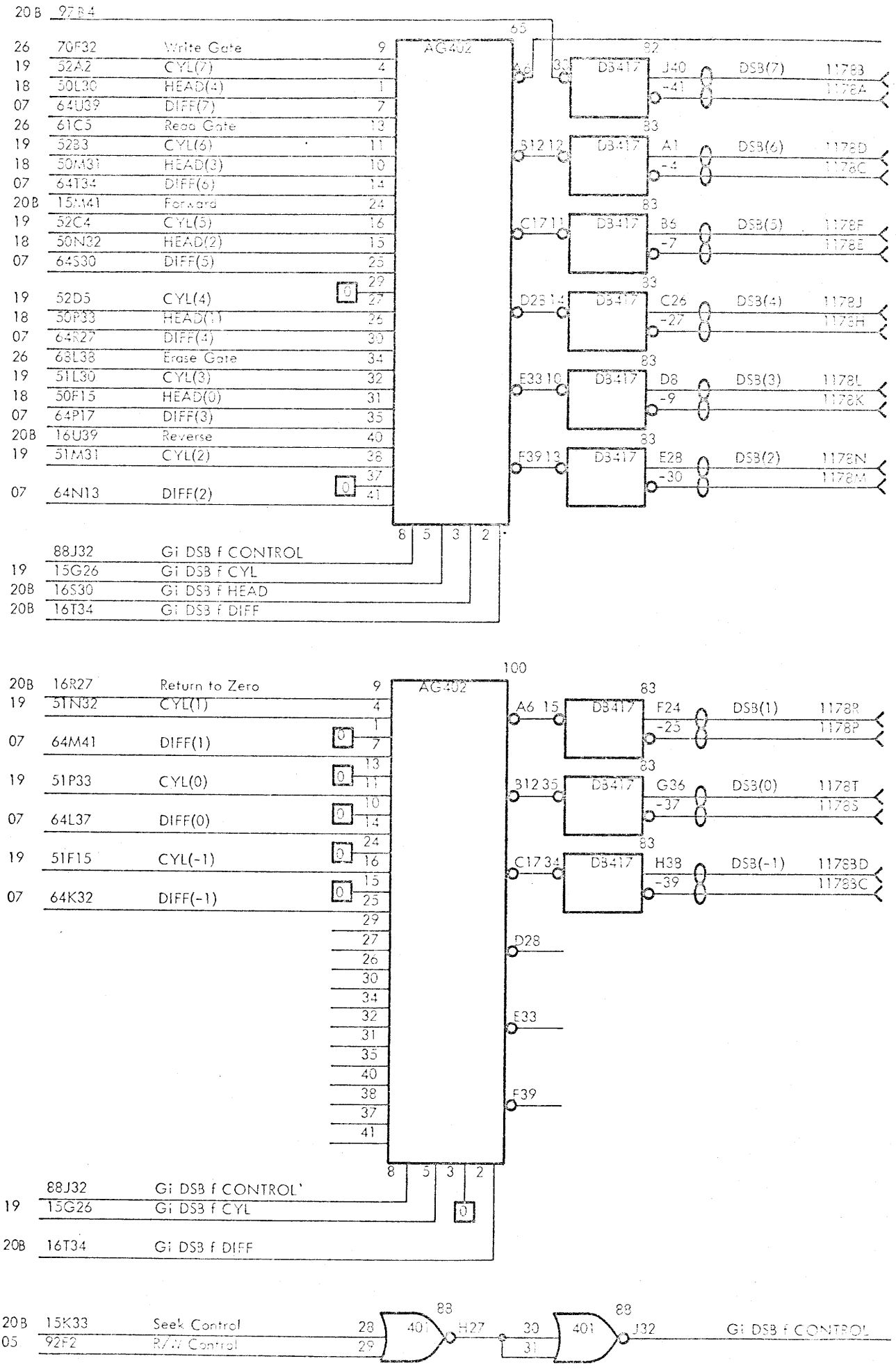
DFC 403
RC4000

CYLINDER COUNTER, CYL(-1:7)

DFC19

R 10547

Logic Diagram



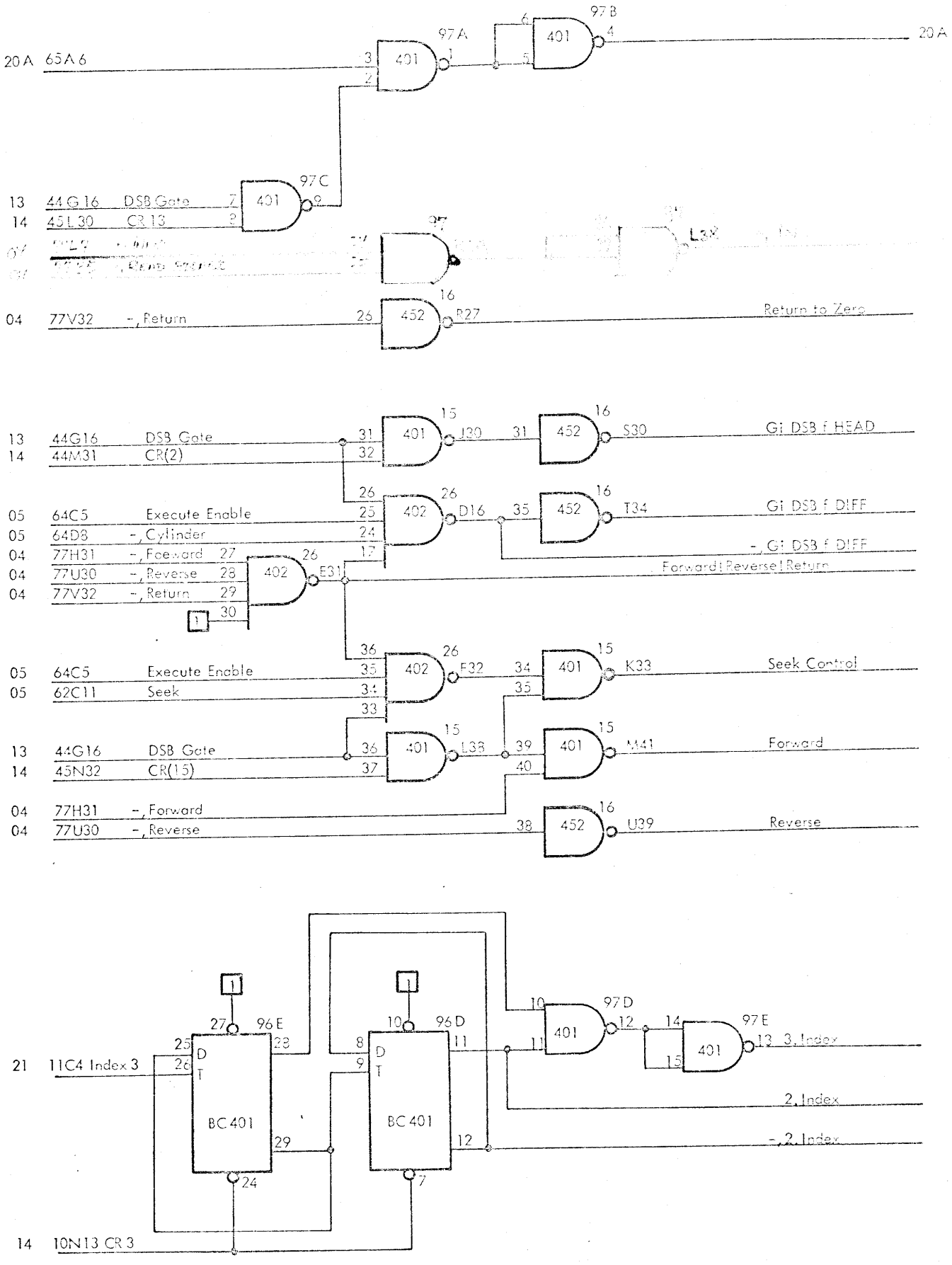
DFC 403
RC 4000

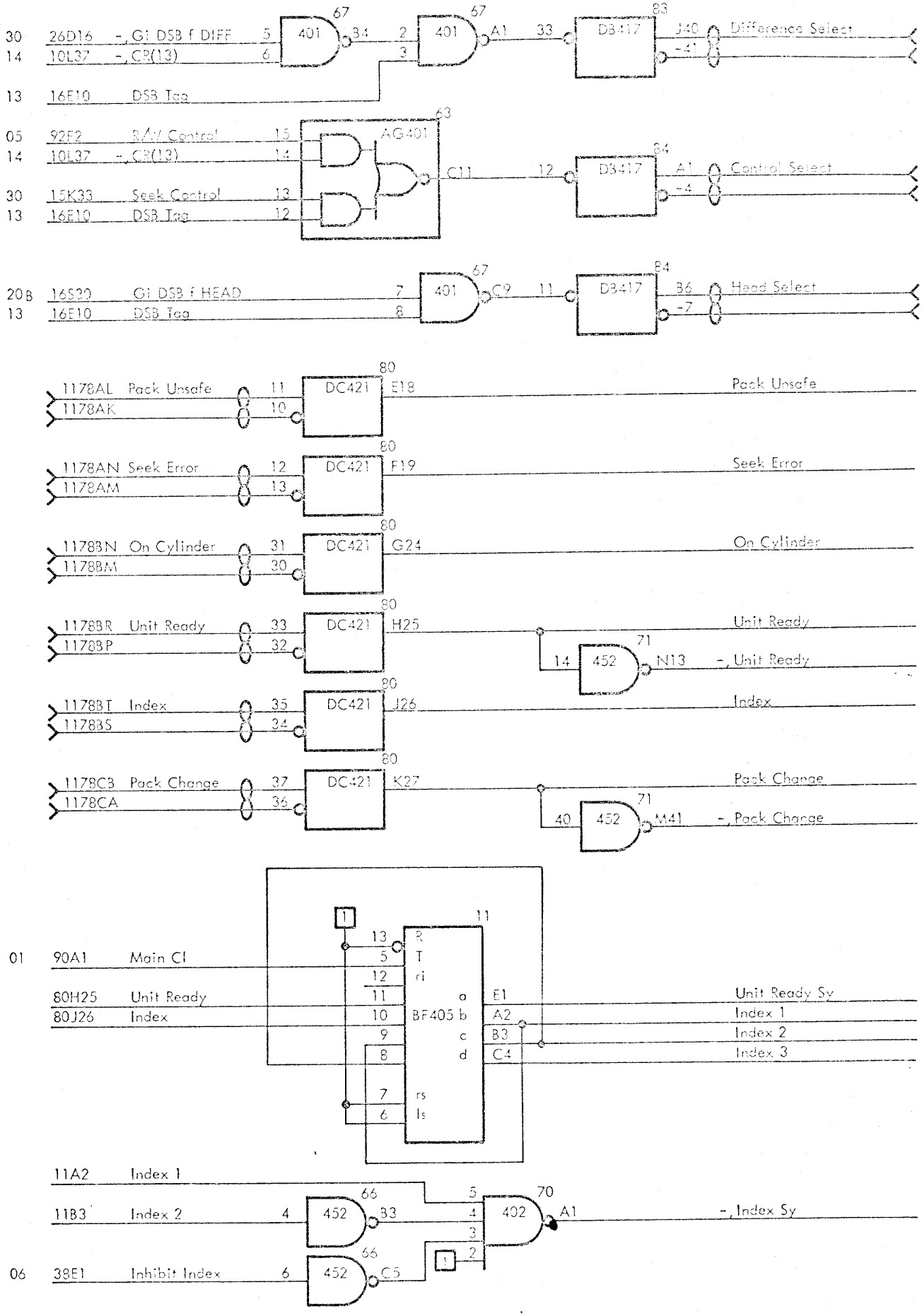
DISC STORAGE BUS, DSB(-1:7)

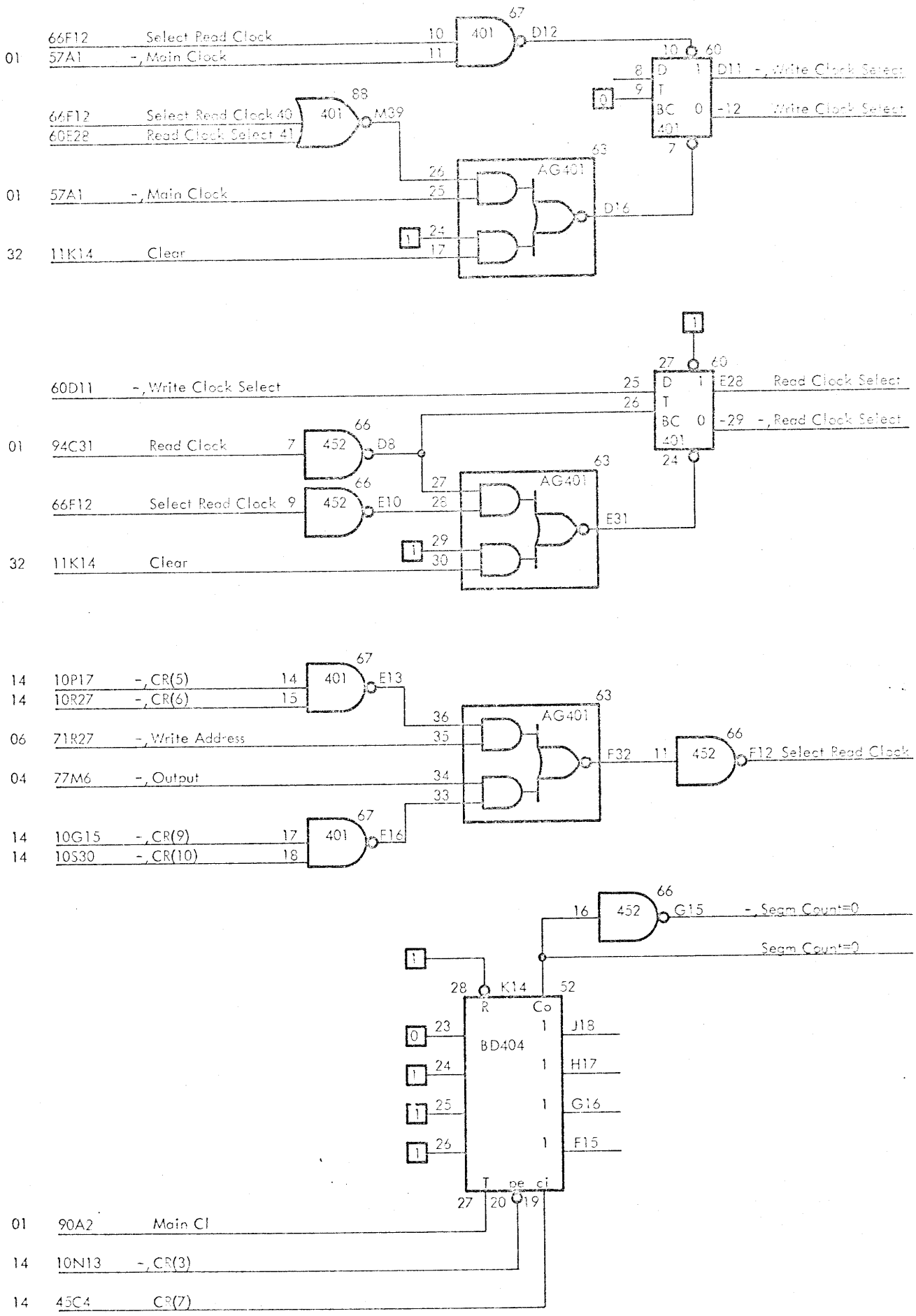
DFC 20 A

R 10548

Logic Diagram


20A 65A6
97A
97B
401
20A
13 44G16 DSB Gate
14 45L30 CR13
97C
04 77V32 -, Return
452
R27
Return to Zero
13 44G16 DSB Gate
14 44M31 CR(2)
S30
Gi DSB f HEAD
05 64C5 Execute Enable
05 64D8 -, Cylinder
04 77H31 -, Forward
04 77U30 -, Reverse
04 77V32 -, Return
402
D16
T34
Gi DSB f DIFF
-, Gi DSB f DIFF
Forward! Reverse! Return
E31
05 64C5 Execute Enable
05 62C11 Seek
E32
K33
Seek Control
13 44G16 DSB Gate
14 45N32 CR(15)
L38
M41
Forward
04 77H31 -, Forward
04 77U30 -, Reverse
U39
Reverse
21 11C4 Index 3
96E
96D
BC401
97D
97E
13 3. Index
2. Index
-, 2. Index
14 10N13 CR3


30 26D16 -, G: DSB f DIFF
14 10L37 -, CP(13)
13 16E10 DSB Tag
401
Difference Select
05 92F2 R/W Control
14 10L37 -, CP(13)
30 15K33 Seek Control
13 16E10 DSB Tag
AG401
Control Select
20B 16S20 G: DSB f HEAD
13 16E10 DSB Tag
Head Select
1178AL Pack Unsafe
1178AK
DC421
Pack Unsafe
1178AN Seek Error
1178AM
Seek Error
1178BN On Cylinder
1178BM
On Cylinder
1178BR Unit Ready
1178BP
Unit Ready
-, Unit Ready
1178BT Index
1178BS
Index
1178C3 Pack Change
1178CA
Pack Change
-, Pack Change
01 90A1 Main Cl
80H25 Unit Ready
80J26 Index
BF405
Unit Ready Sy
Index 1
Index 2
Index 3
11A2 Index 1
11B3 Index 2
06 38E1 Inhibit Index
-, Index Sy



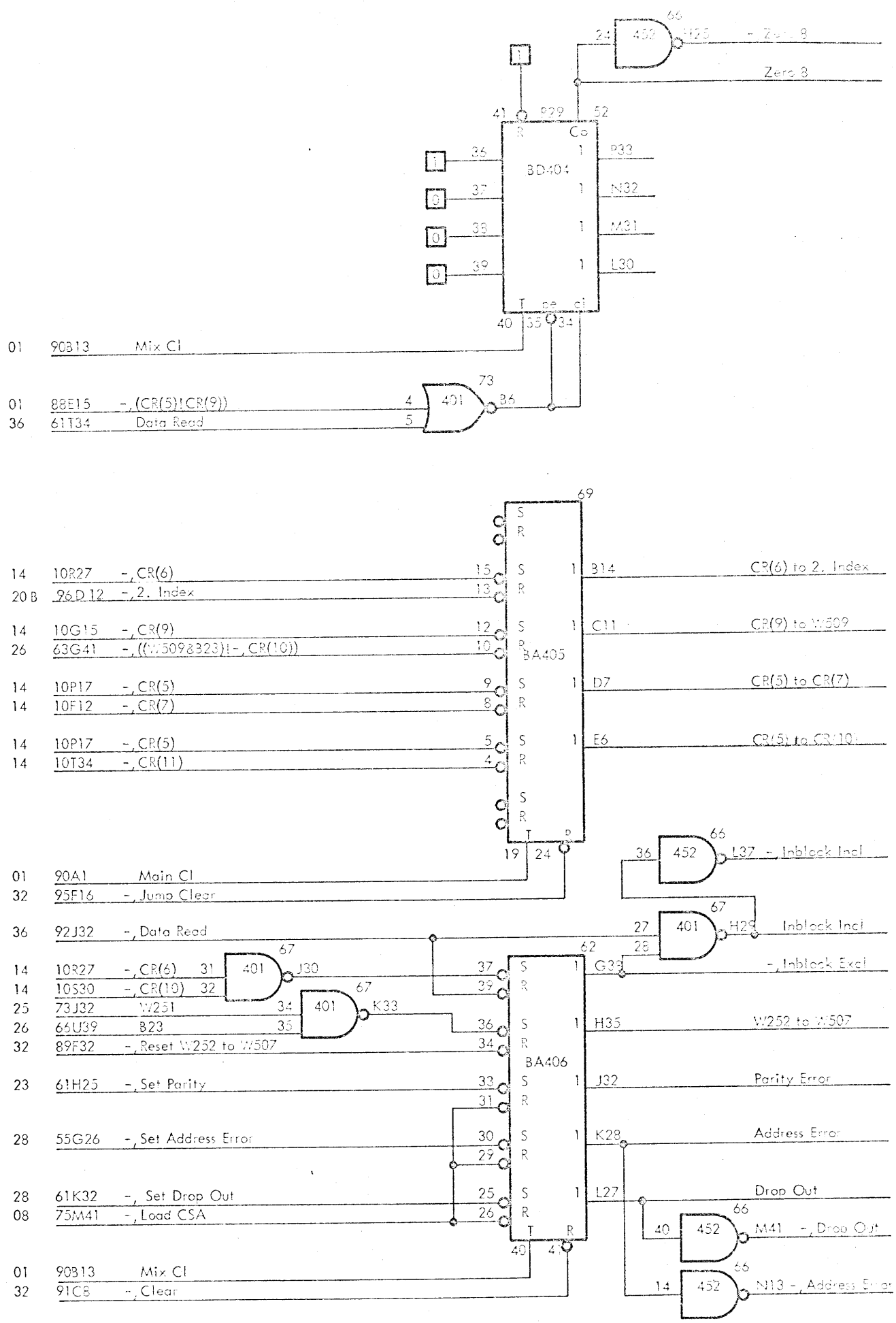
DFC 403
RC4000

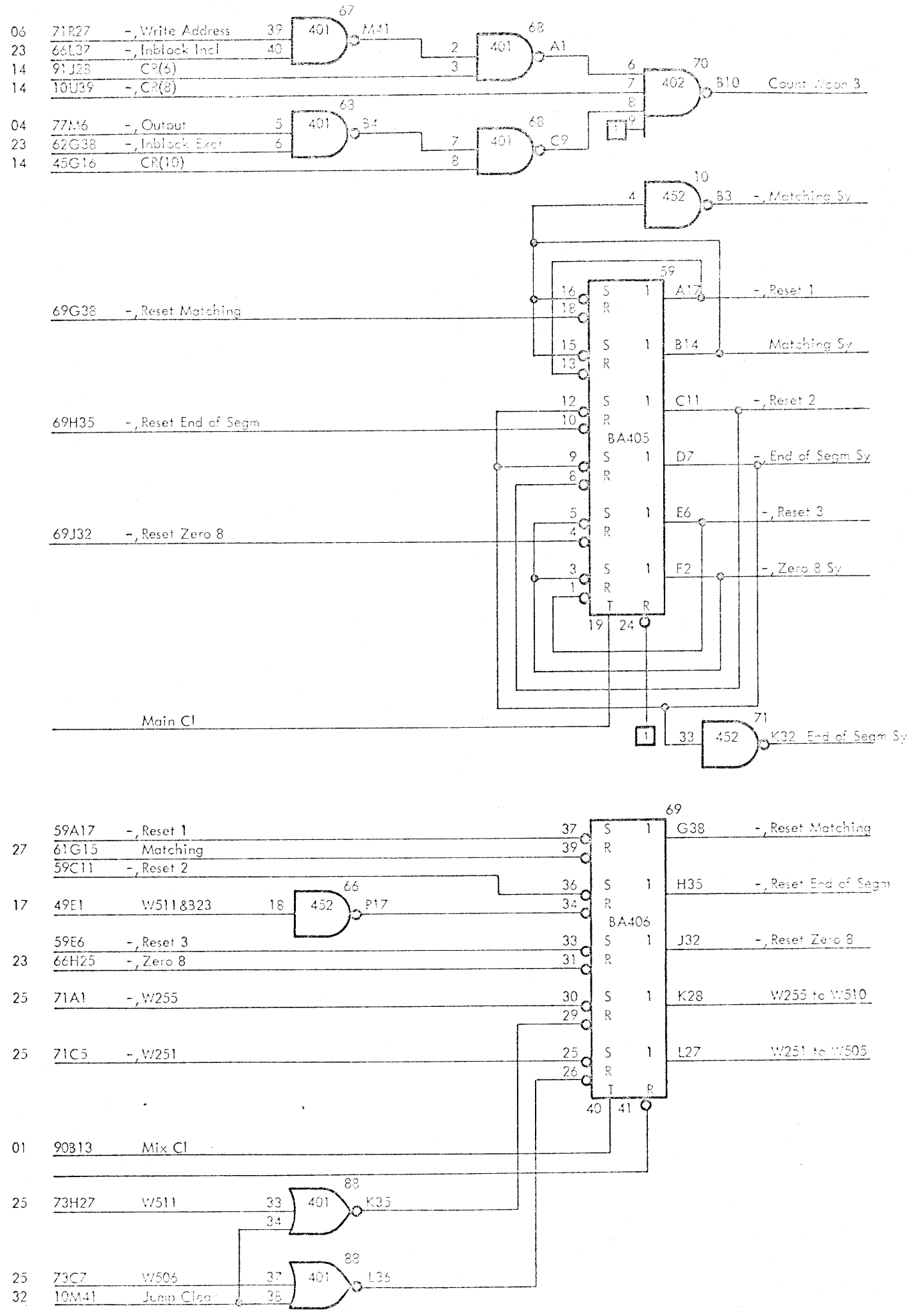
MIXED CLOCK CONTROL LOGIC, SEGMENT COUNT

DFC22

R 10551

Logic Diagram


66
452
H25
- Zero 8
Zero 8
24
41
P29
52
R
Co
BD404
36
37
38
39
P33
N32
M31
L30
T
Pe
ci
40
35
34
01 90B13 Mix CI
73
401
B6
4
5
01 88E15 -, (CR(5)!CR(9))
36 61T34 Data Read
69
S
R
14 10R27 -, CR(6)
20 B 96D 12 -, 2. Index
14 10G15 -, CR(9)
26 63G41 -, ((W509&323)!-, CR(10))
14 10P17 -, CR(5)
14 10F12 -, CR(7)
14 10P17 -, CR(5)
14 10T34 -, CR(11)
BA405
B14
CR(6) to 2. Index
C11
CR(9) to W509
D7
CR(5) to CR(7)
E6
CR(5) to CR(10)
19
24
01 90A1 Main CI
32 95F16 -, Jump Clear
66
452
L37 -, Inblock Incl
36
67
401
H23
Inblock Incl
27
28
-, Inblock Excl
36 92J32 -, Data Read
14 10R27 -, CR(6) 31
14 10S30 -, CR(10) 32
25 73J32 W251 34
26 66U39 B23 35
32 89F32 -, Reset W252 to W507
J30
K33
62
G33
H35
W252 to W507
BA406
23 61H25 -, Set Parity
J32
Parity Error
28 55G26 -, Set Address Error
K28
Address Error
28 61K32 -, Set Drop Out
08 75M41 -, Load CSA
L27
Drop Out
40
M41 -, Drop Out
14
N13 -, Address Error
01 90B13 Mix CI
32 91C8 -, Clear



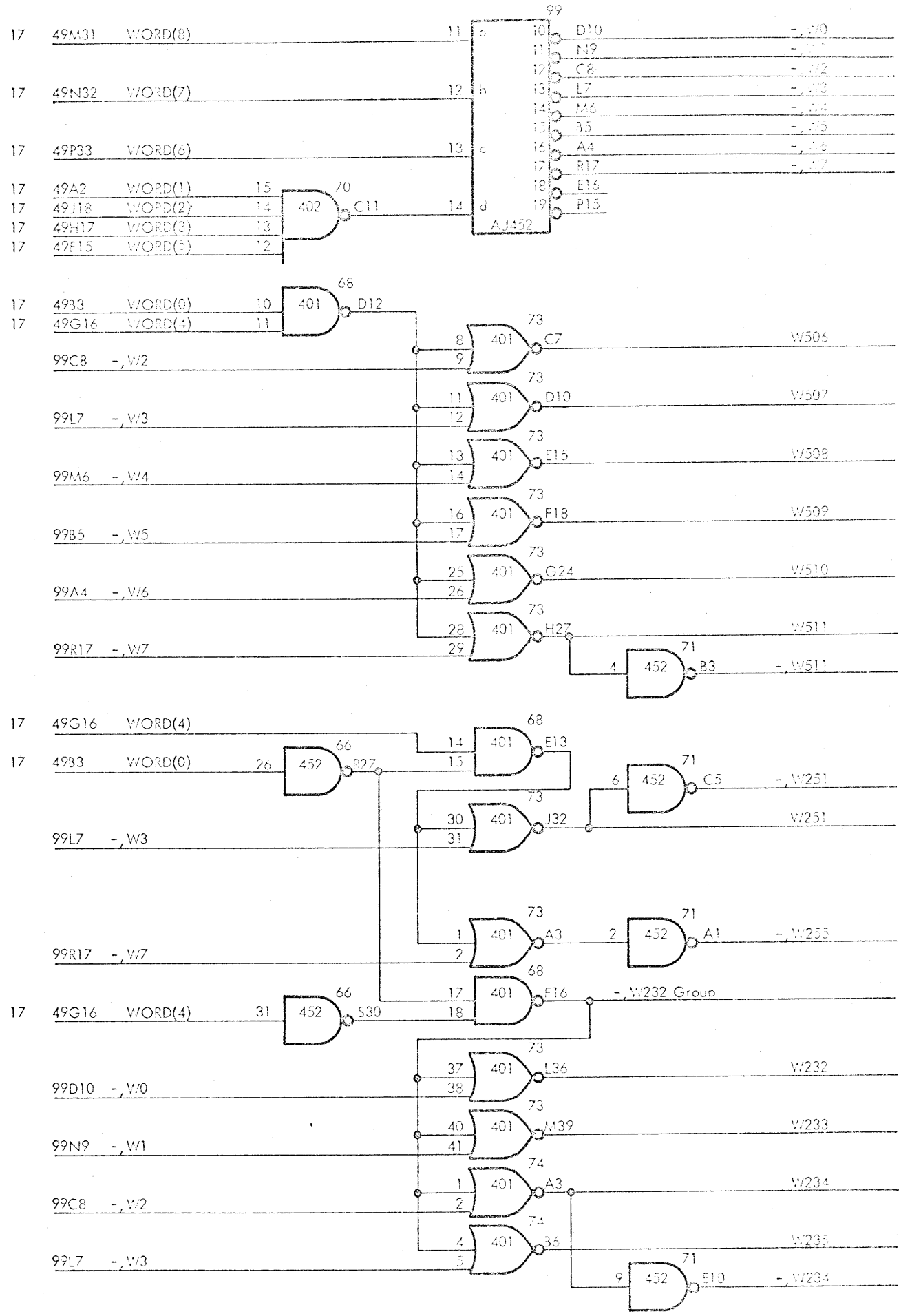
DFC 403
RC 4000

MIX CL TO MAIN CL SYNCHRONISING CIRCUIT

DFC 24

R 10553

Logic Diagram



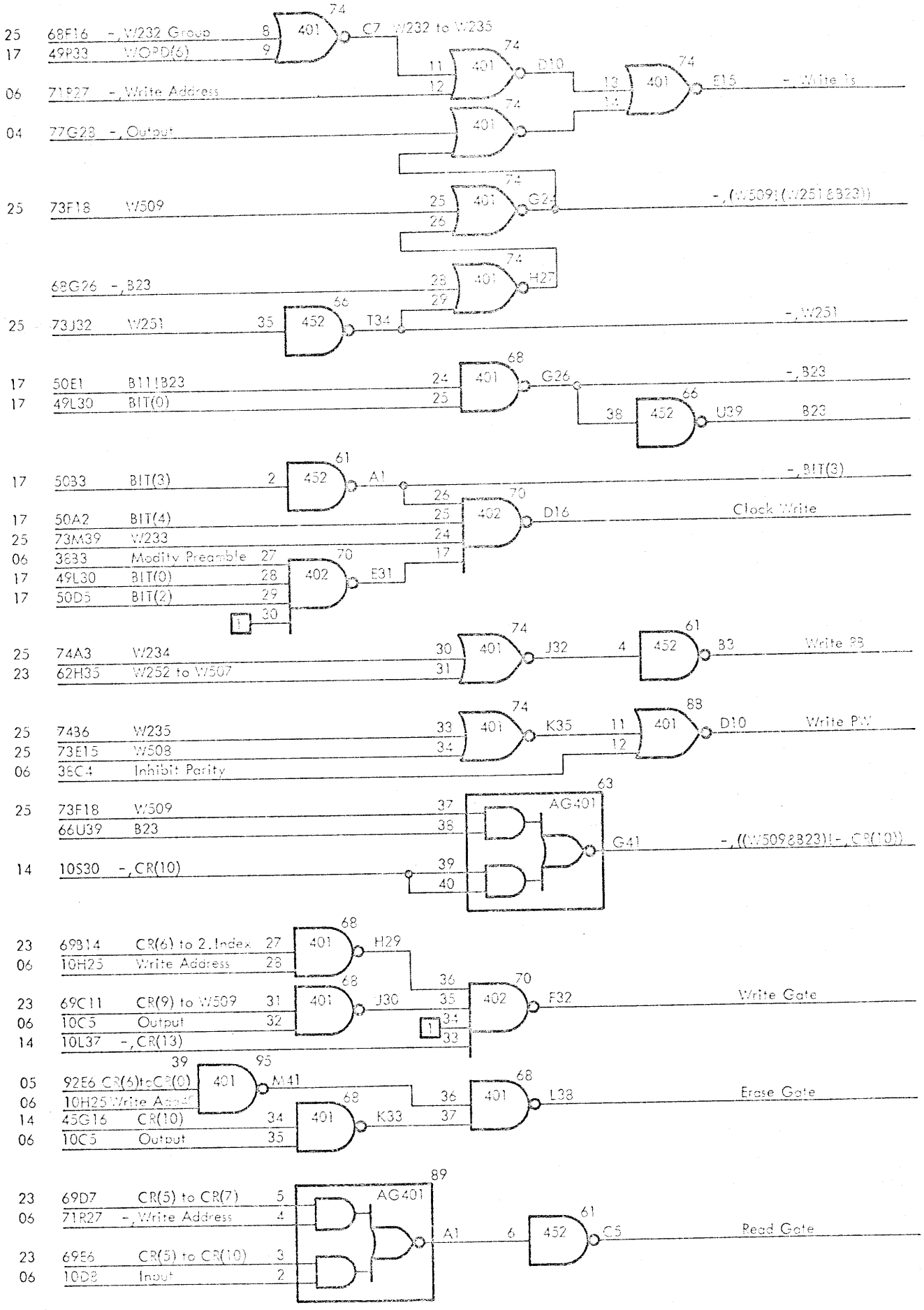
DFC 403
RC4000

WORD DECODING

DFC25

R 10554

Logic Diagram



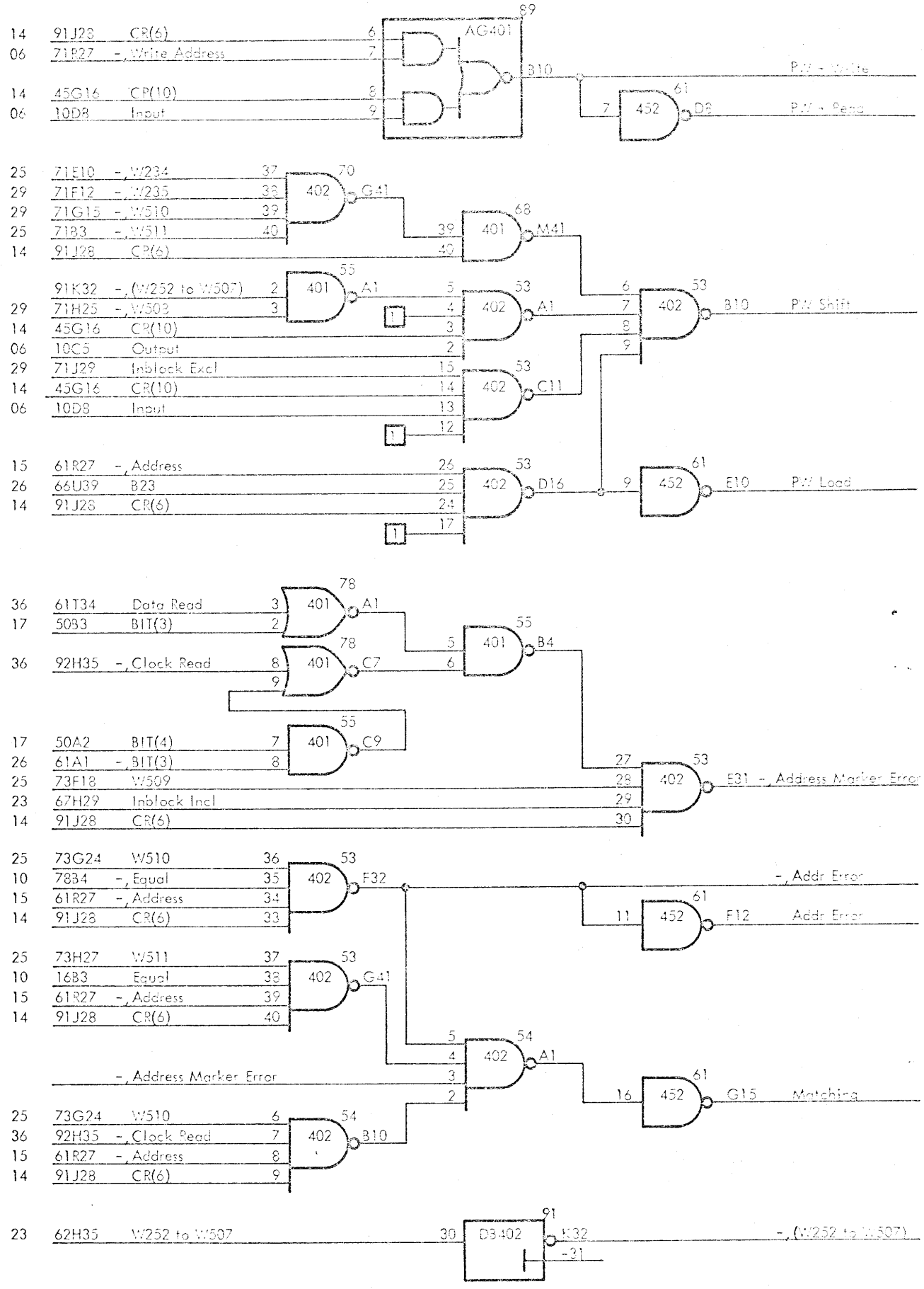
DFC 403
RC4000

WRITE GATE, ERASE GATE AND READ GATE

DFC26

R 10555

Logic Diagram



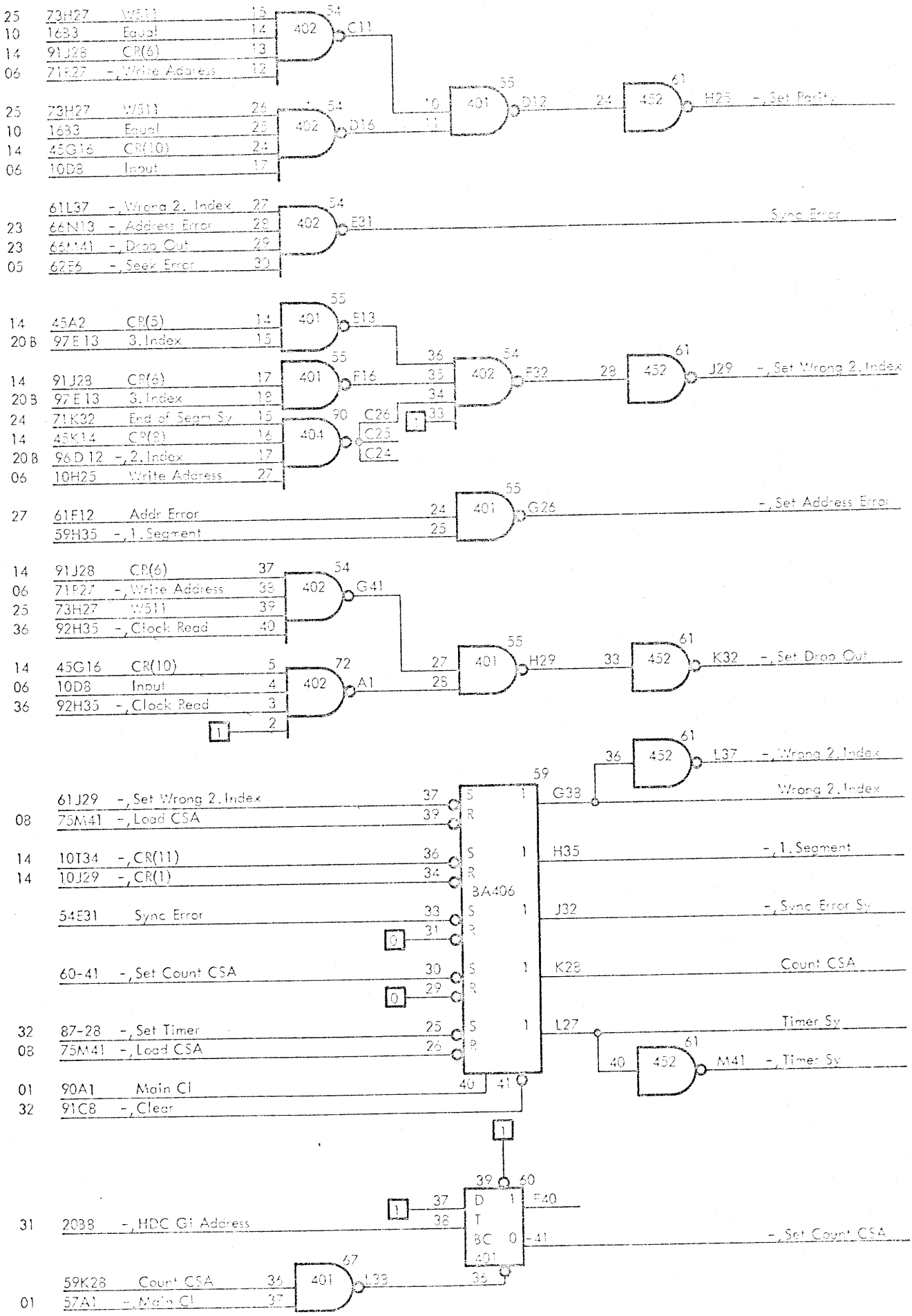
DFC 403
RC4000

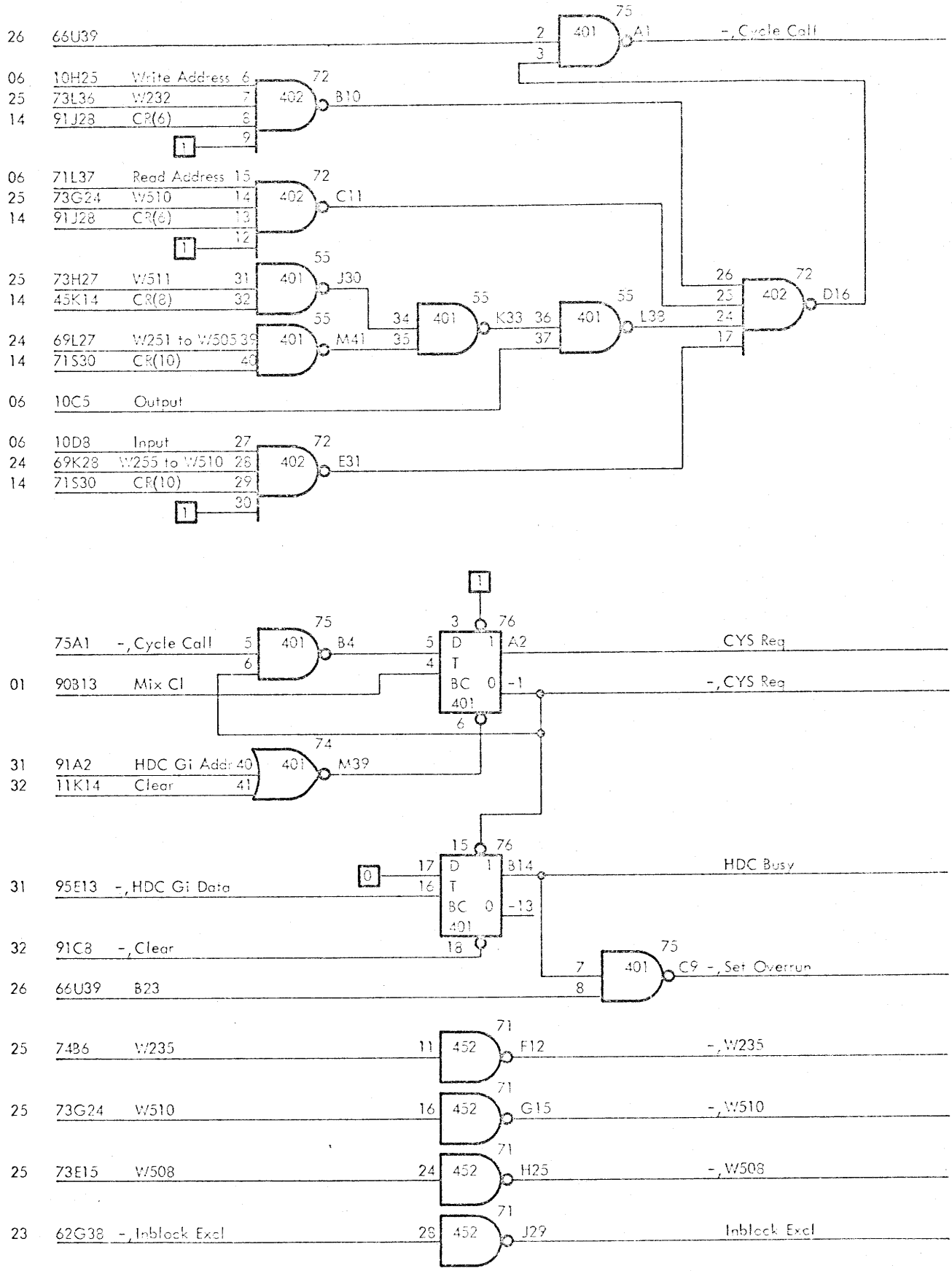
P/W CONTROL, ADDRESS MATCHING

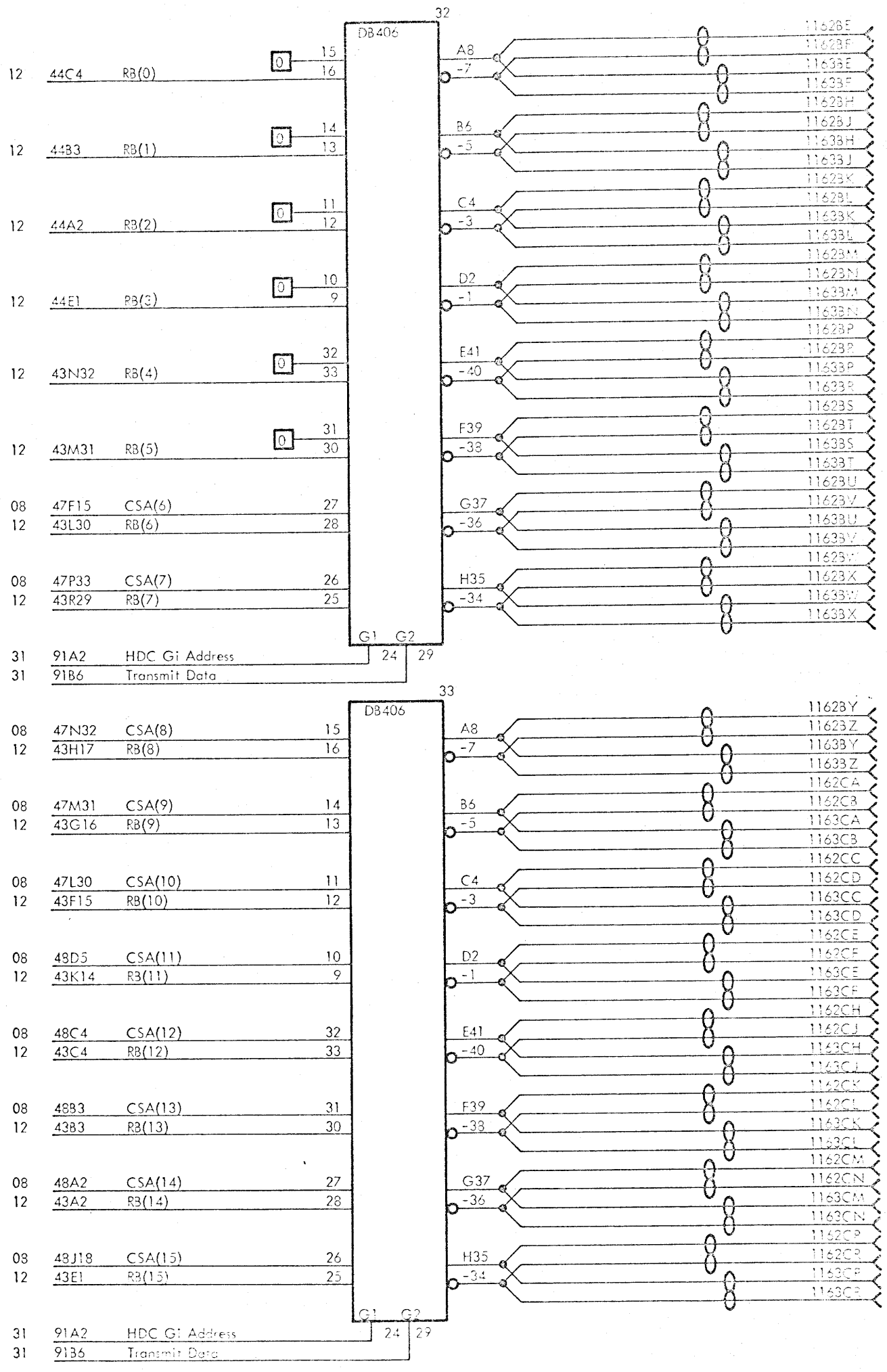
DFC07

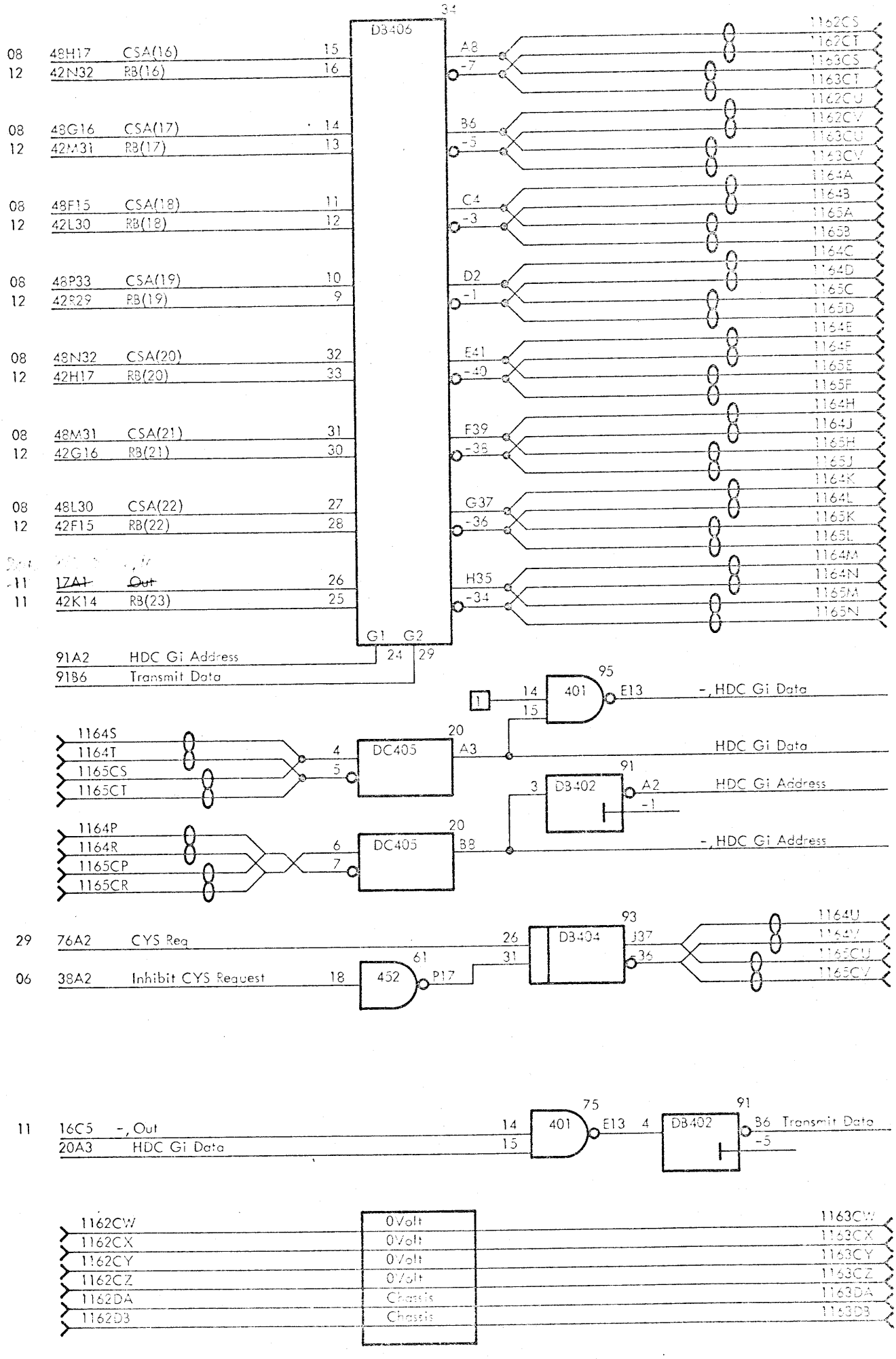
R 10556

Logic Diagram


25 Z3H27 W511 15
10 16B3 Equal 14
14 91J28 CR(6) 13
06 71F27 -, Write Address 12
54 402 C11
25 Z3H27 W511 26
10 16B3 Equal 25
14 45G16 CR(10) 24
06 10D8 Input 17
54 402 D16
10 11
55 401 D12
24
61 452 H25 -, Set Parity
61L37 -, Wrong 2. Index 27
23 66N13 -, Address Error 28
23 66M41 -, Drop Out 29
05 62E6 -, Seek Error 30
54 402 E31
Sync Error
14 45A2 CR(5) 14
20B 97E13 3. Index 15
55 401 E13
14 91J28 CR(6) 17
20B 97E13 3. Index 18
55 401 F16
24 71K32 End of Seqm Sy 15
14 45K14 CR(8) 16
20B 96D12 -, 2. Index 17
06 10H25 Write Address 27
90 404 C26 C25 C24
36 35 34 33
54 402 F32
28
61 452 J29 -, Set Wrong 2. Index
27 61F12 Addr Error 24
59H35 -, 1. Segment 25
55 401 G26
-, Set Address Error
14 91J28 CR(6) 37
06 71P27 -, Write Address 38
25 73H27 W511 39
36 92H35 -, Clock Read 40
54 402 G41
14 45G16 CR(10) 5
06 10D8 Input 4
36 92H35 -, Clock Read 3
1 2
72 402 A1
27 28
55 401 H29
33
61 452 K32 -, Set Drop Out
36
61 452 L37 -, Wrong 2. Index
59
61J29 -, Set Wrong 2. Index 37
08 75M41 -, Load CSA 39
14 10T34 -, CR(11) 36
14 10J29 -, CR(1) 34
54E31 Sync Error 33
0 31
60-41 -, Set Count CSA 30
0 29
32 87-28 -, Set Timer 25
08 75M41 -, Load CSA 26
01 90A1 Main CI
32 91C8 -, Clear
BA406
S R 1
G38
Wrong 2. Index
H35
-, 1. Segment
J32
-, Sync Error Sy
K28
Count CSA
L27
Timer Sy
40
61 452 M41 -, Timer Sy
40 41
1
39 60
1 37
31 2038 -, HDC Gl Address 38
D T BC 0 1
F40
-41
-, Set Count CSA
401
59K28 Count CSA 34
01 57A1 -, Main CI 37
67 401 L33
36


26 66U39
2
3
401
75
A1
-, Cycle Call
06 10H25 Write Address 6
25 73L36 W232 7
14 91J28 CR(6) 8
9
1
402
72
B10
06 71L37 Read Address 15
25 73G24 W510 14
14 91J28 CR(6) 13
12
1
402
72
C11
25 73H27 W511 31
14 45K14 CR(8) 32
401
55
J30
24 69L27 W251 to W505 39
14 71S30 CR(10) 40
401
55
M41
34
35
401
55
K33
36
37
401
55
L38
26
25
24
17
402
72
D16
06 10C5 Output
06 10D8 Input 27
24 69K28 W255 to W510 28
14 71S30 CR(10) 29
30
1
402
72
E31
1
75A1 -, Cycle Call 5
6
401
75
B4
3
5
4
D
T
BC
401
1
0
76
A2
-1
CYS Req
-, CYS Req
01 90B13 Mix CI
6
31 91A2 HDC Gi Addr 40
32 11K14 Clear 41
401
74
M39
15
17
16
0
D
T
BC
401
1
0
76
B14
-13
HDC Busy
31 95E13 -, HDC Gi Data
32 91C8 -, Clear
18
7
8
401
75
C9
-, Set Overrun
26 66U39 B23
25 74B6 W235 11
452
71
F12
-, W235
25 73G24 W510 16
452
71
G15
-, W510
25 73E15 W508 24
452
71
H25
-, W508
23 62G38 -, Inblock Excl 28
452
71
J29
Inblock Excl


32
DB406
12 44C4 RB(0) 15 16
12 44B3 RB(1) 14 13
12 44A2 RB(2) 11 12
12 44E1 RB(3) 10 9
12 43N32 RB(4) 32 33
12 43M31 RB(5) 31 30
08 47F15 CSA(6) 27
12 43L30 RB(6) 28
08 47P33 CSA(7) 26
12 43R29 RB(7) 25
A8 -7
B6 -5
C4 -3
D2 -1
E41 -40
F39 -38
G37 -36
H35 -34
11628E 11628F 11638E 11638F 11628H 11628J 11638H 11638J 11628K 11628L 11638K 11638L 11628M 11628N 11638M 11638N 11628P 11628R 11638P 11638R 11628S 11628T 11638S 11638T 11628U 11628V 11638U 11638V 11628W 11628X 11638W 11638X
G1 G2
31 91A2 HDC Gi Address 24
31 91B6 Transmit Data 29
33
DB406
08 47N32 CSA(8) 15
12 43H17 RB(8) 16
08 47M31 CSA(9) 14
12 43G16 RB(9) 13
08 47L30 CSA(10) 11
12 43F15 RB(10) 12
08 48D5 CSA(11) 10
12 43K14 RB(11) 9
08 48C4 CSA(12) 32
12 43C4 RB(12) 33
08 48B3 CSA(13) 31
12 43B3 RB(13) 30
08 48A2 CSA(14) 27
12 43A2 RB(14) 28
08 48J18 CSA(15) 26
12 43E1 RB(15) 25
A8 -7
B6 -5
C4 -3
D2 -1
E41 -40
F39 -38
G37 -36
H35 -34
11628Y 11628Z 11638Y 11638Z 1162CA 1162CB 1163CA 1163CB 1162CC 1162CD 1163CC 1163CD 1162CE 1162CF 1163CE 1163CF 1162CH 1162CJ 1163CH 1163CJ 1162CK 1162CL 1163CK 1163CL 1162CM 1162CN 1163CM 1163CN 1162CP 1162CR 1163CP 1163CR
G1 G2
31 91A2 HDC Gi Address 24
31 91B6 Transmit Data 29



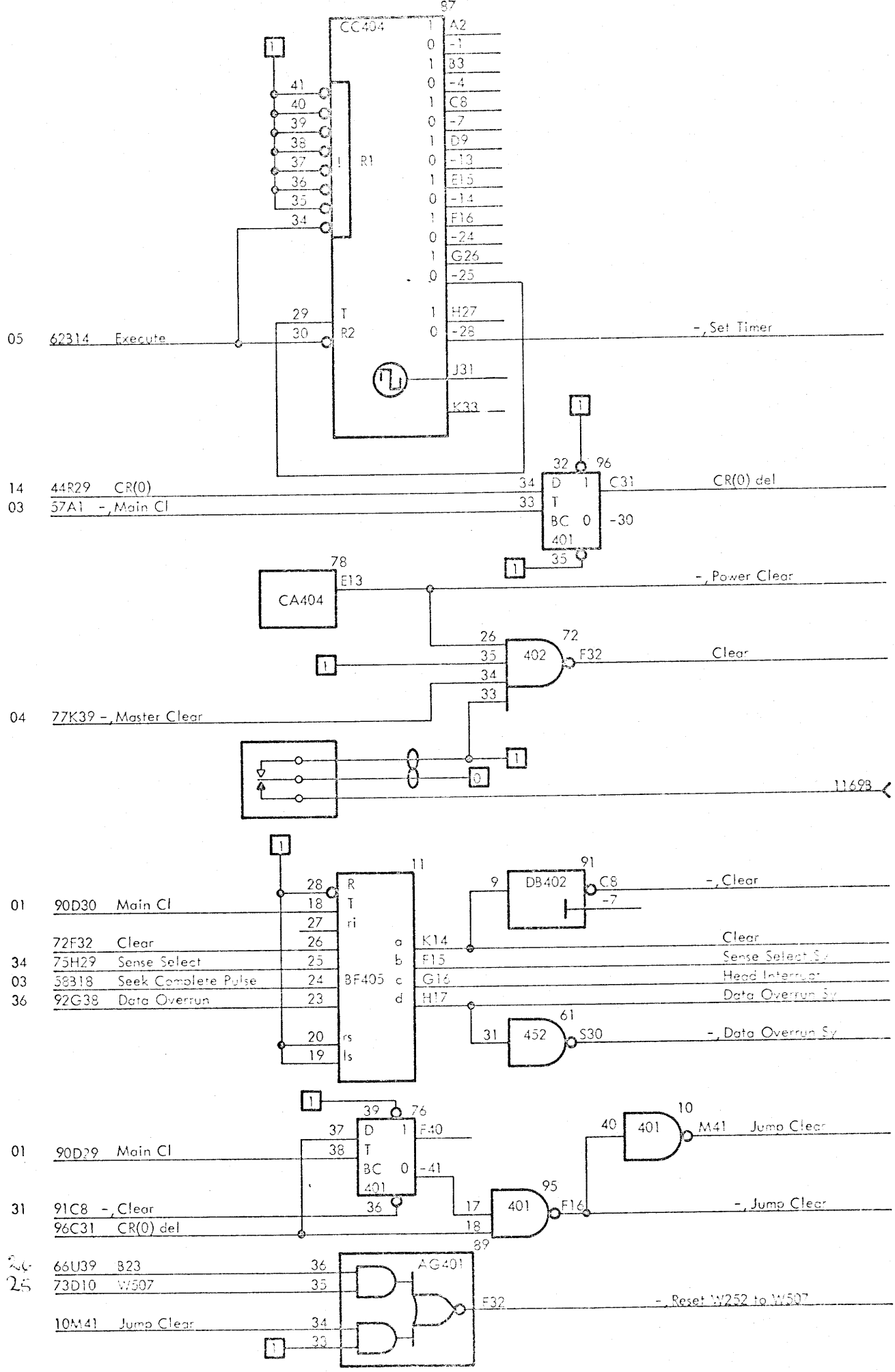
DFC 403
RC4000

HDC TRANSMITTERS AND HDC CONTROL SIGNALS

DFC31

R 10560

Logic Diagram



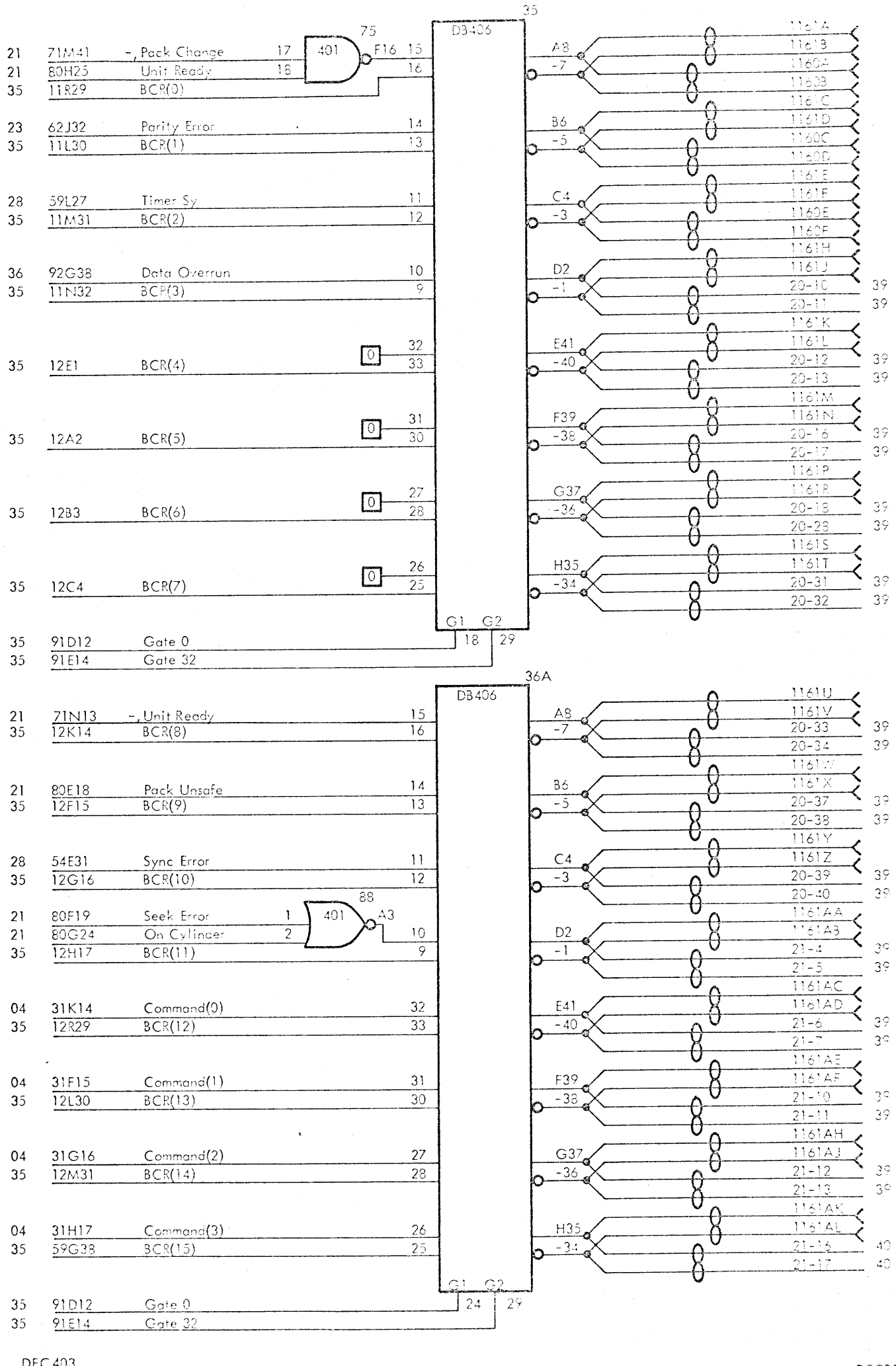
DFC403
RC4000

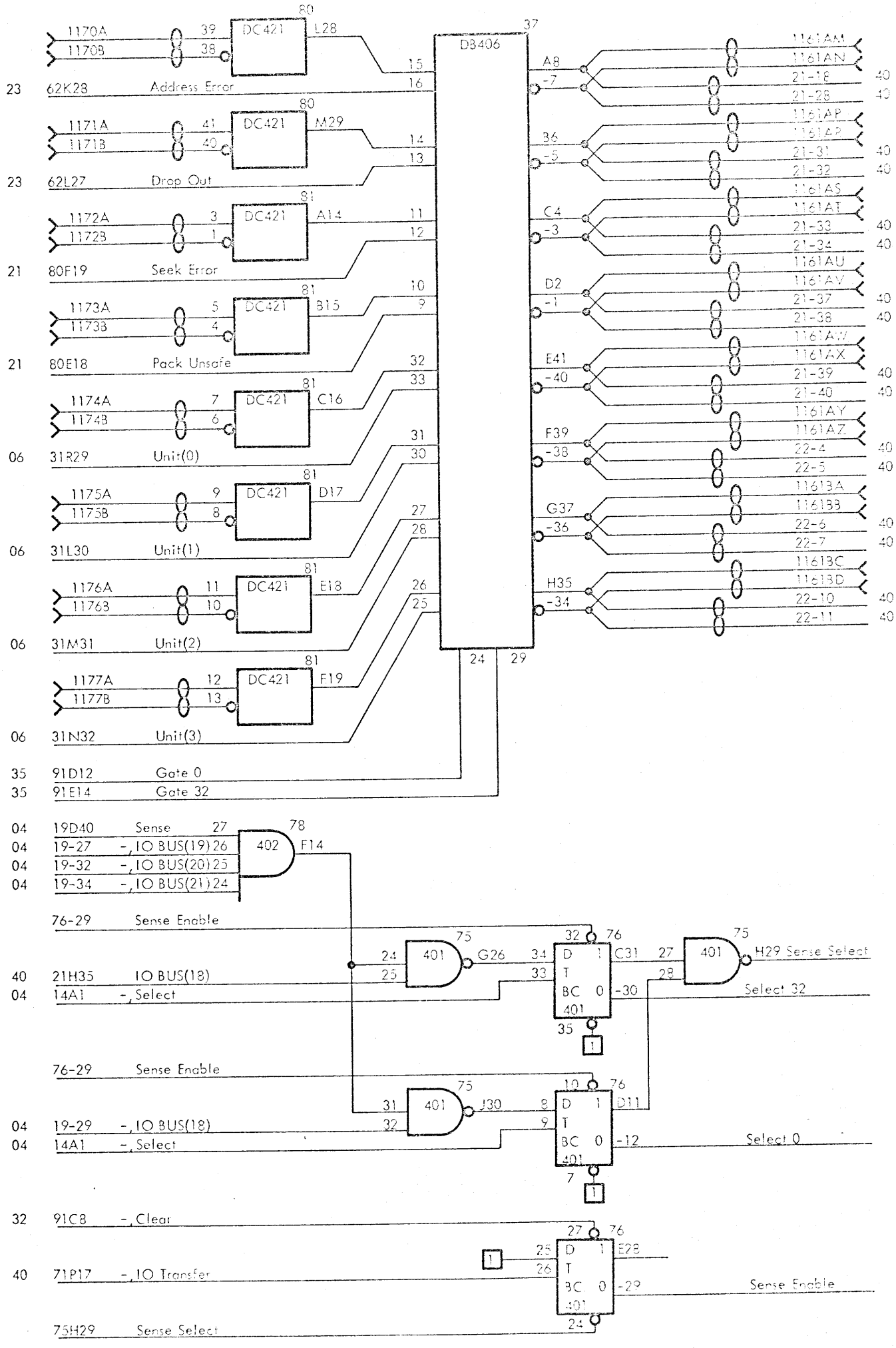
TIMER AND CLEAR SIGNALS

DFC32

R 10561

Logic Diagram


35
DB406
75
401
F16
21 71M41 -, Pack Change 17
21 80H25 Unit Ready 18
35 11R29 BCR(0) 15
16
23 62J32 Parity Error 14
35 11L30 BCR(1) 13
28 59L27 Timer Sy 11
35 11M31 BCR(2) 12
36 92G38 Data Overrun 10
35 11N32 BCR(3) 9
35 12E1 BCR(4) 0 32 33
35 12A2 BCR(5) 0 31 30
35 12B3 BCR(6) 0 27 28
35 12C4 BCR(7) 0 26 25
A8 -7
B6 -5
C4 -3
D2 -1
E41 -40
F39 -38
G37 -36
H35 -34
1161A 1161B 1160A 1160B 1161C 1161D 1160C 1160D 1161E 1161F 1160E 1160F 1161H 1161J 1161K 1161L 1161M 1161N 1161P 1161R 1161S 1161T
20-10 39
20-11 39
20-12 39
20-13 39
20-16 39
20-17 39
20-18 39
20-28 39
20-31 39
20-32 39
G1 G2
18 29
35 91D12 Gate 0
35 91E14 Gate 32
36A
DB406
21 71N13 -, Unit Ready 15
35 12K14 BCR(8) 16
21 80E18 Pack Unsafe 14
35 12F15 BCR(9) 13
28 54E31 Sync Error 11
35 12G16 BCR(10) 12
88
401
A3
21 80F19 Seek Error 1
21 80G24 On Cylinder 2
35 12H17 BCR(11) 10 9
04 31K14 Command(0) 32
35 12R29 BCR(12) 33
04 31F15 Command(1) 31
35 12L30 BCR(13) 30
04 31G16 Command(2) 27
35 12M31 BCR(14) 28
04 31H17 Command(3) 26
35 59G38 BCR(15) 25
A8 -7
B6 -5
C4 -3
D2 -1
E41 -40
F39 -38
G37 -36
H35 -34
1161U 1161V 1161W 1161X 1161Y 1161Z 1161AA 1161AB 1161AC 1161AD 1161AE 1161AF 1161AH 1161AJ 1161AK 1161AL
20-33 39
20-34 39
20-37 39
20-38 39
20-39 39
20-40 39
21-4 39
21-5 39
21-6 39
21-7 39
21-10 39
21-11 39
21-12 39
21-13 39
21-16 40
21-17 40
G1 G2
24 29
35 91D12 Gate 0
35 91E14 Gate 32



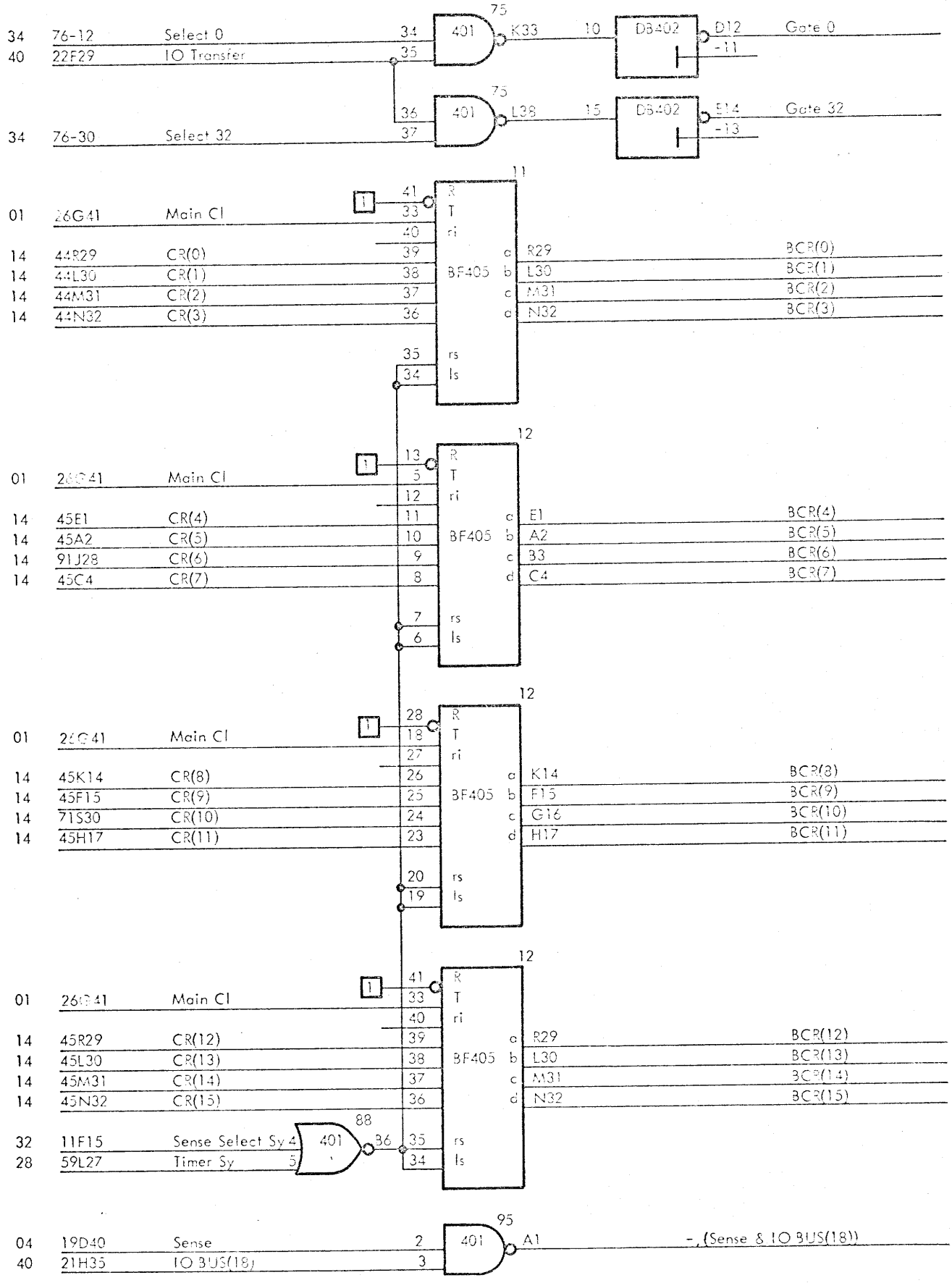
DFC 403
RC4000

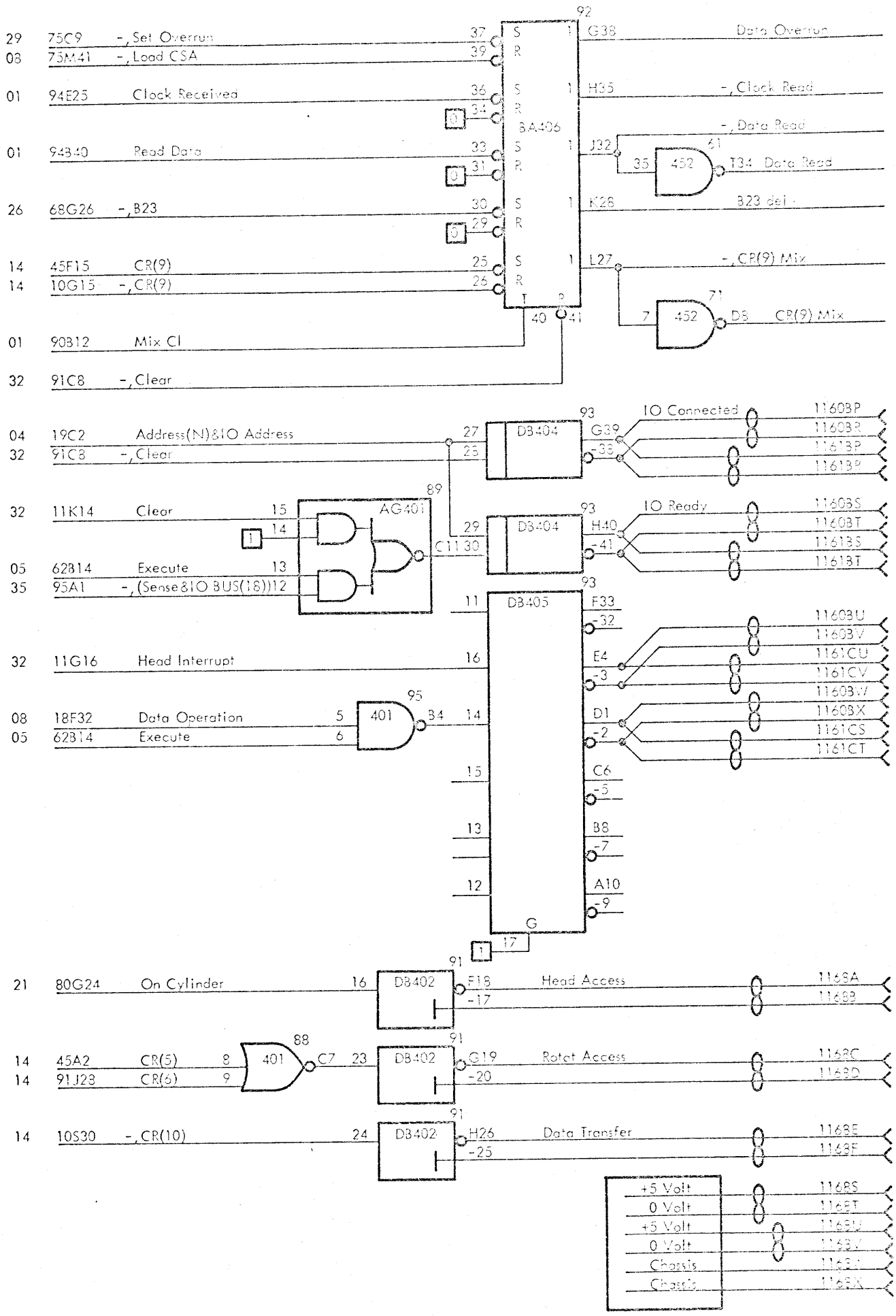
STATUS TRANSMITTERS AND SENCE SELECT LOGIC

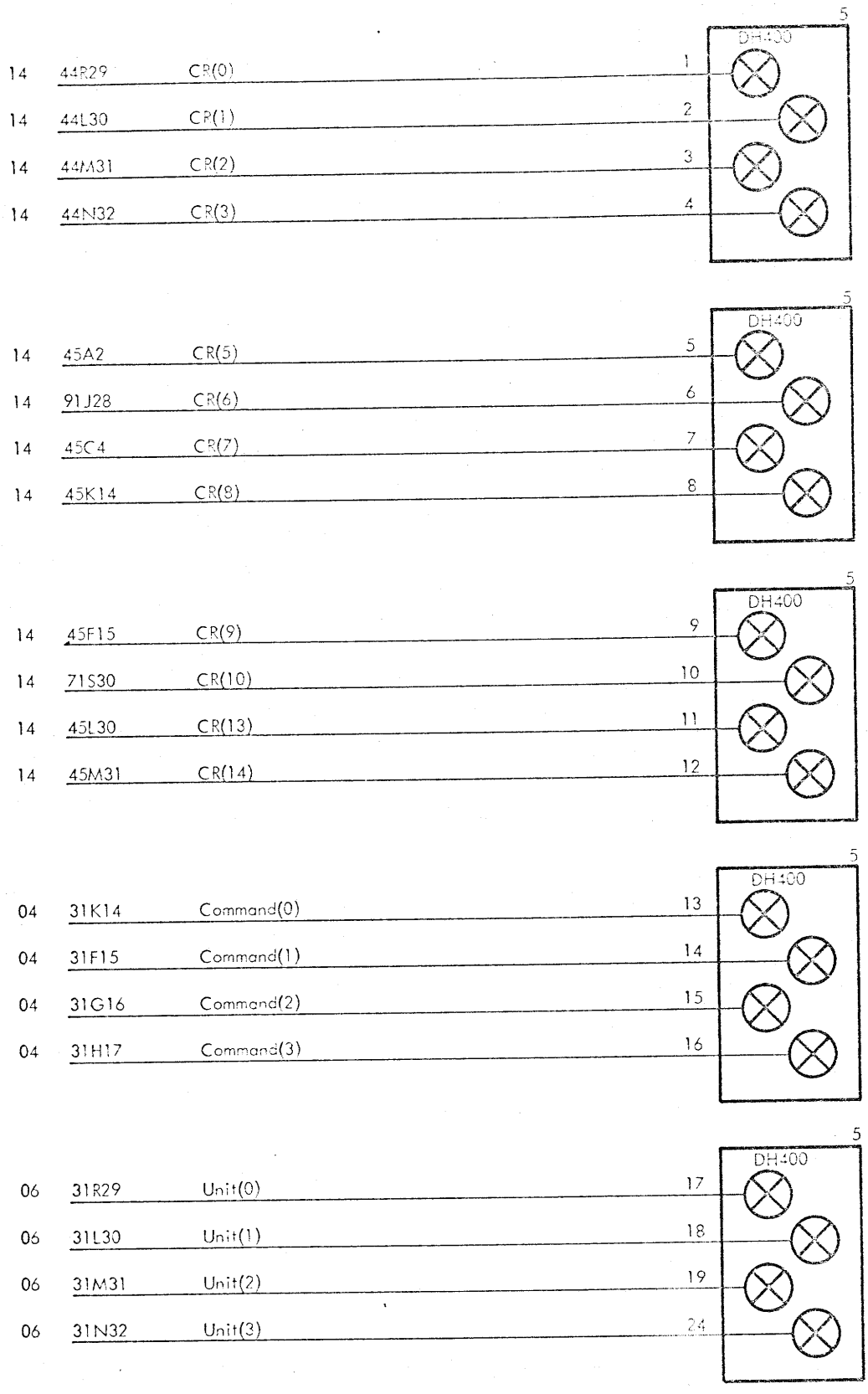
DFC34

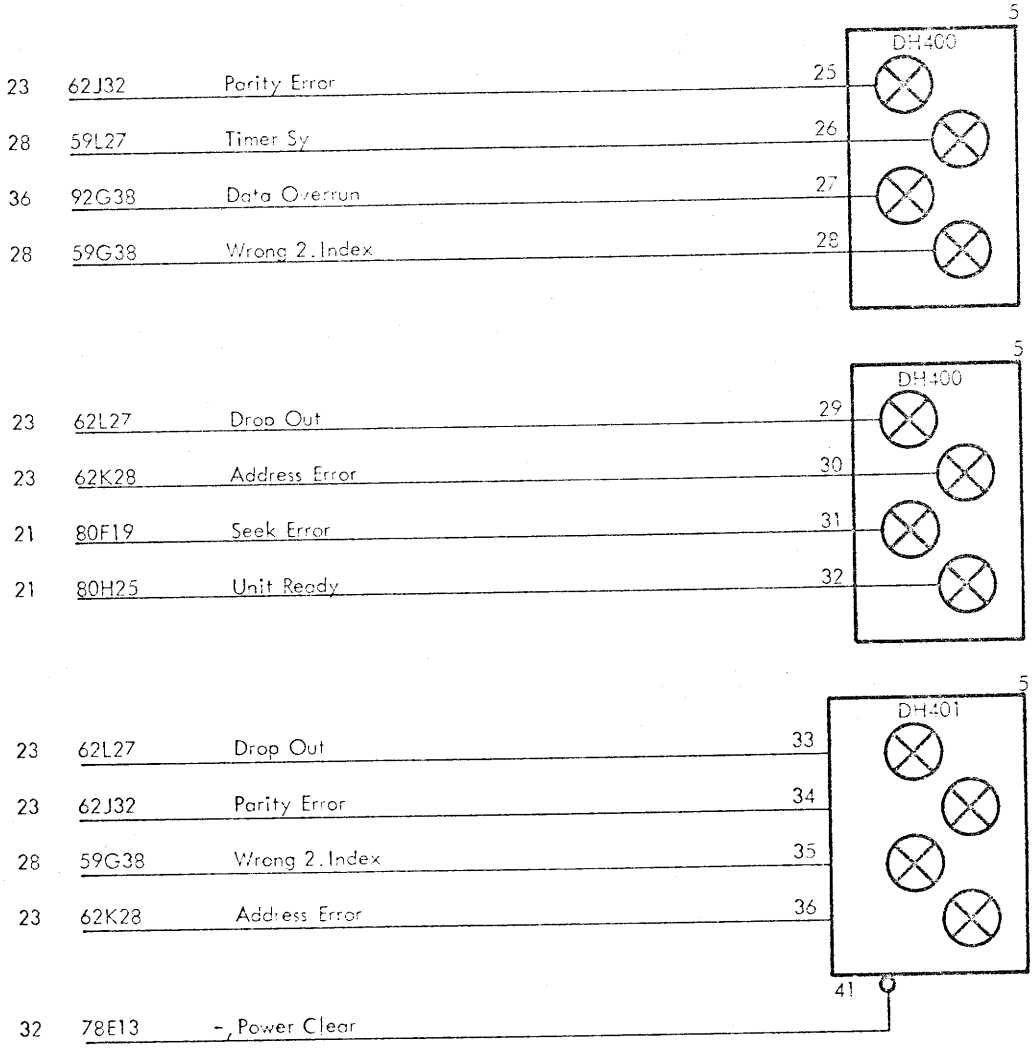
R 10563

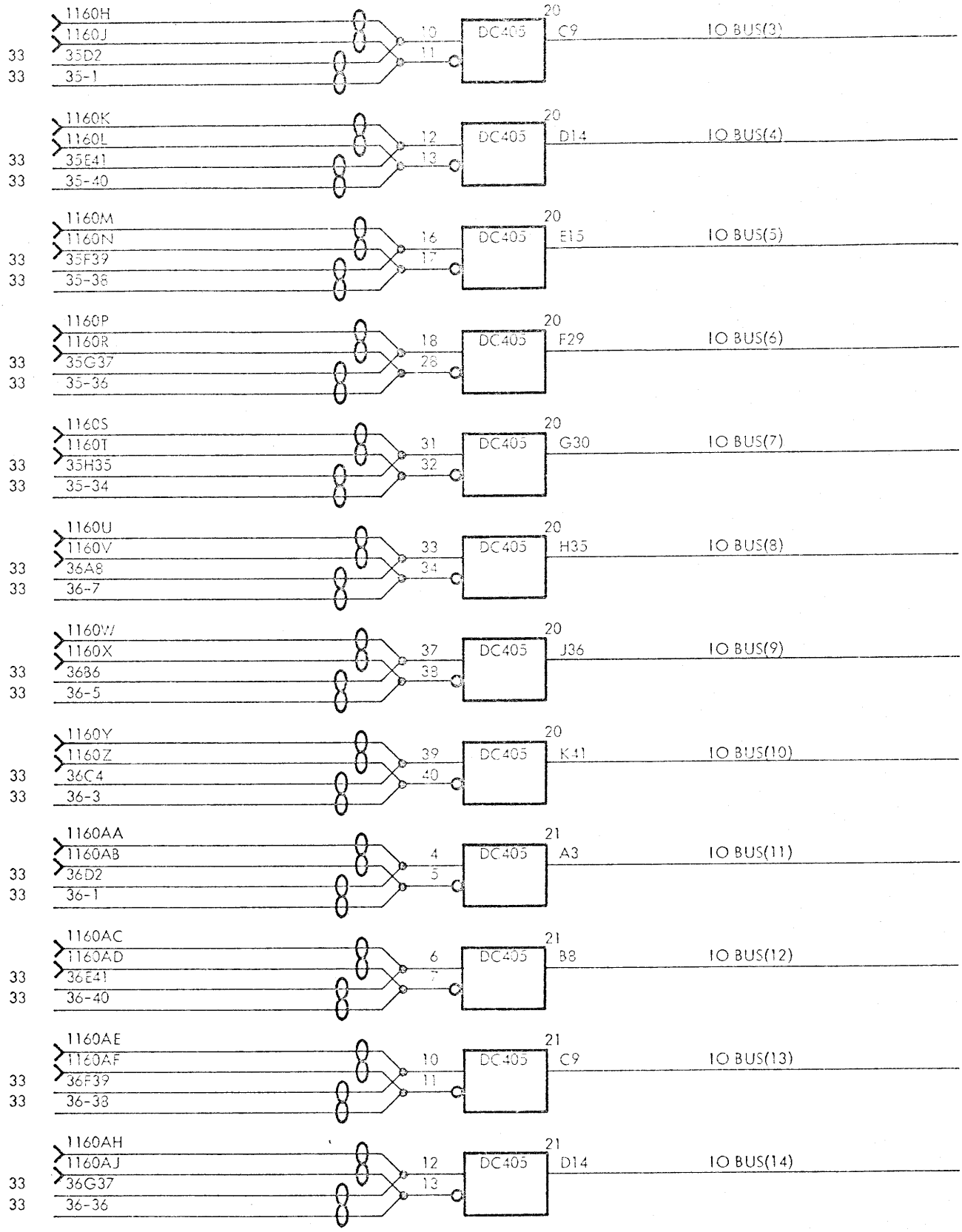
Logic Diagram

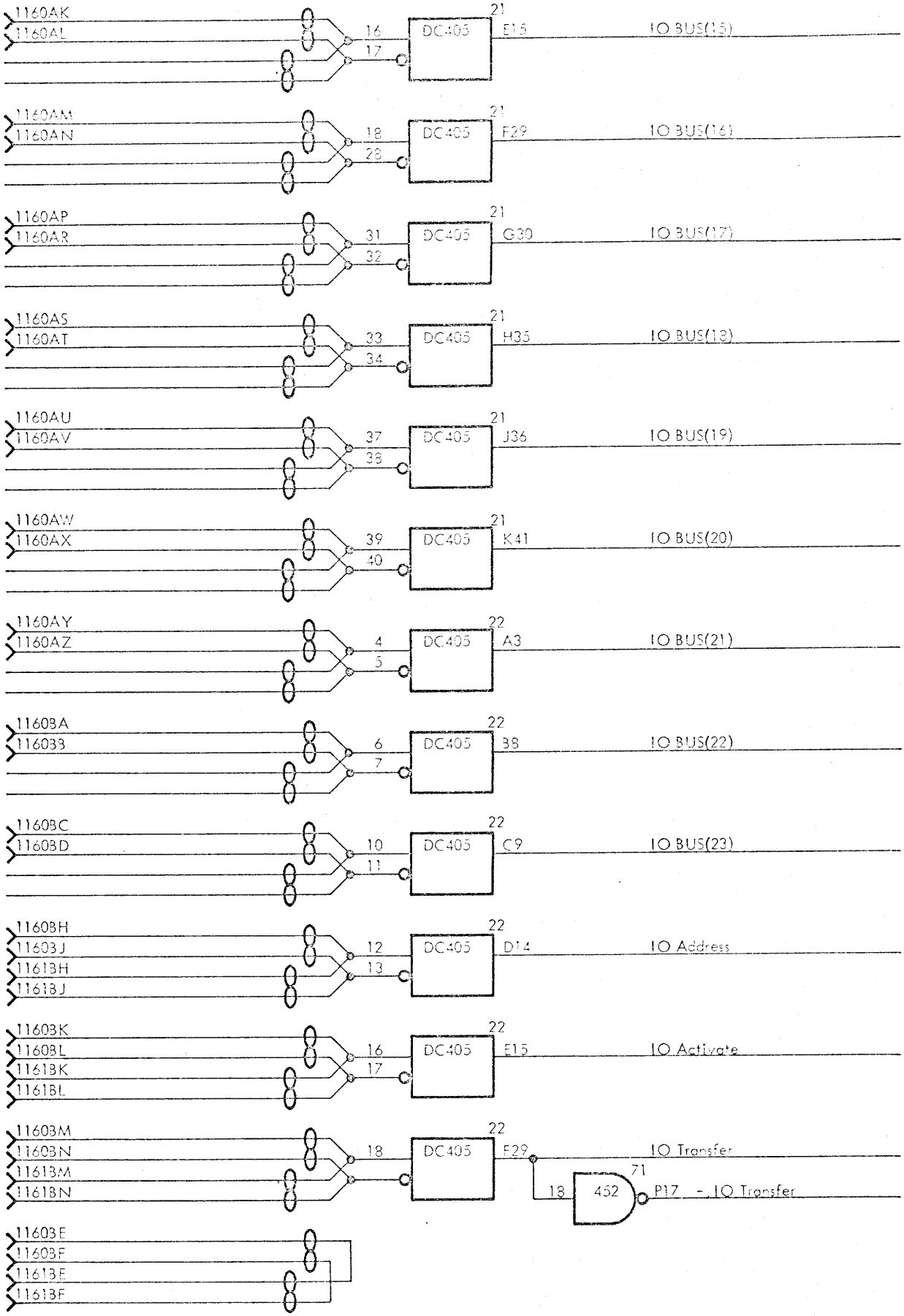

34 76-12 Select 0
40 22F29 IO Transfer
34 76-30 Select 32
75
401
K33
10
DB402
D12
-11
Gate 0
75
401
L38
15
DB402
E14
-13
Gate 32
11
BF405
01 26G41 Main CI
14 44R29 CR(0)
14 44L30 CR(1)
14 44M31 CR(2)
14 44N32 CR(3)
R29 BCR(0)
L30 BCR(1)
M31 BCR(2)
N32 BCR(3)
12
BF405
01 26G41 Main CI
14 45E1 CR(4)
14 45A2 CR(5)
14 91J28 CR(6)
14 45C4 CR(7)
E1 BCR(4)
A2 BCR(5)
B3 BCR(6)
C4 BCR(7)
12
BF405
01 26G41 Main CI
14 45K14 CR(8)
14 45F15 CR(9)
14 71S30 CR(10)
14 45H17 CR(11)
K14 BCR(8)
F15 BCR(9)
G16 BCR(10)
H17 BCR(11)
12
BF405
01 26G41 Main CI
14 45R29 CR(12)
14 45L30 CR(13)
14 45M31 CR(14)
14 45N32 CR(15)
R29 BCR(12)
L30 BCR(13)
M31 BCR(14)
N32 BCR(15)
88
401
32 11F15 Sense Select Sy 4
28 59L27 Timer Sy 5
95
401
04 19D40 Sense
40 21H35 IO BUS(18)
A1
-, (Sense & IO BUS(18))

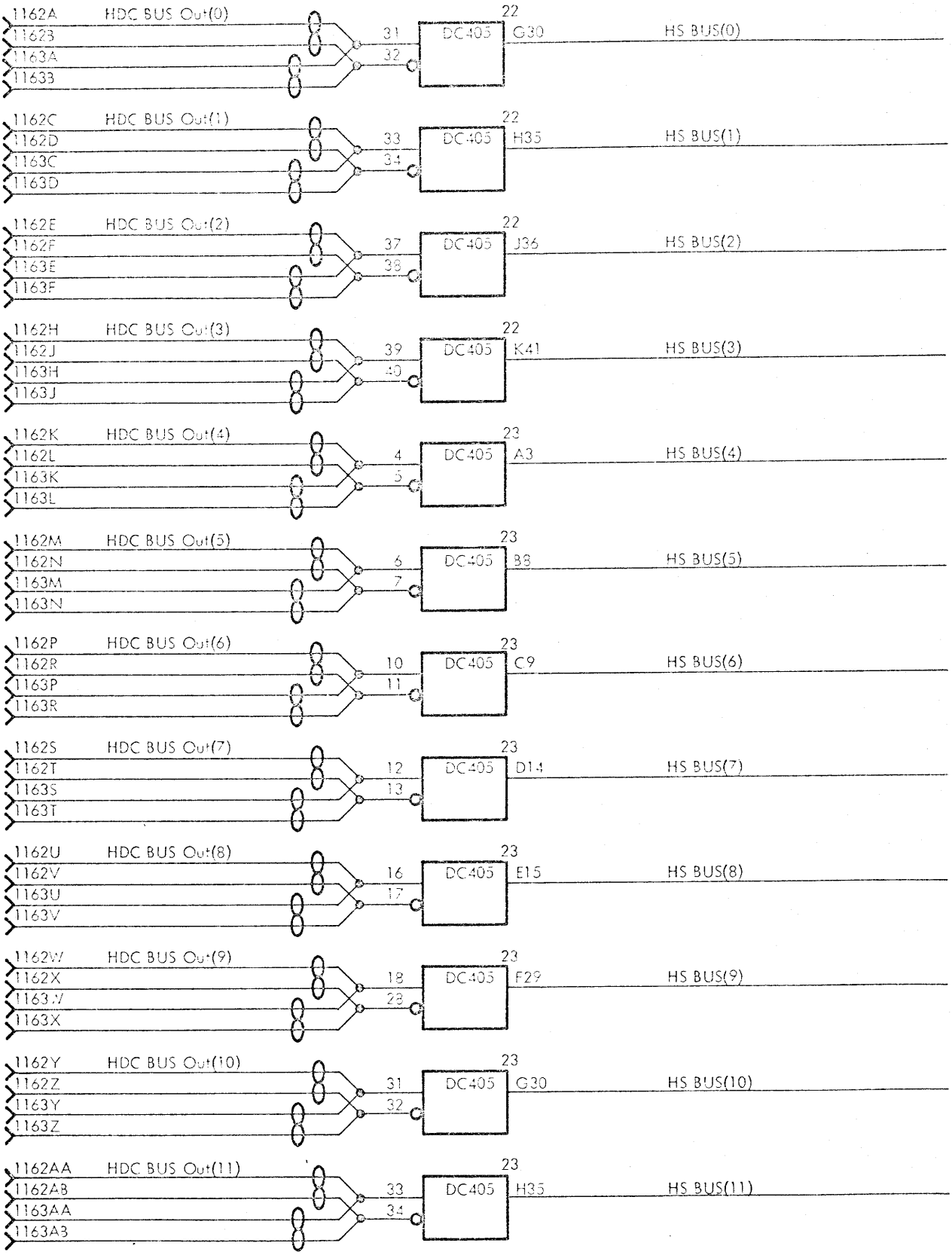

92
29 75C9 -,Set Overrun
08 75M41 -,Load CSA
01 94E25 Clock Received
01 94B40 Read Data
26 68G26 -,B23
14 45F15 CR(9)
14 10G15 -,CR(9)
01 90B12 Mix CI
32 91C8 -,Clear
BA406
G38 Data Overrun
H35 -,Clock Read
-,Data Read
J32
61
452
T34 Data Read
K28 B23 del -
L27 -,CR(9) Mix
71
452
D8 CR(9) Mix
04 19C2 Address(N)&IO Address
32 91C8 -,Clear
93
DB404
G39
IO Connected
11603P
11603R
11613P
11613R
32 11K14 Clear
05 62B14 Execute
35 95A1 -,(Sense&IO BUS(18))12
89
AG401
DB404
H40
IO Ready
11603S
11603T
11613S
11613T
32 11G16 Head Interrupt
08 18F32 Data Operation
05 62B14 Execute
95
401
B4
DB405
F33
E4
D1
C6
B8
A10
11603U
11603V
11161CU
11161CV
11603W
11603X
11161CS
11161CT
21 80G24 On Cylinder
91
DB402
F18
Head Access
1168A
1168B
14 45A2 CR(5)
14 91J23 CR(6)
88
401
C7
91
DB402
G19
Rotat Access
1168C
1168D
14 10S30 -,CR(10)
91
DB402
H26
Data Transfer
1168E
1168F
+5 Volt
0 Volt
+5 Volt
0 Volt
Chassis
Chassis
1168S
1168T
1168U
1168V
1168W
1168X

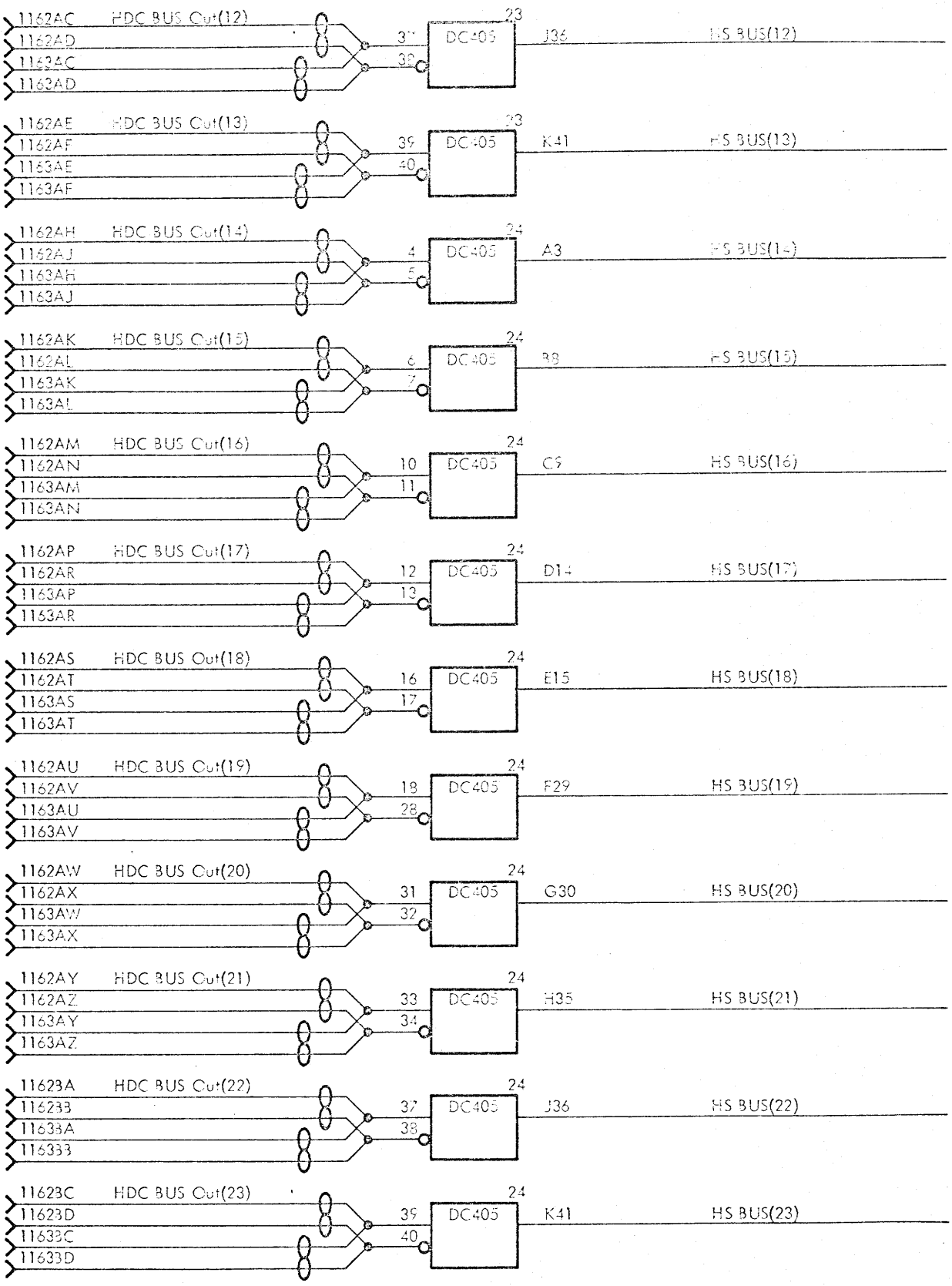

5
DH400
14 44R29 CR(0) 1
14 44L30 CR(1) 2
14 44M31 CR(2) 3
14 44N32 CR(3) 4
5
DH400
14 45A2 CR(5) 5
14 91J28 CR(6) 6
14 45C4 CR(7) 7
14 45K14 CR(8) 8
5
DH400
14 45F15 CR(9) 9
14 71S30 CR(10) 10
14 45L30 CR(13) 11
14 45M31 CR(14) 12
5
DH400
04 31K14 Command(0) 13
04 31F15 Command(1) 14
04 31G16 Command(2) 15
04 31H17 Command(3) 16
5
DH400
06 31R29 Unit(0) 17
06 31L30 Unit(1) 18
06 31M31 Unit(2) 19
06 31N32 Unit(3) 24

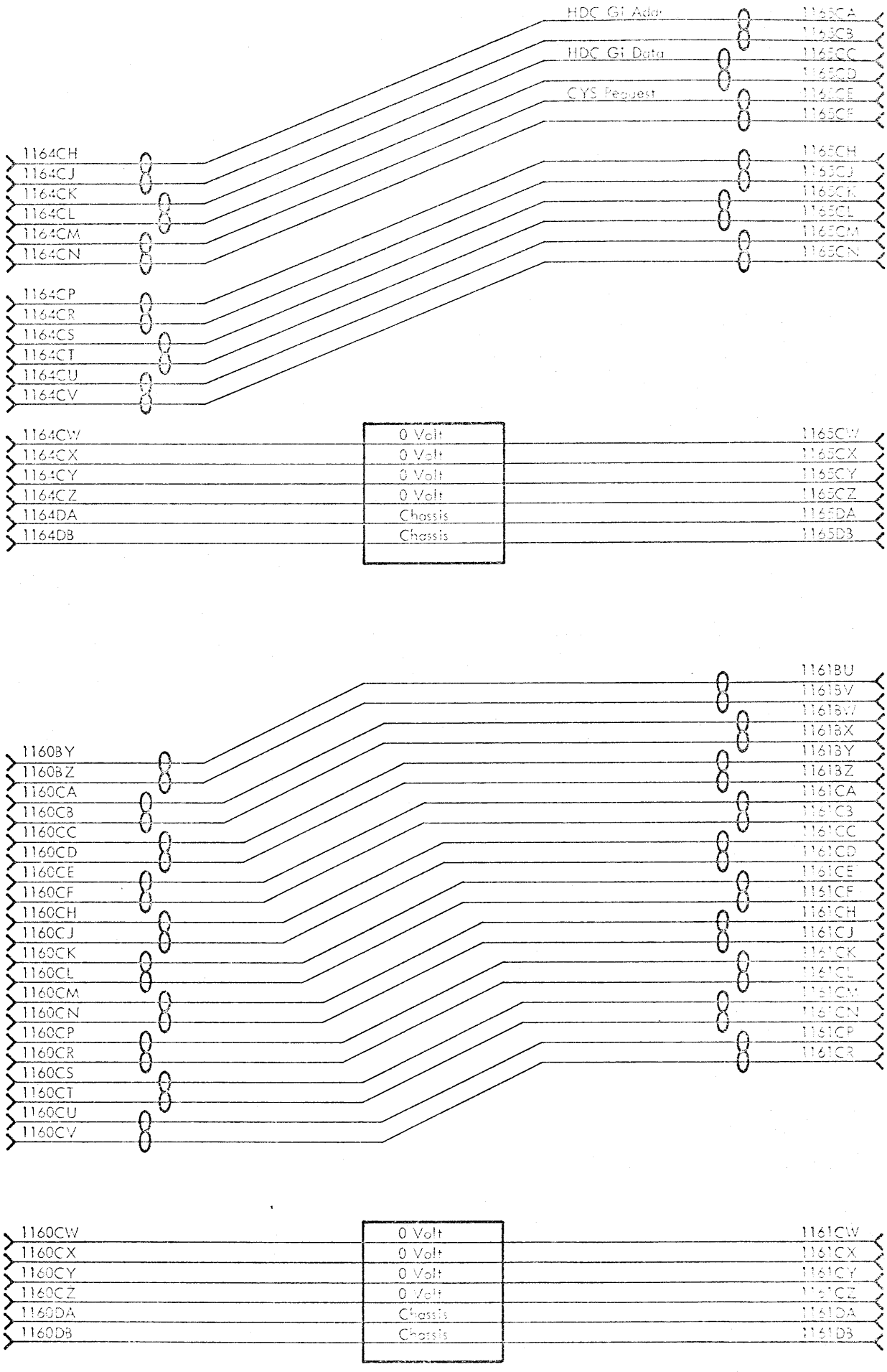

5
DH400
25
26
27
28
23 62J32 Parity Error
28 59L27 Timer Sy
36 92G38 Data Overrun
28 59G38 Wrong 2. Index
5
DH400
29
30
31
32
23 62L27 Drop Out
23 62K28 Address Error
21 80F19 Seek Error
21 80H25 Unit Ready
5
DH401
33
34
35
36
41
23 62L27 Drop Out
23 62J32 Parity Error
28 59G38 Wrong 2. Index
23 62K28 Address Error
32 78E13 -, Power Clear

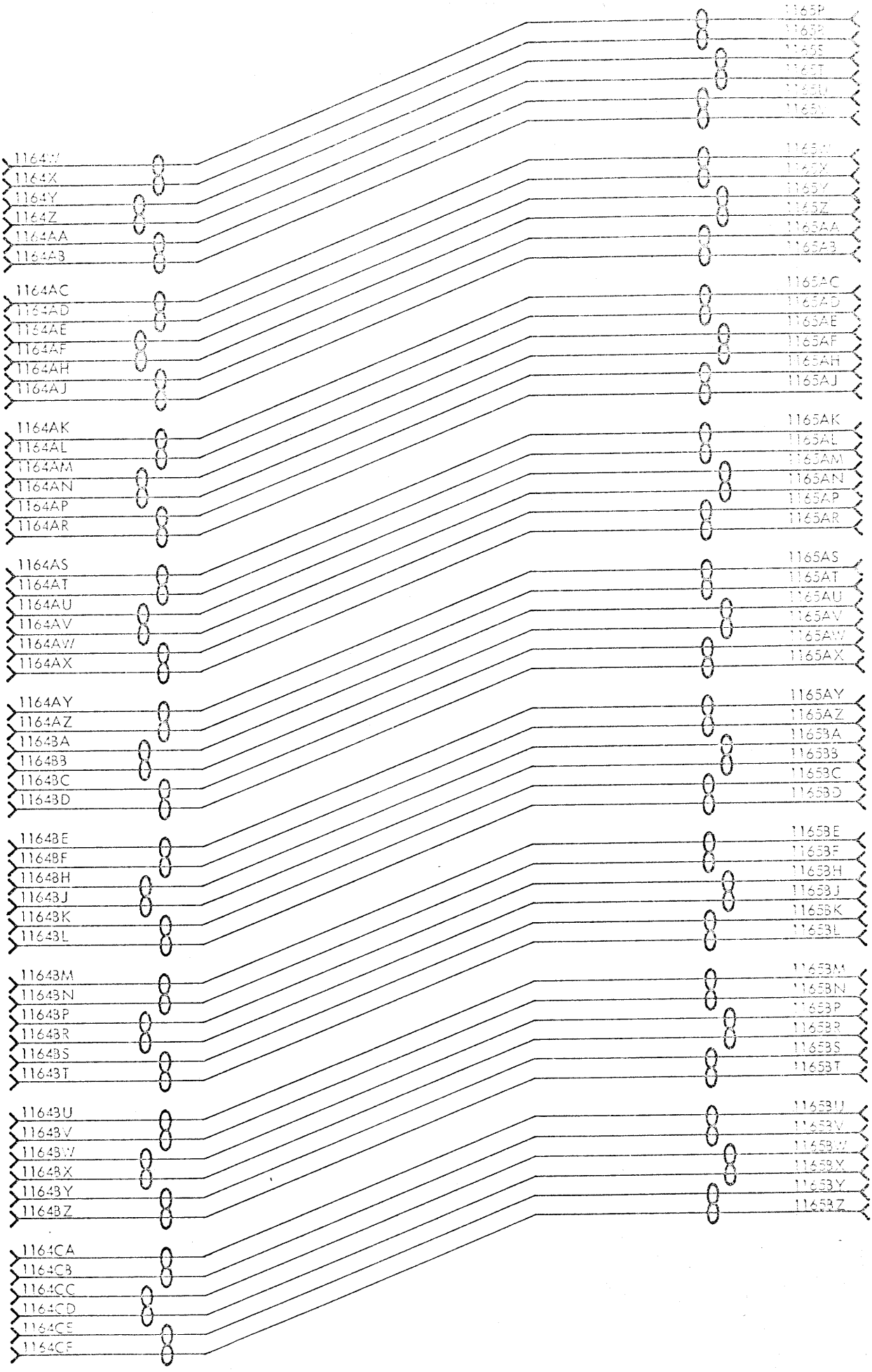

1160H
1160J
33 35D2
33 35-1
10
11
DC405
20
C9
IO BUS(3)
1160K
1160L
33 35E41
33 35-40
12
13
DC405
20
D14
IO BUS(4)
1160M
1160N
33 35F39
33 35-38
16
17
DC405
20
E15
IO BUS(5)
1160P
1160R
33 35G37
33 35-36
18
28
DC405
20
F29
IO BUS(6)
1160S
1160T
33 35H35
33 35-34
31
32
DC405
20
G30
IO BUS(7)
1160U
1160V
33 36A8
33 36-7
33
34
DC405
20
H35
IO BUS(8)
1160W
1160X
33 36B6
33 36-5
37
38
DC405
20
J36
IO BUS(9)
1160Y
1160Z
33 36C4
33 36-3
39
40
DC405
20
K41
IO BUS(10)
1160AA
1160AB
33 36D2
33 36-1
4
5
DC405
21
A3
IO BUS(11)
1160AC
1160AD
33 36E41
33 36-40
6
7
DC405
21
B8
IO BUS(12)
1160AE
1160AF
33 36F39
33 36-38
10
11
DC405
21
C9
IO BUS(13)
1160AH
1160AJ
33 36G37
33 36-36
12
13
DC405
21
D14
IO BUS(14)


1160AK
1160AL
16
17
DC405
21
E15
IO BUS(15)
1160AM
1160AN
18
28
DC405
21
F29
IO BUS(16)
1160AP
1160AR
31
32
DC405
21
G30
IO BUS(17)
1160AS
1160AT
33
34
DC405
21
H35
IO BUS(18)
1160AU
1160AV
37
38
DC405
21
J36
IO BUS(19)
1160AW
1160AX
39
40
DC405
21
K41
IO BUS(20)
1160AY
1160AZ
4
5
DC405
22
A3
IO BUS(21)
1160BA
1160BB
6
7
DC405
22
B8
IO BUS(22)
1160BC
1160BD
10
11
DC405
22
C9
IO BUS(23)
1160BH
1160BJ
1161BH
1161BJ
12
13
DC405
22
D14
IO Address
1160BK
1160BL
1161BK
1161BL
16
17
DC405
22
E15
IO Activate
1160BM
1160BN
1161BM
1161BN
18
DC405
22
F29
IO Transfer
18
452
71
P17 = IO Transfer
1160BE
1160BF
1161BE
1161BF


1162A HDC BUS Out(0)
1162B
1163A
1163B
31
32
DC405
22
G30
HS BUS(0)
1162C HDC BUS Out(1)
1162D
1163C
1163D
33
34
DC405
22
H35
HS BUS(1)
1162E HDC BUS Out(2)
1162F
1163E
1163F
37
38
DC405
22
J36
HS BUS(2)
1162H HDC BUS Out(3)
1162J
1163H
1163J
39
40
DC405
22
K41
HS BUS(3)
1162K HDC BUS Out(4)
1162L
1163K
1163L
4
5
DC405
23
A3
HS BUS(4)
1162M HDC BUS Out(5)
1162N
1163M
1163N
6
7
DC405
23
B8
HS BUS(5)
1162P HDC BUS Out(6)
1162R
1163P
1163R
10
11
DC405
23
C9
HS BUS(6)
1162S HDC BUS Out(7)
1162T
1163S
1163T
12
13
DC405
23
D14
HS BUS(7)
1162U HDC BUS Out(8)
1162V
1163U
1163V
16
17
DC405
23
E15
HS BUS(8)
1162W HDC BUS Out(9)
1162X
1163W
1163X
18
28
DC405
23
F29
HS BUS(9)
1162Y HDC BUS Out(10)
1162Z
1163Y
1163Z
31
32
DC405
23
G30
HS BUS(10)
1162AA HDC BUS Out(11)
1162AB
1163AA
1163AB
33
34
DC405
23
H35
HS BUS(11)


1162AC HDC BUS Out(12)
1162AD
1163AC
1163AD
37
38
DC405
23
J36
HS BUS(12)
1162AE HDC BUS Out(13)
1162AF
1163AE
1163AF
39
40
DC405
23
K41
HS BUS(13)
1162AH HDC BUS Out(14)
1162AJ
1163AH
1163AJ
4
5
DC405
24
A3
HS BUS(14)
1162AK HDC BUS Out(15)
1162AL
1163AK
1163AL
6
7
DC405
24
B8
HS BUS(15)
1162AM HDC BUS Out(16)
1162AN
1163AM
1163AN
10
11
DC405
24
C9
HS BUS(16)
1162AP HDC BUS Out(17)
1162AR
1163AP
1163AR
12
13
DC405
24
D14
HS BUS(17)
1162AS HDC BUS Out(18)
1162AT
1163AS
1163AT
16
17
DC405
24
E15
HS BUS(18)
1162AU HDC BUS Out(19)
1162AV
1163AU
1163AV
18
28
DC405
24
F29
HS BUS(19)
1162AW HDC BUS Out(20)
1162AX
1163AW
1163AX
31
32
DC405
24
G30
HS BUS(20)
1162AY HDC BUS Out(21)
1162AZ
1163AY
1163AZ
33
34
DC405
24
H35
HS BUS(21)
11623A HDC BUS Out(22)
11623B
11633A
11633B
37
38
DC405
24
J36
HS BUS(22)
11623C HDC BUS Out(23)
11623D
11633C
11633D
39
40
DC405
24
K41
HS BUS(23)


HDC Gi Adar
HDC Gi Data
CYS Request
1164CH
1164CJ
1164CK
1164CL
1164CM
1164CN
1164CP
1164CR
1164CS
1164CT
1164CU
1164CV
1165CA
1165CB
1165CC
1165CD
1165CE
1165CF
1165CH
1165CJ
1165CK
1165CL
1165CM
1165CN
1164CW
1164CX
1164CY
1164CZ
1164DA
1164DB
0 Volt
0 Volt
0 Volt
0 Volt
Chassis
Chassis
1165CW
1165CX
1165CY
1165CZ
1165DA
1165DB
1160BY
1160BZ
1160CA
1160CB
1160CC
1160CD
1160CE
1160CF
1160CH
1160CJ
1160CK
1160CL
1160CM
1160CN
1160CP
1160CR
1160CS
1160CT
1160CU
1160CV
1161BU
1161BV
1161BW
1161BX
1161BY
1161BZ
1161CA
1161CB
1161CC
1161CD
1161CE
1161CF
1161CH
1161CJ
1161CK
1161CL
1161CM
1161CN
1161CP
1161CR
1160CW
1160CX
1160CY
1160CZ
1160DA
1160DB
0 Volt
0 Volt
0 Volt
0 Volt
Chassis
Chassis
1161CW
1161CX
1161CY
1161CZ
1161DA
1161DB


1164W
1164X
1164Y
1164Z
1164AA
1164AB
1164AC
1164AD
1164AE
1164AF
1164AH
1164AJ
1164AK
1164AL
1164AM
1164AN
1164AP
1164AR
1164AS
1164AT
1164AU
1164AV
1164AW
1164AX
1164AY
1164AZ
1164BA
1164BB
1164BC
1164BD
1164BE
1164BF
1164BH
1164BJ
1164BK
1164BL
1164BM
1164BN
1164BP
1164BR
1164BS
1164BT
1164BU
1164BV
1164BW
1164BX
1164BY
1164BZ
1164CA
1164CB
1164CC
1164CD
1164CE
1164CF
1165P
1165R
1165S
1165T
1165U
1165V
1165W
1165X
1165Y
1165Z
1165AA
1165AB
1165AC
1165AD
1165AE
1165AF
1165AH
1165AJ
1165AK
1165AL
1165AM
1165AN
1165AP
1165AR
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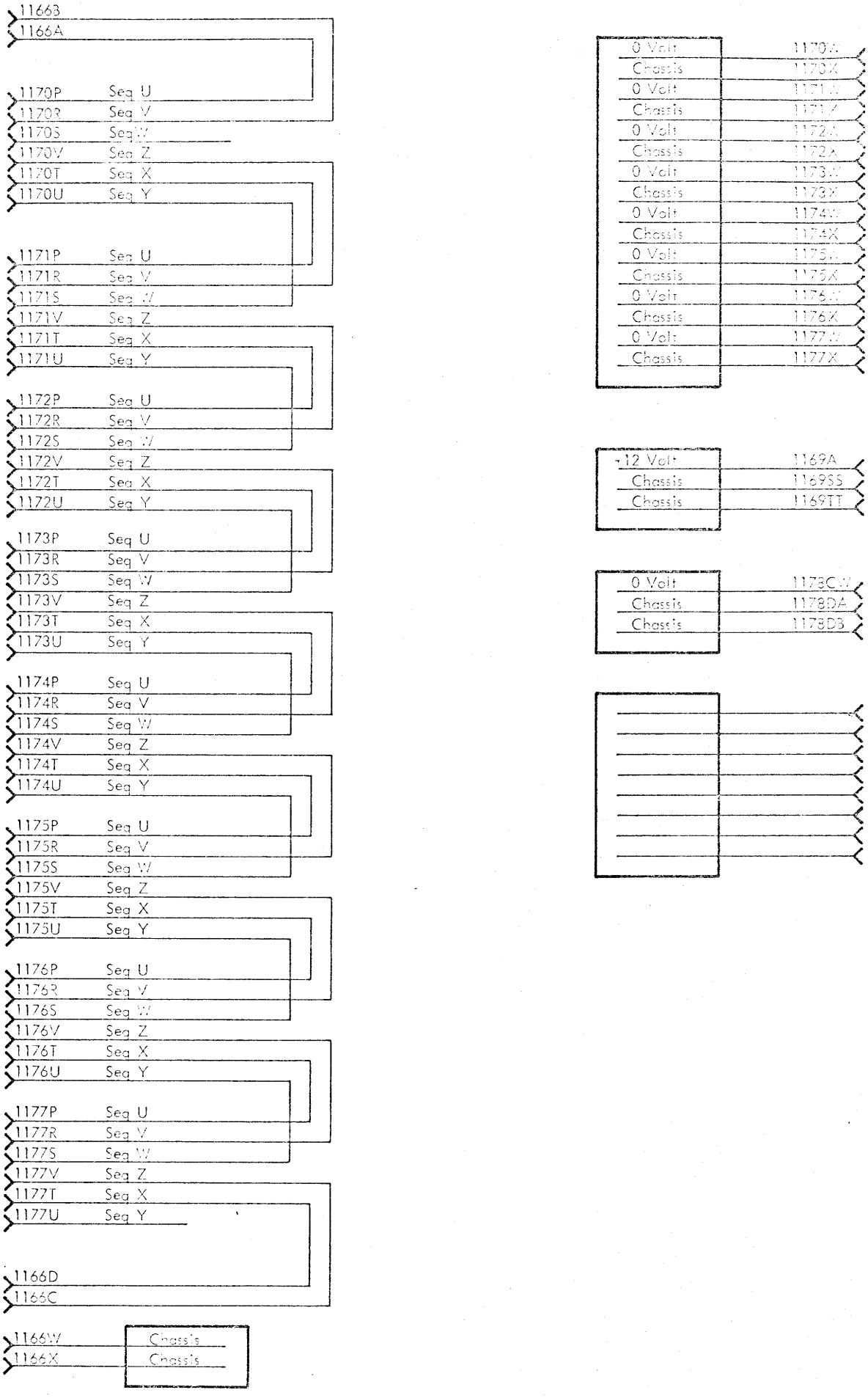
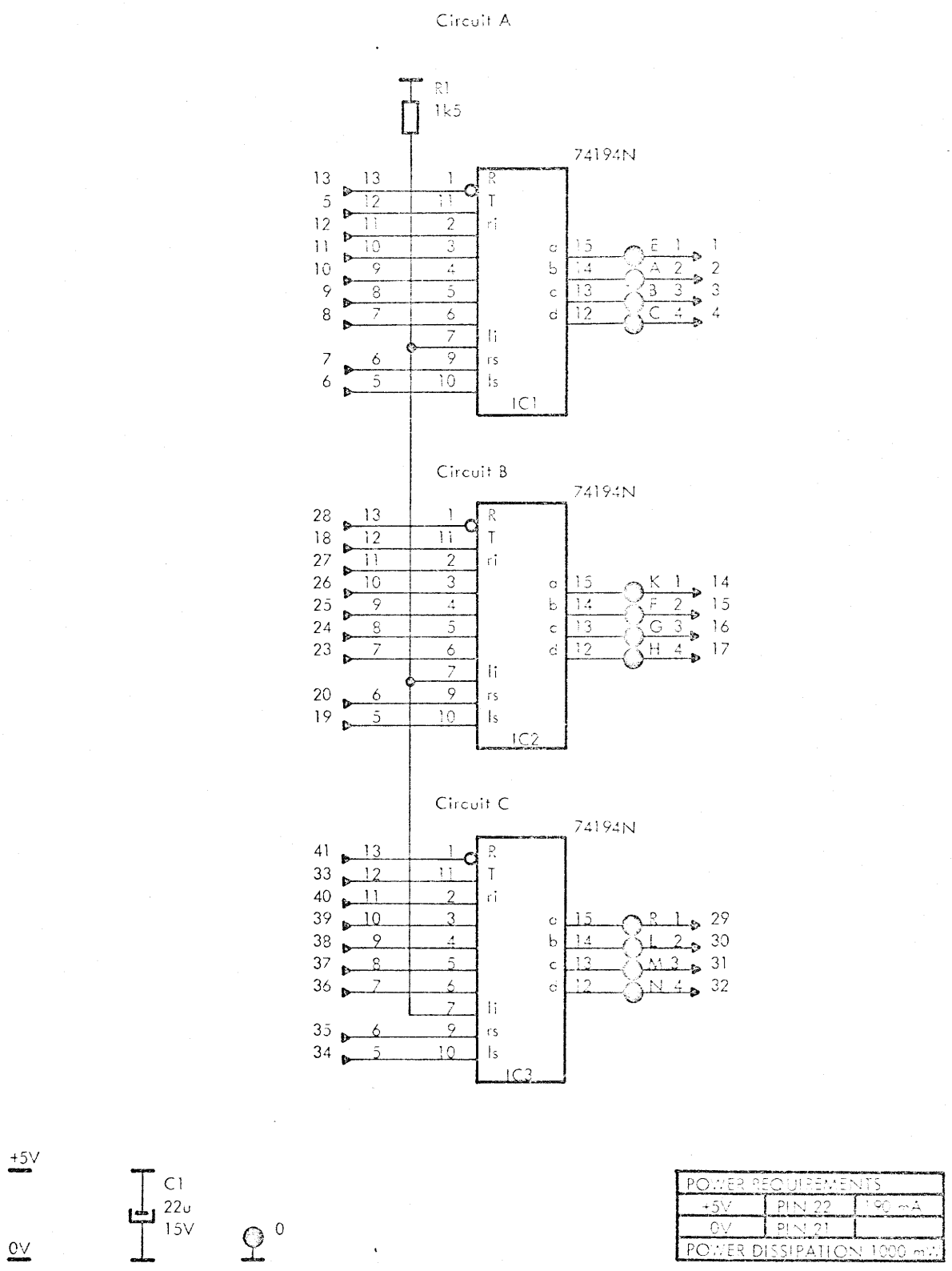
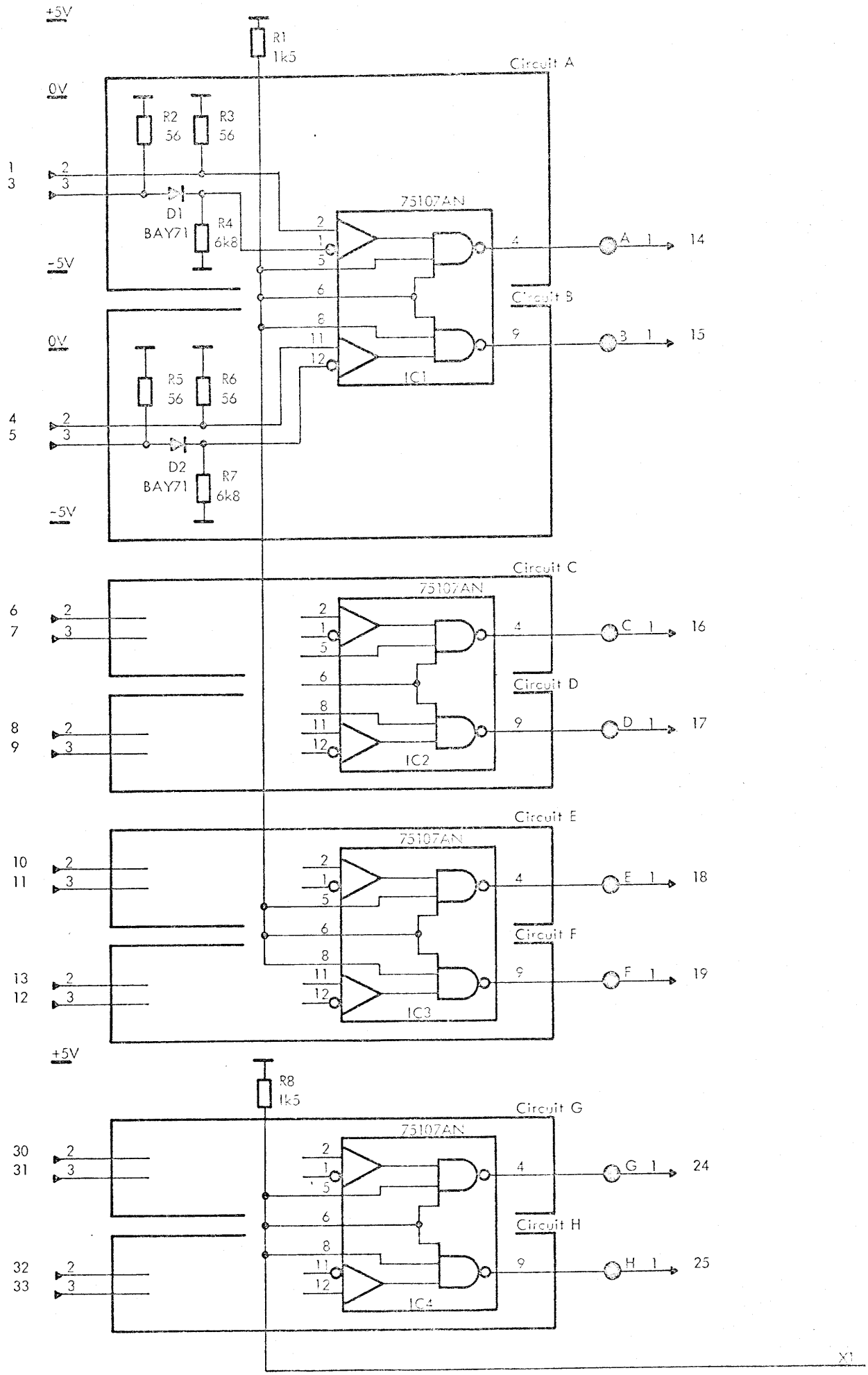
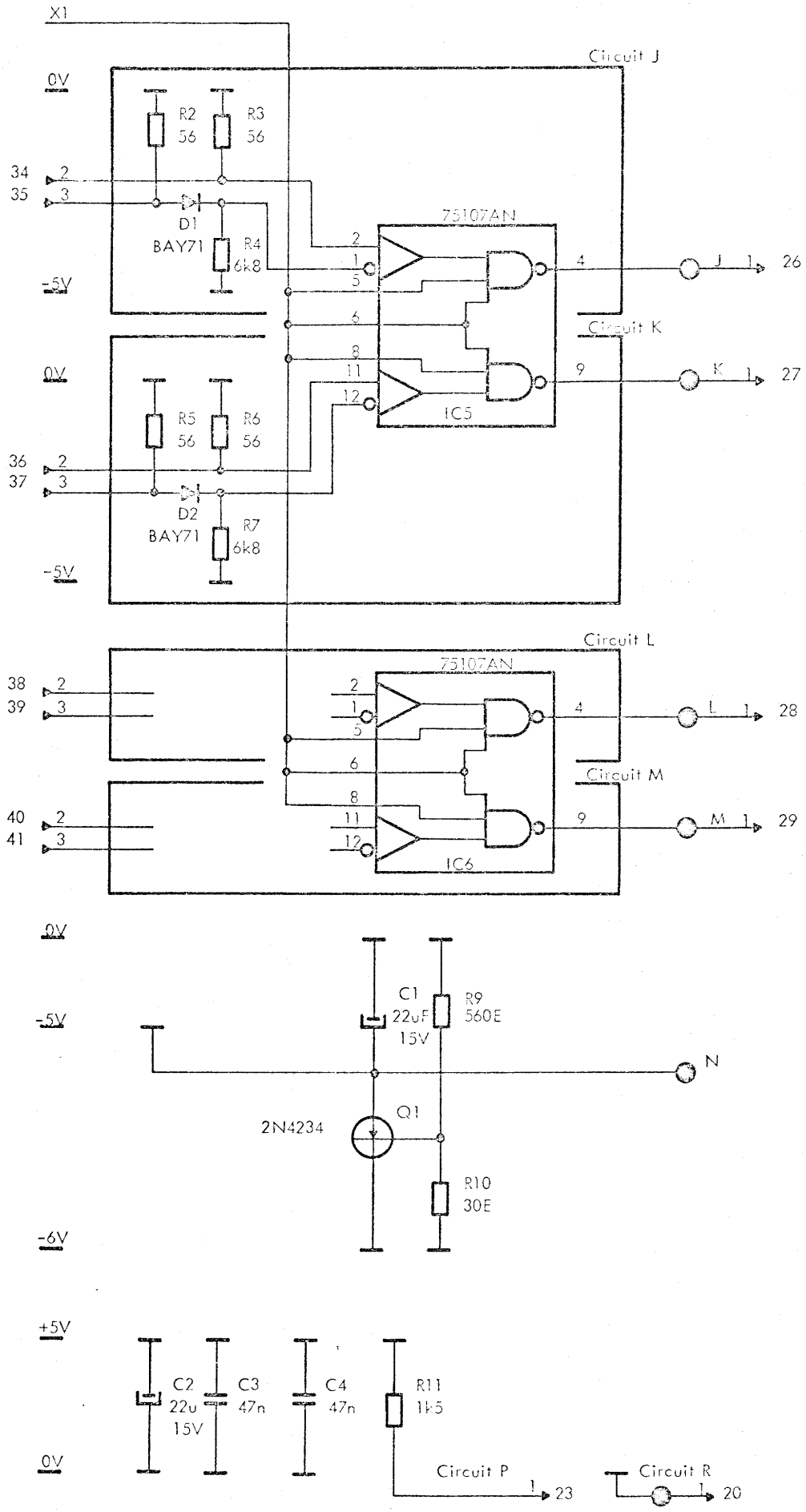
1165BY
1165BZ


1166B
1166A
1170P Seq U
1170R Seq V
1170S Seq W
1170V Seq Z
1170T Seq X
1170U Seq Y
1171P Seq U
1171R Seq V
1171S Seq W
1171V Seq Z
1171T Seq X
1171U Seq Y
1172P Seq U
1172R Seq V
1172S Seq W
1172V Seq Z
1172T Seq X
1172U Seq Y
1173P Seq U
1173R Seq V
1173S Seq W
1173V Seq Z
1173T Seq X
1173U Seq Y
1174P Seq U
1174R Seq V
1174S Seq W
1174V Seq Z
1174T Seq X
1174U Seq Y
1175P Seq U
1175R Seq V
1175S Seq W
1175V Seq Z
1175T Seq X
1175U Seq Y
1176P Seq U
1176R Seq V
1176S Seq W
1176V Seq Z
1176T Seq X
1176U Seq Y
1177P Seq U
1177R Seq V
1177S Seq W
1177V Seq Z
1177T Seq X
1177U Seq Y
1166D
1166C
1166W Chassis
1166X Chassis
0 Volt 1170W
Chassis 1170X
0 Volt 1171W
Chassis 1171X
0 Volt 1172W
Chassis 1172X
0 Volt 1173W
Chassis 1173X
0 Volt 1174W
Chassis 1174X
0 Volt 1175W
Chassis 1175X
0 Volt 1176W
Chassis 1176X
0 Volt 1177W
Chassis 1177X
+12 Volt 1169A
Chassis 1169SS
Chassis 1169TT
0 Volt 1178CW
Chassis 1178DA
Chassis 1178DB

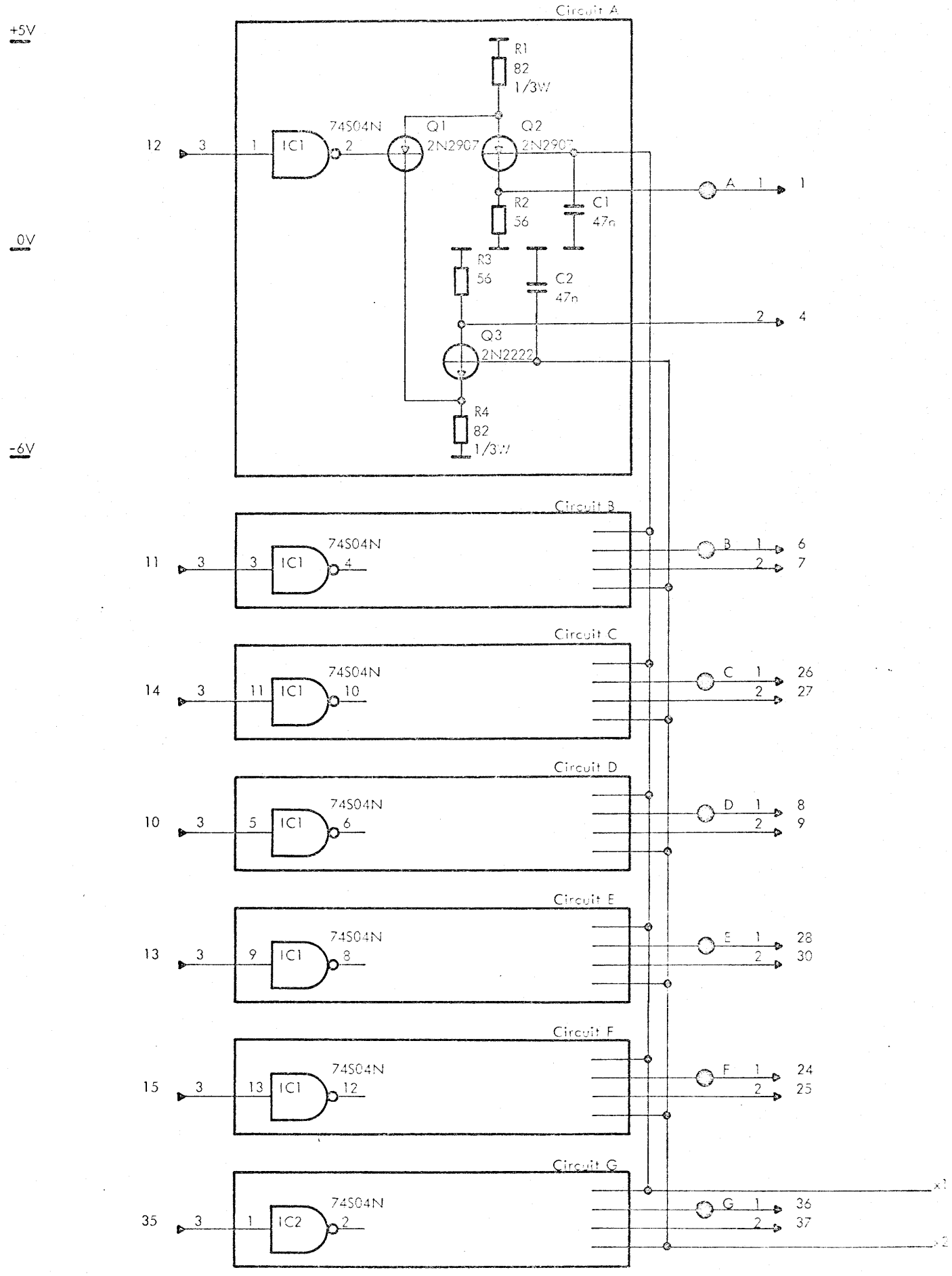


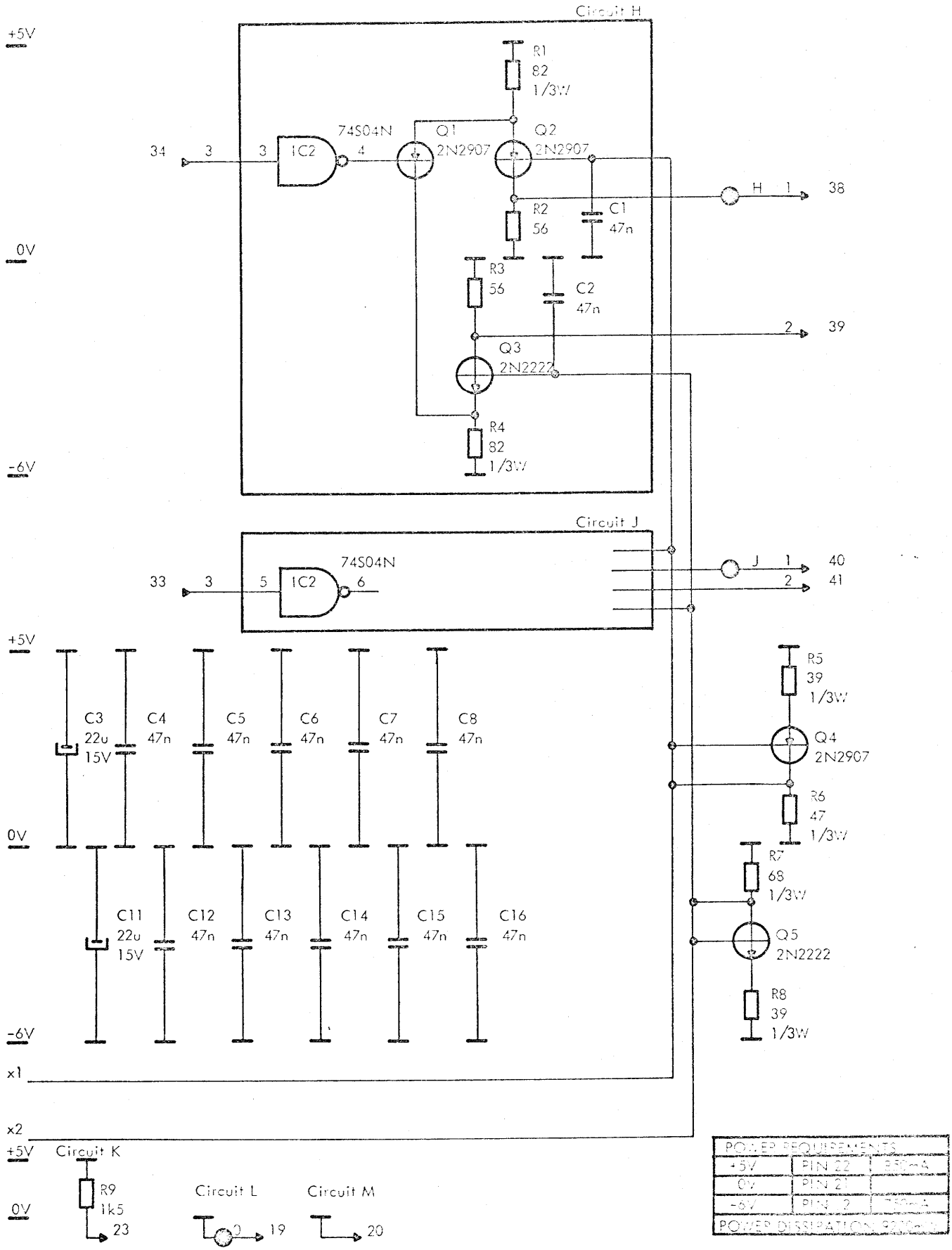
POWER REQUIREMENTS		
+5V	PIN 22	190 mA
0V	PIN 21	
POWER DISSIPATION 1000 mW		

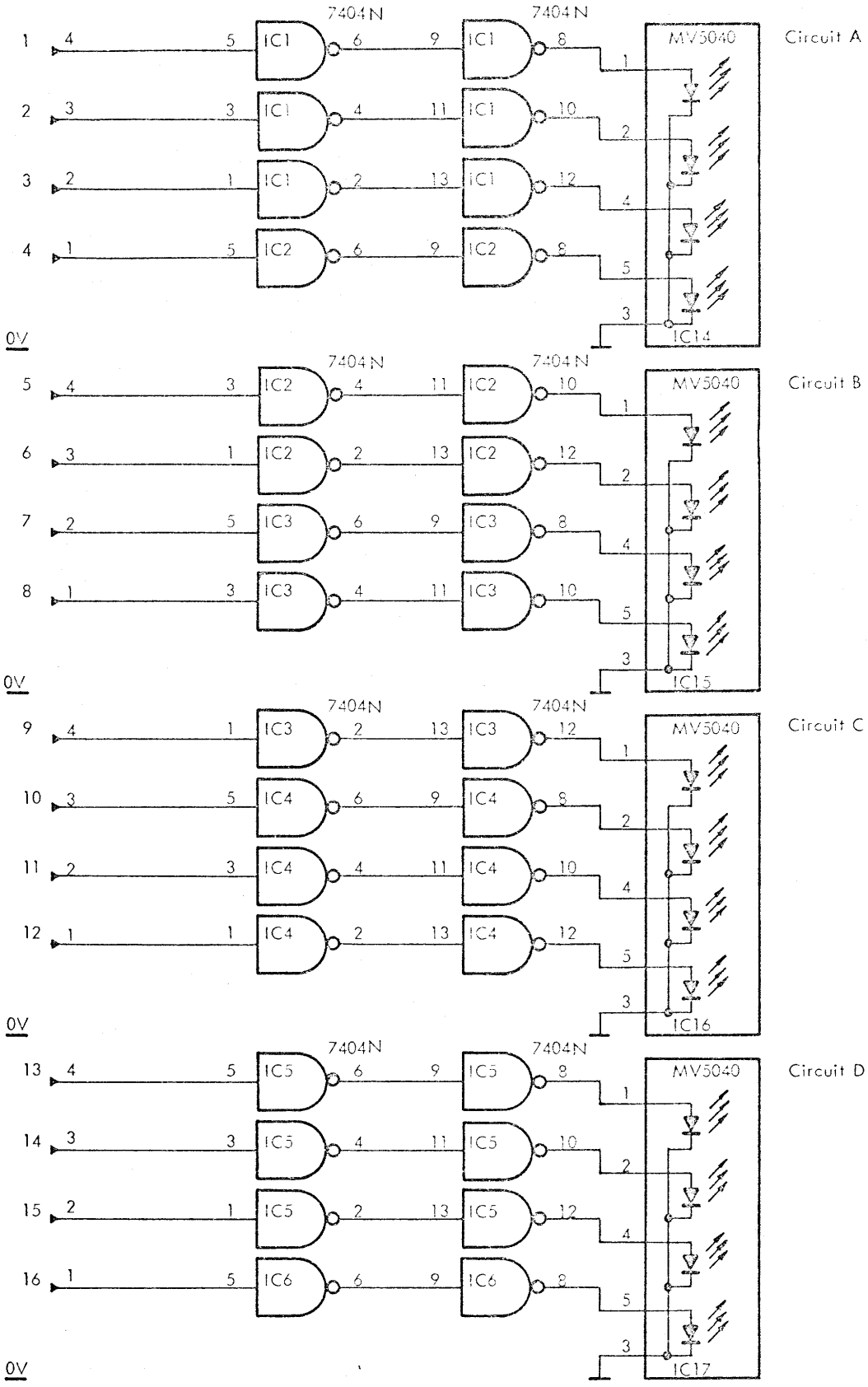

+5V
R1
1k5
Circuit A
0V
R2
56
R3
56
1
2
3
D1
BAY71
R4
6k8
-5V
75107AN
2
1
5
6
4
A 1
14
Circuit B
0V
8
11
12
9
3 1
15
IC1
R5
56
R6
56
4
2
3
5
D2
BAY71
R7
6k8
-5V
Circuit C
6
2
7
3
75107AN
2
1
5
6
4
C 1
16
Circuit D
8
2
9
3
8
11
12
9
D 1
17
IC2
Circuit E
10
2
11
3
75107AN
2
1
5
6
4
E 1
18
Circuit F
13
2
12
3
8
11
12
9
F 1
19
IC3
+5V
R8
1k5
Circuit G
30
2
31
3
75107AN
2
1
5
6
4
G 1
24
Circuit H
32
2
33
3
8
11
12
9
H 1
25
IC4
X1

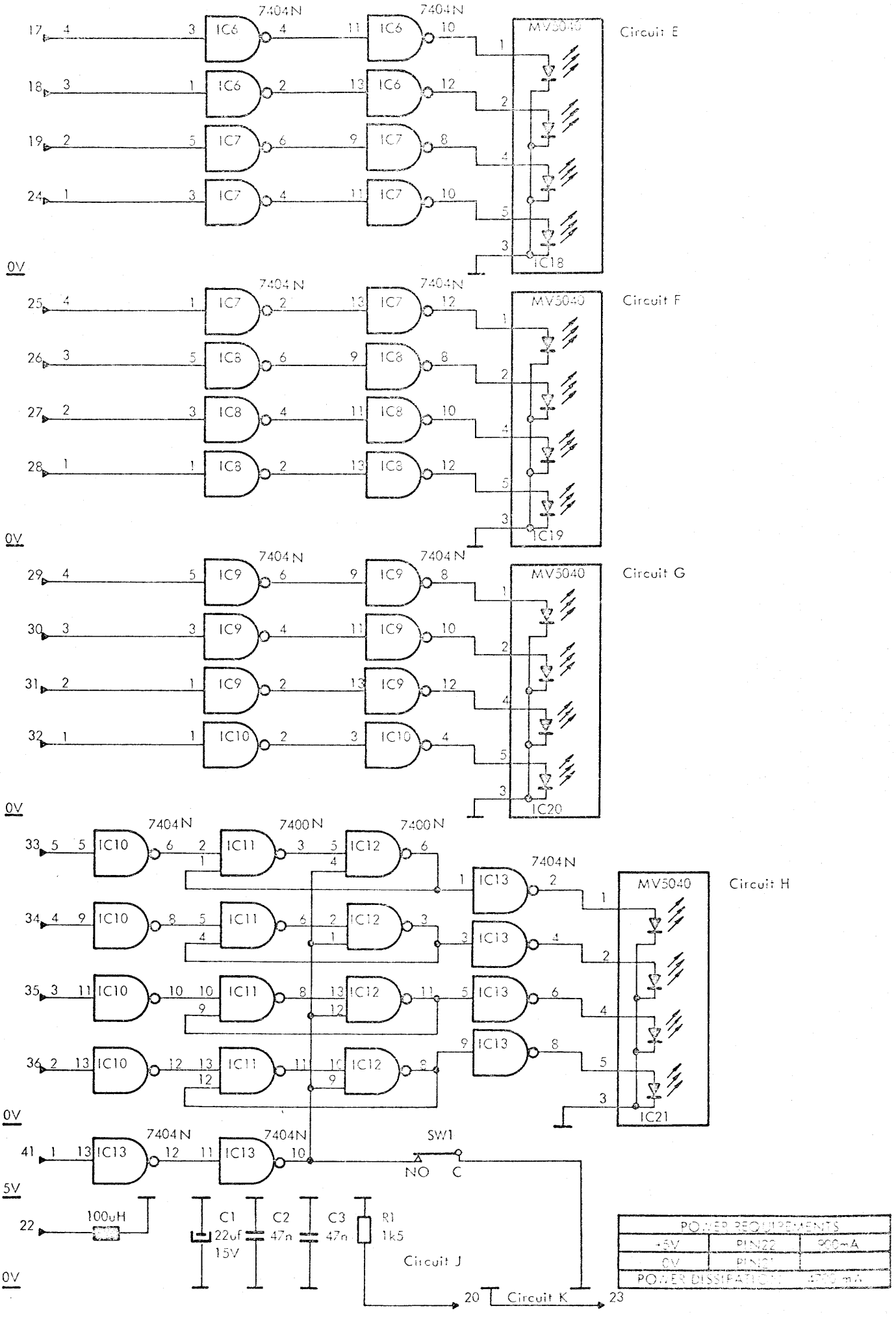


POWER REQUIREMENTS		
+5V	PIN 22	130mA
0V	PIN 21	
-6V	PIN 2	45mA
POWER DISSIP		1625mW

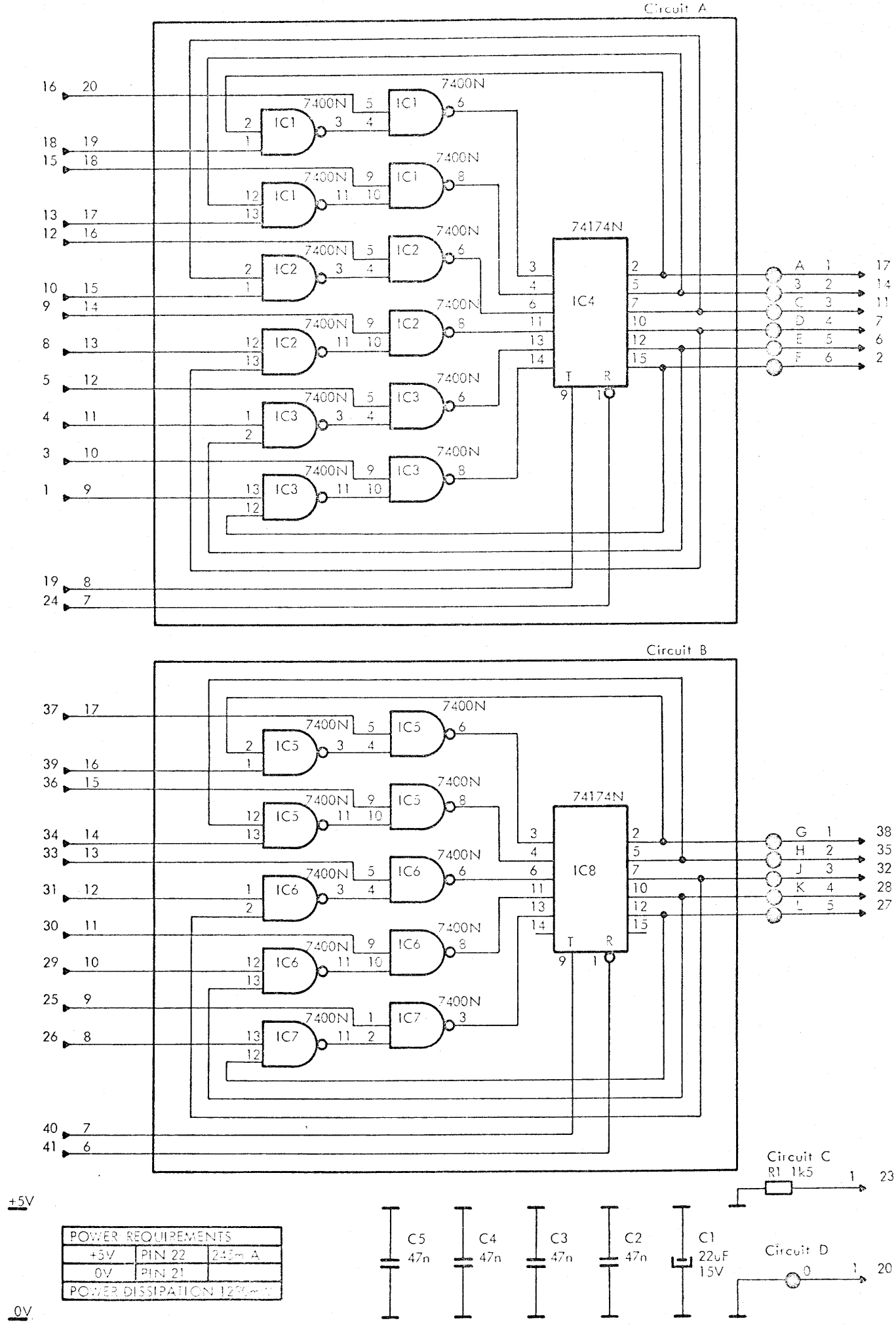

+5V
0V
-6V
Circuit A
R1
82
1/3W
74S04N
IC1
Q1
2N2907
Q2
2N2907
R2
56
C1
47n
R3
56
C2
47n
Q3
2N2222
R4
82
1/3W
12
3
1
2
A 1
1
2
4
Circuit B
11
3
3
4
B 1
6
2
7
Circuit C
14
3
11
10
C 1
26
2
27
Circuit D
10
3
5
6
D 1
8
2
9
Circuit E
13
3
9
8
E 1
28
2
30
Circuit F
15
3
13
12
F 1
24
2
25
Circuit G
35
3
1
IC2
2
G 1
36
2
37


Circuit H
+5V
0V
-6V
R1
82
1/3W
74S04N
IC2
Q1
2N2907
Q2
2N2907
34
3
3
4
H 1
38
R2
56
C1
47n
R3
56
C2
47n
2
39
Q3
2N2222
R4
82
1/3W
Circuit J
74S04N
IC2
33
3
5
6
J 1
40
2
41
+5V
0V
-6V
C3
22u
15V
C4
47n
C5
47n
C6
47n
C7
47n
C8
47n
C11
22u
15V
C12
47n
C13
47n
C14
47n
C15
47n
C16
47n
R5
39
1/3W
Q4
2N2907
R6
47
1/3W
R7
68
1/3W
Q5
2N2222
R8
39
1/3W
x1
x2
+5V
0V
Circuit K
R9
1k5
23
Circuit L
19
Circuit M
20
POWER REQUIREMENTS
+5V
PIN 22
0V
PIN 21
-6V
PIN 2
POWER DISSIPATION


7404N
7404N
MV5040
Circuit A
IC1
IC14
0V
Circuit B
IC2
IC3
IC15
Circuit C
IC4
IC16
Circuit D
IC5
IC6
IC17



POWER REQUIREMENTS		
+5V	PIN22	900mA
0V	PIN21	
POWER DISSIPATION		4700 mA



POWER REQUIREMENTS		
+5V	PIN 22	245m A
0V	PIN 21	
POWER DISSIPATION 1230m W		

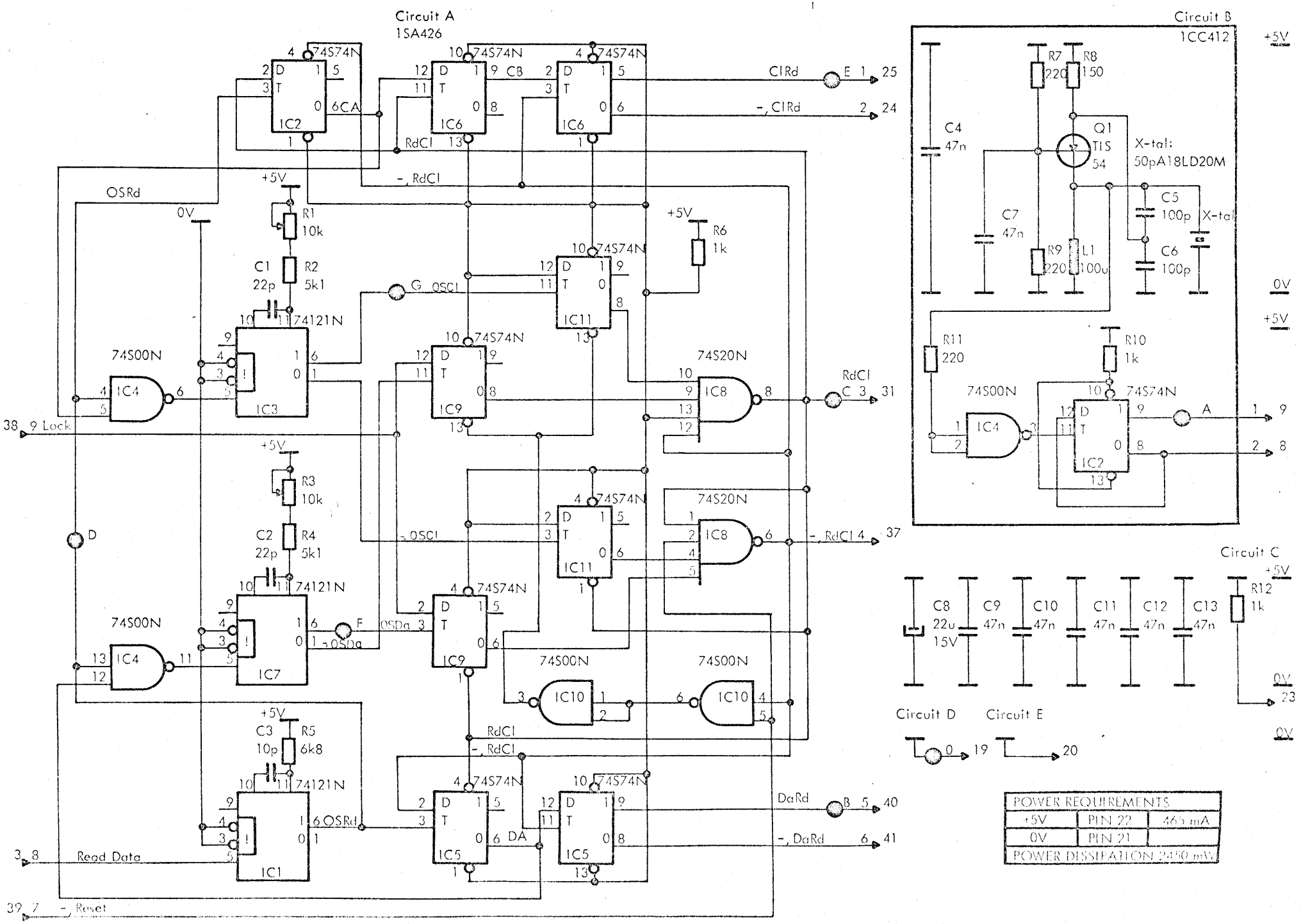
RCLM 400

V13589

1SA426, 1CC412

PCBA Circuit Diagram

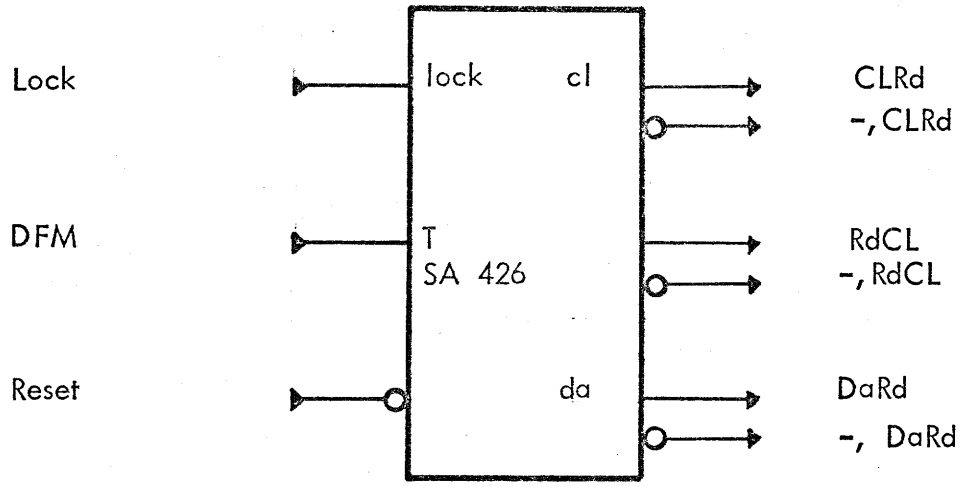
RC2074 - 1



RCSL : 44-RT 598
pp. 1 - 4
Feb. 1973

RCLM 400 DATA SHEET

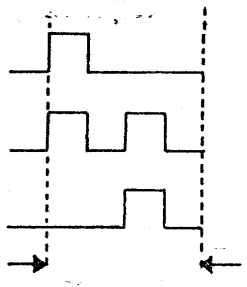
SA 426



CIRCUIT DESCRIPTION

The SA 426 is a 2.5 Mbit/sec readdetector for double freqnency modulated pulse trains. It is capable of detecting three types of "bits", O's, 1's, and * 1's. Their relation to the input pulse train is as follows :

DFM input



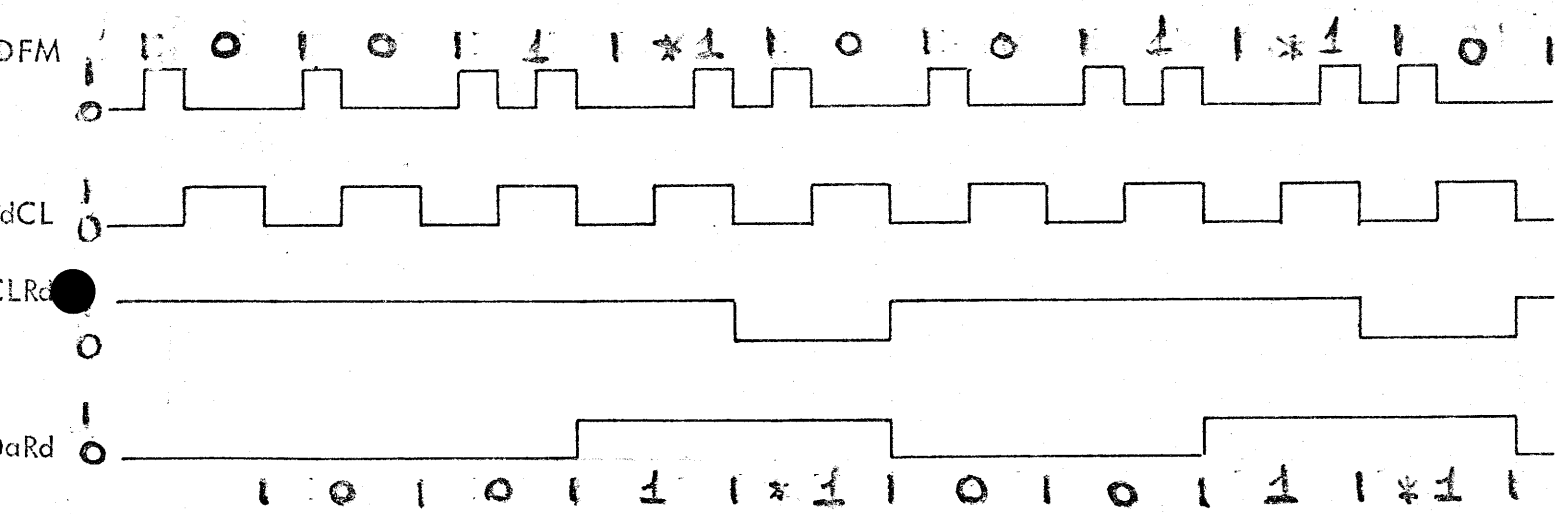
Type	DaRd	CLRD
		1
1	1	1
*1	1	0

bit period = 400ns

The input pulse train is applied to the DFM input .

The readdetector generates a 2.5 MHz , 50% duty cycle bitperiod clock. (RdCL) .Within each bitperiod, the CLRd and DaRd autput defines the type of bit according to the above shown table. The CLRd and DaRd autputs are defined from shortly after the trailing edge of RdCL to the next trailing edge of RdCL.

The autput bit period is delayed approximately 300 ns in relation to the input bit period. A typical sequence may be as follows:



The input Reset clears when low asynchronous the RdCL bistable (RdCL =0) and brings the edgetriggering inputs to this bistable in a well defined initial state.

The input is used to establish a bit period synchronization to a 0's pattern when low. When high, the readdetector keeps synchronization if no pulse- pulse time exceeds 400 ns nominal. In order to keep in synchronization when Lock= 1, a 0- * 1 sequence must be avoided.

The internal working principle of the readdetector is as follows. (Conf. Circuit Diagram V 13589 and Timing Diagram V 13472).

A nominal 100 ns monostable OSRd is triggered at each leading edge of the DFM input.

The state of the RdCl bistable at the raising edge of OSRd determines the classification of the pulse.

If RdCl= O at the OSRd raising edge , the pulse is registered as a "clock" pulse by setting CA= 1.

If RdCL= 1 at the OSRd raising edge , the pulse is registered as a " data " pulse by setting DA = 1.

At the trailing edge of OSRd, one of two nominal 200 ns monostables are triggered (OSCl and OSDa).

If the pulse was registered as a " clock " pulse (CA= 1) , OSCl is triggered.

If the pulse was registered as a " data " pulse (DA = 1), OSDa is triggered.

OSCl and OSDa control together the state of the RdCL bistable.

The RdCL bistable has two edge triggered set inputs and two edge triggered clear inputs.

RdCL is set by the earliest of leading edge OSCl and trailing edge OSDa.

RdCL is cleared by the earliest of trailing edge OSCl and leading edge OSDa.

When lock= O the set - clear inputs from OSDa are inhibited. RdCL is then only controlled by OSCl.

The RdCL and -, RdCL is furthermore used for clocking the CA and DA information into buffers (CB, CLRd and DaRd).

ADJUSTMENT PROCEDURE .

The readdetector may be adjusted off-line as follows.
A 5 MHz clock is applied to the DFM input. Lock= 1 .
The readdetector is reset by shortly applying a 0 to the Reset input.The monostables OSC1 (test point G) and OSDa (test point F) is first adjusted to approximate 250 ns.
RdCL (test point C) is monitored on the scope and the OSC1 time (test point G) Is decreased until it just begins to move the trailing edge of RdCL.
In the same way the OSDa time (test point F) is decreased until it just begins to move the leading edge of RdCL.
Finally check , that OSRd leading edge (test pnt. D) fall approxmately in the middle of each RdCL half period. To obtain this, the OSRd should be approximately 6o ns wide.

D-h

Fredag d. 15.11.74

Kl 9 00

A/S REGNECENTRALEN

HOVEDVEJEN 9 — DK 2600 GLOSTRUP

CABLES: indudatamat - TELEX: 154 68 rc dk - PHONE (01) 96 53 66

Date : September 1974

udført SP

TITLE : FIELD CHANGE ORDER No. 4032

APPLICABLITY : Disc File Controller type RC 4818 C, model DFC 403. Field change must be executed on units with S/N below 98267.

CLASSIFICATION : Mandatory, warranty.

SCOPE : During write operations a data overrun situation may cause destruction of a word in the output area in the core store. This is due to the fact that data overrun terminates the operation resting bit 23 on the HDC at "zero". A pending cys call may now cause the fatal transport. The present modification will rest HDC 23 at "one" after termination.

DOCUMENTATION ENCLOSED :

DFC 403 logic diagrams, revised page 20B and page 31.
List of wiring changes.

PARTS REQUIRED : 6 wrap pins,
3 m wrap wire.

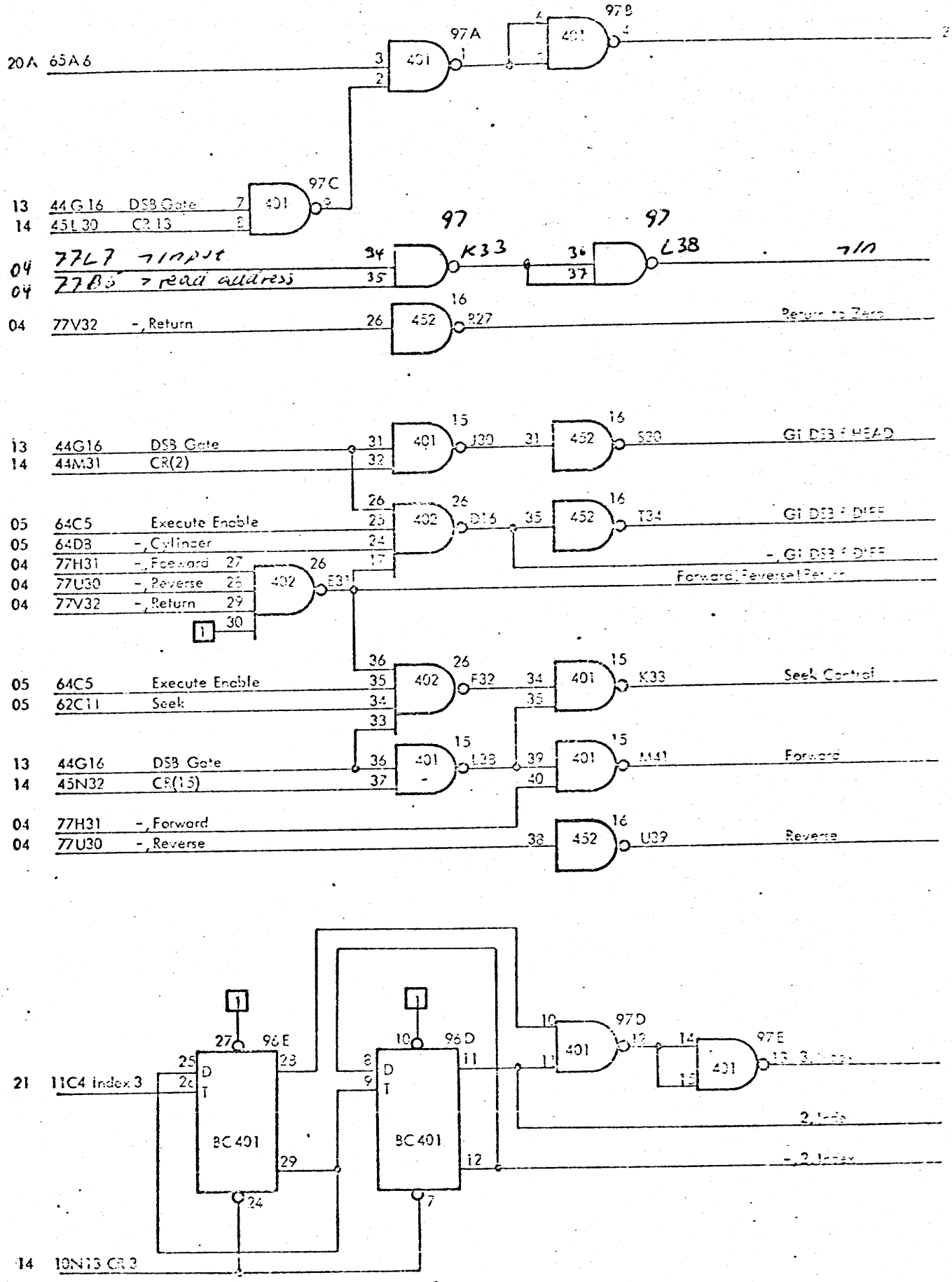
FIELD INSTRUCTION : Normal testrun plus test of read and write address should be performed when the FCO has been made.

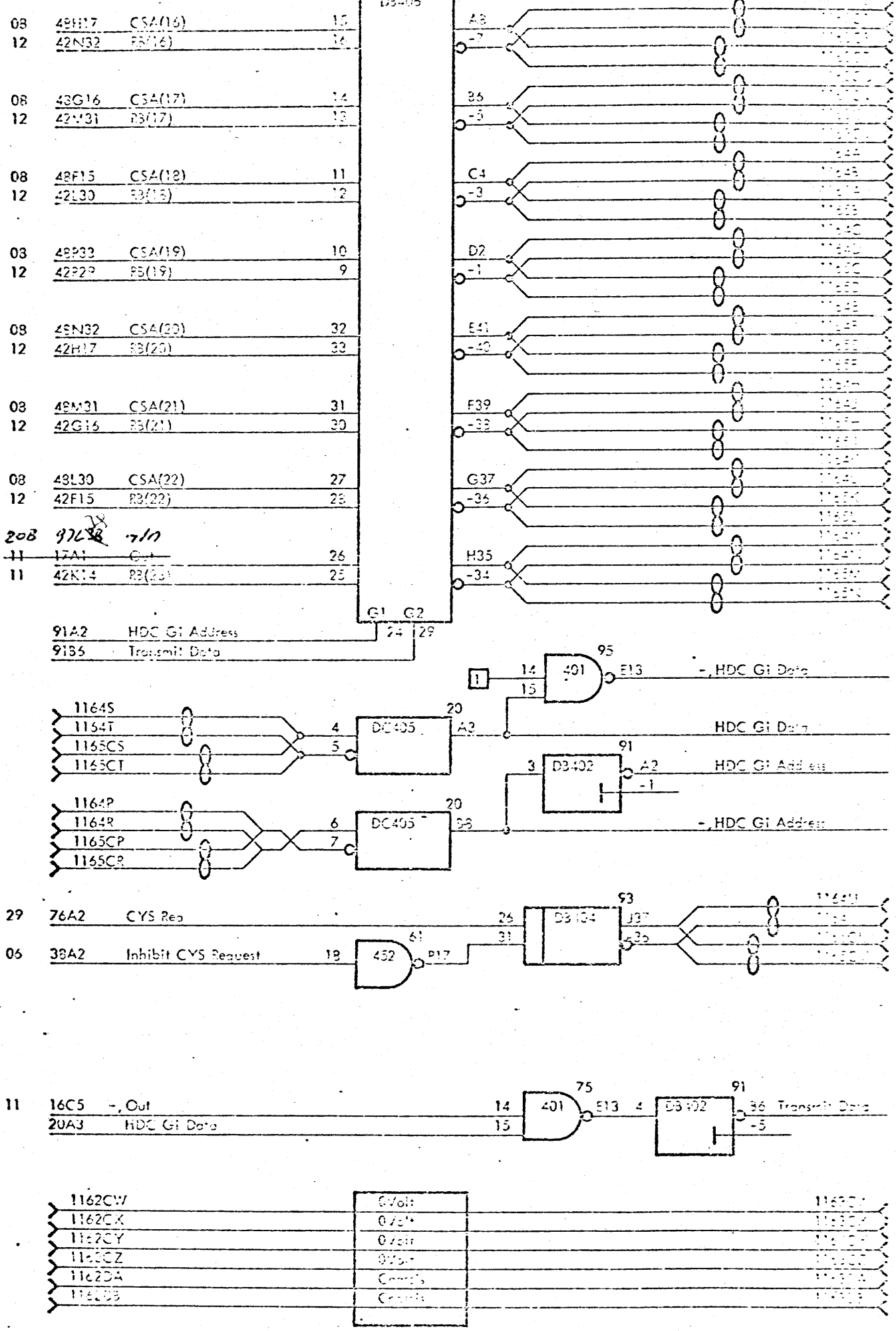
TIME REQUIRED : 1 hour.

A/S Regnecentralen

Per Hansen

Per Hansen


20A 65A6
97A
97B
97C
13 44G16 DSB Gate
14 45L30 CR13
04 77L7 →input
04 77B5 → read address
97
K33
97
L38
→IN
04 77V32 -, Return
Return to Zero
13 44G16 DSB Gate
14 44M31 CR(2)
Gi DSB ↑ HEAD
05 64C5 Execute Enable
05 64D8 -, Cylinder
04 77H31 -, Forward
04 77U30 -, Reverse
04 77V32 -, Return
Gi DSB ↑ DIFF
-, Gi DSB ↑ DIFF
Forward/Reverse/Return
05 64C5 Execute Enable
05 62C11 Seek
Seek Control
13 44G16 DSB Gate
14 45N32 CR(15)
Forward
04 77H31 -, Forward
04 77U30 -, Reverse
Reverse
21 11C4 Index 3
96E
96D
97D
97E
BC401
BC401
2, Index
-2, Index
14 10N13 CR3


08 48H17 CSA(16) 15
12 42N32 FB(16) 16
08 48G16 CSA(17) 14
12 42M31 FB(17) 13
08 48F15 CSA(18) 11
12 42L30 FB(18) 12
08 48P33 CSA(19) 10
12 42P29 FB(19) 9
08 48N32 CSA(20) 32
12 42H17 FB(20) 33
08 48M31 CSA(21) 31
12 42G16 FB(21) 30
08 48L30 CSA(22) 27
12 42F15 FB(22) 28
208 97C8 -7/0
11 17A1 Out 26
11 42K14 FB(23) 25
A8 -7
B6 -5
C4 -3
D2 -1
E41 -40
F39 -38
G37 -36
H35 -34
G1 G2
24 29
91A2 HDC GI Address
91B6 Transmit Data
95
401
E13
-, HDC GI Data
1164S
1164T
1165CS
1165CT
4
5
DC405
20
A3
HDC GI Data
91
DB402
A2
-1
3
HDC GI Address
1164P
1164R
1165CP
1165CR
6
7
DC405
20
B6
-, HDC GI Address
29 76A2 CYS Req
06 38A2 Inhibit CYS Request
18
452
61
P17
93
DB104
26
31
11 16C5 -, Out
20A3 HDC GI Data
14
15
75
401
E13
4
DB402
91
B6 Transmit Data
-5
1162CW
1162CX
1162CY
1162CZ
1162DA
1162DB
0 Volt
0 Volt
Ground
Ground

XX = TWISTED PAIR

A/S REGNECENTRALEN Modification formular Hardwaredocumentation UNIT: DFC 403 Designed PEH / BZH

Signal name	Wire description on input- and/or outputform									In	Out	Executed
	(16-6)	(17-1)	(14-35)	(42-6)	(41-6)	(41-19)	(40-19)	(41-34)	(40-34)		X	
	(40-34)	(34-26) XX	(89-28)								X	
	(16-6)	(17-1)	(14-35)	(42-6)	(41-6)	(41-19)	(40-19)	(40-34)	(40-34)	X		
	(40-34) XX	(89-28)								X		
V	(97-38) XX	(34-26)								X		
V	(97-36)	(97-33)	(97-37)							X		
	(10-7) XX	(77-1)	(18-26)								X	
	(10-7) XX	(77-1)	(97-34) XX	(18-36)						X		
	(10-2)	(18-34)	(77-5)	(75-11)	(71-36)						X	
	(10-2)	(18-31)	(77-5)	(75-11)	(71-36)	(97-35)				X		