DCC 701

REFERENCE MANUAL

Abstract: This paper describe the logical structure of the disk cartridge controller for the CPU 702 processor.

CONTENTS

1. MAIN DESCRIPTION

A disk cartridge drive is connected to the CPU bus via a disk
cartridge adaptor and the disk cartridge controller DCC 701.
The DCC 701 is placed in chassis CHS 701.
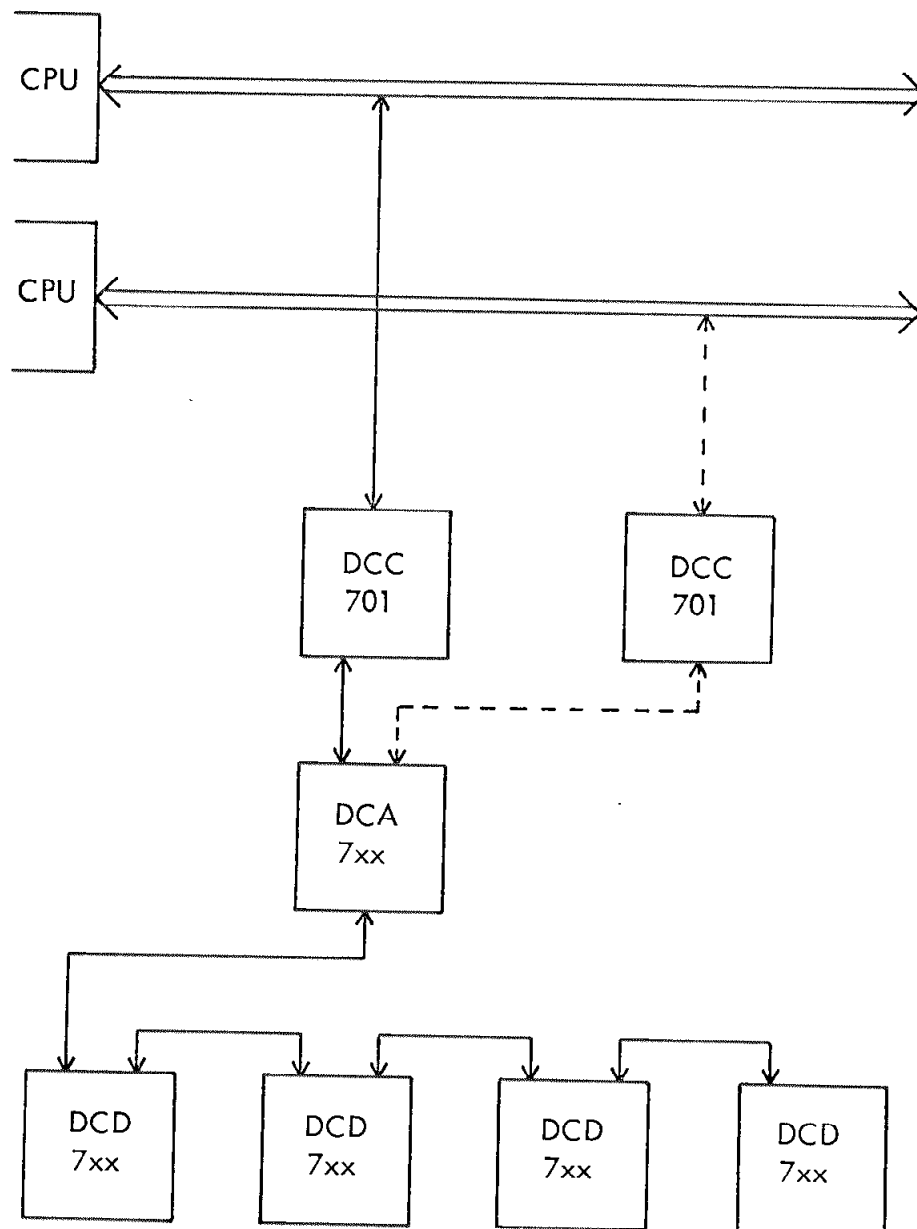
2. OPERATIONAL LIMITS

A DCD 701 can handle max. :

2.1 4 disk drive units.

2.2 32 heads pr. unit.

2.3 16 sectors pr. track.

2.4 256 cylinders.

2.5 The core address range is 32K words of 16 bit.

2.6 1.6 MHz bit rate.

3. HARDWARE DESCRIPTION

The disk cartridge controller DCC 701 has three major logic groups.

3.1 The input/output section receive instructions from the RC 7000 processor and manipulate and destribute them to the register and timing section.

3.2 The register section is an input/output data storage medium in which the data from/to the disk is converted from/to serial to/from parallel.

Data is information read or written on the disk. Data is also the disk channel status and core address for the disk data. There are two types of status; operational status e.g. contents of unit, head, sector and sector count register's, and error status. (Described in the logic structure section.)

3.3 The timing section produce control signals from signals received from input/output section, register section, and the disk cartridge adaptor 7XX. The control signals again are distributed to the above mentioned circuits.

3.4 Adaptor interface signals.

The interface signals between DCC 701 and the disk cartridge adaptor are listed in the technical manual.

4. LOGIC DESCRIPTION

4.1 Program control of the DCD 701 is provided through six I/O instructions. Busy and Done are controlled and sensed in I/O instruction with device code 73 (octal).

Interrupt disable is controlled by interrupt priority mask bit 7.

Start will set Busy and clear Done. The Clear function will clear Busy and Done. Done will be set by checkword error and this again clear Busy. Read/write Done will set Done and clear Busy.

Iorst clear Done and Busy and all the register's. Power start up perform the same operation.

The Pulse function is used to start a seek or recall operation.

4.2 The DOA instruction load the interrupt reset register, mode and Cylinder address into the disc controller.

The DOA instruction perform the function specified by F.

DOA-instruction

0	1	1	A	C	0	1	0	F		Device address					
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

AC:

Status reset	Interrupt reset			X	Mode		Cylinder address							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

X = not used.

Bit 0 clear status and Done.

Bits (1:4) clear seek Done (0:3) and this again clear interrupt.

The mode field bits (6:7) has following function :

6	7	
0	0	Read
0	1	Write
0	1	Seek
1	1	Recalibrate

A read and write command is initiated by a Doas which will
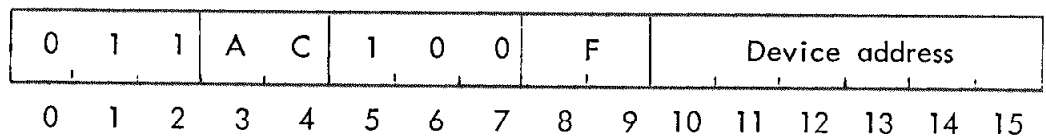set Busy and clear Done.

If the adaptor is busy or the disk is not ready, Busy is set and
read command has no function.

A seek and recalibrate command is initiated by a Doap. It has
no function on Busy and Done but does require 50 μsec to
initiate DCD 701.

The cylinder address field bits (8:15) is loaded in the cylinder
address register. Bit 8 is the most significant bit.

4.3   The DOB instruction load the contents of the specified accumulator
into the core address register with the starting core address.

DOB instruction

0	1	1	A	C	1	0	0	F	Device address					
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

AC :

Core address															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
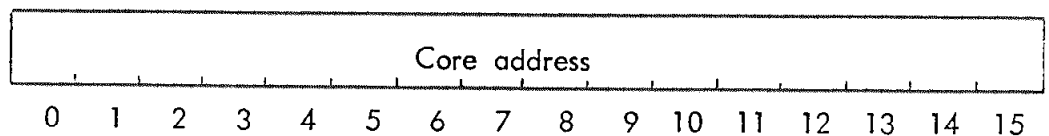
4.4 The DOC instruction load the contents of the specified accumulator into the disk unit, head, sector, and sector count address register.

DOC instruction

0	1	1	A	C	1	1	0	F	Device address
0	1	2	3	4	5	6	7	8 9 10 11	12 13 14 15

AC :

unit	F	Head	Sector	Sector count
0 1	2	3 4 5 6 7	8 9 10 11	12 13 14 15

Bit (0:1) select the unit to be operated.

0 1	
0 0	unit 0
0 1	unit 1
1 0	unit 2
1 1	unit 3

Bit 2. A zero in this bit indicate that this is not a formatting operation. Formatting is not required for disk cartridge systems.

Bit (3:7). This bits specified from which head a read/write operation should take place. $0 - 31$

Bit 3 is the most significant bit.

With bit (3:7) all zeroes indicate an operation on the upper head head in a two head system.

Bits (8:11). This sector register is incremented every time a sector is read or written. $0 - 15$

Bit 8 is the most significant bit.

Bits (12:15). The sector count register is loaded prior to the start of the operation with the 2's complement of the total number of consecutive sectors to be read or written. The sector count register is incremented every time a sector is read or written. $0 - (-15)$.

Bit 12 is the most significant bit.

4.5 The DIA instruction read the status of the disk into the specified accumulator from the controller status register.

DIA instruction

0	1	1	A	C	0	0	1	F	Device address			
0	1	2	3	4	5	6	7	8	9	10	11	12 13 14 15

AC:

Rd/Wr Done	Seek Done		Seeking		(a)	(b)	(c)	(d)	(e)	(f)	(g)
0	1 2	3 4	5 6	7 8	9	10	11	12	13	14	15

(a) : Disk Rdy.

(b) : Seek error.

(c) : End of cyl.

(d) : Add error or unsafe.

(e) : Check error.

(f) : DATA late.

(g) : Error.

Bit 0 with a logic one indicate that a read or write operation has finished.

Bits (1:4). A logic one indicate in which unit a operation has finished.

Bit	
1	unit 0
2	unit 1
3	unit 2
4	unit 3

Bits (5:8). A logic one indicate that a unit is seeking.

Bit	
5	unit 0
6	unit 1
7	unit 2
8	unit 3

Bit 9. This bit indicates if the disk is ready to seek, read, or write, or not.

A logic one indicate disk ready.

A logic zero indicate disk not ready.

Bit 10   with a logic one show that the selected disk did not complete a seek.

Bit 11   with a logic one indicate that the head address register has incremented beyond the last head of the cylinder. This condition will cause a consecutive sector read or write to stop transfer.

Bit 12   with a logic one indicate that the disk selected by the program is unsafe for operation or the address selected on the   . disk does not agree. Address errors are a mismatch between the header data and the cylinder header being sought.
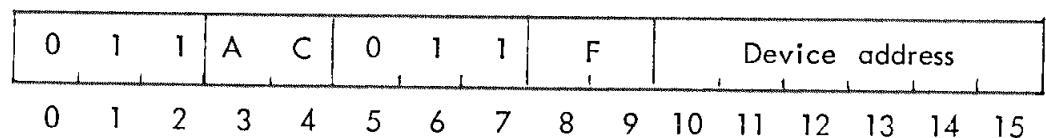
Bit 13   with a logic one indicate that in read, the cyclic checkword read from the disk surface did not agree with the checkword computed by the control.

Bit 14   show, with a logic one, that the data channel fail to respond in time to a request for access.
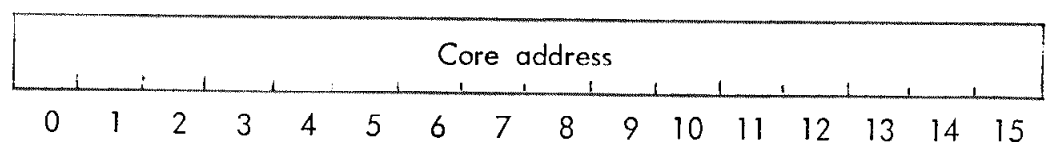
Bit 15   with a logic one indicate the "or" condition of bits (10:14) exists.

4.6   The DIB instruction read the contents of the address counter into the specified accumulator.

DIB instruction

0	1	1	A	C	0	1	1	F	Device address					
0	1	2	3	4	5	6	7	8 9	10	11	12	13	14	15

AC:

Core address														
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14 15

Core address is starting core address + 256X + 2, where X is the number of sector's written.

4.7 The DIC instruction read the present contents of the unit, head address, sector address, and sector count registers into the specified accumulator.

DIC instruction

0	1	1	A	C	1	0	1	F		Device address				
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

AC:

unit		Head						Sector				Sector count		
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

For further informations : See DOC instructions.

5. ENVIRONMENTAL

5.1 Mechanical layout.

DCC 701 is placed in chassis CHS 701 and use one slot.

The slot size and weight is the standard controller board.

5.1 Power.

Power needed is +5 Vol. 2.3 Amp., which is supplied from POW 701 also placed in CHS 701.

5.3 Cabling.

1001 connector is not used.

1002 connector perform the interface to a disk cartridge adaptor.

1003 connector interface the DCC 701 to the RC 7000 central processor bus.

1004 connector is not used.

5.4 Temperature range : 16 - 32° C.

Relative humidity : 20 - 80%.

6. APPLICABLE DOCUMENTS

    1.   How to use the NOVA Computers.

    2.   Drawings for DCC 701.

    3.   DCA 701 Reference Manual.

    4.   Drawings for DCA 701.

    5.   Technical Manual for exchangeable Disk Drive, Series 30.