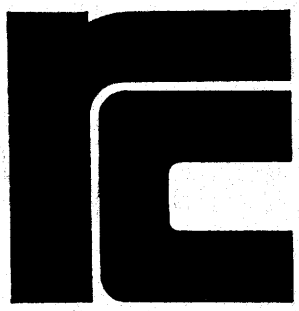
Victor Jorgensen



TECHNICAL MANUAL

DFC 402 8/1-70
KABELFORDELING

ANTAL PLADER = 66
ANTAL KABELSTIK = 8
ANTAL RESERVEREDE POSITIONER = 0

TYPE	ANTAL	RC-NR.	KREDSLØB
1	7	834-1	12AC401
2	5	839-1	7AC402
3	2	838-1	4AC403
5	1	860-2	4DD402
14	1	884-1	9BA403/1AA405
16	4	835-1	6BC401
17	3	847-1	7AG401
23	1	8016-38	38 POL ELCO
24	7	8016-90	90 POL ELCO
26	1	837-1	3BB401
35	1	836-1	5AC404
37	1	890-1	11DB402/1DB403
41	1	894-1	4DB404/1DB405
43	1	858-1	1AG402
50	1	893-2	1FF402
55	3	898-1	1DB406
56	6	897-1	10DC405
58	1	901-1	1AJ408
60	1	903-1/	1AJ407/1BG407/1CC406
69	1	909-1/	6CB402
72	2	933-1	8DB409
73	8	934-1	3BF403
74	8	935-1	3BD404
75	2	936-1	18DC408
76	1	834-2	12AM401
77	4	3032-1	12AD401

DFC 402 8/1-70
UBLE POSITION LIST

FORMAT = 3 x 26

IND	AKT	TYP	SYM	TYP
1	64	16	49	72
2	66	16	50	72
3	62	60	70	56
4	65	69	52	75
5	67	1	53	75
6	21	2	36	37
7	44	77	23	17
8	10	14	22	1
9	9	17	9	17
10	16	74	8	14
11	15	74	57	35
12	45	1	18	77
13	75	50	19	74
14	74	5	17	74
15	23	3	11	74
16	22	1	10	74
17	14	74	31	73
18	12	77	30	73
19	13	74	21	76
20	41	74	51	43
21	19	76	6	2
22	8	1	16	1
23	7	17	15	3
24	42	74	46	17
25	40	74	44	73
26	39	74	45	73
27	70	16	76	55
28	50	77	77	55
29	68	26	78	55
30	18	73	35	73
31	17	73	34	73
32	33	73	33	73
33	32	73	32	73
34	31	73	71	56
35	30	73	72	56
36	6	37	73	56
37	46	2	74	56
38	48	1	55	58
39	47	77	26	74
40	69	2	25	74
41	72	16	20	74
42	49	2	24	74
43	51	1	56	2
44	25	73	7	77
45	26	73	12	1
46	24	17	37	2
47	71	3	39	77
48	52	1	38	1
49	1	72	42	2
50	2	72	28	77
51	20	43	43	1
52	4	75	48	1
53	5	75		
54	73	41		

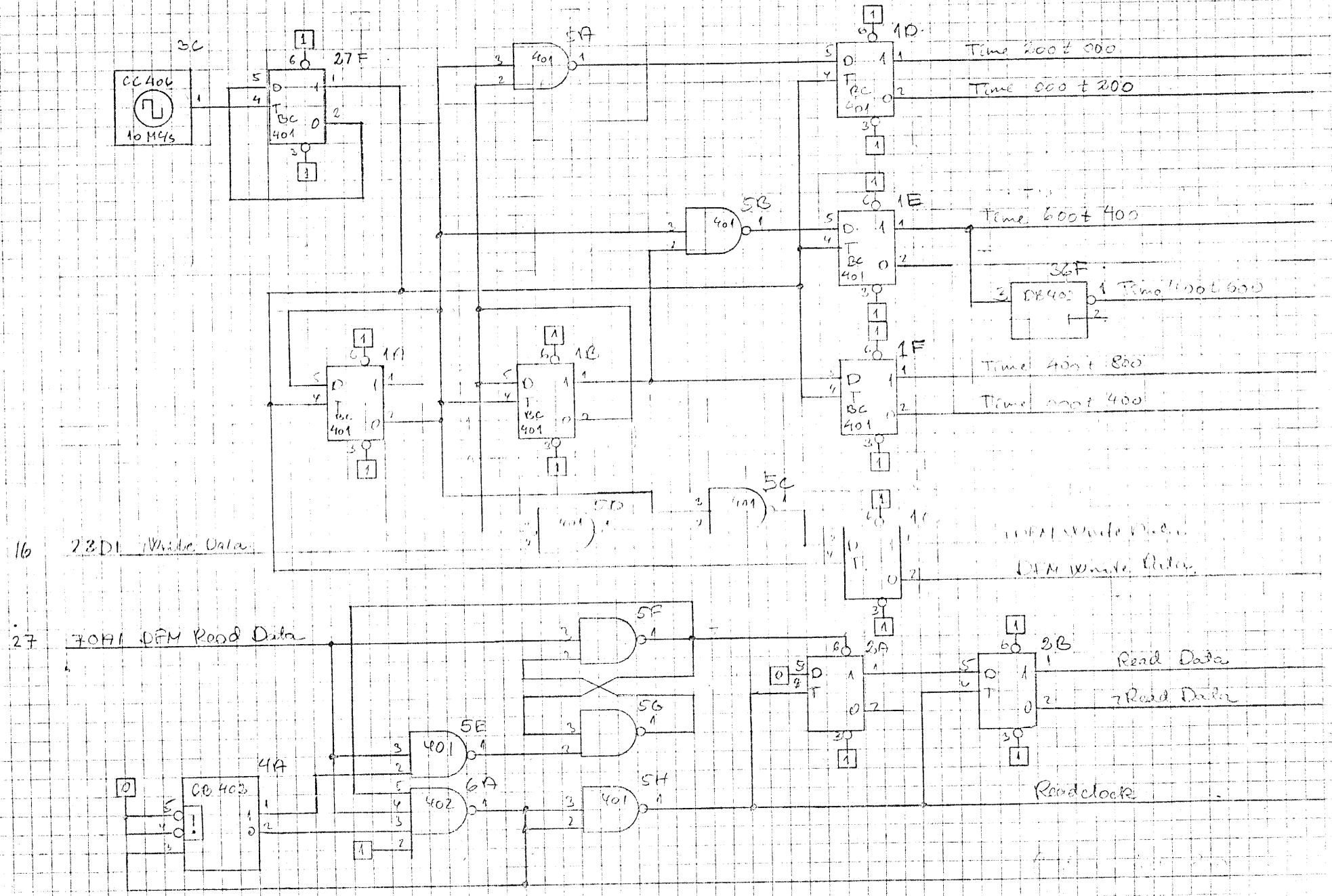
55	38	58		
56	43	2		
57	11	35		
62			3	60
63			75	56
64			1	16
65			4	69
66			2	16
67			5	1
68			29	26
69			40	2
70	3	56	27	16
71	34	56	47	3
72	35	56	41	16
73	36	56	54	41
74	37	56	14	5
75	63	56	13	50
76	27	55		
77	28	55		
78	29	55		

KABP	X	Y	TYPE
1360	37	393	24
1361	37	-30	24
1362	195	395	24
1363	195	-30	24
1364	350	395	24
1365	350	-30	24
1366	-60	55	24
1369	-60	105	23

A/S REGNECENTRALEN	Designed by	Drawn by	Dwg. Office Chk.	Design Check	Replaces Dwg. No.	due to ECN	Replaces Dwg. No.

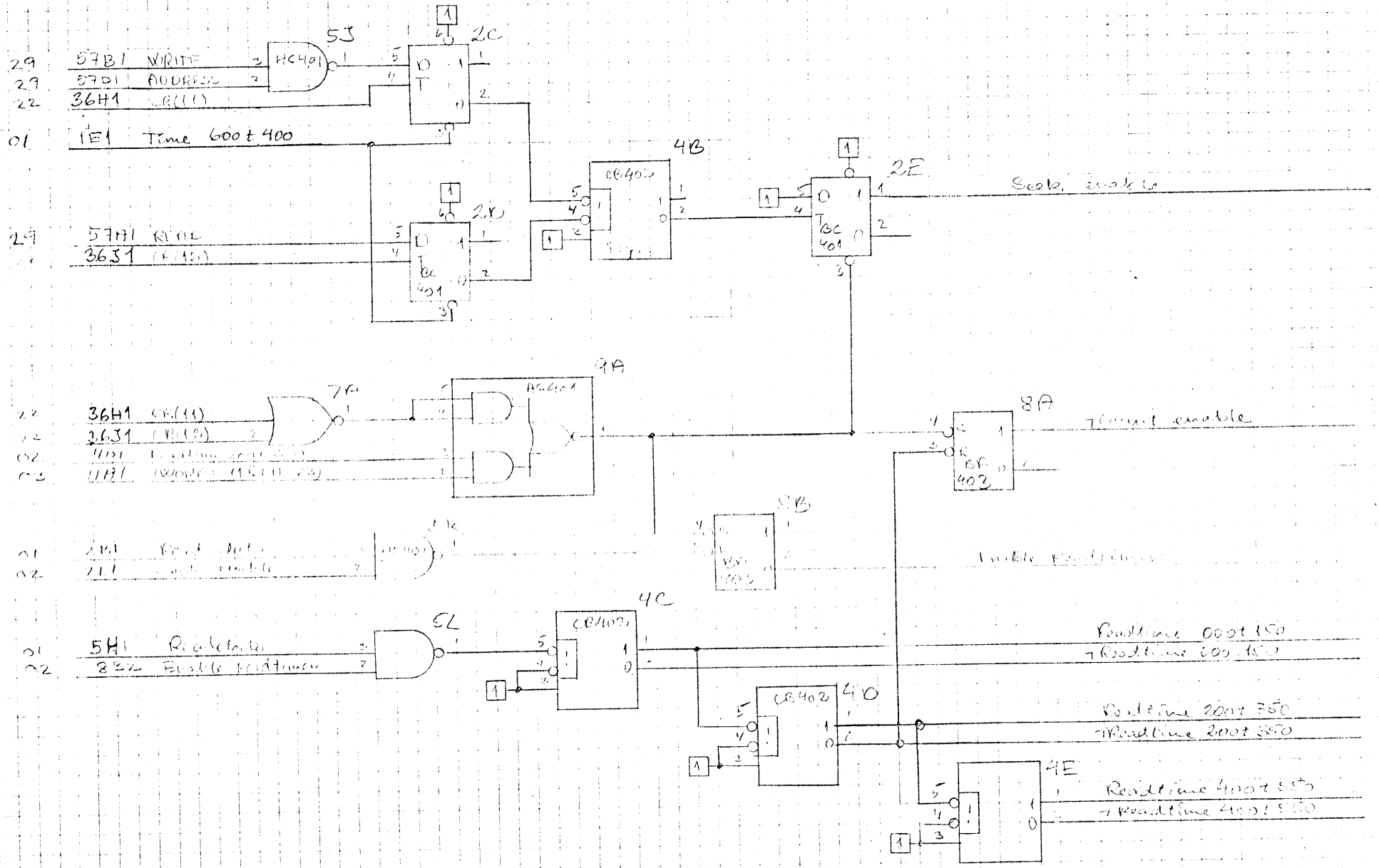
CLOCKGENERATION, WRITE MODULATION AND READ DETECTOR

Page Drawing



A/S REGNECENTRALEN	Designed by	Drawn by	Dwg. Office C	Design Check	Replaces Dwg. No.	due to ECN	Rep y Dwg. No.

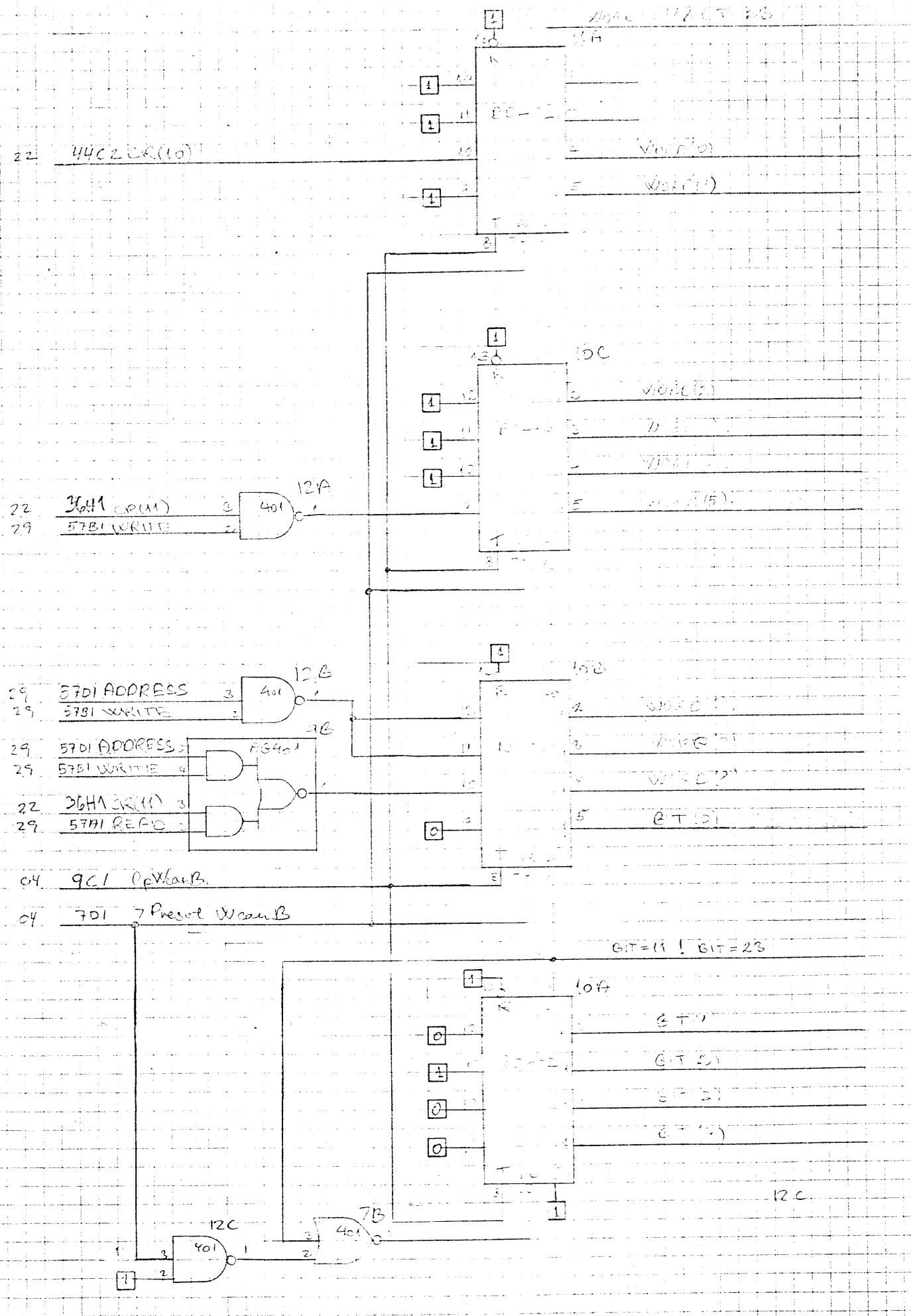
Unit RC4000 Dwg.No. VB 140



REAL SYNCHRONIZER

logic Diagram

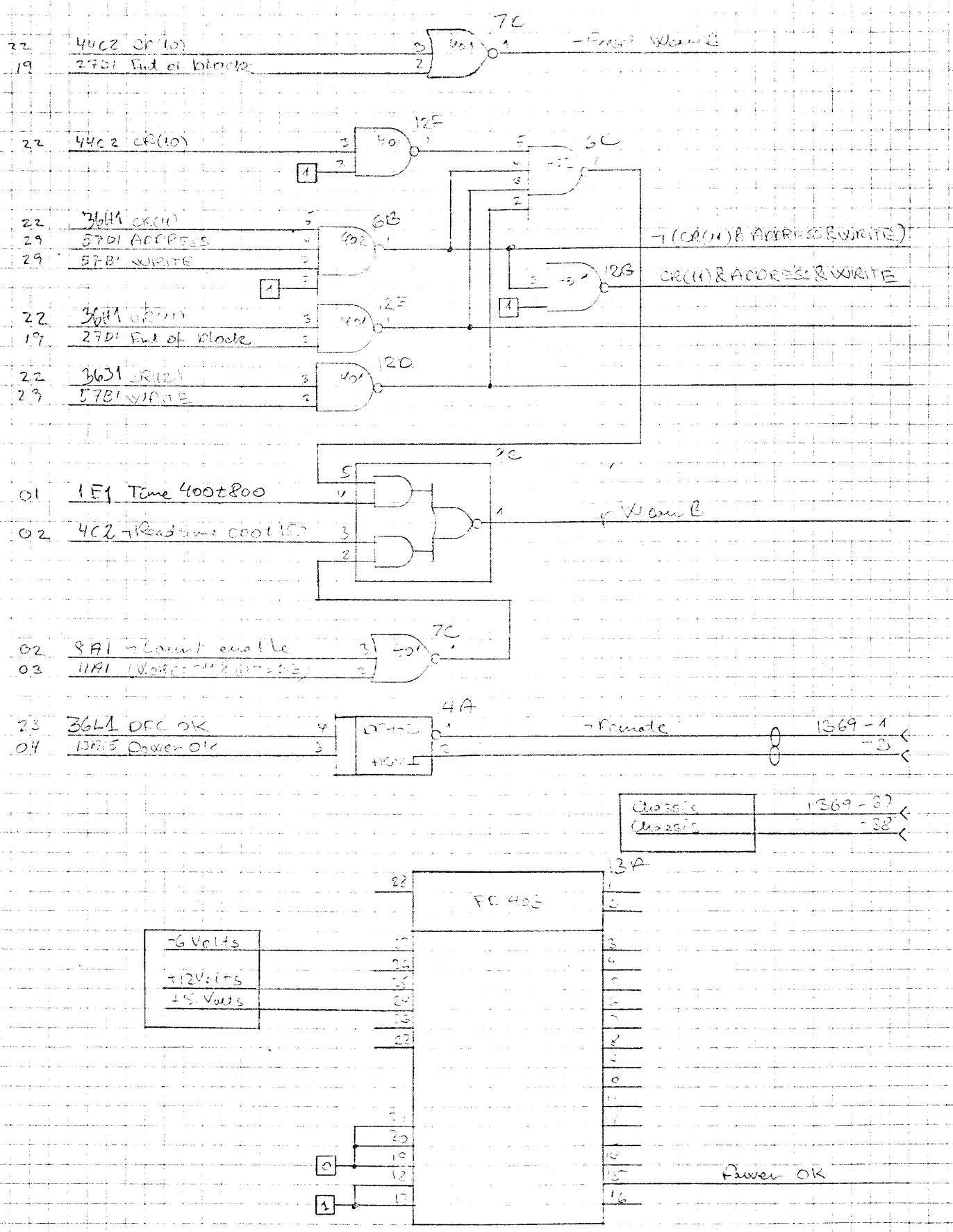
OPC-2



Unit RC4000	WORD AND BIT COUNTER (BIT (0-3) BIT (0-4)	DPC -
Dwg. No. V11803		

A/S REGNECENTRALEN | Designed by | Drawn by | Dwg. Office | Design Check | Replaces Dwg. No. | due to ECN | Rel. by Dwg. No.

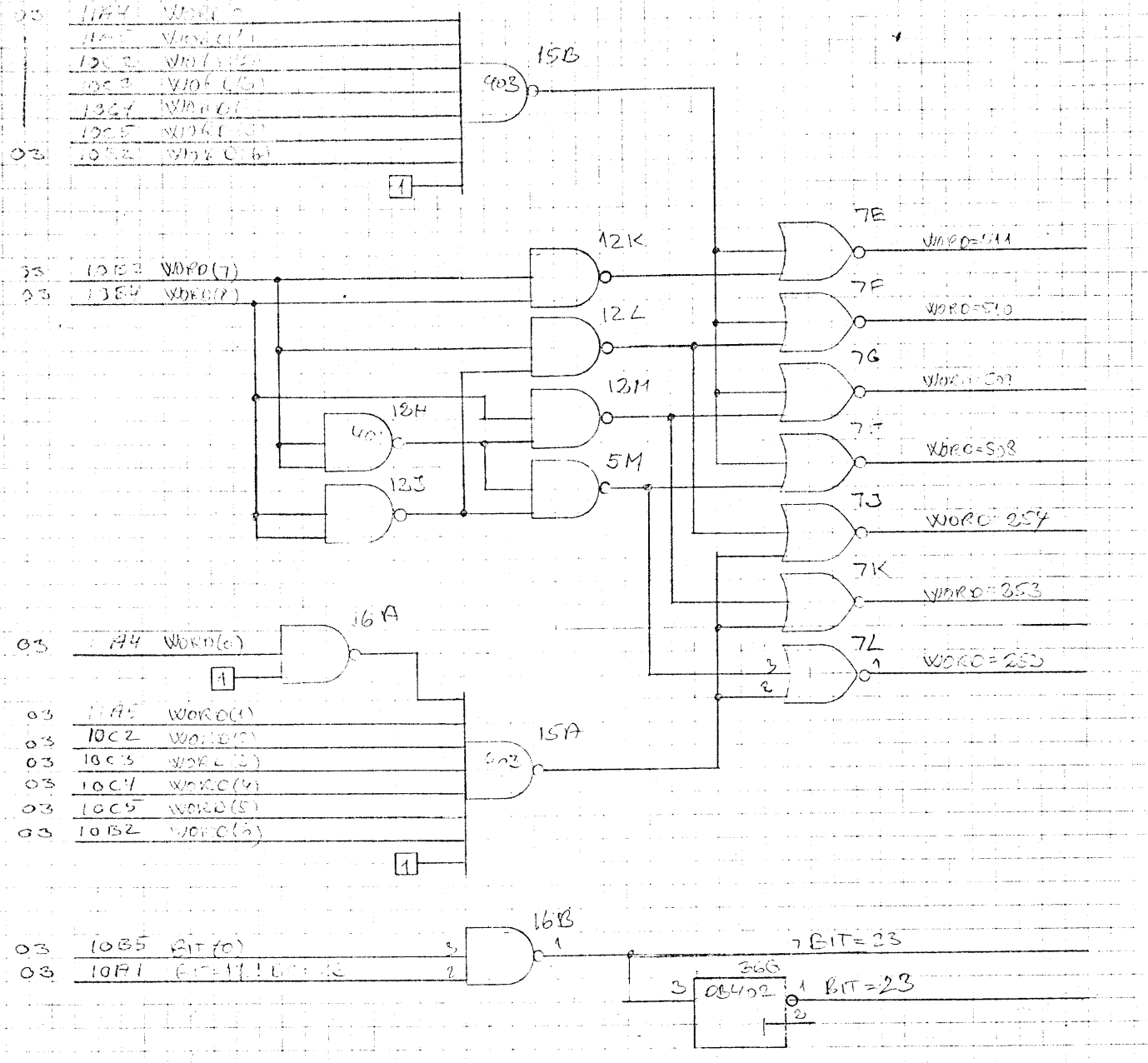
RC doc VB 149



A/S REGNECENTRALEN	Unit R64000	WORD AND BIT COUNTER CONTROL	
	Dwg. No. V11804		

Designed by | Drawn by | Dwg. Office Check | Design Check | Replaces Dwg. No. | Repl. due to ECN | Dwg. No.

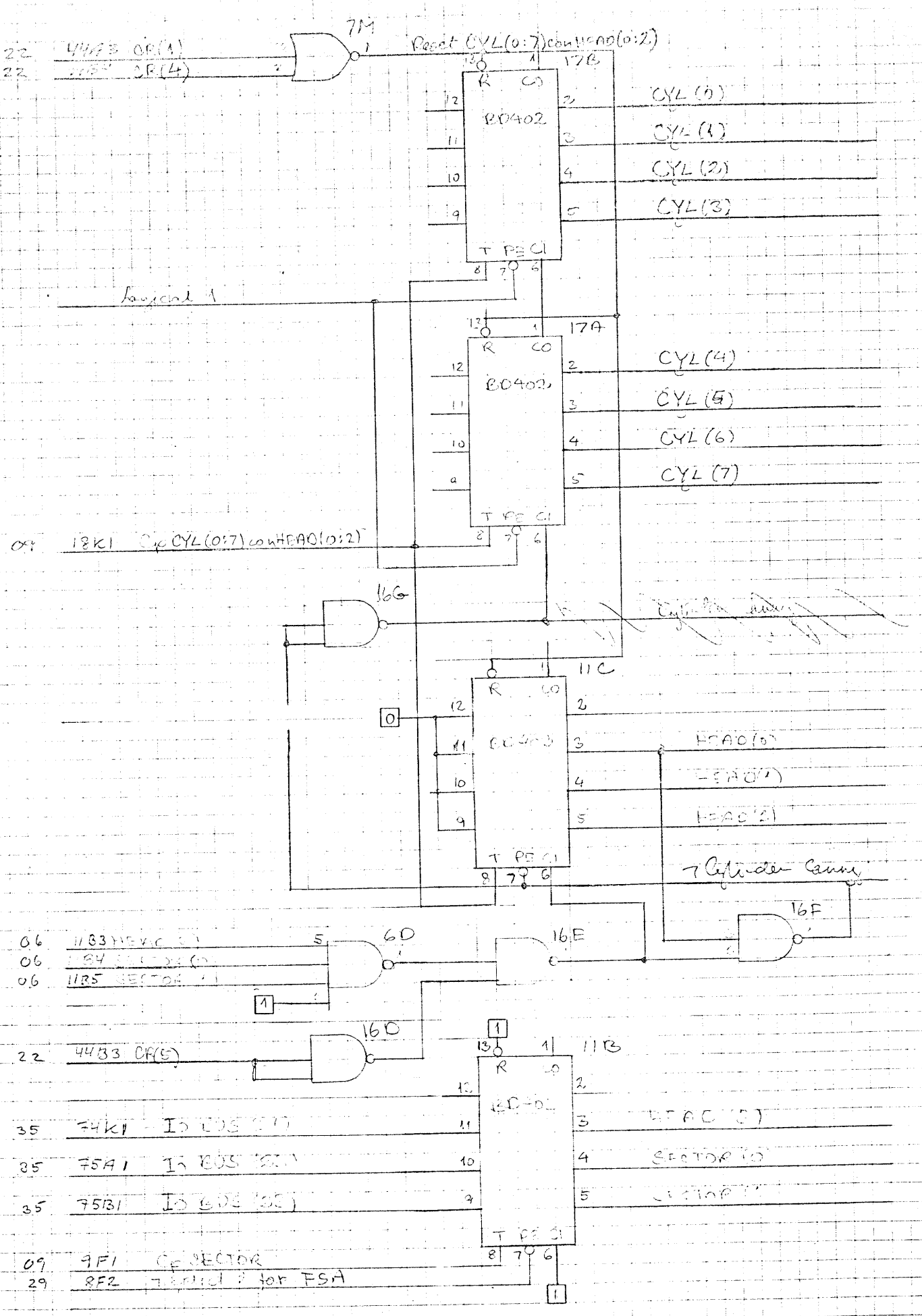
VC doc. V8.140



Unit RC4000	WORD AND BIT PRECODINGS		OFC-5
Dwg. No. V11805	Logic Diagram		

A/S REGNECENTRALEN | Designed by | Drawn by | Dwg. Office Check | Design Check | Replaces Dwg. No. | due to ECN | Re... by Dwg. No.

RC doc. V8.140



Unit	RC4000	SECTOR(0:1), HEAD(0:3), CYL(0:7)	DEC-6
Dwg. No.	V11806	Logic Diagram	

A/S REGNECENTRALEN

Designed by 13/11 69 FBKO

Drawn by

Dwg. Office Check

Design Check

Replaces Dwg. No.

due to ECN

Repla... Dwg. No.

RC doc. V8 140

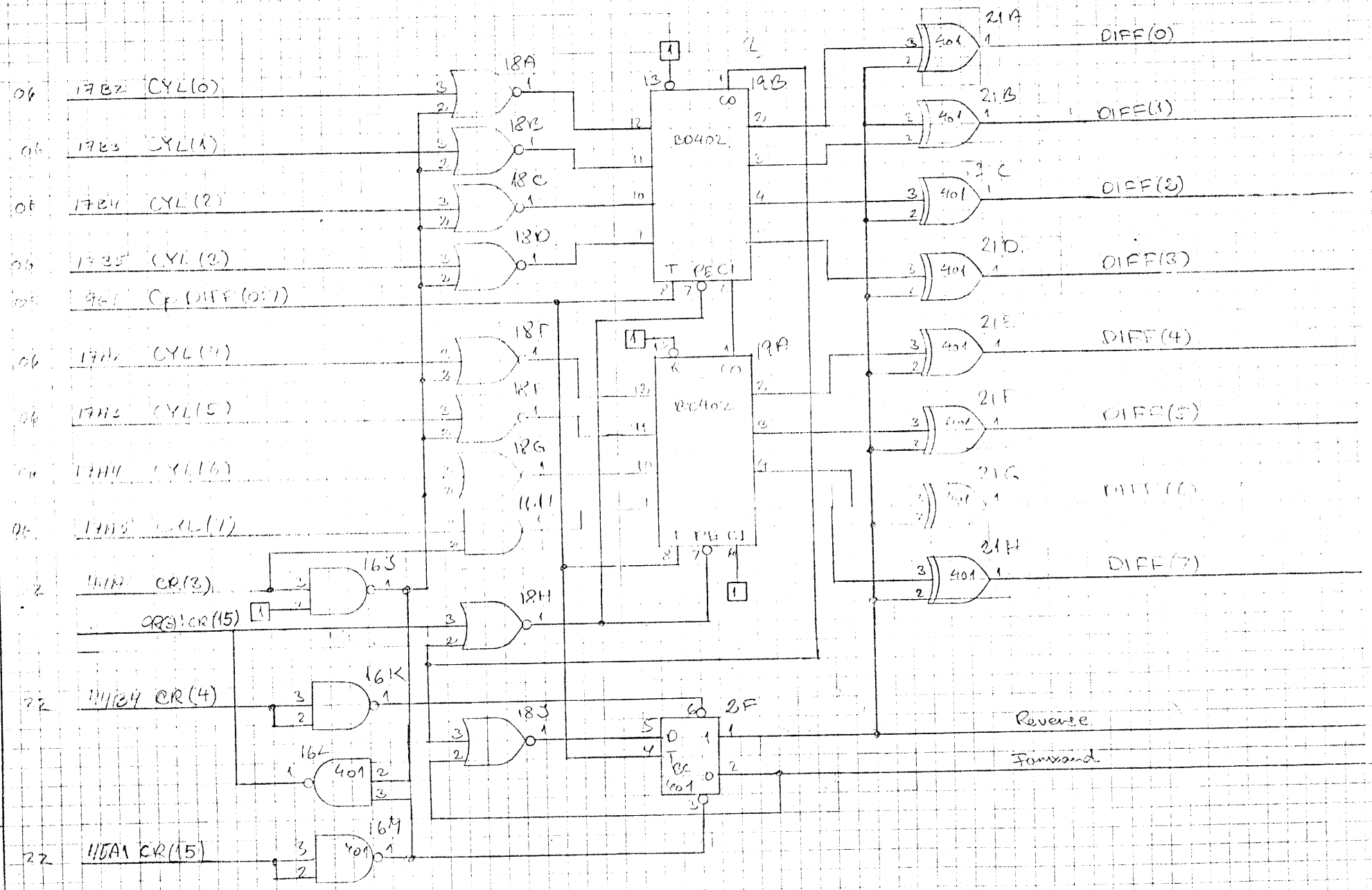
RC doc: VB 140

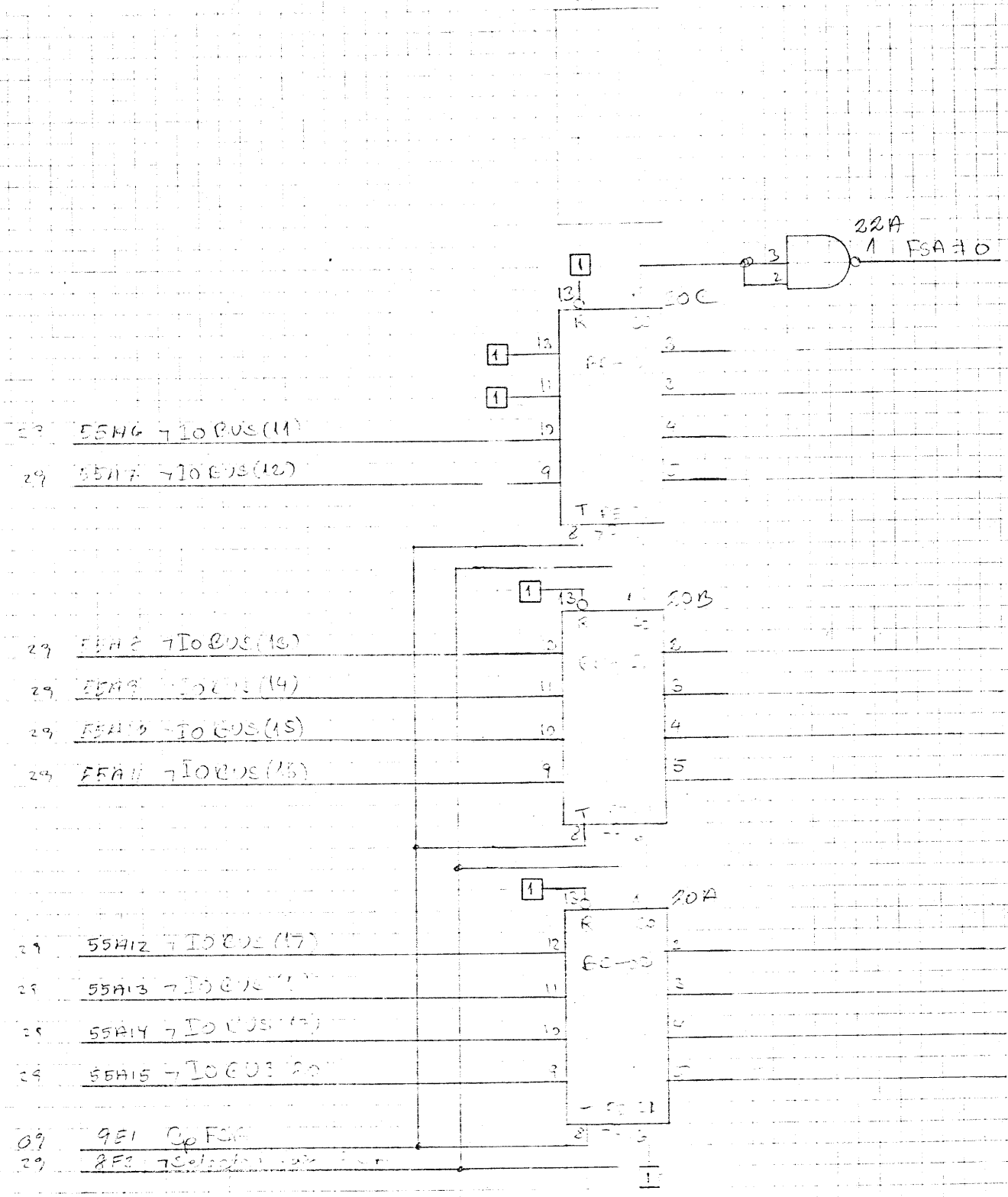
A/S REGNECENTRALEN	Designed by	Drawn by	Dwg. Office Che	Design Check	Replaces Dwg. No.	due to ECN	Replac	Dwg. No.

Dwg. No. VM SC7 Unit

CYLINDER DIFFERENCE (DIFF)

Basic Diagram



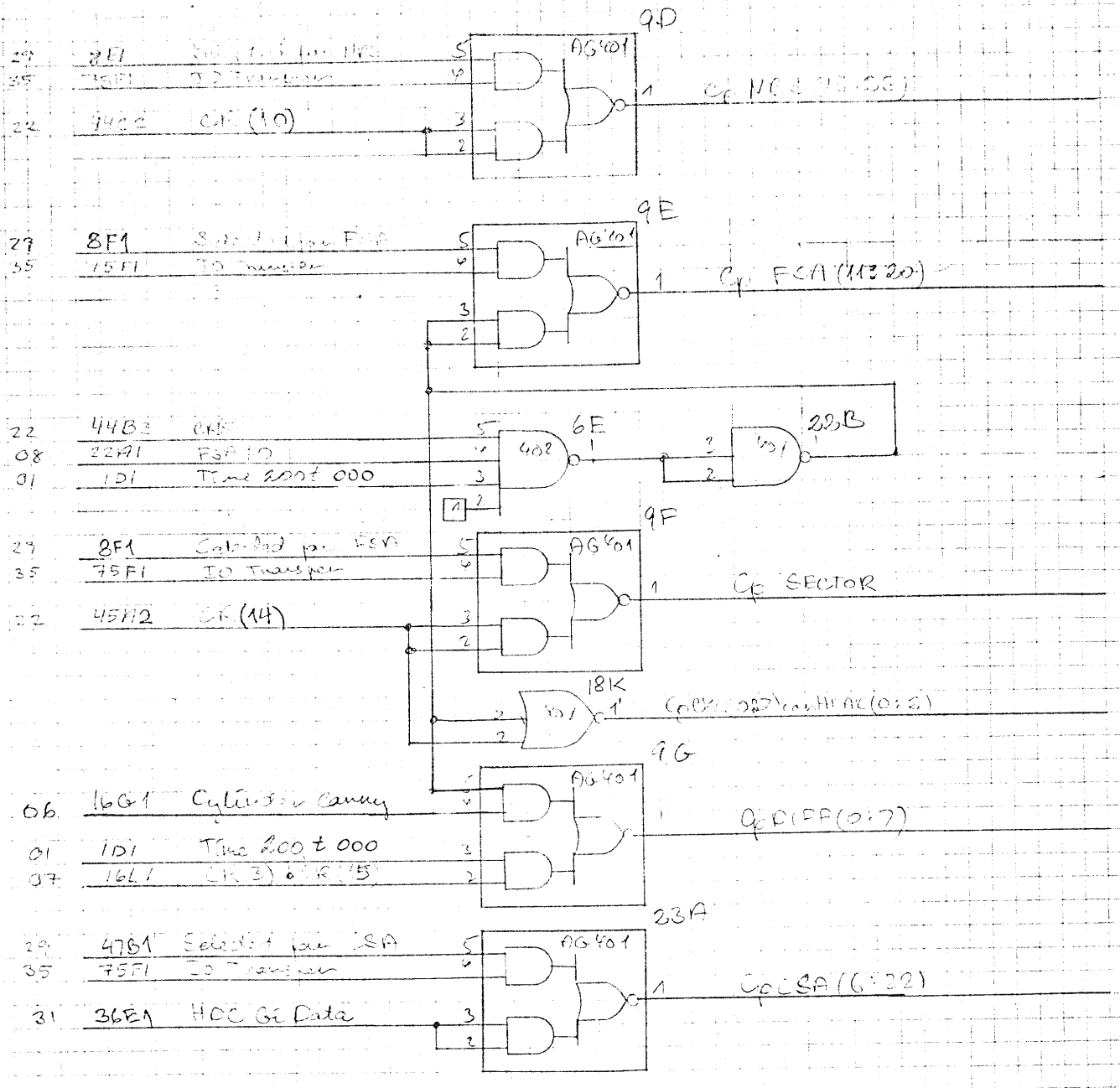


Unit R4000		
Dwg. No. V11308		

A/S REGNECENTRALEN

Designed by | Drawn by | Dwg. Office C | Design Check | Replaces Dwg. No. | due to ECN | Repl. by Dwg. No.

IEC cos. VB 140



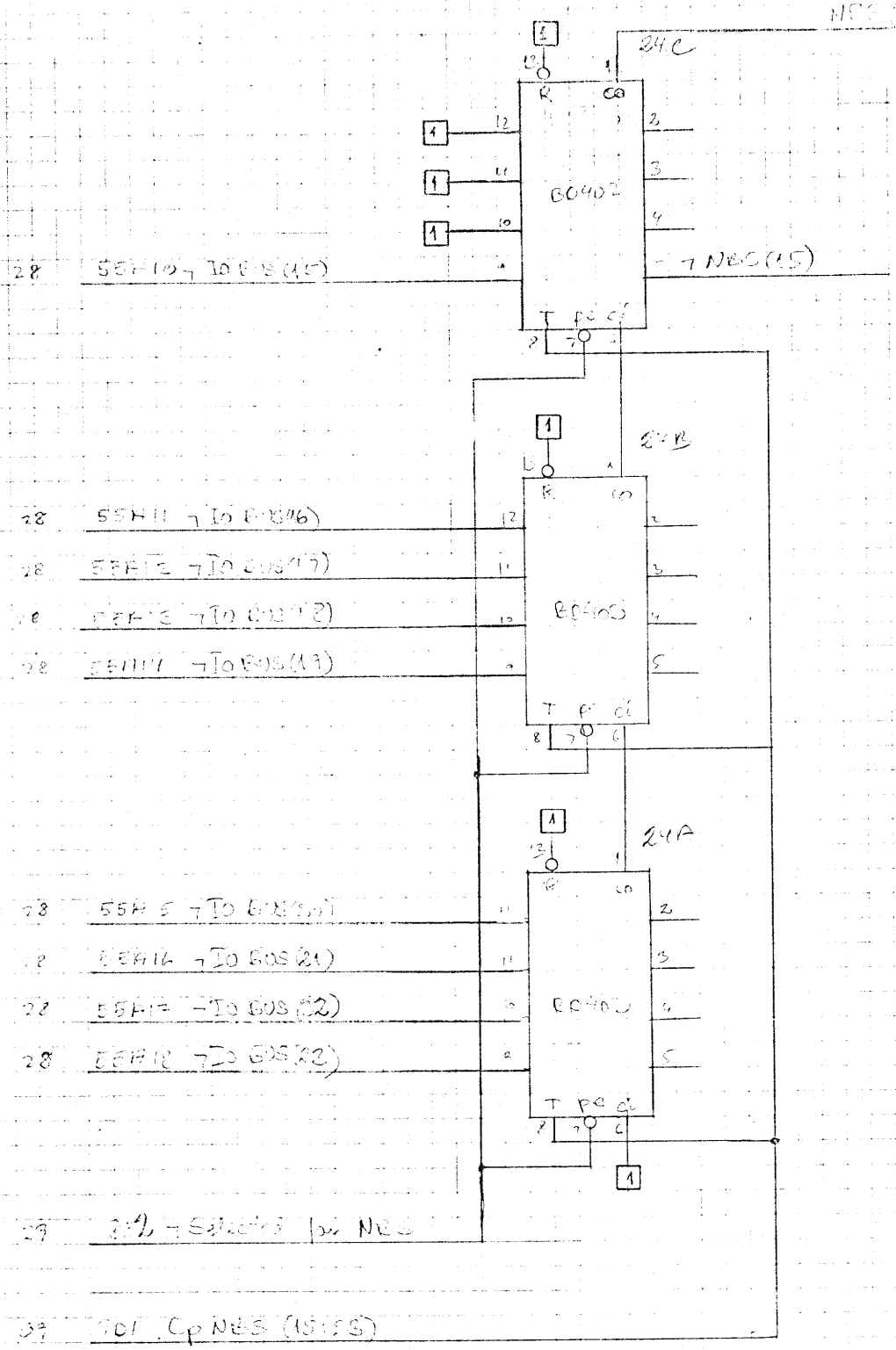
Unit	CLOCKPULSES FOR NBS, ESA, SECTOR, CYL, HEAD, DIFF AND CSA
Dwg. No. V11809	Logic Diagram

DFC-9

RC doc. V3.140

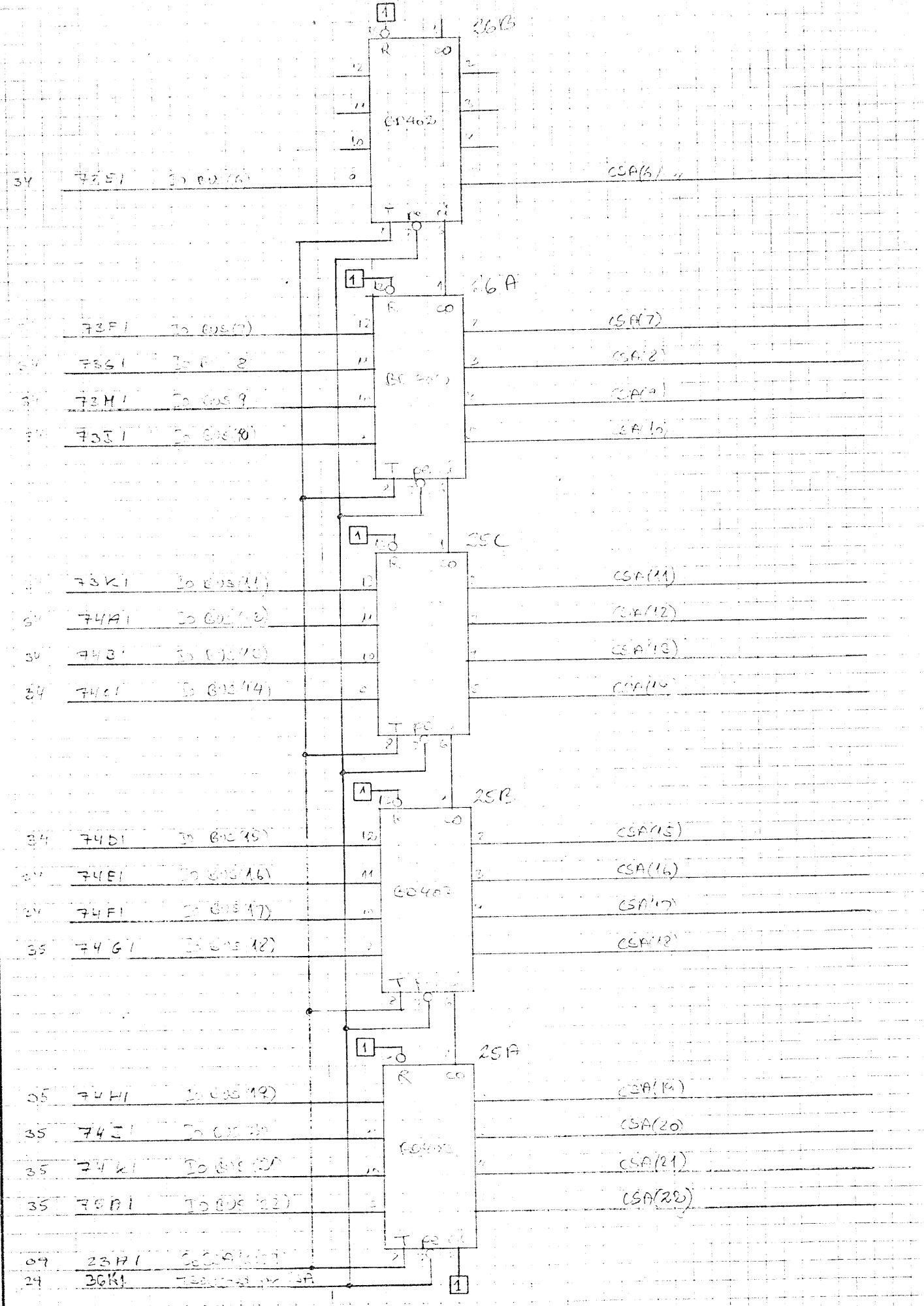
A/S REGNECENTRALEN

Designed by | Drawn by | Dwg. Office | Design Check | Replaces Dwg. No. | due to ECN | Revised by Dwg. No.



A/S REGNTRALEN	Unit KC4xx0	NUMBER OF SEGMENTS, NBS(15:2:3)
Designed by	Dwg. No. V11810	Logic Diagram
Drawn by		RFC-10
Dwg. Office		
Design Check		
Replaces Dwg. No.		
due to ECN		
by Dwg. No.		

RC doc: VB 140

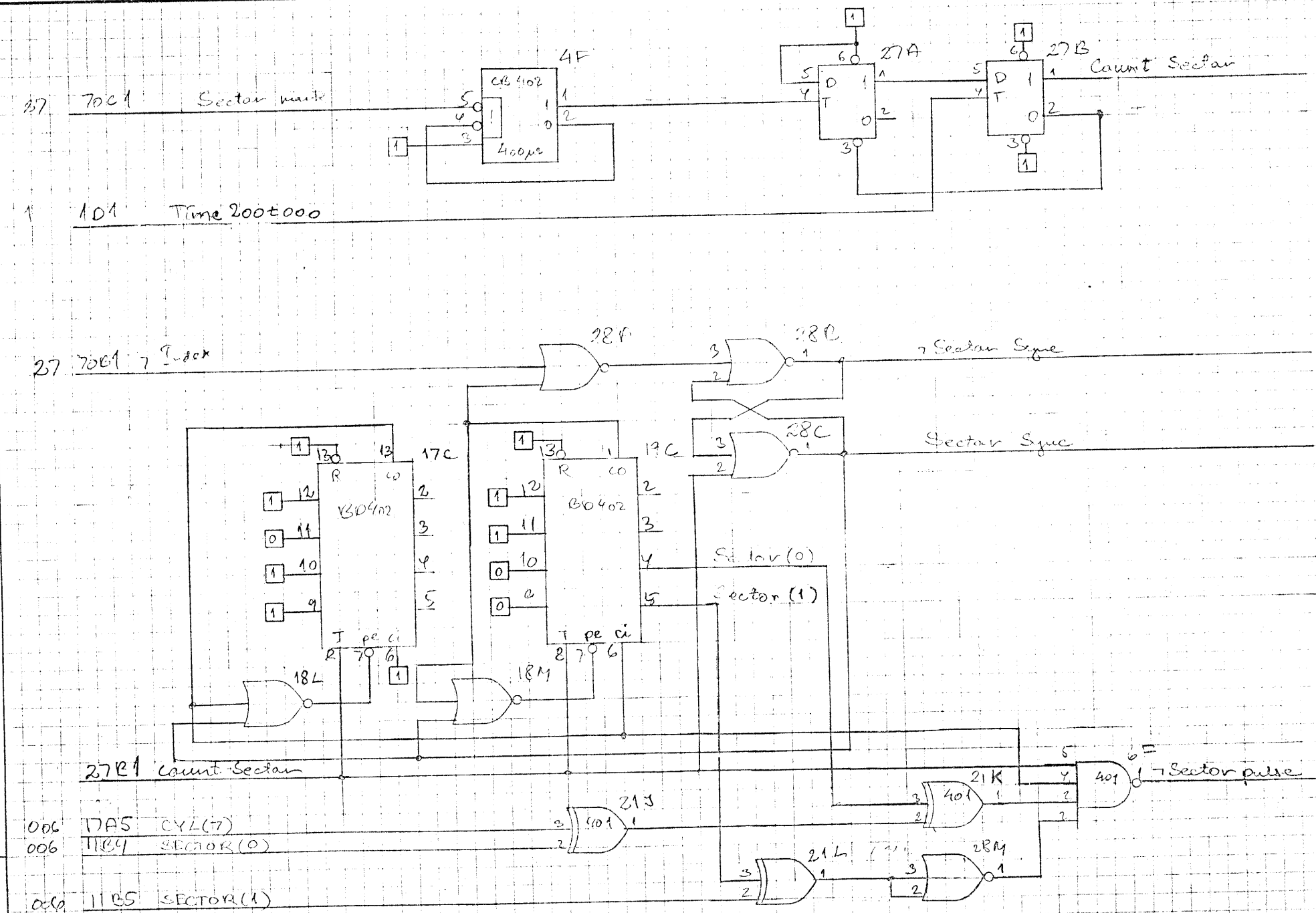


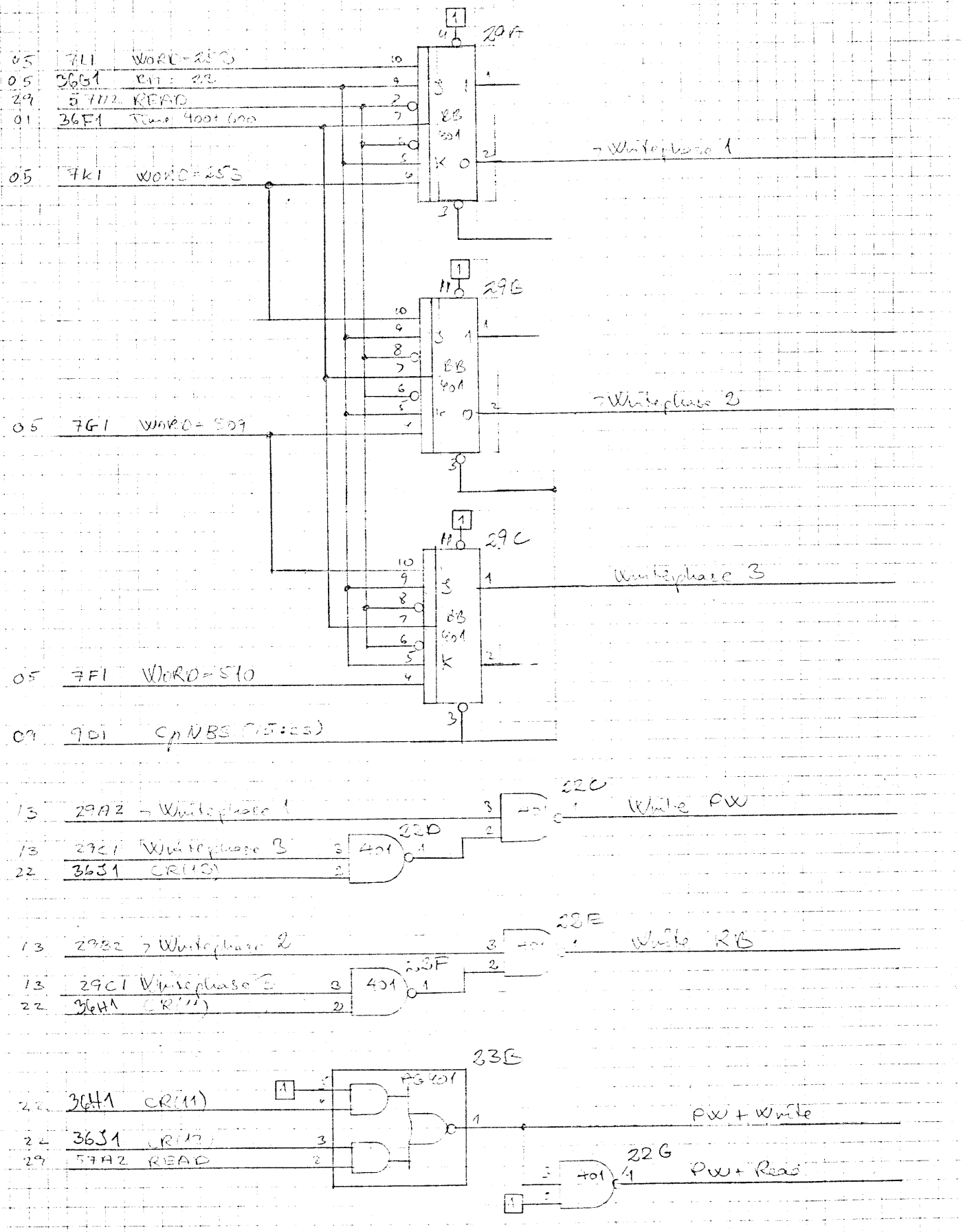
Unit	RC4000
Dwg. No.	V11811
	CSA6:22, CSA(6:22)
	Logic Diagram
	DFC-1

Designed by | Drawn by | Design Check | Replaces Dwg. No. | due to ECN | Released by Dwg. No.

A/S REGNECENTRALEN

RC doc V8 140


4F
CB 402
400µs
27A
27B
Count Sectar
27 70C1 Sector mark
1 101 Time 200t000
28F
28B
28C
Sector Sync
Sector Sync
17C
17C
B0402
B0402
Sector (0)
Sector (1)
18L
18M
27R1 Count Sectar
21K
21J
21L
28M
401
401
401
Sector pulse
006 17A5 CYL(7)
006 11B4 SECTOR(0)
006 11B5 SECTOR(1)

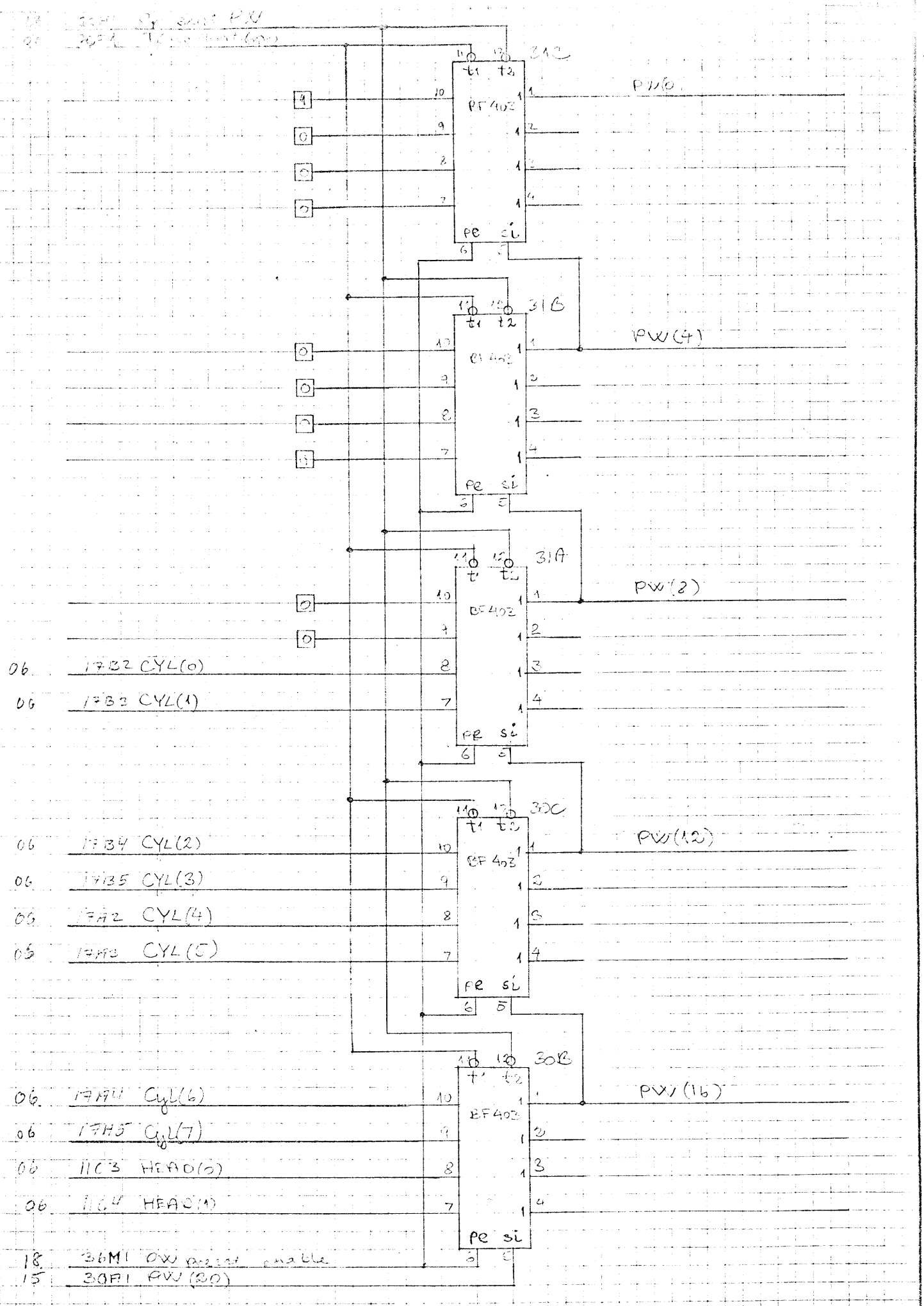


Unit	WRITE CONTROL	DFC-16
Dwg. No. V11813	logic Diagram	

A/S REGNECENTRALEN

Designed by | Drawn by | Dwg. Office | Design Check | Replaces Dwg. No. | due to ECN | Re by Dwg. No.

DEC.dsk V8.110

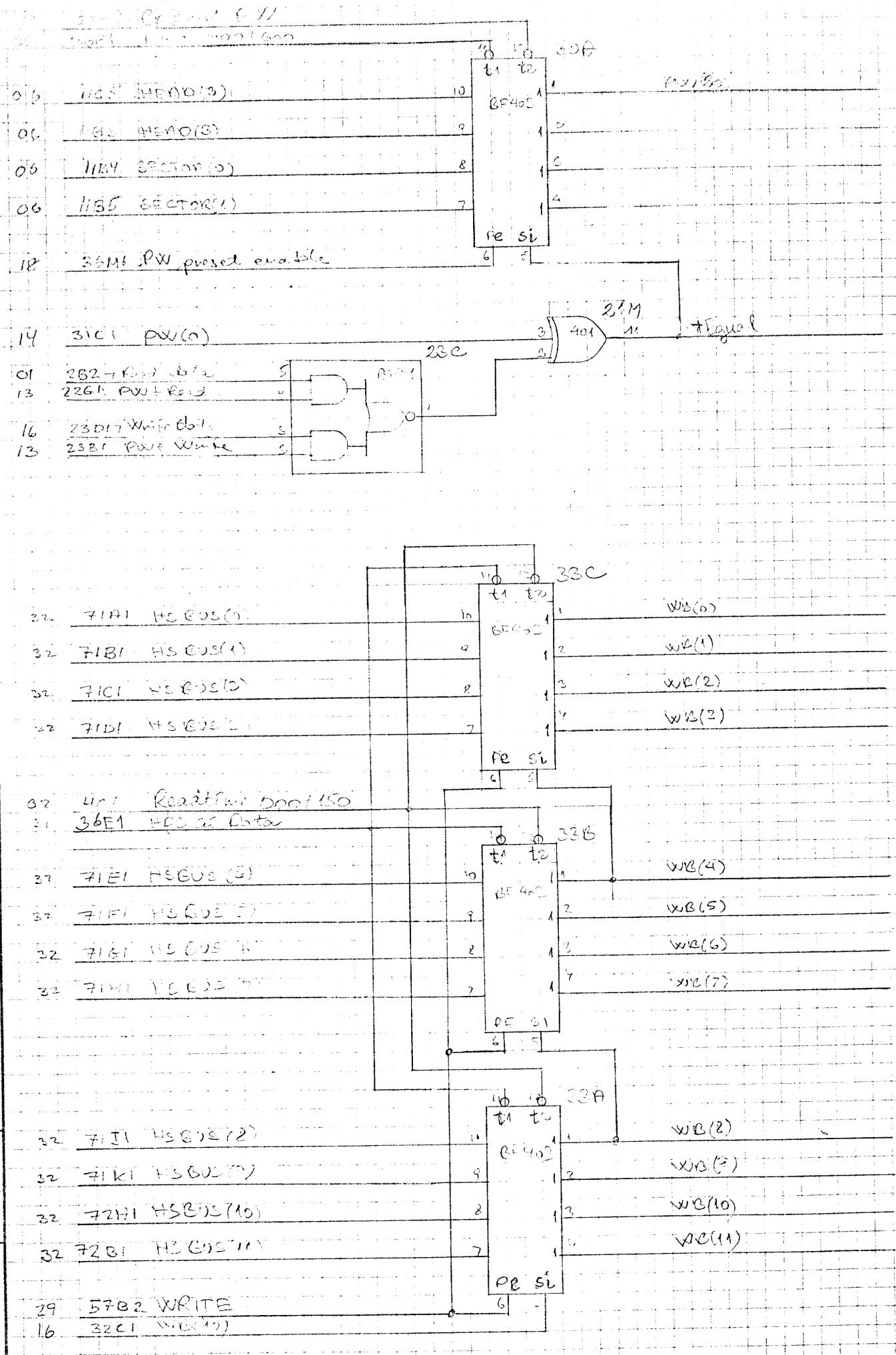


Designed by 12/1/67 FBP	Drawn by	Dwg. Office	Design Check
Replaces Dwg. No.	due to ECN	Released by Dwg. No.	

A/S REGNECENTRALEN

Unit RC4000	PARITY WORD, PW (0:19)	DFC - 12
Dwg. No. V11814	Logic Diagram	

RC 1967 V8.1#0



Unit	RC4000
Dwg. No.	V11815
Designed by	131169 FBP
Drawn by	
Design Check	
Dwg. Office	
Replaces Dwg. No.	
due to ECN	
Re by Dwg. No.	

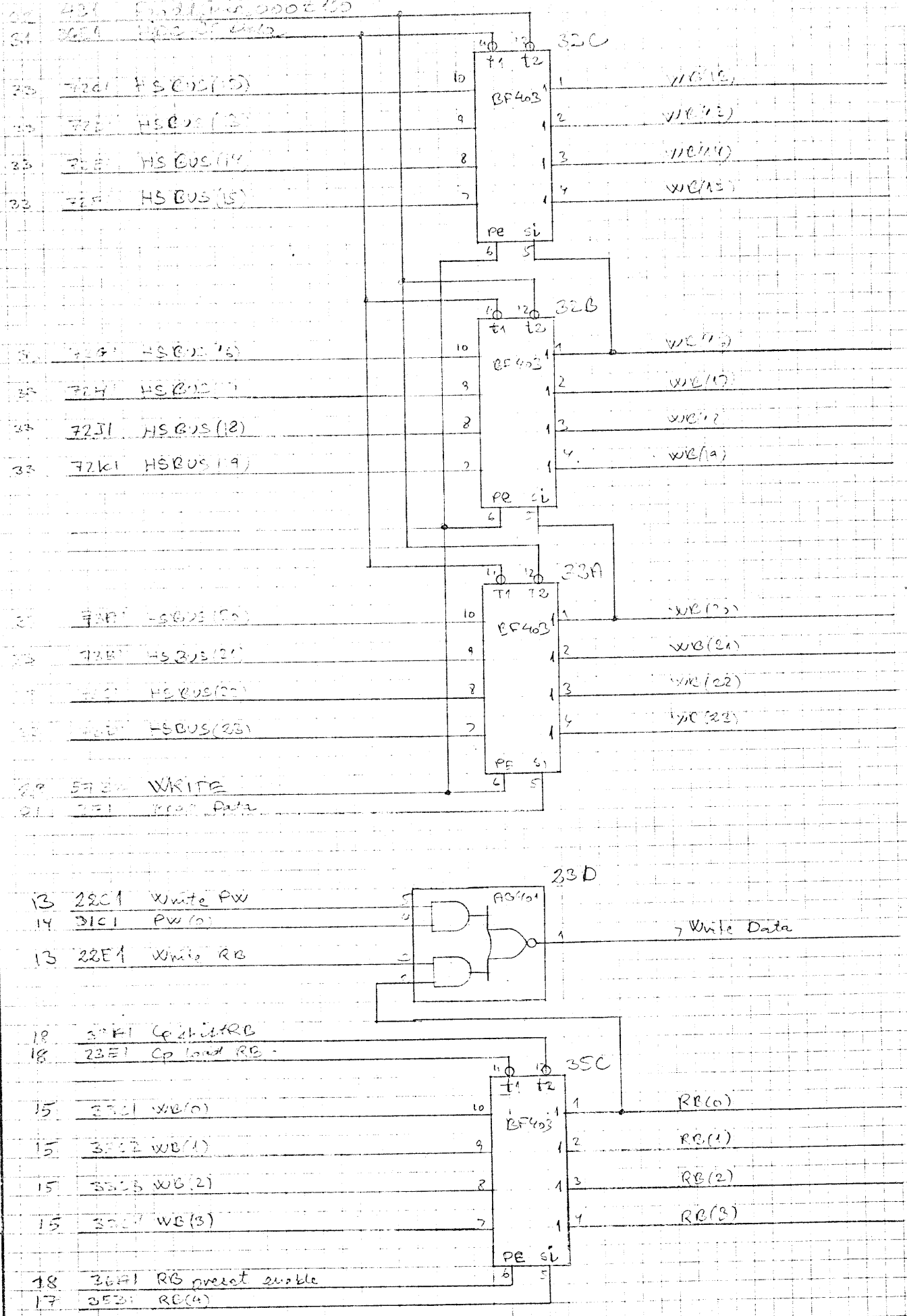
WRITE BUFFER, WB(0:11), PARITY WCRD, PW(20:25)

Logic Diagrams

DFC-75

A/S REGNCENTRALEN

RC doc VB 140



Unit	RC4000	READ BUFFER RB(0:3) ; WRITE BUFFER WB(12:33)
Dwg. No.	V11816	Logic Diagram

A/S REGNECENTRALEN

Designed by EVD 18/11 69

Drawn by

Dwg. Office C

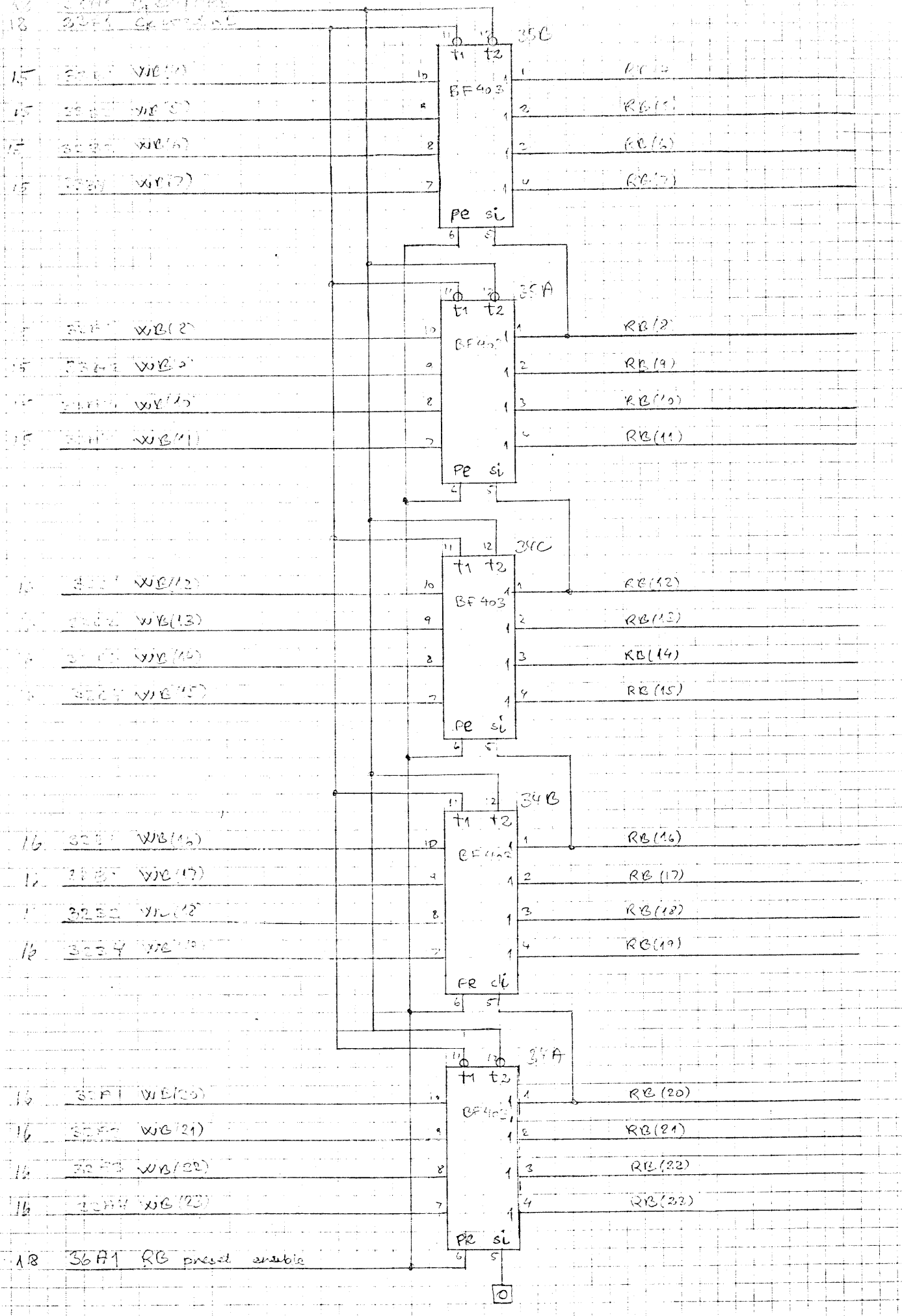
Design Check

Replaces Dwg. No.

due to ECN

Repl

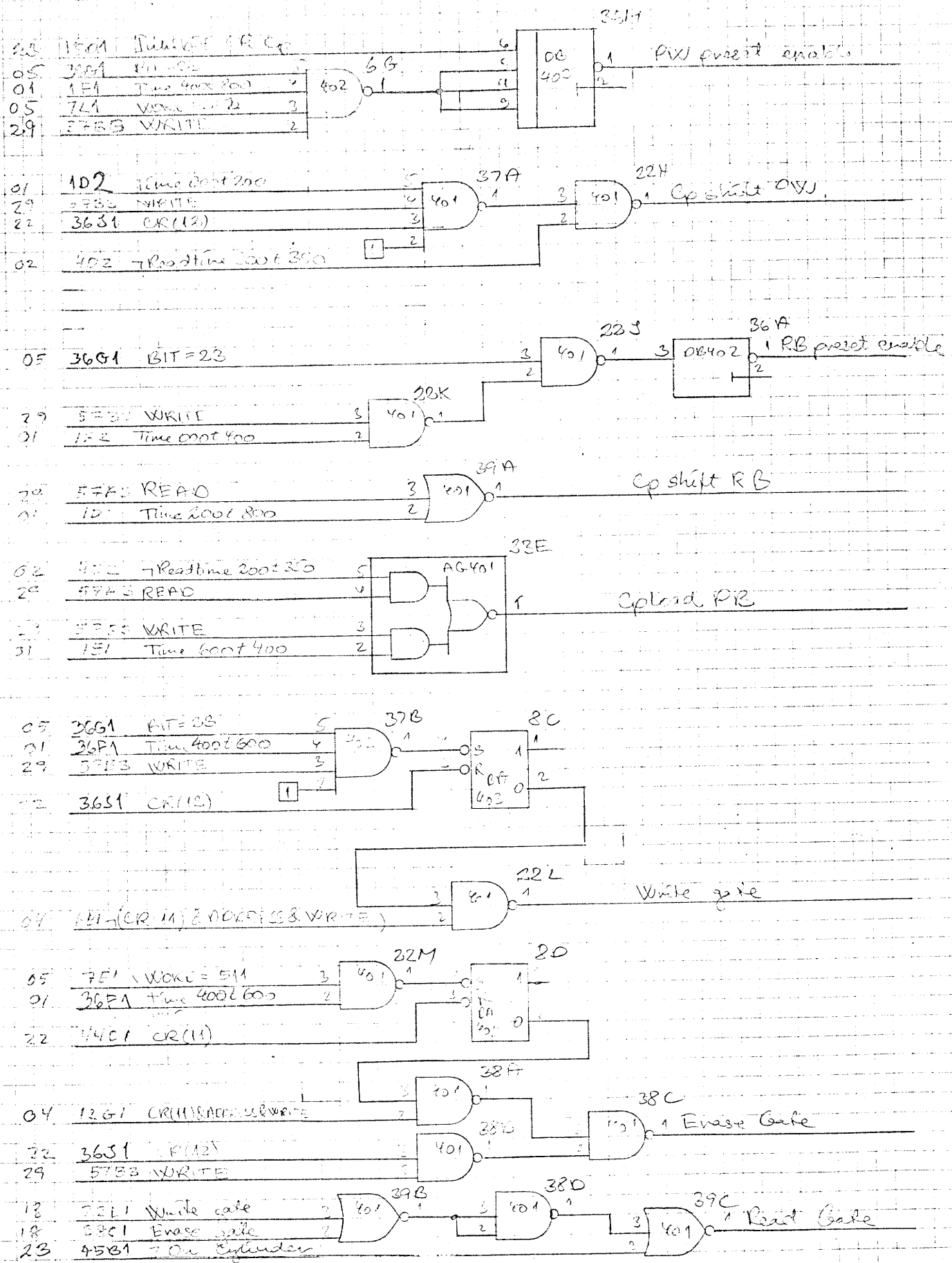
Dwg. No.



Unit	IC 4000	READ BUFFER RB(4:23)			DFC-17
Dwg. No.	V11817	Logic Diagram			
Designed by	12/1/69 FBD	Drawn by	Design Check	Dwg. Office C	Replaces Dwg. No. / due to ECN / Rep

NORSK REGNESENTRALEN

IC 4000 V8 140

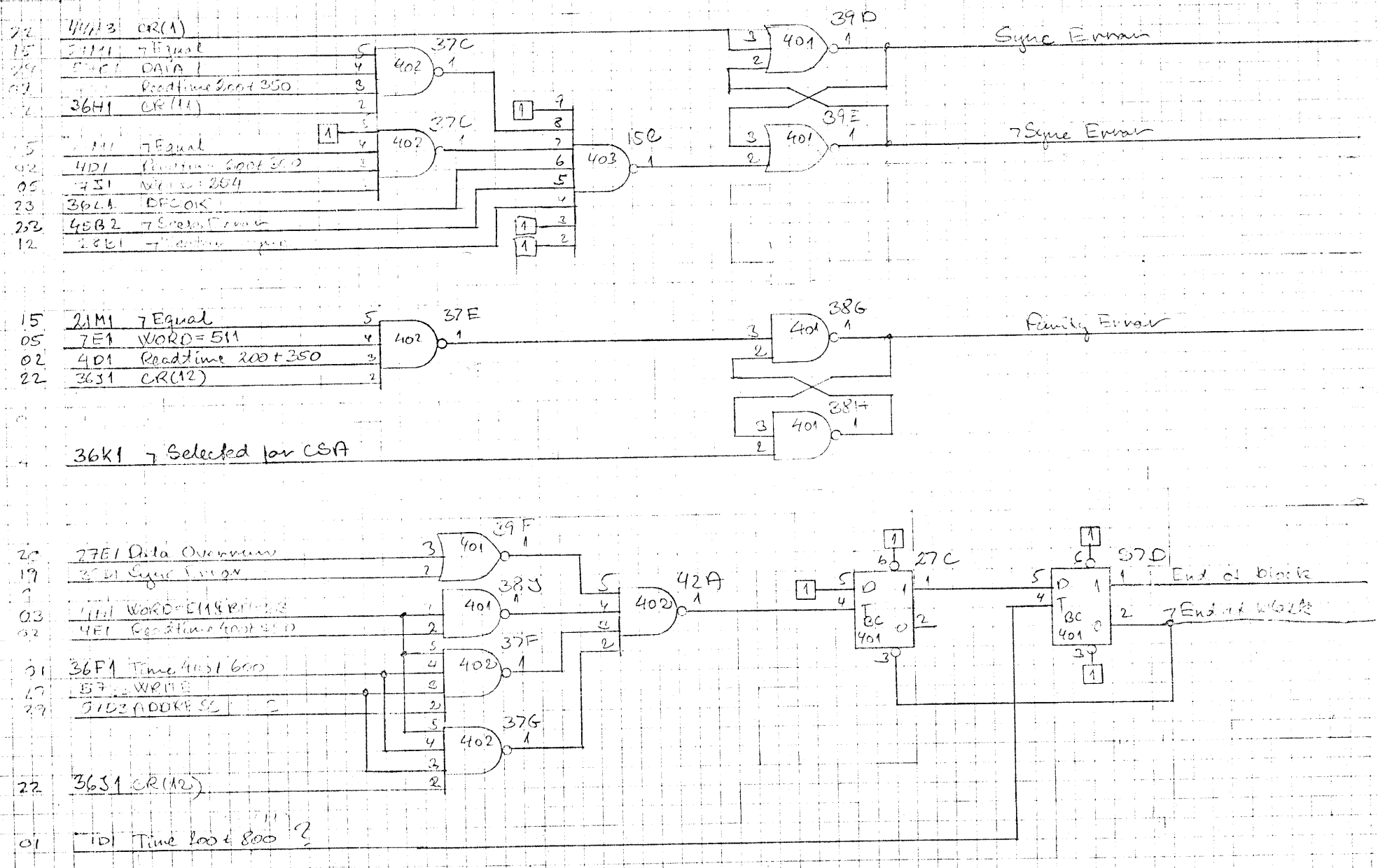


Unit	RC 4000	PW, RC CONTROL, DSD READ-WRITE CONTROL	DEC-
Dwg. No.	V11818		

A/S REGNECENTRALEN

RC doc. V8.140

Designed by | Drawn by | Dwg. Office Check | Design Check | Replaces Dwg. No. | due to ECN | Rep. by Dwg. No.



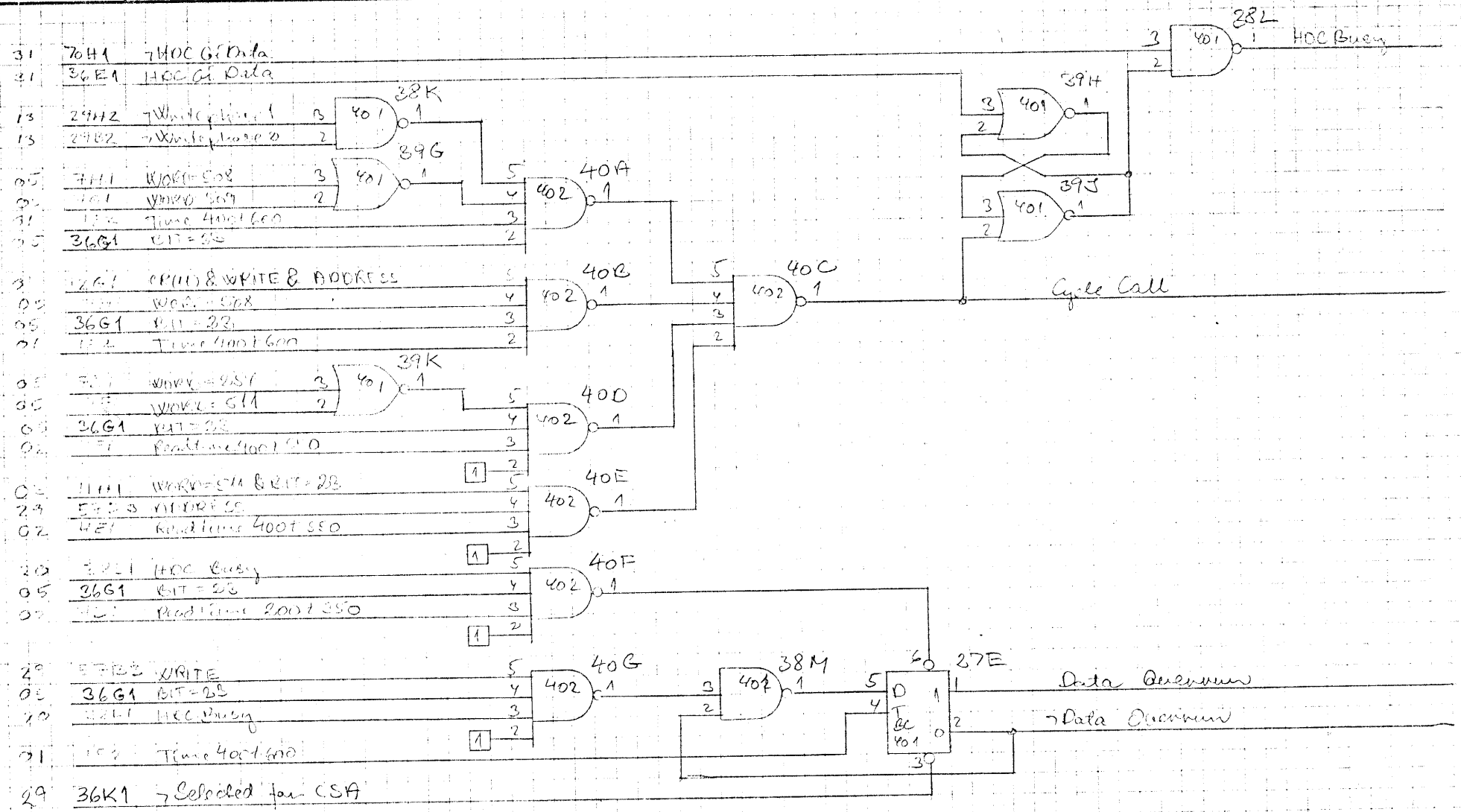
SYNCHRONIZATION ERROR, FAMILY ERROR, END OF BLOCK

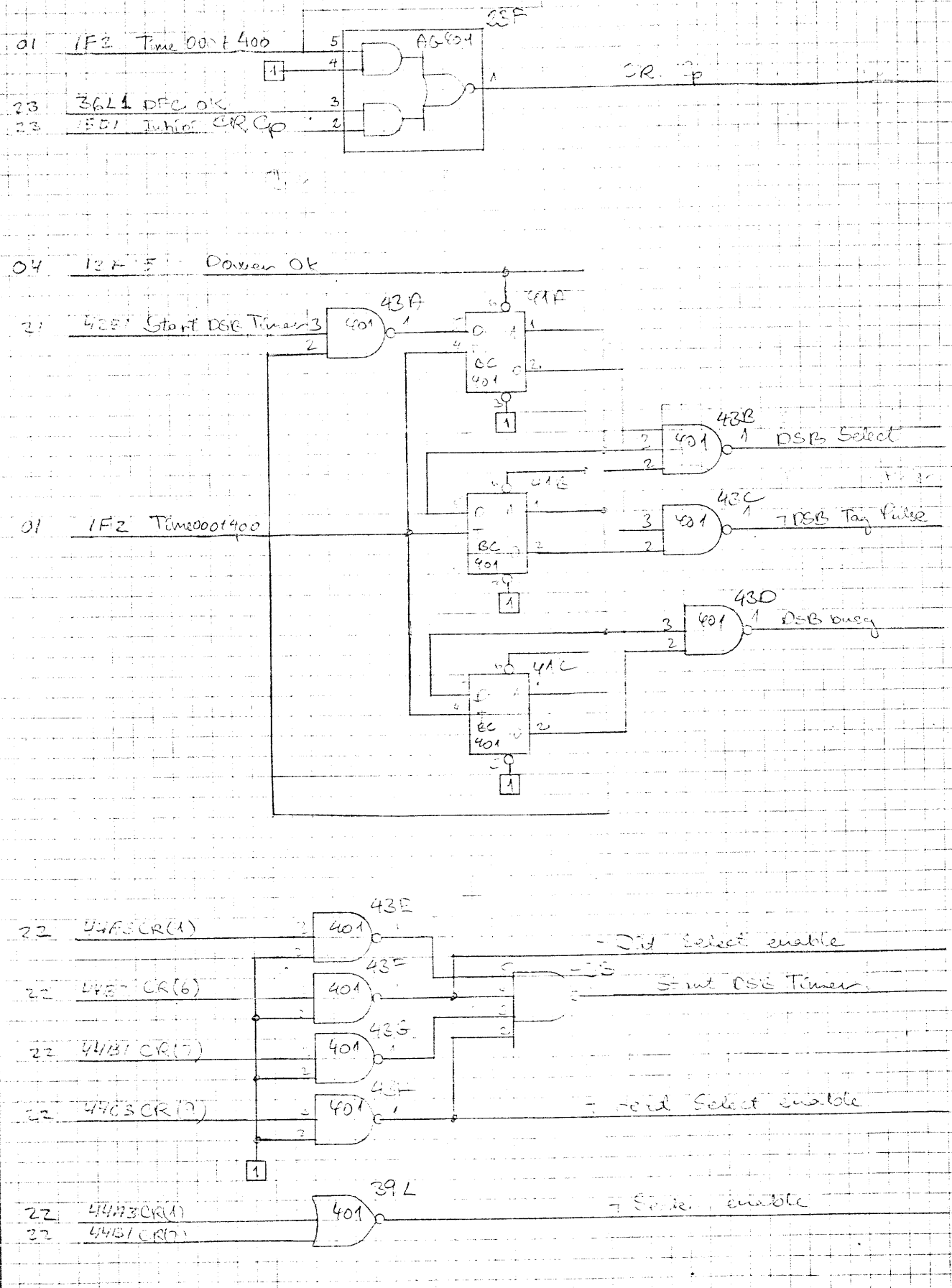
Logic Diagram

Doc: V8.140

A/S REGNECENTRALEN	Designed by	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaces Dwg. No.

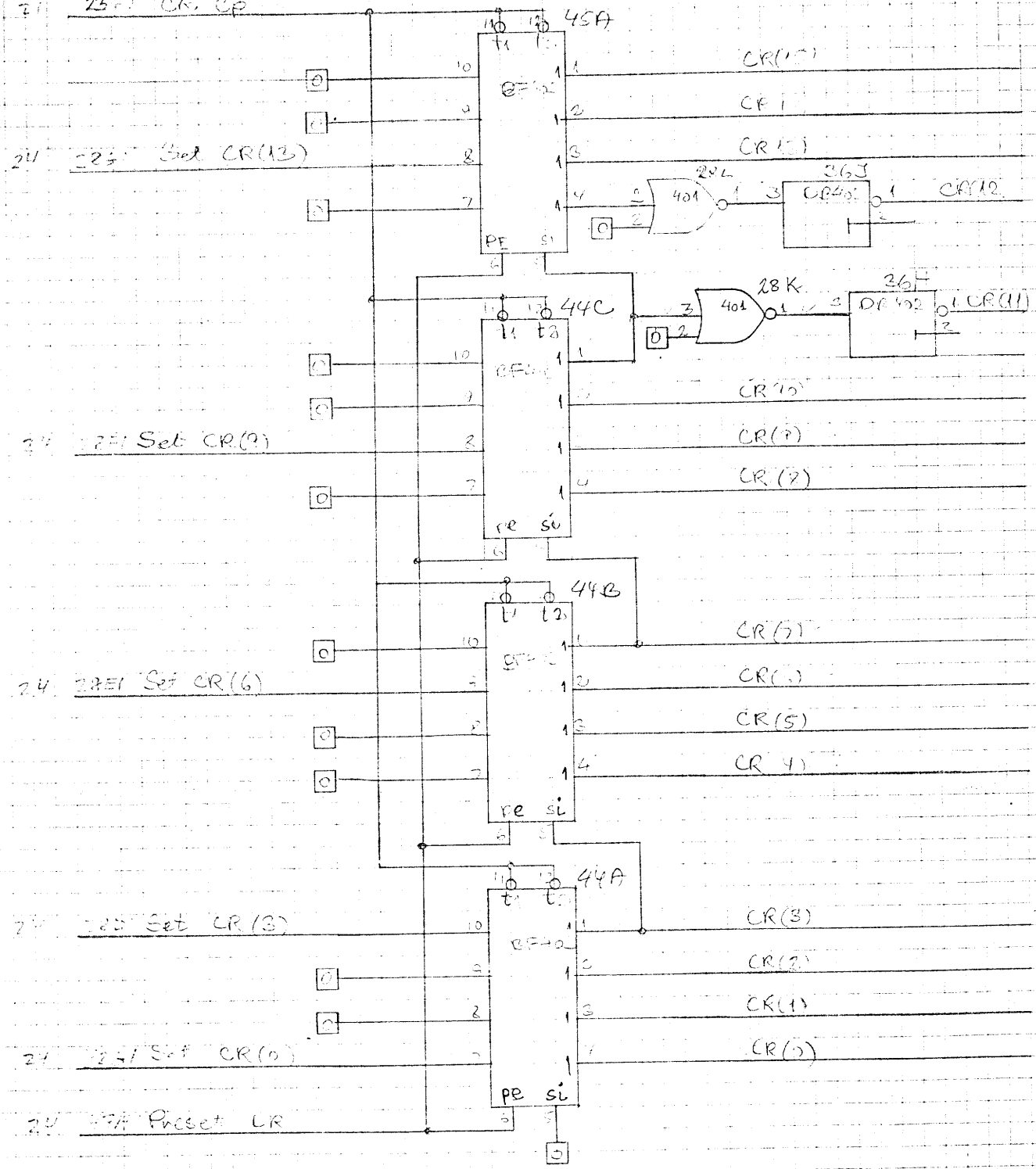
Unit RC4000 Dwg. No. V11R20





Unit	DISK STORAGE BUS TIMER	
Dwg. No. V11821	Logic Diag	

Designed by 17/11/67 FBP
Drawn by
Dwg. Office C
Design Check
Replaces Dwg. No.
due to ECN
Rep
y Dwg. No.
A/S REGNE NTRALEN

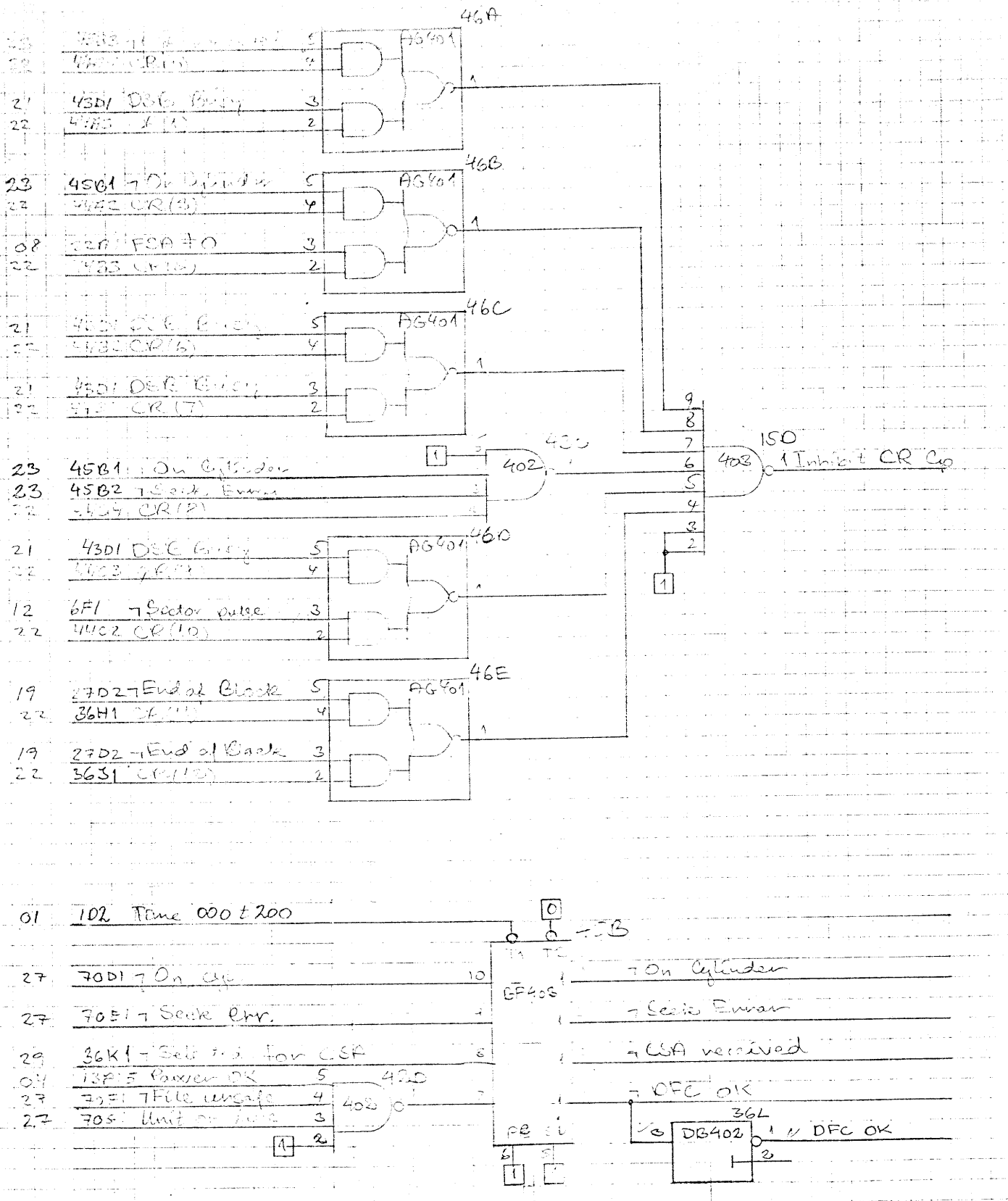


Designed by	Replaces Dwg. No.		
Drawn by	due to ECN		
Dwg. Office Check	Replaced by Dwg. No.		
Design Check			

A/S REGNECENTRALEN

Unit RC4000	CONTROL REGISTER, CR (0:15)	DPC-
Dwg. No. V11822	Logic Diagram	

FC Form V8 140



Unit	CR CONTROL
Dwg. No.	V11823
Designed by	
Drawn by	
Design Check	
Dwg. Office C	
Replaces Dwg. No.	
due to ECN	
Rep. by Dwg. No.	

A/S REGNECENTRALEN

RC doc! V8 140

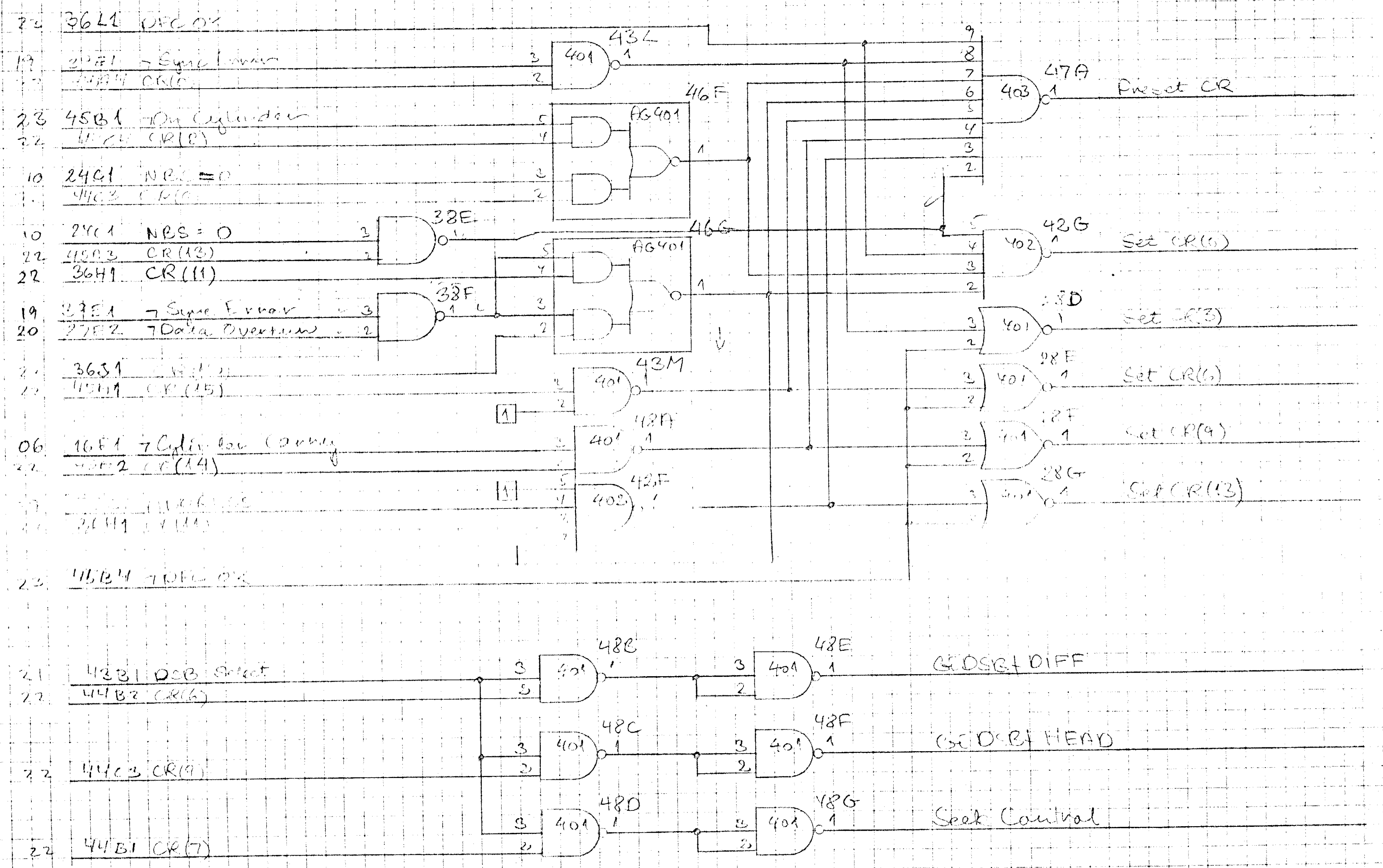
RC doc. VB 140

A/S REGNECENTRALEN	Designed by	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.
	27/1 69 FBP						

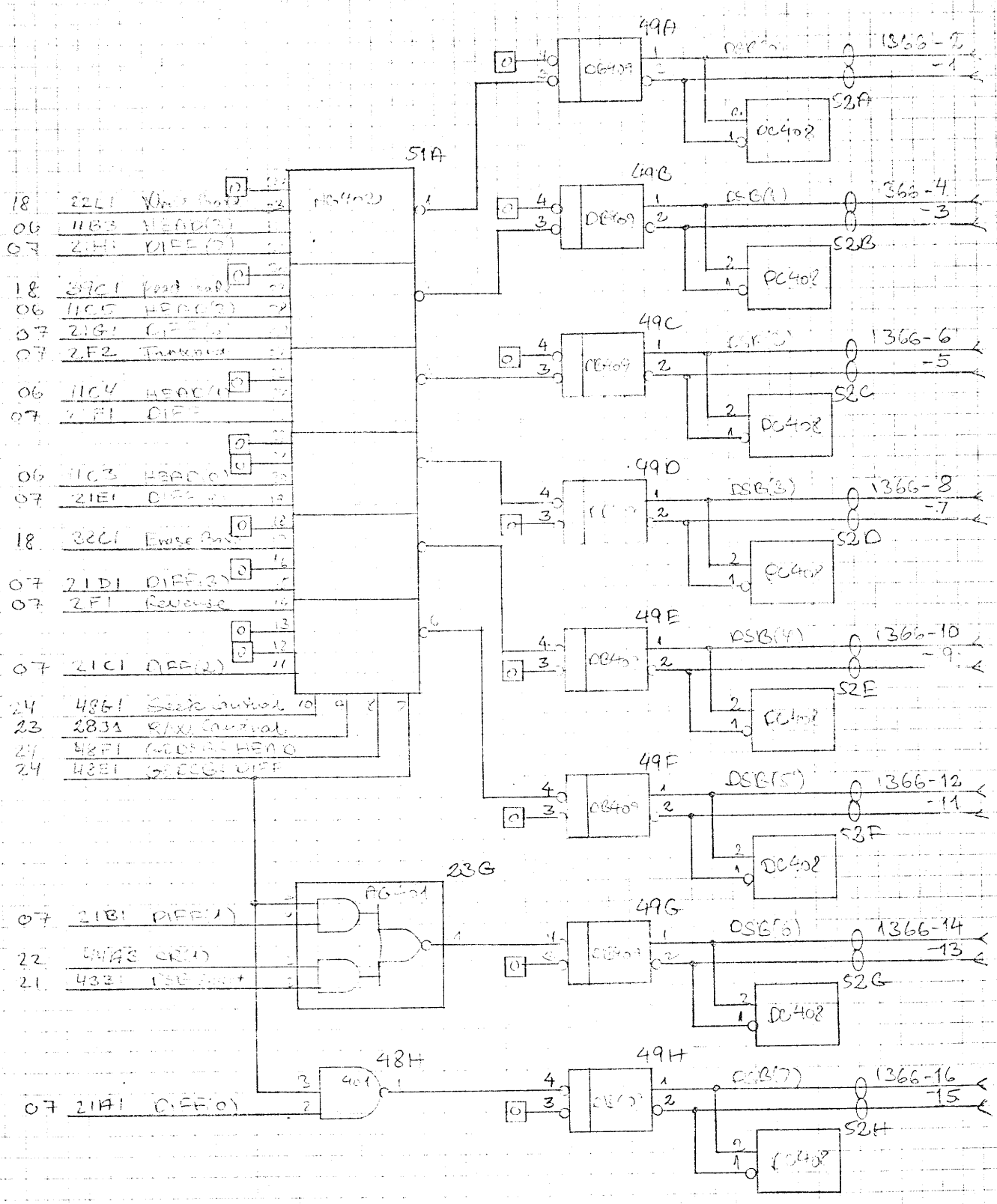
Unit: RC4000

Dwg. No.: V11824

CR JUMP CONTROL
Logic Diagram



DFC-2?

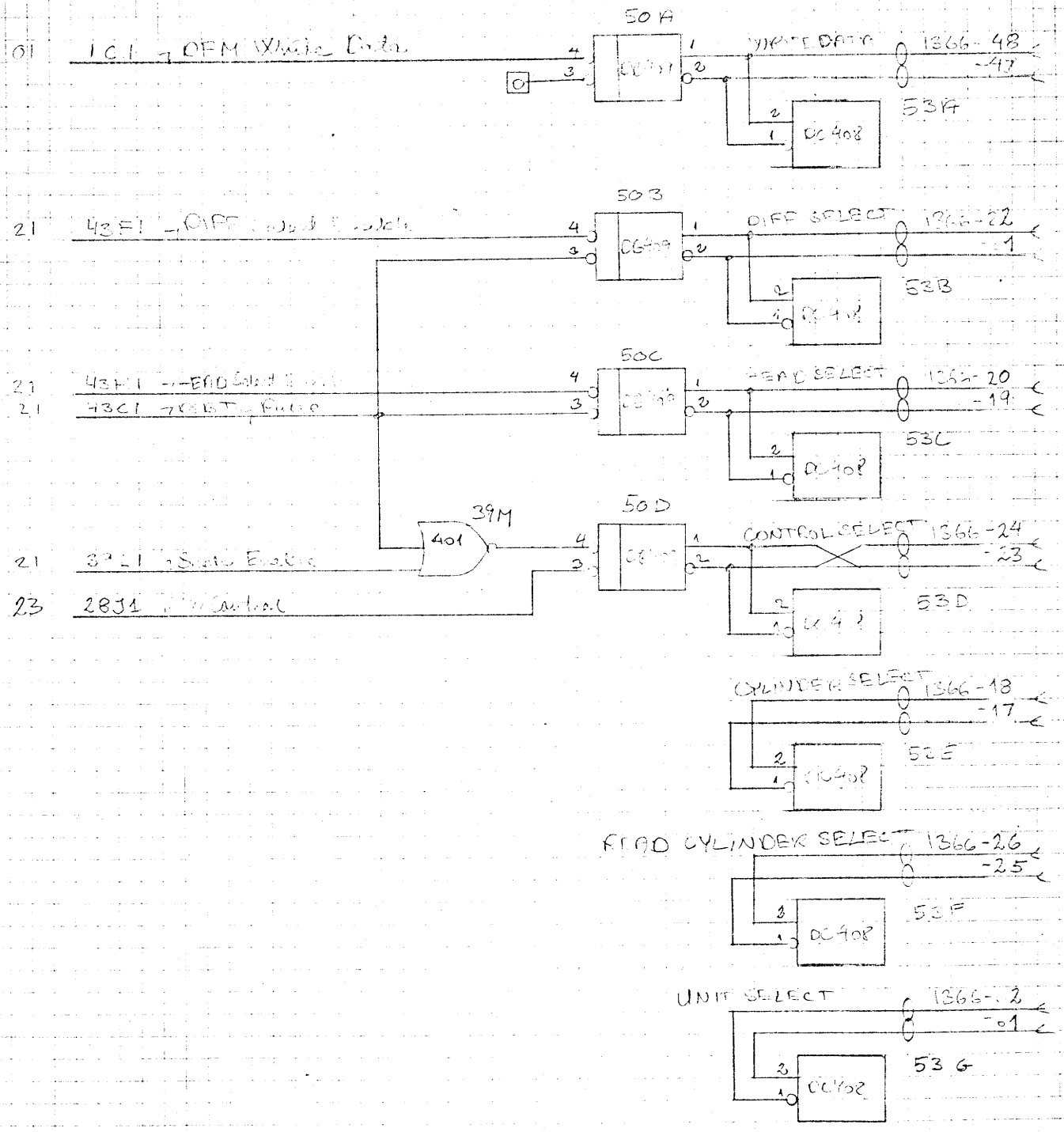


Unit: DC4000	DISK STORAGE BUS, DSB(0-7)		DFC-C25
Dwg. No.: V11825	Logic Diagram		

Designed by: 27/11 68 FHP
Drawn by:
Design Check
Dwg. Office Ch.
Replaces Dwg. No.
Rep. by Dwg. No.
due to ECN

A/S REGNECENTRALEN

DC 4000 V9.140

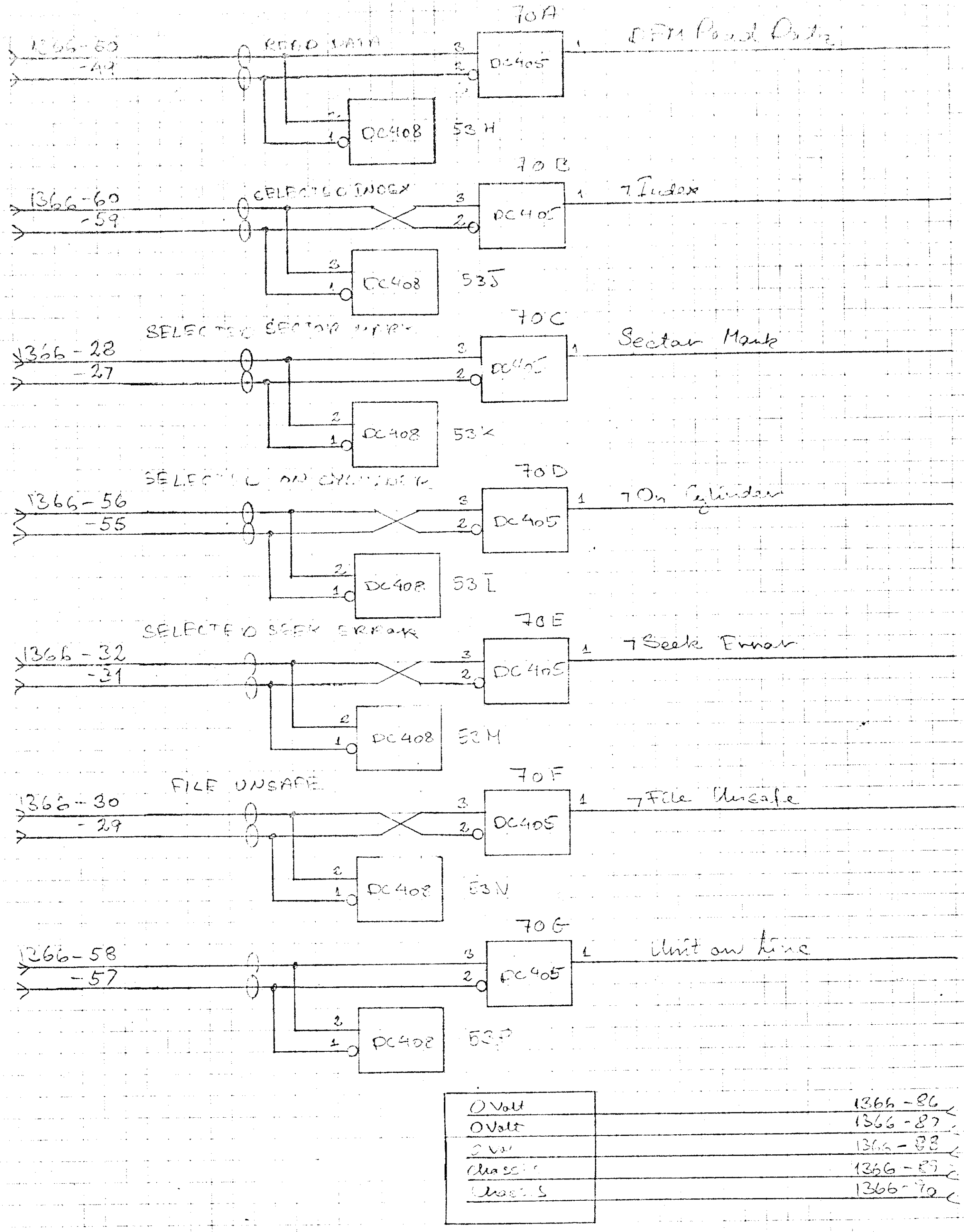


Rep. by Dwg. No.					
due to ECN					
Replaces Dwg. No.					
Design Check					
Dwg. Office C					
Drawn by					
Designed by					

A/S REGNECENTRALEN

Unit RC4000	SIGNALS FROM CONTROLLER TO DSD	DFC-033
Dwg. No. V11826	Logic Diagram	

IC doc. V3.140



Replaced by Dwg. No. | due to ECN | Replaces Dwg. No. | Design Check | Dwg. Office Check | Drawn by | Designed by 20.10.69 FBF

A/S REGNECENTRALEN

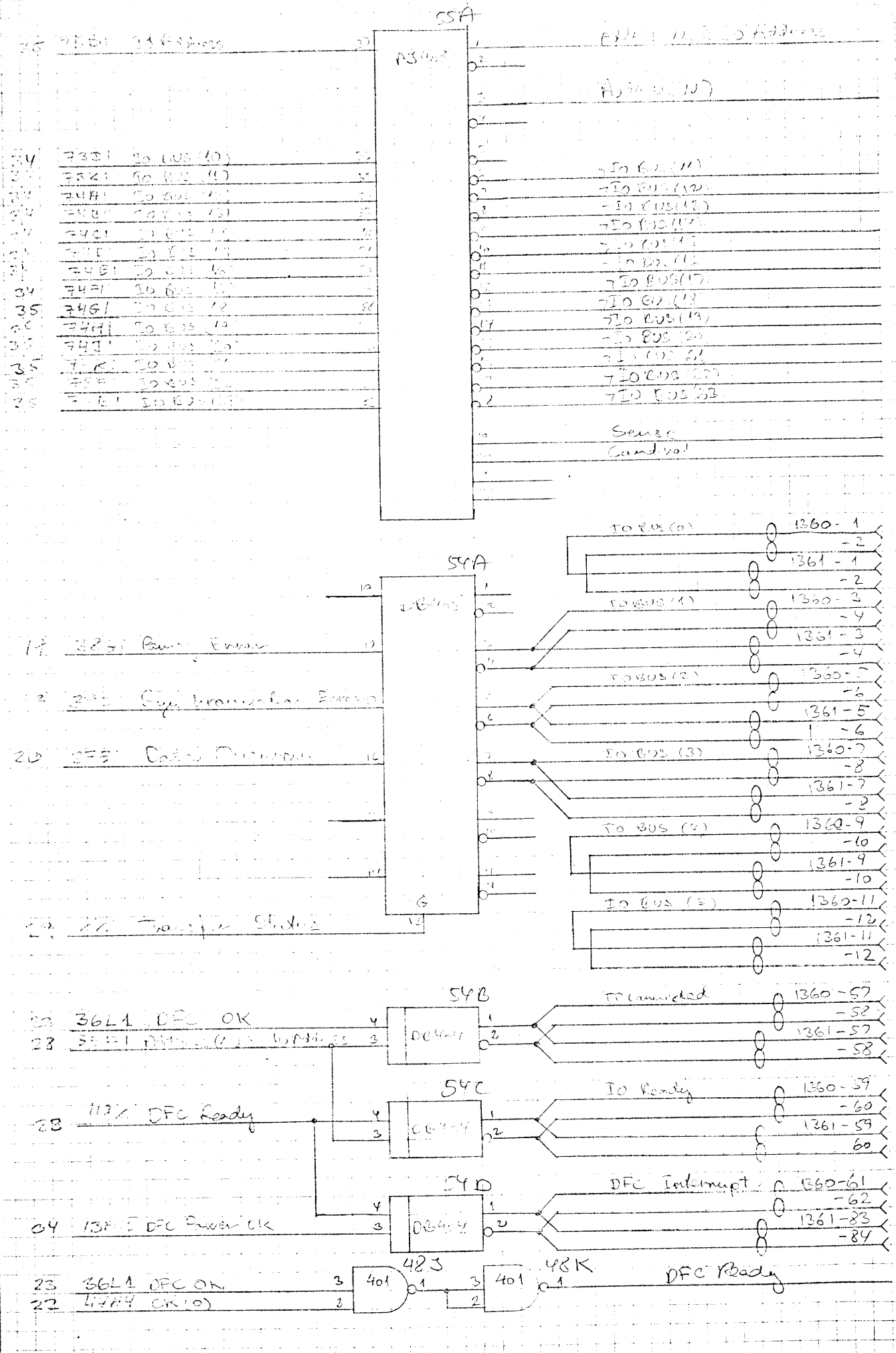
Unit: RC 4000

Dwg. No. V11827

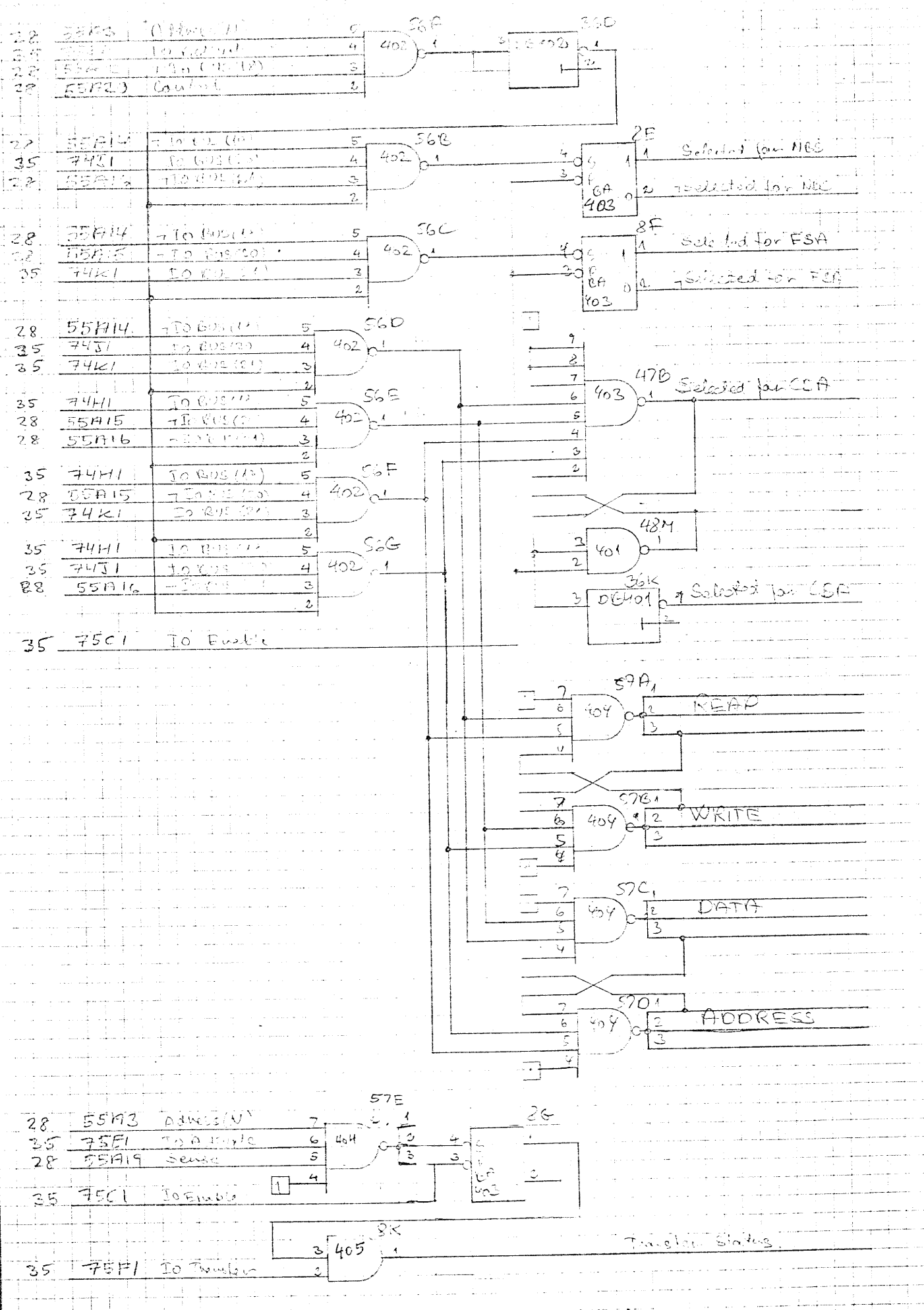
Signals from UCD to ...

Logic Diagram

DFC-27



Unit	DFC-22		
Dwg. No. V11828	Logic Diagram		

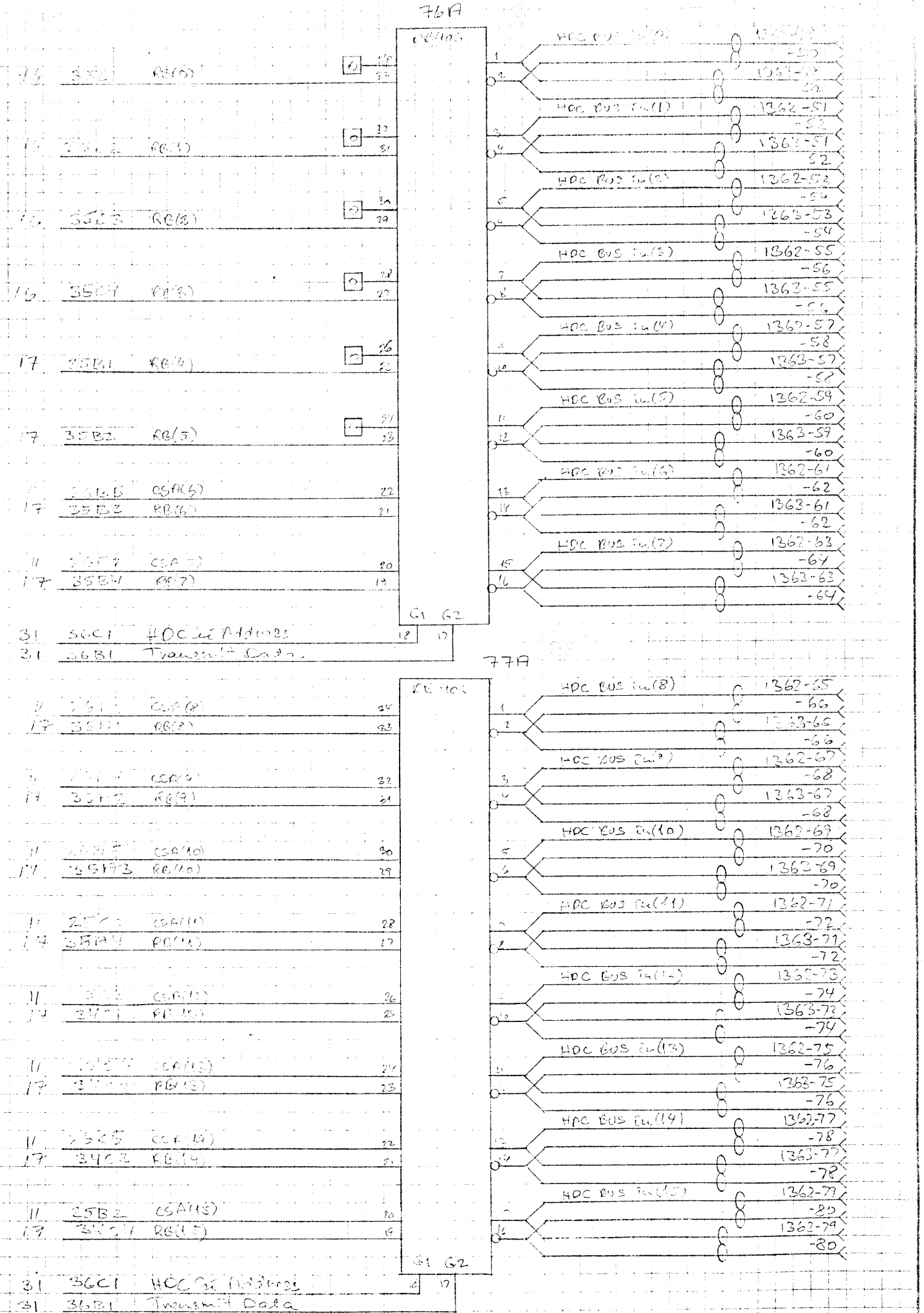


Unit

Dwg. No. V11829

A/S REGNECENTRALEN

Designed by | Drawn by | Dwg. Office Check | Replaces Dwg. No. | Replaces Dwg. No. due to ECN

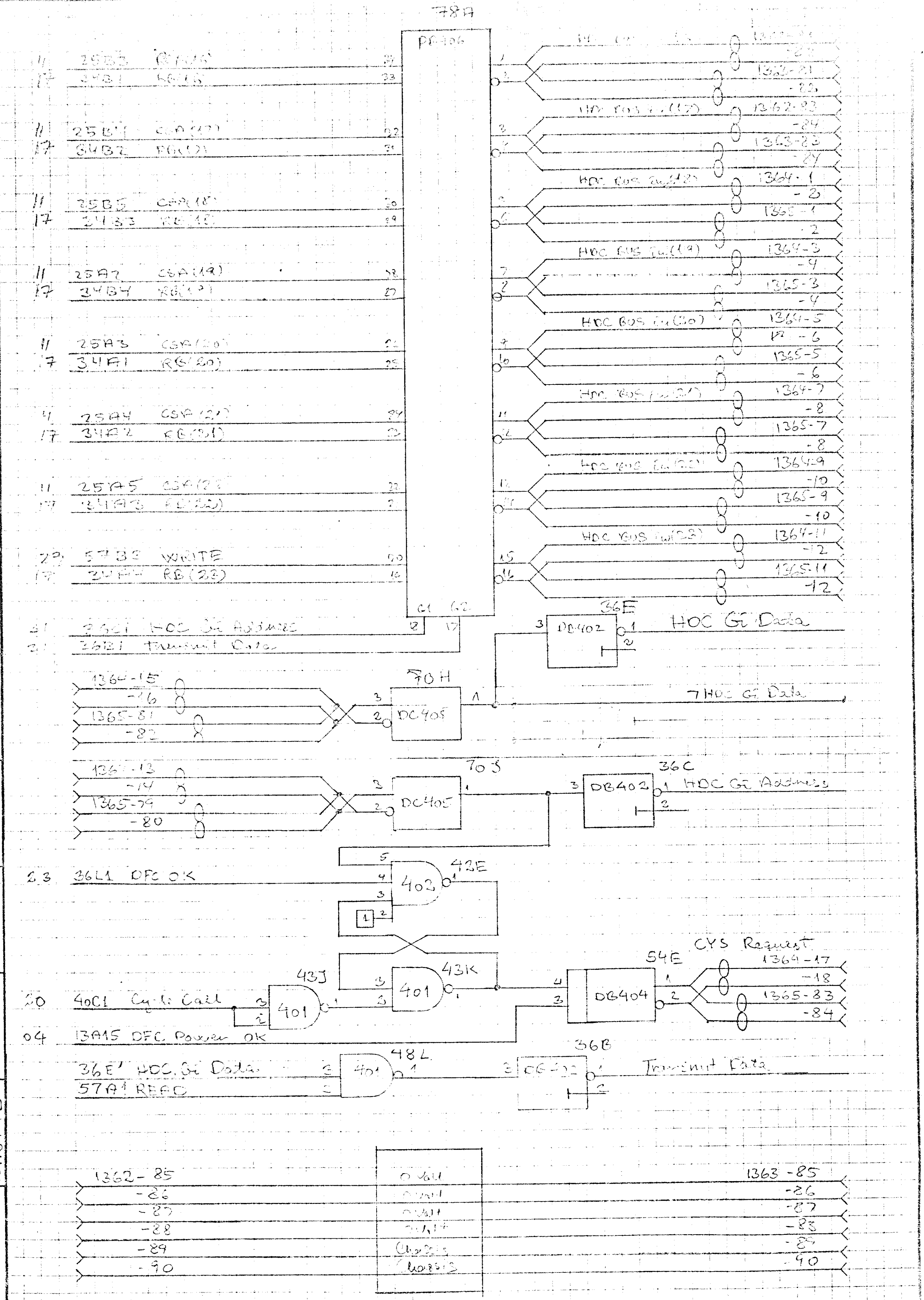


Unit	R4000	HDC BUS Ch(0:15)
Dwg. No.	V11830	basic Drawing

HDC-30

A/S REGNTRALEN

Designed by | Drawn by | Dwg. Office | Design Check | Replaces Dwg. No. | due to ECN | Rel. by Dwg. No.



A/S REGNECENTRALEN

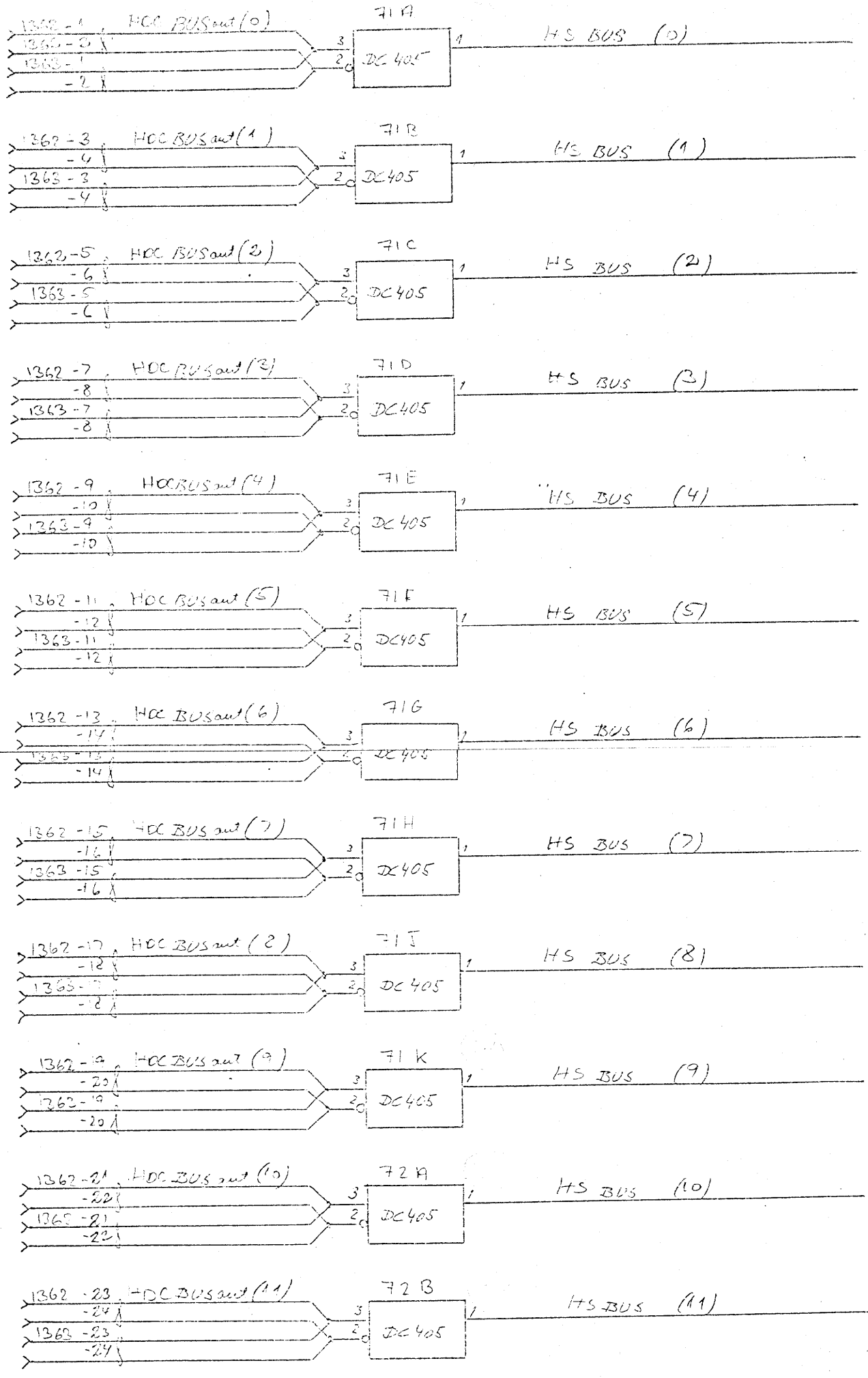
Designed by 18.11.69 FBP | Drawn by | Dwg. Office Check | Design Check | Replaces Dwg. No. | due to ECN | Replaced by Dwg. No.

Unit: RC 4000

Dwg. No. V11831

HDC BUS In(16:23) and HDC Control

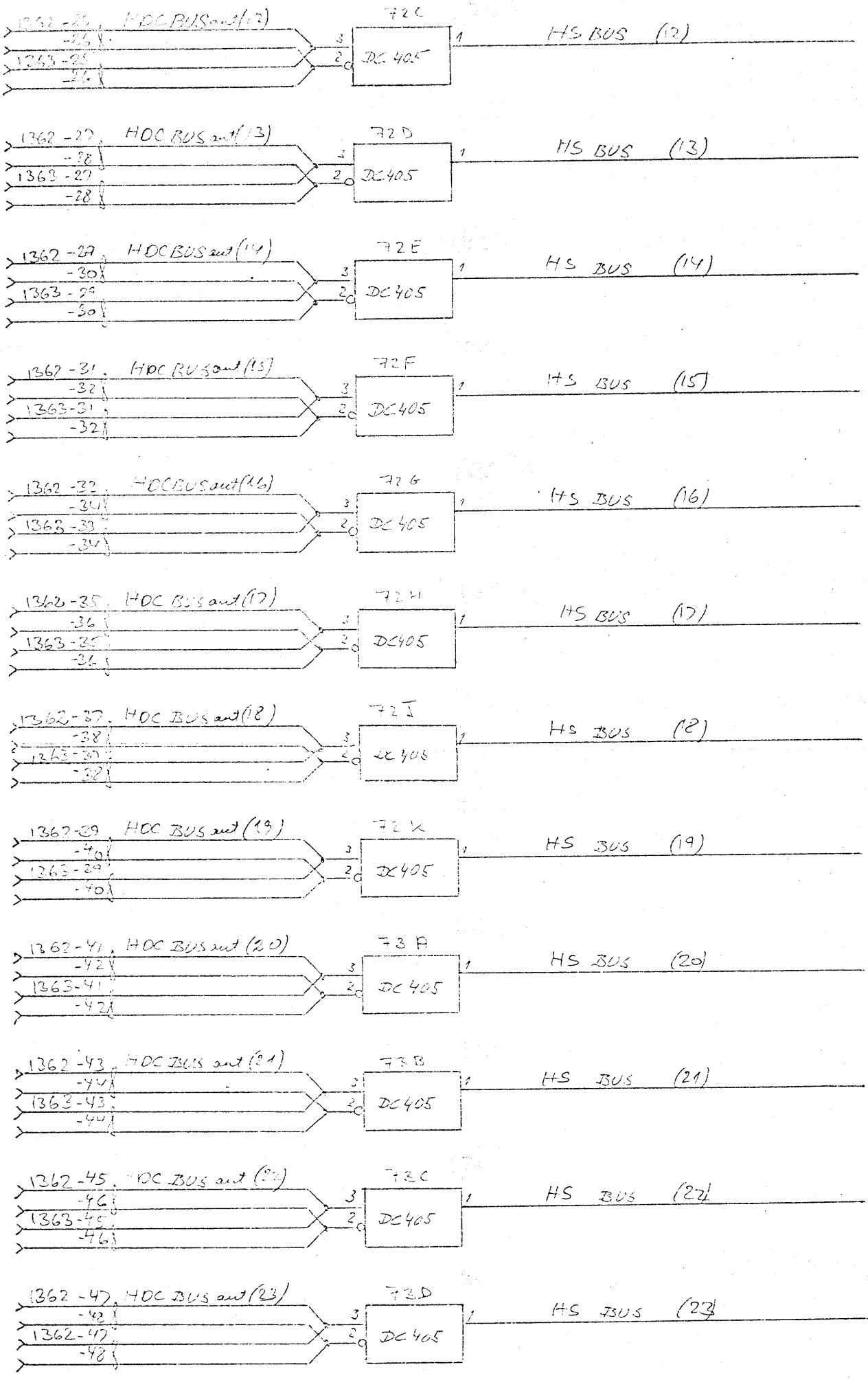
Logic Diagram



Unit RC4000	HDC BUS-out (0:11)	DPC-0882
Dwg. No. V11832	Logic Diagram	

Designed by 221169 FBK
Drawn by
Dwg. Office
Design Check
Replaces Dwg. No.
Dwg. No. due to ECN
By
AIS REGNECENTRALEN

PEP formular 6/11 68



Unit: RC4000

Dwg. No. V11833

HDC BUS ant (12:23)

Logic Diagram

OFC 033

A/S REGNTRALEN

Designed by 3821169 FBK

Drawn by

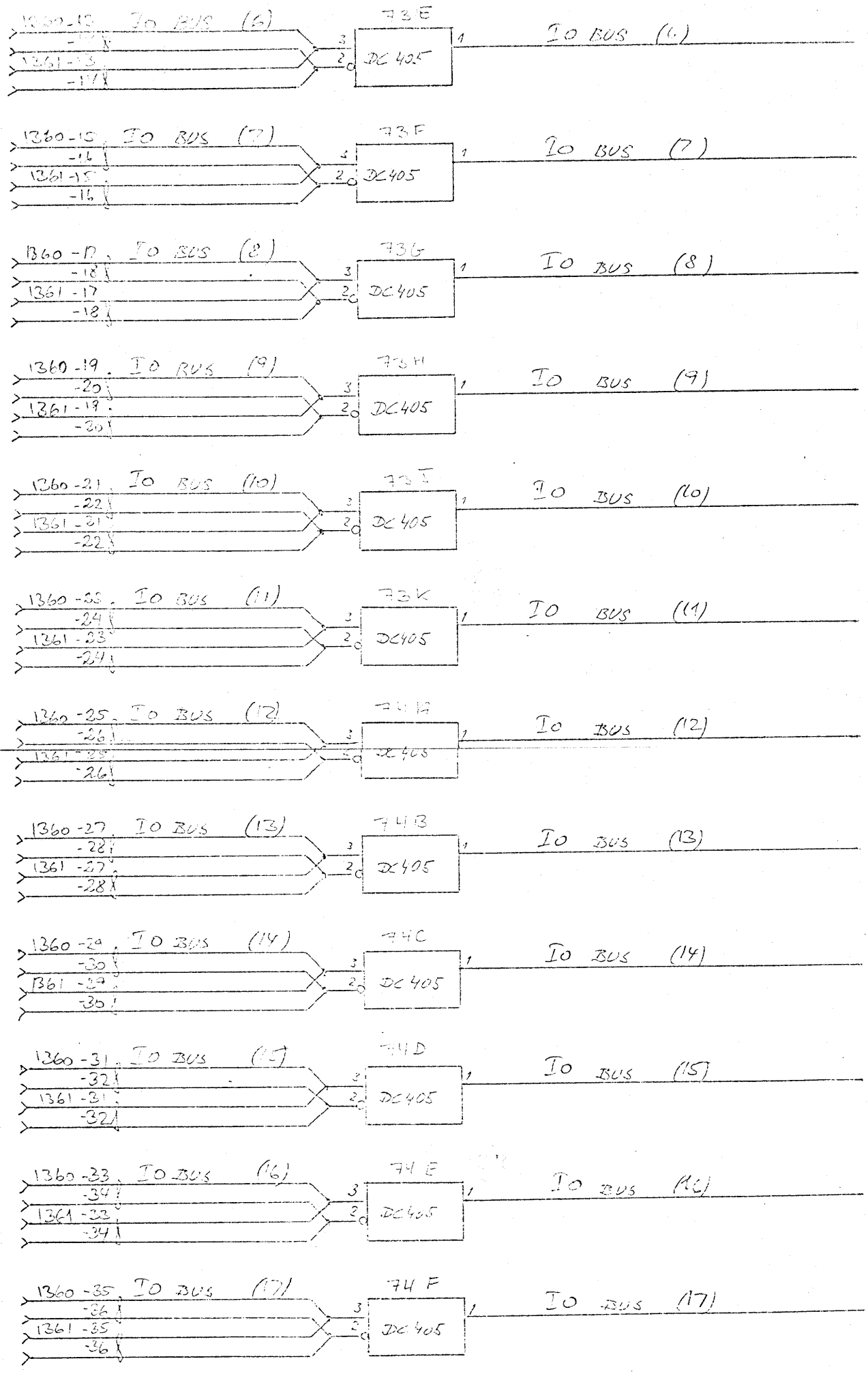
Design Check

Dwg. Office

Replaces Dwg. No.

Issued due to ECN

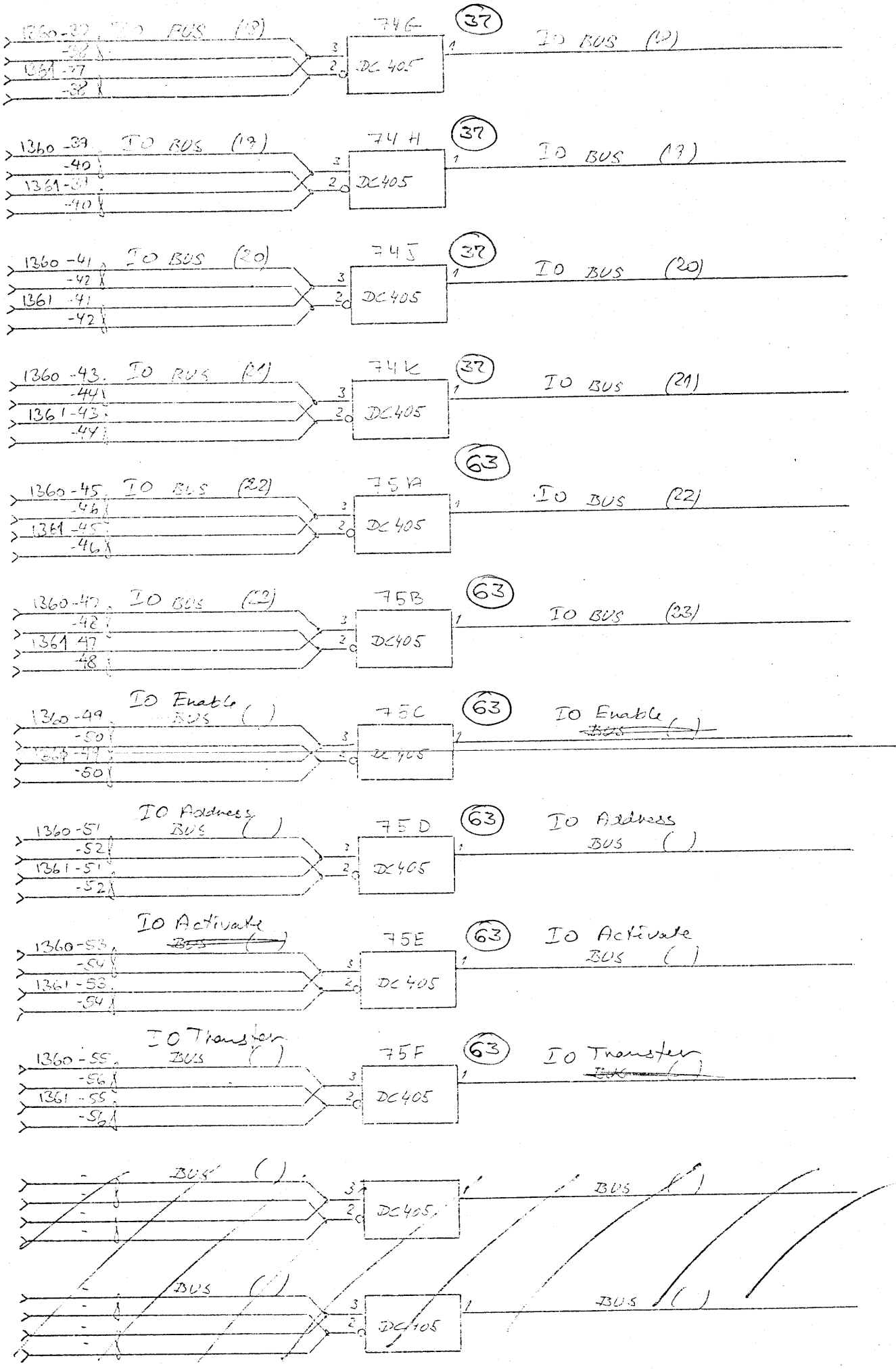
Issued by Dwg. No.



Replaces
Design Check
Dwg. Office
Drawn by
Designed by 28/11/69 FRP
ITRALEN
A/S REGN

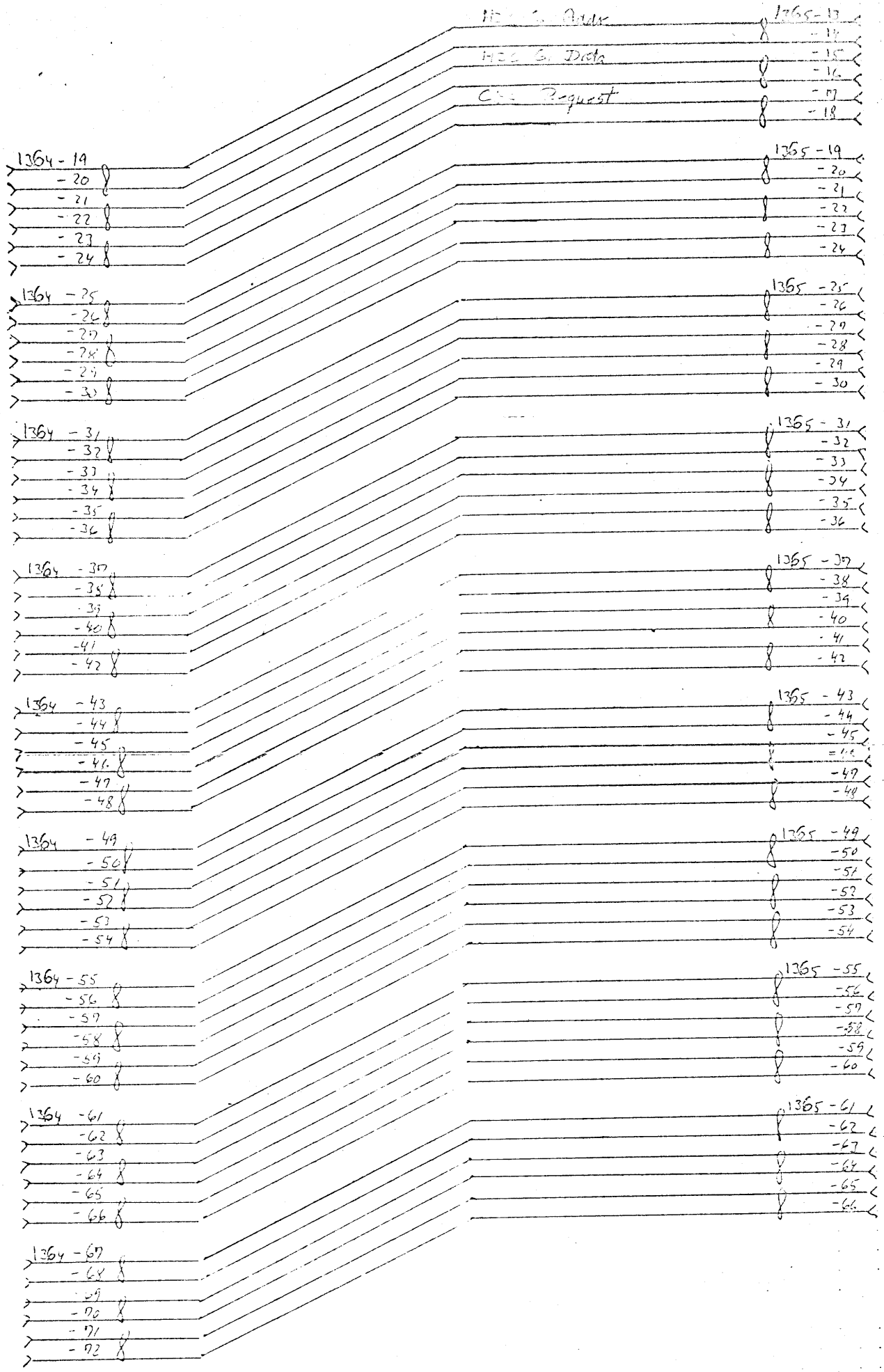
Unit RC4000
Dwg. No. V11834
IO BUS (6:17)
Logic Diagram
DFC 334

EPICP formular 8/11 68



Unit: RC4000	IO BUS (18:23) IO Enable, IO Address, IO Activate, and IO Transfer Logic Diagram	DRG 025
Dwg. No. V11835		

A/S REGNTRALEN
Designed by 28/11 69
Drawn by
Dwg. Office
Design Check
Replaces Dwg. No.
Revised by Dwg. No. due to ECN



Designed by
Drawn by
Dwg. Office
Design Check
Replaces Dwg. No.
R' by Dwg. No.
due to ECN

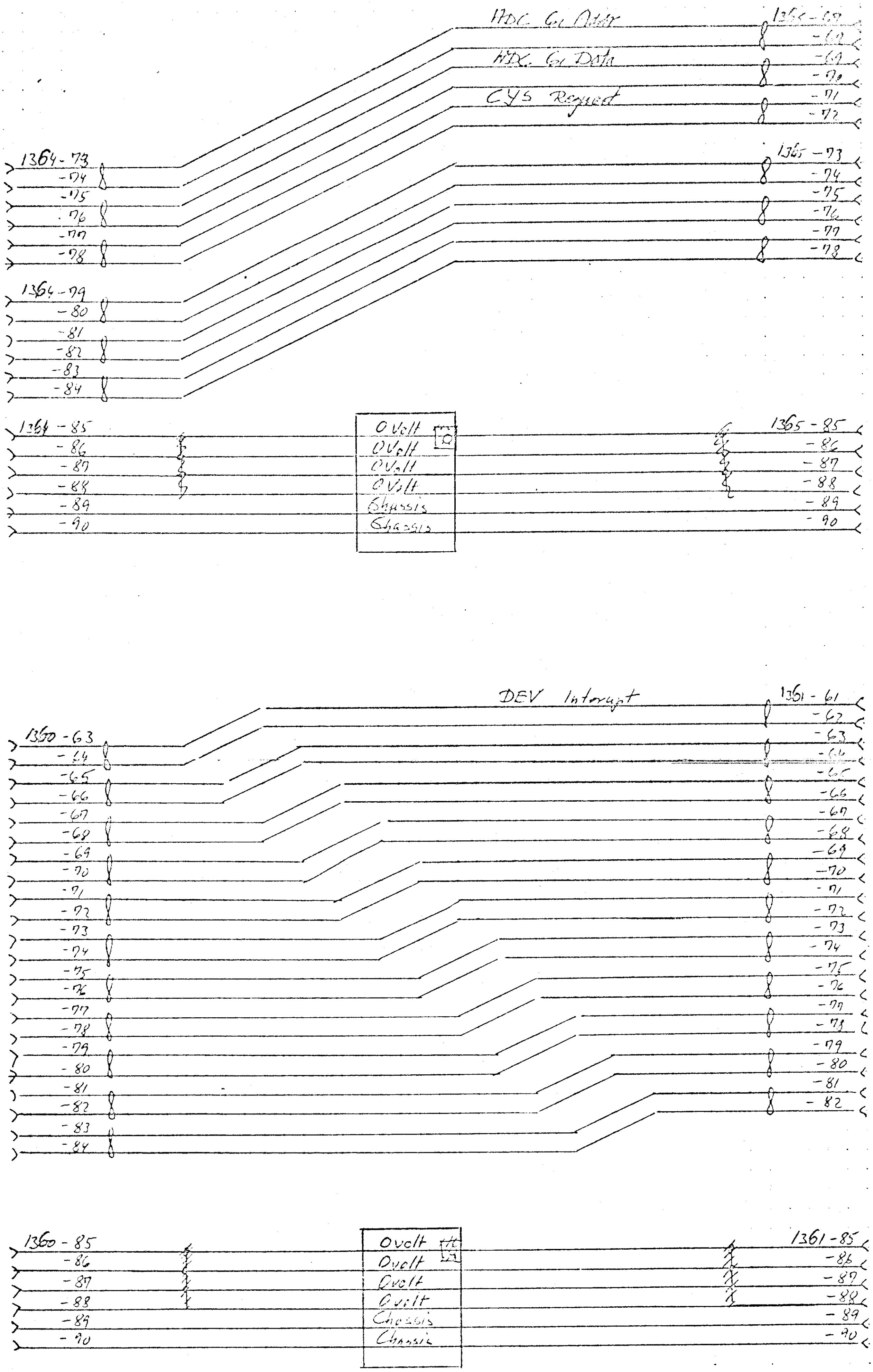
CENTRALEN A/S REGN

Unit RC4000

Dwg. No. V11836

HDC Cable Connections
Logic Diagram

DFC036



Designed by 22/10-68 PEP · 090369 PEP · 281169 PEP
Drawn by
Dwg. Office
Design Check
Replaced Dwg. No.
due to ECN
Replaced by Dwg. No.

A/S REGNECENTRALEN

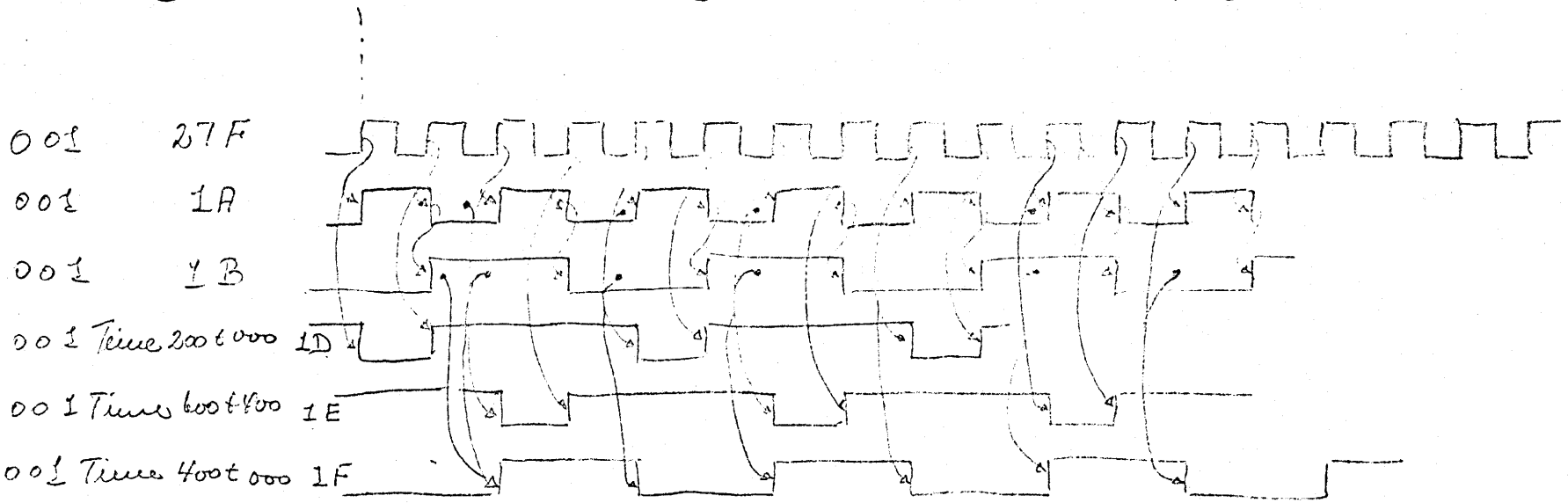
Unit: RC4000

Dwg. No. V11837

HDC and LDC Cable Connections

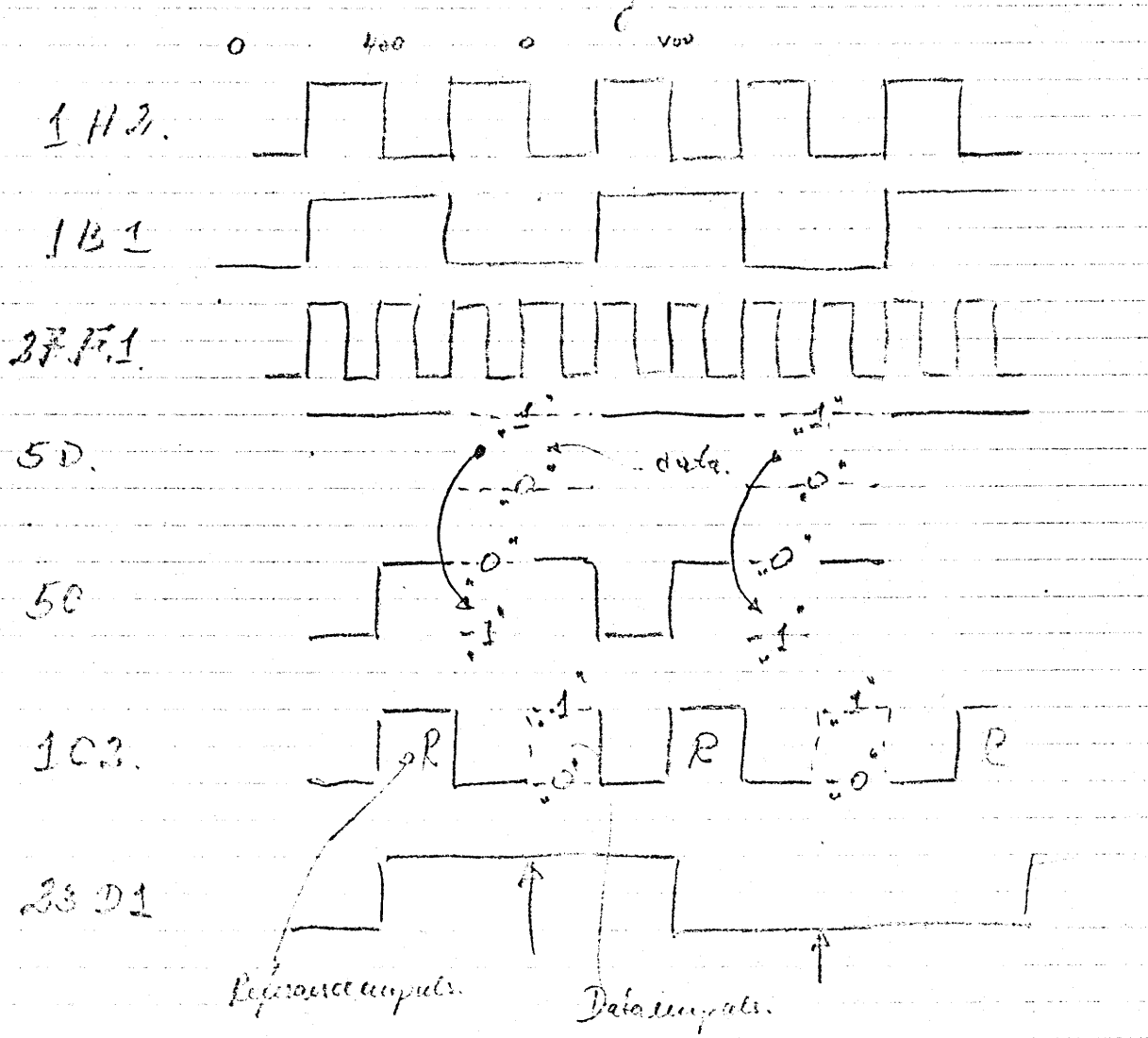
Logic Diagram

DFC037

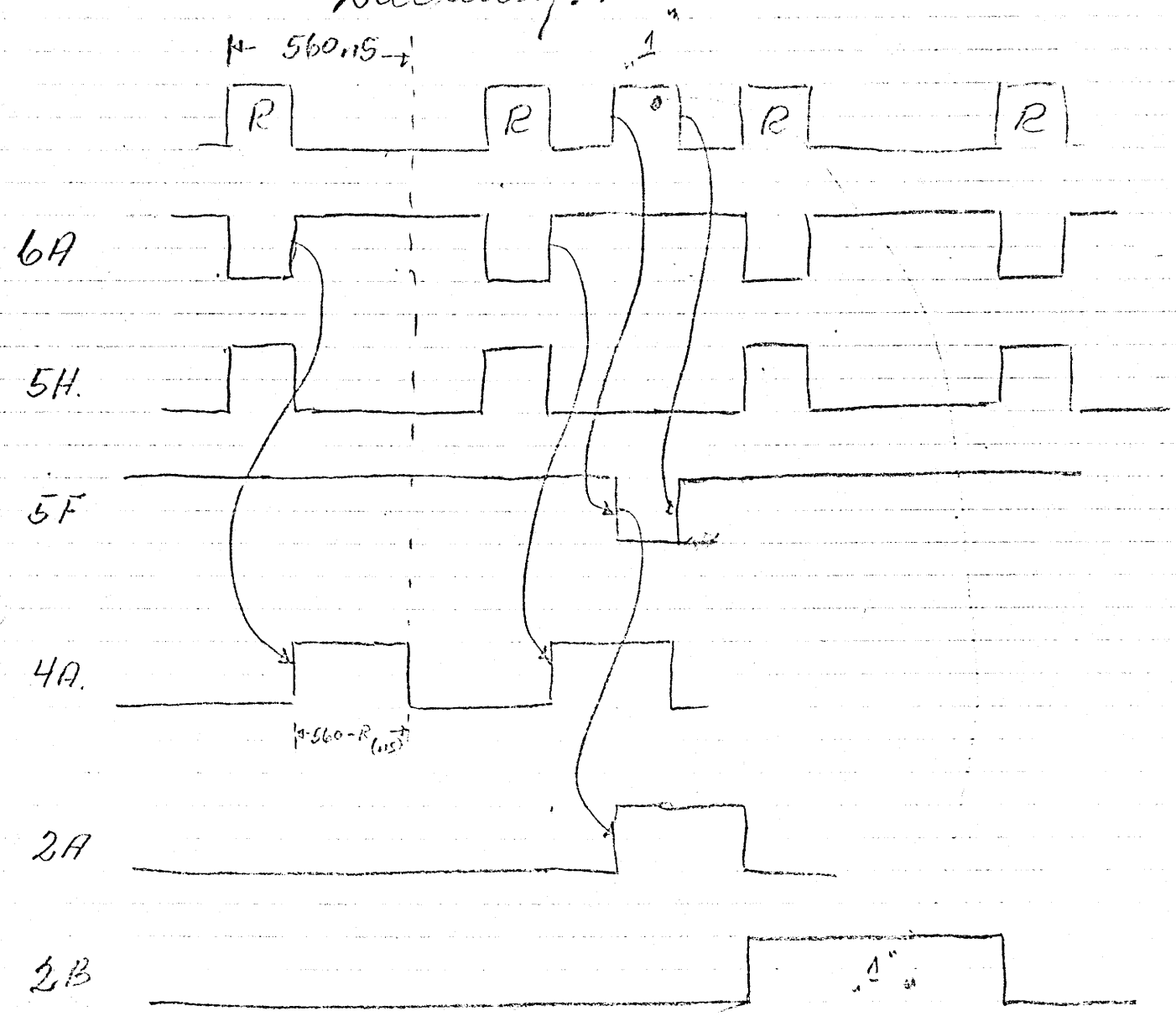


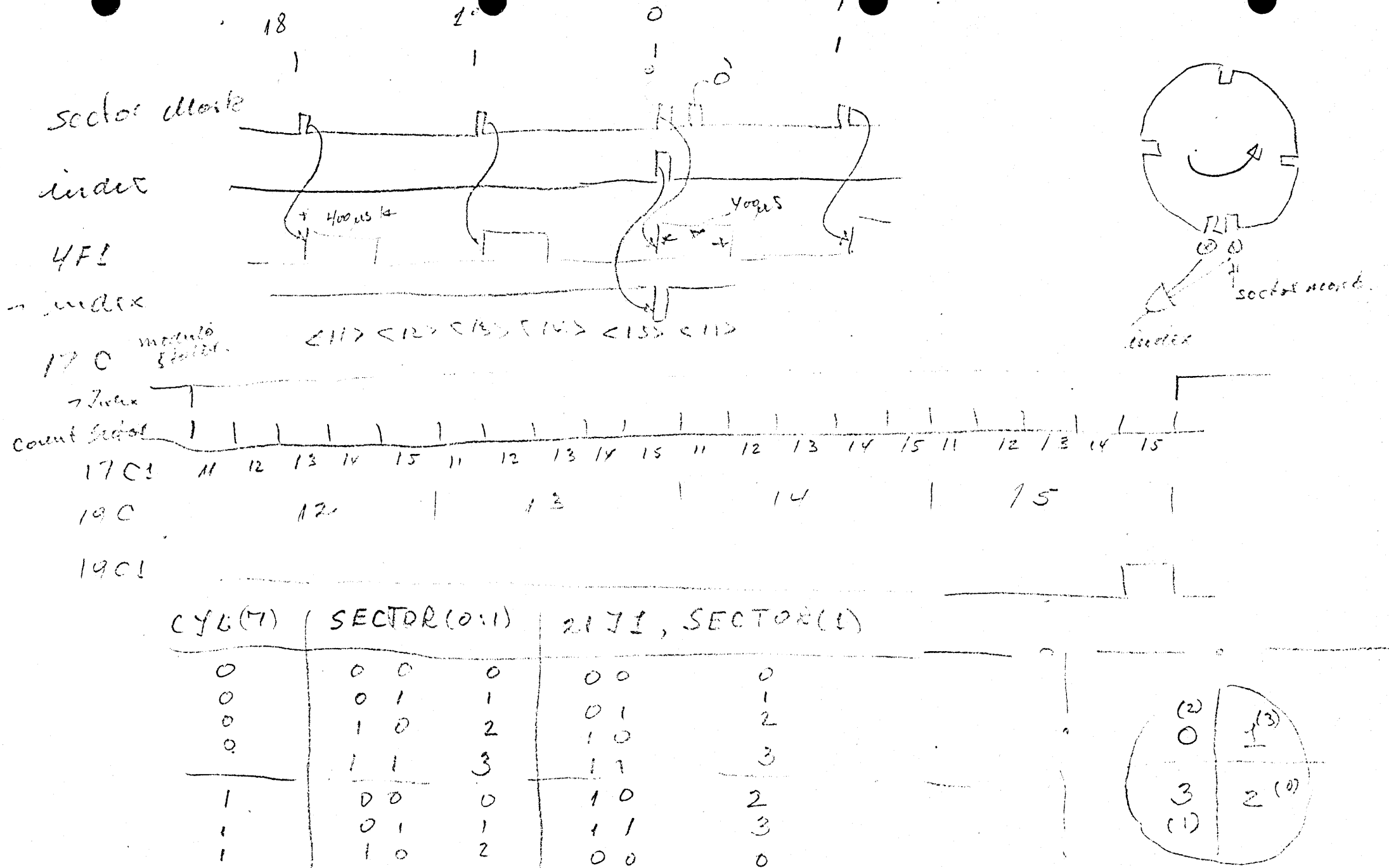
Indus Timing.

Séquence.

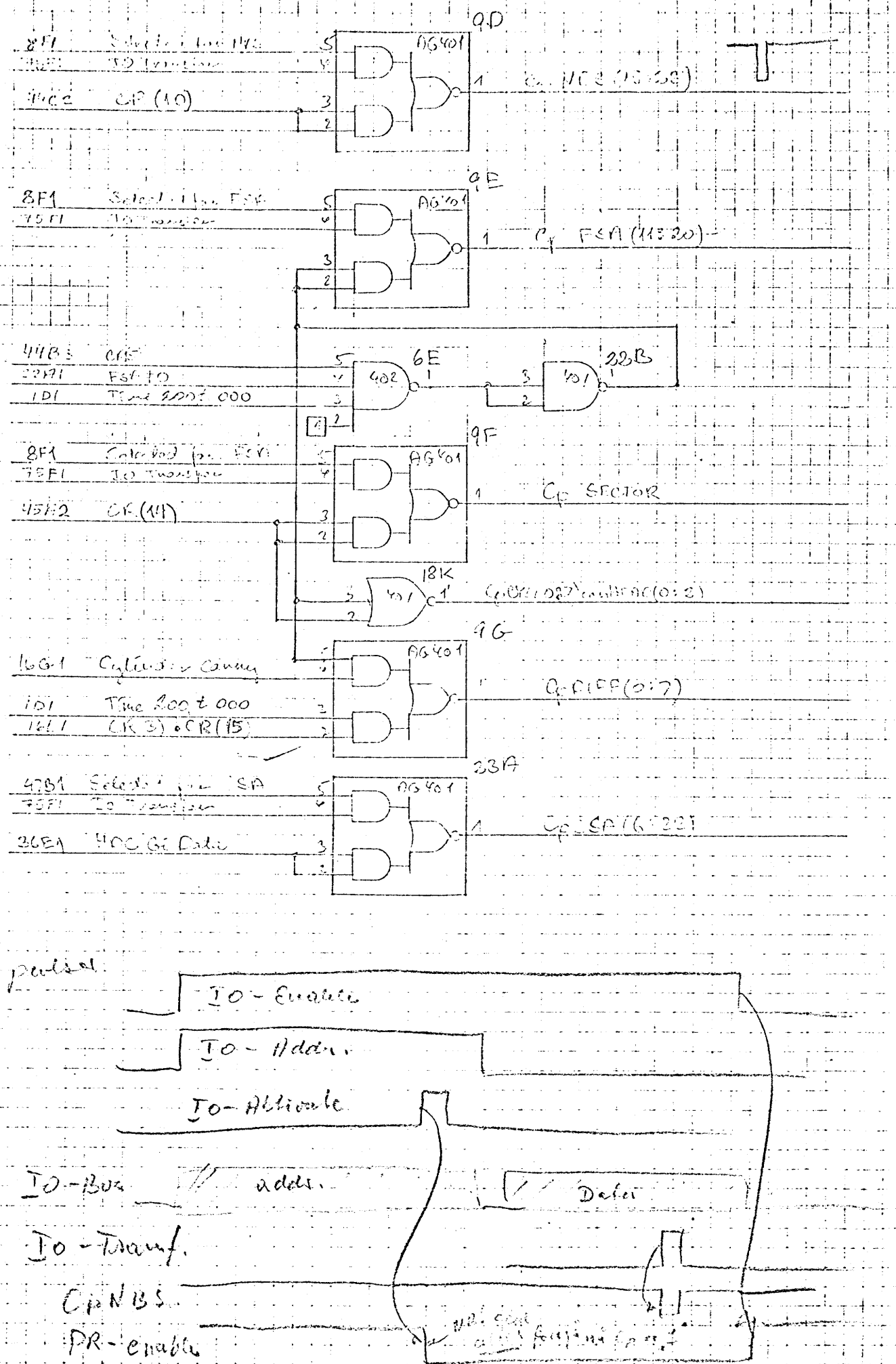

0
+5V
0
+5V
1 H2.
1 B1
23 F1.
5 D.
data.
5 C
1 C2.
R
R
R
23 D1
Reference impuls.
Data impuls.

Loesung!!





CYL(7)	SECTOR(0:1)		21 J1, SECTOR(1)	
0	0 0	0	0 0	0
0	0 1	1	0 1	1
0	1 0	2	1 0	2
0	1 1	3	1 1	3
1	0 0	0	1 0	2
1	0 1	1	1 1	3
1	1 0	2	0 0	0
1	1 1	3	1 0	1

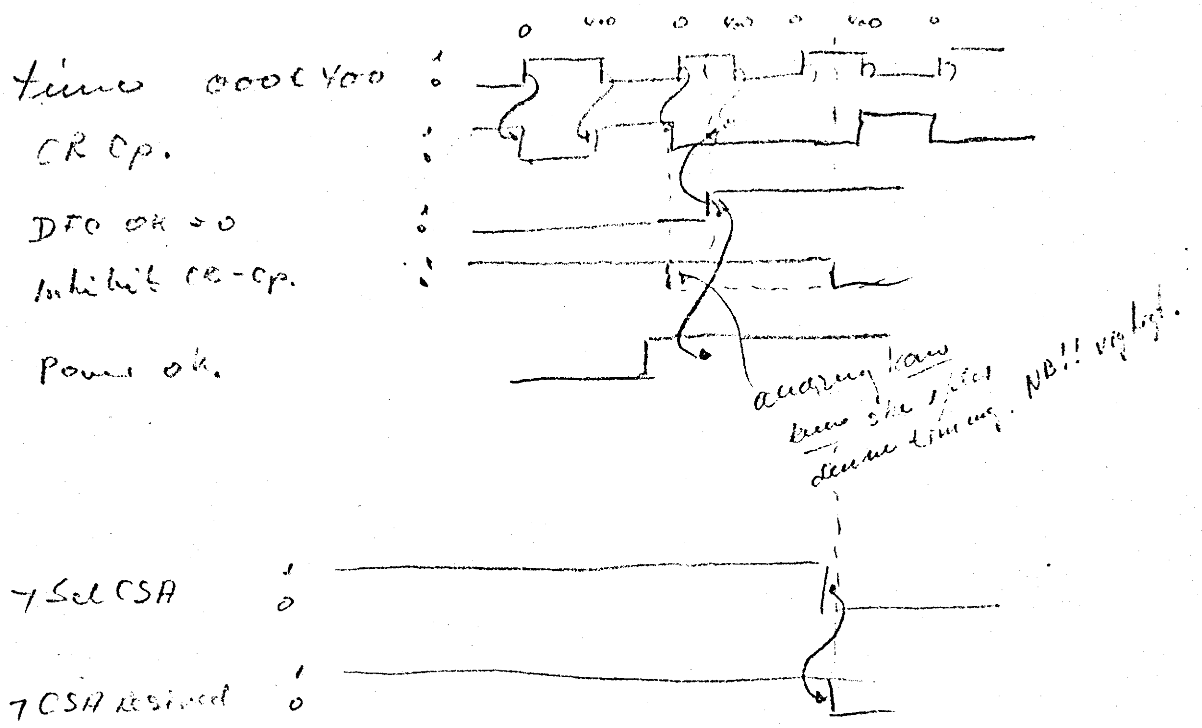


Unit	CLOCKPULSES FOR MBG, FSA, SECTOR, CYL. ADDRESS			DEC - 7
Dwg. No.				CSA

Drawn by | Designed by | Dwg. Office | Design Check | Replaces Dwg. No. | Due to ECN | Dwg. No.

NTRALEN

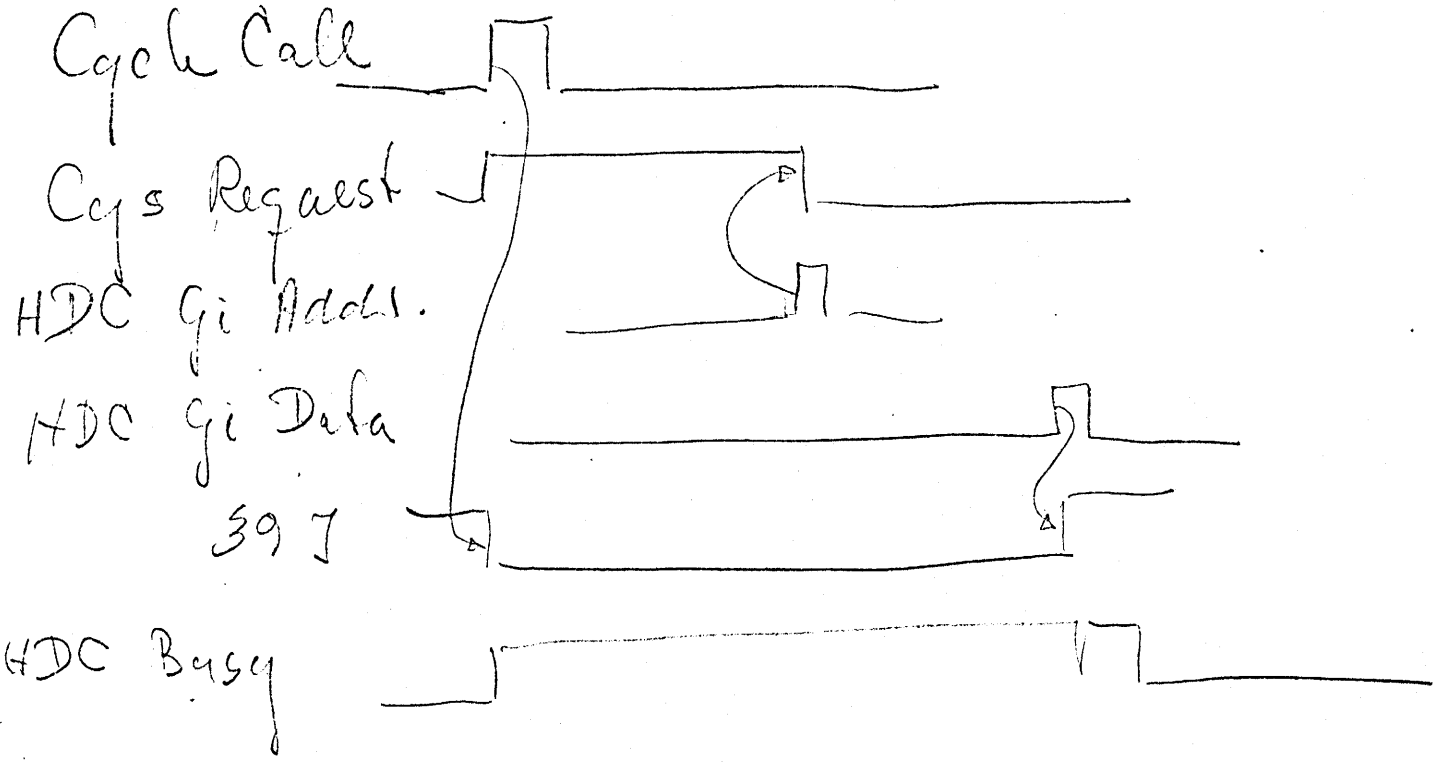
A/S REGI

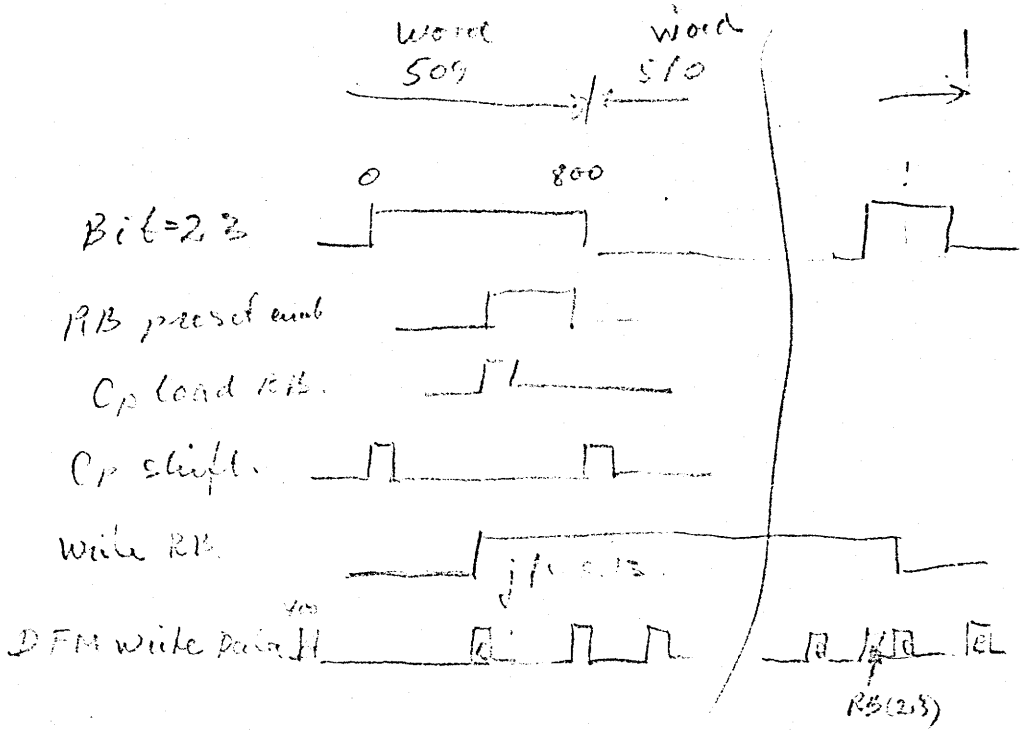


41 D1

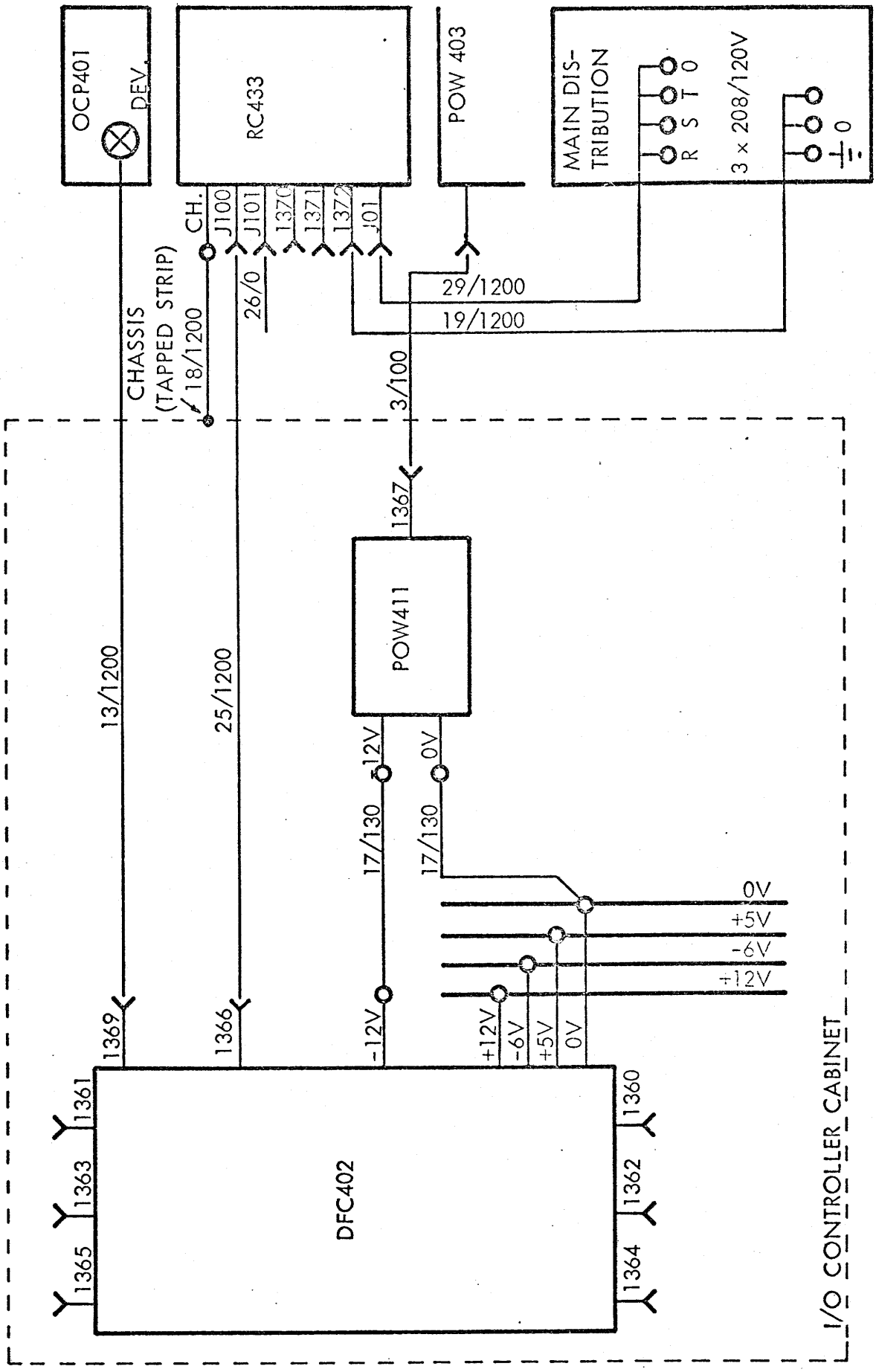
41 B1

41 C1


Cycle Call
Cycs Request
HDC Cycle Addr.
HDC Cycle Data
397
HDC Busy


word 509
word 510
0
800
Bit=23
RB preset numb
Cp load RB.
Cp shift.
Write RB
DFM write Data
RB(23)

PEH



RCSL: 51-VB851

INTERCONNECTION PLAN FOR RC4318 AND RC433
RC4000 INSTALLATION: _____

Dwg. No.
_____

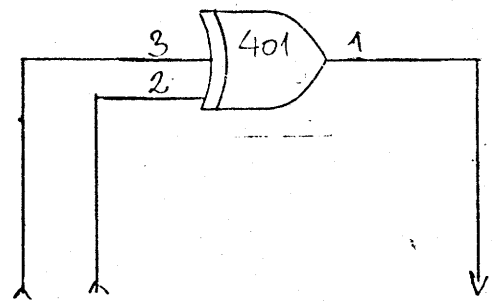
DFC 402

PCBA Position List

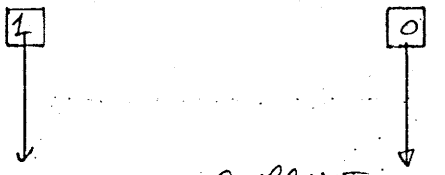
Position	PCBA
DFC 001	RC0933-1
DFC 002	RC0933-1
DFC 003	RC0897-1
DFC 004	RC0936-1
DFC 005	RC0936-1
DFC 006	RC0890-1
DFC 007	RC0847-1
DFC 008	RC0834-1
DFC 009	RC0847-1
DFC 010	RC0884-1
DFC 011	RC0836-1
DFC 012	RC3032-1
DFC 013	RC0935-1
DFC 014	RC0935-1
DFC 015	RC0935-1
DFC 016	RC0935-1
DFC 017	RC0934-1
DFC 018	RC0934-1
DFC 019	RC0834-2
DFC 020	RC0858-1
DFC 021	RC0839-1
DFC 022	RC0834-1
DFC 023	RC0838-1
DFC 024	RC0847-1
DFC 025	RC0934-1
DFC 026	RC0934-1
DFC 027	RC0898-1
DFC 028	RC0898-1
DFC 029	RC0898-1
DFC 030	RC0934-1
DFC 031	RC0934-1
DFC 032	RC0934-1

DFC 402

Position	PCBA
DFC 033	RC0934-1
DFC 034	RC0897-1
DFC 035	RC0897-1
DFC 036	RC0897-1
DFC 037	RC0897-1
DFC 038	RC0901-1
DFC 039	RC0935-1
DFC 040	RC0935-1
DFC 041	RC0935-1
DFC 042	RC0935-1
DFC 043	RC0839-1
DFC 044	RC3032-1
DFC 045	RC0834-1
DFC 046	RC0839-1
DFC 047	RC3032-1
DFC 048	RC0834-1
DFC 049	RC0839-1
DFC 050	RC3032-1
DFC 051	RC0834-1
DFC 052	RC0834-1
DFC 062	RC0903-2/1
DFC 063	RC0897-1
DFC 064	RC0835-1
DFC 065	RC0903-1/5
DFC 066	RC0835-1
DFC 067	RC0834-1
DFC 068	RC0837-1
DFC 069	RC0839-1
DFC 070	RC0835-1
DFC 071	RC0838-1
DFC 072	RC0835-1
DFC 073	RC0894-1
DFC 074	RC0860-2
DFC 075	RC0893-3



CIRCUIT			
A	2	3	A 1
B	5	6	B 4
C	7	8	C 9
D	10	11	D 12
E	14	15	E 13
G	17	18	F 16
G	24	25	G 26
H	27	28	H 29
J	31	32	J 30
K	34	35	K 33
L	36	37	L 38
M	39	40	M 41



CIRCUIT
N 23

CIRCUIT
P 19
R 20

POWER REQUIREMENTS:

0V (Pin 21)

+5V (Pin 22) 150mA

Power dissipation 790 mW.

Unit: RCLM 400	Designed 17.10.69 FK	PCARD SPECIFICATION	Drawing No
A/S REGNE CENTRALEN	Approved	12 AM 401, RC 082 - 2	Drawn by
	Checked		Checked
	Last Revision		Sheets / Sheet

Form. 304-100. 8. 69

CIRCUIT TYPES SN5486, SN7486
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

- Input-Clamping Diodes Simplify System Design
- Fully Compatible with TTL, DTL, and Other MSI Circuits
- Typical Propagation Delay Times: 12 ns

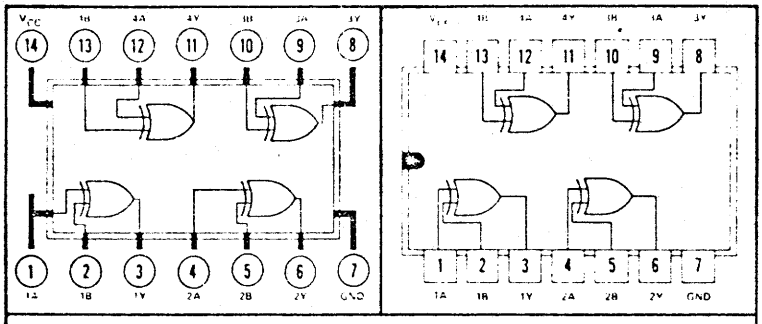
logic

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

S
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = A \oplus B$

description

Each of these monolithic, quadruple 2-input exclusive-OR gates utilize TTL circuitry to perform the function: $Y = A\bar{B} + \bar{A}B$. When the input states are complementary, the output goes to a logical 1.

These circuits are fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out of 20 is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Propagation delay is 12 nanoseconds and power dissipation is 37.5 milliwatts typically for each exclusive-OR function.

The SN5486 is characterized for operation over the full military temperature range of −55°C to 125°C and the SN7486 is characterized for operation from 0°C to 70°C.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Note 1)	5.5 V
Operating Case Temperature Range: SN5486S	−55°C to 125°C
Operating Free-Air Temperature Range: SN5486J, SN5486N	−55°C to 125°C
SN7486 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

CIRCUIT TYPES SN5495, SN7495
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

A TTL MSI PARALLEL-IN PARALLEL-OUT REGISTER

for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

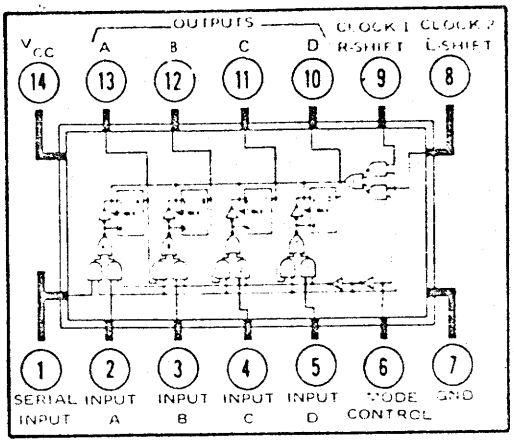
description

This monolithic shift register, utilizing transistor-transistor-logic (TTL) circuits in the familiar Series 54/74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, one AND-OR-INVERT gates, one AND-OR gate, and six inverter-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shifter or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

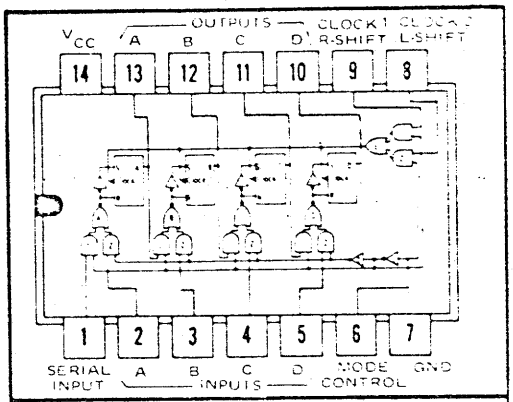
When a logical 0 level is applied to the mode control input, the number-1 AND gates are enabled and the number-2 AND gates are inhibited. In this mode the output of each flip-flop is coupled to the R-S inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number-2 AND gates.

When a logical 1 level is applied to the mode control input, the number-1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number-2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register, or with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (D_{out} to input C, and etc.), and serial data is entered at input D.

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

Mode control = 0 for right shift
Mode control = 1 for left shift or parallel load

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking. Transfer of information to the output pins occurs when the clock input goes from a logical 1 to a logical 0.

This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is typically 250 milliwatts.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Case Temperature Range: SN5495S Circuits . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN5495J, SN5495N Circuits . . . . . −55°C to 125°C
SN7495 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5495 Circuits	4.5	5	5.5	V
SN7495 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output			10	
Width of Clock Pulse $t_{p(clock)}$ (See Figure 9): SN5495 Circuits	20	10		ns
SN7495 Circuits	15	10		ns
Setup Time Required at Serial, A, B, C, or D Inputs t_{setup} (See Figure 9)	20	10		ns
Hold Time Required at Serial, A, B, C, or D Inputs t_{hold} (See Figure 9)	0	−10		ns
Logical 0 Level Setup Time Required at Mode Control (t1 in Figure 10) (With Respect to Clock 1 input)	20			ns
Logical 1 Level Setup Time Required at Mode Control (t2 in Figure 10) (With Respect to Clock 2 input)	20			ns
Logical 0 Level Setup Time Required at Mode Control (t3 in Figure 10) (With Respect to Clock 2 input)	10			ns
Logical 1 Level Setup Time Required at Mode Control (t4 in Figure 10) (With Respect to Clock 1 input)	10			ns

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 3	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2 and 4	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 and 3	V_{CC} = MIN,	I_{load} = −400 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	2 and 4	V_{CC} = MIN,	I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at any input except mode control	5	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at mode control	5	V_{CC} = MAX,	V_{in} = 0.4 V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except mode control	6	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at mode control	6	V_{CC} = MAX,	V_{in} = 2.4 V			80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current§	7	V_{CC} = MAX		−18		−57	mA
I_{CC}	Supply current	8	V_{CC} = MAX	SN5495		50	72	mA
				SN7495		50	82	mA

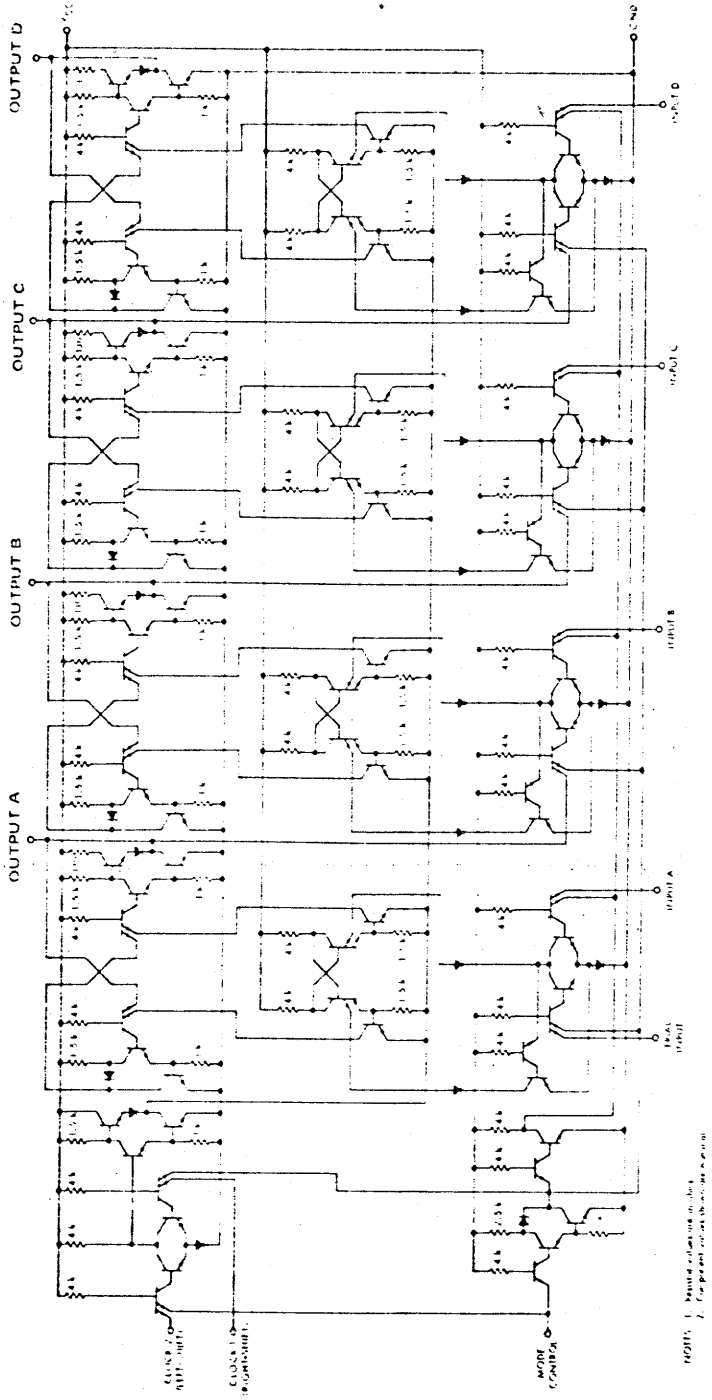
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS*		MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	9	C_L = 15 pF,	R_L = 400 Ω	20	31		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF,	R_L = 400 Ω		26	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF,	R_L = 400 Ω		24	35	ns

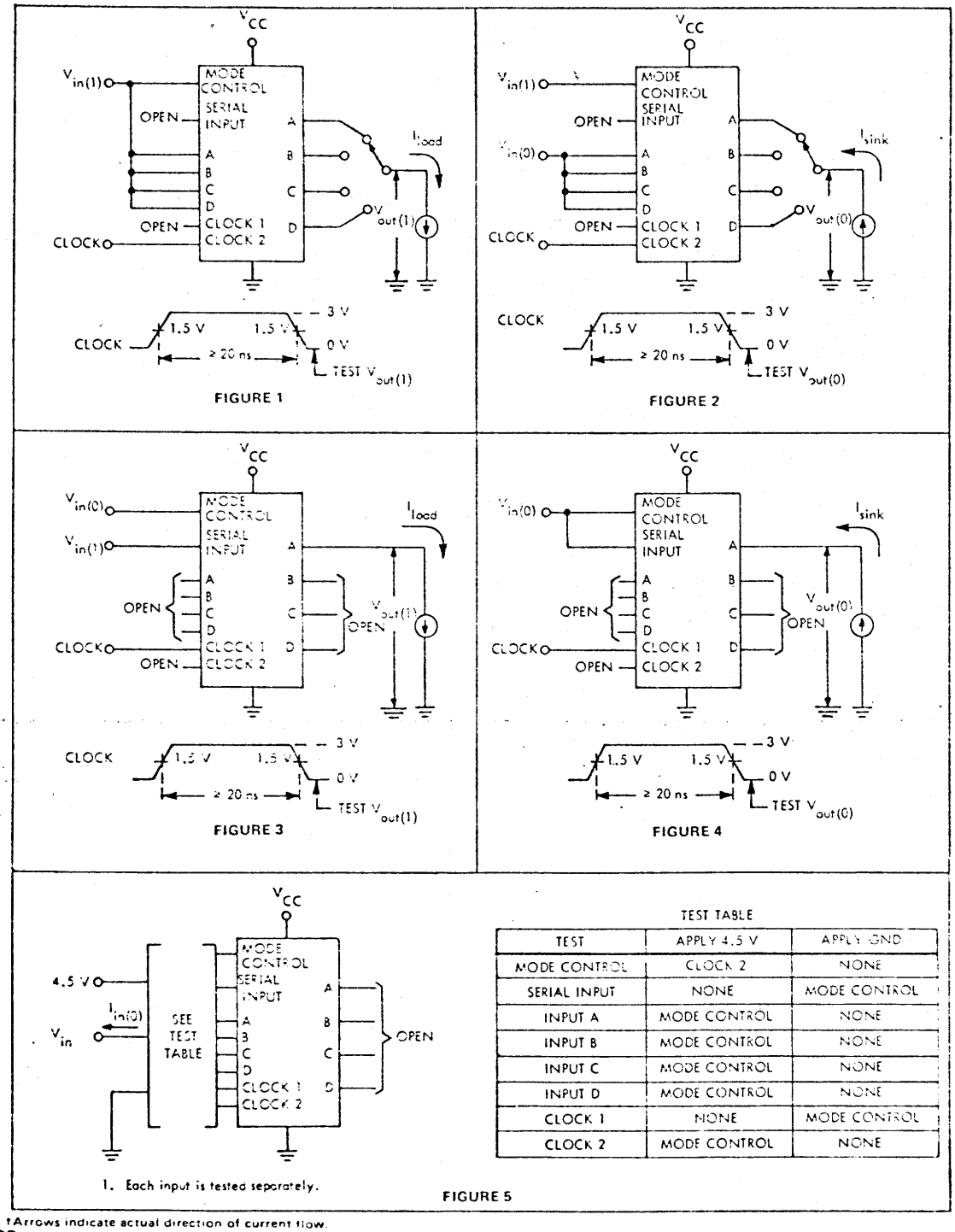
– SEE ORDERING INSTRUCTIONS PAGE 1-1 –

schematic



PARAMETER MEASUREMENT INFORMATION

* d-c test circuits†



TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	CLOCK 2	NONE
SERIAL INPUT	NONE	MODE CONTROL
INPUT A	MODE CONTROL	NONE
INPUT B	MODE CONTROL	NONE
INPUT C	MODE CONTROL	NONE
INPUT D	MODE CONTROL	NONE
CLOCK 1	NONE	MODE CONTROL
CLOCK 2	MODE CONTROL	NONE

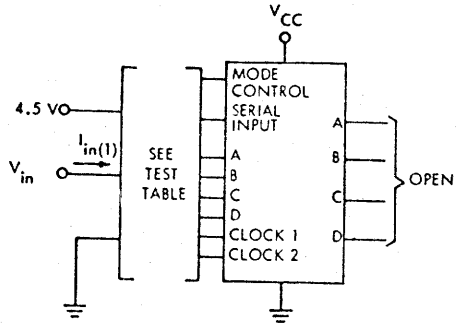
1. Each input is tested separately.

FIGURE 5

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

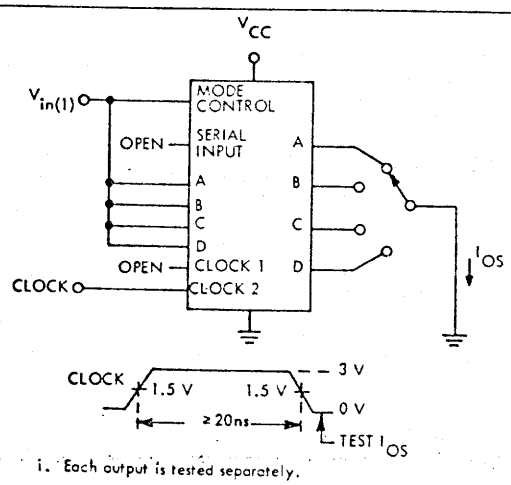
d-c test circuits† (continued)



TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	NONE	CLOCK 2
SERIAL INPUT	MODE CONTROL	NONE
INPUT A	NONE	MODE CONTROL
INPUT B	NONE	MODE CONTROL
INPUT C	NONE	MODE CONTROL
INPUT D	NONE	MODE CONTROL
CLOCK 1	MODE CONTROL	NONE
CLOCK 2	NONE	MODE CONTROL

FIGURE 6



1. Each output is tested separately.

FIGURE 7

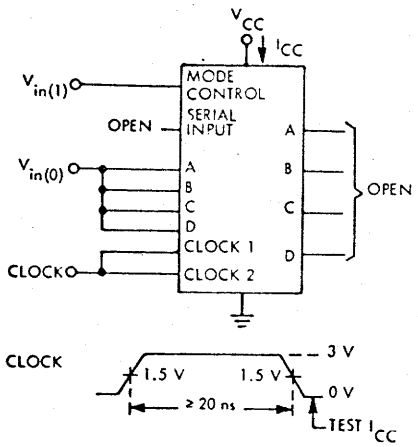
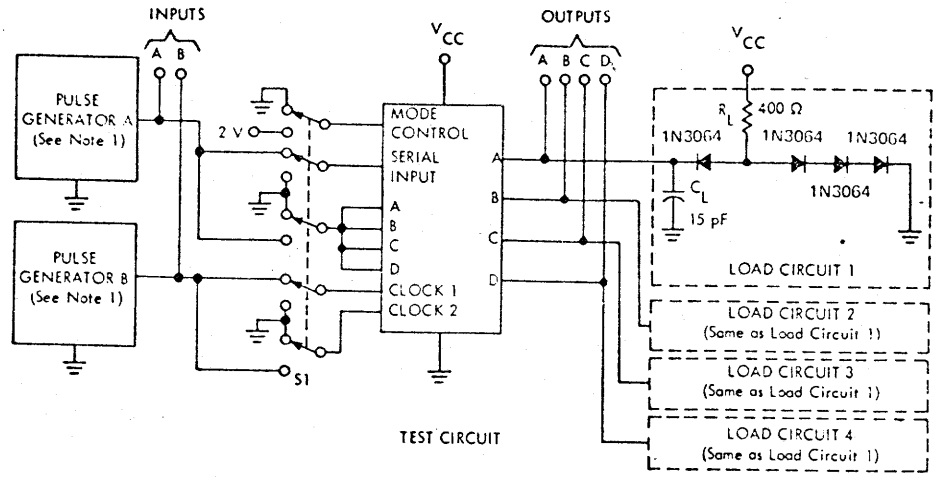


FIGURE 8

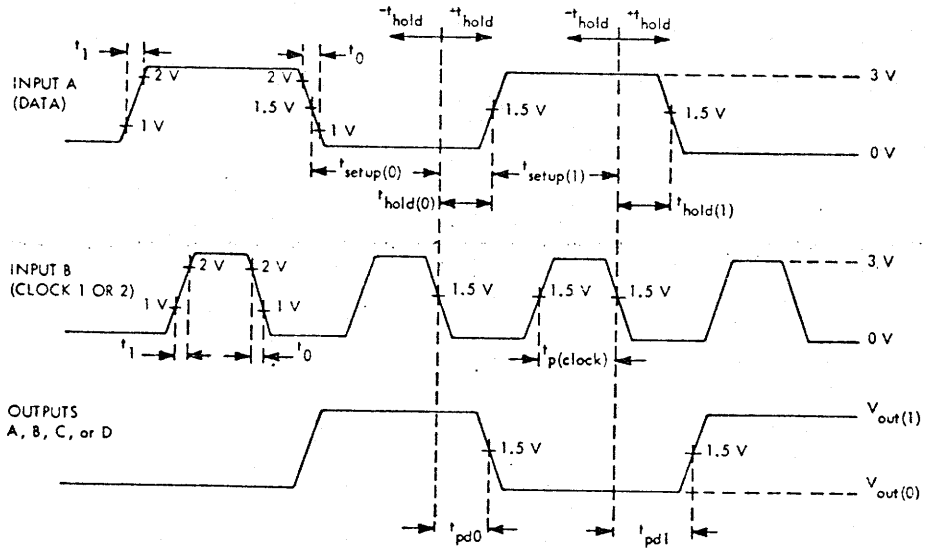
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching charateristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

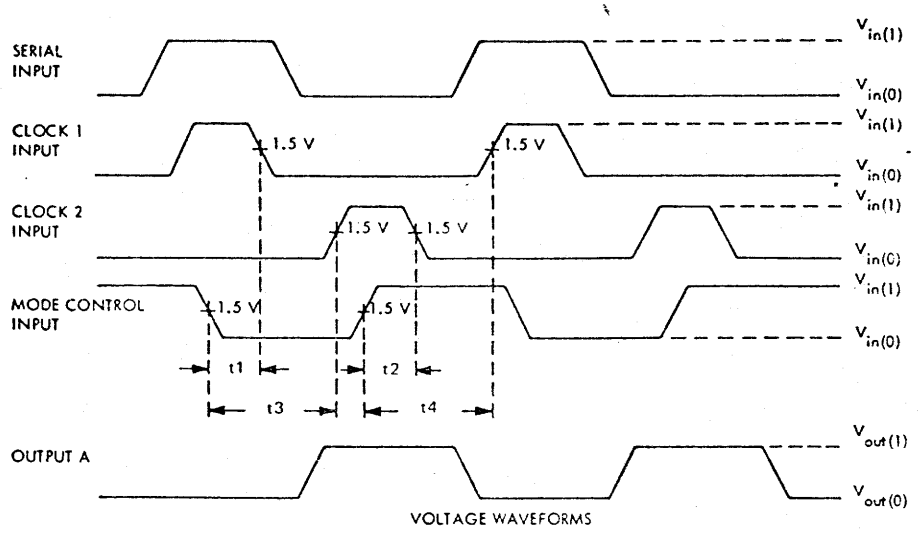
NOTES: 1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 + t_0 \geq$ 10 ns, and $Z_{out} \approx$ 50 Ω. For pulse generator A: $t_p \leq$ 20 ns and PRR = 500 kHz. For pulse generator B: $t_p \geq$ 15 ns and PRR = 1 MHz. When testing f_{max} vary PRR.

2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.

FIGURE 9–SWITCHING TIMES

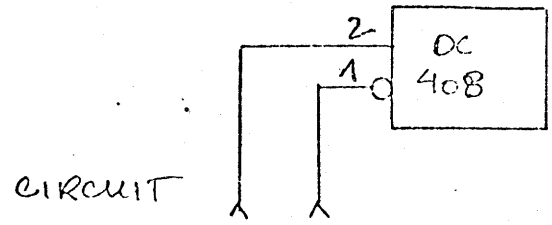
PARAMETER MEASUREMENT INFORMATION

recommended mode control setup times



NOTE: Input A is at $V_{in(0)}$.

FIGURE 10–MODE CONTROL SETUP TIMES



CIRCUIT		
A	11	12
B	14	13
C	16	15
D	18	17
E	20	19
F	9	10
G	7	8
H	5	6
J	2	3
K	33	32
L	30	31
M	28	29
N	26	27
P	24	25
R	35	34
S	37	36
T	39	38
U	41	40

POWER REQUIREMENTS

0 V (Pin 21)

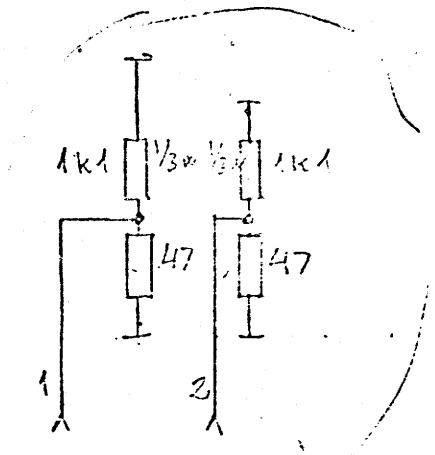
+12V (Pin 1) 180 mA

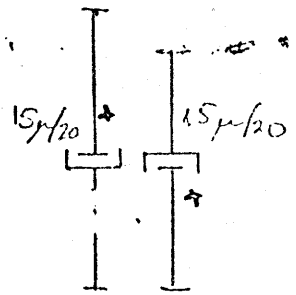
-12V (Pin 4) 180 mA

Power dissipation 5300 mW

Unit: RCLH-100	Designed [illegible]	CARD SPECIFICATION	Drawing No
A/S REGNECENTRALEN	Approved	18 DC 408	Drawn by
	Checked		Checked
	Last Revision		Sheets / Sheet

Form. 304-100. 6. 69





CIRCUIT

12	A	11
13	B	14
15	C	16
17	D	18
19	E	20
10	F	9
8	G	7
6	H	5
4	J	2
32	K	33
31	L	30
29	M	28
27	N	26
25	P	24
34	R	35
36	S	37
38	T	39
40	U	41

Unit:	Designed	CIRCUIT DIAGRAM 12 DC 408	Drawing No
A/S REGNE CENTRALEN	Approved		Drawn by
	Checked		Checked
	Last Revision		Sheets / Sheet

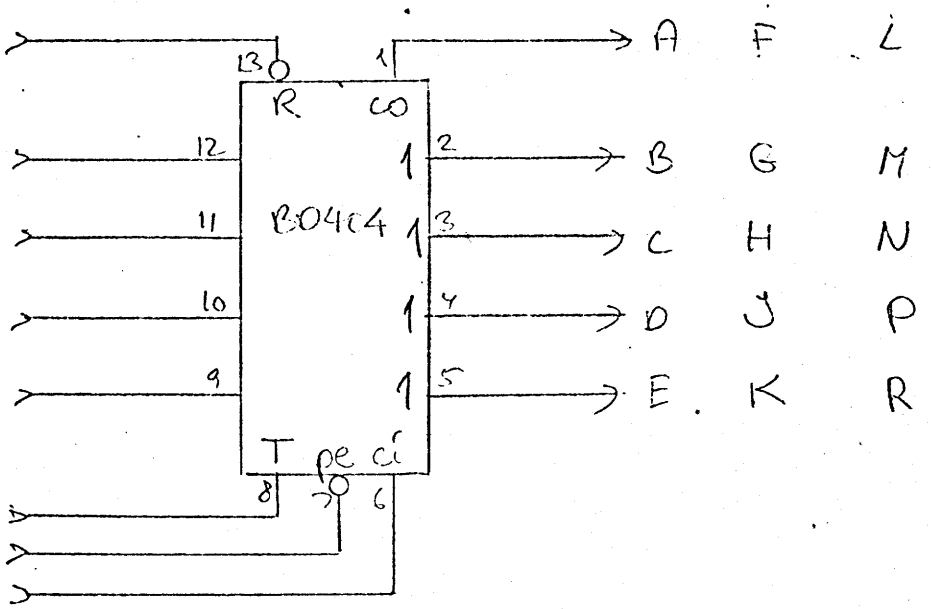
Form. 304-100. 6. 69

CIRCUIT

A B C

CIRCUIT

A' B C



POWER REQUIREMENTS

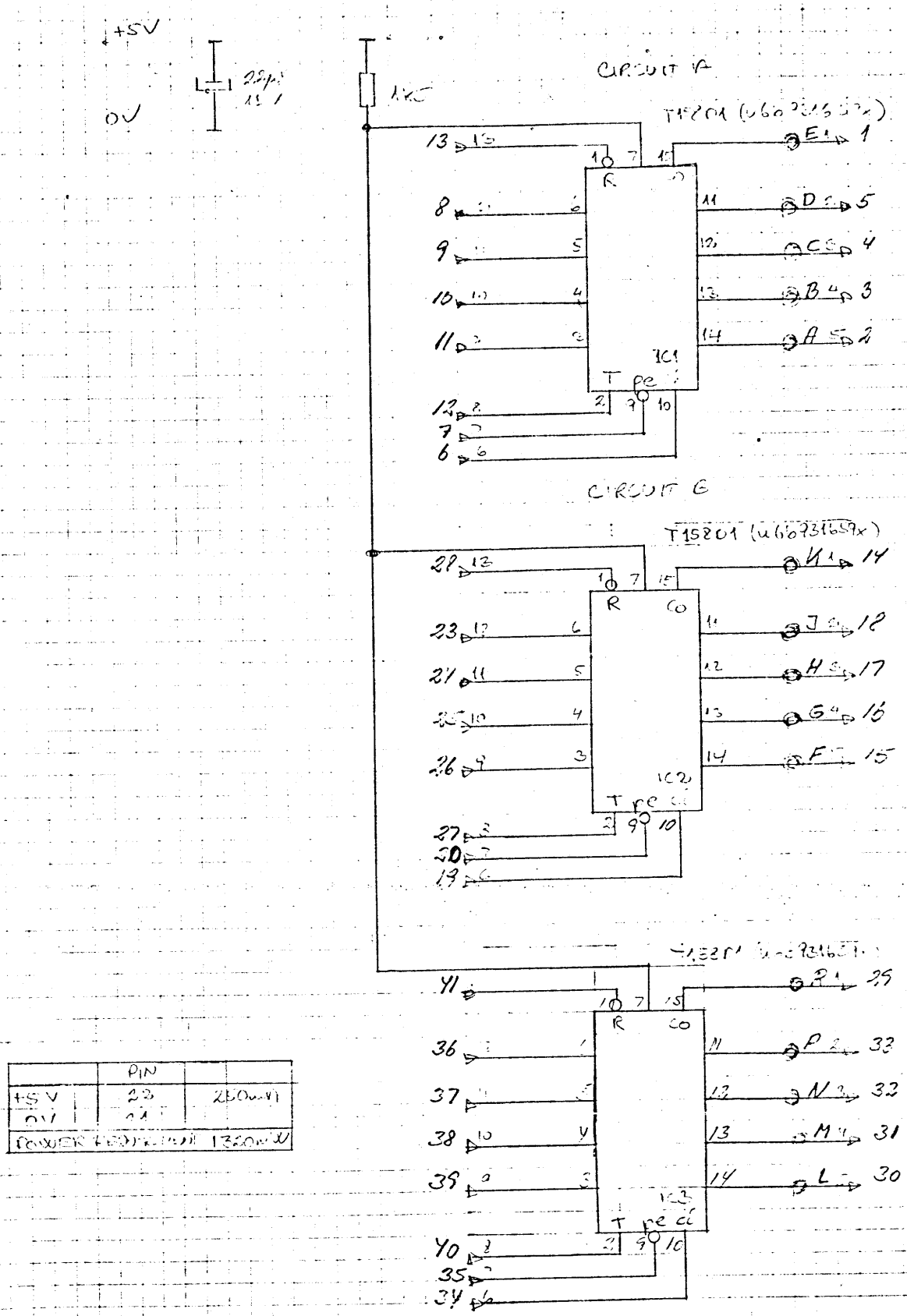
0V (Pin 21)

+5V (Pin 22) 250mA

Power dissipation 1250mW

Unit:	Designed 20/11 69 PEA	CARD SPECIFICATION	Drawing No
A/S REGNE CENTRALEN	Approved	3BO4C4 RC0935-1	Drawn by
	Checked		Checked
	Last Revision		Sheets / Sheet

Form. 304-100. 8. 69



	PIN	
+5 V	22	250mA
0 V	11	
POWER DISSIPATION		1320mW

Designed by	21.11.82 FBK
Drawn by	
Dwg. Office Check	
Design Check	
Replaces Dwg. No.	
due to ECN	
Replaced by Dwg. No.	

A/S REGNECENTRALEN

RC doc. V8 140

Unit	RCLM 4000
Dwg. No.	3BC404

PC BA Circuit Diagram

RC093

93

MSI 4-BIT BINARY COUNT

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODU

GENERAL DESCRIPTION — The 9316 is a high speed synchronous 4-bit binary decade counter. It is a synchronously presetable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Several stages of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

FEATURES:

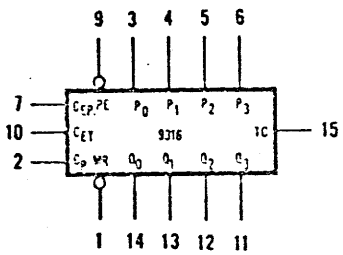
- SYNCHRONOUS COUNTING AND PARALLEL ENTRY
- DECODED TERMINAL COUNT
- BUILT-IN CARRY CIRCUITRY
- TYPICAL POWER DISSIPATION OF 300 mW
- THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, AND TTμL FAMILIES (CCSL).
- ALL CERAMIC HERMETIC 16 PIN DUAL IN-LINE PACKAGE AND FLAT PACKAGE
- INPUT DIODE CLAMPING

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION — Specify U6S9316XXX for 16-pin Dual In-Line Package, U3L9316XXX for 16-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to 75°C temperature range.

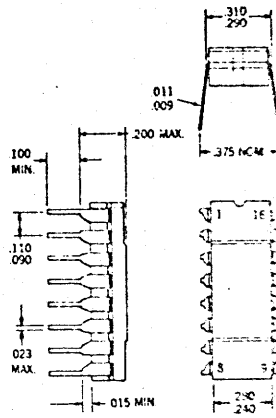
LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

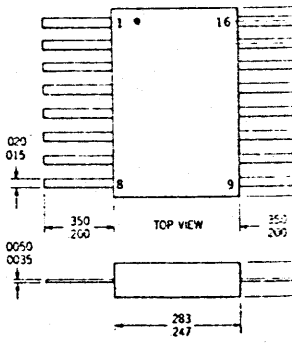
PHYSICAL DIMENSIO

DUAL IN-LINE PACKAG



NOTE:
1. Leads are intended for insertion in hole rows ... 300" centers. They are purposely shipped ... "positive" (.375) misalignment to facilitate ...

FLAT PACKAGE



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

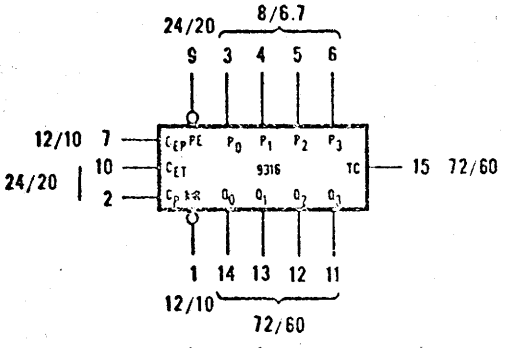
FAIRCHI
SEMICONDUC
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT

FUNCTIONAL DESCRIPTION — A clock buffer and inverter drives the four clocked RS master-slave flip flops in parallel, so that synchronous operation is obtained. When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low to high transition of CP, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now stored information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady as long as the clock input remains high, and regardless of the logic state at any other input to the device. During the high to low transition of the clock input, first the transfer path from master to slave are inhibited, leaving the slave steady in its present state, secondly, the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Some restrictions are placed on the manner of selection. First, the transition of CEP or CET from high to low or of PE from low to high may only be done when CP is high. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics." The asynchronous MR clears the counter independent of any other input.

Note: CE (count enable) = CEP • CET
TC = CET • Q_0 • Q_1 • Q_2 • Q_3

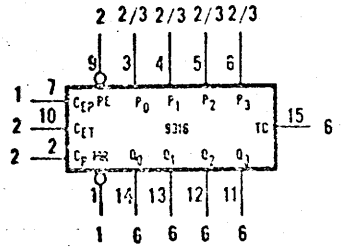
LOADING RULES

CCSL LOAD AND DRIVE FACTORS



Vcc = Pin 16
Gnd = Pin 8

TTμL LOAD AND DRIVE FACTORS



Vcc = Pin 16
Gnd = Pin 8

(1 U.L. = 1 TTμL input gate load)

ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 9.6 mA V_{CC} = 4.5 V, I_{OL} = 7.44 mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current MR, CEP		−1.6		−1.0	−1.6		−1.6	mA	
$2I_F$	Input Load Current CP, PE, CET		−3.2		−2.0	−3.2		−3.2	mA	V_{CC} = 5.5 V V_F = 0.4 V
$\frac{1}{2}I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current MR, CEP		60		10	60		60	μA	
$2I_R$	Input Leakage Current CP, PE, CET		120		20	120		120	μA	V_{CC} = 5.5 V V_R = 4.5 V
$\frac{1}{2}I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+75°C MIN.	MAX.	UNITS	CONDITIONS & COMM
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.36 m
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 9.6 mA V_{CC} = 4.75 V, I_{OL} = 8.5 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current MR, CEP		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE, CET		−3.2		−2.0	−3.2		−3.2	mA	V_{CC} = 5.25 V V_F = 0.4 V
$^2/_3 I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current MR, CEP		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE, CET		120		20	120		120	μA	V_{CC} = 5.25 V V_R = 4.5 V
$^2/_3 I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMEN
t_{pd+} (Q)	Turn-Off Delay		20		ns	V_{CC} = 5.0 V C_L = 15 pF (Fig. 1)
t_{pd-} (Q)	Turn-On Delay		15		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		35		ns	
t_{pd-} (TC)	Turn-On Delay for TC		20		ns	
t_s (SE)	Set-Up Time for CE		14		ns	V_{CC} = 5.0 V C_L = 15 pF (Fig.2)
t_r (CE)	Release Time for CE		12		ns	
t_s	Set-Up Time for Data		13		ns	V_{CC} = 5.0 V C_L = 15 pF (Fig. 3)
t_r	Release Time for Data		17		ns	
t_s (PE)	Set-Up Time for PE		30		ns	
t_r (PE)	Release Time for PE		28		ns	
t_{pd-} (MR)	Turn-On Delay for MR		33		ns	V_{CC} = 5.0 V, C_L = 15 pF (F
$t_{P\pm}$	Propagation Delay for CET to TC		14		ns	V_{CC} = 5.0 V, C_L = 15 pF (F

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from to high in order for the flip-flop(s) not to respond.

SWITCHING TIME WAVEFORMS

Fig. 1

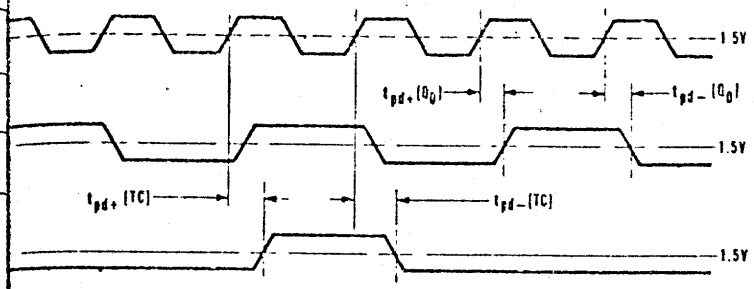


Fig. 2

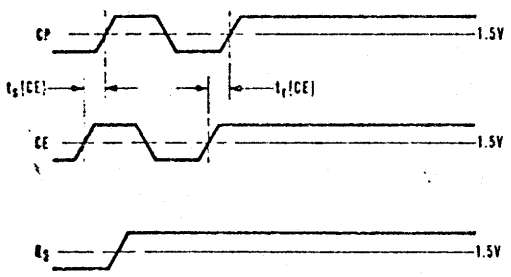


Fig. 3

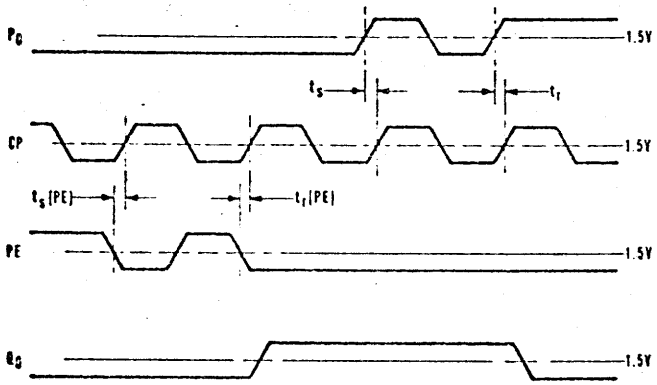


Fig. 4

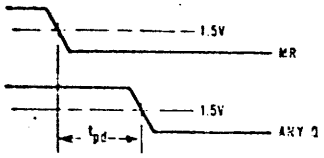
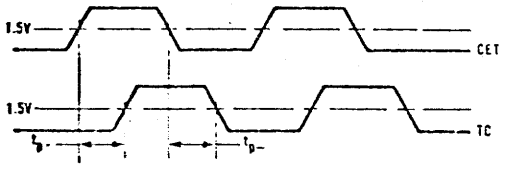
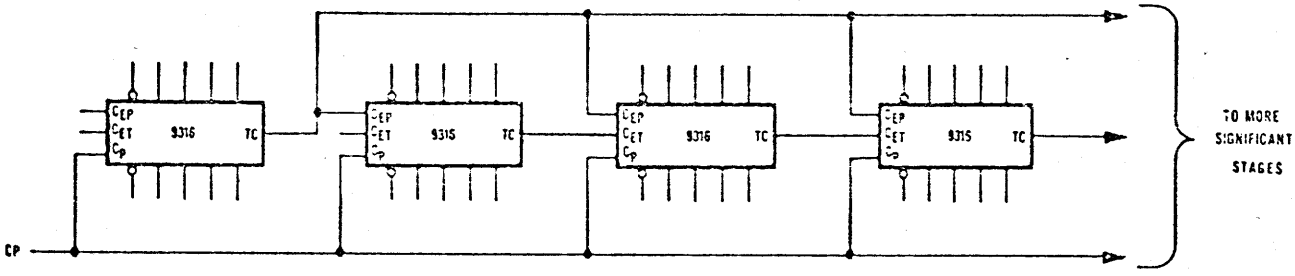


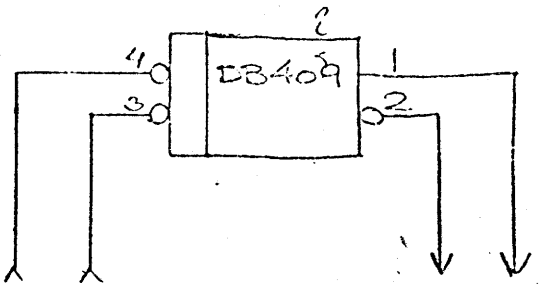
Fig. 5



APPLICATIONS



SYNCHRONOUS COUNTING SCHEME



CIRCUIT				
A	2	3	11	A12
B	5	6	13	B14
C	8	7	15	C16
D	10	9	24	D25
E	28	29	26	E27
F	31	30	36	F37
G	33	32	38	G39
H	34	35	40	H41

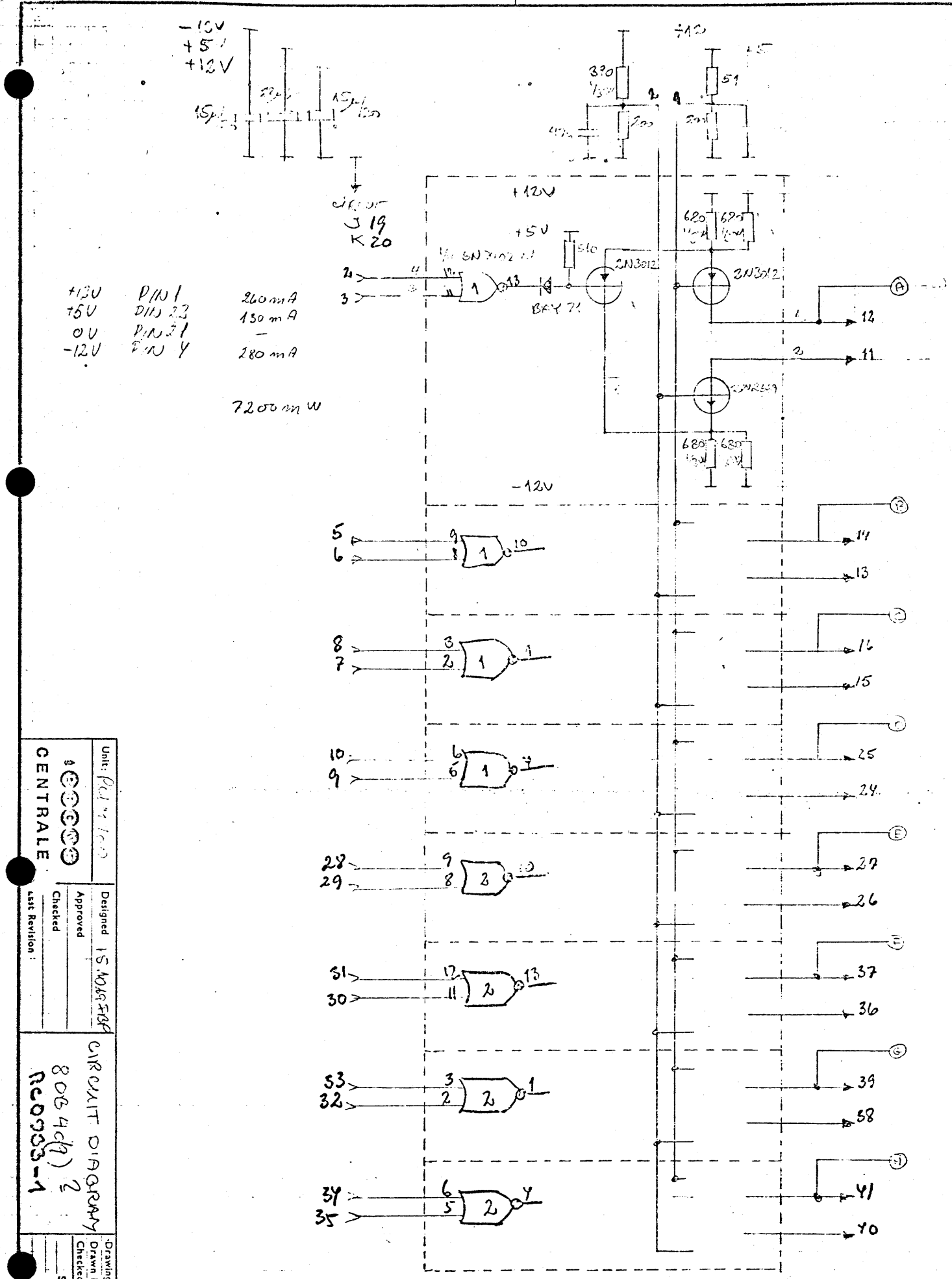
CIRCUIT	
J	19
K	20

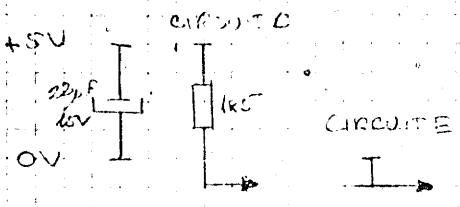
POWER REQUIREMENTS:

0V	(Pin 21)	
+5V	(Pin 22)	130 mA
+12V	(Pin 1)	260 mA
-12V	(Pin 4)	280 mA
Power dissipation		7200 mW

Unit: [illegible]	Designed [illegible]	CARD SPECIFICATION	Drawing No	
A/S REGNECENTRALEN	Approved	8DB409	Drawn by	
	Checked	0933-1	Checked	
	Last Revision		Sheets / Sheet	

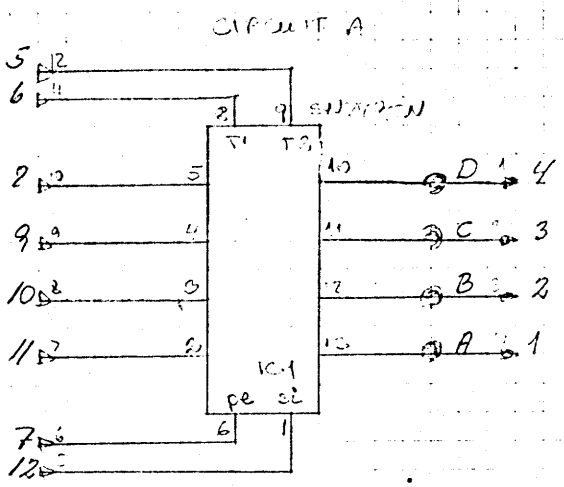
m. 304-100. 8. 69

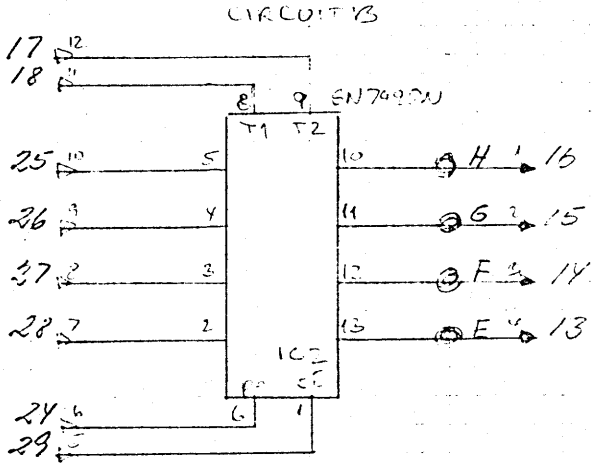

-12V
+5V
+12V
+12V
+5V
+12V
330
51
510
2N3012
2N3012
BAY 71
620
620
680
680
+12V
+5V
-12V
P/N 1
P/N 23
P/N 21
P/N 4
260 mA
130 mA
280 mA
7200 mW
CIRCUIT DIAGRAM
8064(9) 2
RC0933-1
CENTRALE
Designed
Approved
Checked
Last Revision
Drawing No
Drawn by
Checked
Sheets
Sheet

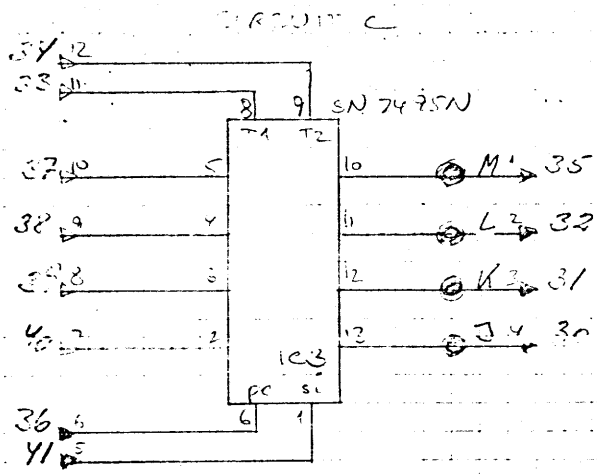


CIRCUIT C

CIRCUIT E







	PIN	
+5V	22	220 mA
0V	21	
POWER REQUIREMENTS 14mW		

Designed by 21/1/69 RBP	Drawn by	Dwg. Office Check
Design Check	Replaces Dwg. No.	due to ECN
		Replaced by Dwg. No.

A/S REGNECENTRALEN

Unit RC 4000	3 BF 403	RC 8934
Dwg. No.	RCBX Circuit Diagram	

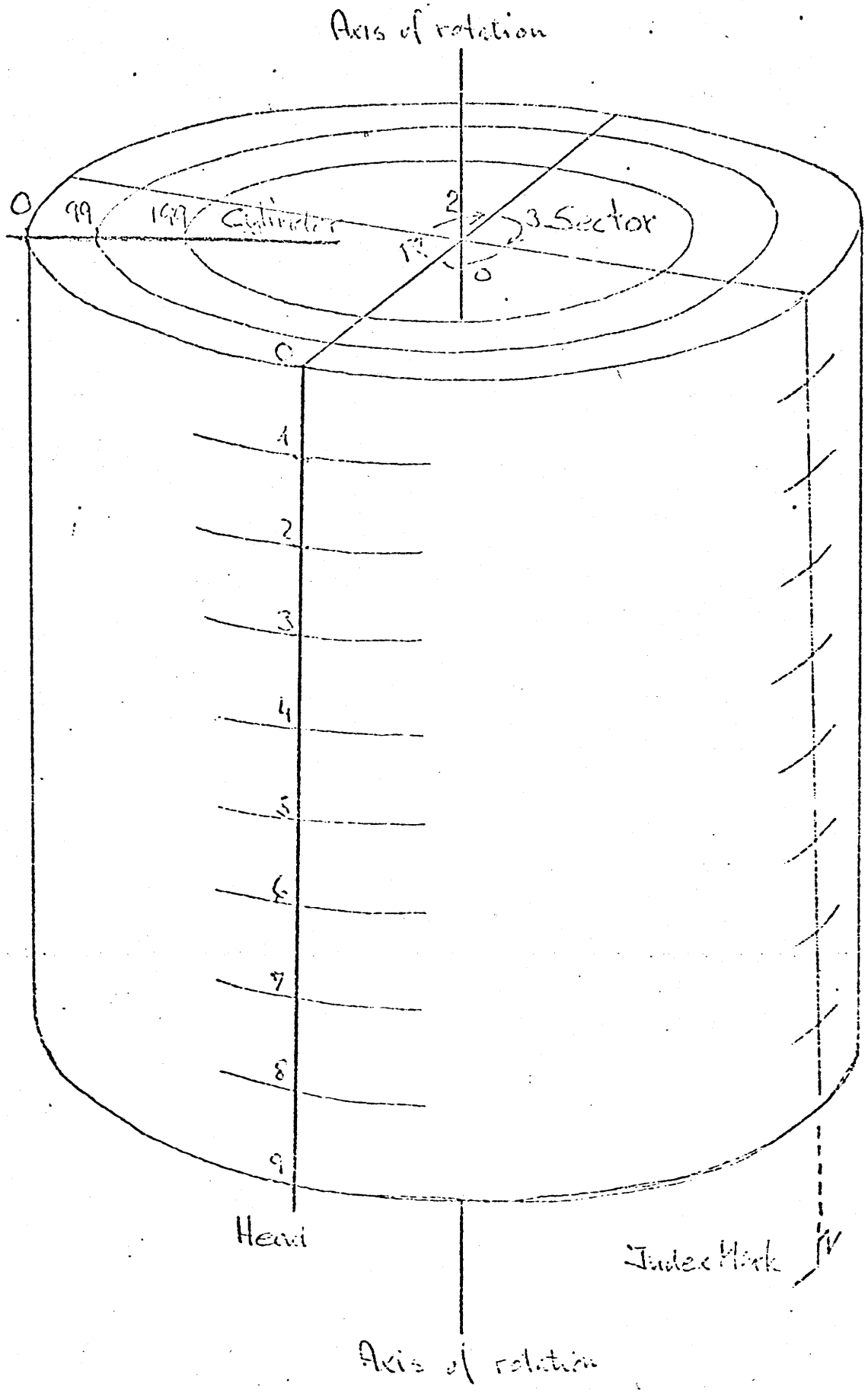


Figure ____ location of Cylinders, Heads, and Sectors on a Disc Kit.

The Disc Segment Number is 40 x Cylinder + 4 x Head + Sect

DFC 402 8/1-70
[ADEFORDELING

ANTAL PLADER = 66
ANTAL KABELSTIK = 8
ANTAL RESERVEREDE POSITIONER = 0

TYPE	ANTAL	RC-NR.	KREDSLØB
1	7	834-1	12AC401
2	5	839-1	7AC402
3	2	838-1	4AC403
5	1	860-2	4DD402
14	1	884-1	9BA403/1AA405
16	4	835-1	6BC401
17	3	847-1	7AG401
23	1	8016-38	38 POL ELCO
24	7	8016-90	90 POL ELCO
26	1	837-1	3BB401
35	1	836-1	5AC404
7	1	890-1	11DB402/1DB403
41	1	894-1	4DB404/1DB405
43	1	858-1	1AG402
50	1	893-2	1FF402
55	3	898-1	1DB406
56	6	897-1	10DC405
58	1	901-1	1AJ408
60	1	903-1/	1AJ407/1BG407/1CC406
69	1	909-1/	6CB402
72	2	933-1	8DB409
73	8	934-1	3BF403
74	8	935-1	3BD404
75	2	936-1	18DC408
76	1	834-2	12AM401
77	4	3032-1	12AD401

DFC 402 8/1-70

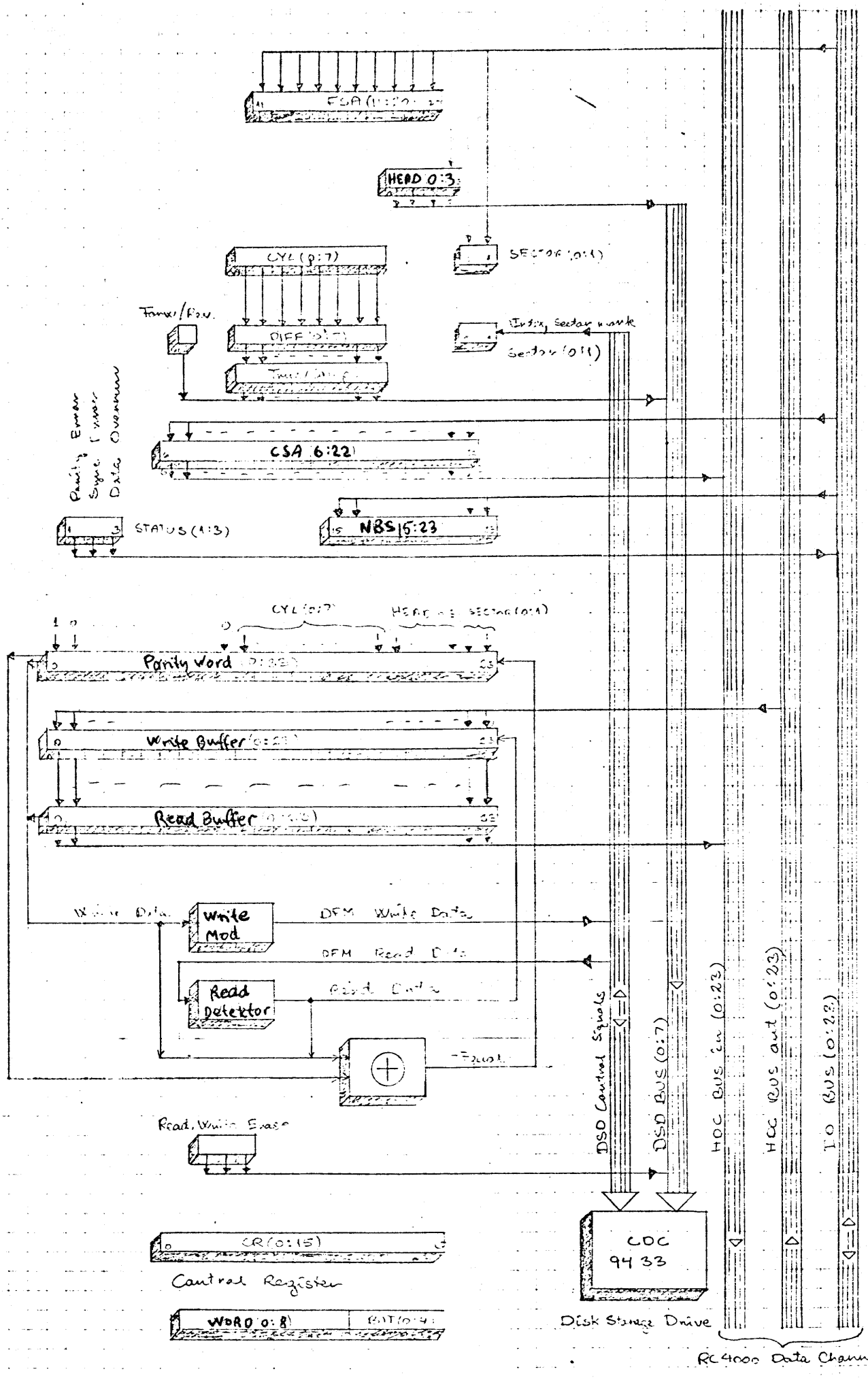
UBLE POSITION LIST

FORMAT = 3 × 26

IND	AKT	TYP	SYM	TYP
1	64	16	49	72
2	66	16	50	72
3	62	60	70	56
4	65	69	52	75
5	67	1	53	75
6	21	2	36	37
7	44	77	23	17
8	10	14	22	1
9	9	17	9	17
10	16	74	8	14
11	15	74	57	35
12	45	1	18	77
13	75	50	19	74
14	74	5	17	74
15	23	3	11	74
16	22	1	10	74
17	14	74	31	73
18	12	77	30	73
19	13	74	21	76
20	41	74	51	43
21	19	76	6	2
22	8	1	16	1
23	7	17	15	3
24	42	74	46	17
25	40	74	44	73
26	39	74	45	73
27	70	16	76	55
28	50	77	77	55
29	68	26	78	55
30	18	73	35	73
31	17	73	34	73
32	33	73	33	73
33	32	73	32	73
34	31	73	71	56
35	30	73	72	56
36	6	37	73	56
37	46	2	74	56
38	48	1	55	58
39	47	77	26	74
40	69	2	25	74
41	72	16	20	74
42	49	2	24	74
43	51	1	56	2
44	25	73	7	77
45	26	73	12	1
46	24	17	37	2
47	71	3	39	77
48	52	1	38	1
49	1	72	42	2
50	2	72	28	77
51	20	43	43	1
52	4	75	48	1
53	5	75		
54	73	41		

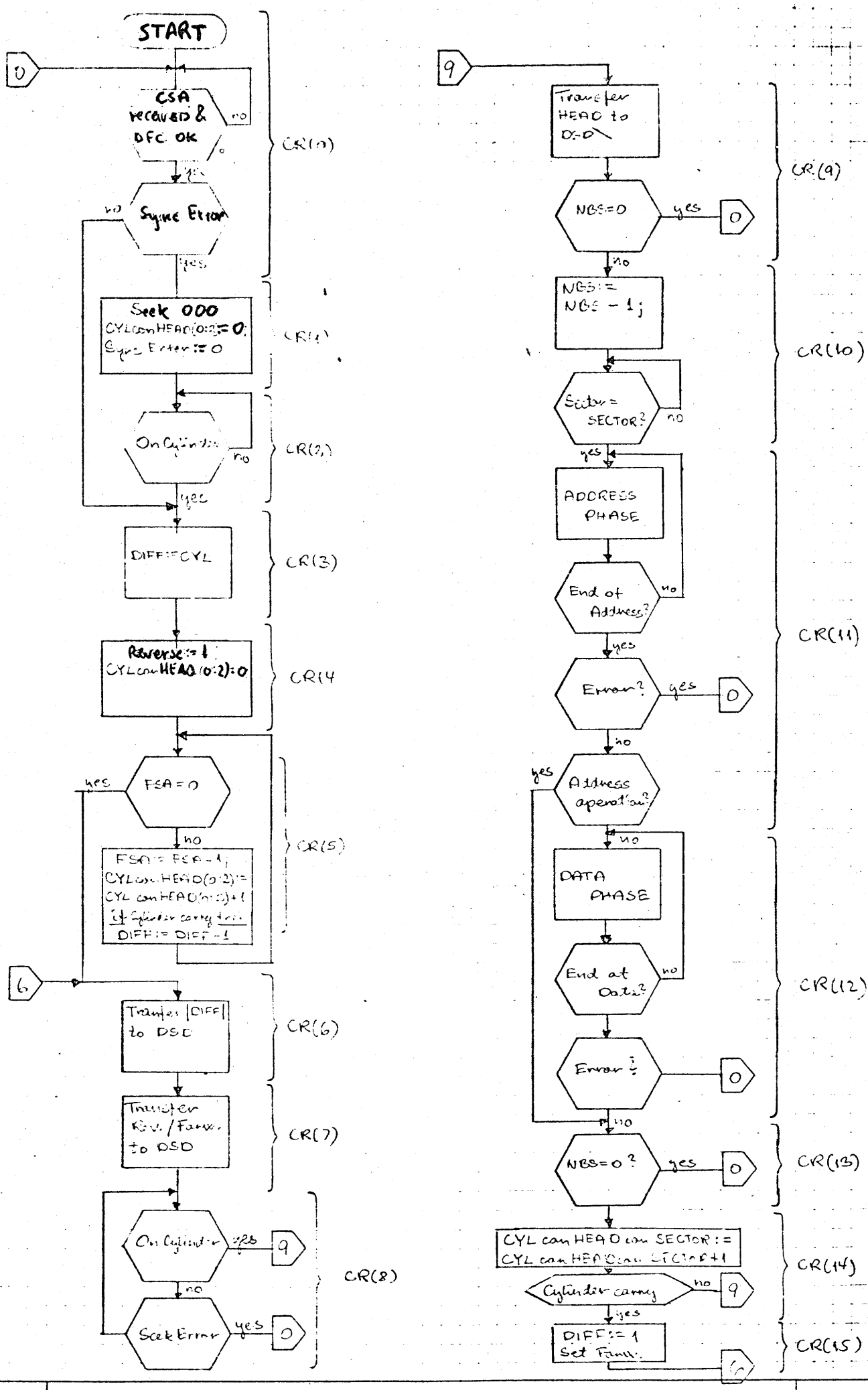
	55	38	58		
	56	43	2		
	57	11	35		
	62			3	60
	63			75	56
	64			1	16
	65			4	69
	66			2	16
	67			5	1
	68			29	26
	69			40	2
	70	3	56	27	16
	71	34	56	47	3
	72	35	56	41	16
	73	36	56	54	41
	74	37	56	14	5
	75	63	56	13	50
	76	27	55		
	77	28	55		
	78	29	55		

KABP	X	Y	TYPE
1360	37	393	24
1361	37	-30	24
1362	195	395	24
1363	195	-30	24
1364	350	395	24
1365	350	-30	24
1366	-60	55	24
1369	-60	105	23



Replaces Dwg. No.	due to ECN	Design Check	Dwg. Office C...	Drawn by	Designed by	A/S REGNECENTRALEN	Unit	OEC 403			
					04.09.70 FEG		Dwg. No.	DISK STRUCTURE			

RC 855 VR 140



Designed by	040270 FGP	
Drawn by		
Dwg. Of		
Design Check		
Replaces Dwg. No.		
due to ECN		
by Dwg. No.		

TRALEN

A/S REC

RC doc V8 140

Unit

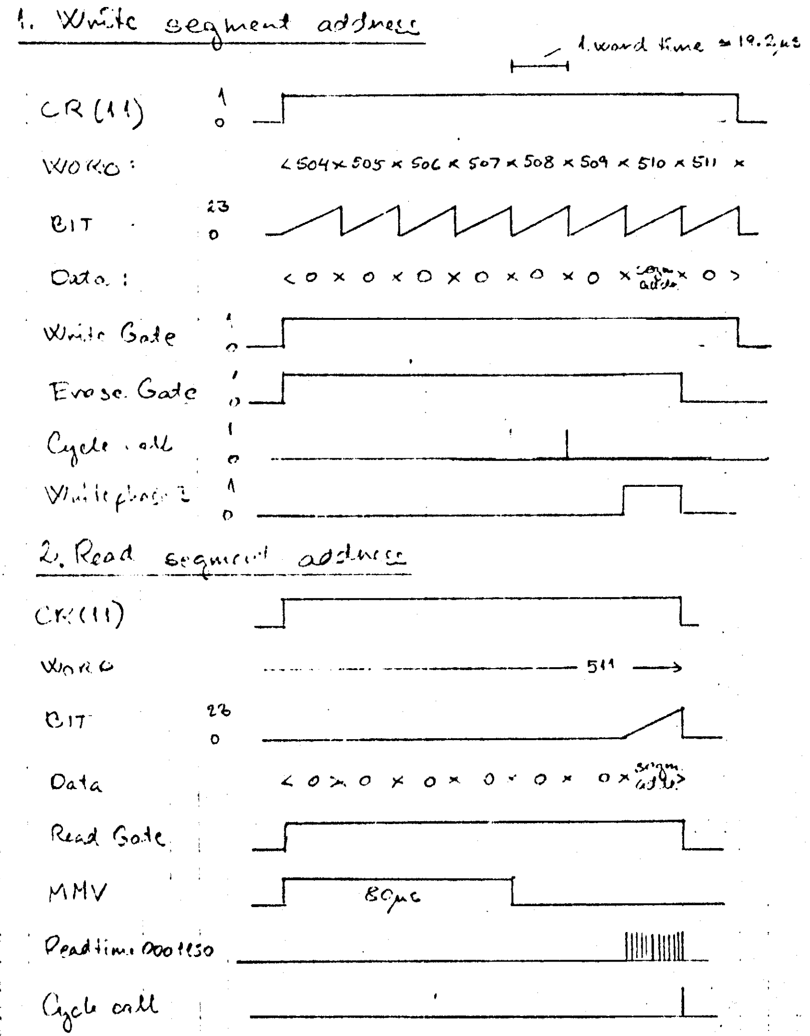
Dwg. No.

DFC 402
FLOW DIAGRAM

RC doc VB 140

A/S REGNECENTRALEN

Designed by	Drawn by	Dwg. Office		Design Check	Replaces Dwg. No.	due to ECN	Rep.	Dwg. No.
040?70 FRF								



Segment address format:

1 0 0 0 0 0 0 0 0 0 < cyl. address × head × sect.>

Unit

Dwg. No.

WRITE SEGMENT ADDRESS, READ SEGMENT ADDRESS
TIMING DIAGRAM

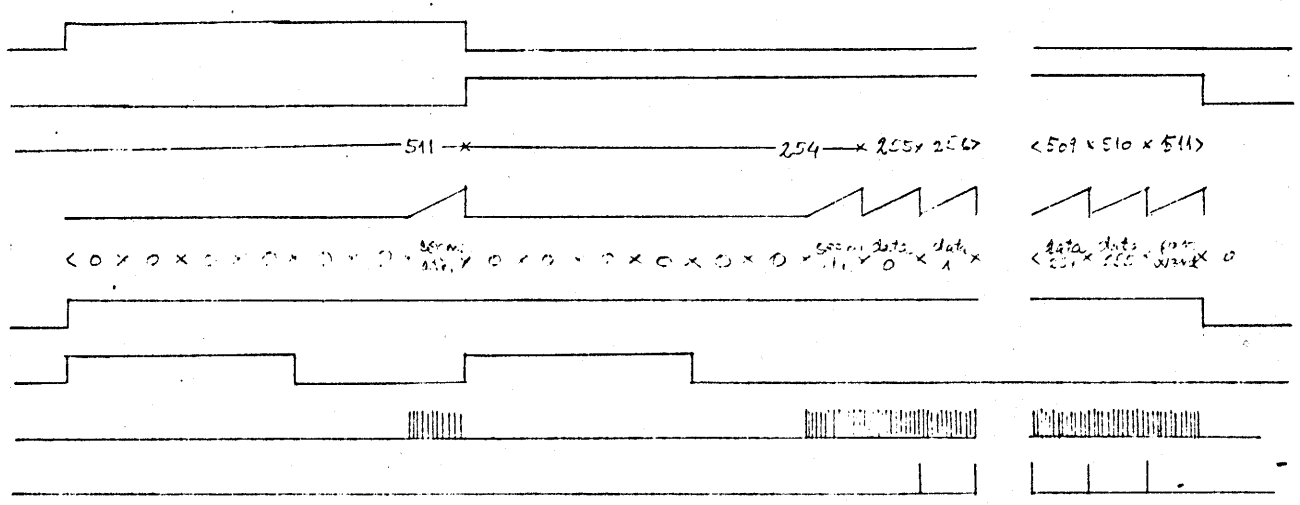
RC doc VB 140

A/S REGNE..NTRALEN	Designed by 040270 FBF	Drawn by	Dwg. Office C	Design Check	Replaces Dwg. No.	due to ECN	Repla..by Dwg. No.

Dwg. No. | Unit

READ DATA TIMING DIAGRAM

4. Read Data.



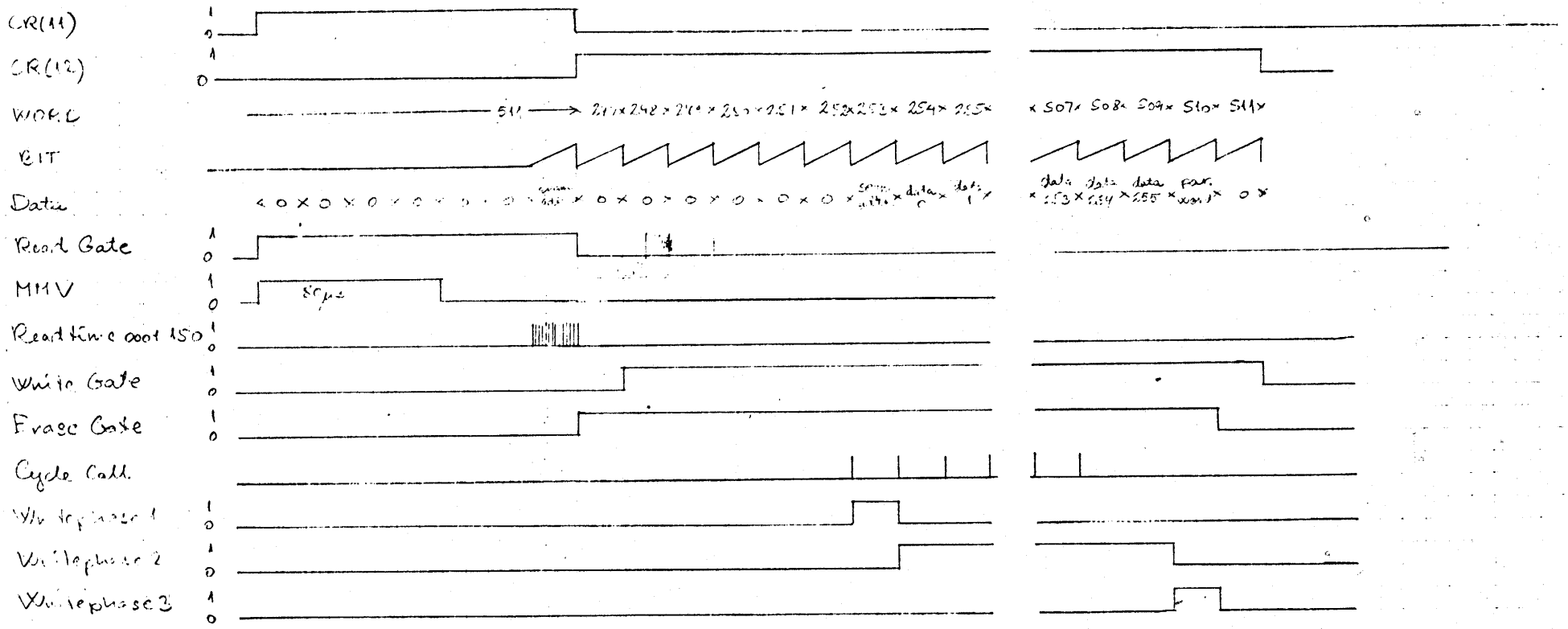
RC doc. V8 140

A/S REGNECENTRALEN	Designed by	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.
	04.07.70 FBF						

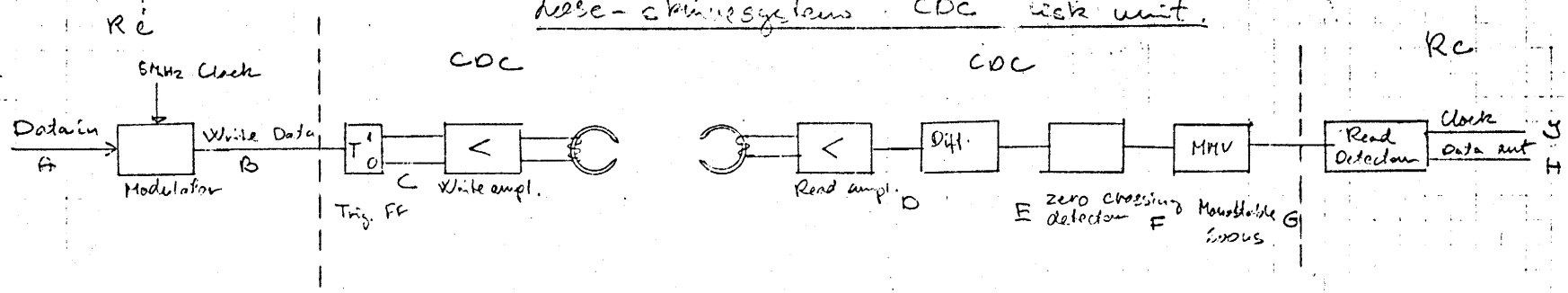
Dwg. No. | Unit

WRITE DATA TIMING DIAGRAM

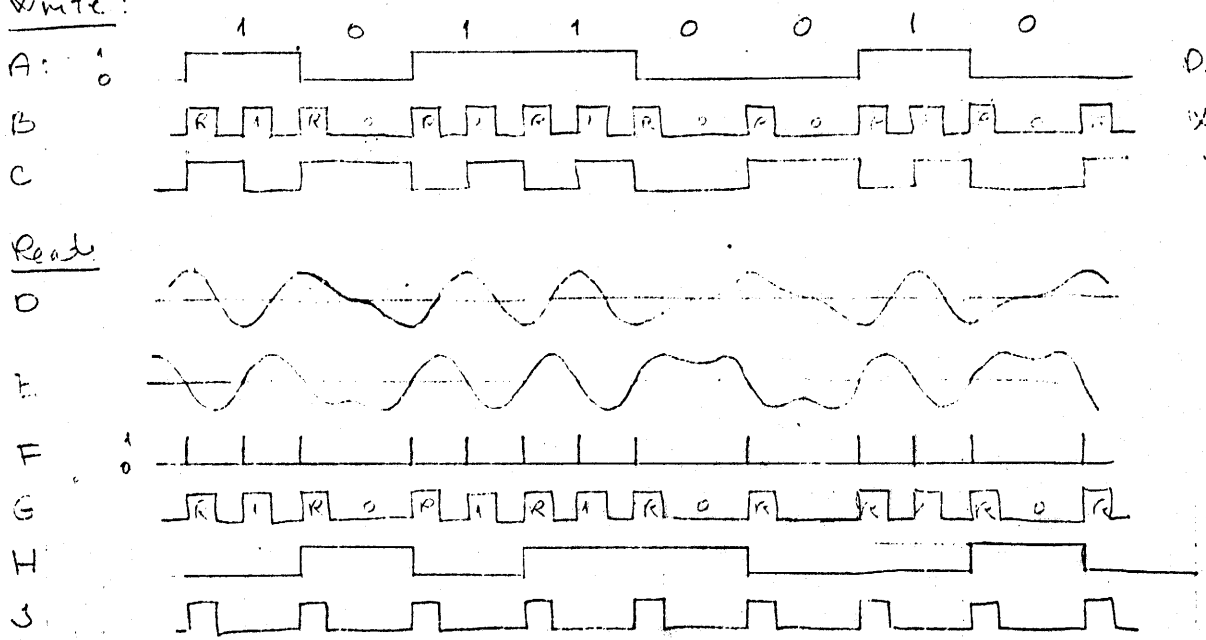
3. Write Data



Lese-skrivesystem CDC disk unit.



Write:



Data in

Write Data (CDC input)

Write Current

Playback signal

diff. playback signal

peaks on playback signal

Read Data (CDC output)

Data out

Clock

Unit: DFC	Designed 7.10.69	Read - Write signals	Drawing No
CENTRALEN	Approved		Drawn by
	Checked		Checked
	Last Revision		Sheets / Sheet