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Programmer's Reference Manual for IOM501
Dual RC350x I/O Interface to RC850

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Keywords: RC850, IOM501, RC3502.

Abstract: This paper describes the logical structure of the IOM501, RC350x interface to RC850.

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CONTENTS PAGE

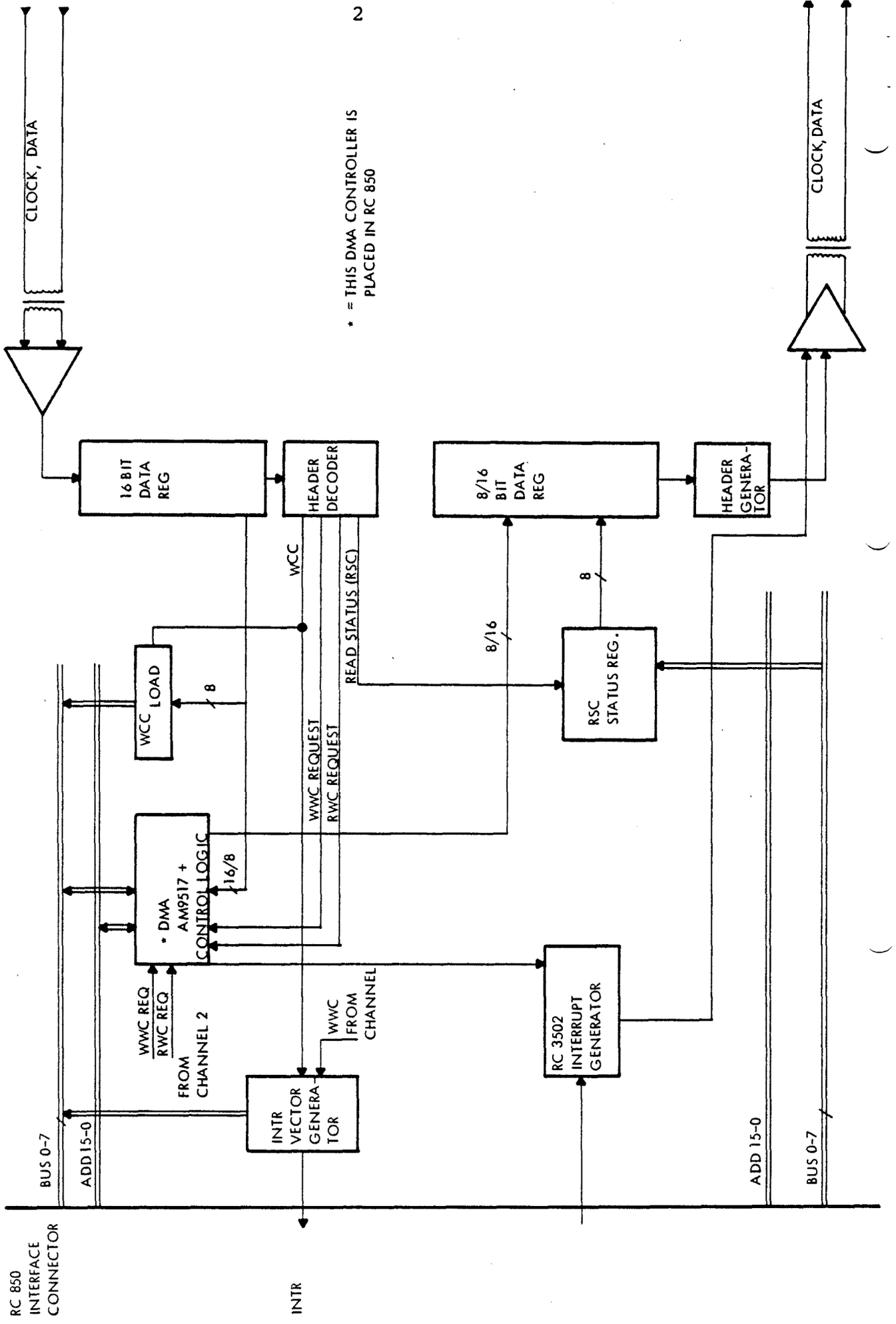
1. SHORT DESCRIPTION 1.

The IOM501 is connected to two RC350x I/O channels either on the same RC350x or on two RC350x.

The two I/O interfaces in IOM501 are totally independent of each other.

The block diagram for one I/O interface is shown on fig. 1.0.

Physically the IOM501 is placed inside the RC85x cabinet and powered from the RC85x power supply.



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IOM 501

BLOCKDIAGRAM FOR THE RC 3502 I/O CHANNEL INTERFACE.
ONLY CHANNEL 1 IS SHOWN, CHANNEL 2 HAS THE SAME LOGIC LAYOUT

Fig. 1.0

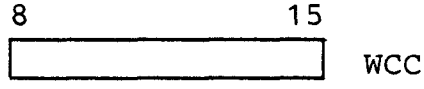
2. PROGRAMMING SPECIFICATION FROM RC350x 2.

The following section describes the possible I/O instructions seen from the RC350x programmer's point of view.

The Z80 device numbers mentioned in brackets refer to I/O CHANNEL 2.

2.1 WRITE CONTROL 2.1

From RC350x to IOM501.



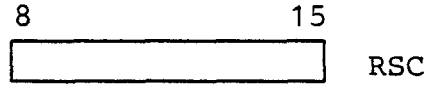
This command sets an 8-bits register with the information sent out.

This command interrupts Z80 (refer to section 3.4) and Z80 reads the contents of WCC by IN 38_H ($3C_H$).

Z80 BUS (7:0) := WCC (8:15).

2.2 READ STATUS 2.2

From IOM501 to RC350x.



This command transfers the contents of an 8-bits register in IOM501 to RC350x.

This register is set from Z80 by OUT 38_H ($3C_H$).

RSC (8:15) := Z80 BUS (7:0).

2.3 WRITE BLOCK OF BYTES 2.3

From RC350x to RC350x.

This command is used to transfer a block of bytes from RC350x to the Z80 memory using DMA channel 1 (3) to the RC850 controller (refer to RCSL: 31-D594, RC850 Controller Reference Manual).

Before starting this command, the Z80 has to be commanded to set up the DMA channel for input to the Z80 memory.

2.4 READ BLOCK OF BYTES 2.4

This command transfers a block of bytes from the Z80 memory to RC350x using DMA channel 1 (3).

3. PROGRAMMING SPECIFICATION FROM Z80 3.

The following description contains the specification of the hardware in IOM501 seen from the Z80 in RC850. Only CHANNEL 1 is described, but the device numbers for CHANNEL 2 are mentioned in brackets.

This paper is written as an extension of the RC850 Controller Reference Manual, RCSL: 31-D594.

3.1 Read WCC 3.1

IN 38_H Reads the contents of WCC I/O channel 1

IN $3C_H$ Reads the contents of WCC I/O channel 2

3.2 SET RSC 3.2

OUT 38_H Writes into RSC I/O channel 1

OUT $3C_H$ Writes into RSC I/O channel 2

3.3 GENERATE INTERRUPT TO RC350x 3.3

The following situations generate interrupts on I/O channel 1:

1) OUT $3B_H$ Sends interrupt.

2) OUT $3A_H$ Sends interrupt, requesting first data byte in a write block of bytes.

3) When the DMA channel 1 has a byte ready in a "read block of bytes" or is ready to accept a byte in "write block of bytes".

I/O channel 2 interrupt:

1) OUT $3F_H$

2) OUT $3E_H$

3) DMA channel 3 in RC850

3.4 INTERRUPT TO Z80 3.4

A Z80-CTC Timer/Counter circuit is used to generate interrupt vectors to Z80 whenever a "write control command" is decoded on I/O channel 1 or 2 from RC350x.

WCC from channel 1 is connected to Timer 2 (device 42_H) of the CTC and channel 2 to Timer 3 (device 43_H). The CTC should be initialized as follows:

```
TIM0   =   40H
TIM2   =   42H        ; Device number Timer 2
TIM3   =   43H        ; Device number Timer 3
CHINT  =   ?          ; Base interrupt vector from CTC
MCTC   =   D7H        ; Mode to CTC

; Begin

  LDA      CHINT      ; a := CHINT
  OUT      TIM0'
  LDA      MCTC       ; a := mode register contents
  OUT      TIM2
  OUT      TIM3

; end
```

For details about the CTC refer to Appendix A.

3.5 DMA Use

I/O channel 1 is connected to RC850 DMA chan 1 and I/O channel 2 to DMA chan 3.

When a transfer to or from the display is wanted, the following should be performed:

. set mode register as follows:
  select channel 1 (3)
  read or write transfer (read means read from)
  single mode (Z80 memory)
  Address increment
  Autoinitialize disable

. set base address

(OUT $3A_H$ ($3E_H$) if write block of bytes)
. set base word count
(OUT 39_H ($3D_H$) } if read block of bytes)
OUT $3B_H$ ($3F_H$) }

as follows:

```
LDA ...                          ; set register A to mode contents
OUT  FB_H                        ; output to mode register
OUT  FC_H                        ; clear internal Flip/Flop

LDA  'LOW BYTE                   ; set base address
OUT   F2_H (F6_H)
LDA  ' high BYTE
OUT   F2_H (F6_H)
(OUT  3A_H (3E_H)                ; if write
OUT   FC_H                       ; clear internal Flip/Flop
LDA  'LOW BYTE'                  ; set byte count
OUT   F3_H (F7_H)
```

```
LDA    'HIGH BYTE'
OUT    F3H (F7H)
OUT    39H (3DH)          ; if read
OUT    3BH (3FH)          ; if read
```

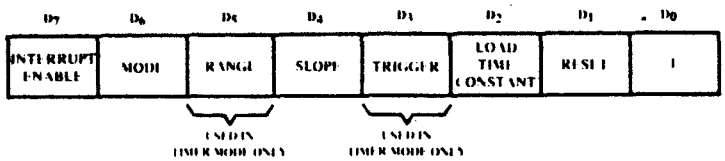
4. Z80 DEVICE NUMBERS USED IN IOM501 4.

No. (Hex)	FUNCTION	
	INPUT	OUTPUT
38	WRITE CONTROL REG (WCC) FROM RC3502 CHANNEL 1	SET STATUS REG (RSC) RO RC3502 CHANNEL 1
39	DUMMY	RESET FOR INPUT (READ Block of Bytes) to RC3502 CHANNEL 1
3A	DUMMY	RESET FOR OUTPUT (Write Block of Bytes) from RC3502 CHANNEL 1
3B	DUMMY	SEND INTERRUPT ON RC3502 CHANNEL 1
3C	WRITE CONTROL REG (WCC) FROM RC3502 CHANNEL 2	SET STATUS REG (RSC) TO RC3502 CHANNEL 2
3D	DUMMY	RESET FOR INPUT CHANNEL 2
3E	DUMMY	RESET FOR OUTPUT CHANNEL 2
3F	DUMMY	SEND INTERRUPT ON CHANNEL 2
40	COUNT/TIME Z80A-CTC TIMER 0 } NOT USED	
41	COUNT/TIME Z80A-CTC TIMER 1 } NOT USED	
42	COUNT/TIME Z80A-CTC TIMER 2 INTR CHANNEL 1	
43	COUNT/TIME Z80A-CTC TIMER 3 INTR CHANNEL 2	

A. Z80-CTC PROGRAMMING

SELECTING AN OPERATING MODE

When selecting a channel's operating mode, bit Ø is set to 1 to indicate this word is to be stored in the channel control register.



Bit 7 = Ø — Channel interrupts disabled.

Bit 7 = 1 — Channel interrupts enabled to occur every time Down Counter reaches a count of zero. Setting Bit 7 does not let a preceding count of zero cause an interrupt.

Bit 6 = Ø — Timer Mode – Down counter is clocked by the prescaler. The period of the counter is:

$t_C \bullet P \bullet TC$

t_C = system clock period

P = prescale of 16 or 256

TC = 8 bit binary programmable time constant (256 max)

Bit 6 = 1 — Counter Mode – Down Counter is clocked by external clock. The prescaler is not used.

Bit 5 = Ø — Timer Mode Only–System clock Φ is divided by 16 in prescaler.

Bit 5 = 1 — Timer Mode Only–System clock Φ is divided by 256 in prescaler.

Bit 4 = Ø — Timer Mode – negative edge trigger starts timer operation.
Counter Mode – negative edge decrements the down counter.

Bit 4 = 1 — Timer Mode – positive edge trigger starts timer operation.
Counter Mode – positive edge decrements the down counter.

Bit 3 = Ø — Timer Mode Only – Timer begins operation on the rising edge of T_2 of the machine cycle following the one that loads the time constant.

Bit 3 = 1 — Timer Mode Only – External trigger is valid for starting timer operation after rising edge of T_2 of the machine cycle following the one that loads the time constant. The Prescaler is decremented 2 clock cycles later if the setup time is met, otherwise 3 clock cycles.

Bit 2 = Ø — No time constant will follow the channel control word. One time constant must be written to the channel to initiate operation.

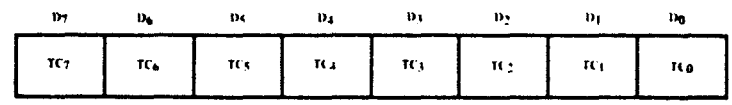
Bit 2 = 1 — The time constant for the Down Counter will be the next word written to the selected channel. If a time constant is loaded while a channel is counting, the present count will be completed before the new time constant is loaded into the Down Counter.

Bit 1 = Ø — Channel continues counting.

Bit 1 = 1 — Stop operation. If Bit 2 = 1 channel will resume operation after loading a time constant, otherwise a new control word must be loaded.

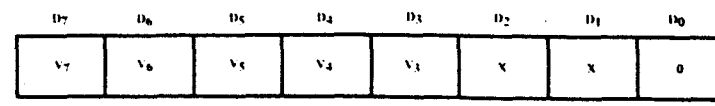
LOADING A TIME CONSTANT

An 8-bit time constant is loaded into the Time Constant register following a channel control word with bit 2 set. All zeros indicate a time constant of 256.

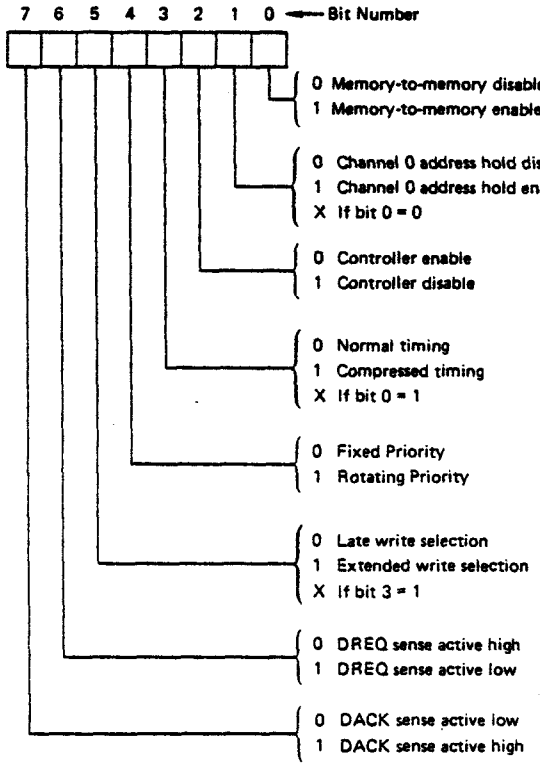


LOADING AN INTERRUPT VECTOR

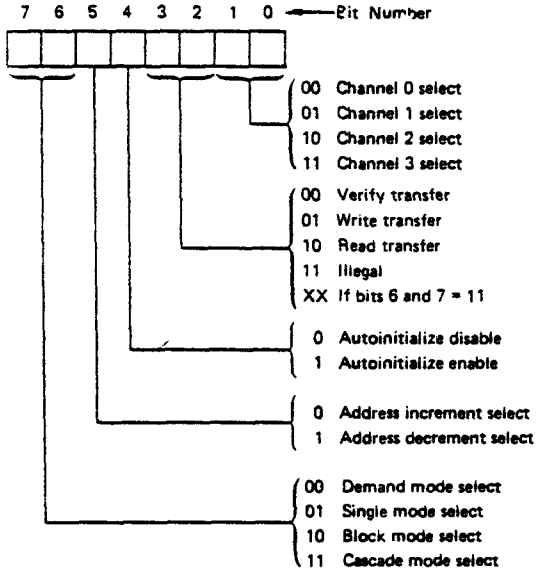
The Z80-CPU requires that an 8-bit interrupt vector be supplied by the interrupting channel. The CPU forms the address for the interrupt service routine of the channel using this vector. During an interrupt acknowledge cycle the vector is placed on the Z80 Data Bus by the highest priority channel requesting service at that time. The desired interrupt vector is loaded into the CTC by writing into channel Ø with a zero in DØ. D7-D3 contain the stored interrupt vector, D_2 and D_1 are not used in loading the vector. When the CTC responds to an interrupt acknowledge, these two bits contain the binary code of the highest priority channel which requested the interrupt and DØ contains a zero since the address of the interrupt service routine starts at an even byte. Channel Ø is the highest priority channel.



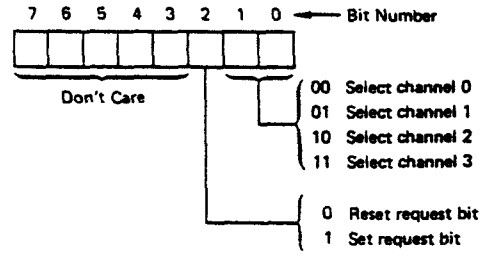
Command Register: This 8-bit register controls the operation of the Am9517A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset. The following table lists the function of the command bits. See Figure 4 for address coding.



Mode Register: Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register it to be written.

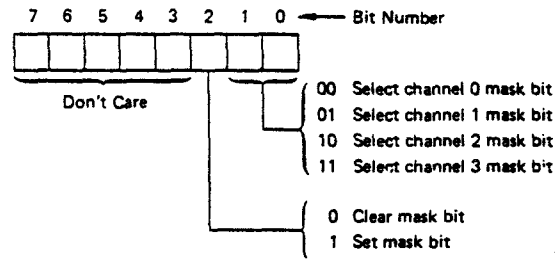


Request Register: The Am9517A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are nonmaskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 4 for address coding.

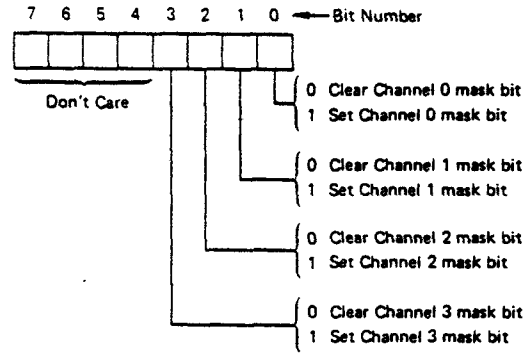


Software requests will be serviced only if the channel is in Block mode. When initiating a memory-to-memory transfer, the software request for channel 0 should be set.

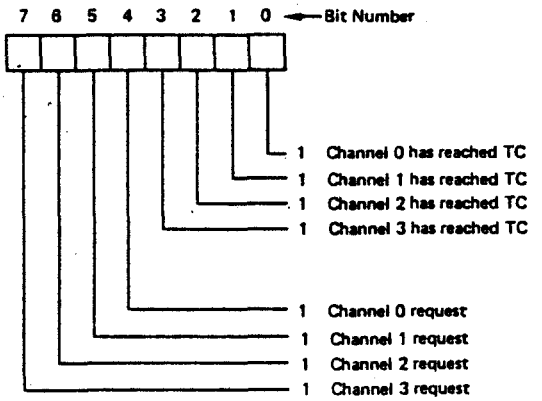
Mask Register: Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. See Figure 4 for instruction addressing.



All four bits of the Mask Register may also be written with a single command.



Status Register: The Status registers may be read out of the Am9517A by the microprocessor. It indicates which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set each time a TC is reached by that channel, including after each Autoinitialization. These bits are cleared by Reset and each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service.



Temporary Register: The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Software Commands: There are two special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The two software commands are:

Clear First/Last Flip/Flop: This command may be issued prior to writing or reading Am9517A address or word count information. This initializes the flip/flop to a known state so that subsequent accesses to register contents by the microprocessor will address lower and upper bytes in the correct sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary and Internal First/Last Flip/Flop registers are cleared and the Mask register is set. The Am9517A will enter the Idle cycle.

Figure 4 lists the address codes for the software commands.

Device No.	Interface Signals						Operation
	A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
F8	1	0	0	0	0	1	Read Status Register
	1	0	0	0	1	0	Write Command Register
F9	1	0	0	1	0	1	Illegal
	1	0	0	1	1	0	Write Request Register
FA	1	0	1	0	0	1	Illegal
	1	0	1	0	1	0	Write Single Mask Register Bit
FB	1	0	1	1	0	1	Illegal
	1	0	1	1	1	0	Write Mode Register
FC	1	1	0	0	0	1	Illegal
	1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
FD	1	1	0	1	0	1	Read Temporary Register
	1	1	0	1	1	0	Master Clear
FE	1	1	1	0	0	1	Illegal
	1	1	1	0	1	0	Illegal
FF	1	1	1	1	0	1	Illegal
	1	1	1	1	1	0	Write All Mask Register Bits

Figure 4. Register and Function Addressing.

Channel	Register	Operation	Signals							Internal Flip/Flop	Data Bus DB0–DB7	Device No.
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0			
0	Base & Current Address	Write	0	1	0	0	0	0	0	0	A0-A7	
			0	1	0	0	0	0	0	1	A8-A15	
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7	
			0	0	1	0	0	0	0	1	A8-A15	
	Base & Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7	
			0	1	0	0	0	0	1	1	W8-W15	
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7	
			0	0	1	0	0	0	1	1	W8-W15	
1	Base & Current Address	Write	0	1	0	0	0	1	0	0	A0-A7	F2
			0	1	0	0	0	1	0	1	A8-A15	
I/O channel 1	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7	
			0	0	1	0	0	1	0	1	A8-A15	
	Base & Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7	F3
			0	1	0	0	0	1	1	1	W8-W15	
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7	
			0	0	1	0	0	1	1	1	W8-W15	
2	Base & Current Address	Write	0	1	0	0	1	0	0	0	A0-A7	
			0	1	0	0	1	0	0	1	A8-A15	
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7	
			0	0	1	0	1	0	0	1	A8-A15	
	Base & Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7	
			0	1	0	0	1	0	1	1	W8-W15	
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7	
			0	0	1	0	1	0	1	1	W8-W15	
3	Base & Current Address	Write	0	1	0	0	1	1	0	0	A0-A7	F6
			0	1	0	0	1	1	0	1	A8-A15	
I/O channel 2	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7	
			0	0	1	0	1	1	0	1	A8-A15	
	Base & Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7	F7
			0	1	0	0	1	1	1	1	W8-W15	
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7	
			0	0	1	0	1	1	1	1	W8-W15	

Fig. 5: Word Count and Address Register Command Codes.

RETURN LETTER

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Title: Dual RC350x I/O Interface to RC850 RCSL No.: 52-AA1028

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