RCSL No: 52-AA1044

Edition: May, 1981

Author: Knud E. Hansen

Title:

Technical Description for IQM501

RCSL 42-11592

A/S REGNECENTRALEN
af 1979

Keywords:

RC853, IOM501, Technical Description.

Abstract:

This paper contains all technical information about IOM501, dual RC350x I/O interface to RC850.

(46 printed pages).

Printed by A/S Regnecentralen af 1979, Copenhagen

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1. SHORT DESCRIPTION 1.

The IOM501 is connected to two RC350x I/O channels, either on the same RC350x or on two RC350x.

The two I/O interfaces in IOM501 are totally independent of each other.

Physically the IOM501 is placed inside the RC85x cabinet and powered from the RC85x power supply.

Before continuing reading this manual the reader should be familiar with the Z80 microprocessor system in the RC85x display and the paper RCSL: 52-AA1028, Programmer's Reference Manual for IOM501.

2. FUNCTIONAL DESCRIPTION 2.

Logically the IOM501 interface consists of two identical RC350x controllers, each divided into two parts:

1. I/O Interface (IOI)
2. RC850 Interface

In the following each unit is further described, only for channel 1; the numbers in brackets refer to channel 2.

2.1 I/O Interface 2.1

The IOI takes care of the communication between RC350x and the IOM. For details refer to block diagram fig. 2.0.

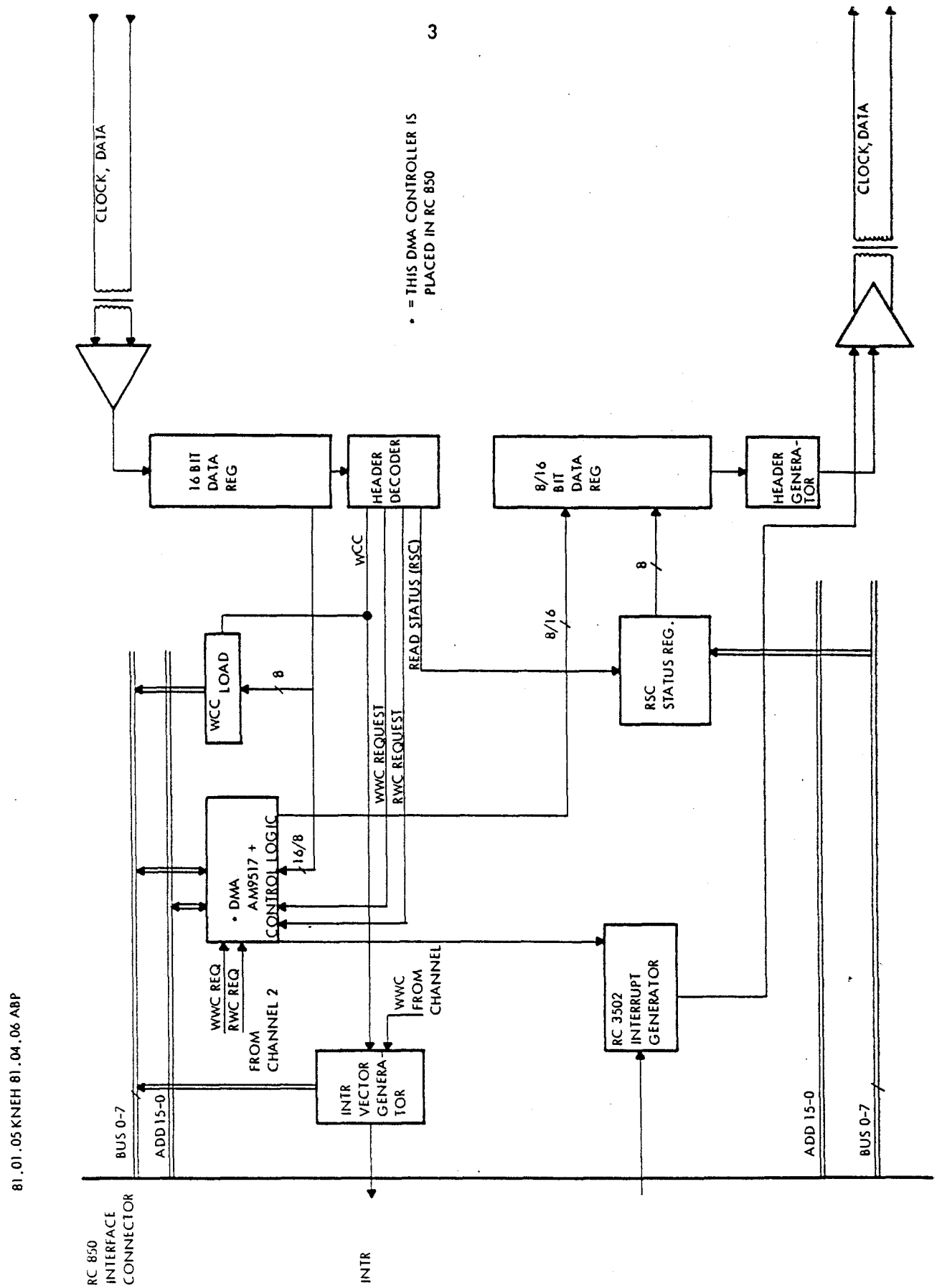
2.1.1 Line Receiver and Demodulator 2.1.1

For details refer to logic diagram 1.

Two balanced signals are received from RC350x, serial data on DATA OUT A-B and clock on CLOCK OUT A-B.

By using transformer coupling, galvanic separation is obtained between RC350x and the IOM interface.

In the demodulator the serial data stream is synchronized with the received clock so that a negative shift on DATA OUT corresponds to a trailing edge on CLOCK OUT.



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IOM 501

BLOCKDIAGRAM FOR THE RC 3502 I/O CHANNEL INTERFACE.
ONLY CHANNEL 1 IS SHOWN, CHANNEL 2 HAS THE SAME LOGIC LAYOUT

Fig. 2.0

2.1.2 Line Driver and Modulator

2.1.2

For details refer to logic diagram 2.

In the modulator the serial data (DATA IN) and the interrupt signal (-, SITR) are mixed, because an interrupt is sent as a logic 1 element on the data lines DATA IN A-B. RC350x decodes a logic 1 on DATA IN A-B as an interrupt whatever moment an input instruction (Read Data, Read Status) is not in progress on the I/O channel in question.

2.1.3 DATA OUT Register and HEADER DECODER

2.1.3

For details refer to logic diagram 3 (7).

The serial data received on DATA OUT is shifted into the DATA OUT register. The received word contains 20 bits, 16 data bits and 4 header bits. When the first synchronization bit in the Header is recognized in the bottom of the register, the SHIFT CLOCK is stopped and the header is decoded in accordance with the following table:

Command	Header $1\ x_1\ x_0\ 1$	Strobe pulse
WRITE CONTROL	1 1 1 1	-, WRITE CONTROL 1 (2)
WRITE DATA	1 0 1 1	-, WRITE DATA 1 (2)
READ DATA	1 0 0 1	-, READ DATA 1 (2)
READ STATUS	1 1 0 1	-, READ STATUS 1 (2)
	↑	First bit on DATA OUT

2.1.4 DATA IN/STATUS Register and Header Generator 2.1.4

For details refer to logic diagram 4 (8).

This is a 12 bits parallel to serial shift register.

If a READ DATA Header is decoded, the strobe pulse READ DATA 1 (2) loads the register with the Read Data byte; and the contents of the register is shifted serial to the demodulator (section 2.1.3) by CLOCK IN. The Read Data word is 8 bits.

If a READ STATUS Header is decoded, the strobe pulse READ STATUS 1 (2) loads the register with the Status byte; and the contents of the register is shifted serial to the modulator (section 2.1.3) by CLOCK IN. The Status word is 8 bits.

The Header contains the following information:

Command	Header 1 x_1 x_0 1
READ DATA	1 0 1 1
READ STATUS	1 0 1 1
	↑ The first bit sends on DATA IN

2.1.5 Interrupt Circuit 2.1.5

For details refer to logic diagram 3 (7).

Whenever data is received from RC350x (CLOCK OUT is pulsed) a monostable is started to block transmission of interrupts. The monostable runs 6 µs. after the last CLOCK OUT pulse to secure that the data byte as response to a READ DATA command is transmitted to RC350x before enabling interrupt transmission.

2.2 RC850 Interface 2.2

This logic module is divided into the following sections:

a. Z80 I/O address decoder
b. Z80 Interrupt generator
c. Command/Status sequence
d. DMA logic

2.2.1 Z80 I/O Address Decoder 2.2.1

For details refer to logic diagram 11.

This circuit consists of a ROM (ROA623) decoding the value on Z80 address bus ADD 7-0. During DMA operations -, HOLD ACK disables the decoder. On fig. 2.1 is shown the contents of this decoder ROM.

2.2.2 Z80 Interrupt Generator 2.2.2

For details refer to logic diagram 11.

Z80A-CTC (4 timer circuit) is used as interrupt generator to the Z80 CPU system. The counters are initialized to 1; when a write control is received, the corresponding counts down to zero causing an interrupt to Z80; the Z80 interrupt routine sets the counter back to 1.

2.2.3 Command/Status Sequence 2.2.3

Refer to logic diagram 6 (10).

The write control byte from RC350x is loaded into an 8 bits register, accessible by I/O read from the Z80; in addition an interrupt is sent to the Z80.

I/O DEVICE NUMBER DECODER (ROA623)															
ADDRESS INPUT (pin numbers)										PIN-OUT									
19	18	17	16	5	4	3	2	1	HEX	6	7	8	9	11	12	13	14	FUNCTION
$0\text{-}377_8$									0-FF	1	0	0	0	1	0	0	1	IDLE
$400\text{-}467_8$									100-137	1	0	0	0	1	0	0	1	IDLE
470_8									138	1	0	0	0	0	0	1	1	-, EN WCC1 / -, SET STATUS1
471_8									139	1	1	0	0	1	0	1	1	-, SET FIRST REQ1
472_8									13A	1	0	1	0	1	0	1	1	-, START WRITE1
473_8									13B	1	1	1	0	1	0	1	1	-, SEND ITR1
474_8									13C	1	0	0	1	1	0	1	0	-, EN WCC2 / -, SET STATUS2
475_8									13D	1	1	0	1	1	0	1	1	-, SET FIRST REQ2
476_8									13E	1	0	1	1	1	0	1	1	-, START WRITE2
477_8									13F	1	1	1	1	1	0	1	1	-, SEND ITR2
$500\text{-}503_8$									140-143	0	0	0	0	1	0	0	1	Enable Z80A-CTC
$504\text{-}777_8$									144-1FF	1	0	0	0	1	0	0	1	IDLE

Fig. 2.1

Z80 can set an 8 bit status register accessible from RC350x by READ STATUS.

2.2.4 DMA Logic 2.2.4

For details refer to logic diagram 5 (9).

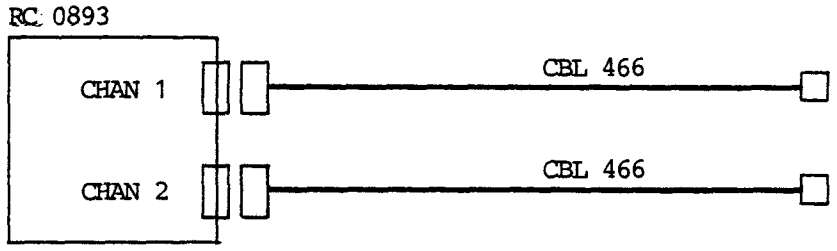
The IOM501 interface uses two free DMA channels in the RC850 DMA controller (AM9517).

I/O channel 1 is connected to DMA channel 1.
I/O channel 2 is connected to DMA channel 3.

WRITE DATA/READ DATA from RC350x starts the DMA sequence; when the DMA is ready again, an interrupt is sent to RC350x.

To start transfer from Z80 memory to RC350x a special I/O write from Z80 is necessary to get the first byte from Z80 memory.

3. INSTALLATION 3.



CBL466 is used as connection between RC853 and an I/O channel on RC350x.

Internal CBL681 is used to connect IOM501 with the back panel of RC853.

CHAN1 on RC853 is connected to J2 on IOM501.
CHAN2 - RC853 - - - J3 - IOM501.

SIGNAL	DESTINATION	DESCRIPTION
CLOCK OUT 1	p. 3	CLOCK OUT channel 1
CLOCK OUT 2	p. 7	CLOCK OUT channel 2
¬ DATA 1	p. 1	Serial DATA from channel 1
¬ DATA 2	p. 1	Serial DATA from channel 2
DATA OUT 1	p. 3	DATA OUT 1
DATA OUT 2	p. 7	DATA OUT 2

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Unit		
IOM501		
Dwg. No. A25893		p. 1 of 12

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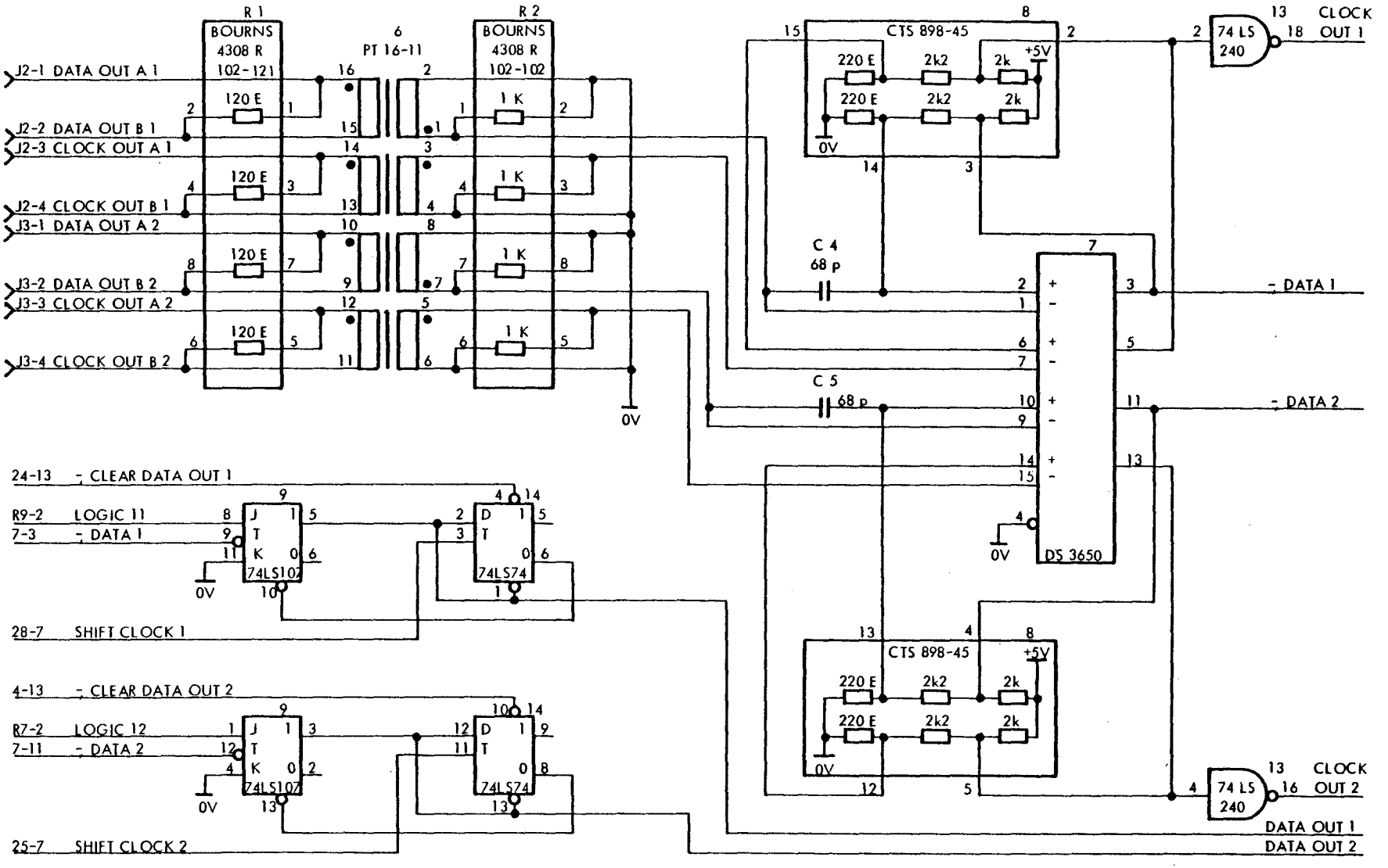

SIGNAL	DESTINATION	DESCRIPTION
CLOCK IN	p. 2 p. 3 p. 4 p. 7 p. 8	Internal clock 4.9152 MHz
-, CLOCK IN	p. 2 p. 3 p. 7	Same as above

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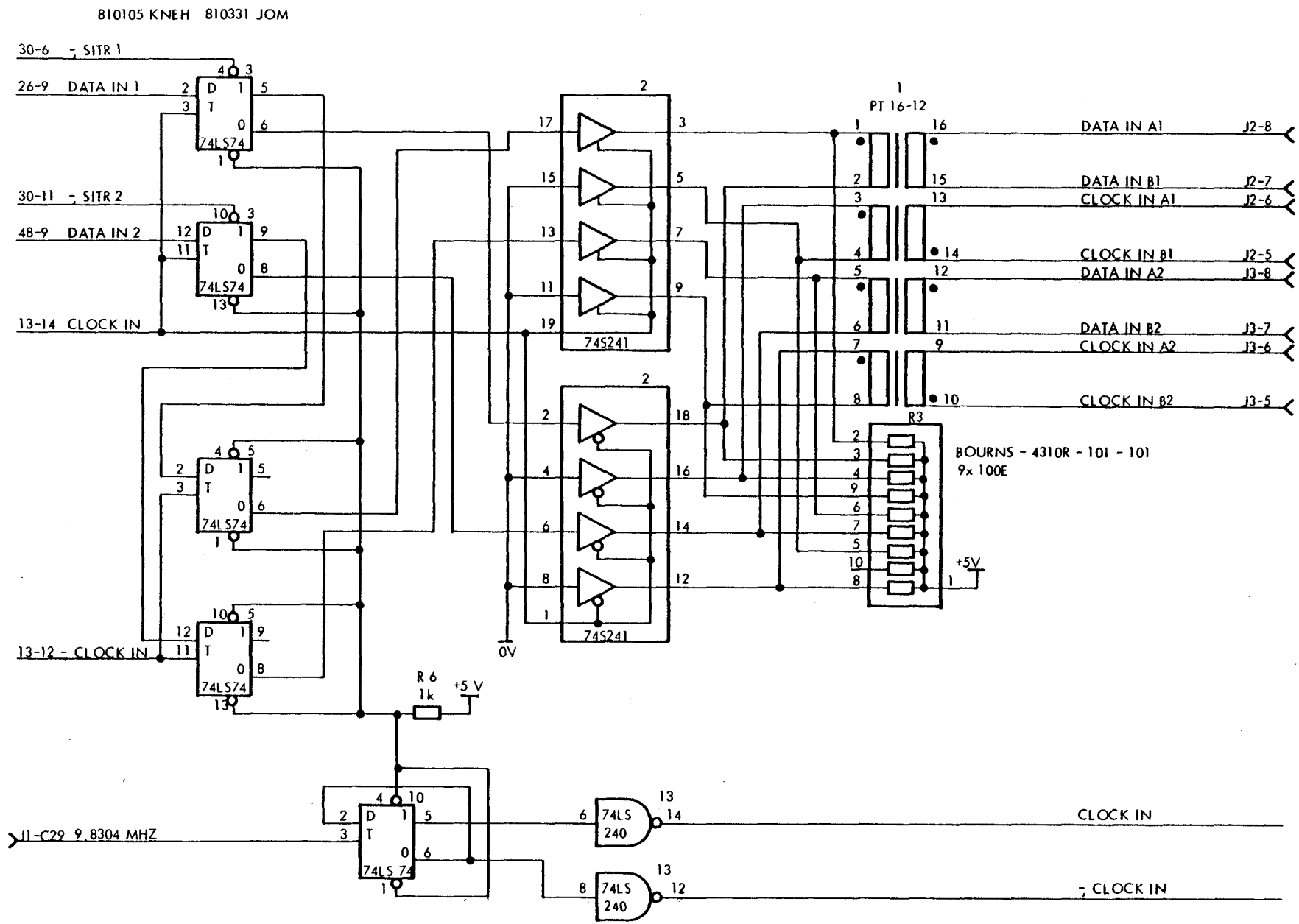
810105 KNEH 810331 JOM
30-6 - SITR 1
26-9 DATA IN 1
30-11 - SITR 2
48-9 DATA IN 2
13-14 CLOCK IN
13-12 - CLOCK IN
74LS74
74S241
R 6
1k
+5 V
0V
R3
BOURNS - 4310R - 101 - 101
9x 100E
+5V
PT 16-12
DATA IN A1
DATA IN B1
CLOCK IN A1
CLOCK IN B1
DATA IN A2
DATA IN B2
CLOCK IN A2
CLOCK IN B2
J2-8
J2-7
J2-6
J2-5
J3-8
J3-7
J3-6
J3-5
11-C29 9.8304 MHZ
74LS 74
74LS 240
CLOCK IN
- CLOCK IN

SIGNAL	DESTINATION	DESCRIPTION
-, CLEAR DATA OUT 1	p. 1	-, CLEAR DATA OUT register
DATA OUT 81-151	p. 5 p. 6	Parallel output from the DATA OUT register
READ DATA 1	p. 4	READ DATA output from header decoder
-, READ DATA 1	p. 5	Same as above
READ STATUS	p. 4	READ STATUS output from header decoder. Load the DATA IN register with status information.
SHIFT CLOCK 1	p. 1	SHIFT CLOCK to the DATA OUT register
-, SITR 1	p. 2	-, Send InTeRrupt on channel 1
LOGIC 11	p. 1 p. 3 p. 4	
-, WRITE CONTROL 1	p. 6	Header decode output
-, WRITE DATA 1	p. 5	Header decode output

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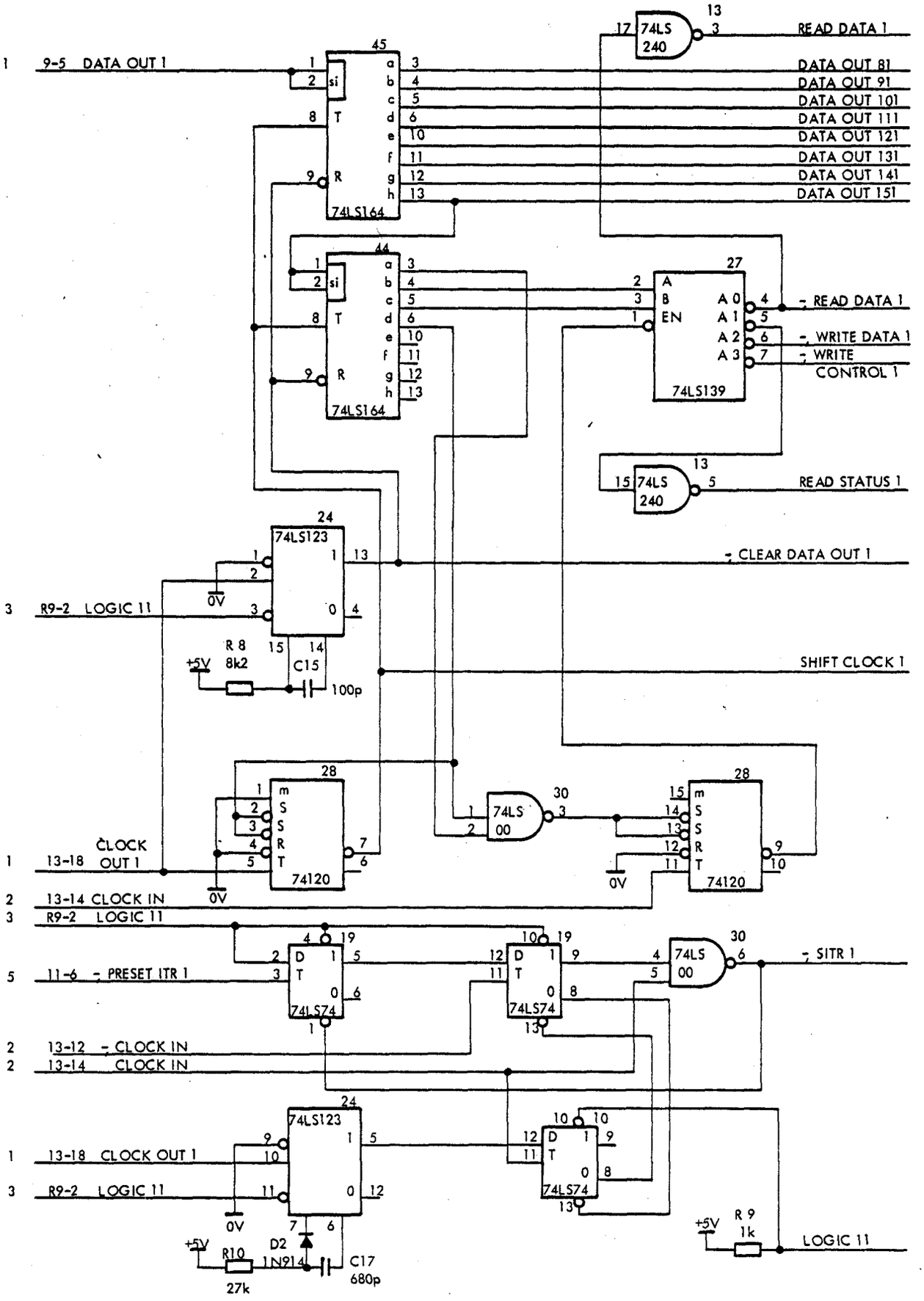

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SIGNAL	DESTINATION	DESCRIPTION
DATA IN 1	p. 2	Serial output from the DATA IN register to the modulator

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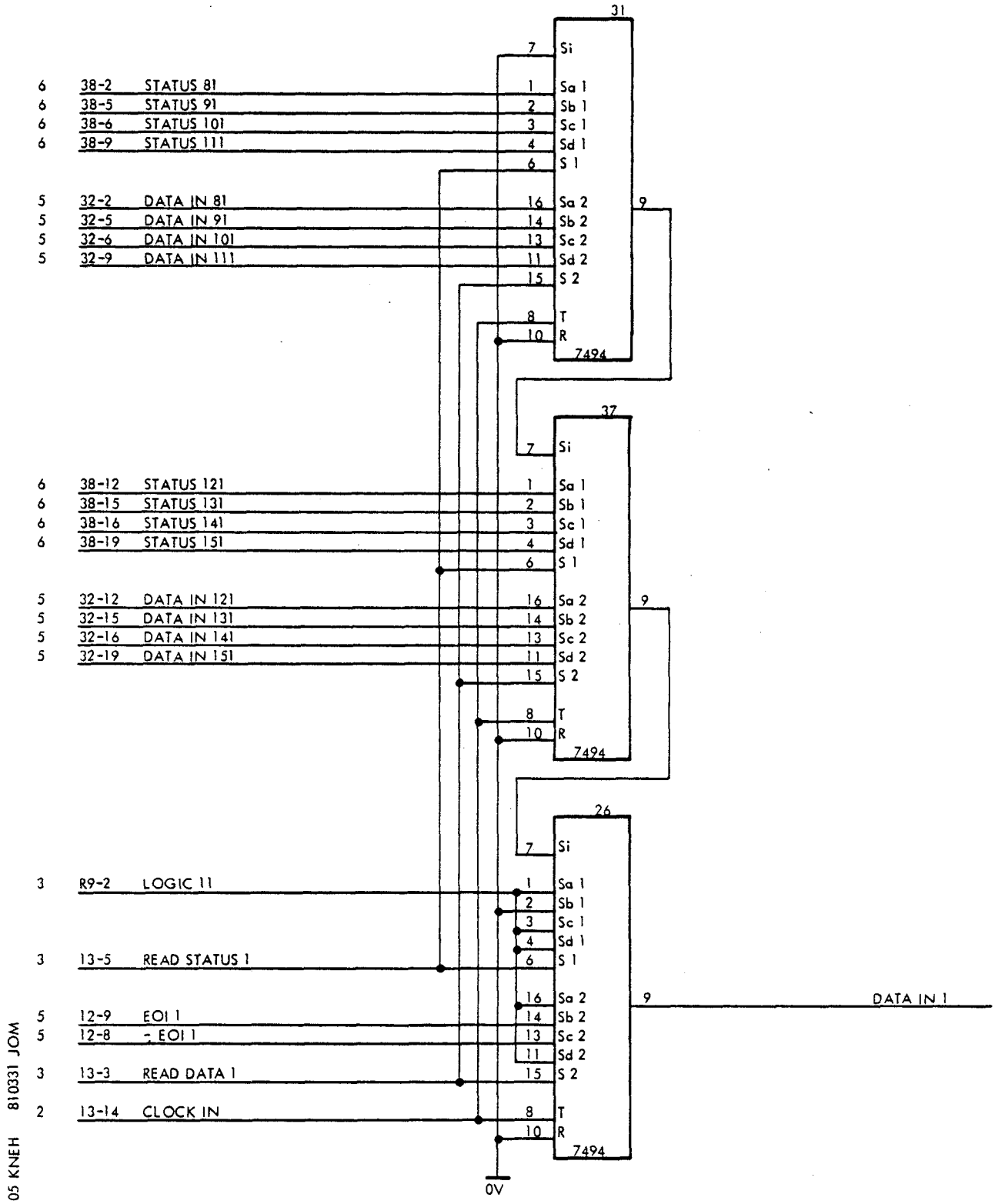
31
7 Si
6 38-2 STATUS 81 — 1 Sa 1
6 38-5 STATUS 91 — 2 Sb 1
6 38-6 STATUS 101 — 3 Sc 1
6 38-9 STATUS 111 — 4 Sd 1
6 S 1
5 32-2 DATA IN 81 — 16 Sa 2
5 32-5 DATA IN 91 — 14 Sb 2
5 32-6 DATA IN 101 — 13 Sc 2
5 32-9 DATA IN 111 — 11 Sd 2
15 S 2
8 T
10 R
9
7494
37
7 Si
6 38-12 STATUS 121 — 1 Sa 1
6 38-15 STATUS 131 — 2 Sb 1
6 38-16 STATUS 141 — 3 Sc 1
6 38-19 STATUS 151 — 4 Sd 1
6 S 1
5 32-12 DATA IN 121 — 16 Sa 2
5 32-15 DATA IN 131 — 14 Sb 2
5 32-16 DATA IN 141 — 13 Sc 2
5 32-19 DATA IN 151 — 11 Sd 2
15 S 2
8 T
10 R
9
7494
26
7 Si
3 R9-2 LOGIC 11 — 1 Sa 1
2 Sb 1
3 Sc 1
4 Sd 1
3 13-5 READ STATUS 1 — 6 S 1
16 Sa 2
5 12-9 EOI 1 — 14 Sb 2
5 12-8 - EOI 1 — 13 Sc 2
11 Sd 2
3 13-3 READ DATA 1 — 15 S 2
2 13-14 CLOCK IN — 8 T
10 R
9
DATA IN 1
7494
0V
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SIGNAL	DESTINATION	DESCRIPTION
BUS 0-7	p. 12	Z80 data bus. BUS 0 carries the LSB.
DATA IN 81-151	p. 4	Data read from the Z80 memory by DMA channel 1.
-, DRQ 1	J1	-, Dma ReQuest 1
-, END ITR 1	p. 11	Interrupt to Z80 if Termination on DMA channel 1
EOI 1	p. 4	End Of Information 1. Set -, END ITR 1. Clear'ed when starting a DMA transfer from Z80.
-, EOI 1	p. 4	Same as above
-, PRESET ITR 1	p. 3	Send ITR on RC3500 channel 1

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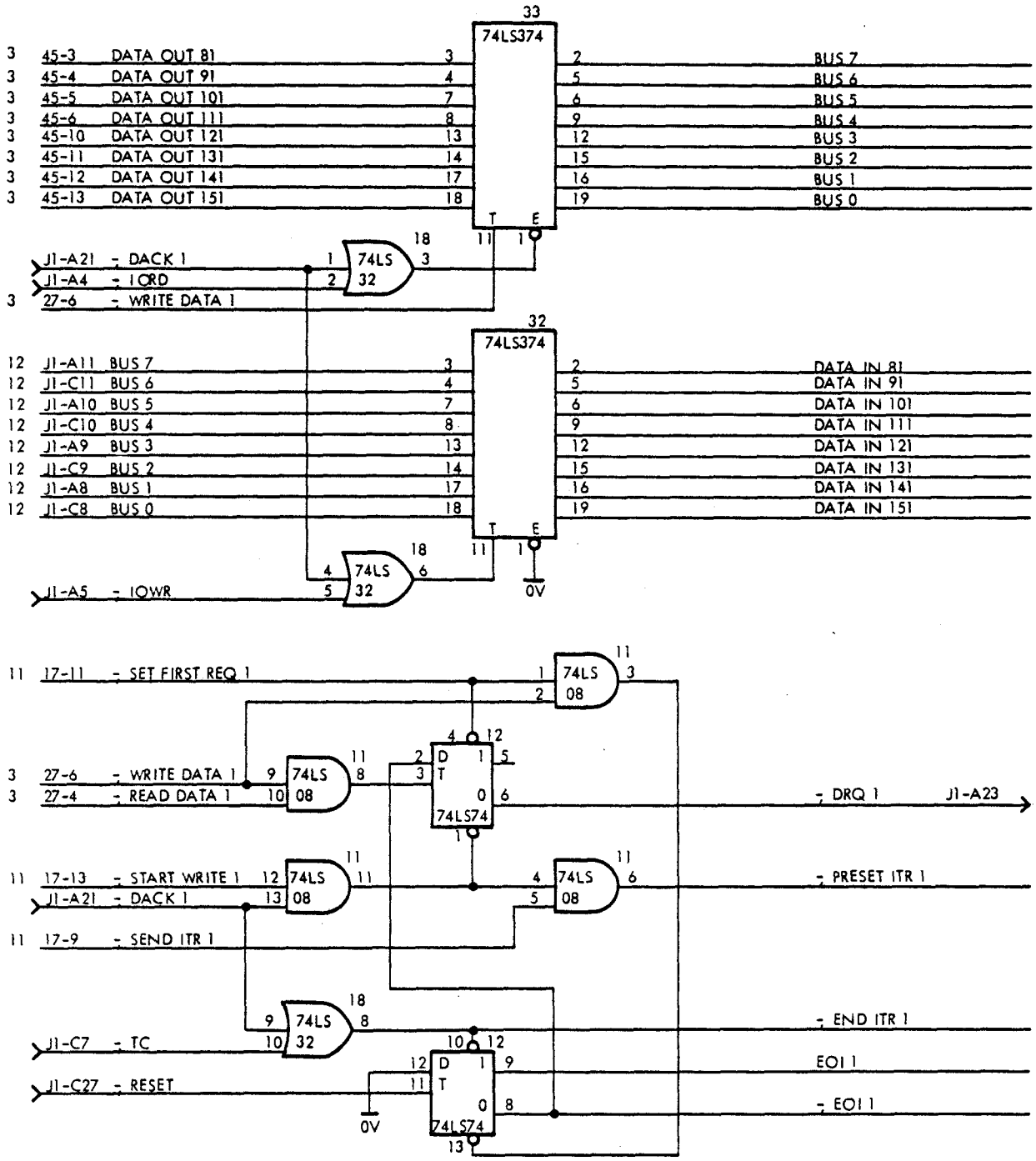

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SIGNAL	DESTINATION	DESCRIPTION
BUS 0-7	p. 12	Z80 data bus. BUS 0 is the LSB.
STATUS 81-151	p. 4	Status register output set by Z80.
-, WCC ITR 1	p. 11	-, send WCC Interrupt to Z80.

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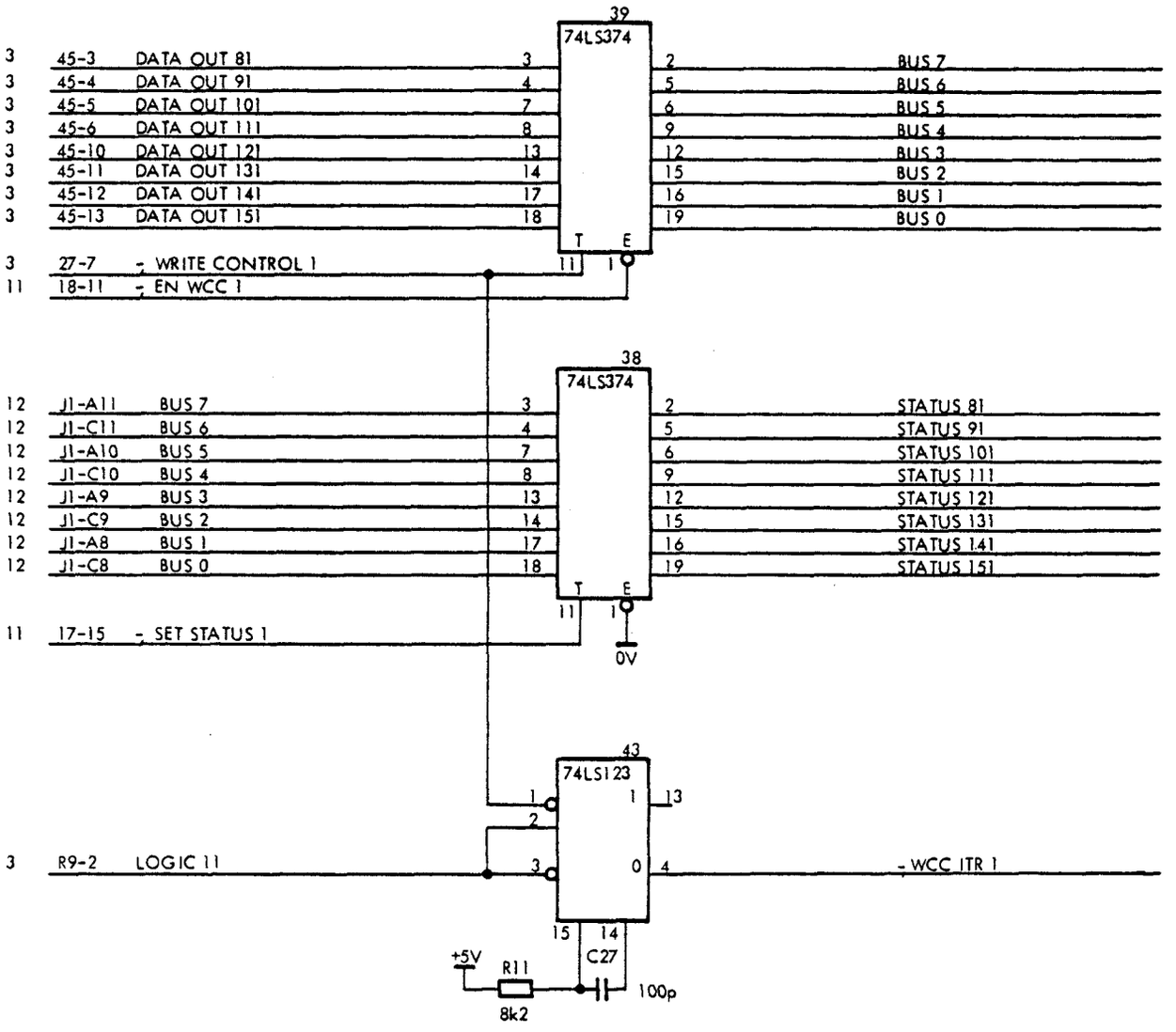

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SIGNAL	DESTINATION	DESCRIPTION
-, CLEAR DATA OUT 2	p. 1	-, CLEAR DATA OUT register
DATA OUT 82-152	p. 9 p. 10	Parallel output from the DATA OUT register
READ DATA 2	p. 8	READ DATA output from header decoder
-, READ DATA 2	p. 9	Same as above
READ STATUS 2	p. 8	READ STATUS output from header decoder. Load the DATA IN register with status information.
SHIFT CLOCK 2	p. 1	SHIFT CLOCK to the DATA OUT register
-, SITR 2	p. 2	-, Send InTeRrupt on channel 2
LOGIC 12	p. 1 p. 7 p. 8	
-, WRITE CONTROL 2	p. 10	Header decode output
-, WRITE DATA 2	p. 9	Header decode output

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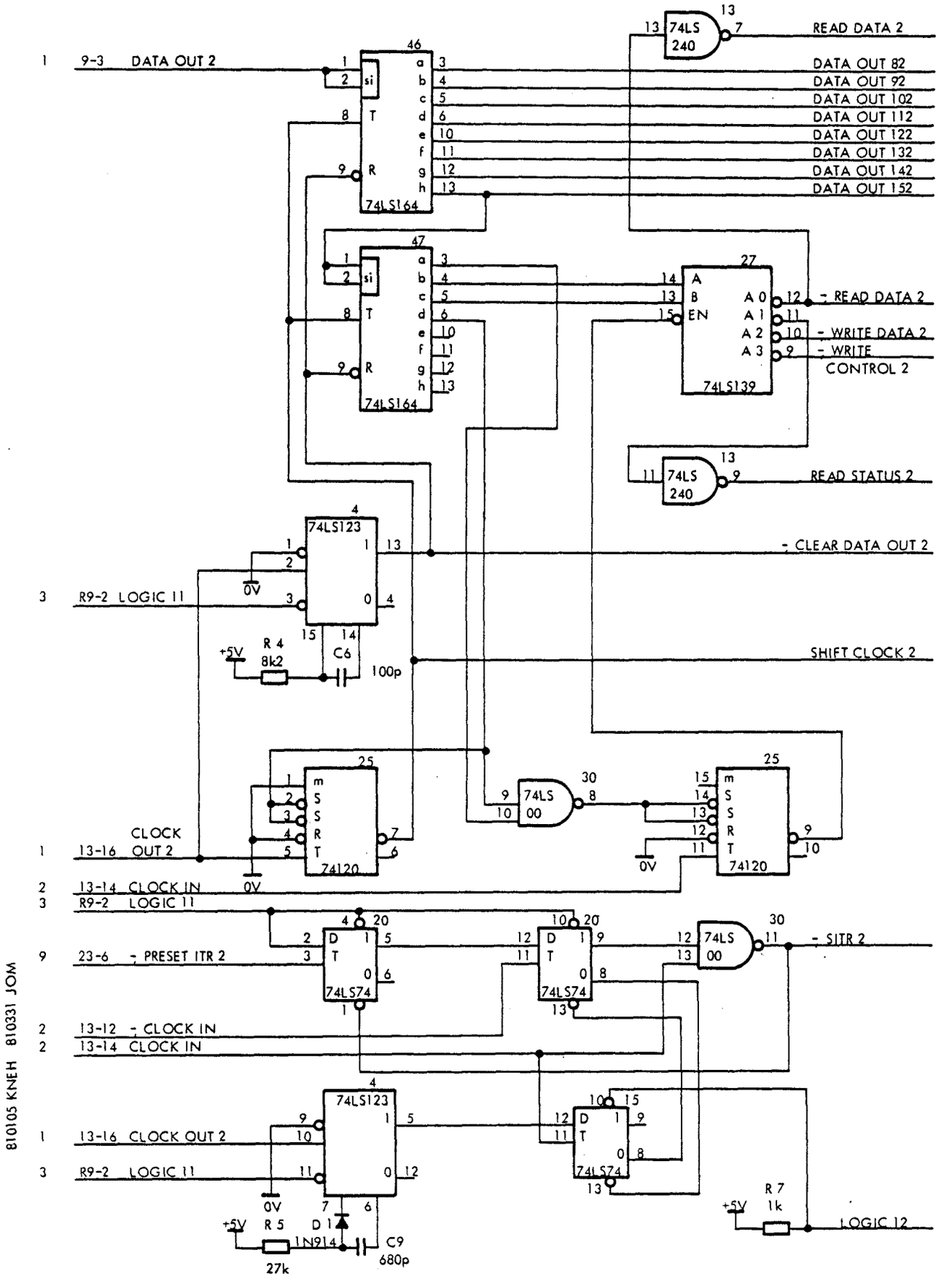

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SIGNAL	DESTINATION	DESCRIPTION
DATA IN 2	p. 2	Serial output from the DATA IN register to the modulator

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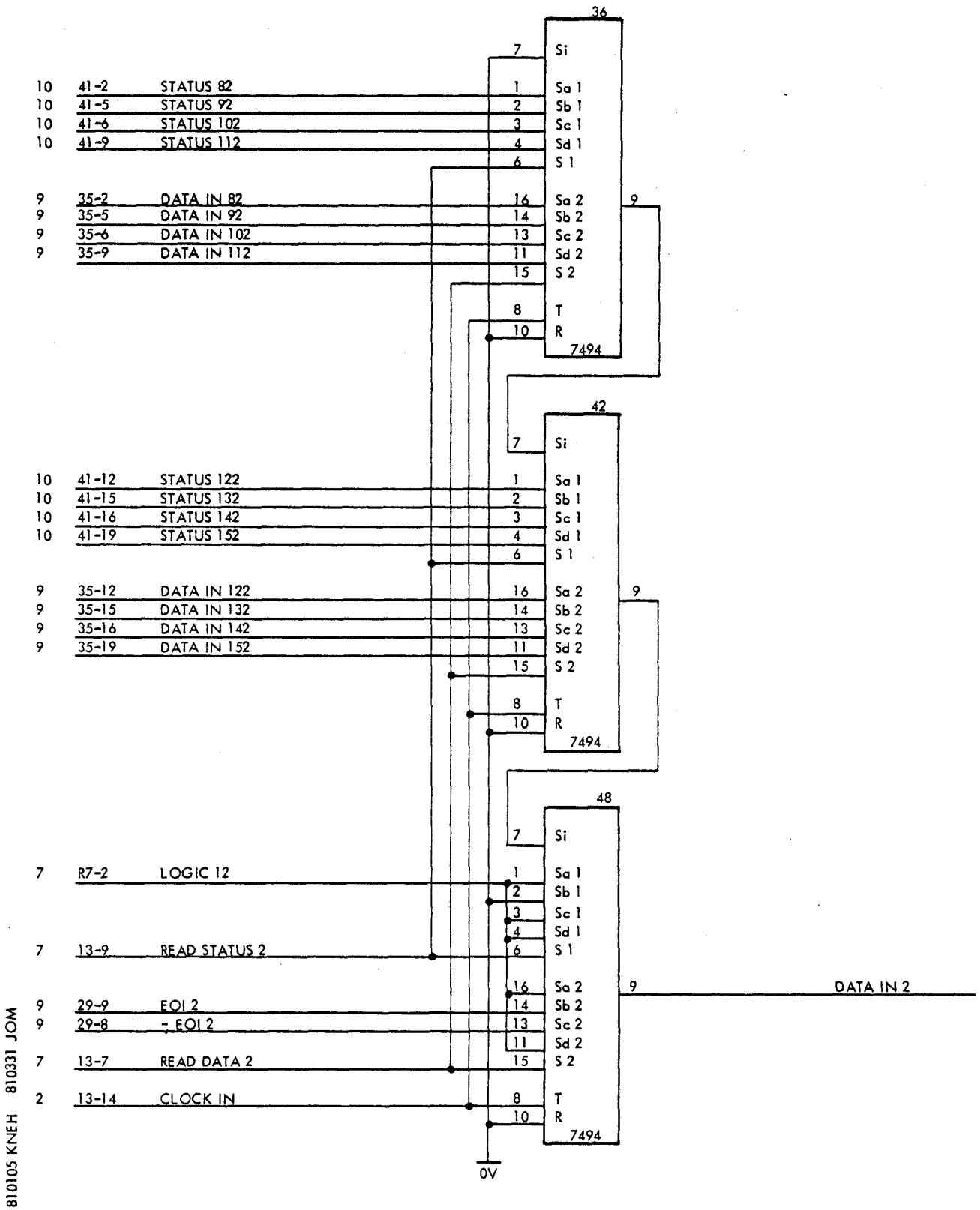
36
7 Si
10 41-2 STATUS 82 — 1 Sa 1
10 41-5 STATUS 92 — 2 Sb 1
10 41-6 STATUS 102 — 3 Sc 1
10 41-9 STATUS 112 — 4 Sd 1
6 S 1
9 35-2 DATA IN 82 — 16 Sa 2
9 35-5 DATA IN 92 — 14 Sb 2
9 35-6 DATA IN 102 — 13 Sc 2
9 35-9 DATA IN 112 — 11 Sd 2
15 S 2
8 T
10 R
7494
9
42
7 Si
10 41-12 STATUS 122 — 1 Sa 1
10 41-15 STATUS 132 — 2 Sb 1
10 41-16 STATUS 142 — 3 Sc 1
10 41-19 STATUS 152 — 4 Sd 1
6 S 1
9 35-12 DATA IN 122 — 16 Sa 2
9 35-15 DATA IN 132 — 14 Sb 2
9 35-16 DATA IN 142 — 13 Sc 2
9 35-19 DATA IN 152 — 11 Sd 2
15 S 2
8 T
10 R
7494
9
48
7 Si
7 R7-2 LOGIC 12 — 1 Sa 1
2 Sb 1
3 Sc 1
4 Sd 1
7 13-9 READ STATUS 2 — 6 S 1
16 Sa 2
9 29-9 EOI 2 — 14 Sb 2
9 29-8 - EOI 2 — 13 Sc 2
11 Sd 2
7 13-7 READ DATA 2 — 15 S 2
2 13-14 CLOCK IN — 8 T
10 R
7494
9 DATA IN 2
0V
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SIGNAL	DESTINATION	DESCRIPTION
BUS 0-7	p. 12	Z80 data bus. BUS 0 carries the LSB.
DATA IN 82-152	p. 8	Data read from the Z80 memory by DMA channel 2.
-, DRQ 3	J1	-, Dma ReQuest 3
-, END ITR 1	p. 11	Interrupt to Z80 if Termination on DMA channel 1
EOI 1	p. 8	End Of Information 2. Set -, END ITR 2. Clear'es when starting a DMA transfer from Z80.
-, EOI 1	p. 8	Same as above
-, PRESET ITR 1	p. 7	Send ITR on RC3500 channel 2

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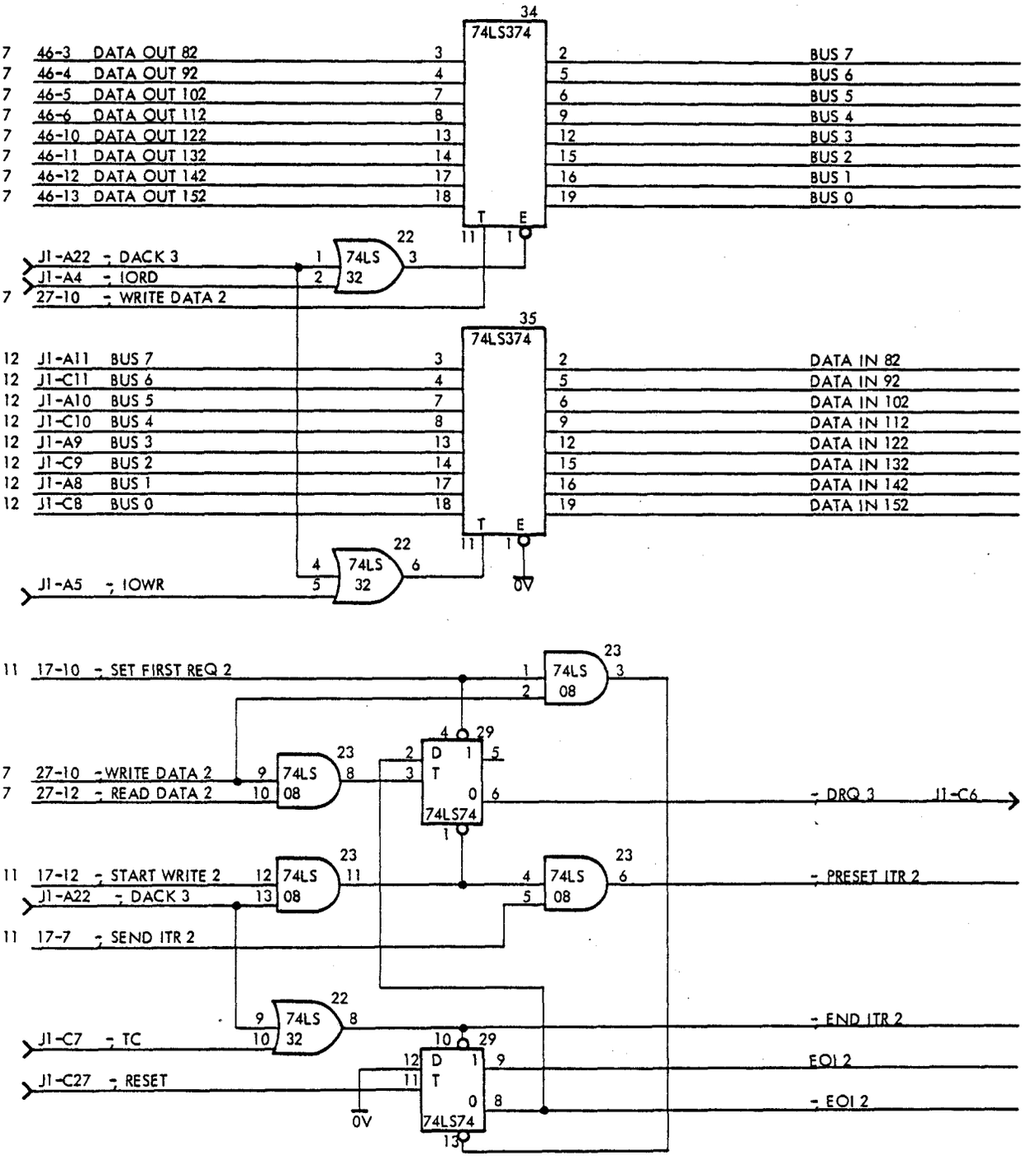

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SIGNAL	DESTINATION	DESCRIPTION
BUS 0-7	p. 12	Z80 data bus. BUS 0 is the LSB.
STATUS 82-152	p. 8	Status register output set by Z80
-, WCC ITR 2	p. 11	-, send WCC Interrupt to Z80

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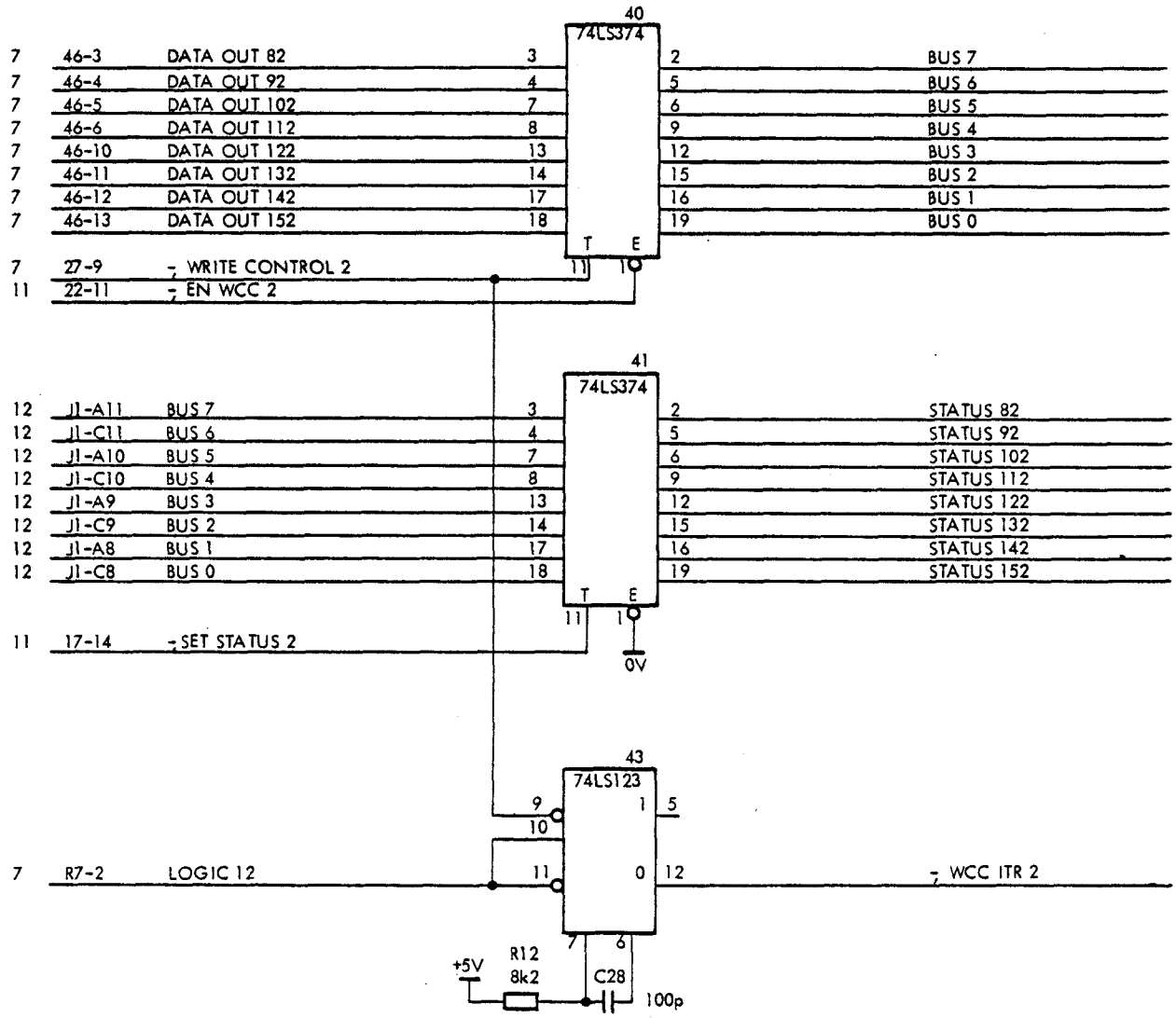

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SIGNAL	DESTINATION	DESCRIPTION
CHAIN 4	J1	Priority chain output
-, EN ITR VECTOR	p. 11	Chip Enable to Z80A-CTC
-, EN WCC 1	p. 6	-, ENable WCC register 1
-, EN WCC 2	p. 10	-, ENable WCC register 2
-, INT	J1	INTerrupt request to Z80
-, SET FIRST REQ 1	p. 5	-, SET FIRST REQuest 1
-, SET FIRST REQ 2	p. 9	-, SET FIRST REQuest 2
-, SEND ITR 1	p. 5	
-, SEND ITR 2	p. 9	
-, SET STATUS 1	p. 6	
-, SET STATUS 2	p. 10	
-, START WRITE 1	p. 5	
-, START WRITE 2	p. 9	

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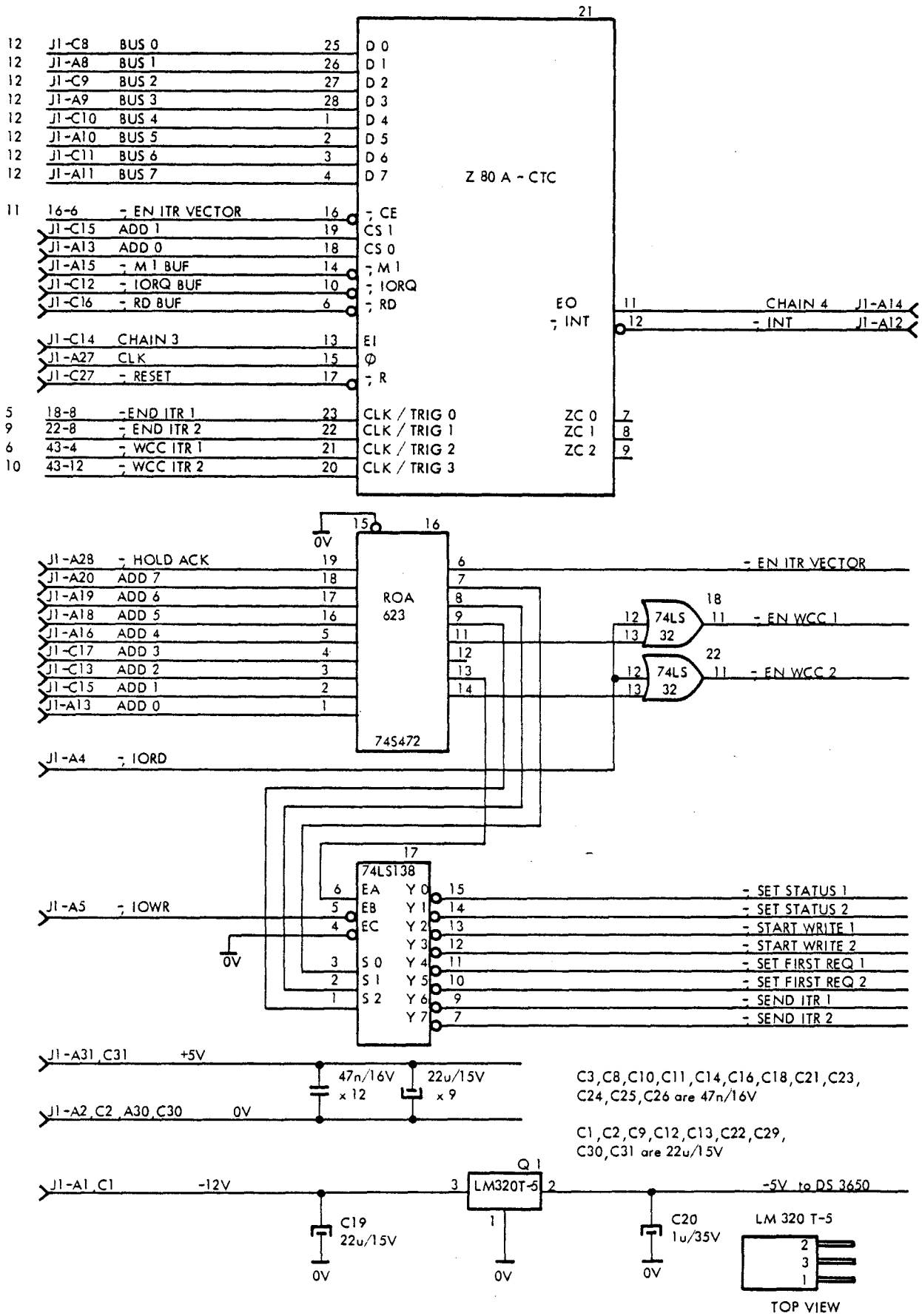

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SIGNAL	DESTINATION	DESCRIPTION
BUS 0-7	J1 p. 5 p. 6 p. 9 p. 10 p. 11	Z80 data bus

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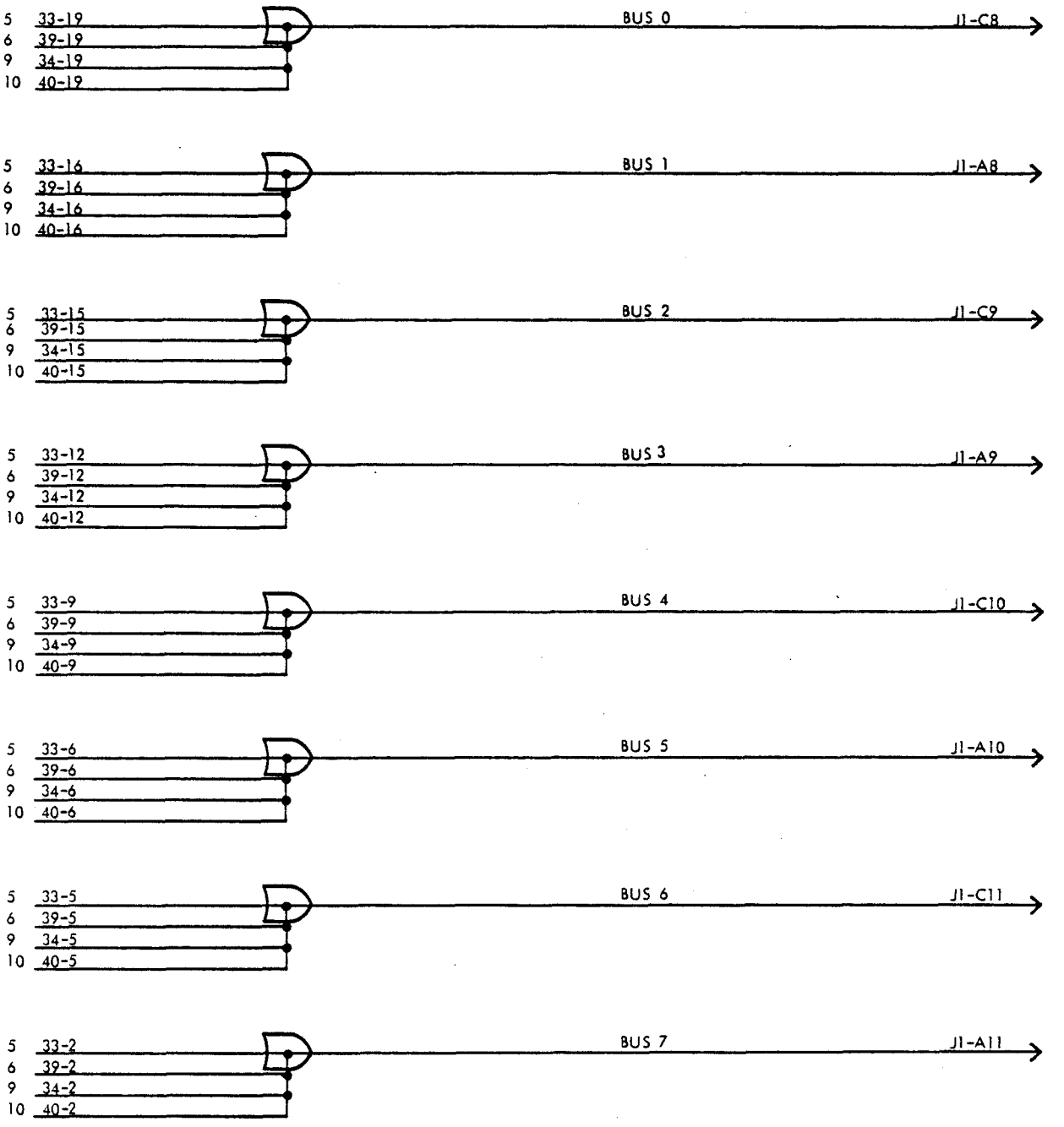

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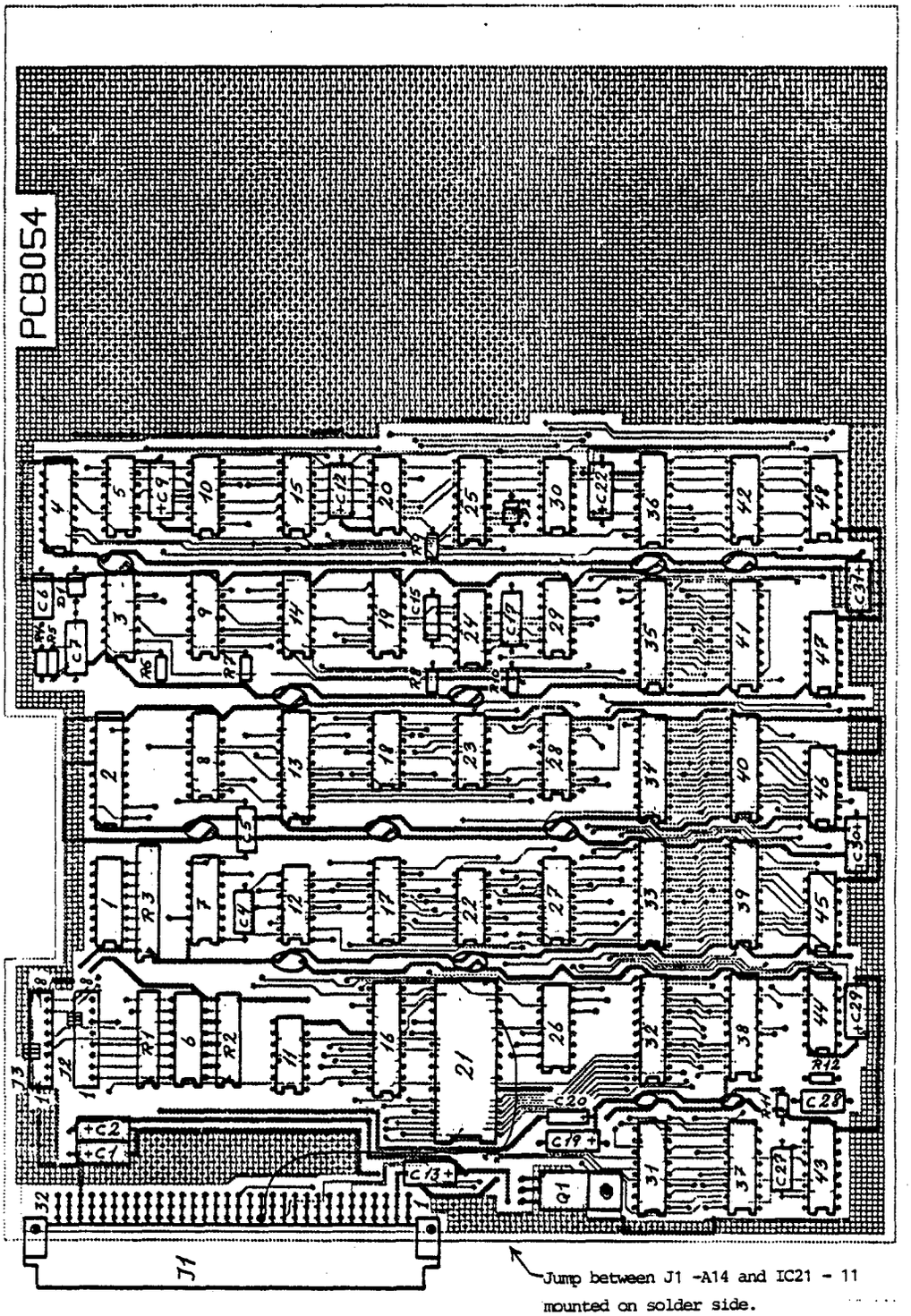

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IOM 501
A14053

PCB Assembly Drawing

CONNECTOR : J1								
PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME
A 1		- 12V	B 1			C 1		- 12V
A 2		0V	B 2			C 2		0V
A 3		-; FD REQ	B 3			C 3		-; RESET IN
A 4		-; IORD	B 4			C 4		-; EXT AEN
A 5		-; IOWR	B 5			C 5		-; EXT AD STB
A 6		-; MEM RD	B 6			C 6		-; DRQ 3
A 7		-; MEM WR	B 7			C 7		-; TC
A 8		BUS 1	B 8			C 8		BUS 0
A 9		BUS 3	B 9			C 9		BUS 2
A10		BUS 5	B10			C10		BUS 4
A11		BUS 7	B11			C11		BUS 6
A12		-; INT	B12			C12		-; IORQ BUF
A13		ADD 0	B13			C13		ADD 2
A14		CHAIN 4	B14			C14		CHAIN 3
A15		-; M1 BUF	B15			C15		ADD 1
A16		ADD 4	B16			C16		-; RD BUF
A17		-; WAIT	B17			C17		ADD 3
A18		ADD 5	B18			C18		ADD 15
A19		ADD 6	B19			C19		ADD 14
A20		ADD 7	B20			C20		ADD 13
A21		-; DACK 1	B21			C21		ADD 12
A22		-; DACK 3	B22			C22		ADD 11
A23		-; DRQ 1	B23			C23		ADD 10
A24		-; WRBUF	B24			C24		ADD 9
A25		-; MREQ BUF	B25			C25		ADD 8
A26		-; RFSH BUF	B26			C26		-; NMI
A27		CLK	B27			C27		-; RESET
A28		-; HOLD ACK	B28			C28		-; HALT BUF
A29		-; HOLD	B29			C29		9.8304 MHZ
A30		0V	B30			C30		0V
A31		+ 5V	B31			C31		+ 5V
A32		+ 12V	B32			C32		+ 12V

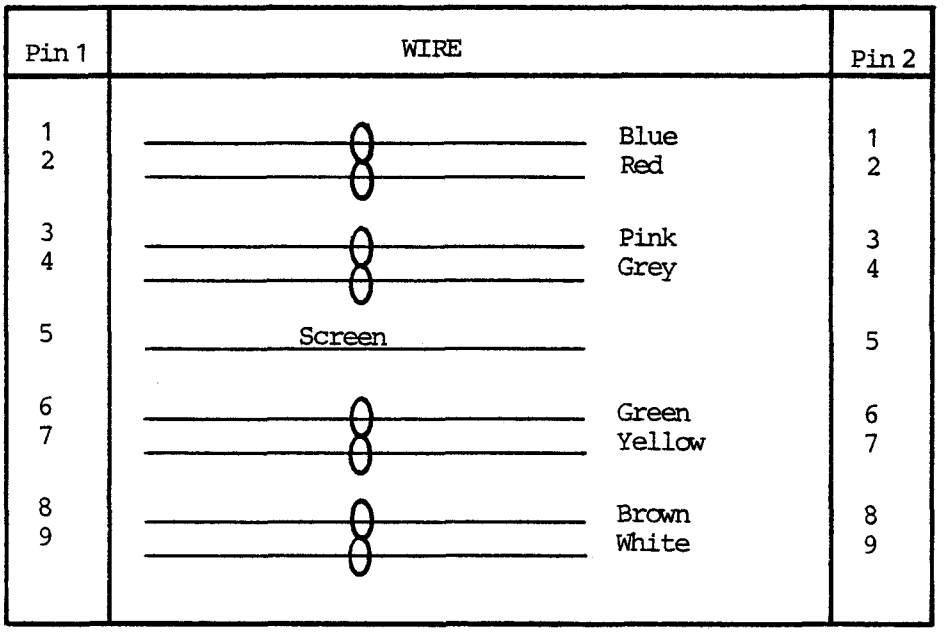
J2		
PIN	GEN. ADR.	SIGNAL NAME
1		DATA OUT A1
2		DATA OUT B1
3		CLOCK OUT A1
4		CLOCK OUT B1
5		CLOCK IN B1
6		CLOCK IN A1
7		DATA IN B1
8		DATA IN A1

J3		
PIN	GEN. ADR.	SIGNAL NAME
1		DATA OUT A2
2		DATA OUT B2
3		CLOCK OUT A2
4		CLOCK OUT B2
5		CLOCK IN B2
6		CLOCK IN A2
7		DATA IN B2
8		DATA IN A2

CONNECTOR 1: Cannon Plug DEC-9P

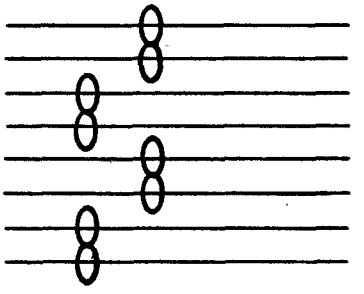
CONNECTOR 2: Cannon Plug DEC-9P

CABLE: 6 x 2 x 0.25 mm CY Coferro

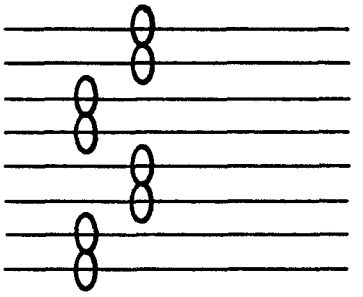


Cable List, CBL466

P2	WIRE	CHAN1
1	DATA OUT A1	8
2	DATA OUT B1	9
3	CLOCK OUT A1	6
4	CLOCK OUT B1	7
5	CLOCK IN B1	2
6	CLOCK IN A1	1
7	DATA IN B1	4
8	DATA IN A1	3



P3	WIRE	CHAN1
1	DATA OUT A1	8
2	DATA OUT B1	9
3	CLOCK OUT A1	6
4	CLOCK OUT B1	7
5	CLOCK IN B1	2
6	CLOCK IN A1	1
7	DATA IN B1	4
8	DATA IN A1	3



Cable List, CBL681

RETURN LETTER

Title: Technical Description for IOM501 RCSL No.: 52-AA1044

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