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IML501
Technical Description

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Keywords:

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Abstract:

This publication is a technical description of an Image Load Module designed for the RC850 display unit.

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1. DESCRIPTION 1.

The IMage Load module is built around an EPROM array consisting of 16 UV erasable, electrical programmable read only memories, each consisting of 4096 bytes. The total capacity becomes 65536 bytes, each consisting of 8 bits.

The IML module is intended for use in the RC855 stand-alone Display Unit. In the stand-alone version there are no down-load possibilities from external sources (e.g. floppy-disc or transmission lines), instead the IML module is used. During power-up software in the IML module is moved to the ram-memory by means of a bootstrap loader located in MIC504.

The EPROM's located on the IML module may be programmed while located on the printed circuit board, if an external programming voltage is connected to JACK 2.

The EPROM module connects to MIC504 via JACK 1.

2. SPECIFICATIONS

2.1 Performance Specifications

EPROM TYPE : Ultraviolet light erasable, electrically programmable read-only memories, with a capacity of 4K x 8 bits. INTEL 2732/2732A or TEXAS 2532 are recommended.

BYTE LENGTH : 8 bits.

CAPACITY : 65536 bytes.

READ ACCESS TIME : Read access time measured from leading edge of the -, IORD pulse to valid data on BUS 0:7, typ. 60 nS.

EPROM data addressed are latched in output register at the leading edge of -, IORD, and approx. 100-150 nS. later the address counter is incremented to next address.

WRITE TIME : Write time measured from leading edge of -, IOWR pulse to next DMA request, approx. 53.5 mS.

Write data are stored in input register at the trailing edge of -, IOWR and the programming timer is started. Approx. 53.5 mS. later the address counter is incremented and a new DMA request issued.

TRANSFER MODE : Initialization and start are executed by means of standard I/O instructions:

out 39_H = set address counter low byte (LS byte)

out 38_H = set address counter high byte (MS byte), and reset IML501

out $3A_H$ = start DMA channel 1 transfer

Data transfer is executed by means of DMA transfers via the DMA controller. Single transfer mode is used.

OPERATIONAL MODES : Read/verify/write.

PROGRAMMING TIME : Programming time for the entire array is approx. 60 minutes.

2.2 Electrical Specifications 2.2

SUPPLY VOLTAGE : + 5V DC $\pm$ 5%/1A

EXTERNAL PROGRAMMING VOLTAGE : 26V $\pm$ 0V5/200mA for INTEL 2732 or TEXAS 2532

22V $\pm$ 0V2/200mA for INTEL 2732A

2.3 Environmental Specifications 2.3

AMBIENT TEMPERATURE : 10-35^{o}C

RELATIVE HUMIDITY : 20-80% (non-condensing)

3. INSTALLATION 3.

3.1 Installation of the Module 3.1

The EPROM module is installed in the RC850 display unit in the interface position, which is the position nearest the picture-tube.

CAUTION: THE PCB BOARD MUST NEITHER BE REMOVED FROM NOR INSERTED IN THE INTERFACE POSITION WHILE + 5V DC VOLTAGE OR EXTERNAL PROGRAMMING VOLTAGE ARE PRESENT.

INSTALLATION OF THE MODULE OR PROGRAMMING OF THE EPROM'S MUST ONLY TAKE PLACE UNDER THE ASSISTANCE OF AUTHORIZED SERVICE PERSONNEL, SINCE REMOVAL OF DISPLAY UNIT COVER IS REQUIRED.

3.2 Installation of the EPROM's 3.2

EPROM type TEXAS 2532, INTEL 2732/2732A or equivalent types may be mounted in 16 24-pins sockets (see fig. 3.1). Be careful not to bend EPROM pins while mounting the EPROM's. The EPROM types must never be mixed. Mount either 16 x 2532, or 16 x 2732, or 16 x 2732A.

3.3 Strapping Possibilities 3.3

EPROM module is designed to use three types of EPROM's: INTEL 2732/2732A - TEXAS 2532 or equivalent. INTEL and TEXAS EPROM's are, however, not completely compatible, so 5 strap positions have been introduced, Pos. 25, Pos. 26, Pos. 27, Pos. 28, and Pos. 29.

Strapping is executed by means of three strapplatforms and two IC's (74LS138), which are mounted as indicated in fig. 3.2. Refer also to fig.3.1.

To change strapping from INTEL 2732/2732A to TEXAS 2532 or vice versa, do as follows:

1. Turn the 16-pins strapplatform B in position 29, 180 degrees.

2. Interchange strapplatforms A by IC's 74LS138.

CAUTION: IT IS EMPHASIZED THAT DAMAGE OCCURS TO THE EPROM'S AND THE IC'S 74LS138 IF THE STRAPPING DOES NOT CORRESPOND TO THE EPROM'S USED.

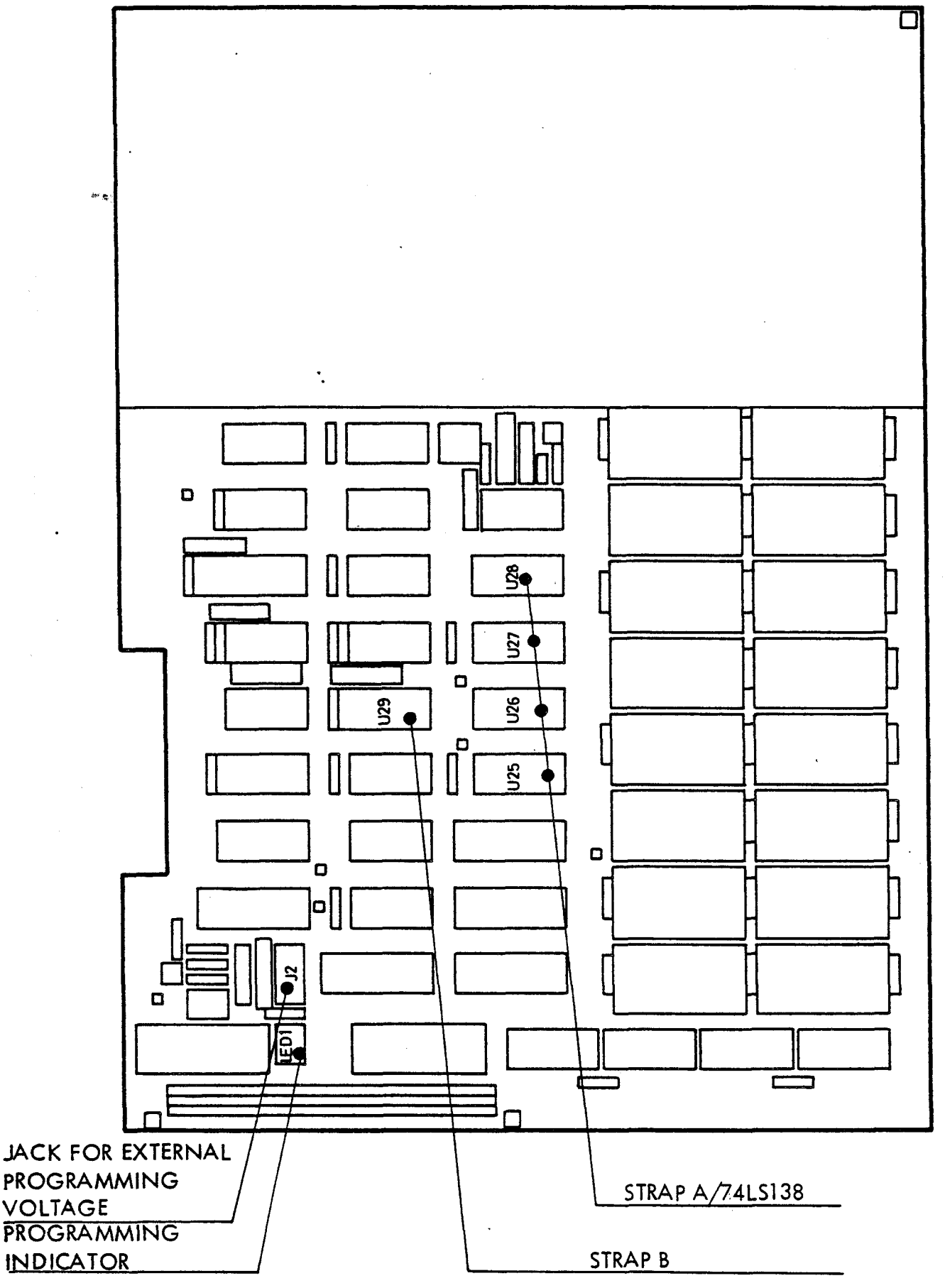


Fig. 3.1
IML501 LAYOUT

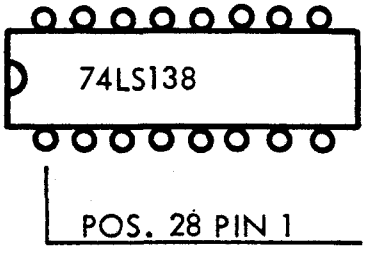
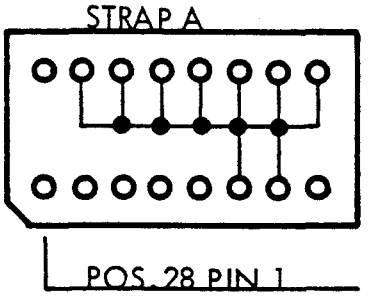
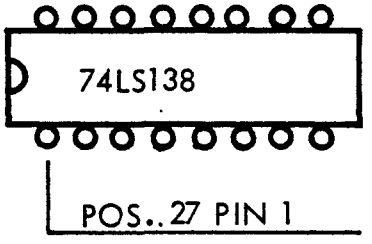
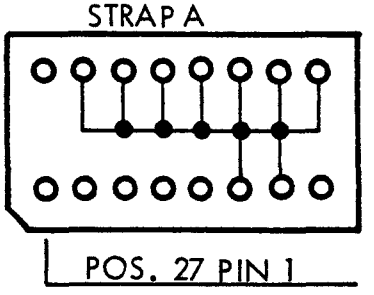
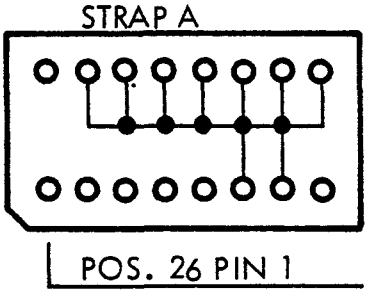
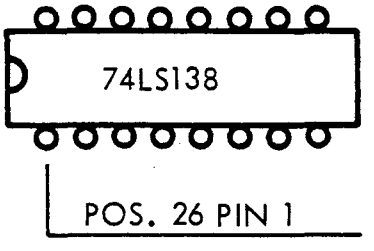
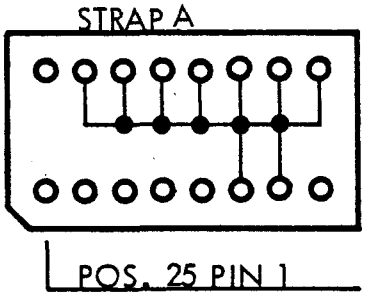
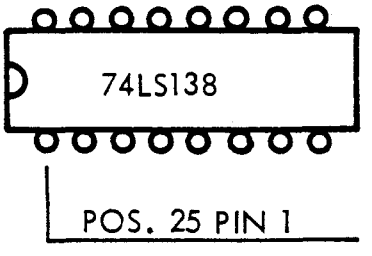
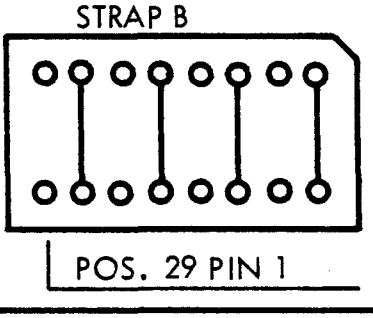
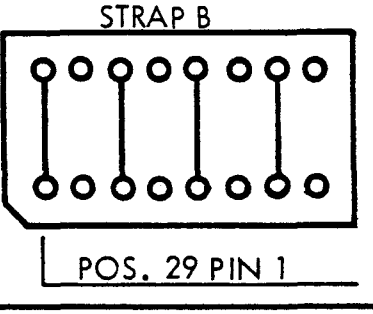
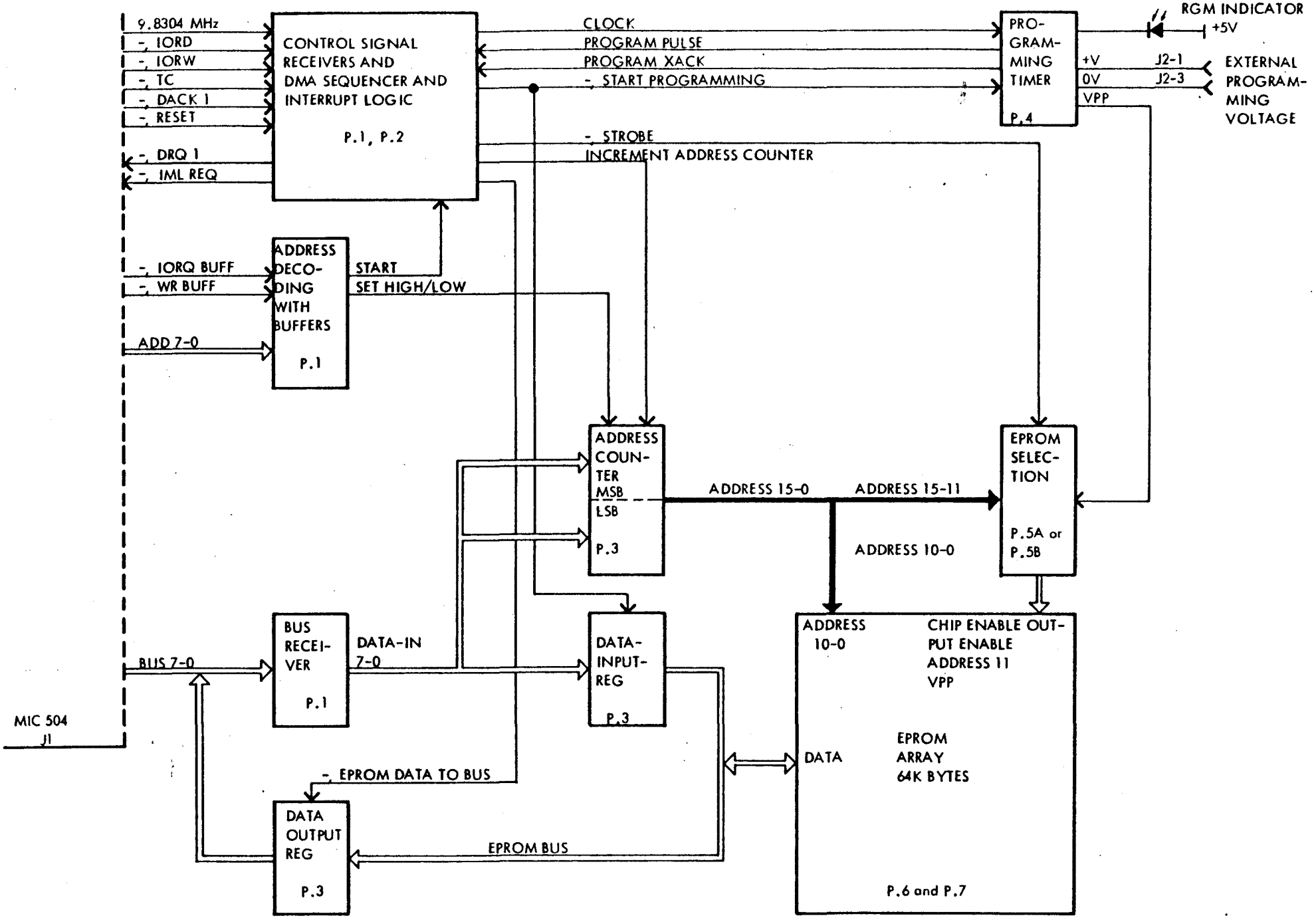
STRAP POSITION	PROGRAM, VERIFY AND READ 2532	PROGRAM, VERIFY AND READ 2732/2732A
28		
27		
26		
25		
29		

Fig. 3.2
IML501 STRAPS

4. BLOCK DIAGRAM 4.

The major functional blocks of the EPROM module appear on the block diagram. The numbers in the blocks refer to logic diagram numbers.



BLOCK DIAGRAM

5. TIMING DIAGRAMS 5.

Timing diagram 1 shows standard I/O transfer timing. Timing diagram 2 shows DMA transfer from IML501 to ram-memory, and timing diagram 3 shows DMA transfer from ram-memory to IML501 (programming timing).

AT CPU Z80A INPUTS/OUTPUTS

CLK (Φ)

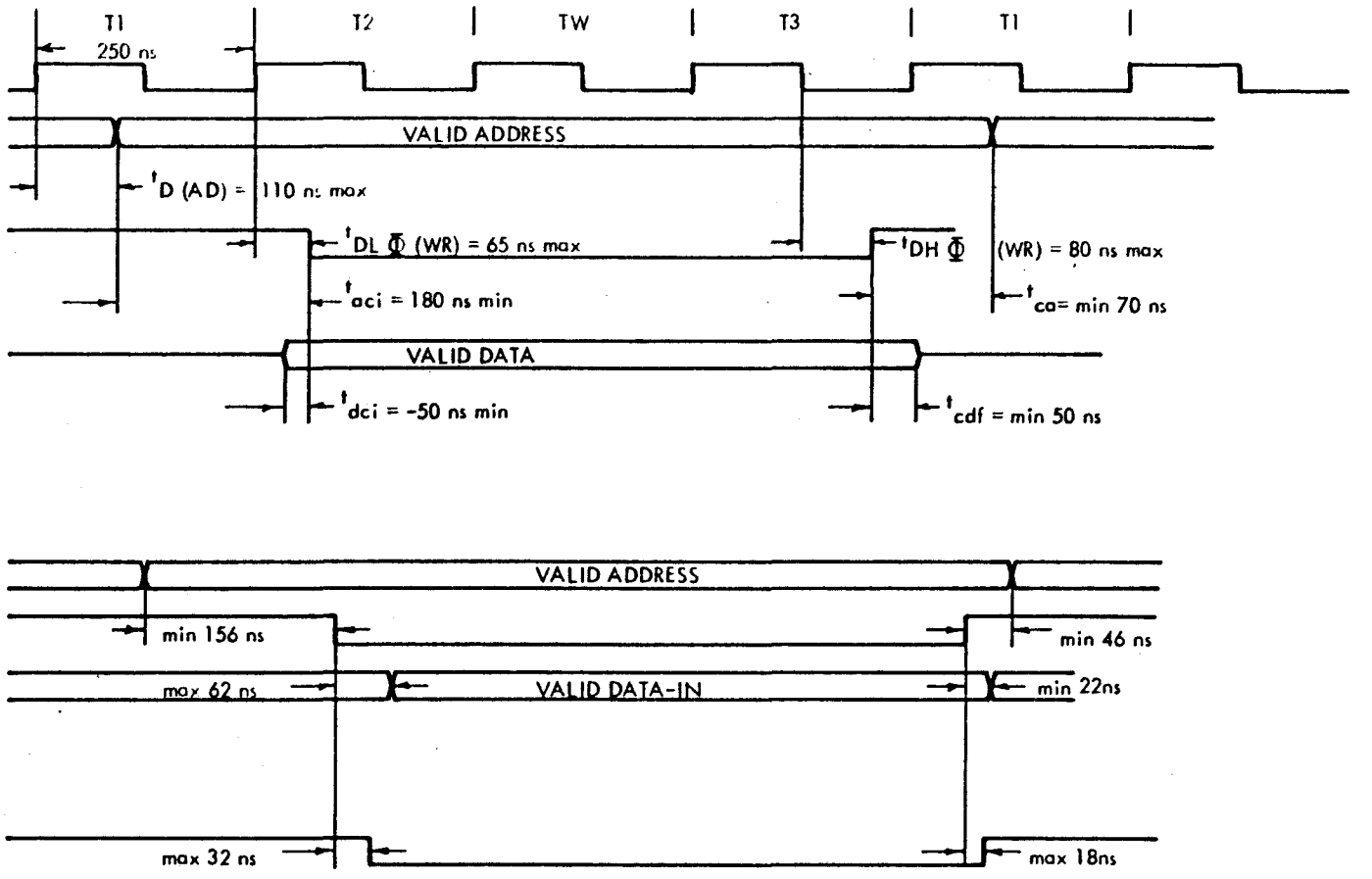
CPU ADD 15:0

-, WR

D7:0

AFTER IML 501 RECEIVERS

ADD 7:0	1	
-, WRITE ADDRESS	1	
DATA-IN 7:0	1	
-, SET HIGH BYTE	1	5-15
or		
-, SET LOW BYTE	1	5-14
or		
-, START	1	5-13

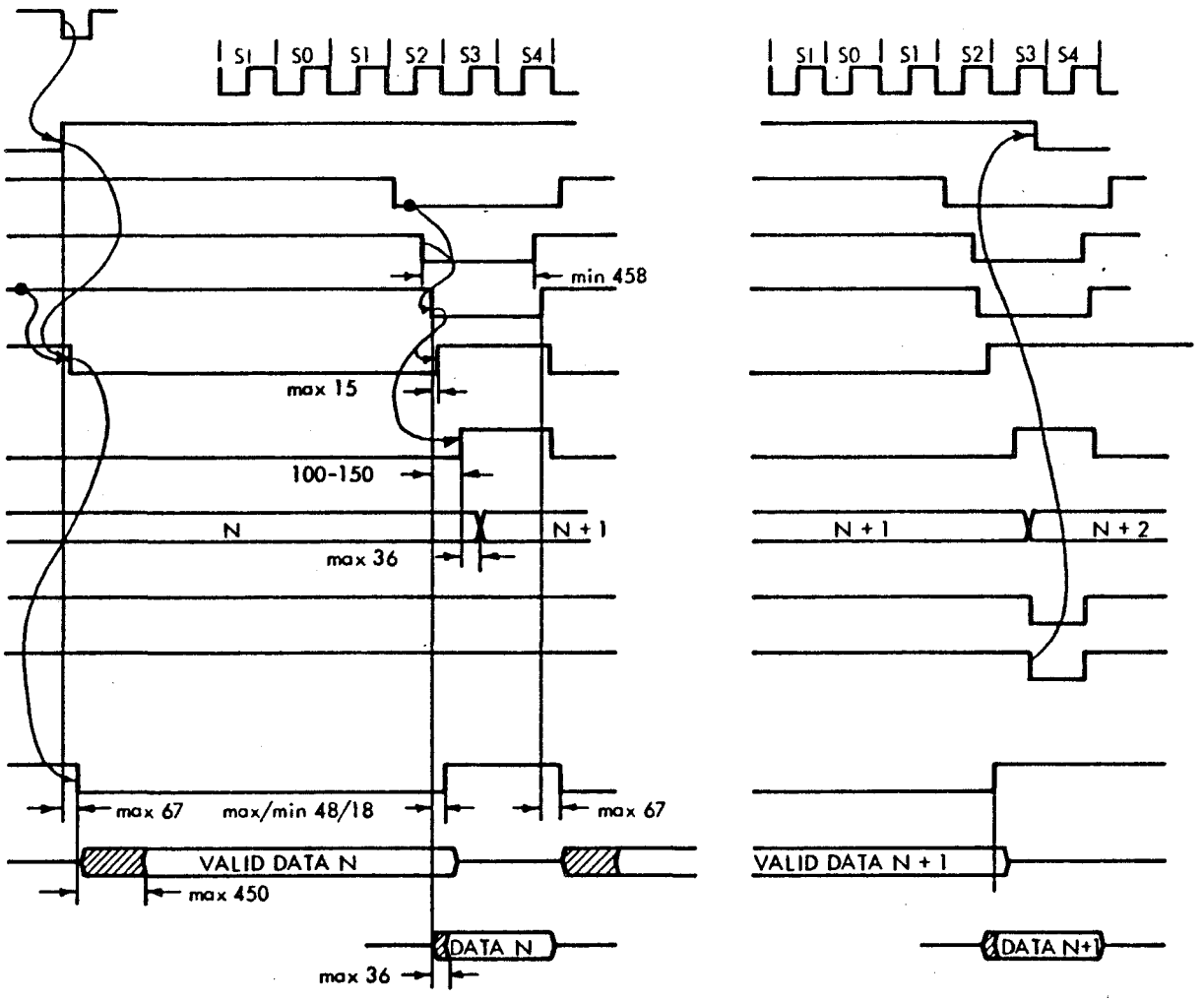


Note: Timing not shown to scale

	81.09.09 VH	81.09.09 ABP
-, START	1	5-13
DMA CLK		
DMA REQ 1	2	6-5
-, DMA ACK 1	1	2-12
-, READ DATA	1	2-14
-, EPROM DATA TO BUS	3	8-11
-, STROBE	2	19-3
INCREMENT ADDRESS COUNTER	2	9-8
ADDRESS COUNTER	3	
-, TERMINAL COUNT	1	2-5
-, READ ITR	2	8-3
-, CE/A11 0-15 or	5A	
VPP/-, STROBE 0-15	5B	
EPROM BUS 7:0	3	
BUS 7:0	3	

READ TIMING DMA WRITE TRANSFERS
TRANSFER OF TWO BYTES SHOWN

Timing Diagram.

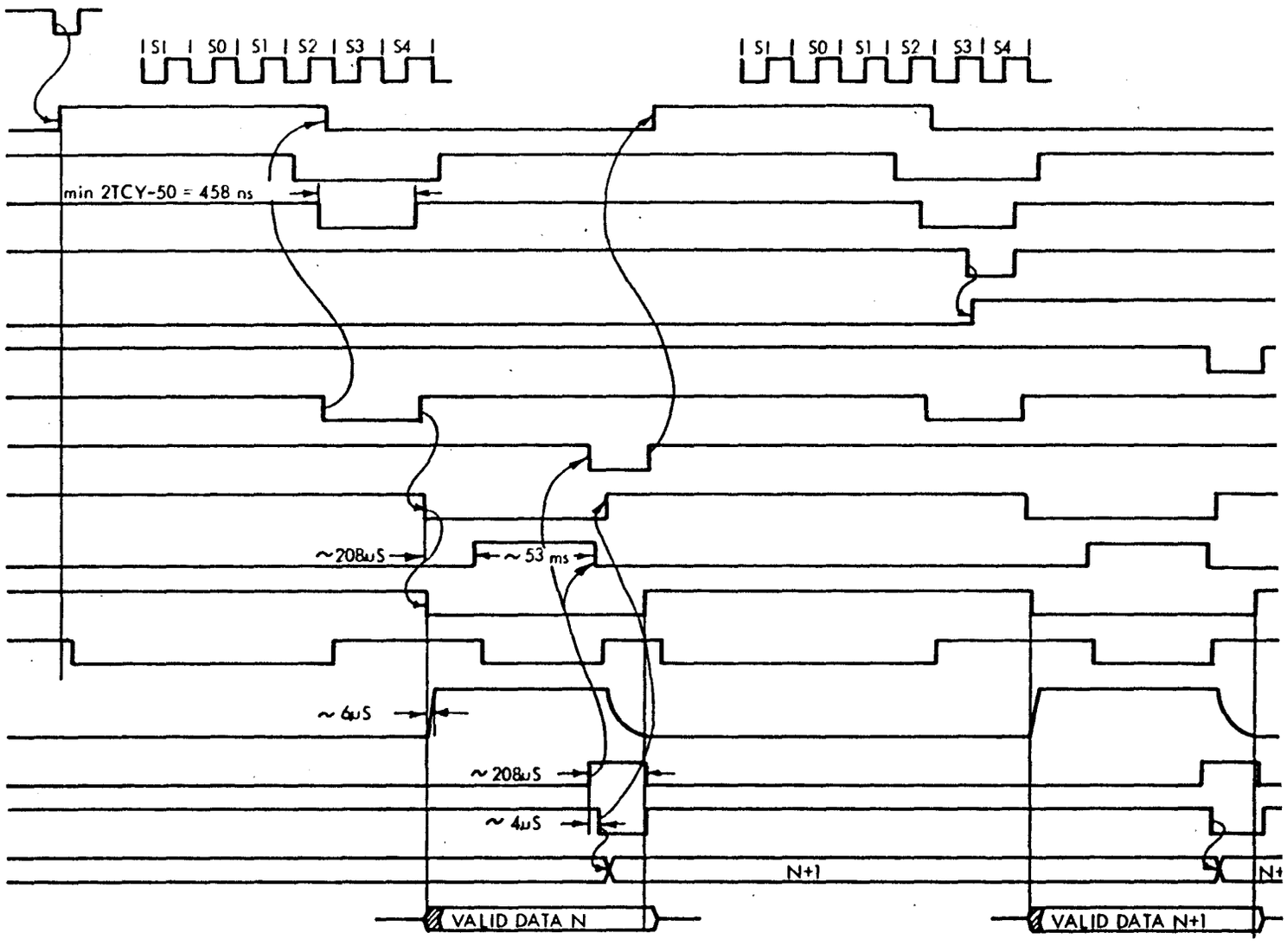


From -, IORD leading edge to data on bus max 76 ns
From -, IORD leading edge to -, CAS (for RAM) min 150 ns

Note: Timing not shown to scale
All time values in ns
No wait states are drawn

-, START	1	5-13
DMA CLK		
DMA REQ 1	2	6-5
-, DMA ACK 1	1	2-12
-, WRITE DATA	1	2-7
-, TERMINAL COUNT	1	2-5
ENABLE WRITE ITR	2	6-9
-, INTERRUPT	2	7-8
-, START PROGRAMMING	3	8-8
-, SET DMA REQUEST	2	9-6
-, VPP ON	4	18-6
PROGRAM PULSE	4	21-1
RESET TIMER	4	19-8
-, STROBE	2	19-3
VPP	4	TR1
PROGRAM XACK	4	24-8
-, DELAY'D PROGRAM XACK	4	11-6
ADDRESS COUNTER	3	
EPROM BUS	3	

WRITE TIMING ~ DMA READ TRANSFERS
TRANSFER OF TWO BYTES SHOWN
Timing Diagram



Note: Timing not shown to scale.
No wait states are drawn

6. FUNCTIONAL DESCRIPTION 6.

The functional description will refer to block diagram, timing diagrams, and logic diagrams using the abbreviations BD, TD, and LD.

6.1 EPROM Module Operation 6.1

Initialization
Read EPROM's
Program EPROM's

6.1.1 Initialization (TD1) 6.1.1

Since IML501 uses DMA-transfers via channel 1 of the DMA controller and generates interrupts via the CTC controller channel 3, these two devices must be initialized. Refer to DMA use and CTU use in IML501 REFERENCE MANUAL [1].

IML is set up and started by means of three standard I/O output instructions:

out <39_H> This instruction loads IML501 address counter least significant byte with information from BUS (7:0). Bit 7 is the most significant bit.

out <38_H> This instruction terminates all IML501 activity and places IML501 in a well defined state. Besides this the IML501 address counter most significant byte is loaded with the information from BUS (7:0). Bit 7 is the most significant bit.

out <$3A_H$> This instruction starts DMA-transfer via DMA controller channel 1.

6.1.2 Read from EPROM Memory (TD2) 6.1.2

When the software has initialized the DMA controller for write transfer and started IML501, the transfer of information to the ram-memory takes place without the engagement of the Z80-processor. The transfer continues until DMA byte count is zero; at this time the Z80 software is interrupted via CTC channel 3. The DMA is used in Single Transfer Mode, which will ensure one full machine cycle execution between DMA transfers.

The out $<39_H>$, out $<38_H>$ instructions load IML501 address counter with the start address. The out $<3A_H>$ instruction sets the DMA request FF, which causes the addressed EPROM to be selected and the information to be supplied to the inputs of the data-out register. Upon the arrival of the -, DACK 1 and -, IORD signals from the DMA controller the following sequence of events takes place:

- EPROM data are latched in the data out register. Latching occur as long as the -, EPROM DATA TO BUS signal is at low level.

- Contents of data-out register are gated to BUS (7:0) while the -, EPROM DATA TO BUS signal is at low level.

- EPROM array is deselected while the -, EPROM DATA TO BUS signal is at low level.

- Address counter is incremented by 1 approx. 100 nS. after the leading edge of the -, EPROM DATA TO BUS signal, and at the trailing edge of the signal the addressed EPROM becomes selected.

The above mentioned sequence is repeated for every byte transferred to ram-memory. The DMA request FF remains set until reset

by the TERMINAL COUNT pulse from the DMA controller. This pulse is generated when the current byte count register, associated with DMA channel 1, goes to zero. The TERMINAL COUNT pulse causes an interrupt signal to be generated.

6.1.3 Program EPROM Memory (TD3)

6.1.3

During programming of EPROM's all DMA transfers to/from IML501 are usually one byte transfer, since a verification immediately follows the programming of one EPROM cell. The recommended programming procedure is described in the IML501 REFERENCE MANUAL [1].

When the software has initialized the DMA controller for read transfer and started IML501, the transfer of information and the programming of the addressed EPROM cell takes place without the engagement of the Z80 processor. Although it is not recommended, EPROM cells may be programmed without verification cycles in between. The transfer of information and the programming do always continue until DMA byte count is zero. An interrupt is sent to the software via CTC channel 3, when the last byte has been programmed.

The out $<39_H>$, out $<38_H>$ instructions load IML501 address counter with the start address. The out $<3A_H>$ instruction sets the DMA request FF. Upon the arrival of the -, DACK 1 and -, IOWR signals from the DMA controller the following sequence of events takes place:

- DMA request FF is reset at the leading edge of -, START PROGRAMMING signal, which is the "and" of -, DACK 1 and -, IOWR.

- Data on BUS (7:0) is loaded into the input register by the trailing edge of the -, START PROGRAMMING signal.

- The programming voltage is switched on.

- The contents of the input register is gated to the inputs of the EPROM array, and the programming timer is started.

- After a delay of approx. 208 uS. a 53.1 mS. wide programming pulse is generated, and the information held in the input register is programmed into the addressed EPROM cell.

- Approx. 4 uS. after the trailing edge of programming pulse the programming voltage is switched off and the address counter is incremented by 1.

- Approx. 208 uS. after the trailing edge of the programming pulse a new DMA-request is issued.

The above mentioned sequence is repeated for every byte programmed, however, when DMA-byte count becomes zero the TERMINAL COUNT pulse will prevent further DMA requests. Instead of a new DMA-request an interrupt pulse is generated when the last byte has been programmed.

6.2 Timing Generators 6.2

6.2.1 Read Timing (TD2, LD2, LD3) 6.2.1

No read access delay exists. The EPROM's are accessed between the DMA cycles. This gives sufficient time for the addressed EPROM data to settle before the data is latched in the output register.

The first byte to be read is gated to the inputs of the data out register when the START pulse sets the DMA-request FF.

The response to the DMA-request is the -, DACK 1 and -, IORD signals by means of which the -, EPROM DATA TO BUS signal is generated. This signal latches the addressed EPROM information in the output register, strobes this information to BUS (7:0) and disables the EPROM array while the address counter is incremented. When the -, EPROM DATA TO BUS signal changes from low to high the EPROM array becomes enabled again, allowing the contents of the addressed EPROM cell to appear at the input lines of the data out register.

6.2.2 Programming Timer (TD3, LD4)

The programming timer is used during programming of the EPROM's. The timing sequence is initiated when the -, START PROGRAMMING signal changes from low to high level. At this time, the programming voltage (VPP) is applied to the EPROM array via the transistor switch, and simultaneously a 20-bits counter is allowed to count as the RESET TIMER signal changes to low level. The counter is incremented by one every 101.7 nS. Approx. 208 uS. after the release of the counter a 53.1 mS. wide PROGRAM PULSE is generated. This pulse causes data present in the input register to be programmed into the addressed EPROM location. The programming voltage is switched off at the trailing edge of the PROGRAM pulse and simultaneously the EPROM array is disabled while the address counter is incremented. After further 208 uS. of time the timing counter is reset, which terminates the write timing sequence.

6.3 Address Path (BD, LD3, LD5, LD6, LD7)

As mentioned in section 6.1.1 the address counter is loaded by means of the out $<39_H>$, out $<38_H>$ instructions.

ADDRESS bits 15:12 from the address counter are connected to the EPROM selection circuits to select one EPROM out of 16.

ADDRESS bits 11:0 are connected to the address inputs of the EPROM's to select one EPROM location out of 4096 locations. Notice that ADDRESS bit 11 passes strap platforms, which takes into account the pin incompatibility of the 2532 and the 2732/ 2732A EPROM's.

6.4 Data Path (BD, LD1, LD3, LD6, LD7) 6.4

The BUS (7:0) receiver is a 74LS244 octal line receiver. After the receiver the data lines are named DATA-IN (7:0), and these lines are connected to the input of the address counter and the data input register. The EPROM bus connects the bidirectional information lines from the EPROM array with the outputs of the data in register and the inputs of the data out register. Data stored in the addressed EPROM location are sent via the EPROM bus to the data out register during DMA write transfers. Data held in the input register are sent via the EPROM bus to the addressed EPROM location during DMA read transfers (programming of EPROM's).

6.5 Programming Mode Indicator (LD2, LD4) 6.5

To be able to monitor the programming of the EPROM's, IML501 is equipped with a programming mode indicator, which turns on when the external programming voltage is connected to JACK 2.

The PGM indicator gleams synchronously with the PROGRAM PULSE when programming the EPROM's. By means of a toggle FF every second PROGRAM PULSE produces a flash.

6.6 EPROM Array (LD6, LD7)

6.6

The EPROM's in the array may be TEXAS 2532, INTEL 2732/2732A, or PROM's which are equivalent to these types.

CAUTION: THE EPROM TYPES ON THE PCB MUST NEVER BE MIXED. MOUNT EITHER 16 x 2532 OR 16 x 2732 OR 16 x 2732A.

NOTICE THAT EXTERNAL PROGRAMMING VOLTAGE FOR 2732A IS ONLY 22V.

EXTERNAL PROGRAMMING VOLTAGE FOR 2532 and 2732 is 26V.

SIGNAL	DESTINATION	DESCRIPTION
-, SET HIGH BYTE	p. 2 p. 3	Generated during the out <38_H> instruction to terminate all IML501 activity and place the logic in a well defined state. Besides this the most significant byte of the address counter is loaded with information from BUS (7:0).
-, SET LOW BYTE	p. 3	Generated during the out <39_H> instruction to load the least significant byte of the address counter with information from BUS (7:0).
-, START	p. 2	Generated during the out <$3A_H$> instruction to start DMA transfers between IML501 and display unit RAM memory.
-, READ DATA	p. 3	Buffered -, IORD pulse used to access IML501 EPROM data during a DMA write transfer.
-, DMA ACK 1	p. 3	Buffered -, DACK 1 pulse used to notify IML501 when it has been granted a DMA cycle.
-, RESET IML 501	p. 2	Buffered -, RESET signal, which is generated during power-up. The signal places the logic of IML501 in a well defined state.
-, WRITE DATA	p. 3	Buffered -, IOWR signal used to load data into IML501 data-in register during DMA read transfer.
-, TERMINAL COUNT	p. 2	Buffered -, TC signal used to notify IML501 when DMA byte count has reached zero.
-, IML REQ	J1-A3	Buffered interrupt request from IML501. Refer to -, INTERRUPT signal on page 2.
DATA IN 7:0	p. 3	Data/start address received from BUS (7:0) via bus receivers.

Designed by

Drawn by

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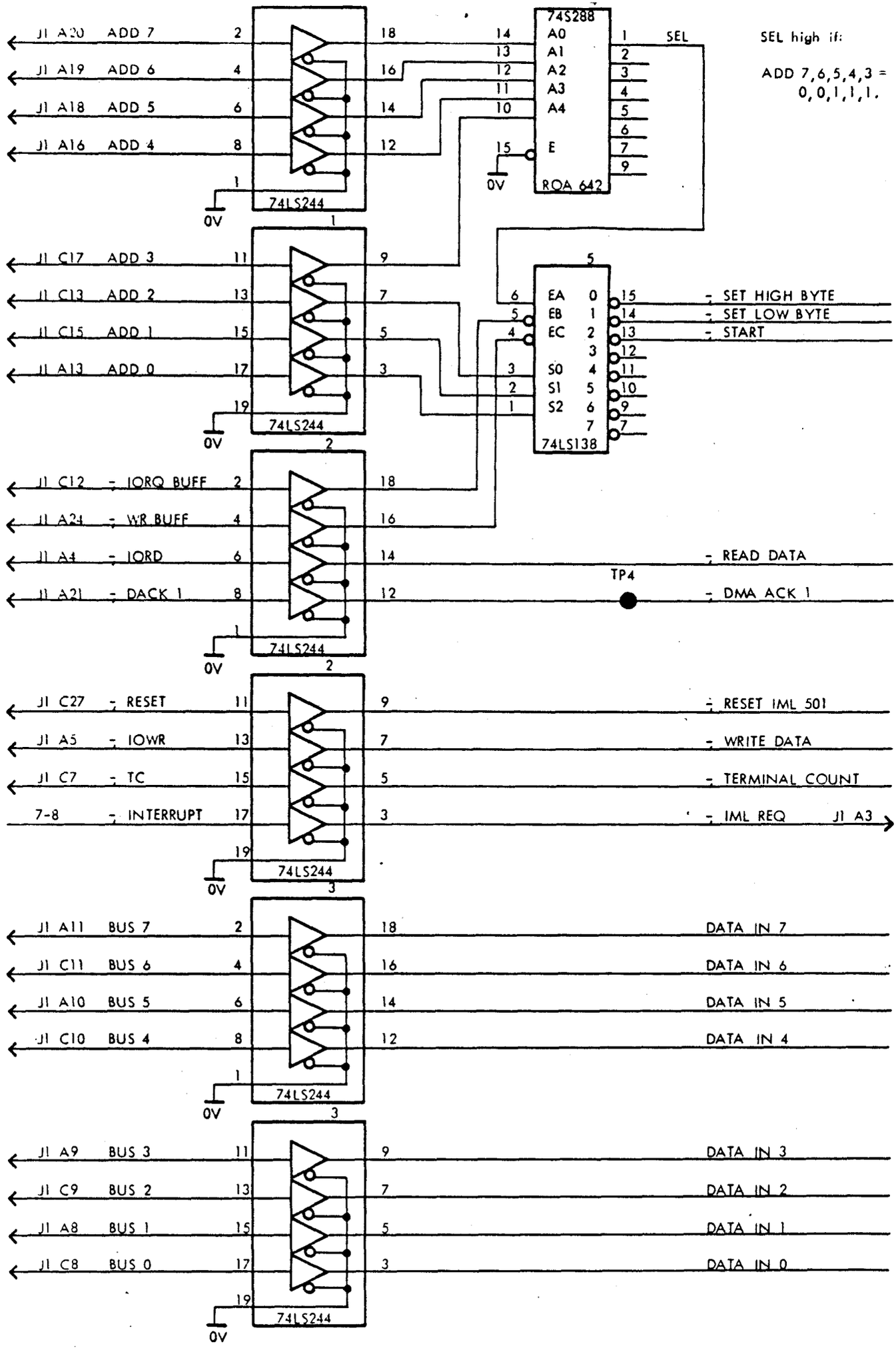

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IML 501

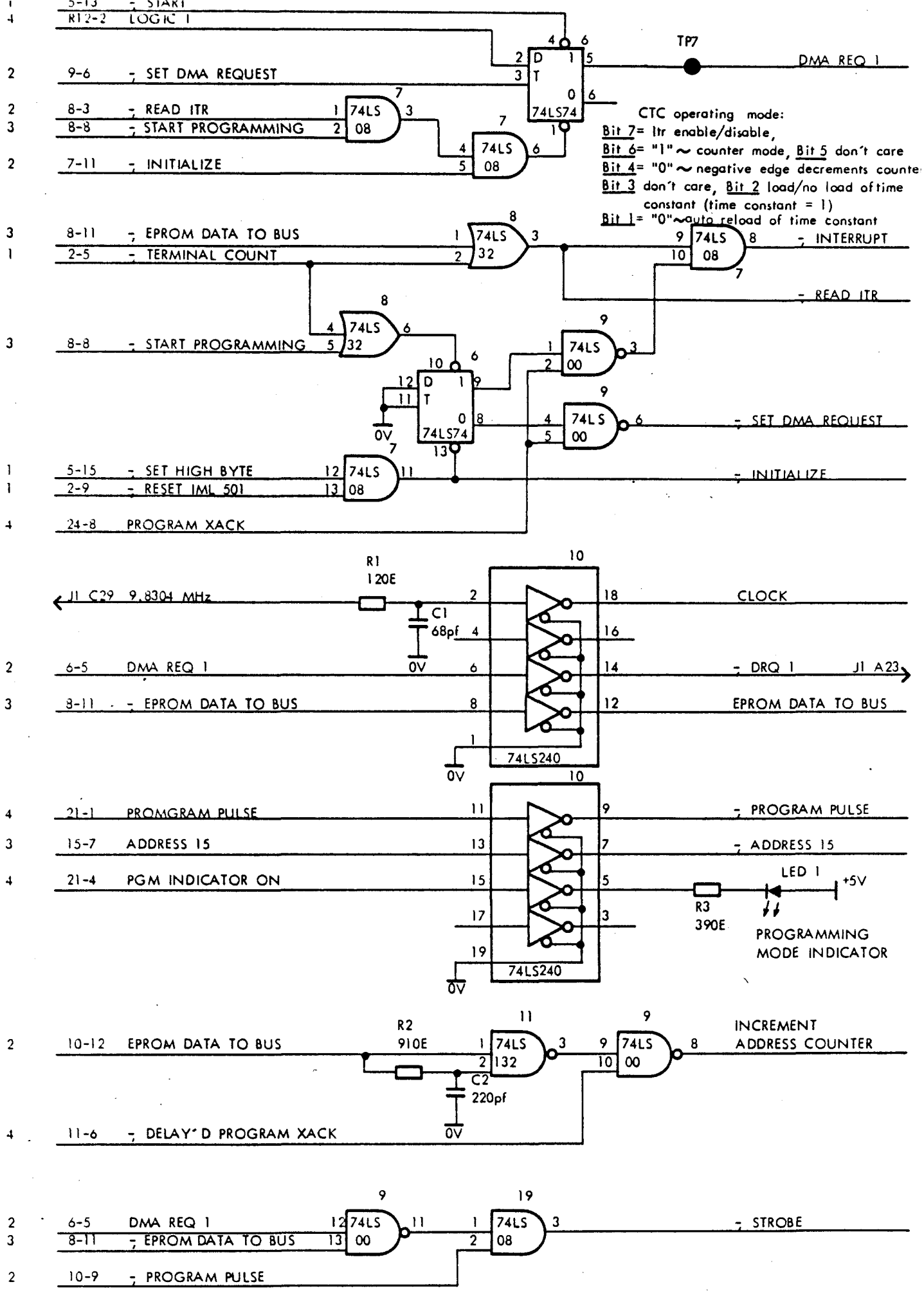
ADDRESS DECODING, CONTROL SIGNAL BUFFER and BUS BUFFER

Circuit Diagram

P. 1

A14107

SIGNAL	DESTINATION	DESCRIPTION
DMA REQ 1	p. 2	DMA request FF. This FF is set when IML501 requires DMA service.
¬, INTERRUPT	p. 1	During read from EPROM's an interrupt signal is generated when the last byte is transferred to the display unit RAM memory. During programming of EPROM's an interrupt signal is generated when the last requested byte has been programmed into the addressed EPROM location. The interrupt signal is sent to the Z80 processor via CTC device channel 3. The trailing edge of the signal causes the interrupt of the Z80 processor.
¬, READ ITR	p. 2	¬, Read Interrupt. Generated during read from EPROM's when DMA byte count becomes zero. The signal resets the DMA request FF.
¬, SET DMA REQUEST	p. 2	Generated during programming of EPROM's to set the DMA request FF, thus requesting the next byte to be programmed.
¬, INITIALIZE	p. 2 p. 4	This signal terminates all IML502 activity and places the logic in a well defined state.
CLOCK	p. 4	Buffered 9.8304MHz clock used by the programming timer.
¬, DRQ 1	J1-A23	Buffered DMA request from IML501.
EPROM DATA TO BUS	p. 2	Generates the INCREMENT ADDRESS COUNTER signal during read from EPROM's.
¬, PROGRAM PULSE	p. 2 p. 4	The program pulse is a 53.1 mS wide pulse used during programming of the EPROM's. Refer also to the description of the programming timer on p. 4.
¬, ADDRESS 15	p. 5A p. 5B	Inverted Address Counter bit 15.
PROGRAMMING MODE INDICATOR	p. 2	To be able to monitor the programming of the EPROM's, IML501 is equipped with a programming mode indicator, which turns on when the external programming voltage is connected to JACK 2. The PGM indicator gleams synchronously with the PROGRAM PULSE when programming the EPROM's. By means of a toggle FF every second PROGRAM PULSE produces a flash.
INCREMENT ADDRESS COUNTER	p. 3	This signal increments the address counter by one for every byte transferred between EPROM's and display unit RAM memory.
¬, STROBE	5A 5B	This signal strobes data from the addressed EPROM location to the EPROM bus during read of EPROM's. During programming of the EPROM's data held in the input register are programmed into the addressed EPROM location by means of this signal.



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IML 501

DMA SEQUENCER AND INTERRUPT CIRCUITS

p. 2

A14108

Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
ADDRESS 15 ADDRESS 14:11 ADDRESS 10:0	p. 2 p. 5A p. 5B p. 5A p. 5B p. 6 p. 7	Address Counter bits 15:0. I/O output instructions out <38_H> and out <39_H> load the address counter with the start address. During DMA write/read transfers the address counter is incremented by one for every byte transferred to/from display unit RAM memory.
EPROM BUS 7:0	p. 3 p. 6 p. 7	The EPROM bus connects the bidirectional information lines from the EPROM array with the outputs of the data in register and the inputs of the data out register. Data stored in the addressed EPROM location are sent via the EPROM bus to the data out register during DMA write transfers. Data held in the input register are sent via the EPROM bus to the addressed EPROM location during DMA read transfers (programming of the EPROM's).
-, START PROGRAMMING	p. 2 p. 4	This signal starts the programming timer and loads data from the bus into the data in register.
BUS 7:0	J1 p. 1	Display unit bus 7:0.
-, EPROM DATA TO BUS	p. 2	This signal latches addressed EPROM data in the data out register and gates the data to the diplay unit bus 7:0,

Designed by

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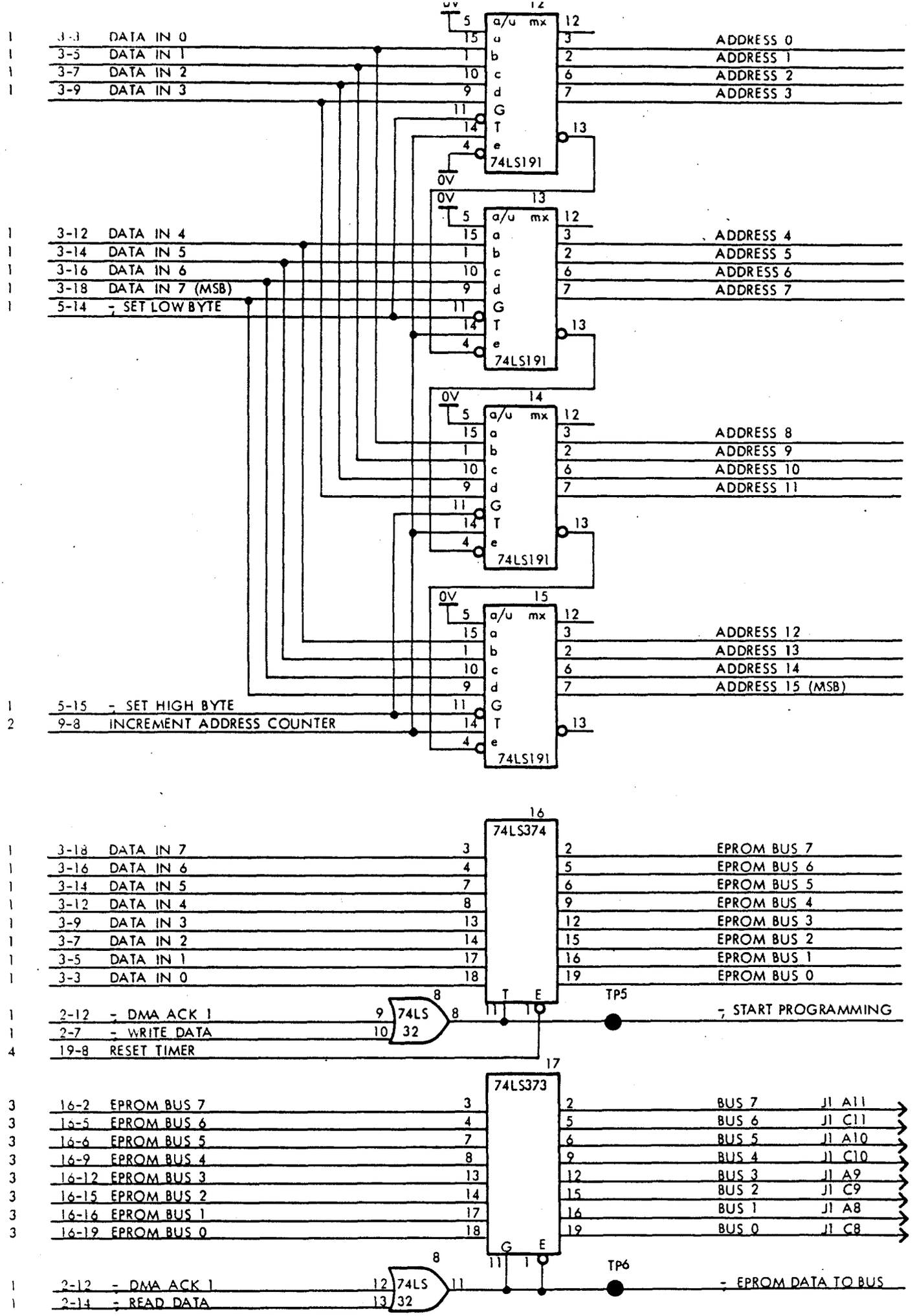

810521 VH 810819 OKJ

SIGNAL	DESTINATION	DESCRIPTION
¬, VPP ON	p. 4	Diagram 4 shows the write timing generator, which is used during programming of the EPROM's.
¬, DELAY'D PROGRAM XACK	p. 2	
RESET TIMER	p. 4 p. 3	The timing sequence is initiated when the ¬, START PROGRAMMING signal changes from low to high level. At this time the programming voltage is applied to the EPROM array via the transistor switch, and simultaneously a 20-bits counter is allowed to count (RESET TIMER at low level). Approx. 208 micro seconds later a 53.1 mS wide PROGRAM PULSE is generated. The programming pulse causes data held in the input register to be programmed into the addressed EPROM location.
PROGRAM PULSE	p. 2	
416.6 uS	p. 4	
PROGRAM XACK	p. 4 p. 2	
		The programming voltage is switched off at the trailing edge of programming pulse, and simultaneously a 208 micro second wide PROGRAM XACK pulse is generated.
		The trailing edge of the program xack pulse sets the DMA request FF if there are further bytes to be programmed, if not an interrupt is generated. The timer counter is also reset at the trailing edge of the program xack pulse thus ending the timing sequence.
VPP	p. 5A p. 5B	Programming Voltage. For INTEL 2732 and TEXAS 2532 this voltage must be 25V. For INTEL 2732A this voltage must be 21 volt.
PROGRAMMING VOLTAGE	p. 4	External Programming voltage via diode 1N 4005.
PGM INDICATOR ON	p. 2	This signal controls the programming mode indicator.
LOGIC 1	p. 4 p. 2	LOGIC 1 generator.

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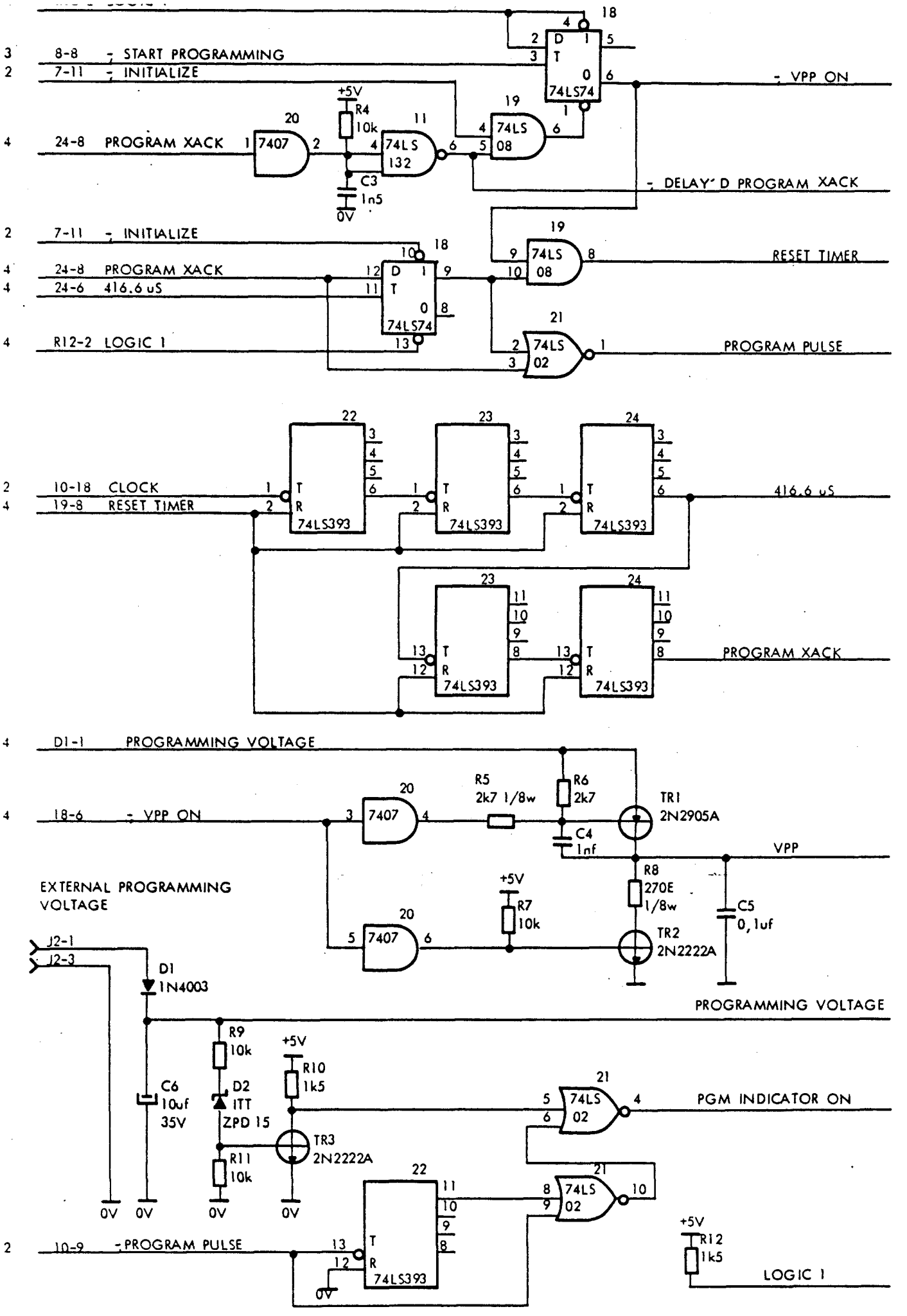

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SIGNAL	DESTINATION	DESCRIPTION
		Diagram 5A shows EPROM selection circuit valid if INTEL 2732/2732A EPROM's are used.
-, CE/A11 0:7	p. 6	-, Chip Enable or Address Counter bit 11 to the EPROM array.
-, CE/A11 8:15	p. 7	These signals are applied to pin 18 of the EPROM's in the array. If the module is strapped for INTEL 2732/2732A EPROM's, chip enable signal is applied to pin 18 to enable one EPROM out of sixteen EPROM's. -, CE 0 enables EPROM group 0-4K, -, CE 1 enables EPROM group 4-8K and so on. If the module is strapped for TEXAS 2532 EPROM's, address counter bit 11 is applied to pin 18.
VPP/-, STROBE 0:7	p. 6	Programming Voltage or Output Enable signals to pin 20 of the EPROM array.
VPP/-, STROBE 8:15	p. 7	If the module is strapped for INTEL 2732/2732A EPROM's, the programming voltage is applied to pin 20. If the module is strapped for TEXAS 2532 EPROM's, output enable signal is applied to pin 20. -, STROBE 0 enables EPROM group 0-4K, -, STROBE 1 enables group 4-8K and so on.
A11/VPP	p. 6 p. 7	Address Counter bit 11 or Programming Voltage to pin 21 of the EPROM array. If the module is strapped for INTEL 2732/2732A EPROM's, address counter bit 11 is applied to pin 21. If the module is strapped for TEXAS 2532 EPROM's, the programming voltage is applied to pin 21.

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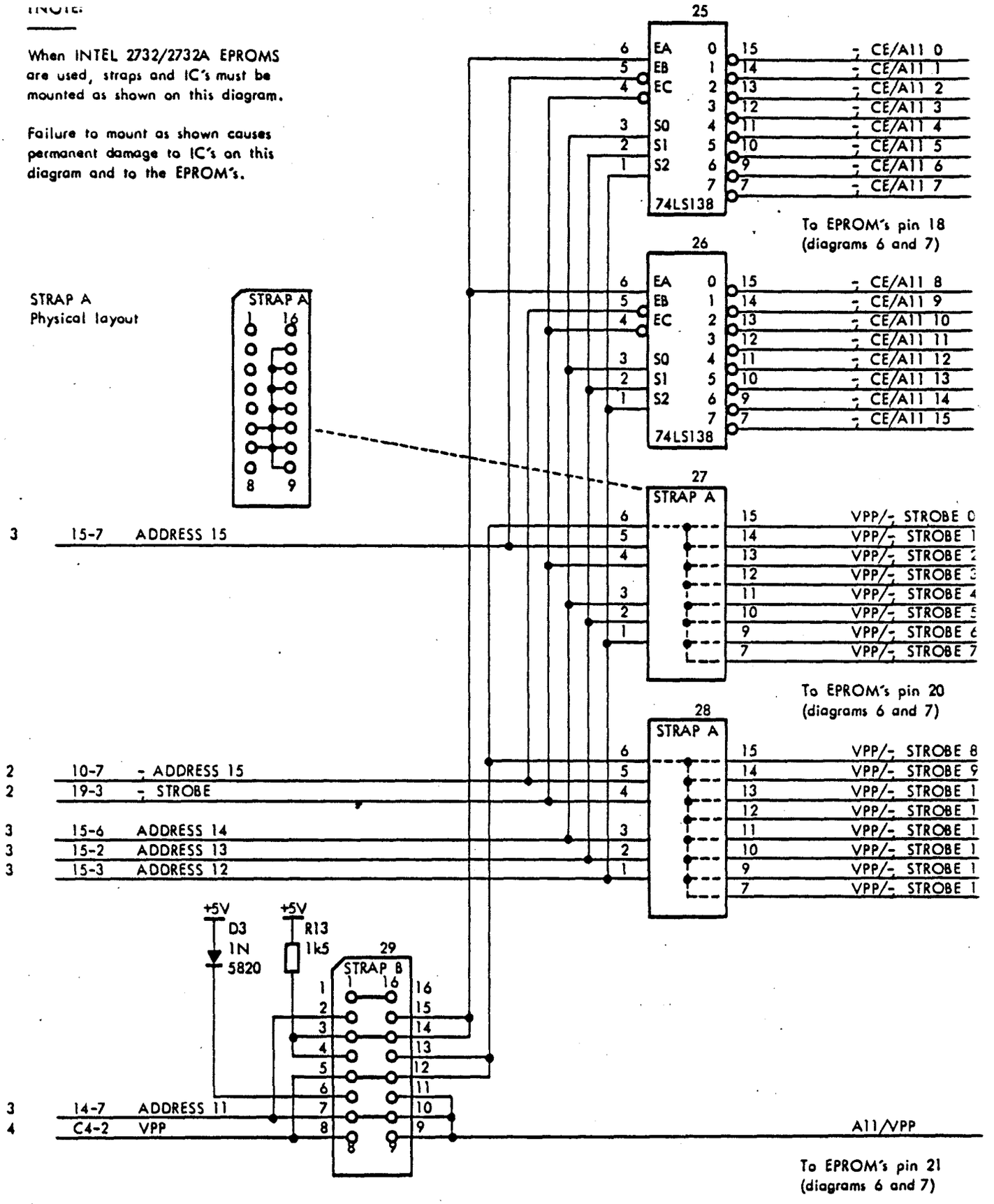
NOTE:

When INTEL 2732/2732A EPROMS are used, straps and IC's must be mounted as shown on this diagram.

Failure to mount as shown causes permanent damage to IC's on this diagram and to the EPROM's.



B10820 OKJ

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SIGNAL	DESTINATION	DESCRIPTION
		Diagram 5B shows EPROM selection circuit valid if TEXAS 2532 EPROM's are used. Refer to signal list p. 5A for signal destination and description.

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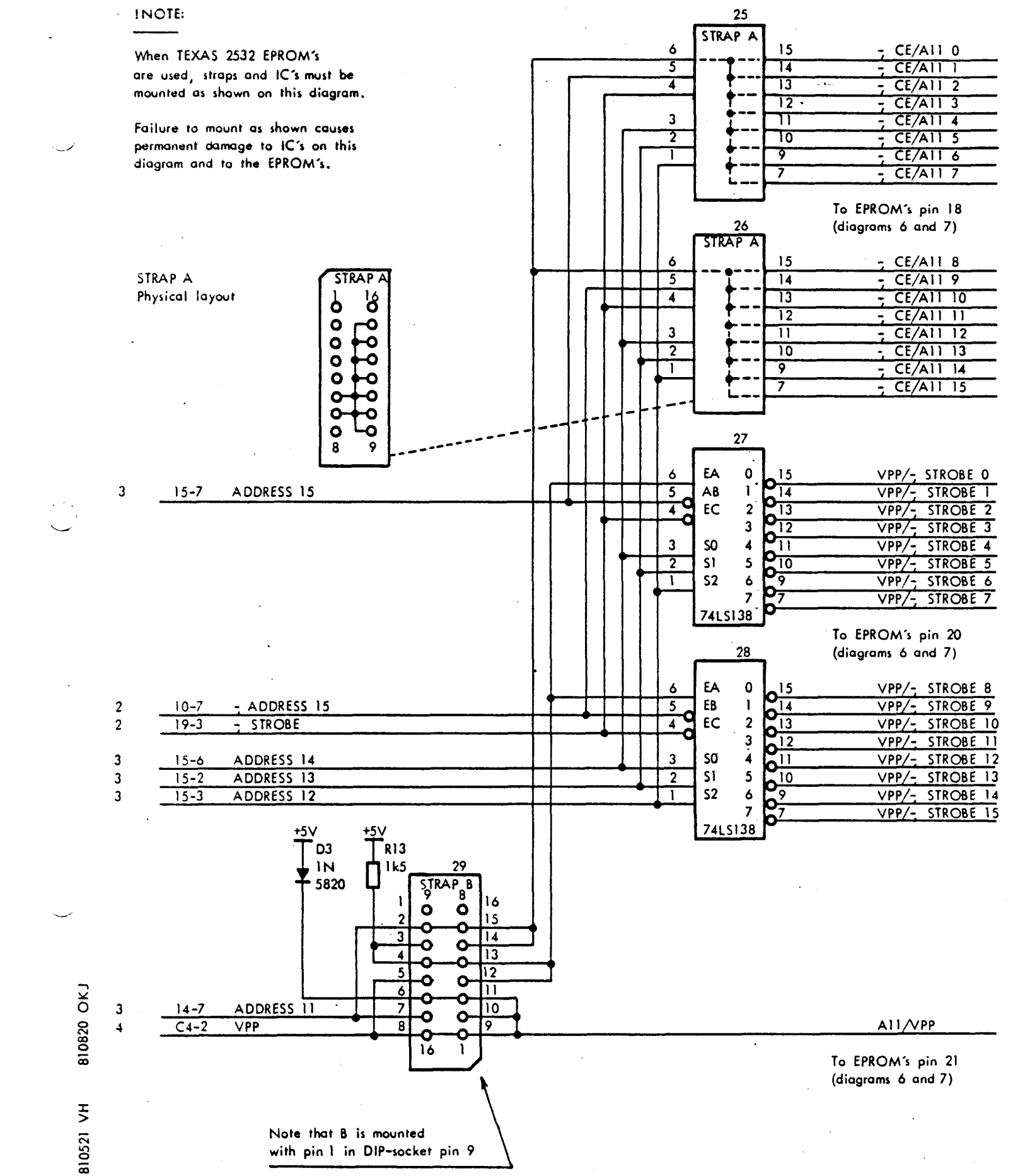
NOTE:

When TEXAS 2532 EPROM's are used, straps and IC's must be mounted as shown on this diagram.

Failure to mount as shown causes permanent damage to IC's on this diagram and to the EPROM's.



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SIGNAL	DESTINATION	DESCRIPTION

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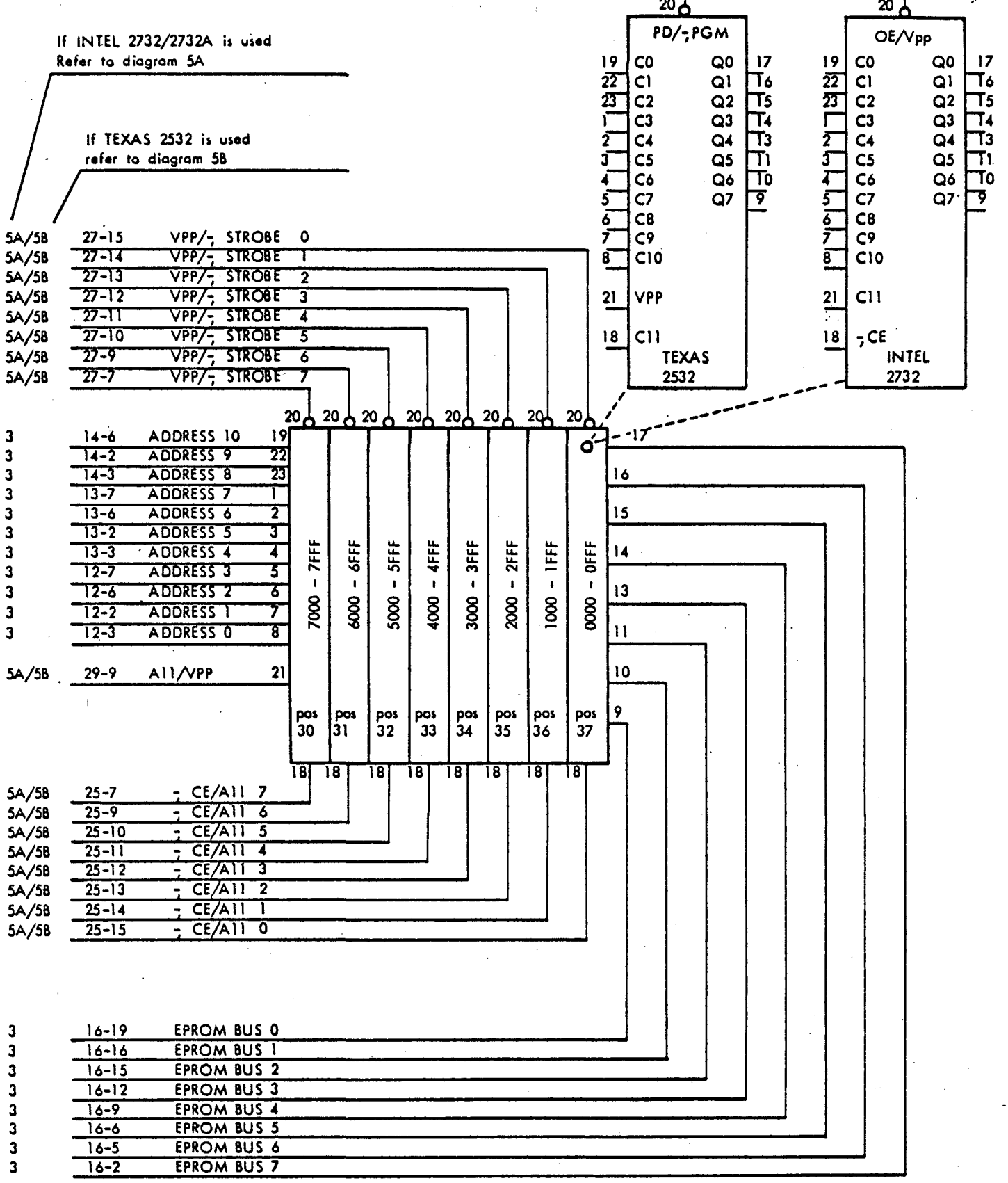
Unit IML501		
Dwg. No. A25967	Signal List	p. 6



810820 OKJ

810522 VH

Following EPROM's are recommended:

INTEL 2732, TEXAS 2532 PROGRAMMING VOLTAGE = 25 VOLT.

INTEL 2732A PROGRAMMING VOLTAGE = 21 VOLT.

SIGNAL	DESTINATION	DESCRIPTION

Designed by

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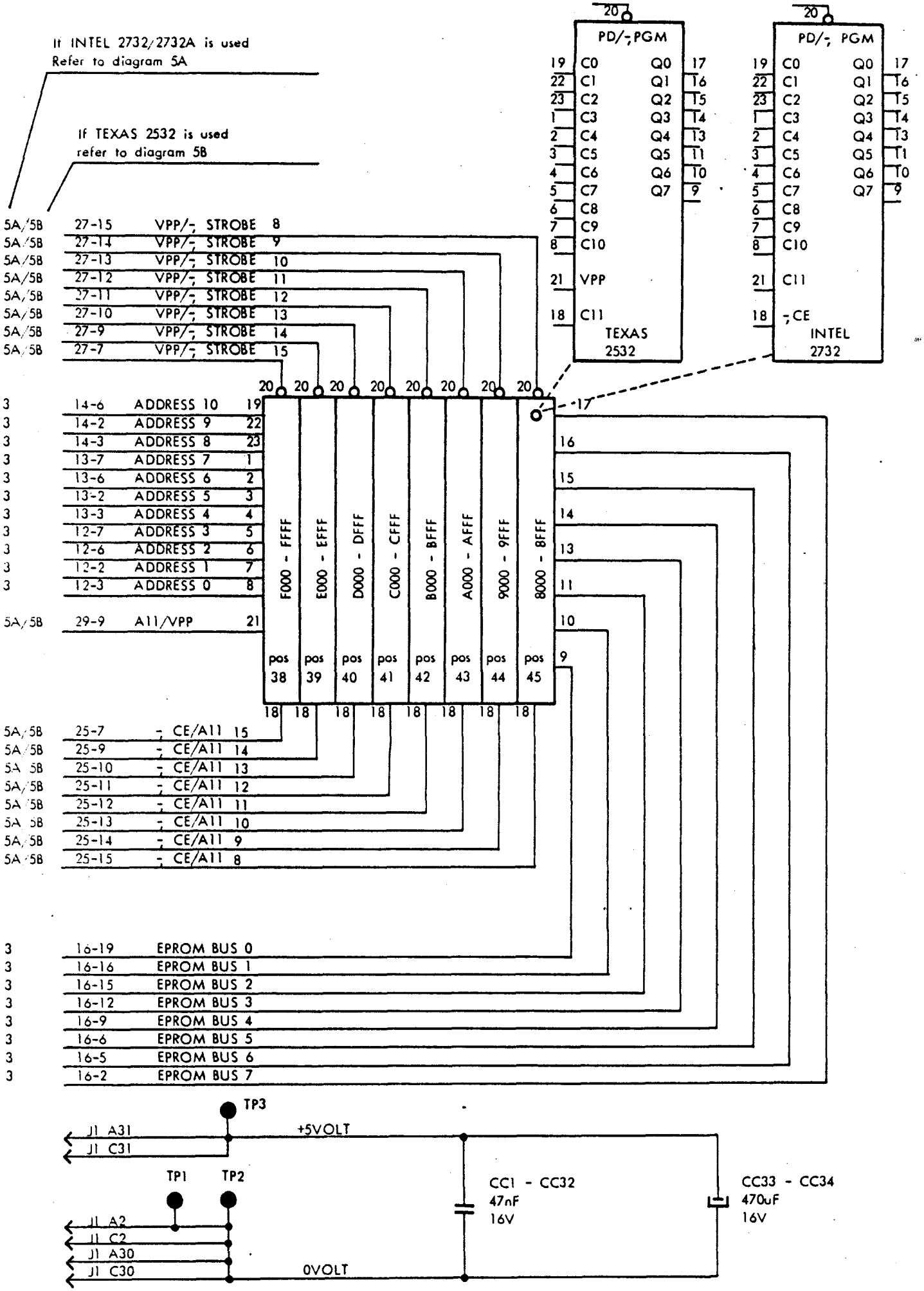
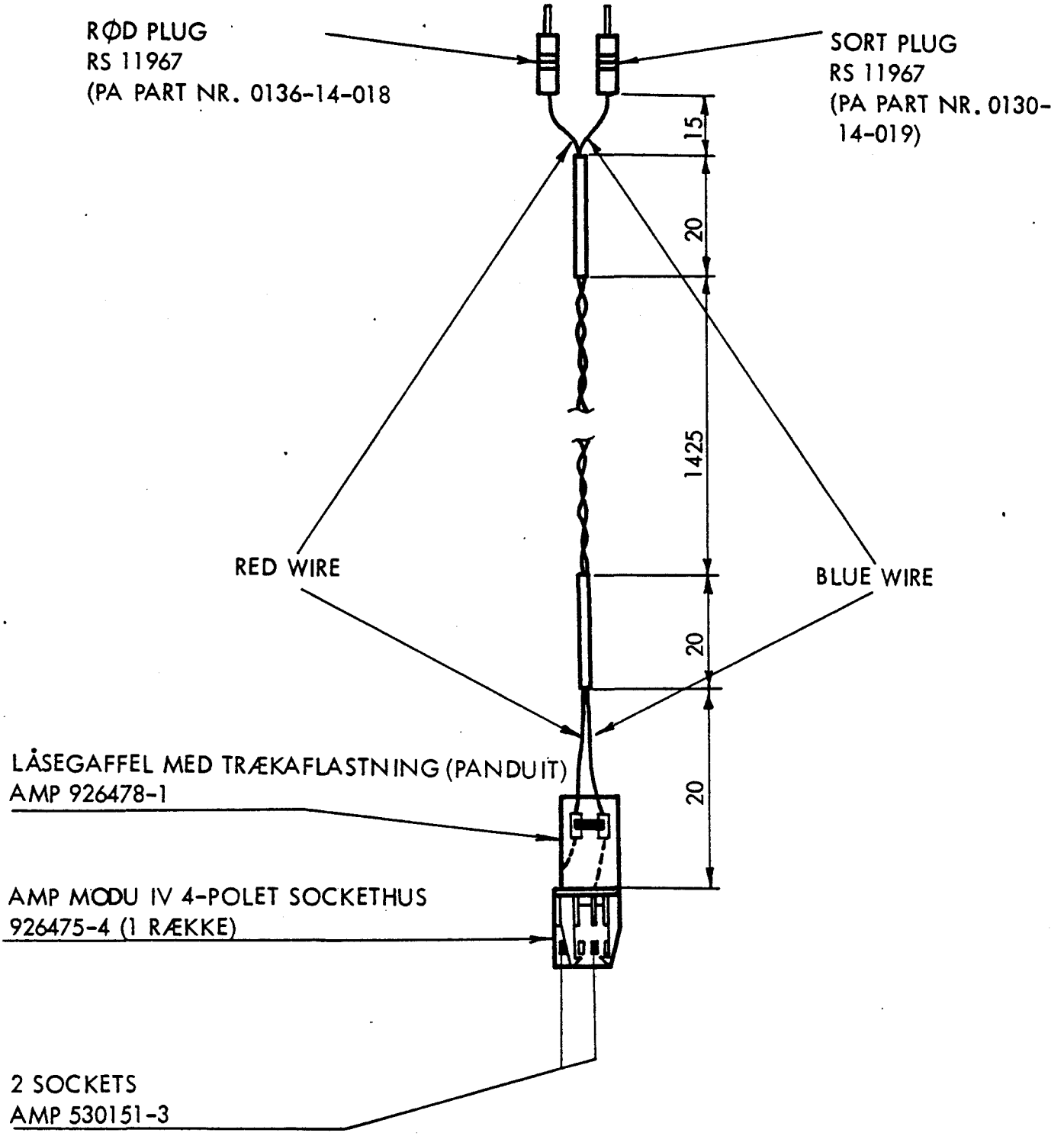

If INTEL 2732/2732A is used
Refer to diagram 5A
If TEXAS 2532 is used
refer to diagram 5B
PD/-;PGM
C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
VPP
TEXAS 2532
PD/-; PGM
-;CE
INTEL 2732
5A/5B 27-15 VPP/-; STROBE 8
5A/5B 27-14 VPP/-; STROBE 9
5A/5B 27-13 VPP/-; STROBE 10
5A/5B 27-12 VPP/-; STROBE 11
5A/5B 27-11 VPP/-; STROBE 12
5A/5B 27-10 VPP/-; STROBE 13
5A/5B 27-9 VPP/-; STROBE 14
5A/5B 27-7 VPP/-; STROBE 15
3 14-6 ADDRESS 10 19
3 14-2 ADDRESS 9 22
3 14-3 ADDRESS 8 23
3 13-7 ADDRESS 7 1
3 13-6 ADDRESS 6 2
3 13-2 ADDRESS 5 3
3 13-3 ADDRESS 4 4
3 12-7 ADDRESS 3 5
3 12-6 ADDRESS 2 6
3 12-2 ADDRESS 1 7
3 12-3 ADDRESS 0 8
5A/5B 29-9 A11/VPP 21
F000 - FFFF
E000 - EFFF
D000 - DFFF
C000 - CFFF
B000 - BFFF
A000 - AFFF
9000 - 9FFF
8000 - 8FFF
pos 38
pos 39
pos 40
pos 41
pos 42
pos 43
pos 44
pos 45
5A/5B 25-7 -; CE/A11 15
5A/5B 25-9 -; CE/A11 14
5A/5B 25-10 -; CE/A11 13
5A/5B 25-11 -; CE/A11 12
5A/5B 25-12 -; CE/A11 11
5A/5B 25-13 -; CE/A11 10
5A/5B 25-14 -; CE/A11 9
5A/5B 25-15 -; CE/A11 8
3 16-19 EPROM BUS 0
3 16-16 EPROM BUS 1
3 16-15 EPROM BUS 2
3 16-12 EPROM BUS 3
3 16-9 EPROM BUS 4
3 16-6 EPROM BUS 5
3 16-5 EPROM BUS 6
3 16-2 EPROM BUS 7
810820 OKJ
810522 VH
TP3
J1 A31
J1 C31
+5VOLT
TP1
TP2
J1 A2
J1 C2
J1 A30
J1 C30
0VOLT
CC1 - CC32
47nF
16V
CC33 - CC34
470uF
16V

CONNECTOR : J1

PIN	GENERATOR ADDRESS	SIGNAL NAME		PIN	GENERATOR ADDRESS	SIGNAL NAME		PIN	GENERATOR ADDRESS	SIGNAL NAME	
A 1		- 12V	*	B 1				C 1		- 12V	*
A 2		0V	*	B 2				C 2		0V	
A 3		- IML REQ	*	B 3				C 3		- RESET IN	*
A 4		- IORD	*	B 4				C 4		- EXT AEN	*
A 5		- IOWR	*	B 5				C 5		- EXT AD STB	*
A 6		- MEM RD	*	B 6				C 6		- DRQ 3	*
A 7		- MEM WR	*	B 7				C 7		- TC	
A 8		BUS 1		B 8				C 8		BUS 0	
A 9		BUS 3		B 9				C 9		BUS 2	
A10		BUS 5		B10				C10		BUS 4	
A11		BUS 7		B11				C11		BUS 6	
A12		- INT	*	B12				C12		- IORQ BUF	
A13		ADD 0		B13				C13		ADD 2	
A14		CHAIN 4	*	B14				C14		CHAIN 3	*
A15		- M1 BUF	*	B15				C15		ADD 1	
A16		ADD 4		B16				C16		- RD BUF	*
A17		- WAIT	*	B17				C17		ADD 3	
A18		ADD 5		B18				C18		ADD 15	
A19		ADD 6		B19				C19		ADD 14	
A20		ADD 7		B20				C20		ADD 13	
A21		- DACK 1		B21				C21		ADD 12	
A22		- DACK 3	*	B22				C22		ADD 11	
A23		- DRQ 1		B23				C23		ADD 10	
A24		- WRBUF		B24				C24		ADD 9	
A25		- MREQ BUF	*	B25				C25		ADD 8	
A26		- RFSH BUF	*	B26				C26		- NMI	*
A27		CLK	*	B27				C27		- RESET	
A28		- HOLD ACK	*	B28				C28		- HALT BUF	*
A29		- HOLD	*	B29				C29		9.8304 MHZ	
A30		0V		B30				C30		0V	
A31		+ 5V		B31				C31		+ 5V	
A32		+ 12V	*	B32				C32		+ 12V	*

* = NOT USED BY IML 501


RØD PLUG
RS 11967
(PA PART NR. 0136-14-018
SORT PLUG
RS 11967
(PA PART NR. 0130-
14-019)
15
20
1425
20
20
RED WIRE
BLUE WIRE
LÅSEGAFFEL MED TRÆKAFLASTNING (PANDUIT)
AMP 926478-1
AMP MODU IV 4-POLET SOCKETHUS
926475-4 (1 RÆKKE)
2 SOCKETS
AMP 530151-3

A. REFERENCES

A.

[1] IML501 Reference Manual
RCSL: 52-AA1057

RETURN LETTER

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