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Title:

SCC705
LOGICAL DIAGRAMS

A/S REGNECENTRALEN
af 1979

Keywords:

CHS 701, Communications Controller

Abstract:

These papers contains diagrams and drawings for the communications controller, SCC705.

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42-i 1286

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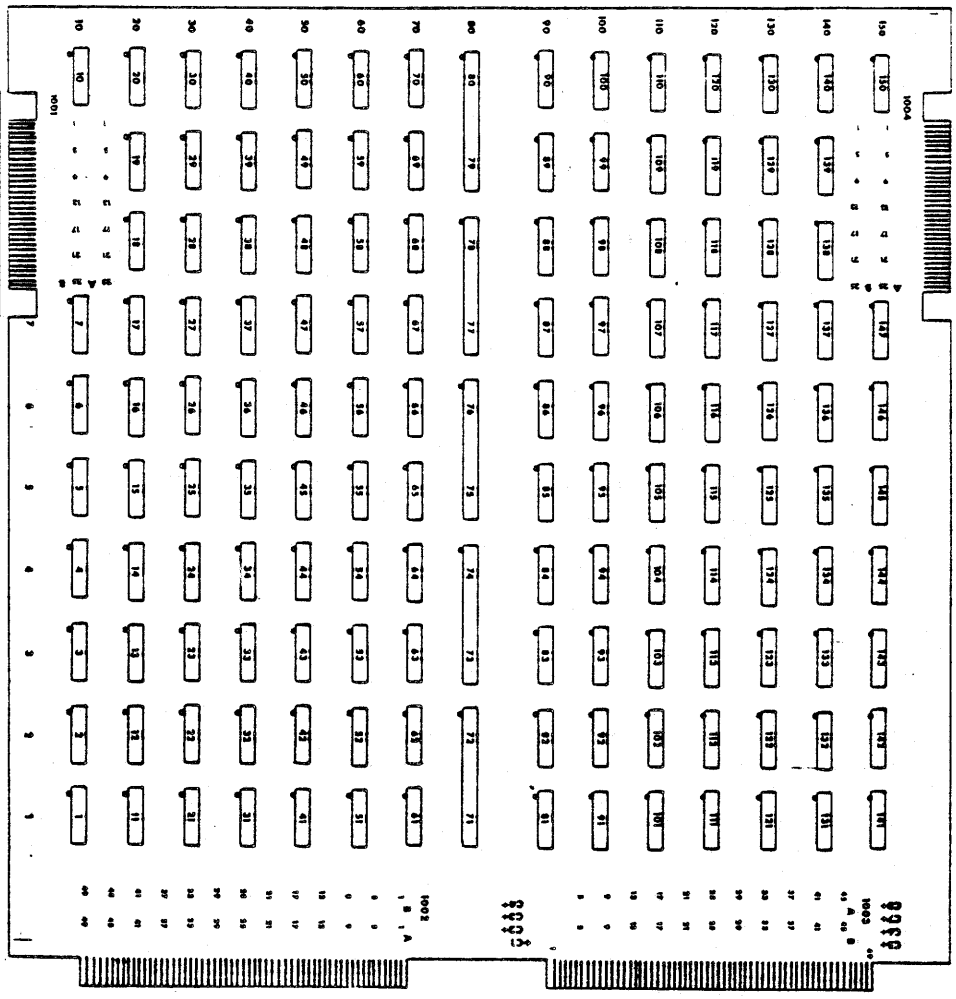

SCC 705
1001

HC

CBL022

150673

SCC 705
J1

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Connector 1001	Gen. addr.	Signal Name	Connector J1	Connector 1001	Gen. addr.	Signal Name	Connector J1
A 1			1	A14		Transmitter clock signal	26
B 1			2	B 14		GND	25
A 2			3	A15		Receiver clock signal	24
B 2			4	B 15		GND	23
A 3		Transmitted data	5	A16			22
B 3		GND	6	B 16			21
A 4		Received data	7	A17			20
B 4		GND	8	B 17			19
A 5		Request to send	9	A18			18
B 5		GND	10	B 18			36
A 6		Ready for sending	11	A19		+ 5 volts	37
B 6		GND	12	B 19		GND = 0 volts	38
A 7		Dataset ready	13	A20		+ 12 volts	39
B 7		GND	14	B 20		GND	40
A 8		Dataterjinal ready	15	A21		- 12 volts	41
B 8		GND	16	B 21		GND	42
A 9		Received carrier	17	A22		GND	43
B 9		GND	35	B 22		GND	44
A10			34	A23			45
B 10			33	B 23			46
A11		Data signaling rate (speed)	32	A24			47
B 11		GND	31	B 24			48
A12			30	A25		Calling signal	49
B 12			29	B 25		GND	50
A13			28			Chassis	51
B 13			27			Chassis	52

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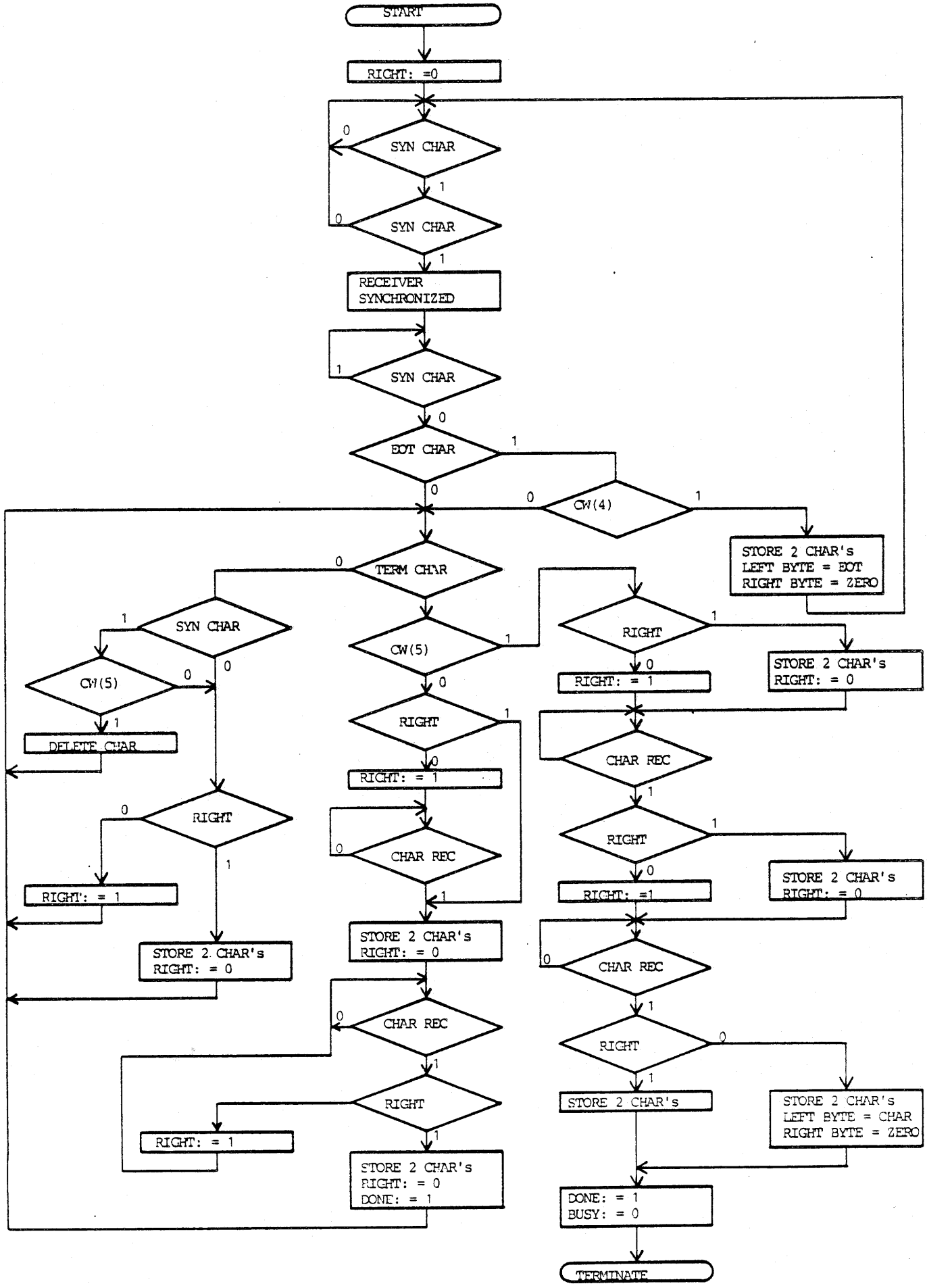

RECEIVER FLOW DIAGRAM

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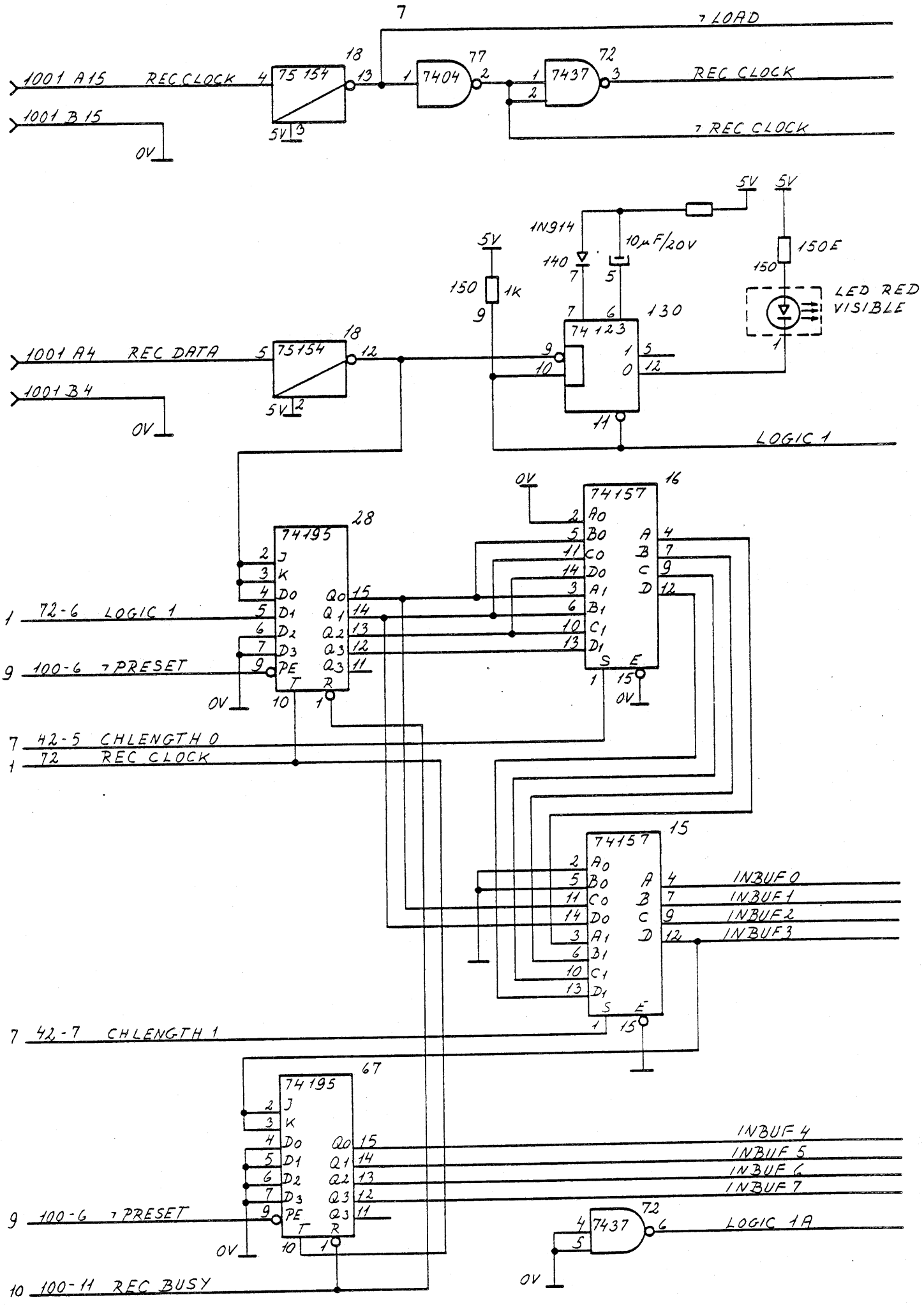

AJJ 7.2.79

SCC 705
R 12 654

RECEIVER SERIAL REGISTER
CHARACTER LENGTH SELECTOR

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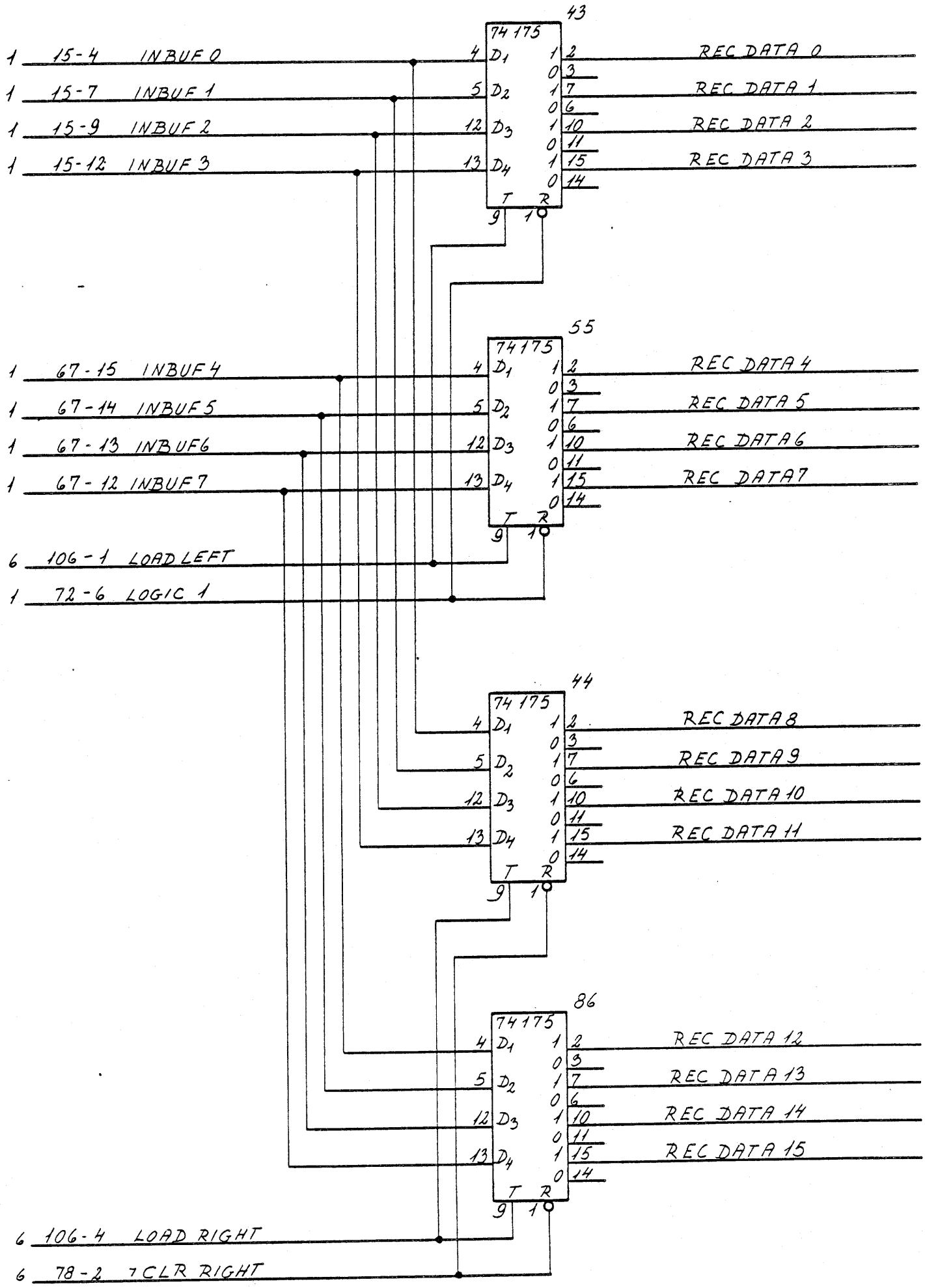
43
74 175
1 15-4 INBUF 0
1 15-7 INBUF 1
1 15-9 INBUF 2
1 15-12 INBUF 3
REC DATA 0
REC DATA 1
REC DATA 2
REC DATA 3
55
74 175
1 67-15 INBUF 4
1 67-14 INBUF 5
1 67-13 INBUF 6
1 67-12 INBUF 7
6 106-1 LOAD LEFT
1 72-6 LOGIC 1
REC DATA 4
REC DATA 5
REC DATA 6
REC DATA 7
44
74 175
REC DATA 8
REC DATA 9
REC DATA 10
REC DATA 11
86
74 175
6 106-4 LOAD RIGHT
6 78-2 CLR RIGHT
REC DATA 12
REC DATA 13
REC DATA 14
REC DATA 15

AAJ 10.4.79

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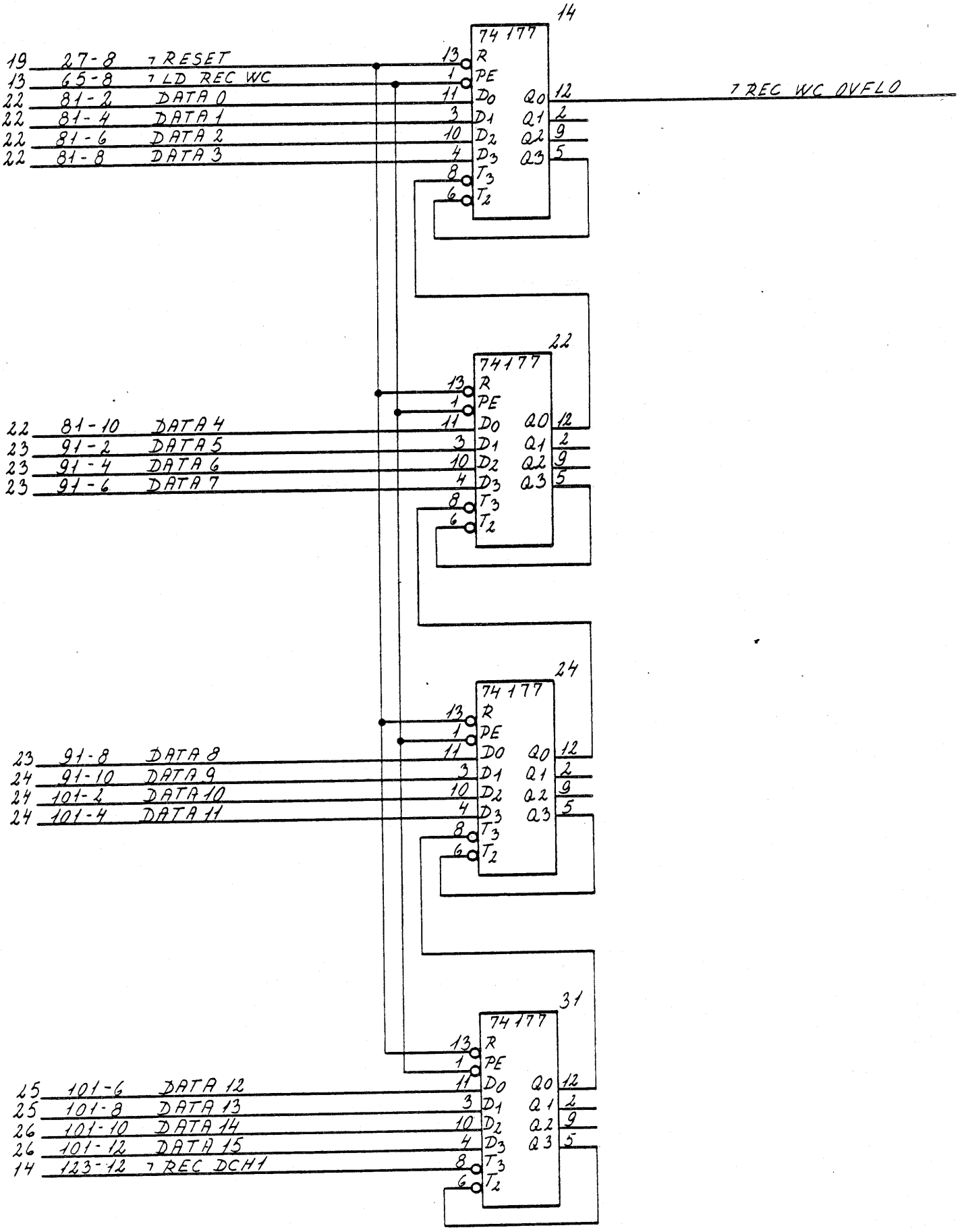

AAJ 10.4.79

SCC 705

R 12697

RECIEVER WORD COUNTER

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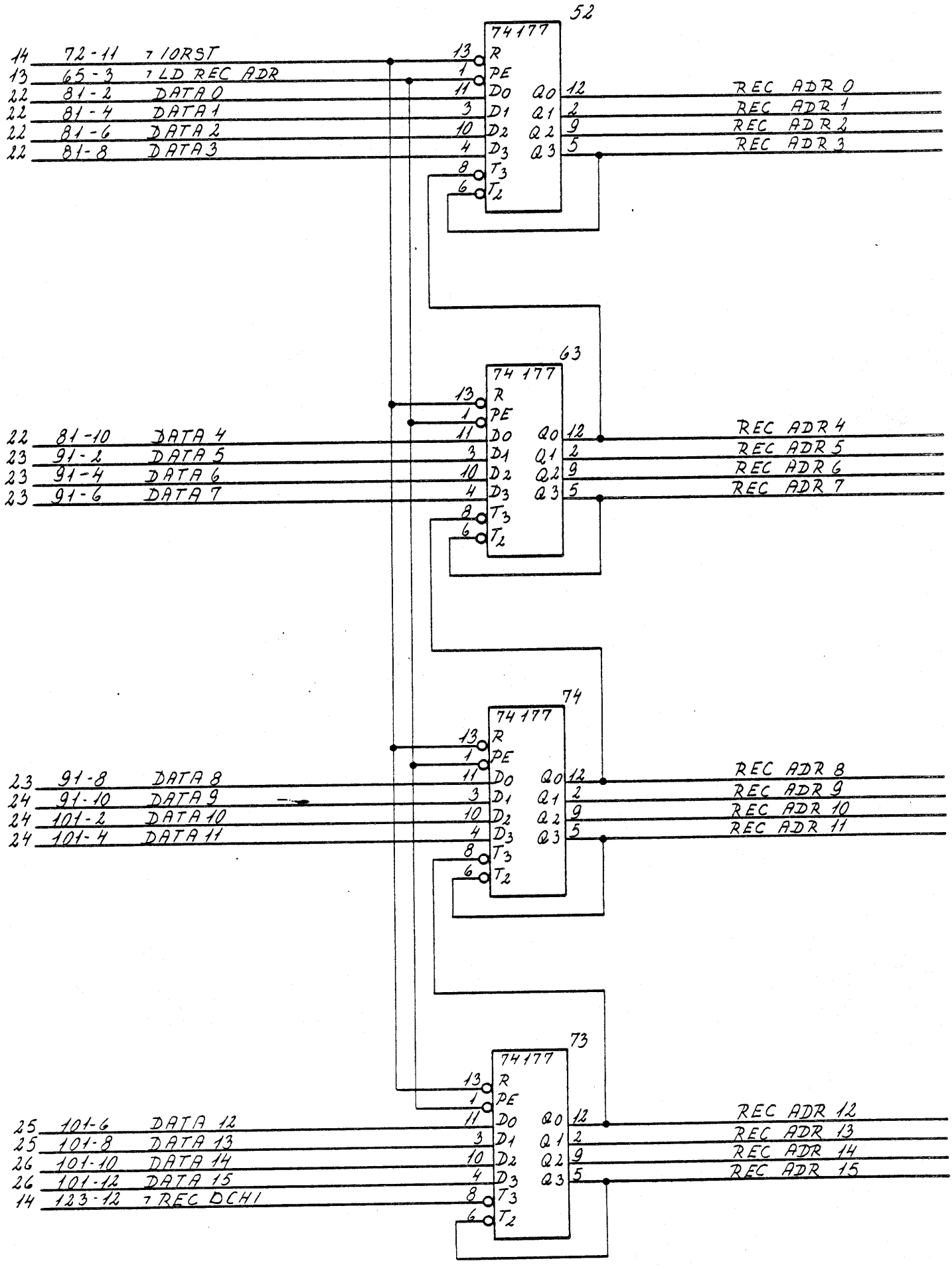

AAJ 10.4.79

SCC 705 RECIEVER ADDRESS COUNTER 4

R 12698

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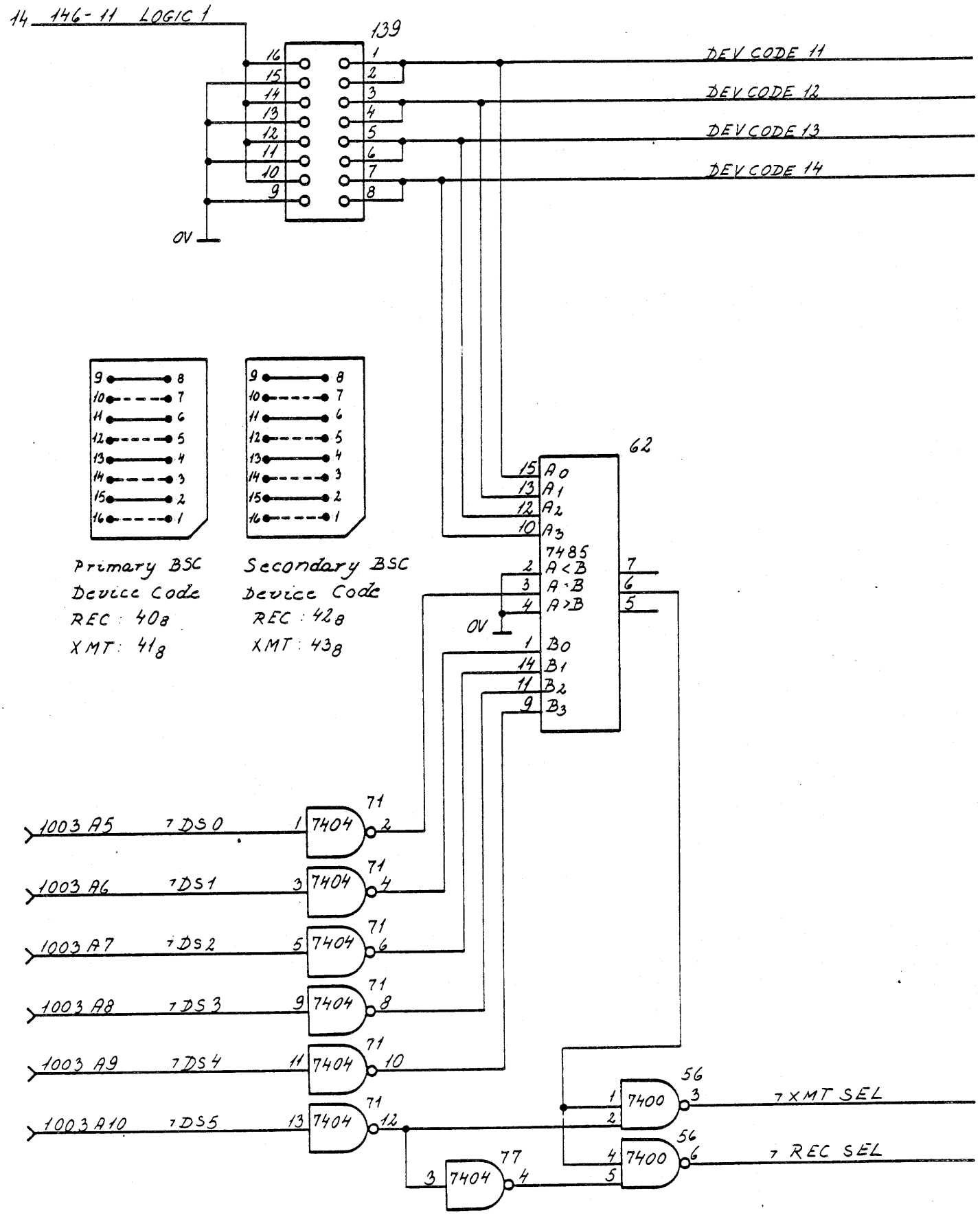

AA3 10.4.79

SCC 705
R 12 699

DEVICE CODE DETECT
AND GENERATE

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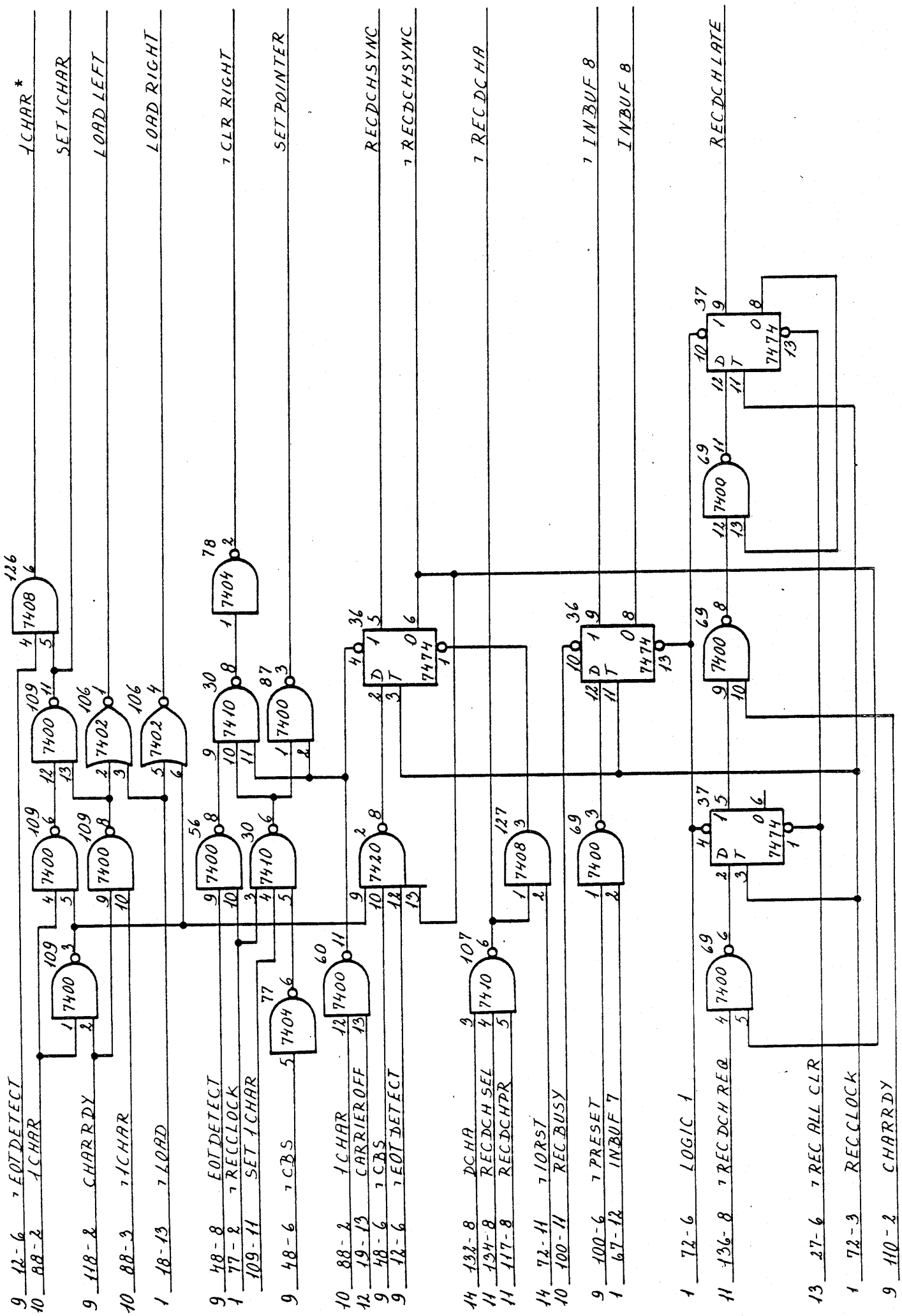

AAJ 10.4.79

SCC 705

RECEIVER CHAR. CONTROL

6

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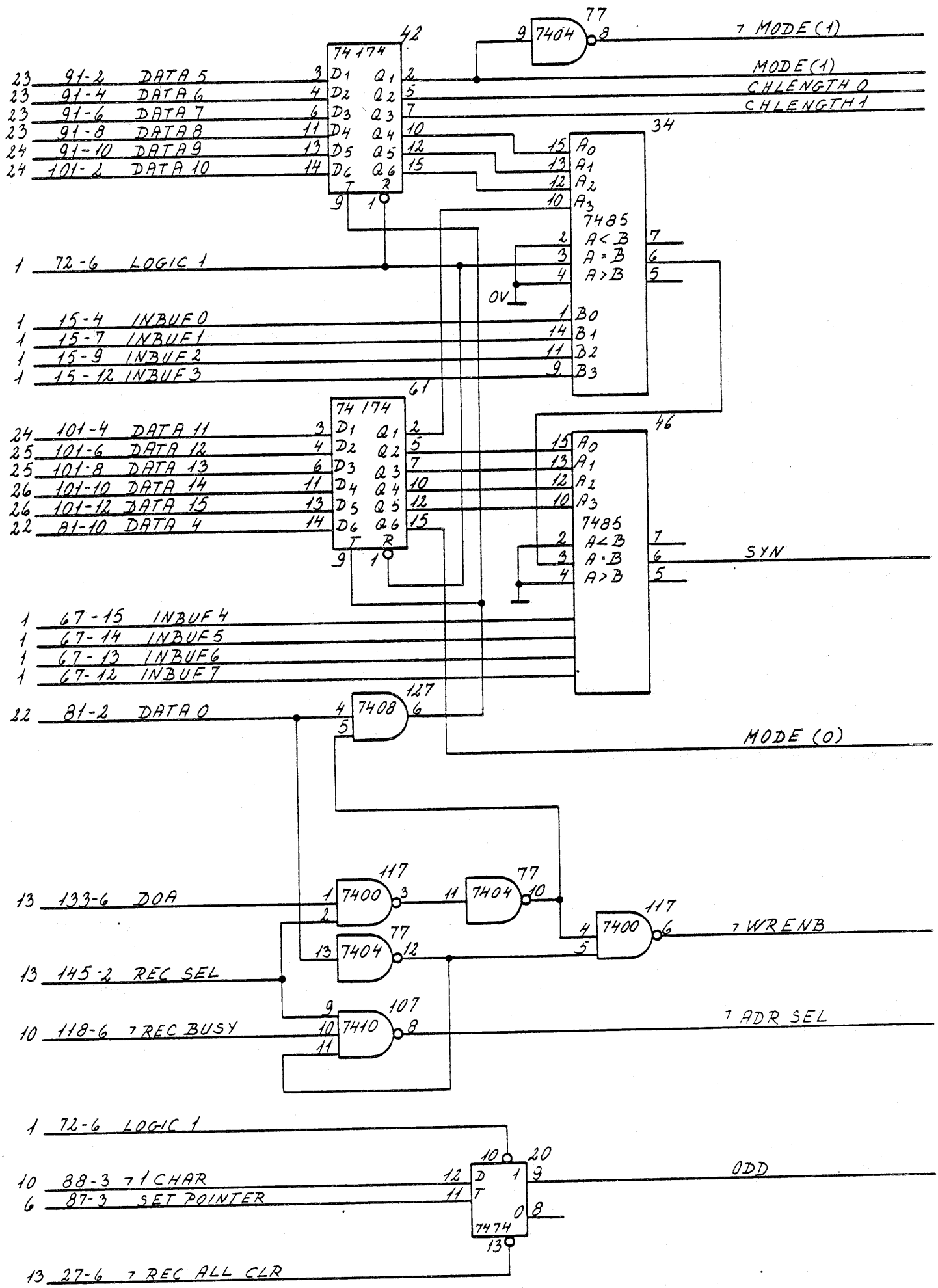
77
7404
7 MODE(1)
MODE(1)
CHLENGTH 0
CHLENGTH 1
42
74 174
23 91-2 DATA 5
23 91-4 DATA 6
23 91-6 DATA 7
23 91-8 DATA 8
24 91-10 DATA 9
24 101-2 DATA 10
34
7485
1 72-6 LOGIC 1
0V
1 15-4 INBUF 0
1 15-7 INBUF 1
1 15-9 INBUF 2
1 15-12 INBUF 3
61
74 174
24 101-4 DATA 11
25 101-6 DATA 12
25 101-8 DATA 13
26 101-10 DATA 14
26 101-12 DATA 15
22 81-10 DATA 4
46
7485
SYN
1 67-15 INBUF 4
1 67-14 INBUF 5
1 67-13 INBUF 6
1 67-12 INBUF 7
22 81-2 DATA 0
127
7408
MODE (0)
117
7400
13 133-6 DOA
77
7404
7 WRENB
13 145-2 REC SEL
107
7410
10 118-6 7 REC BUSY
7 ADR SEL
1 72-6 LOGIC 1
20
7474
10 88-3 7 1 CHAR
6 87-3 SET POINTER
ODD
13 27-6 7 REC ALL CLR

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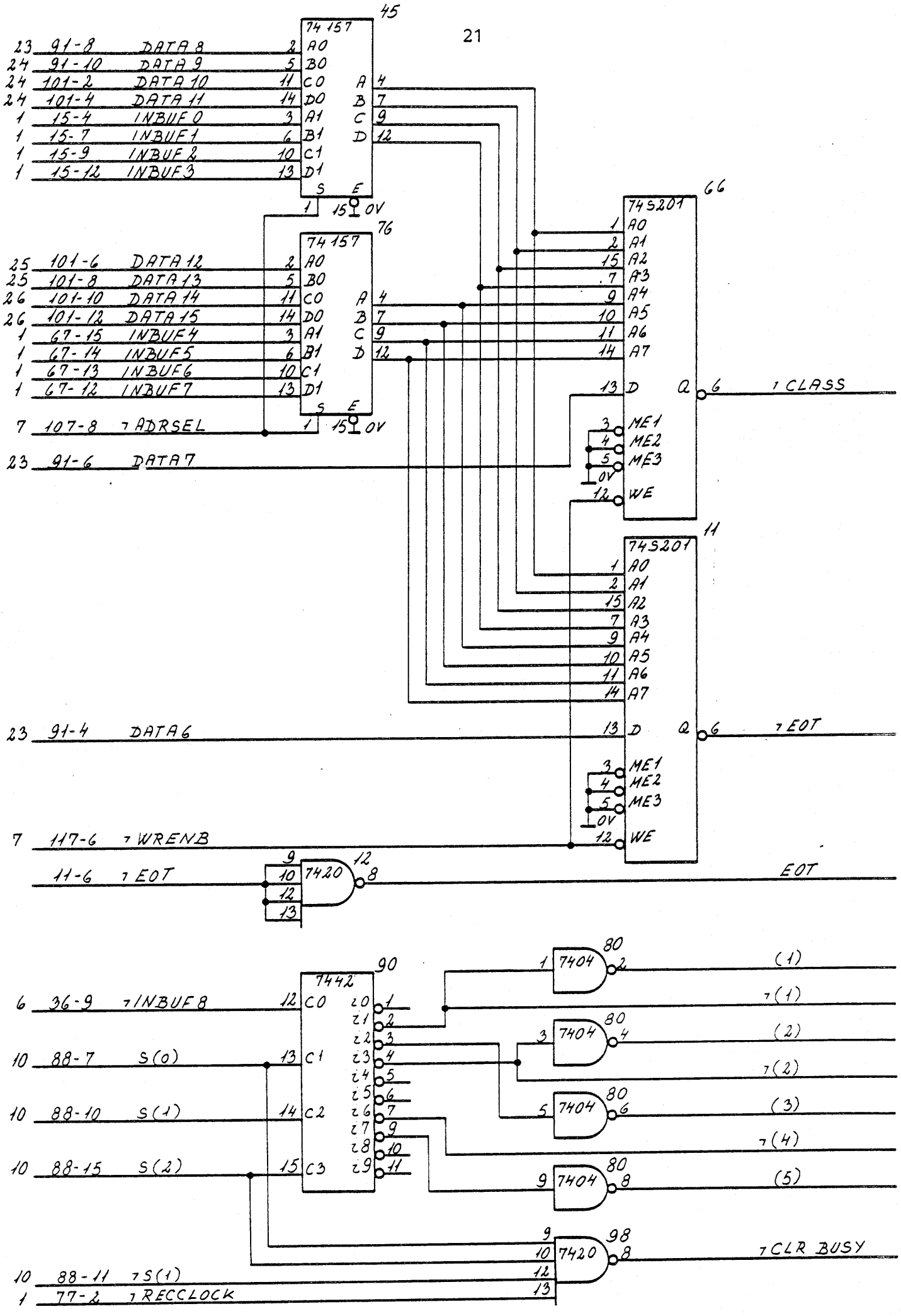
45
74 157
23 91-8 DATA 8
24 91-10 DATA 9
24 101-2 DATA 10
24 101-4 DATA 11
1 15-4 INBUF 0
1 15-7 INBUF 1
1 15-9 INBUF 2
1 15-12 INBUF 3
A0 B0 C0 D0 A1 B1 C1 D1
S E
A B C D
1 15 0V
76
74 157
25 101-6 DATA 12
25 101-8 DATA 13
26 101-10 DATA 14
26 101-12 DATA 15
1 67-15 INBUF 4
1 67-14 INBUF 5
1 67-13 INBUF 6
1 67-12 INBUF 7
7 107-8 ⌐ADRSEL
66
74S201
23 91-6 DATA 7
A0 A1 A2 A3 A4 A5 A6 A7
D Q
ME1 ME2 ME3 0V WE
⌐CLASS
11
74S201
23 91-4 DATA 6
7 117-6 ⌐WRENB
⌐EOT
11-6 ⌐EOT
7420
EOT
90
7442
6 36-9 ⌐INBUF 8
10 88-7 S(0)
10 88-10 S(1)
10 88-15 S(2)
C0 C1 C2 C3
z0 z1 z2 z3 z4 z5 z6 z7 z8 z9
80
7404
(1)
⌐(1)
(2)
⌐(2)
(3)
⌐(4)
(5)
98
7420
⌐CLR BUSY
10 88-11 ⌐S(1)
1 77-2 ⌐RECCLOCK

AAJ 10.4.79

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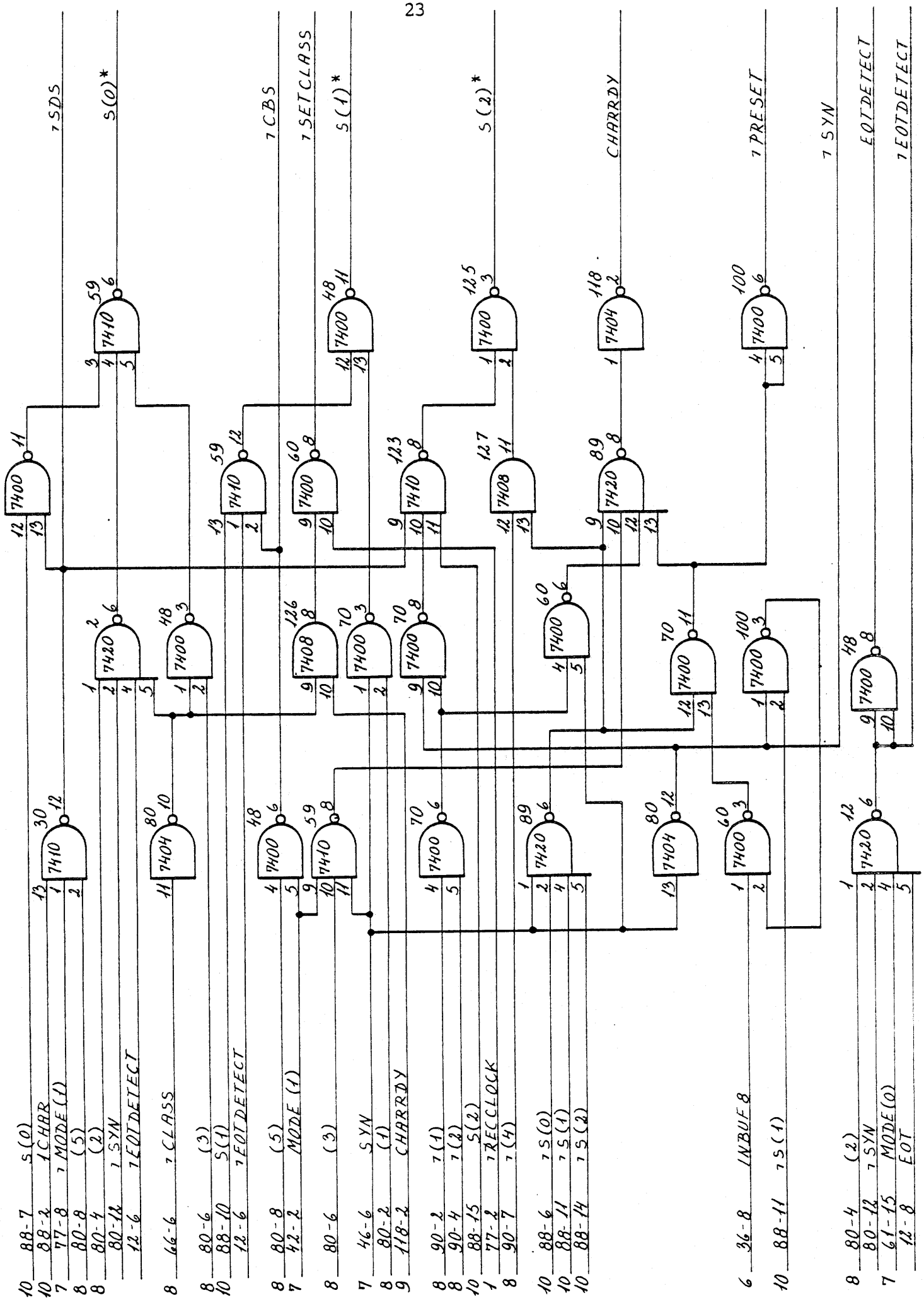
7SDS
S(0)*
7CBS
7SETCLASS
S(1)*
S(2)*
CHARRDY
7PRESET
7SYN
EOTDETECT
7EOTDETECT
7CHAR
7MODE(1)
(5)
(2)
7SYN
7EOTDETECT
7CLASS
(3)
S(1)
7EOTDETECT
(5)
MODE(1)
(3)
SYN
(1)
CHARRDY
7(1)
7(2)
S(2)
7RECCLOCK
7(4)
7S(0)
7S(1)
7S(2)
INBUF8
7S(1)
(2)
7SYN
MODE(0)
EOT

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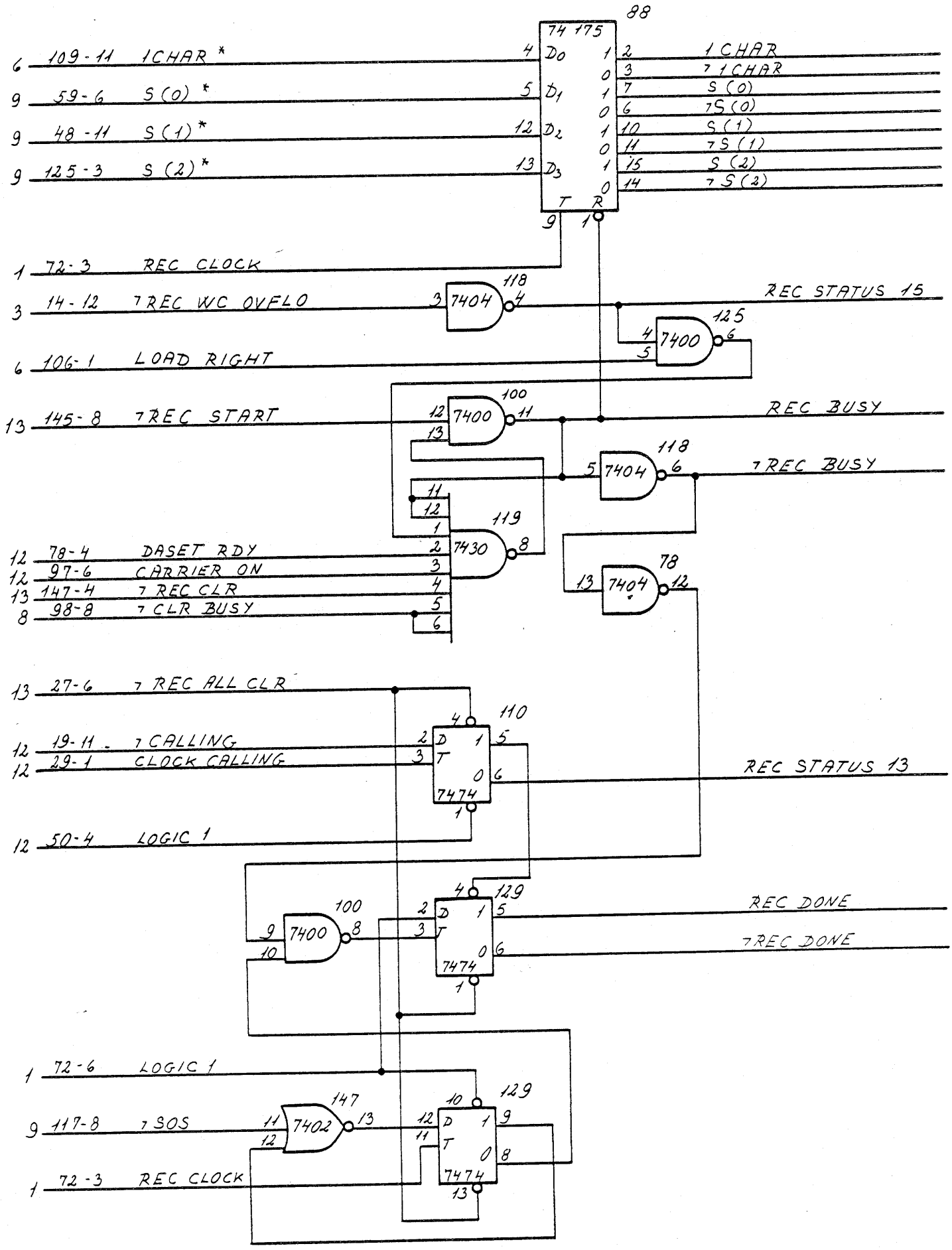
88
74 175
6 109-11 1CHAR *
9 59-6 S(0) *
9 48-11 S(1) *
9 125-3 S(2) *
1 72-3 REC CLOCK
3 14-12 ⁊REC WC OVFLO
6 106-1 LOAD RIGHT
13 145-8 ⁊REC START
12 78-4 DASET RDY
12 97-6 CARRIER ON
13 147-4 ⁊REC CLR
8 98-8 ⁊CLR BUSY
13 27-6 ⁊REC ALL CLR
12 19-11 ⁊CALLING
12 29-1 CLOCK CALLING
12 50-4 LOGIC 1
1 72-6 LOGIC 1
9 117-8 ⁊SOS
1 72-3 REC CLOCK
1CHAR
⁊1CHAR
S(0)
⁊S(0)
S(1)
⁊S(1)
S(2)
⁊S(2)
REC STATUS 15
REC BUSY
⁊REC BUSY
REC STATUS 13
REC DONE
⁊REC DONE
7400
7404
7430
7474
7402
118
125
100
119
78
110
129
147

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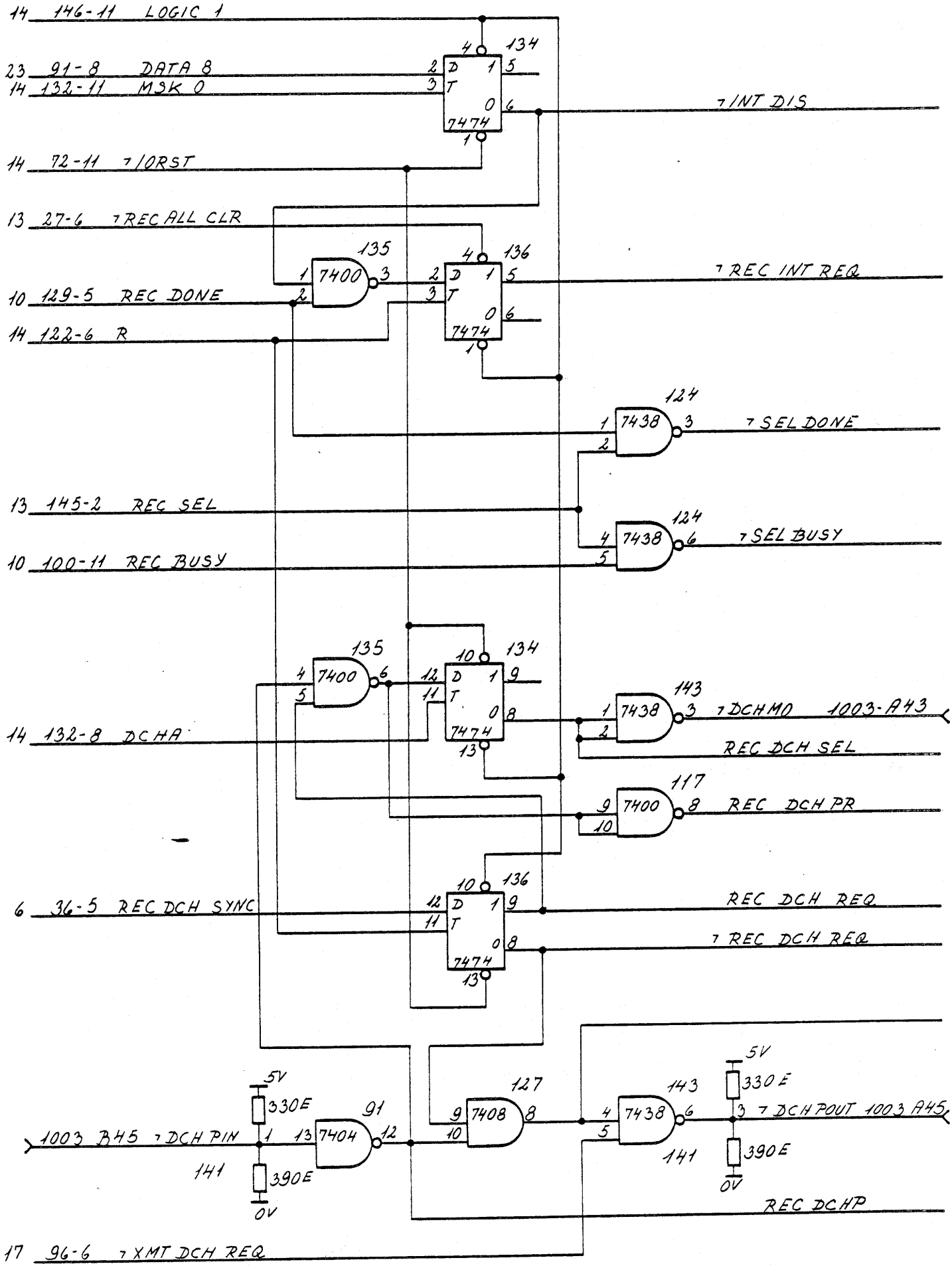
14 146-11 LOGIC 1
23 91-8 DATA 8
14 132-11 MSK 0
14 72-11 ⊽/ORST
13 27-6 ⊽REC ALL CLR
10 129-5 REC DONE
14 122-6 R
13 145-2 REC SEL
10 100-11 REC BUSY
14 132-8 DCHA
6 36-5 REC DCH SYNC
1003 B45 ⊽DCH PIN
17 96-6 ⊽XMT DCH REQ
134
135
136
124
143
117
91
127
141
7400
7474
7438
7404
7408
5V
330E
390E
0V
⊽/INT DIS
⊽REC INT REQ
⊽SEL DONE
⊽SEL BUSY
⊽DCHMO 1003-A43
REC DCH SEL
REC DCH PR
REC DCH REQ
⊽REC DCH REQ
⊽DCH POUT 1003 A45
REC DCHP

AAJ 10.4.79

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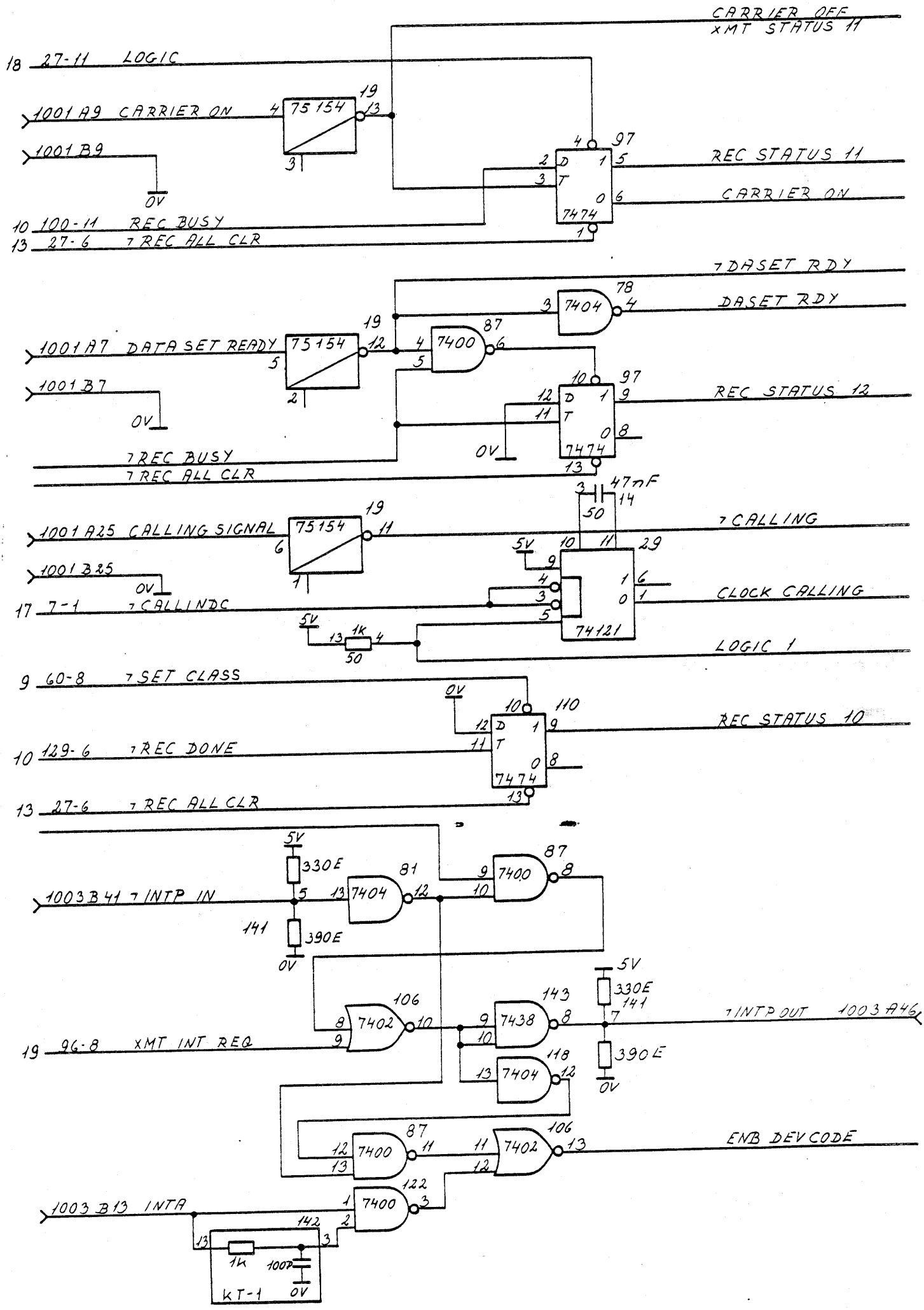

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SCC 705
R 12706

RECEIVER STATUS CONTROL

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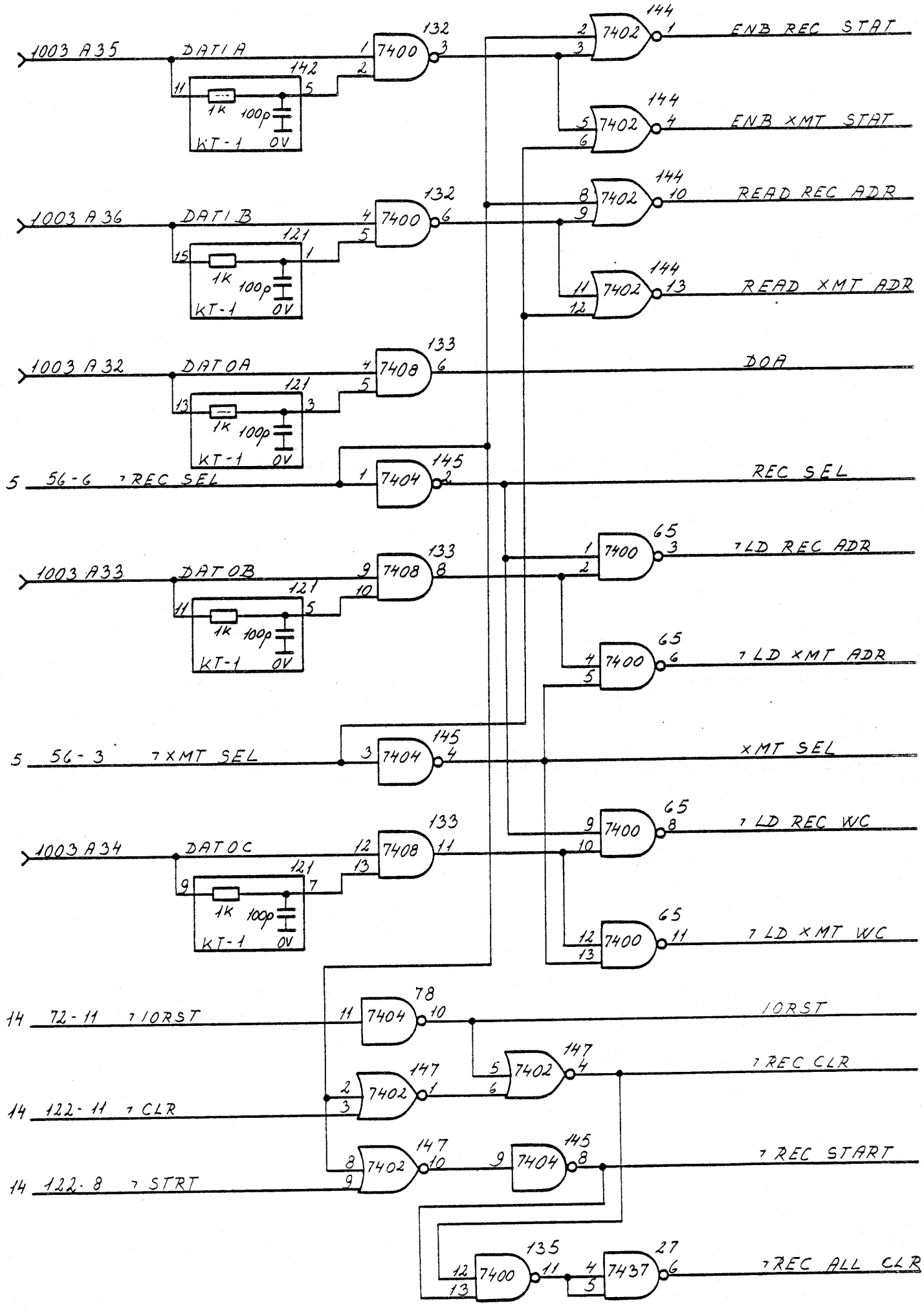
1003 A35
DATI A
7400
132
142
1K
100p
KT-1
0V
7402
144
ENB REC STAT
ENB XMT STAT
1003 A36
DATI B
121
READ REC ADR
READ XMT ADR
1003 A32
DATO A
7408
133
DOA
7404
145
5 56-6 ↗REC SEL
REC SEL
1003 A33
DATO B
7400
65
↗LD REC ADR
↗LD XMT ADR
5 56-3 ↗XMT SEL
XMT SEL
1003 A34
DATO C
↗LD REC WC
↗LD XMT WC
14 72-11 ↗IORST
78
IORST
↗REC CLR
14 122-11 ↗CLR
147
↗REC START
14 122-8 ↗STRT
135
7437
27
↗REC ALL CLR

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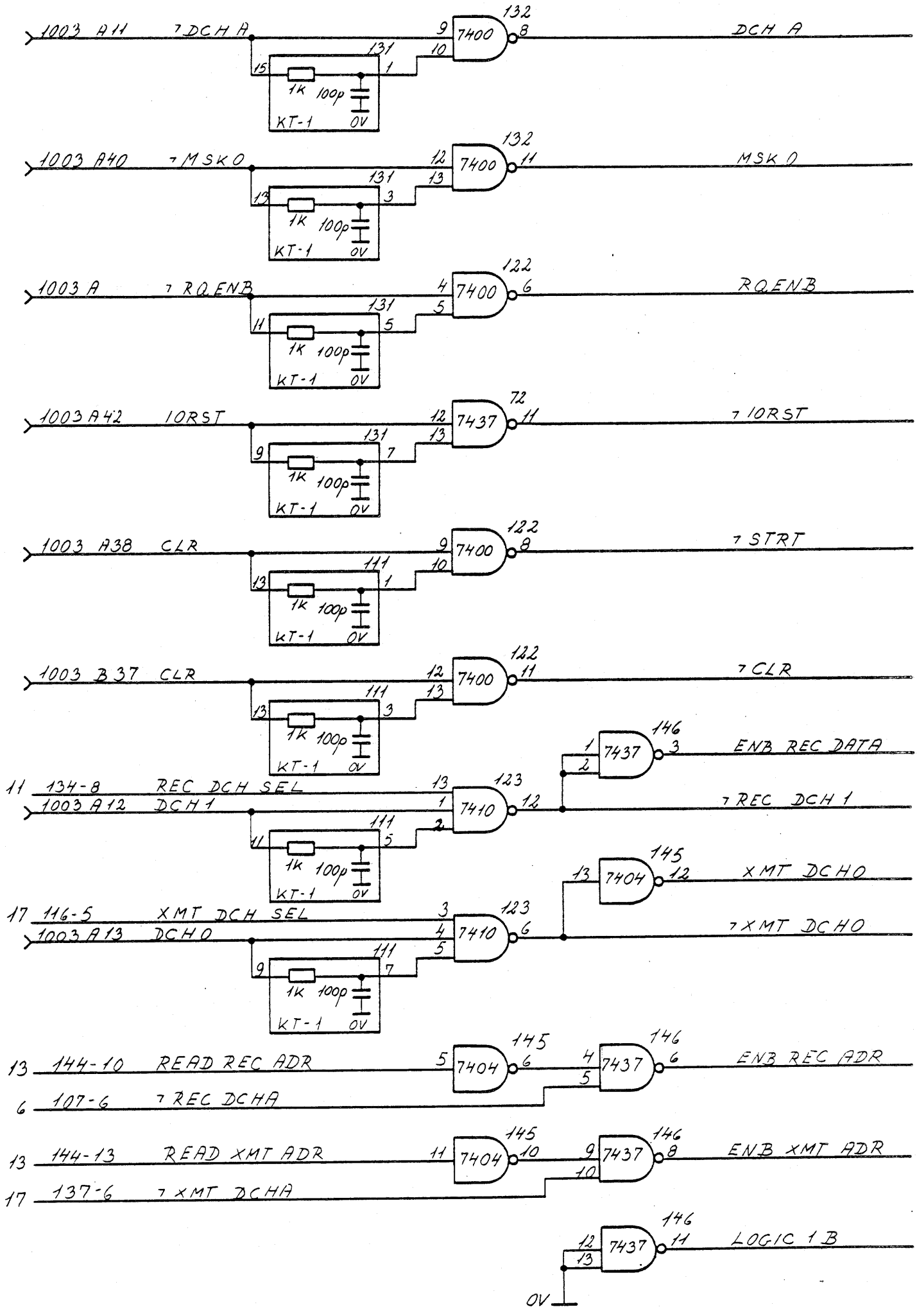
1003 A11 ⁊DCH A
DCH A
1003 A40 ⁊MSK 0
MSK 0
1003 A ⁊RQENB
RQENB
1003 A42 IORST
⁊IORST
1003 A38 CLR
⁊STRT
1003 B37 CLR
⁊CLR
11 134-8 REC DCH SEL
1003 A12 DCH 1
ENB REC DATA
⁊REC DCH 1
17 116-5 XMT DCH SEL
1003 A13 DCH 0
XMT DCH 0
⁊XMT DCH 0
13 144-10 READ REC ADR
6 107-6 ⁊REC DCHA
ENB REC ADR
13 144-13 READ XMT ADR
17 137-6 ⁊XMT DCHA
ENB XMT ADR
LOGIC 1 B
0V
1K 100p KT-1 0V
7400
7437
7410
7404

AAJ 10.4.79

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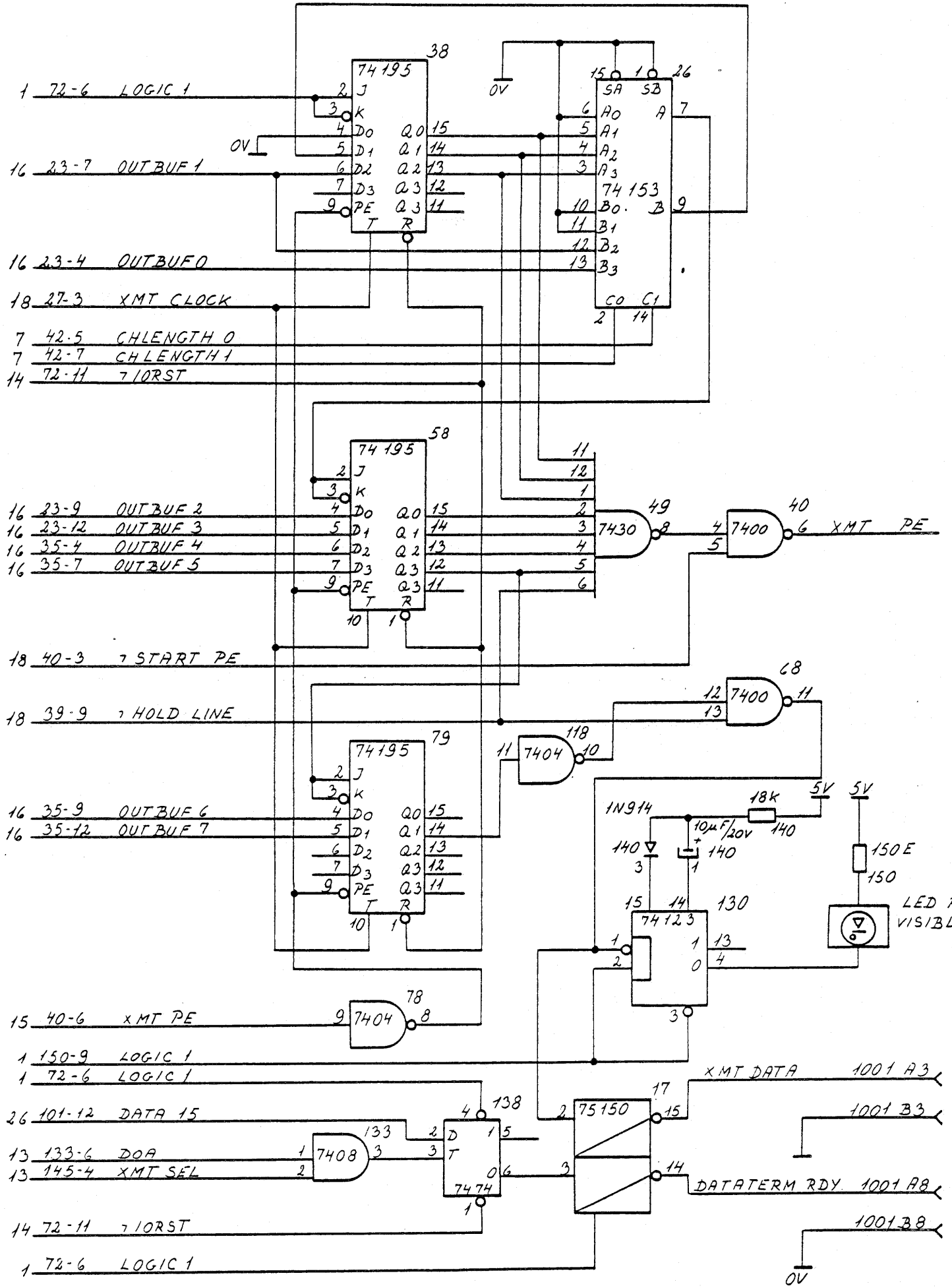

AAJ 10.4.79

SCC 705
R 12709

TRANSMITTER OUTPUT REGISTER

15

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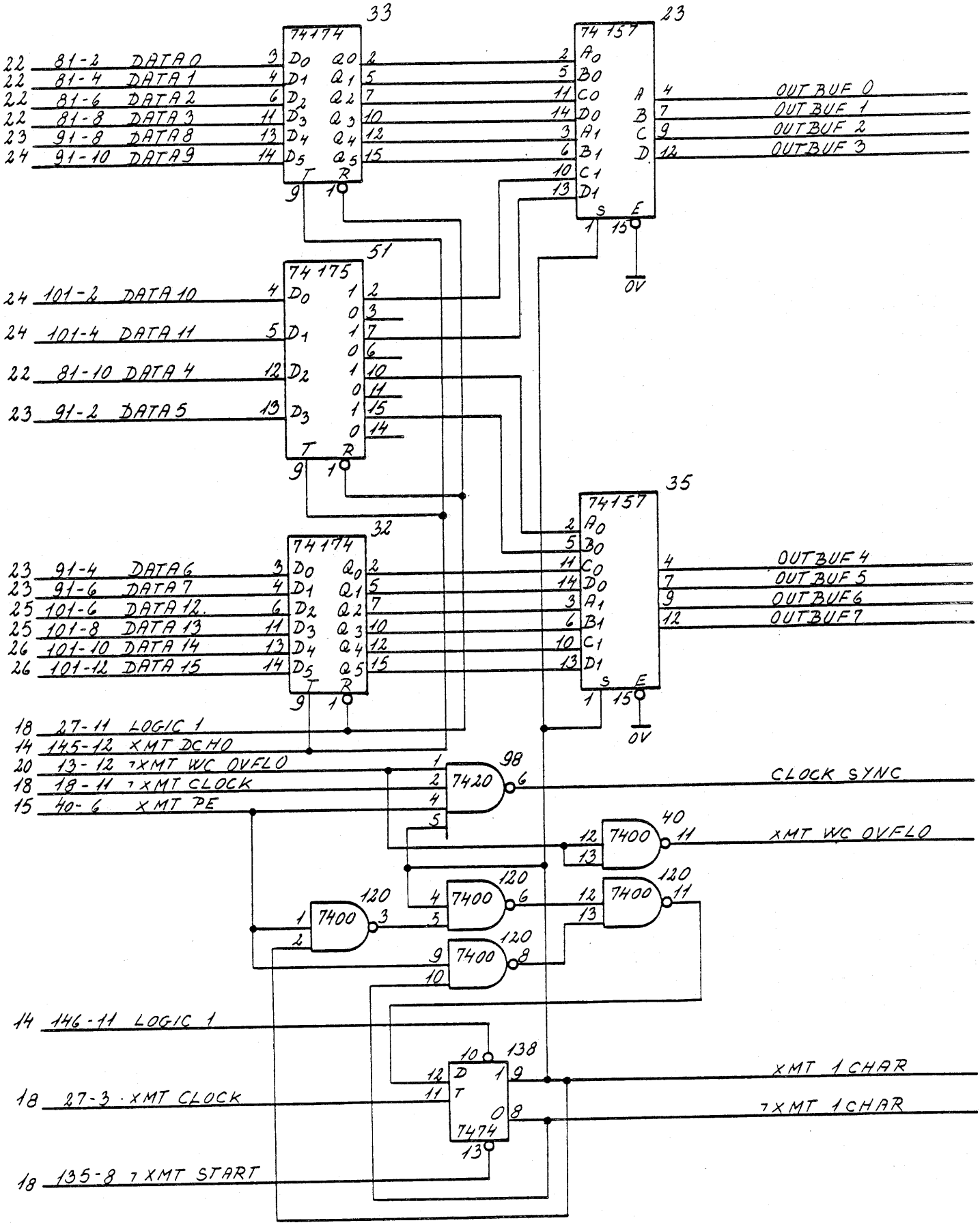

AAJ 10.4.79

SCC 705
R12710

TRANSMITTER INPUT BUFFER

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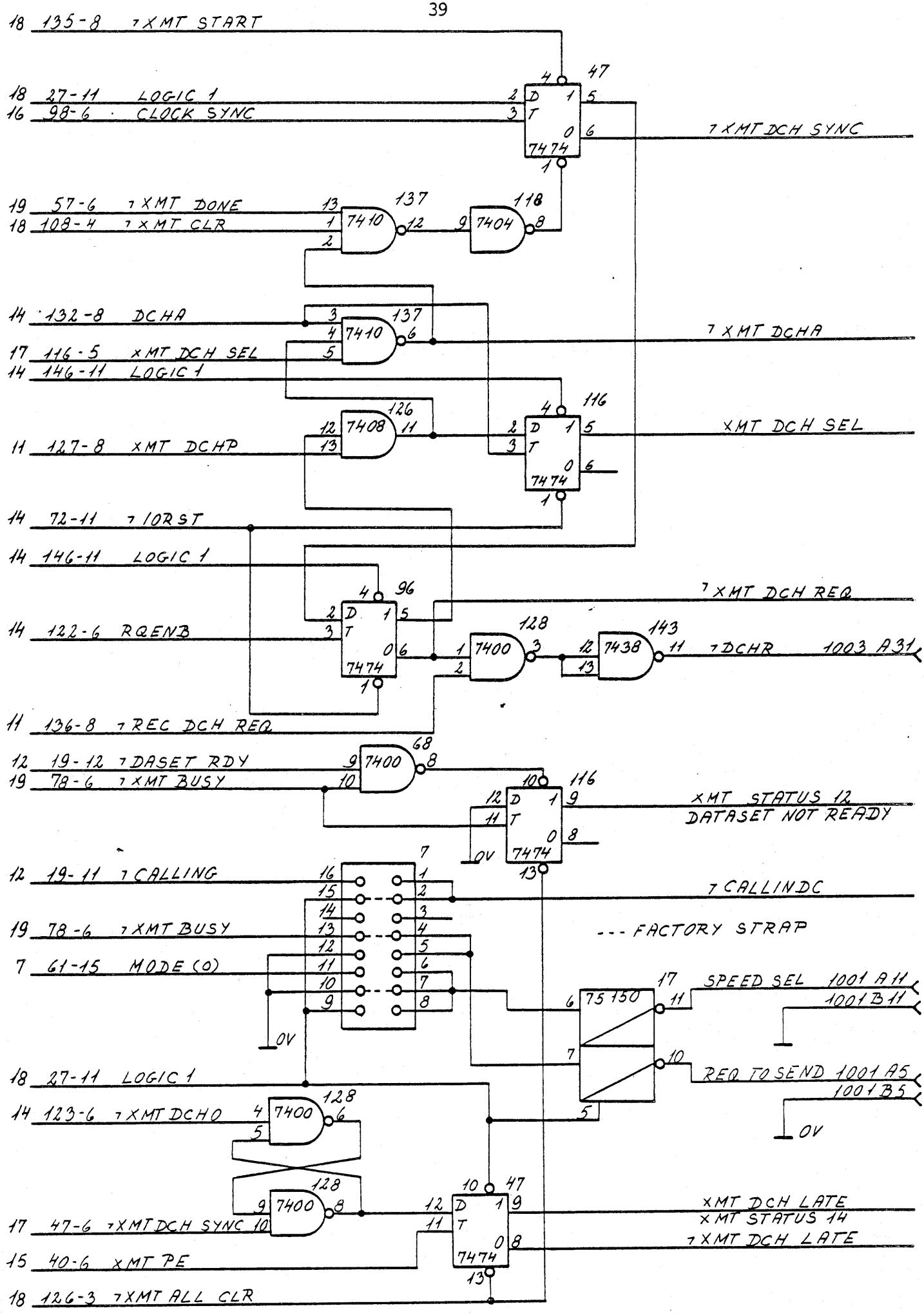
18 135-8 ⅂XMT START
18 27-11 LOGIC 1
16 98-6 CLOCK SYNC
47
7474
⅂XMT DCH SYNC
19 57-6 ⅂XMT DONE
18 108-4 ⅂XMT CLR
7410
137
7404
118
14 132-8 DCHA
⅂XMT DCHA
17 116-5 XMT DCH SEL
14 146-11 LOGIC 1
7408
126
11 127-8 XMT DCHP
116
XMT DCH SEL
14 72-11 ⅂IORST
14 146-11 LOGIC 1
96
⅂XMT DCH REQ
14 122-6 RQENB
7400
128
7438
143
⅂DCHR
1003 A31
11 136-8 ⅂REC DCH REQ
12 19-12 ⅂DASET RDY
19 78-6 ⅂XMT BUSY
68
XMT STATUS 12
DATASET NOT READY
0V
12 19-11 ⅂CALLING
⅂CALLINDC
19 78-6 ⅂XMT BUSY
--- FACTORY STRAP
7 61-15 MODE (0)
75150
SPEED SEL 1001 A11
1001 B11
REQ TO SEND 1001 A5
1001 B5
0V
18 27-11 LOGIC 1
14 123-6 ⅂XMT DCHO
17 47-6 ⅂XMT DCH SYNC
15 40-6 XMT PE
XMT DCH LATE
XMT STATUS 14
⅂XMT DCH LATE
18 126-3 ⅂XMT ALL CLR

AAJ 10.4.79

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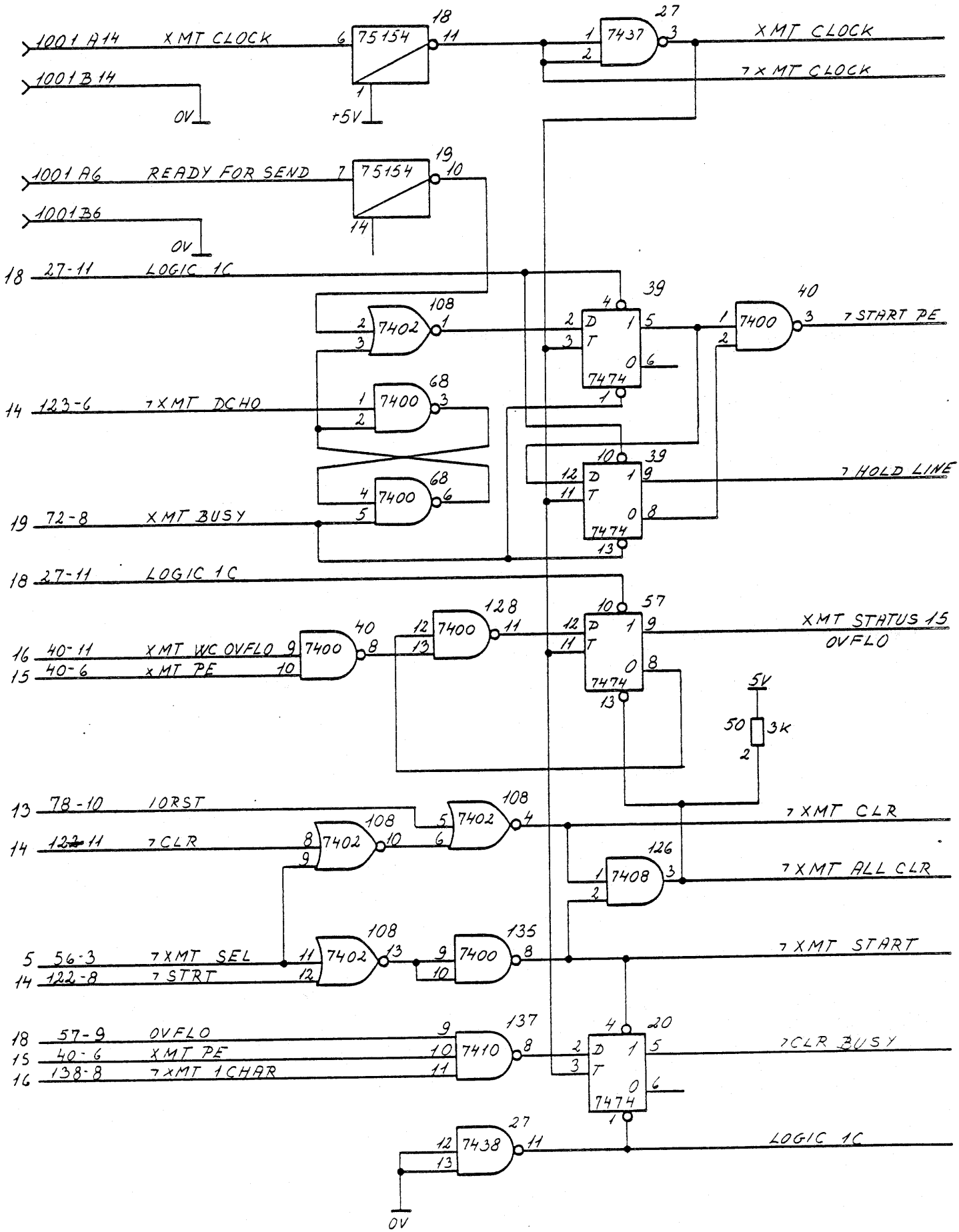

AAJ 10.4.79

SCC 705
R 12 7 12

TRANSMITTER CLOCK, CLEAR AND START SIGNALS

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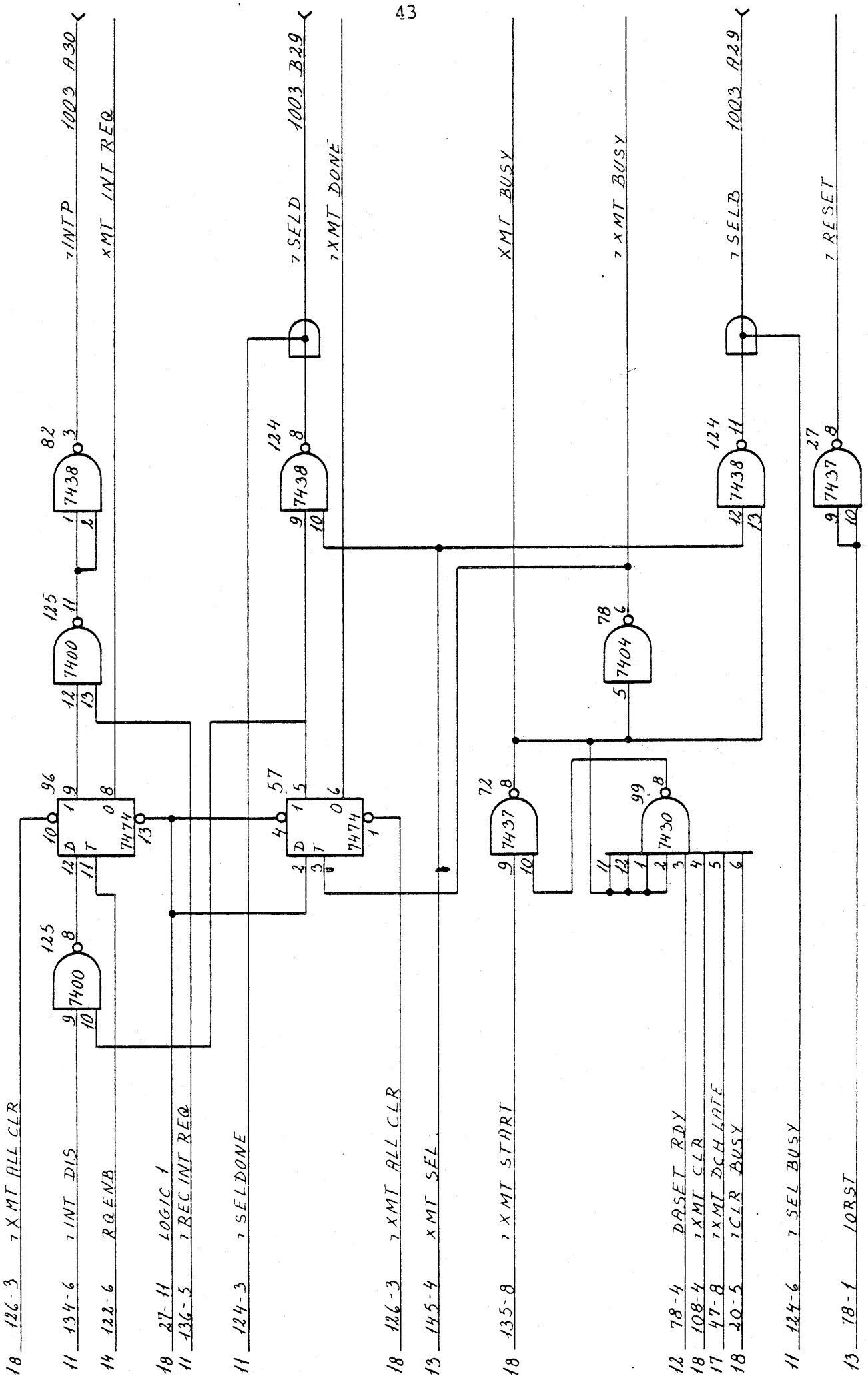

AAJ 10.4.79

SCC 705
R 12713

TRANSMITTER INTERRUPT CONTROL

19

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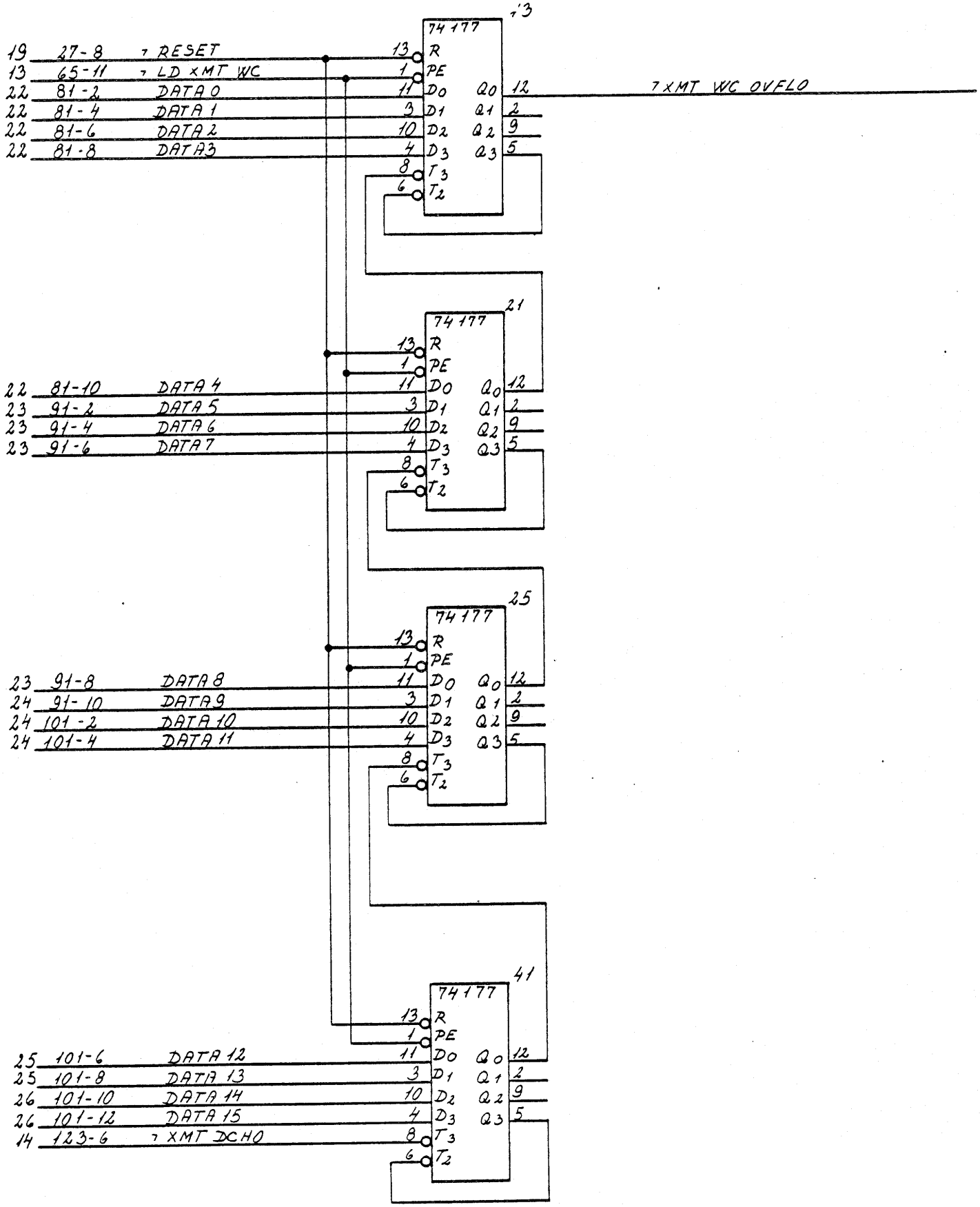
74177
13
R
1
PE
11
D0
3
D1
10
D2
4
D3
8
T3
6
T2
Q0
Q1
Q2
Q3
12
2
9
5
19 27-8 RESET
13 65-11 LD XMT WC
22 81-2 DATA 0
22 81-4 DATA 1
22 81-6 DATA 2
22 81-8 DATA 3
XMT WC OVFLO
22 81-10 DATA 4
23 91-2 DATA 5
23 91-4 DATA 6
23 91-6 DATA 7
23 91-8 DATA 8
24 91-10 DATA 9
24 101-2 DATA 10
24 101-4 DATA 11
25 101-6 DATA 12
25 101-8 DATA 13
26 101-10 DATA 14
26 101-12 DATA 15
14 123-6 XMT DCHO

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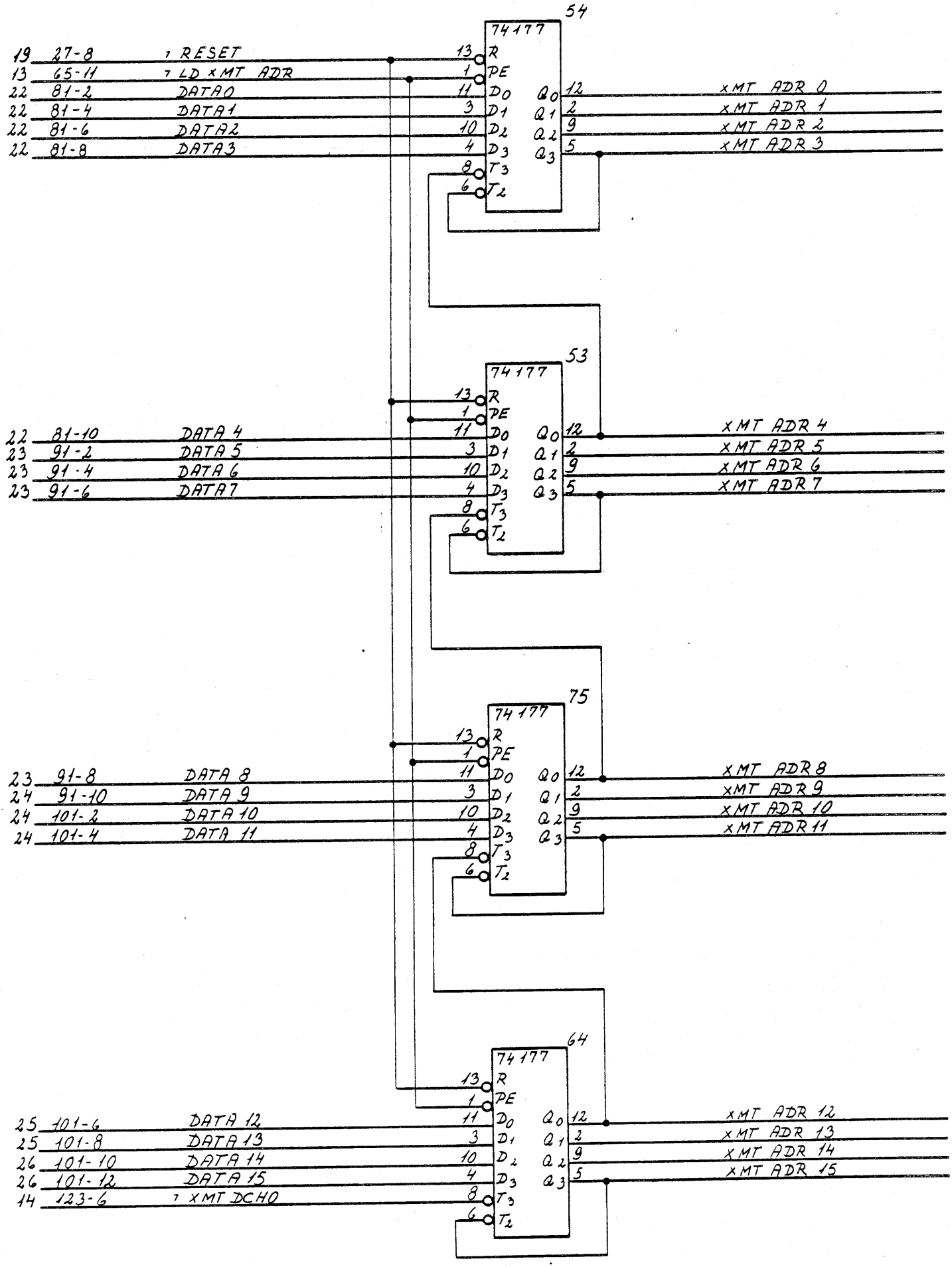
54
74177
19 27-8 ↑ RESET
13 65-11 ↑ LD XMT ADR
22 81-2 DATA0
22 81-4 DATA1
22 81-6 DATA2
22 81-8 DATA3
R
PE
D0
D1
D2
D3
T3
T2
Q0
Q1
Q2
Q3
XMT ADR 0
XMT ADR 1
XMT ADR 2
XMT ADR 3
53
74177
22 81-10 DATA 4
23 91-2 DATA 5
23 91-4 DATA 6
23 91-6 DATA 7
XMT ADR 4
XMT ADR 5
XMT ADR 6
XMT ADR 7
75
74177
23 91-8 DATA 8
24 91-10 DATA 9
24 101-2 DATA 10
24 101-4 DATA 11
XMT ADR 8
XMT ADR 9
XMT ADR 10
XMT ADR 11
64
74177
25 101-6 DATA 12
25 101-8 DATA 13
26 101-10 DATA 14
26 101-12 DATA 15
14 123-6 ↑ XMT DCHO
XMT ADR 12
XMT ADR 13
XMT ADR 14
XMT ADR 15

AAJ 10.4.79

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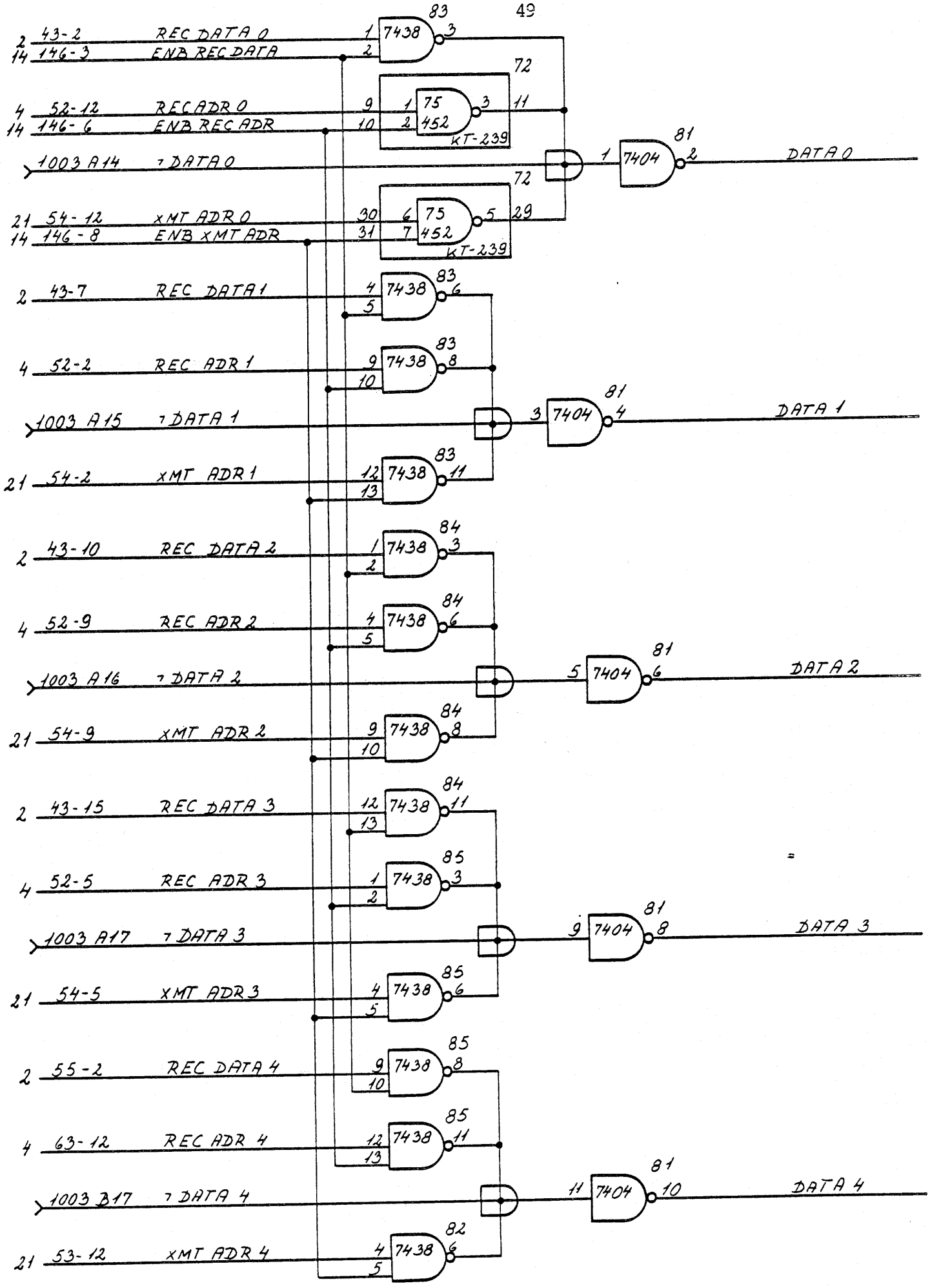
83
43-2 REC DATA 0
146-3 ENB REC DATA
7438
72
52-12 REC ADR 0
146-6 ENB REC ADR
75 452
KT-239
1003 A14 ⊐ DATA 0
81
7404
DATA 0
54-12 XMT ADR 0
146-8 ENB XMT ADR
43-7 REC DATA 1
52-2 REC ADR 1
1003 A15 ⊐ DATA 1
DATA 1
54-2 XMT ADR 1
84
43-10 REC DATA 2
52-9 REC ADR 2
1003 A16 ⊐ DATA 2
DATA 2
54-9 XMT ADR 2
43-15 REC DATA 3
85
52-5 REC ADR 3
1003 A17 ⊐ DATA 3
DATA 3
54-5 XMT ADR 3
55-2 REC DATA 4
63-12 REC ADR 4
1003 B17 ⊐ DATA 4
DATA 4
82
53-12 XMT ADR 4

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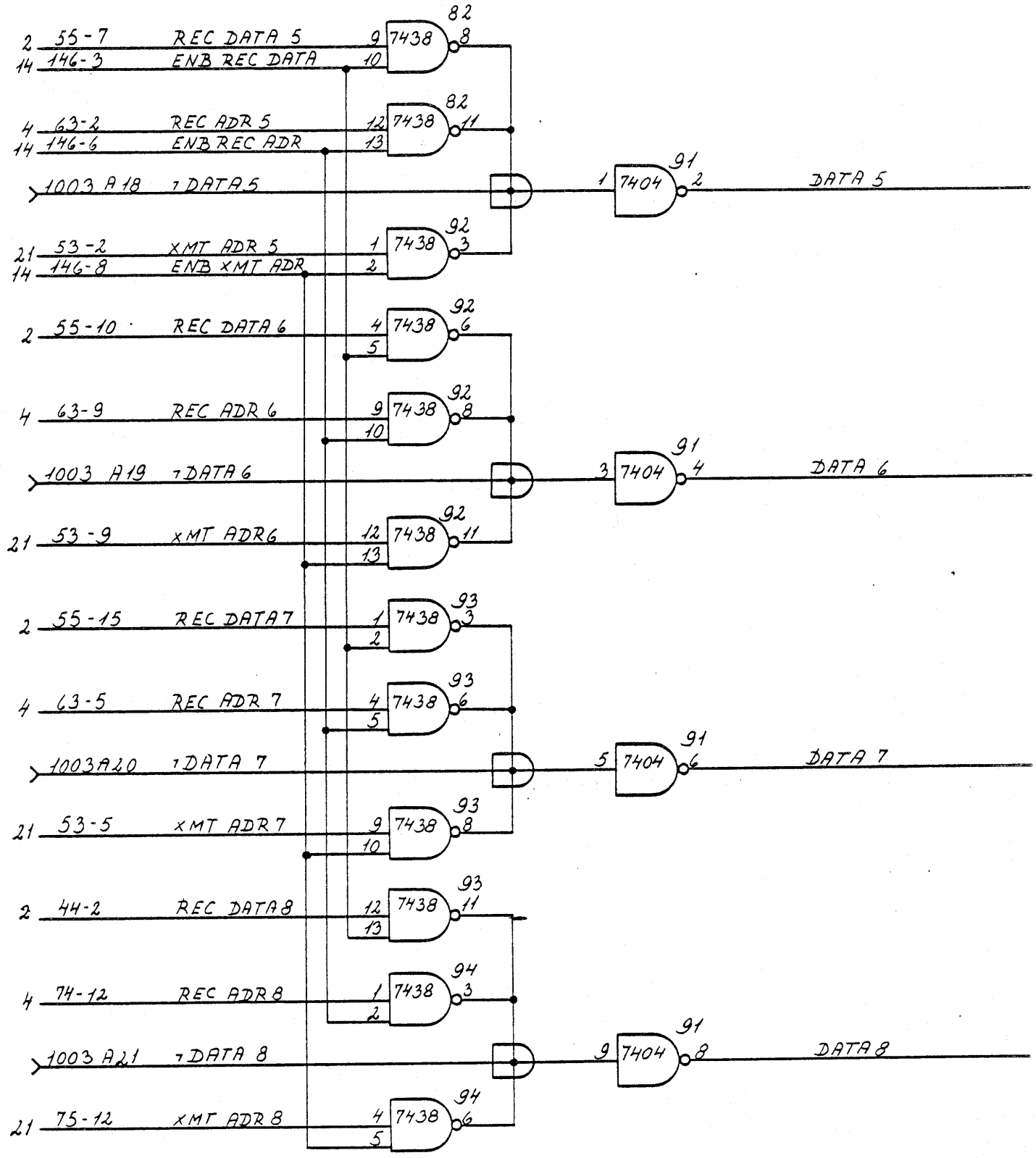
2 55-7 REC DATA 5
14 146-3 ENB REC DATA
82 9 10 7438 8
4 63-2 REC ADR 5
14 146-6 ENB REC ADR
82 12 13 7438 11
1003 A18 ↑DATA 5
91 1 7404 2 DATA 5
21 53-2 XMT ADR 5
14 146-8 ENB XMT ADR
92 1 2 7438 3
2 55-10 REC DATA 6
92 4 5 7438 6
4 63-9 REC ADR 6
92 9 10 7438 8
1003 A19 ↑DATA 6
91 3 7404 4 DATA 6
21 53-9 XMT ADR6
92 12 13 7438 11
2 55-15 REC DATA 7
93 1 2 7438 3
4 63-5 REC ADR 7
93 4 5 7438 6
1003A20 ↑DATA 7
91 5 7404 6 DATA 7
21 53-5 XMT ADR 7
93 9 10 7438 8
2 44-2 REC DATA 8
93 12 13 7438 11
4 74-12 REC ADR 8
94 1 2 7438 3
1003 A21 ↑DATA 8
91 9 7404 8 DATA 8
21 75-12 XMT ADR 8
94 4 5 7438 6

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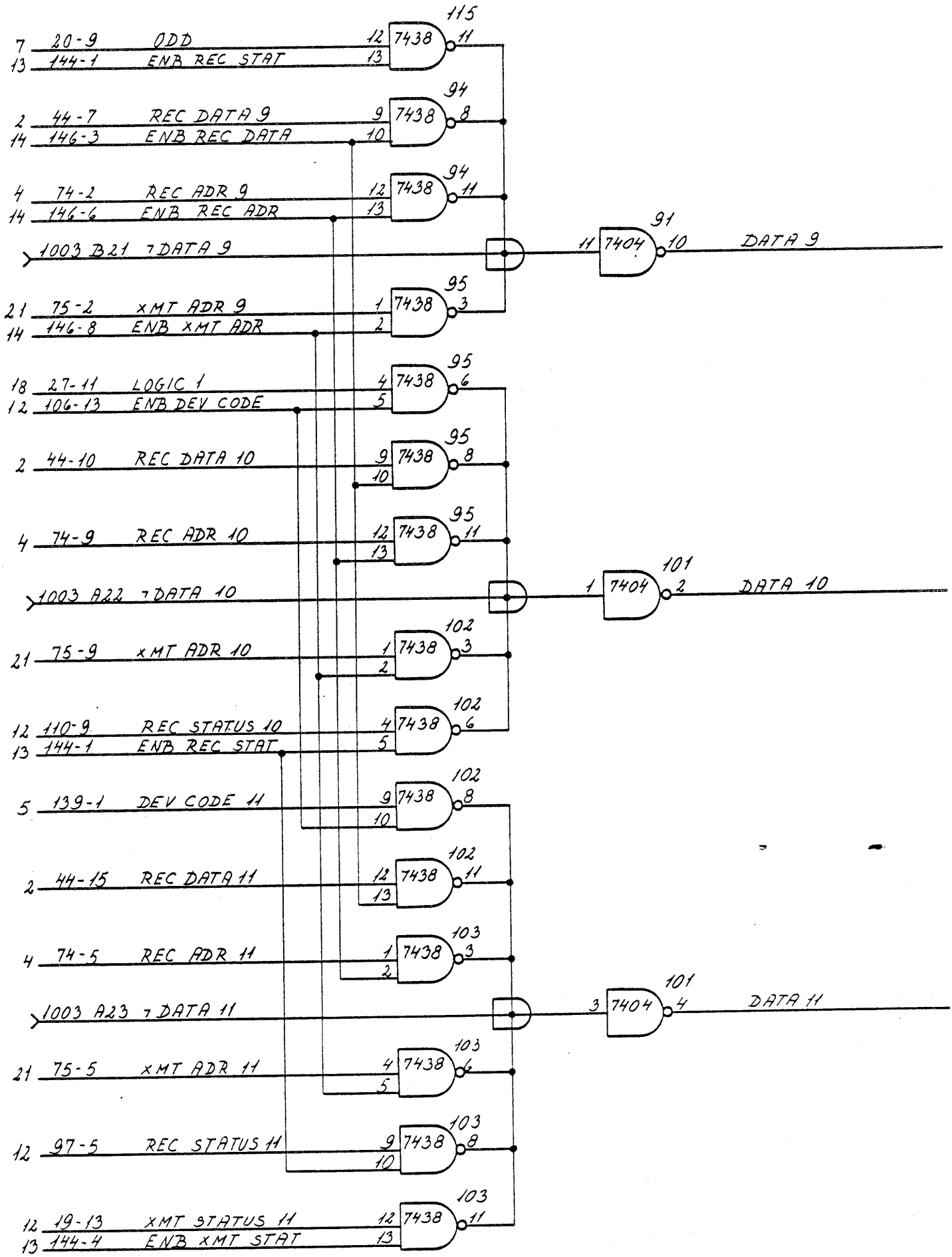
115
7 20-9 ODD
13 144-1 ENB REC STAT
12 13 7438 11
94
2 44-7 REC DATA 9
14 146-3 ENB REC DATA
9 10 7438 8
94
4 74-2 REC ADR 9
14 146-6 ENB REC ADR
12 13 7438 11
91
1003 B21 ⅂DATA 9
11 7404 10 DATA 9
95
21 75-2 XMT ADR 9
14 146-8 ENB XMT ADR
1 2 7438 3
95
18 27-11 LOGIC 1
12 106-13 ENB DEV CODE
4 5 7438 6
95
2 44-10 REC DATA 10
9 10 7438 8
95
4 74-9 REC ADR 10
12 13 7438 11
101
1003 A22 ⅂DATA 10
1 7404 2 DATA 10
102
21 75-9 XMT ADR 10
1 2 7438 3
102
12 110-9 REC STATUS 10
13 144-1 ENB REC STAT
4 5 7438 6
102
5 139-1 DEV CODE 11
9 10 7438 8
102
2 44-15 REC DATA 11
12 13 7438 11
103
4 74-5 REC ADR 11
1 2 7438 3
101
1003 A23 ⅂DATA 11
3 7404 4 DATA 11
103
21 75-5 XMT ADR 11
4 5 7438 6
103
12 97-5 REC STATUS 11
9 10 7438 8
103
12 19-13 XMT STATUS 11
13 144-4 ENB XMT STAT
12 13 7438 11

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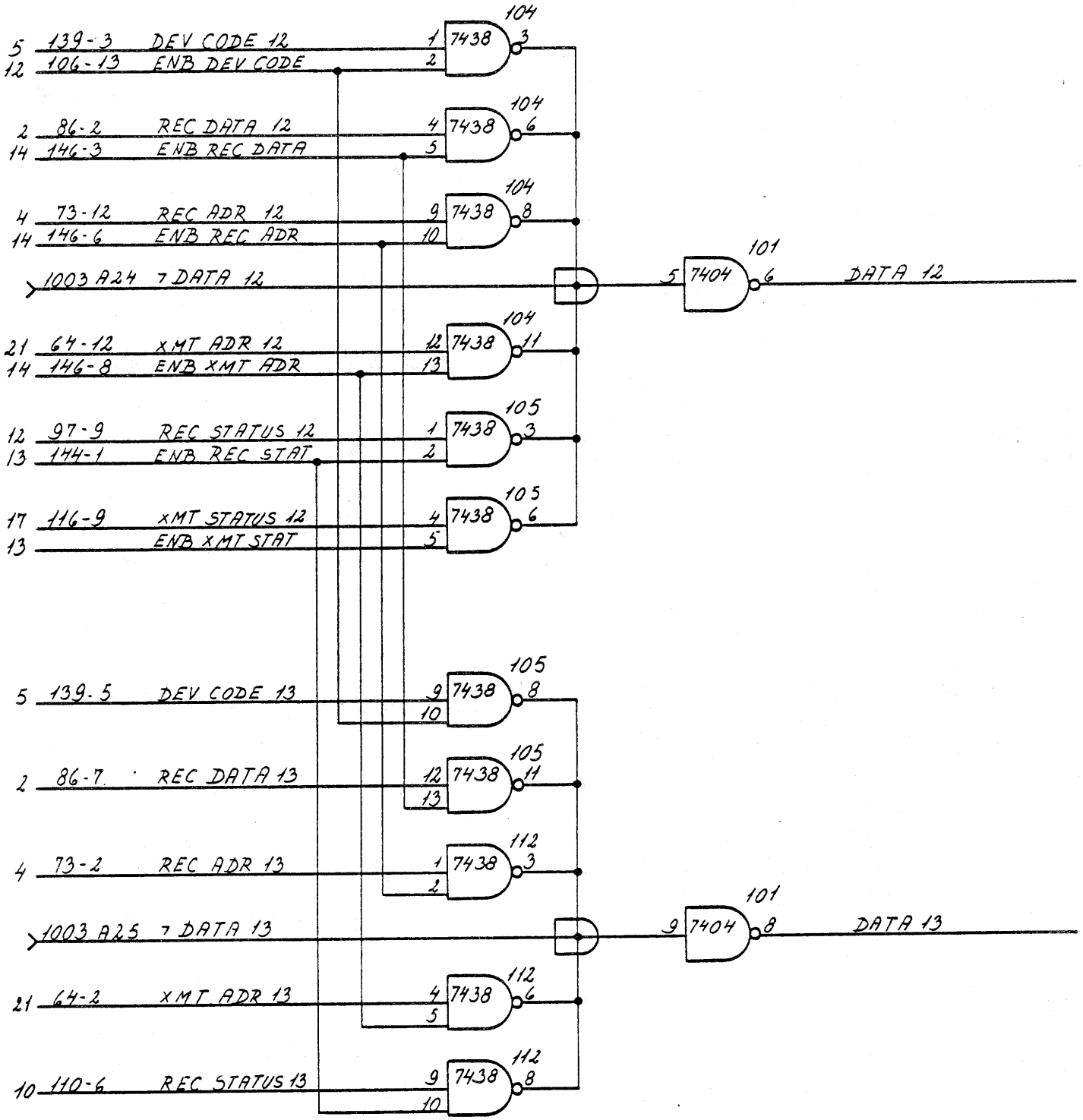
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5 139-3 DEV CODE 12
12 106-13 ENB DEV CODE
1
2
7438
3
104
2 86-2 REC DATA 12
14 146-3 ENB REC DATA
4
5
7438
6
104
4 73-12 REC ADR 12
14 146-6 ENB REC ADR
9
10
7438
8
101
1003 A24 7 DATA 12
5
7404
6
DATA 12
104
21 64-12 XMT ADR 12
14 146-8 ENB XMT ADR
12
13
7438
11
105
12 97-9 REC STATUS 12
13 144-1 ENB REC STAT
1
2
7438
3
105
17 116-9 XMT STATUS 12
13 ENB XMT STAT
4
5
7438
6
105
5 139-5 DEV CODE 13
9
10
7438
8
105
2 86-7 REC DATA 13
12
13
7438
11
112
4 73-2 REC ADR 13
1
2
7438
3
101
1003 A25 7 DATA 13
9
7404
8
DATA 13
112
21 64-2 XMT ADR 13
4
5
7438
6
112
10 110-6 REC STATUS 13
9
10
7438
8

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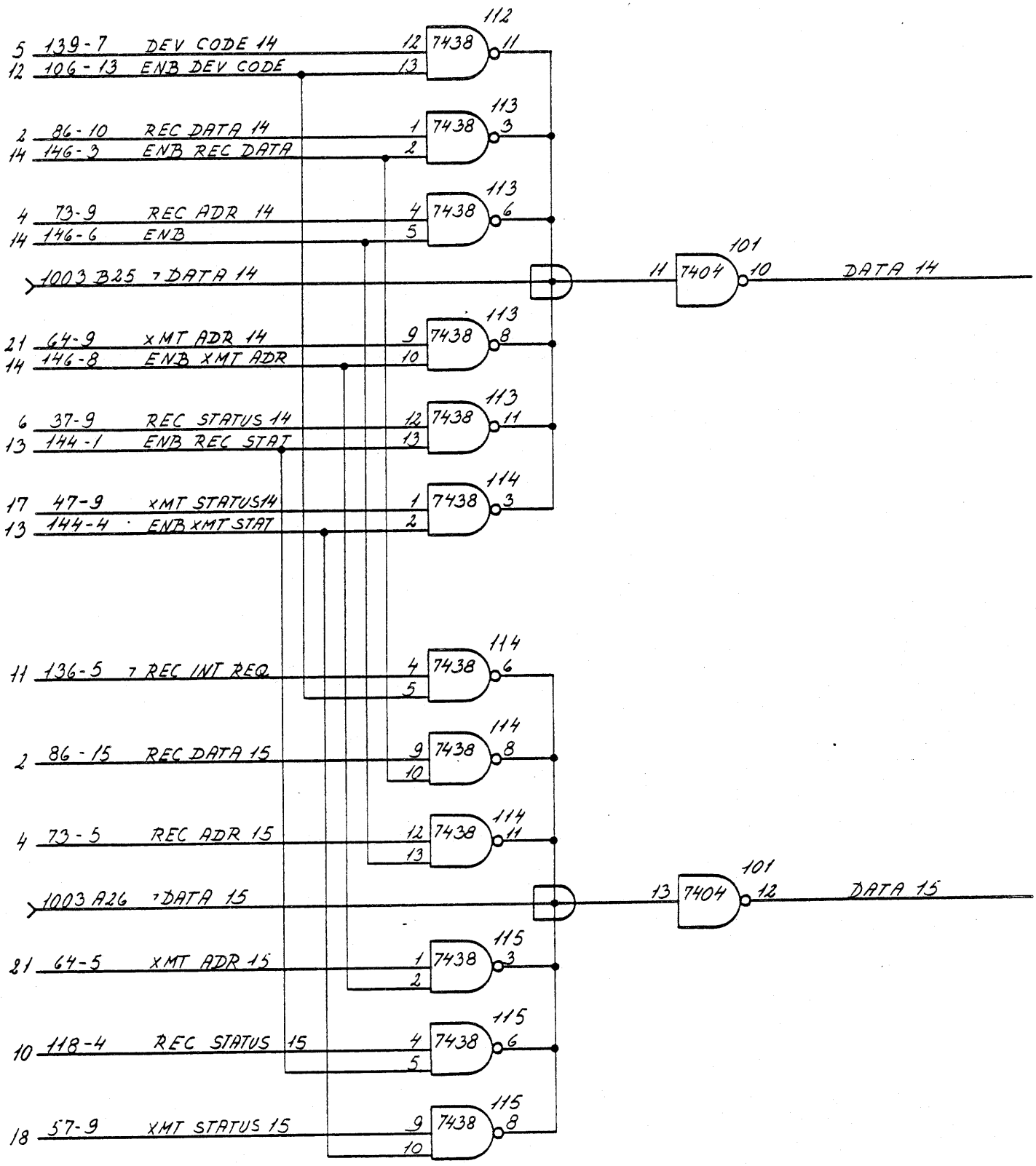
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5 139-7 DEV CODE 14
12 106-13 ENB DEV CODE
12 7438 11
113
2 86-10 REC DATA 14
14 146-3 ENB REC DATA
1 7438 3
113
4 73-9 REC ADR 14
14 146-6 ENB
4 7438 6
5
101
1003 B25 ▽DATA 14
11 7404 10 DATA 14
113
21 64-9 XMT ADR 14
14 146-8 ENB XMT ADR
9 7438 8
10
113
6 37-9 REC STATUS 14
13 144-1 ENB REC STAT
12 7438 11
13
114
17 47-9 XMT STATUS14
13 144-4 ENB XMT STAT
1 7438 3
2
114
11 136-5 ▽REC INT REQ
4 7438 6
5
114
2 86-15 REC DATA 15
9 7438 8
10
114
4 73-5 REC ADR 15
12 7438 11
13
101
1003 A26 ▽DATA 15
13 7404 12 DATA 15
115
21 64-5 XMT ADR 15
1 7438 3
2
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10 118-4 REC STATUS 15
4 7438 6
5
115
18 57-9 XMT STATUS 15
9 7438 8
10

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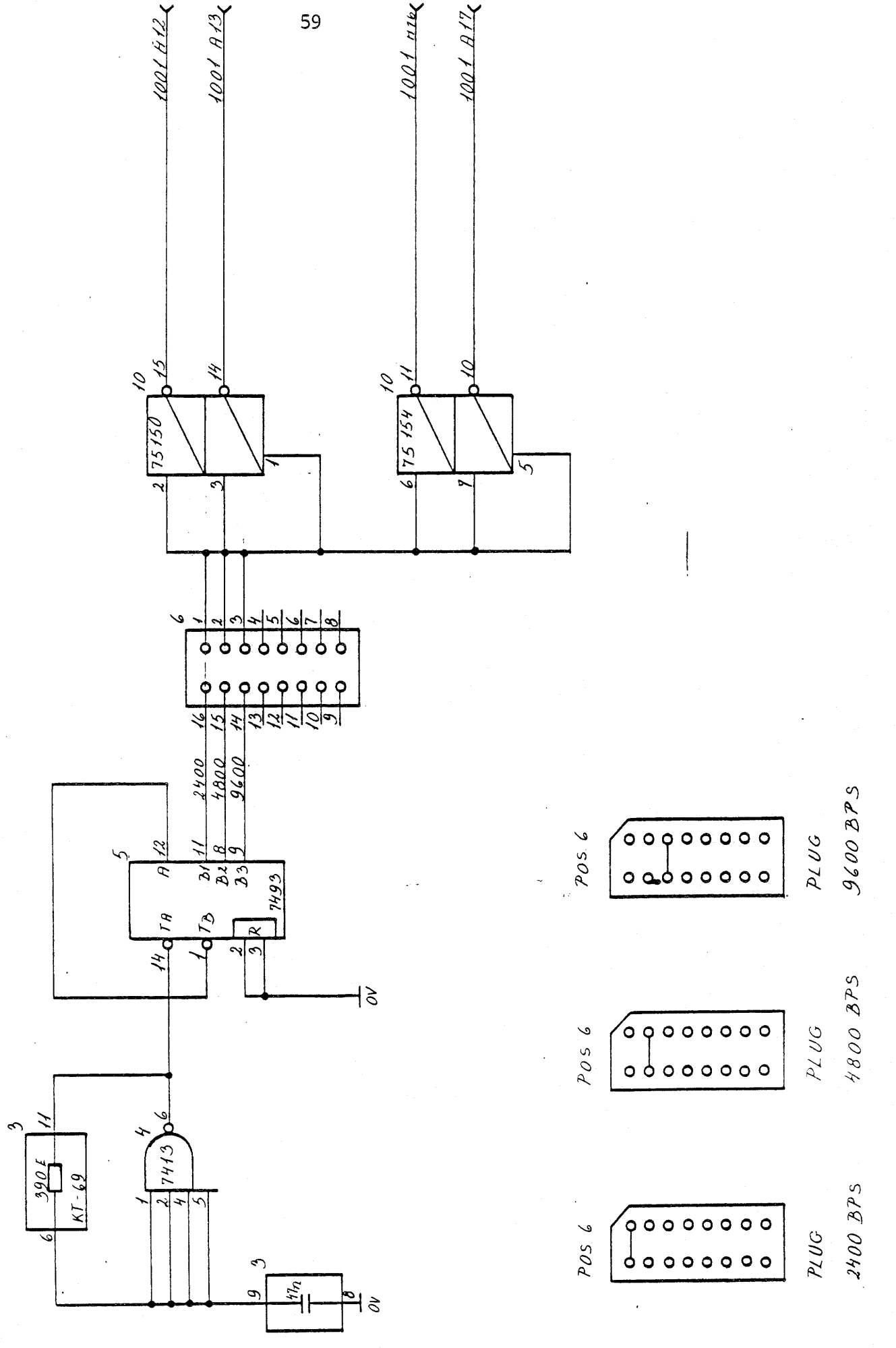

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