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Title:

SCC 705/706
BINARY SYNCHRONOUS COMMUNICATIONS CONTROLLER
Programmer's Reference Manual

Keywords:

SCC 705, SCC 706, BSC

Abstract:

This paper describes the features and the logical structure of the receiver and the transmitter in a binary synchronous communications controller, the SCC 706.

(26 printed pages)

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1. MAIN CHARACTERISTICS

1.

1.1 Description

1.1

The SCC 705/706 is a binary synchronous communication controller consisting of a receiver and a transmitter.

Basically it is two separate controllers each with its own control logics, intended to operate in full or half duplex mode.

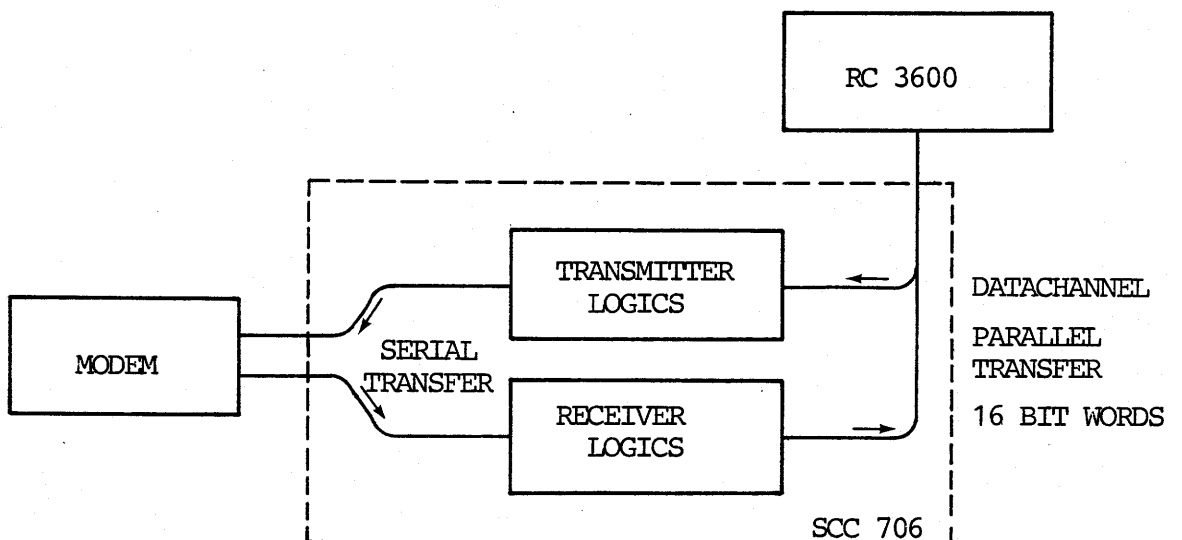
1.2 Data Formats

1.2

The SCC 705/706 receiver transfers information to the computer memory through the datachannel.

Each 16 bit word contains two 6, 7 or 8 bit characters. The bits are received from the modem in serial way with the least significant bit (LSB) received first.

The SCC 705/706 transmitter operates in a similar way but in the other direction of course.



Data Formats

Fig. 1.1

1.3 Applicable Documents

1.3

For further information about the RC3600-computer, refer to RC-3603 Reference Manual and concerning the technical structure of the datatransmission set refer to

C.C.I.T.T Recommendation V.24: "FUNCTIONS AND ELECTRICAL CHARACTERISTICS OF CIRCUITS AT THE INTERFACE BETWEEN DATA TERMINAL EQUIPMENT AND DATA COMMUNICATION EQUIPMENT".

2. PERFORMANCE SPECIFICATIONS

2.

2.1 Transmission Speed

2.1

As the communications controller not contains any clocksource, the transmission speed alone depends on the modem in use.

The controller, however, accepts any clockfrequency until 20 kHz.

If the modem has option for remote speed selection, e.g. 600/1200 or 4800/9600 BPS then it is possible to select the speed from the controller, either hardwired, or selected by the software.

2.2 Interface Specifications

2.2

All data- and controlsignals between modem and the communications controller is in accordance to the C.C.I.T.T. recommendation V.-24, which defines the interchange circuits, here the 100-series.

Following circuits are present:

- Circuit 101 - Protective ground or earth
- 102 - Signal ground or common return
- 103 - Transmitted data
- 104 - Received data
- 105 - Request to send
- 106 - Ready for sending
- 107 - Data set ready
- 108/2- Data terminal ready
- 109 - Data channel received line signal detector
- 111 - Data signaling rate selector
- 114 - Transmitter signal element timing
- 115 - Receiver signal element timing
- 125 - Calling indicator

3. RECEIVER OPERATION

3.

Setting BUSY causes the receiver to monitor the received bit stream continuously until it receives two consecutive SYN-characters. This synchronizes the receiver to the bit stream. When a character different from the SYN-character is received the receiver begins assembling pairs of characters into words which are transferred to the memory locations specified by the address counter. From this point the operation of the receiver depends on the receiver mode specified by bits 4 and 5 of the control word. See also flow diagram on the following page for description of receiver operation.

Control Word(4,5) = 0,0

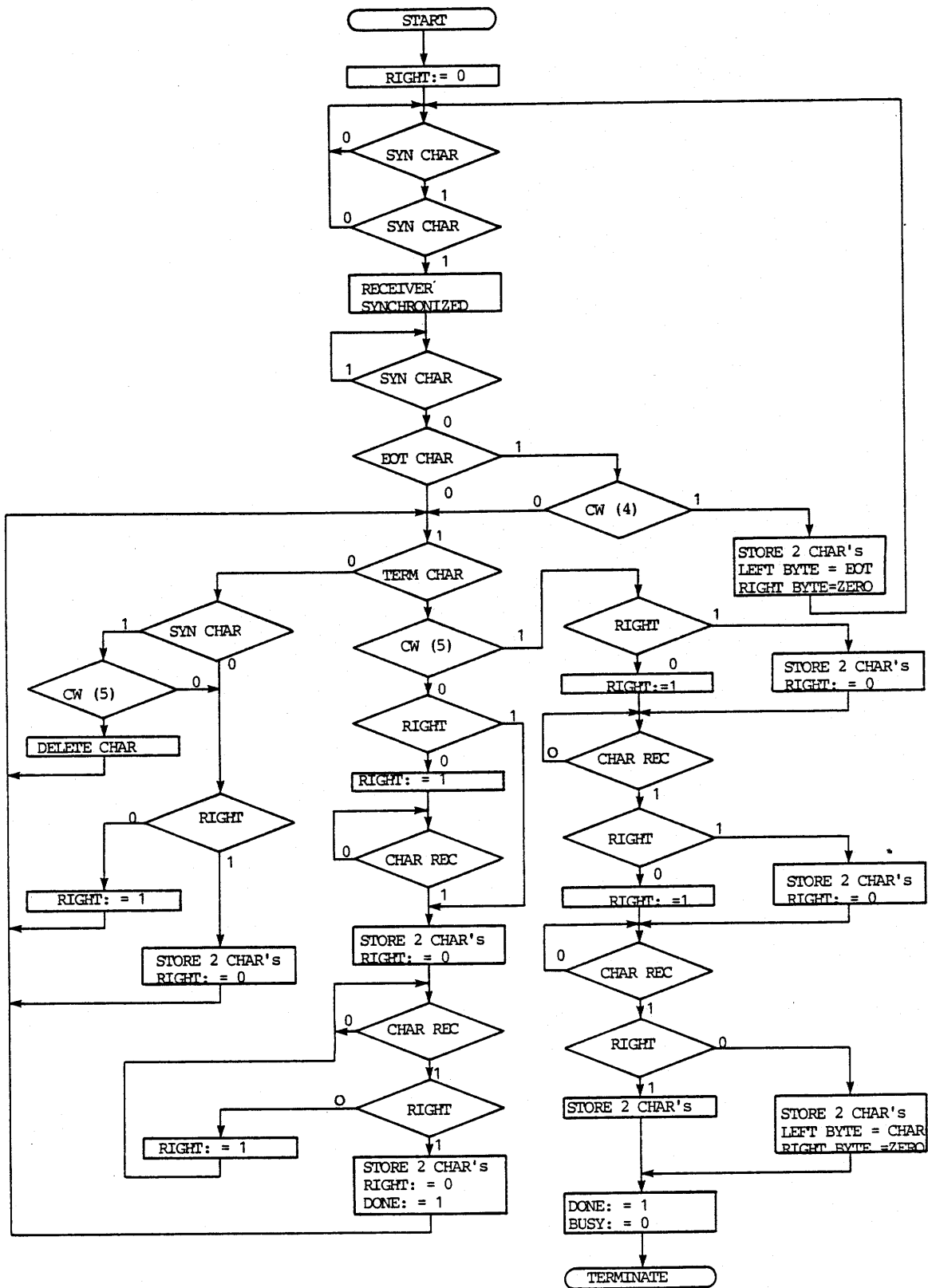
When a TERM character is received the receiver sets DONE after reception of further 2 or 3 characters depending on whether the TERM character is stored in the left or right byte of a word. The receiver remains synchronized and reception continues until termination occurs, e.g. by word count overflow.

Control Word(4,5) = 0,1

In this mode of operation SYN-characters are deleted by the receiver and are not stored. When a TERM-character is received the receiver receives 2 more characters before it terminates reception, sets DONE and clears BUSY. If the last stored word only contains one character, the right byte contains zeros and the character pointer is set to 1.

Control Word(4,5) = 1,0

If the first character received after synchronization is an EOT-character, the receiver will resynchronize, i.e. begin to look for 2 consecutive SYN-characters. The received EOT-character is stored in the left byte of the memory location addressed by the address counter. The right byte is set to zero.



RECEIVER FLOW DIAGRAM

If an EOT-character is not received as the first character after synchronization, operation of the receiver is identical to the operation for control word (4,5) = 0,0.

Control Word(4,5) = 1,1

If the first character received after synchronization is an EOT-character, the receiver will resynchronize, i.e. begin to look for 2 consecutive SYN-characters. The received EOT-character is stored in the left byte of the memory location addressed by the address counter. The right byte is set to zero. If an EOT-character is not received as the first character after synchronization, operation of the receiver is identical to the operation for control word(4,5) = 0,1.

3.1 Device Selection

3.1

The receiver is controlled from the CPU by means of I/O instructions. BUSY and DONE are controlled by bit (8) & (9) (Function Field) in all I/O instructions with the selected device code. The device code is alterable from 40 to 74 (octal) and the receiver will always get an even number - the transmitter the following odd number.

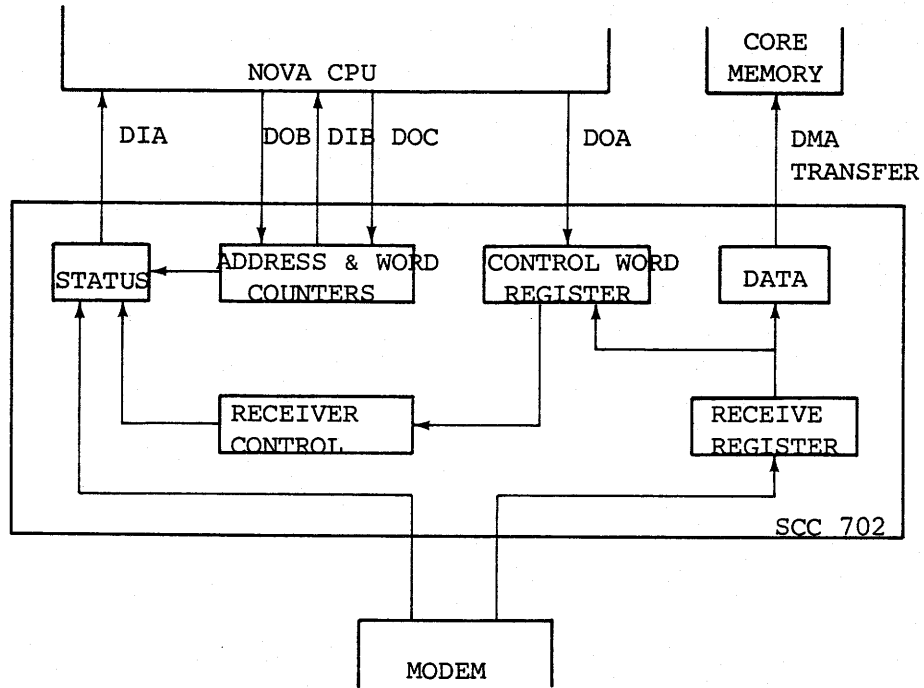
Interrupt Disable is controlled by interrupt priority mask bit (8).

The CLR function (F = 10) clears BUSY and DONE. SIRT (F = 01) sets BUSY and clears DONE and a reception will last as long as it is not terminated as described in 3.5.

In such case BUSY is cleared and DONE is set causing an interrupt if Interrupt Disable is clear.

The P function (F = 11) is not used.

The IORST instruction clears BUSY, DONE, and all the control logics.



Receiver Survey Diagram

Fig. 3.1

3.2 Address and Word counters

3.2

3.2.1 Address Counter

3.2.1

The DOB AC, REC instruction loads the address counter with the contents of AC - i.e. the 16 bit address for the location in the memory where the first two received characters are to be stored. Fig. 3.2.

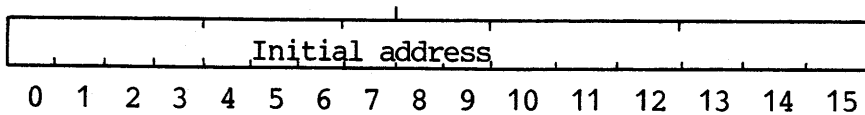


Fig. 3.2

When the reception begins, the address counter is incremented by one every time two characters are stored as a word in the memory.

In this way the contents of the address counter is one greater than the address of the previous stored word if termination occurs.

This address can be read at any time by DIB AC, REC instruction and thus determine the length of an unknown blok. Fig. 3.3.

The DIB instruction will not alter the contents of the address counter.

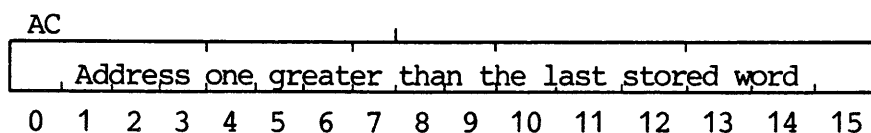


Fig. 3.3

3.2.2 The Word Counter

3.2.2

The DOC AC, REC instruction loads the word counter with the contents of AC - i.e. the 16 bit negative word count. (two's complement) Fig. 3.4.

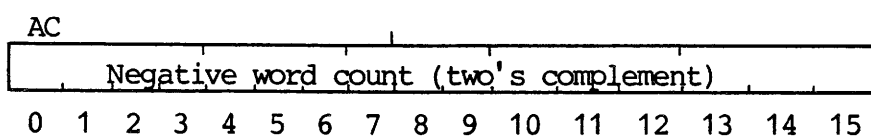


Fig. 3.4

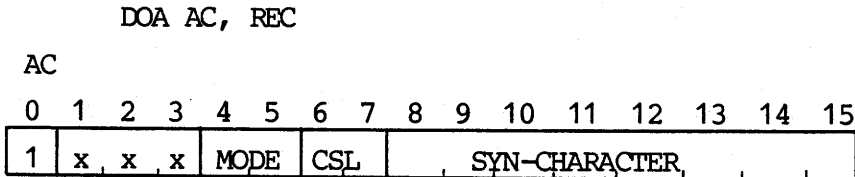
The word counter is incremented together with the address counter, and if overflow occurs, the reception is terminated. (Ref. 3.5.5.)

Before a receiving operation can take place, the word counter must be preset to the desired (negative) block length.

3.3 Controlword Register

The receiver is controlled by the contents of the control word register.

It is loaded by a DOA AC, REC instruction in the following manner:



Bit 4 and 5 determine the receiver mode.

3.3.1 Character set Length (CSL)

3.3.1

The receiver can handle 6, 7 or 8-bit characters i.e. the bits in a received character are right adjusted in the hardware.

Bit 6 and 7 in the control word determine the character length both in the receiver and the transmitter.

Character length	bit(6,7)
6 bits	(1,0)
7 bits	(0,1)
8 bits	(1,1)

3.3.2 SYN - Character

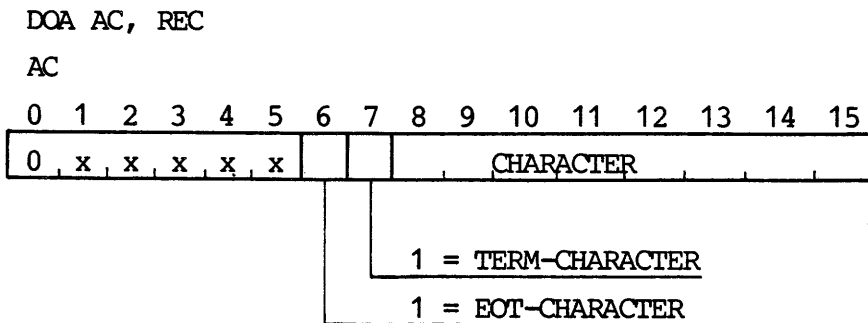
3.3.2

The SYN - character in the controlword bit 8-15 determines which character the receiver must use for synchronisation. It must be right adjusted with leading zero's if the character length is 6 or 7 bits.

3.3.3 Character Class Table

3.3.3

A character may be defined as a TERM-character, an EOT-character, or non of these. Information about the character class is stored in a 256 words by 2 bits Class Table. The table is loaded by means of DOA instructions.



The Class Table can only be loaded when BUSY = 0 and AC bit(0)= 0.

Bit(6) A 1 specifies that the character is an EOT-character.

Bit(7) A 1 specifies that the character is a TERM-character.

Bit(8:15) Contain the bit pattern of the character.

3.4 Bit and Character Configuration

3.4

3.4.1 Bitpacking

3.4.1

The received bits are packed in characters consisting of either 6, 7, or 8 bits, right justified, depending on the selected character code as shown in fig. 3.10

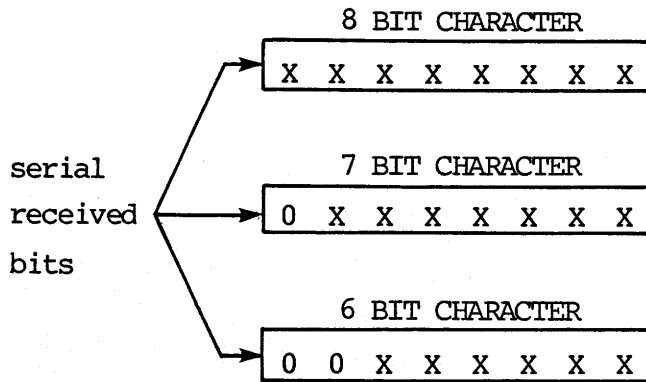
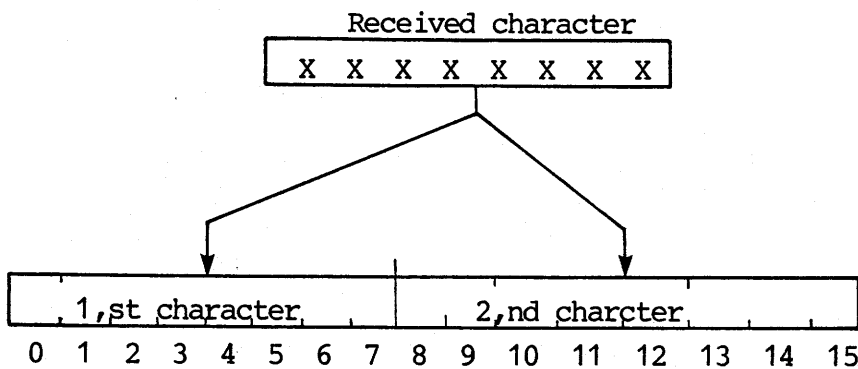


Fig. 3.10

3.4.2 Characterpacking

3.4.2

The received characters are then packed two by two in one word, that is stored in the memory. Fig. 3.10.



stored word

Fig. 3.11

3.5 Termination on errors

3.5

3.5.1 Dataset Not Ready

3.5.1

The receiver stops immediately by setting DONE and clearing BUSY if the modem control signal: Dataset Ready changes from ON to OFF during reception.

If the condition is OFF when applying a START pulse to the controller BUSY will still be zero, and DONE will be one.

3.5.2 Carrier Off

3.5.2

The receiver terminates immediately by setting DONE and clearing BUSY, if the modem control signal: "Datachannel received line signal detector" (Carrier on) changes from ON to Off during reception.

3.5.3 Word Count Overflow

The receiver word counter has reached the specified number of words in a block, and a termination takes place by setting DONE and clearing BUSY, when the present word has been stored.

3.6 Status Register

3.6

If termination occurs during reception, or the receiver asks for an interrupt by setting DONE even if it is not BUSY, the reason can be read from the status register by a DIA AC, REC instruction.

AC																
0	0	0	0	0	0	0	0	0	0	A	B	C	D	E	F	G
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

3.6.1 A Characterpointer, bit(9) 3.6.1

If the last stored word in normal termination was the left byte only, the characterpointer bit (9) is logical 1.

3.6.2 B TERM-Character Received, bit (10) 3.6.2

Reception of a TERM-Character character sets DONE, and statusbit (10) is then logical 1.

3.6.3 C Carrier Off, bit (11) 3.6.3

If the modem control signal Carrier On changes from ON to OFF during reception, there will be an interrupt and statusbit (11) is then logical 1.

3.6.4 D Dataset Not Ready, bit, (12) 3.6.4

If the modem control signal Dataset Ready changes from ON to OFF during reception there will be an interrupt and statusbit (12) is then logical 1.

3.6.5 E Calling Indicator, bit (13) 3.6.5

If the modem control signal Calling Indicator changes from OFF to ON, whether the receiver is BUSY or not, there will be an interrupt and statusbit (13) is then logical 1.

3.6.6 F Datachannel Late, bit (14) 3.6.6

If the datachannel has been in time to store the received word, statusbit (14) will be logical 1. Darachannel late is not a terminating error.

3.6.7 G Word Counter Overflow, bit (15)

3.6.7

If the word counter reaches the specified number of words, there will be an interrupt, and statusbit (15) is then logical 1.

4. TRANSMITTER LOGIC SPECIFICATIONS

4.

4.1 Device Selection

4.1

The transmitter is controlled from the CPU by means of I/O instructions. BUSY and DONE are controlled by bit (8) and (9) (function Field) in all I/O instructions with the selected device code. The device code is alterable from 41 to 75 (octal) and the transmitter will always get an odd number - the receiver the preceding even number.

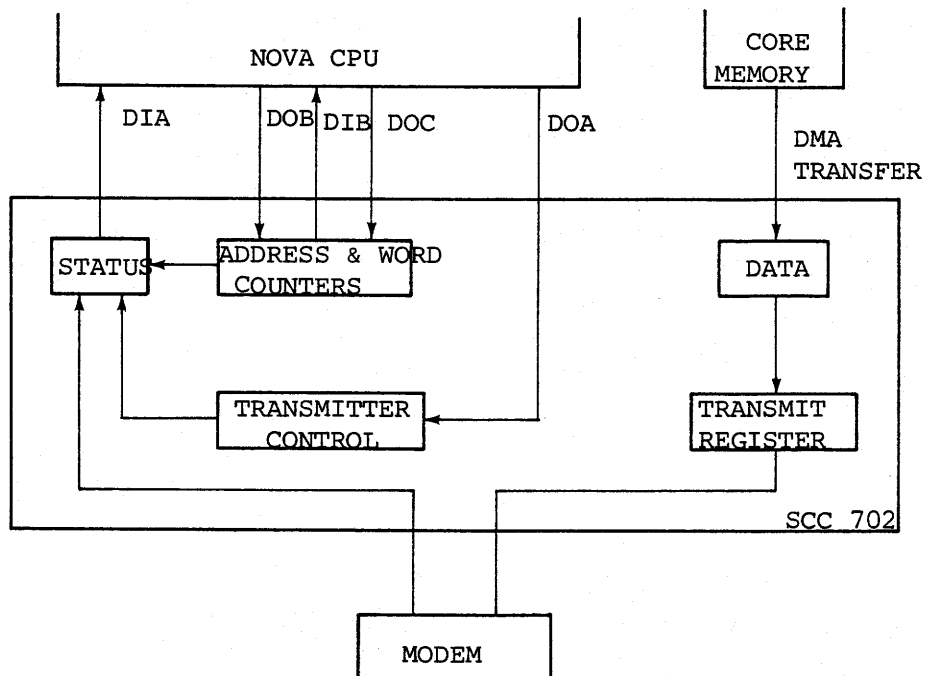
Interrupt Disable is controlled by interrupt mask bit (8).

The CLR function (F = 10) clears BUSY and DONE. STRT (F = 01) sets BUSY and clears DONE and a transmission will last as long as it is not terminated as described in 4.5.

In such case BUSY is cleared and DONE is set causing an interrupt Disable is clear.

The P function (F = 11) is not used.

The IORST instruction clears BUSY, DONE and all the control logics.



Transmitter Survey Diagram

Fig. 4.1

4.2 Address and word Counters

4.2

4.2.1 Address Counter

4.2.1

The DOB AC, XMT instruction loads the address counter with contents of AC - i.e the 16 bit address pointing at the location of the first two characters that are to be transmitted. Fig. 4.2.

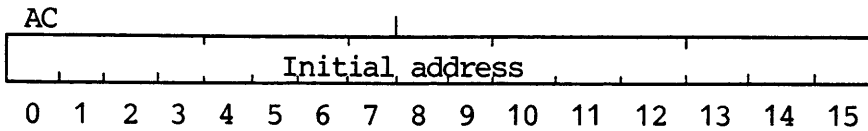


Fig. 4.2

When the transmission begins, the address counter is incremented by one every time two characters are transferred from the memory to the transmitter register.

In this way, the contents of the address counter is one greater than the address of the last transferred word, if termination occurs. Fig. 4.3

This address can be read into the program by a DIB AC, XMT instruction and thus determine the length of an unknown block.

The DIB instruction will not alter the contents of the address counter.

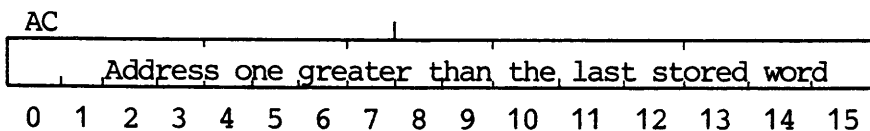


Fig. 4.3

4.2.2 Word Counter

4.2.2

The DOC, XMT instruction loads the word counter with the contents of AC - i.e. the 16 bit negative word count. (two's complement).

Fig. 4.4

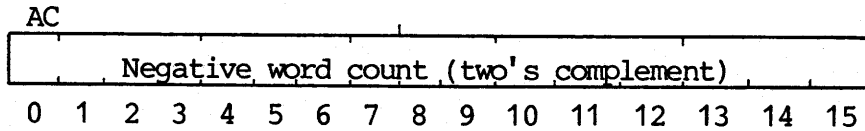


Fig. 4.4

The word counter is incremented together with the address counter, and if overflow occurs, the transmission will terminate. (Ref. 4.5.3).

Before a transmission can take place, the word counter must be preset to the desired (negative) block length.

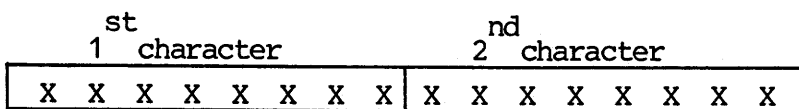
4.3 Word and character configuration

4.3

4.3.1 Word configuration

4.3.1

The characters to be transmitted are transferred from the core memory two by two as shown in fig. 4.5.



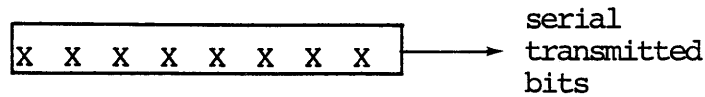
Transferred word

Fig. 4.5

The characters are transferred to the transmitter register according to numbering.

4.3.2 Character configuration

The characters must consist of either 6, 7, or 8 bits, right adjusted as described in 3.3.1 and are then serial transmitted from the register. Fig. 4.6.



Transferred character

Fig. 4.6

4.4 Transmitter Commands

4.4

4.4.1 Dataterminal Ready Command

4.4.1

This signal goes ON by applying AC with 1 in bit (15) in a DOA AC, XMT instruction.

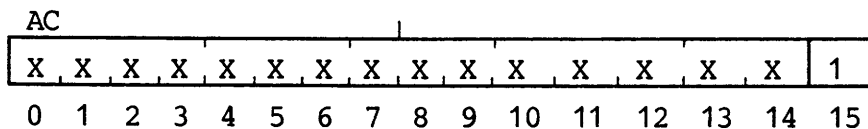


Fig. 4.7

The signal goes OFF again if bit (15) is zero in a DOA AC, XMT instruction, or by an IORST instruction.

4.4.2 Transmitted speed

4.4.2

When using a modem with two data signaling rates e.g. 600/1200 bps, it is possible to hardwire the transmitter to select the modem clock frequency.

4.5 Termination

4.5

The transmitter will stay in transmit mode until it is terminated by one of three reasons.

In every case BUSY is cleared and DONE is set causing an interrupt if Interrupt Disable is clear.

The reason for the termination can be read by the program from a Status Register. (Ref. 3.11)

4.5.1 Data Channel Late

4.5.1

If the datachannel is late in time to transfer the next word, SYNC is lost and the transmission will terminate.

4.5.2 Dataset Not Ready

4.5.2

The transmission will terminate if the modem control signal: Dataset Ready changes from ON to OFF during transmission.

4.5.3 Word Counter Overflow

4.5.3

The specified number of transmitted words is passed and a termination takes place.

4.6 Status Register

4.6

As mentioned above a termination will clear BUSY and set DONE causing an interrupt.

The reason for termination can then be read from a Status Register by a DIA AC, XMT instruction. Fig. 4.8.

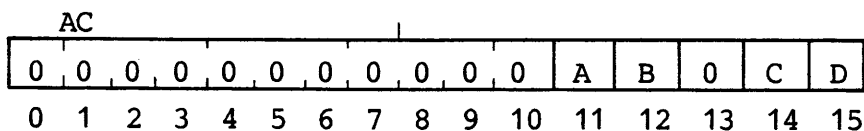


Fig. 4.8

4.6.1

4.6.1 A Carrier Off, bit (11)

If the modem control signal Carrier On changes from ON to OFF then statusbit (11) is logical 1.

This statusbit can only be sensed.

4.6.2

4.6.2 B Dataset Not Ready, bit (12)

If the modem control signal Dataset Ready changes from ON to OFF during transmission, there will be an interrupt and statusbit (12) will be logical 1.

4.6.3

4.6.3 C Datachannel late, bit(14)

If the datachannel is late in time to transfer the next two characters to the transmitter, there will be an interrupt and statusbit (14) will be logical 1.

4.6.4

4.6.4 D Wordcounter Overflow, bit (15)

If the wordcounter reaches the specified number of words, there will be an interrupt, when the present character has been transmitted, statusbit (15) will be logical 1.

5. VARIOUS INFORMATIONS

5.

5.1 Technical Specifications

5.1

The SCC 705/706 communications controller is designed for use in the RC modular system CHS 709.

In addition to the normal +5V power supply, both +12V and -12V power supplies must be present in CHS 701.

Power consumption:

From the	+5V bus	typ. 2.0 A
-	- +12V -	- 25 mA
-	- -12V -	- 15 mA

The mechanical specifications are:

Dimensions: W x D x H: 380 x 390 x 23 mm

Weight: 1.25 kg

Ambient temperature and humidity range: 0- + 45^o C and 20 - 80% without condensation.

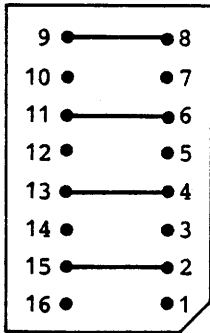
5.2 Device Code Select Plug

As mentioned in the logic specifications, it is possible to alter the device code.

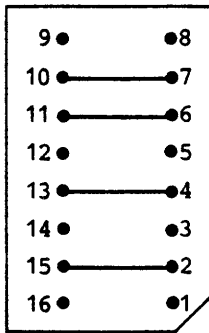
In position 51 (139 on SCC 702 and 705) on the circuitboard a component adapter is placed in a dual-in-line socket.

The device code is changed by soldering as the following sheet shows.

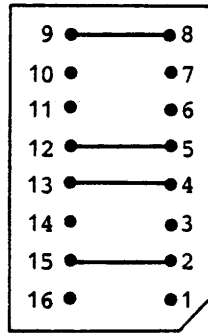
Device Code Select Plug



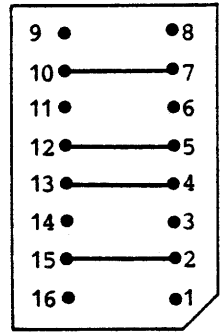
REC: 40
XMT: 41



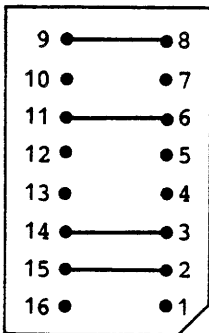
REC: 42
XMT: 43



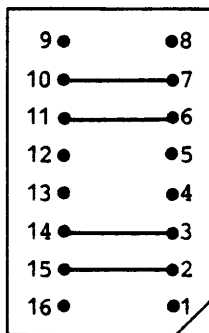
REC: 44
XMT: 45



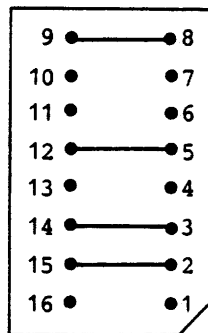
REC: 46
XMT: 47



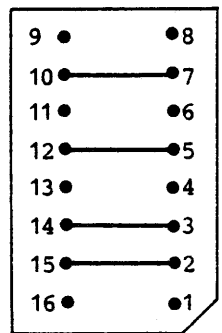
REC: 50
XMT: 51



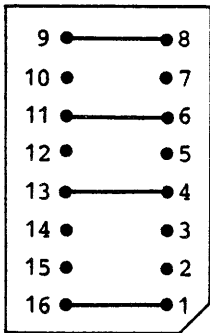
REC: 52
XMT: 53



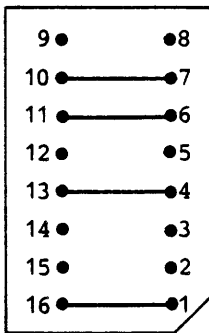
REC: 54
XMT: 55



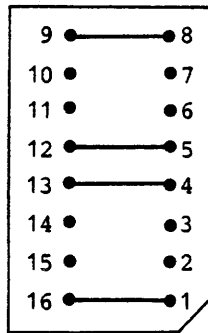
REC: 56
XMT: 57



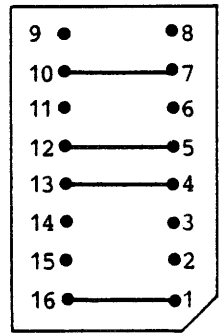
REC: 60
XMT: 61



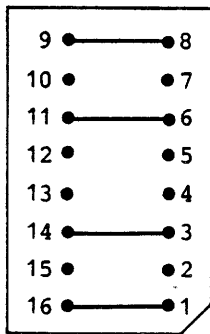
REC: 62
XMT: 63



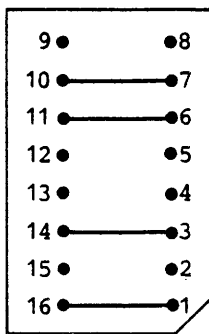
REC: 64
XMT: 65



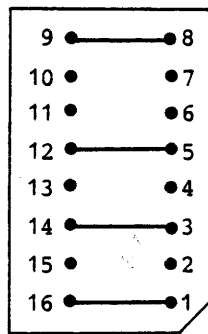
REC: 66
XMT: 67



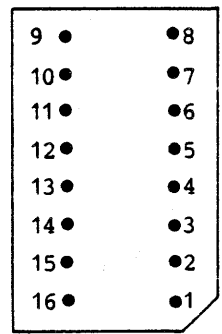
REC: 70
XMT: 71



REC: 72
XMT: 73



REC: 74
XMT: 75



NOT
USED

RETURN LETTER

Title: SCC 705/706, Binary Synchronous
Communication Controller

RCSL No.: 44-RT1948

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How can this manual be improved?

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