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Title:

SMX702

Binary Synchronous Communication

Multiplexer - X.21

Technical Manual

Keywords:

SMX702, BSC, X.21, datex, X.27.

Abstract:

This manual contains the drawings and the technical description of the SMX702.

(72 printed pages)

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1. DESCRIPTION

1.

The SMX702 is a synchronous communication multiplexer with 4 channels.

The SMX702 differs from the SMX701 only in the interface. SMX701 has all interface signals in accordance with CCITT recommendation V.24 (electrical V.28) which is standard for communication on telephone lines (switched as well as leased lines).

The SMX702 has all signals in accordance with CCITT recommendation X.24/X.27, which enables possibility to use recommendation X.21 for line connection and clearing.

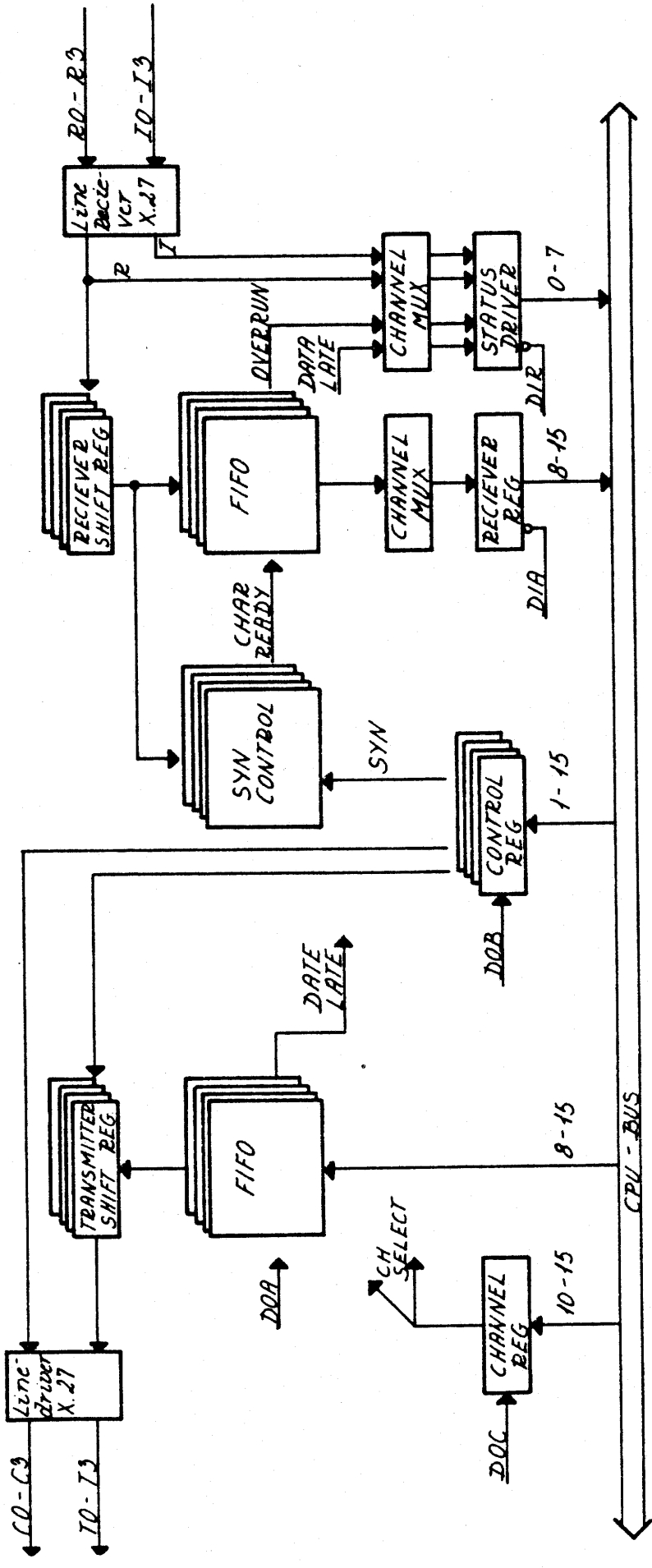
The X.21 is a standard for connection to the NPDN (nordic public data network).

2. BLOCK DIAGRAM

2.



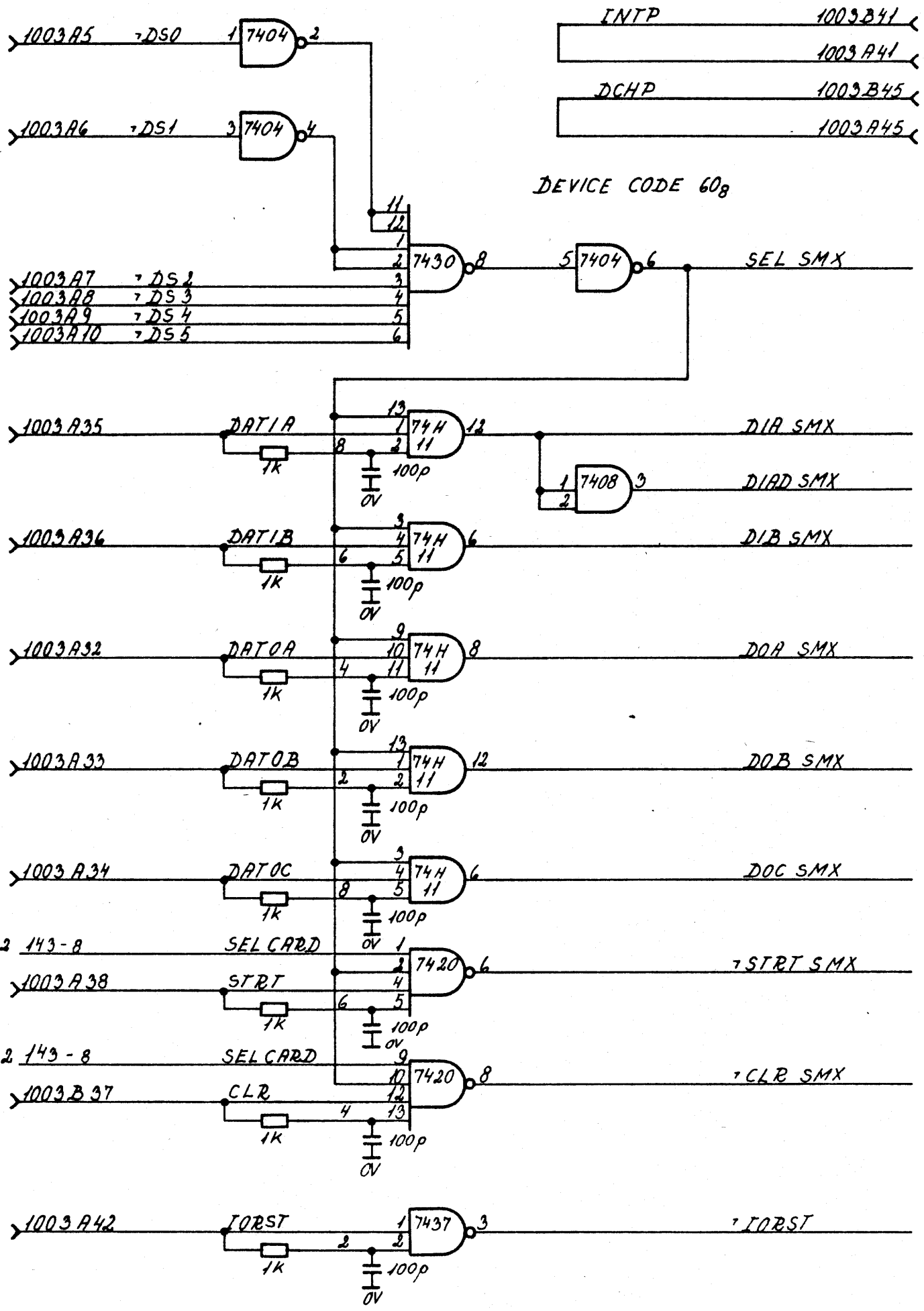
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3. LOGIC DIAGRAMS AND FUNCTIONAL DESCRIPTION

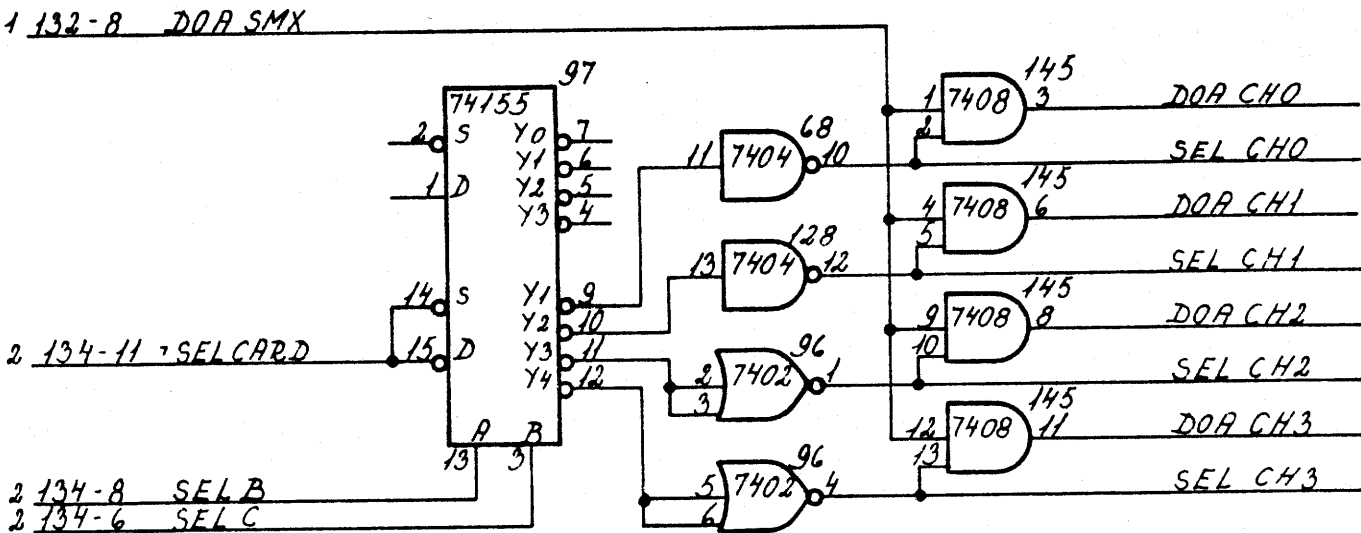
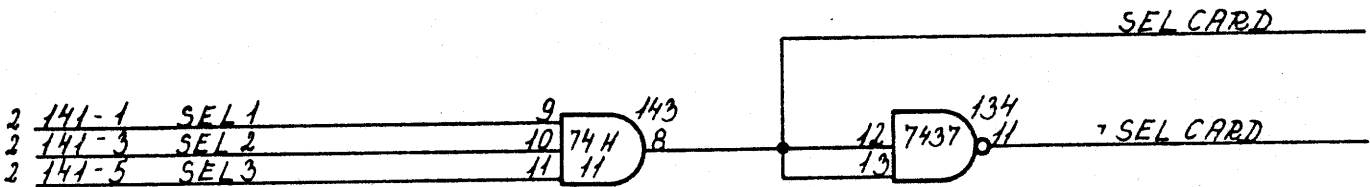
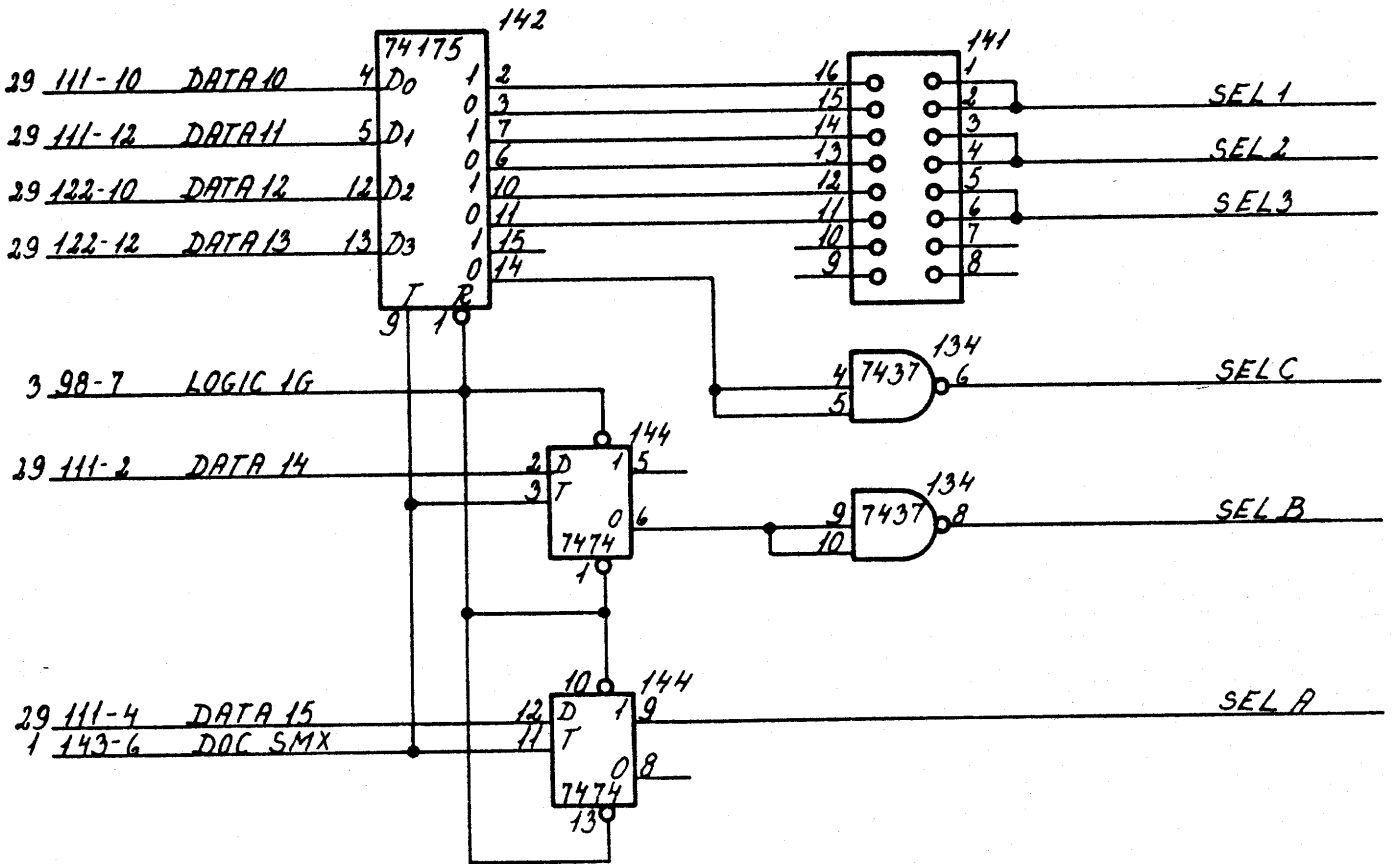
3.

Signal	Destination	Description
SEL SMX	3	select SMX device code 60 octal.
DIA SMX	5,12,17,22,27	Data in A, SMX
DIAD SMX	29	
DIA SMX	28	Data in B, SMX
DOA SMX	2	Data out A, SMX
DOB SMX	11,16,21,26	Data out B, SMX
DOC SMX	2	Data out C, SMX
-,STRT SMX	2	Start SMX
-,CLR SMX	4	Clear SMX
-,IORST	4,11,16,21,26	I/O Reset

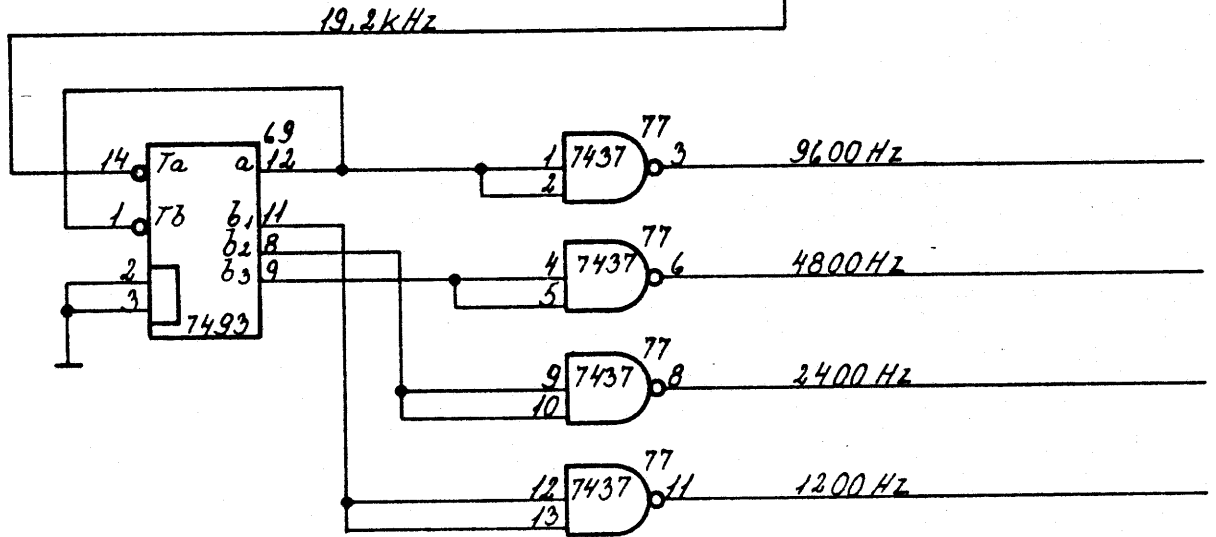
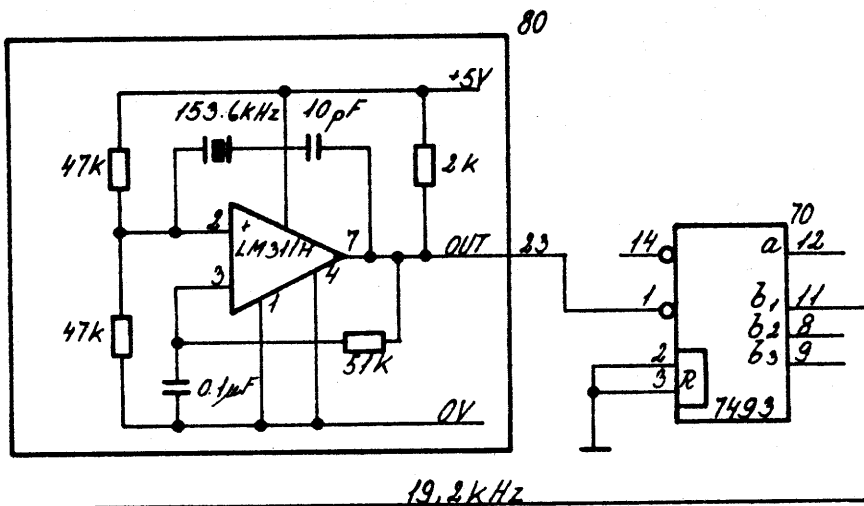


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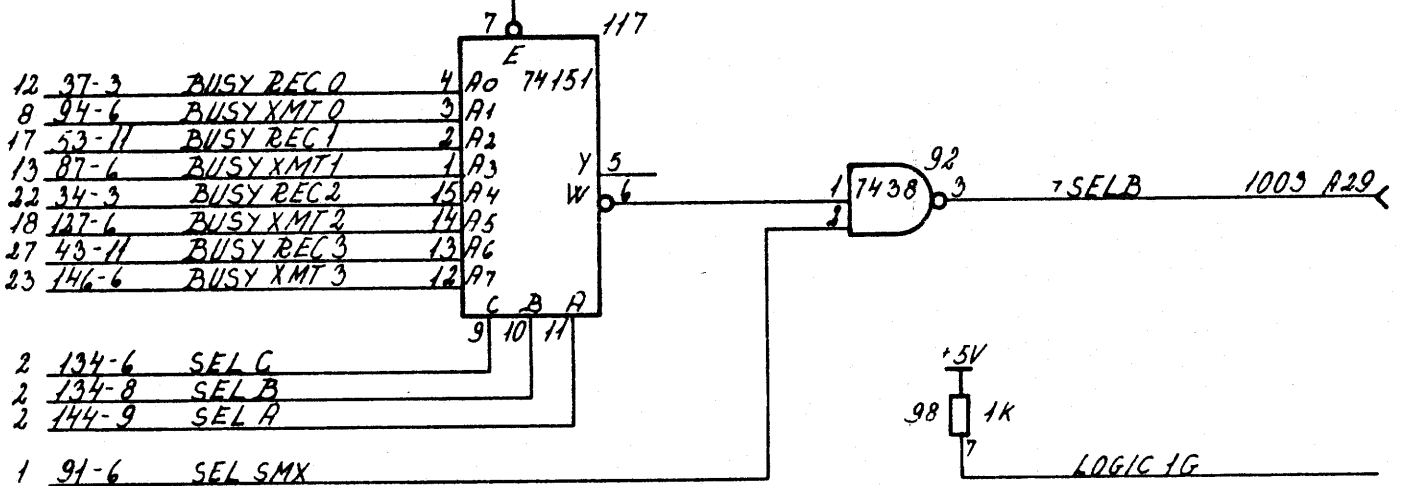
Signal	Destination	Description
SEL 1-3	2	Group selection
SEL B,C	2,3,4,5,7	Channel Selection
SEL A	3,4	Rec/xmit selection
-,SEL CARD	2,5,7	Board Selected
DOA CH0	8	Data out A,
DOA CH1	13	clocking of byte to be
DOA CH2	18	transmitted
DOA CH3	23	
SEL CH0	11,12	Channel selected
SEL CH1	16,17	
SEL CH2	21,22	
SEL CH3	26,27	



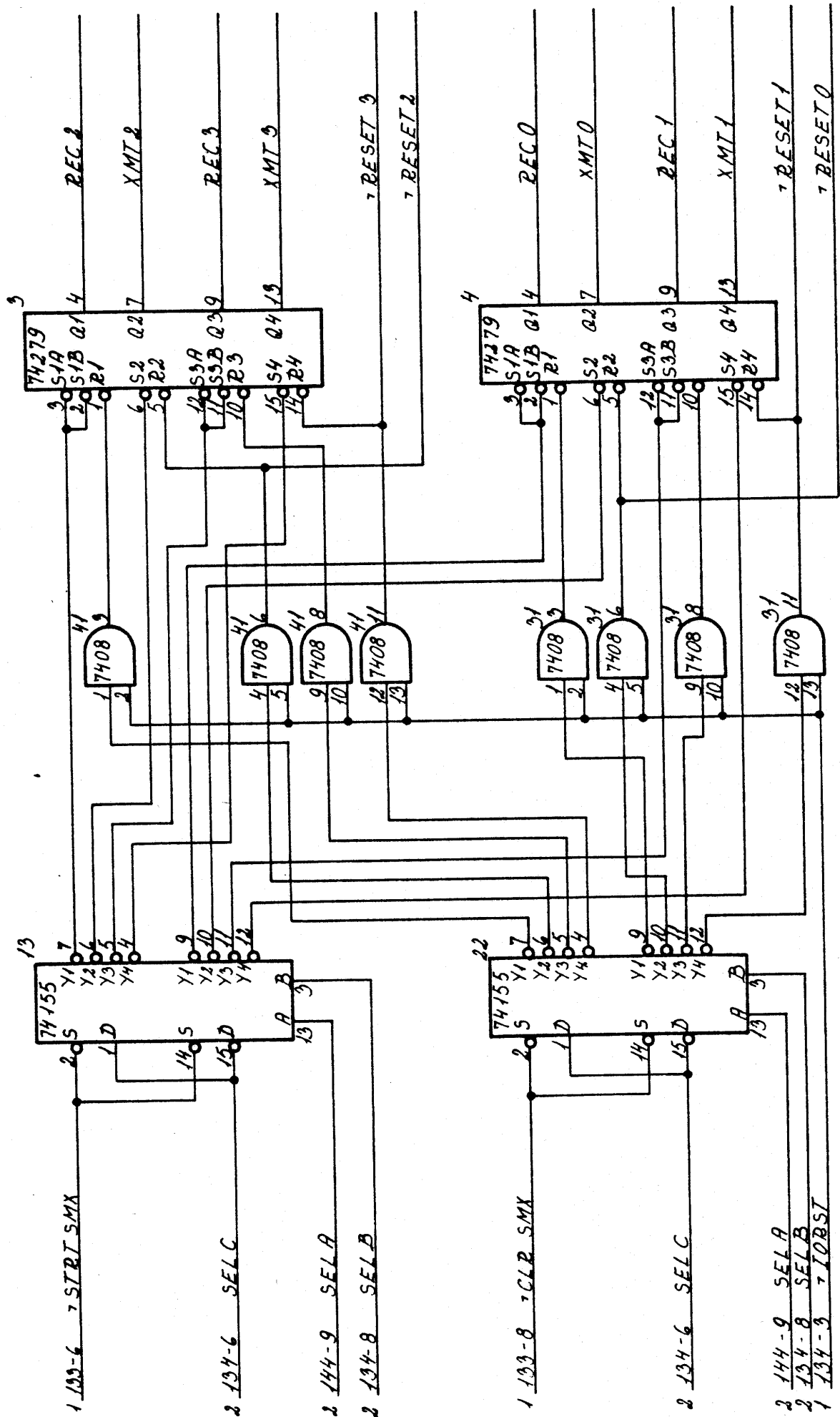
Signal	Destination	Description
9600, 4800, 2400, 1200	9,14,19,24	Selected internal clock. Used for testpurpose
SELB	1003, A29	Selected channel is Busy.



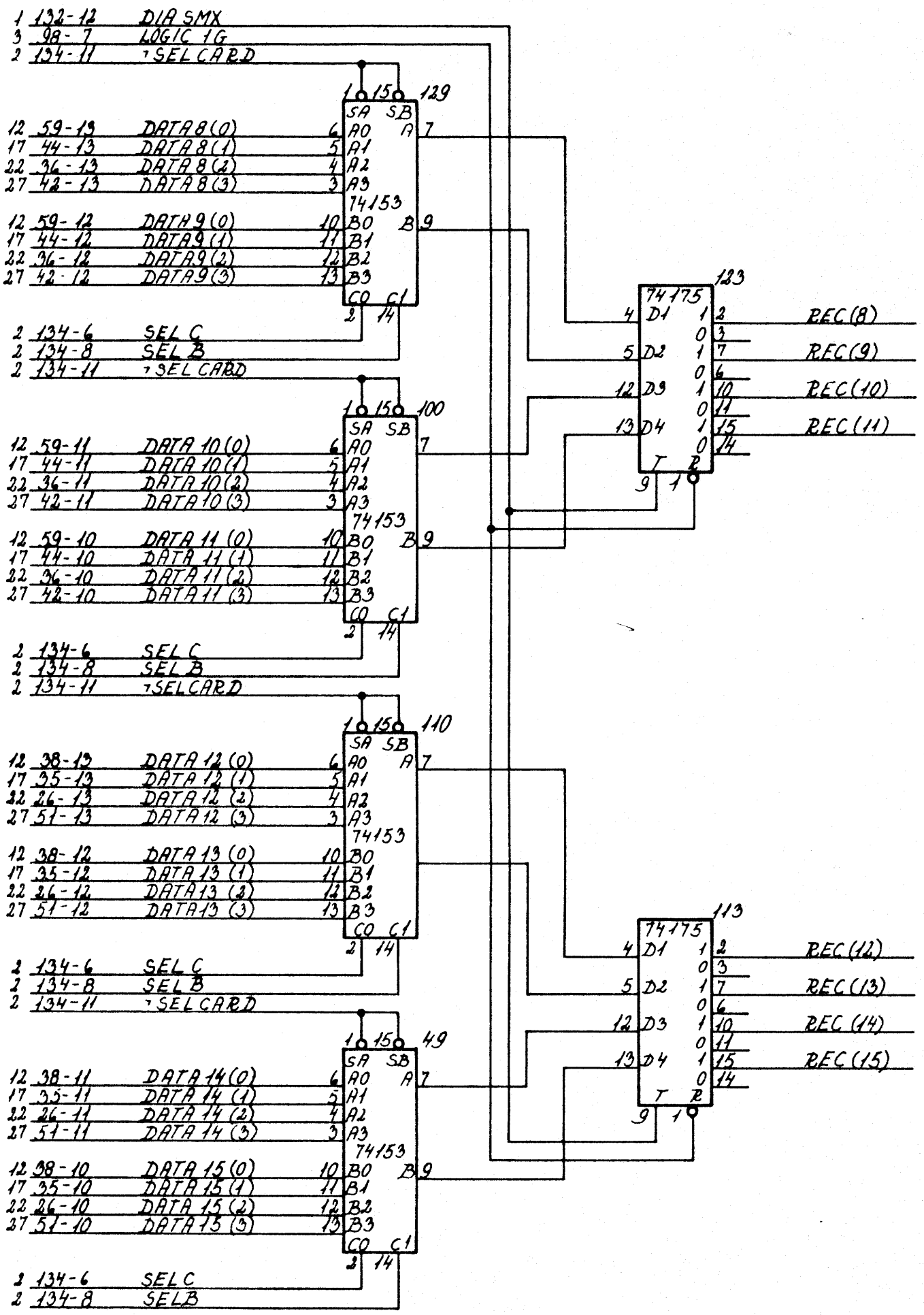
2 134-11 → SEL CARD



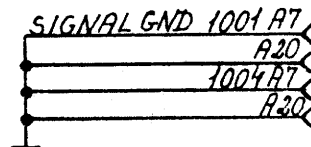
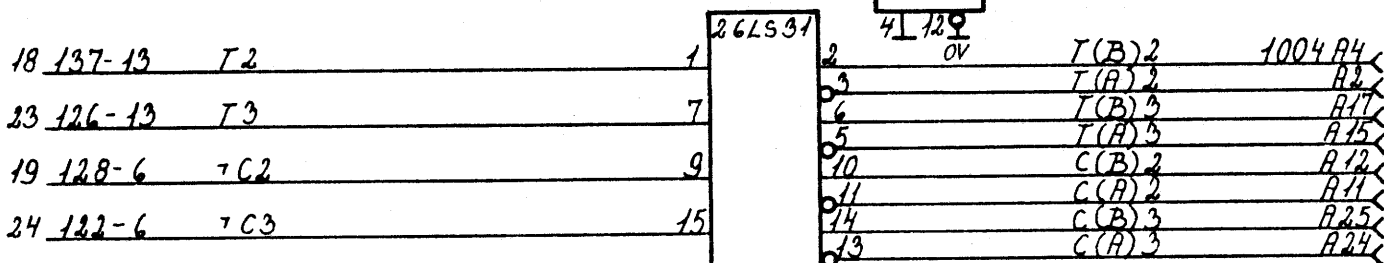
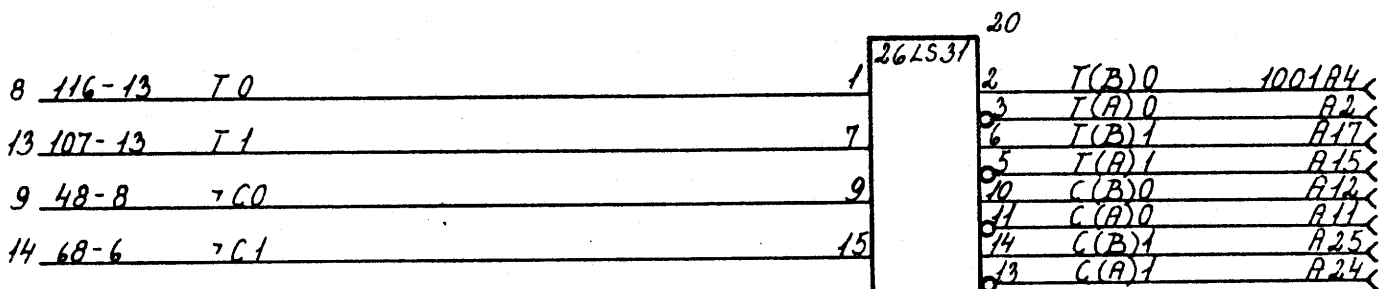
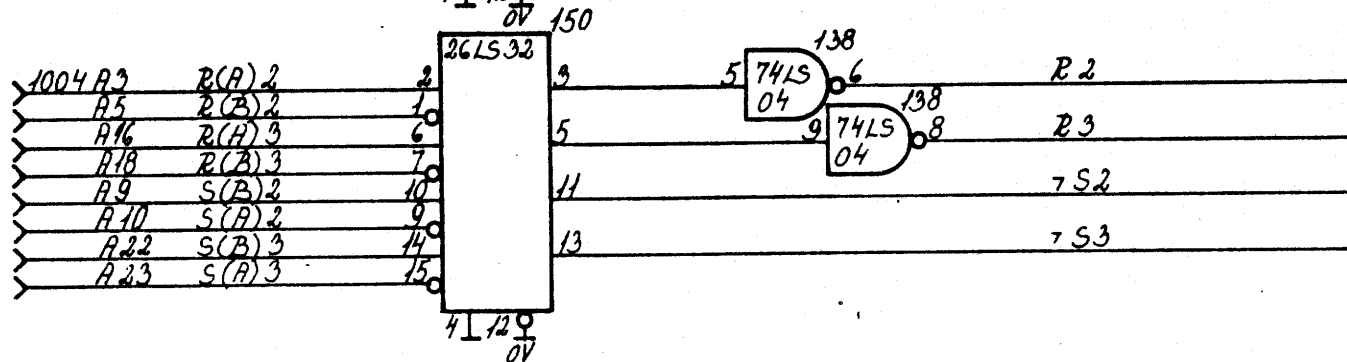
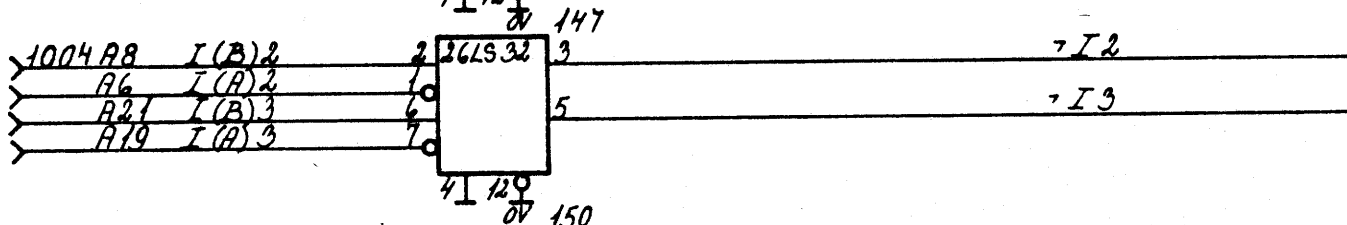
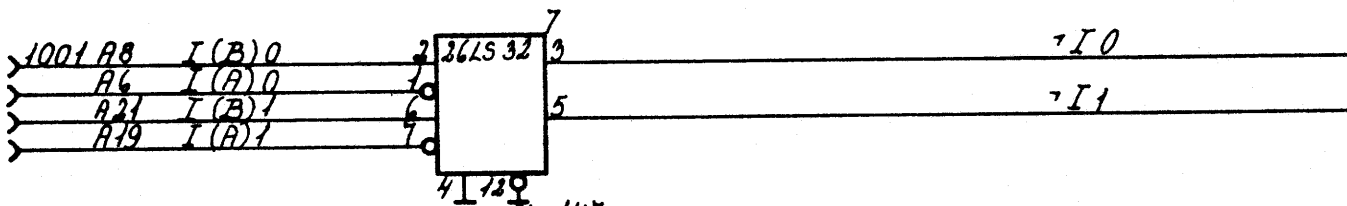
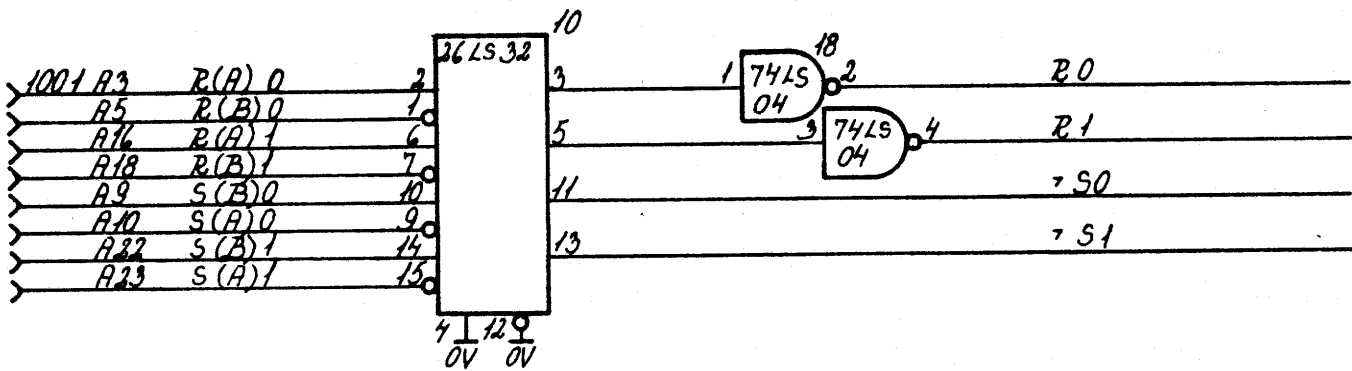
Signal	Destination	Description
REC 0	7,10,12	Receiver active
REC 1	7,15,17	
REC 2	7,20,22	
REC 3	7,25,27	
XMT 0	7,9	Transmitter active
XMT 1	7,14	
XMT 2	7,19	
XMT 3	7,24	
-,RESET 0	8	Reset transmitter fifo
-,RESET 1	13	
-,RESET 2	18	
-,RESET 3	23	



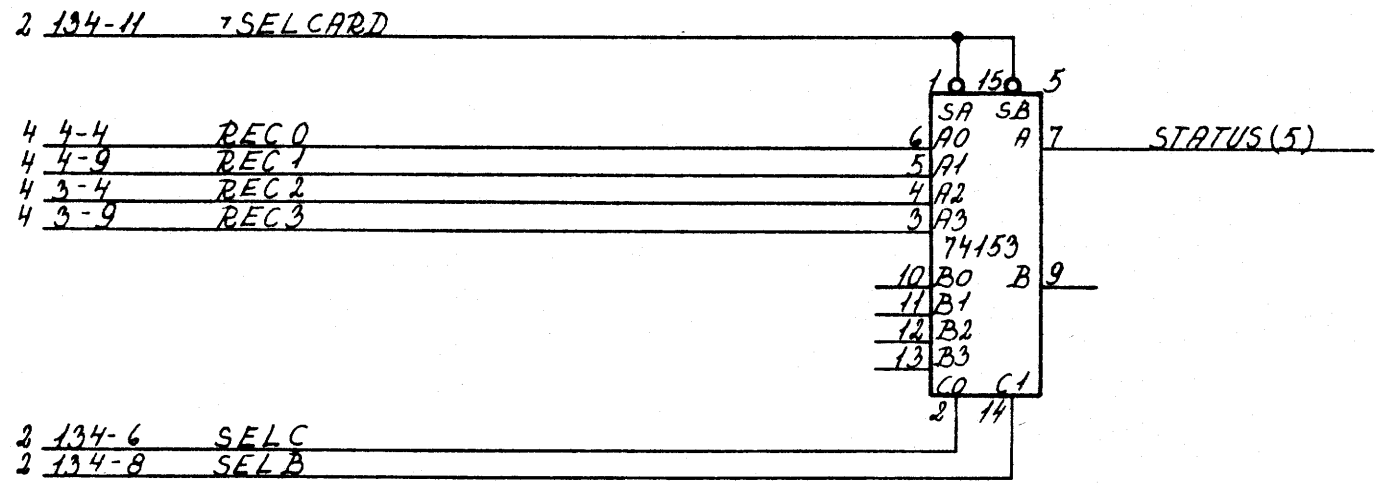
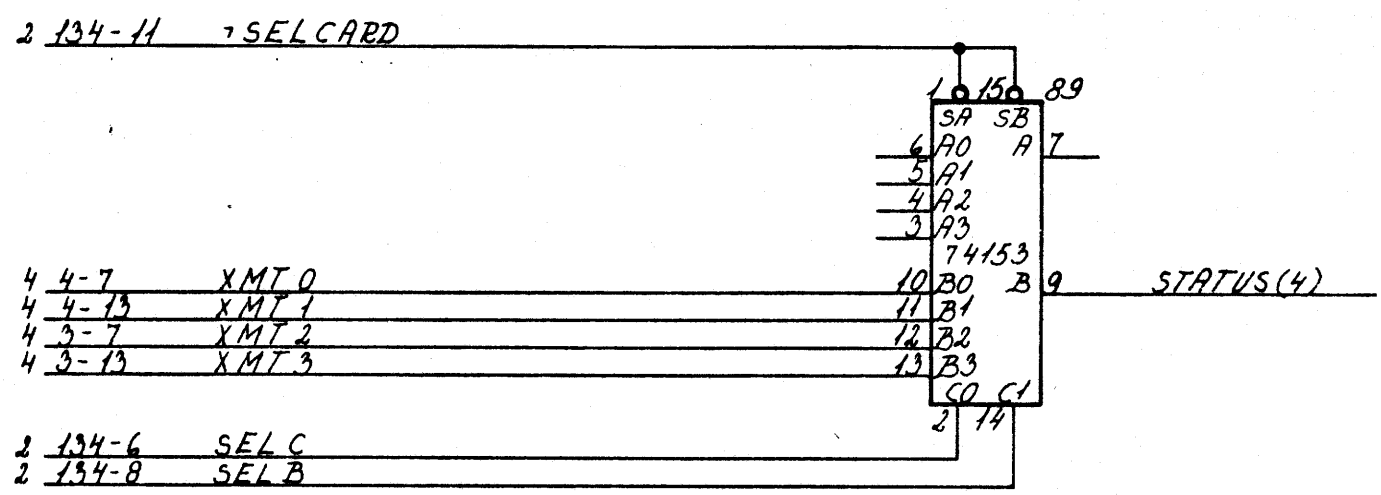
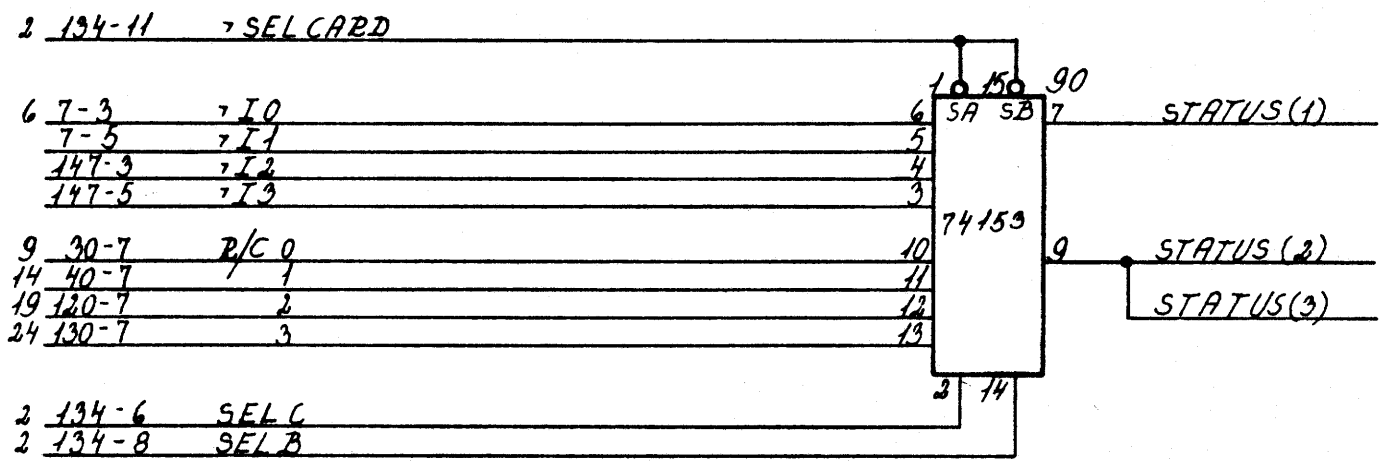
Signal	Destination	Description
REC(8)-REC(15)	29	Receiver data register



Signal	Destination	Description
R0	9,11,30	Serial receiver data
R1	14,16,30	
R2	19,21,30	
R3	24,26,30	
-,I0 - -,I3	7,30	Indication, modem control signal
-,S0	9	Modem clock
-,S1	14	
-,S2	19	
-,S3	24	

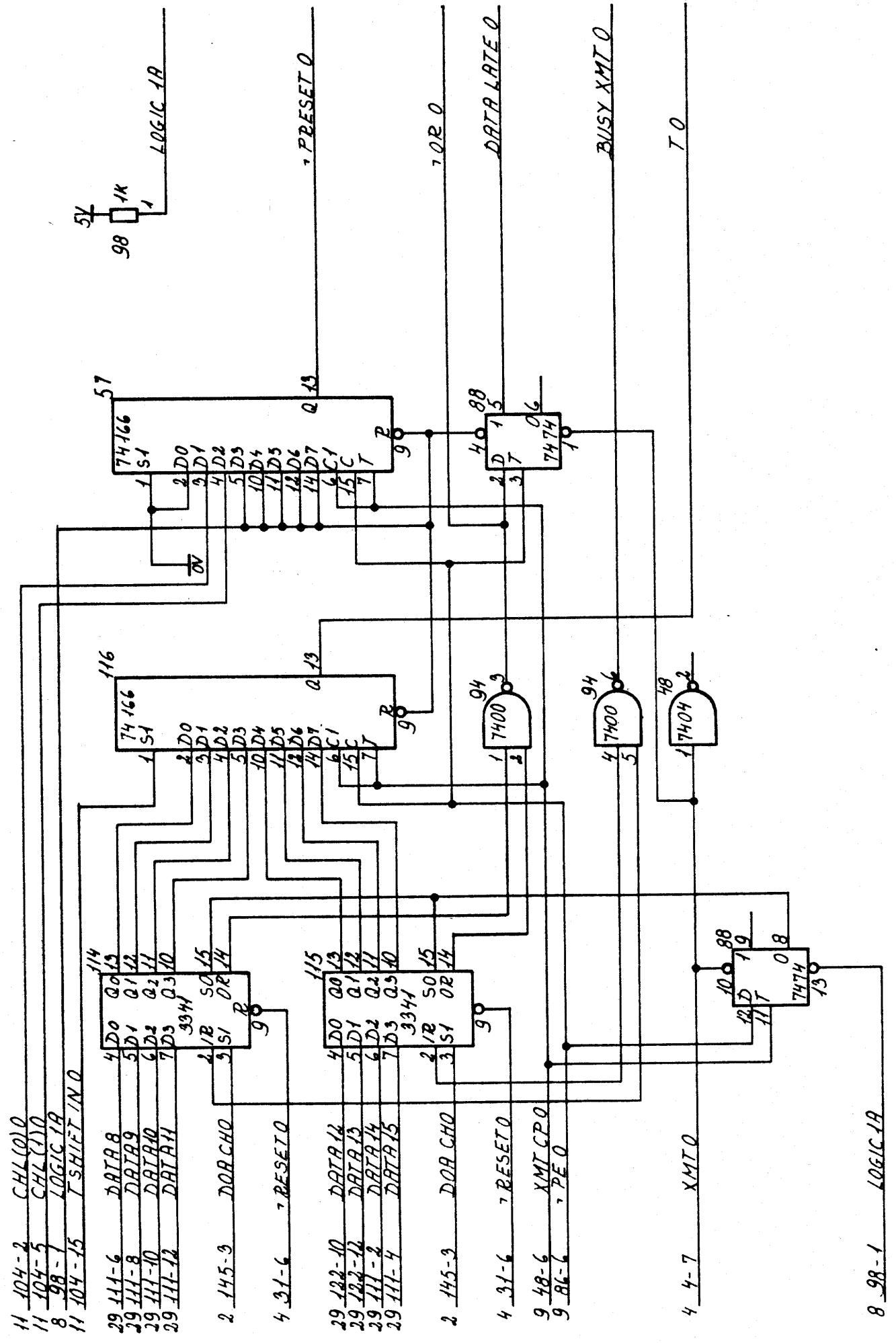


Signal	Destination	Description
STATUS (1-5)	28	Status register



Signal	Destination	Description
-,PRESET 0	9,12	Byte synchronisation.
-,OR 0	9	FIFO output ready.
DATA LATE 0	28	Data late error.
BUSY XMT 0	3	Transmitter not ready for receiving new data.
T 0	6	Serial transmit data.

TRANSMITTER REGISTERS & CONTROL CH0
LOGIC DIAGRAM



- 11 104-2 CHL(0)
- 11 104-5 CHL(1)
- 8 98-1 LOGIC 1A
- 11 104-15 T SHIFT IN 0

- 29 111-6 DATA 8
- 29 111-8 DATA 9
- 29 111-10 DATA 10
- 29 111-12 DATA 11
- 29 111-14 DATA 12
- 29 111-16 DATA 13
- 29 111-18 DATA 14
- 29 111-20 DATA 15

- 2 145-9 DOR CHO
- 4 31-6 RESETO

- 29 122-10 DATA 12
- 29 122-12 DATA 13
- 29 122-14 DATA 14
- 29 122-16 DATA 15

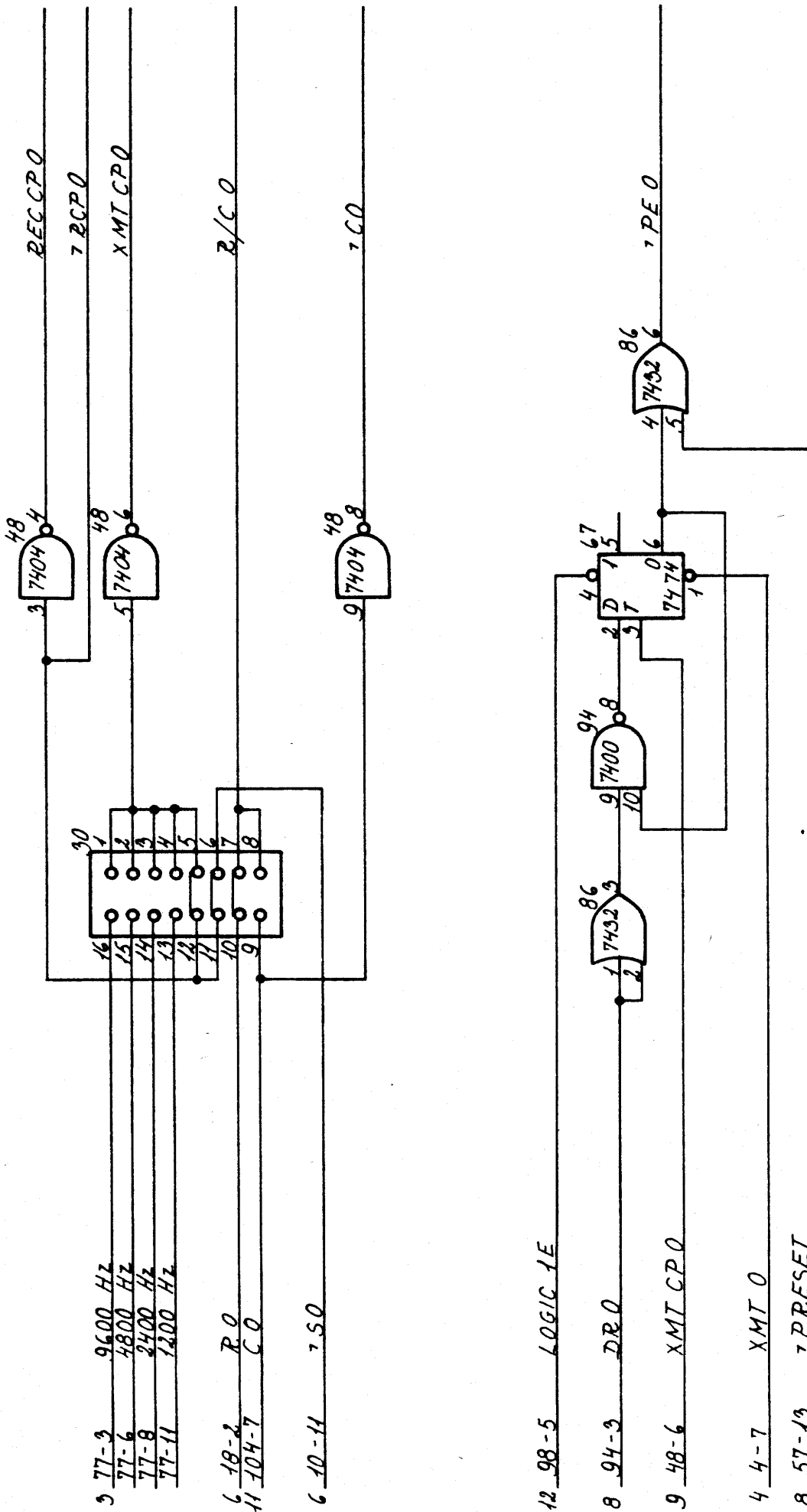
- 2 145-3 DOR CHO
- 4 31-6 RESETO

- 9 48-6 XMI CPO
- 9 86-6 PE O

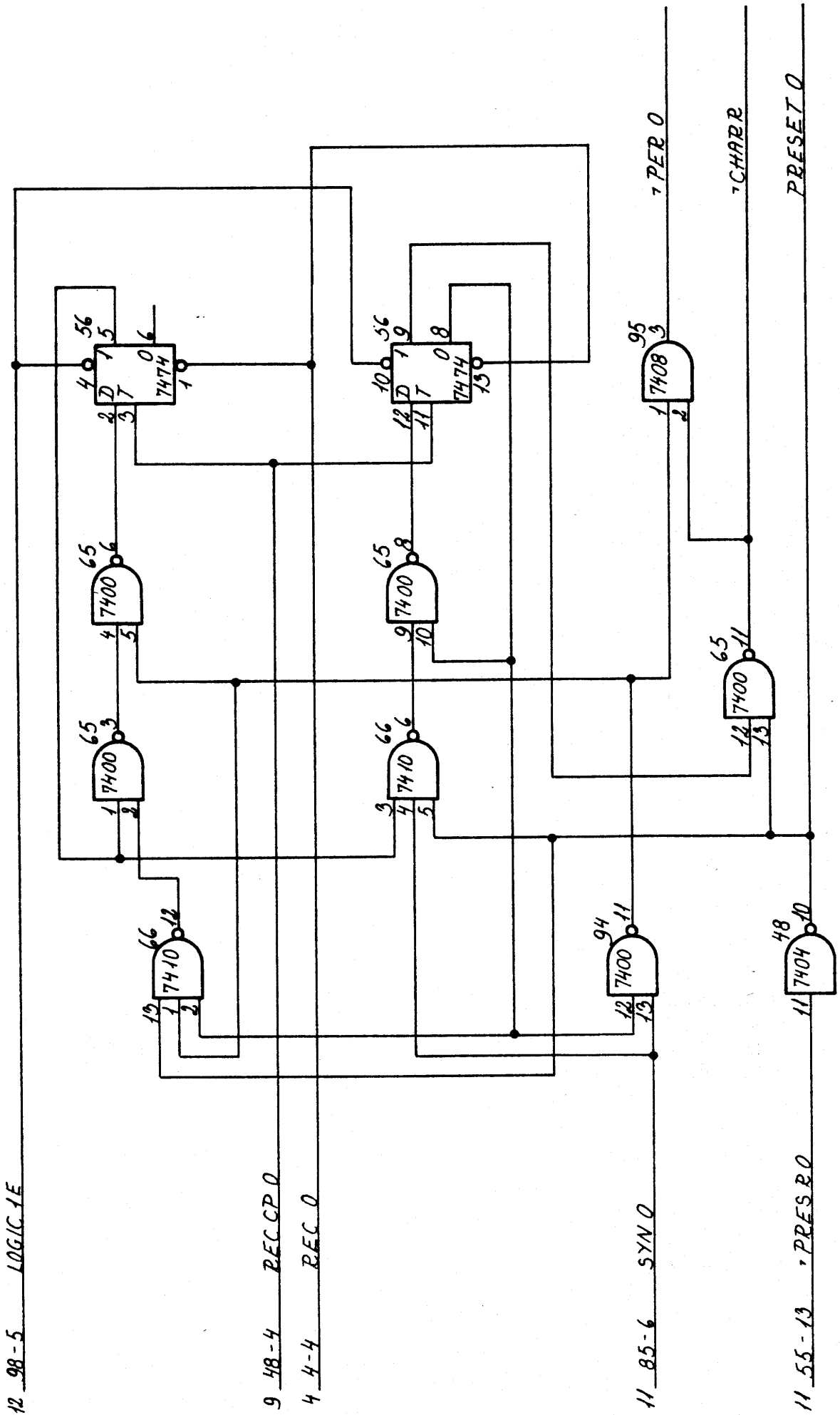
- 4 4-7 XMT O

- 8 98-1 LOGIC 1A

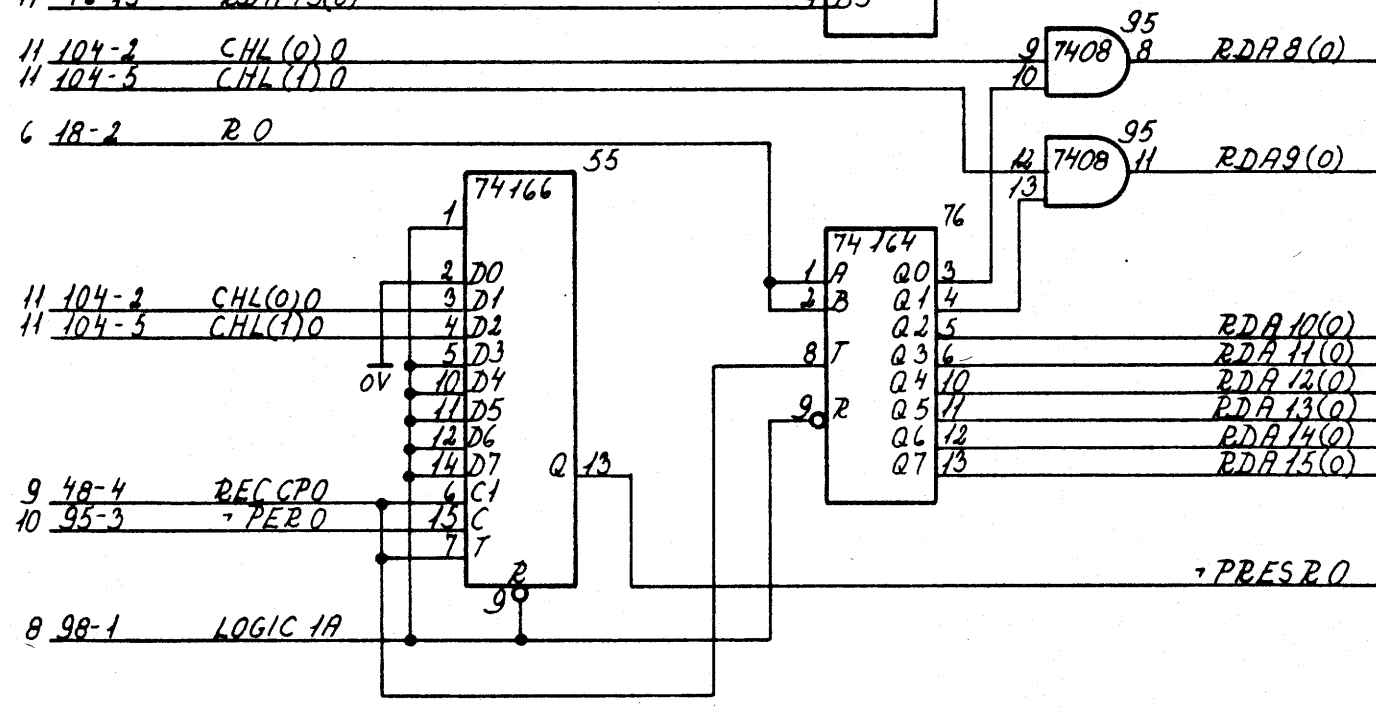
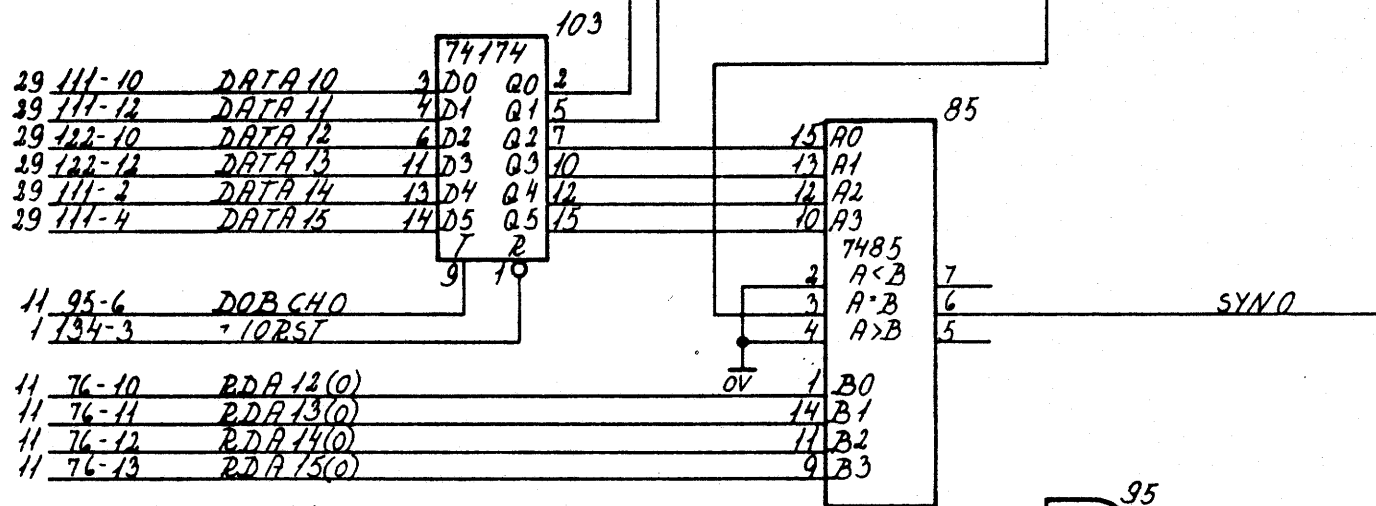
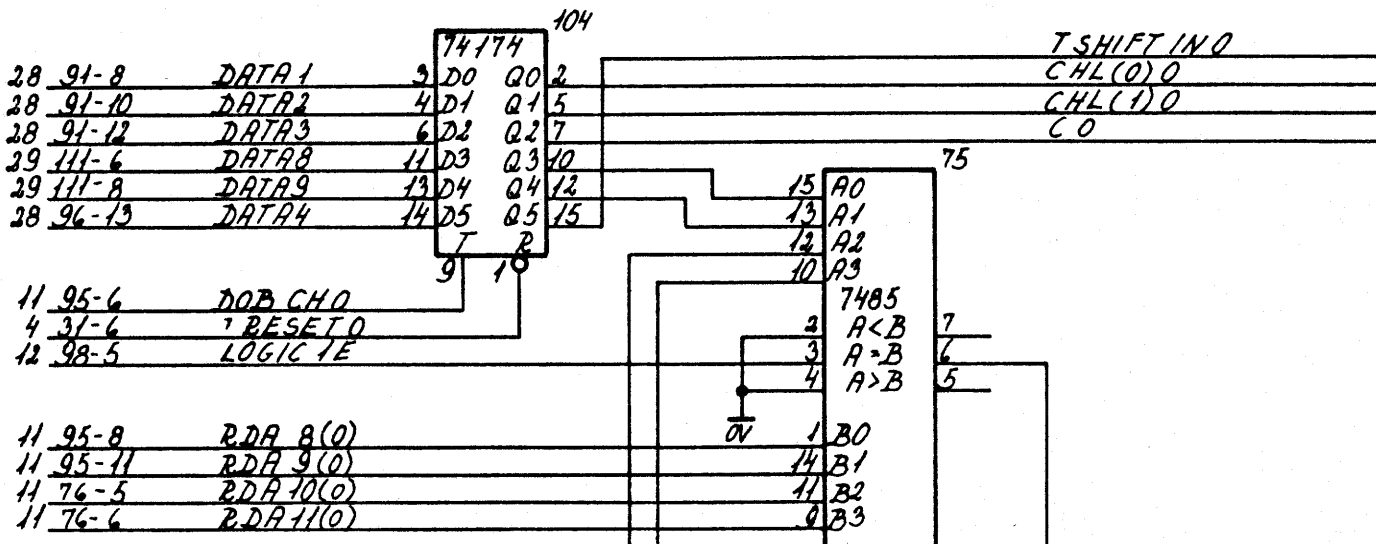
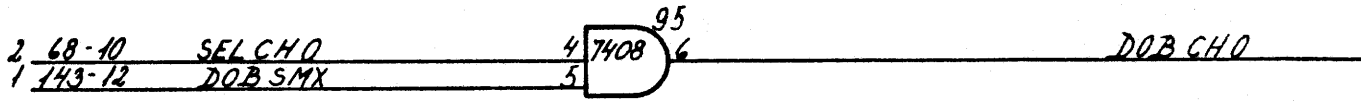
Signal	Destination	Description
REP CP 0 -,RCP 0	10,11 12	Receiver clock.
XMT CP 0	8,9	Transmitter clock.
R/C 0	7	Status signal R. (test: C)
-,C 0	6	Modem control signal.
-,PE 0	8	Parallel enable. Byte synchronisation.



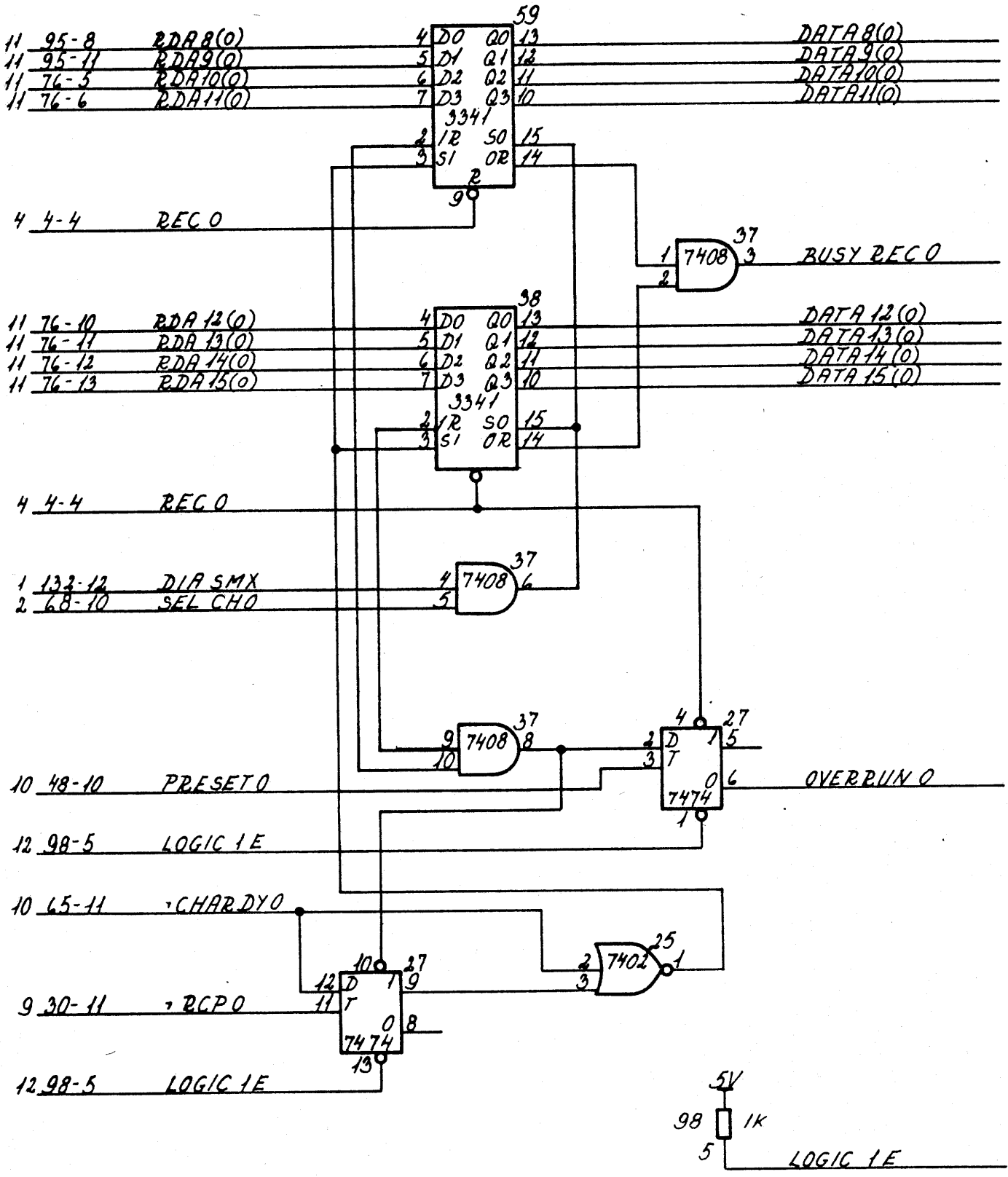
Signal	Destination	Description
-,PER 0	11	Receiver byte synchronisation
CHARRDY 0	12	Character ready to be entered into the fifo.
PRESET 0	12	Receiver byte synchronisation



Signal	Destination	Description
DOB CH 0	11	Data out B, control register load.
TSHIFT IN 0	8	Transmitter level when not started.
CHL(0)-CHL(1) 0 11		Character length.
C 0	6	Modem control signal.
SYN 0	10	Sync byte found.
RDA (8:15) 0	11	Receiver data.
PRES R 0	10	Receiver byte synchronisation.

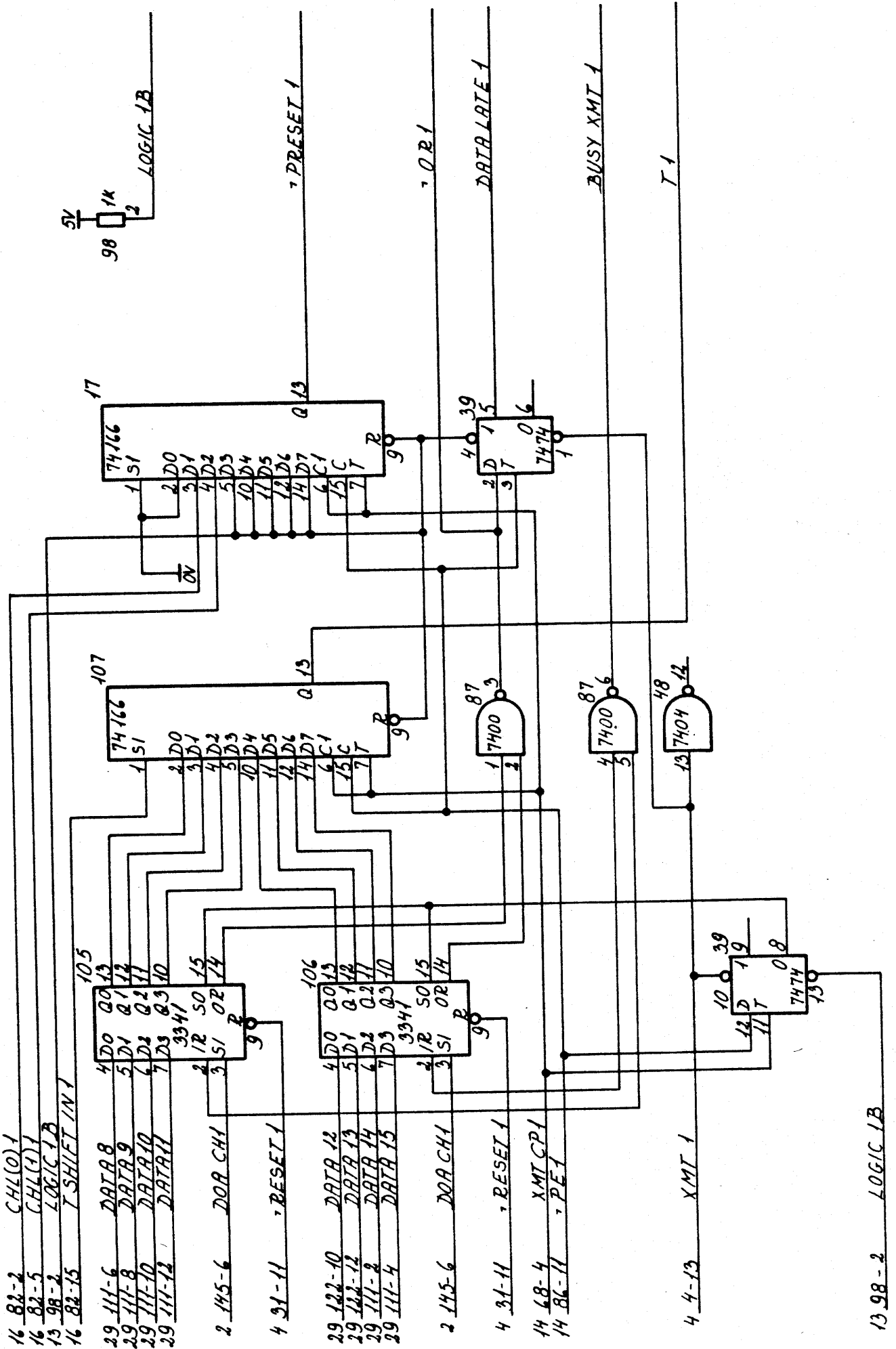


Signal	Destination	Description
DATA (8:15) 0	5	Receiver data to CPU.
BUSY REC 0	3	Receiver busy, no receiver data is ready.
OVERRUN 0	28	The fifo is not able to contain the incoming character.

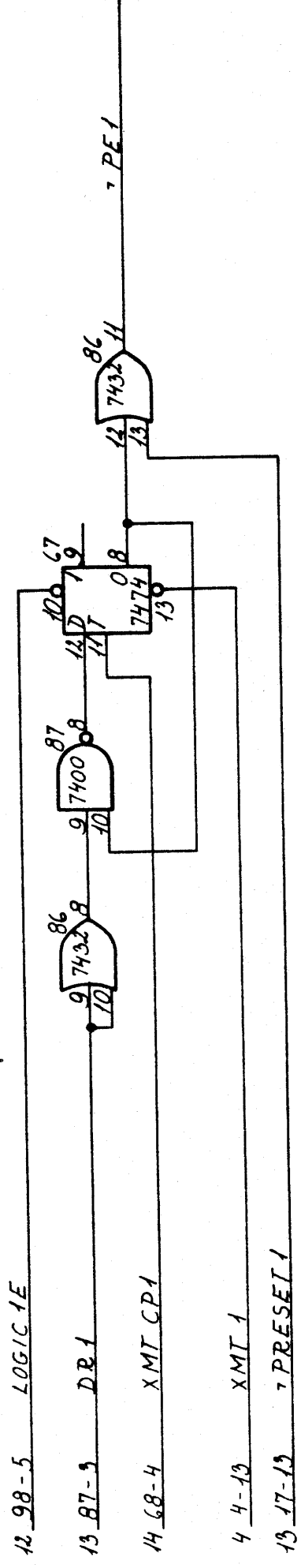
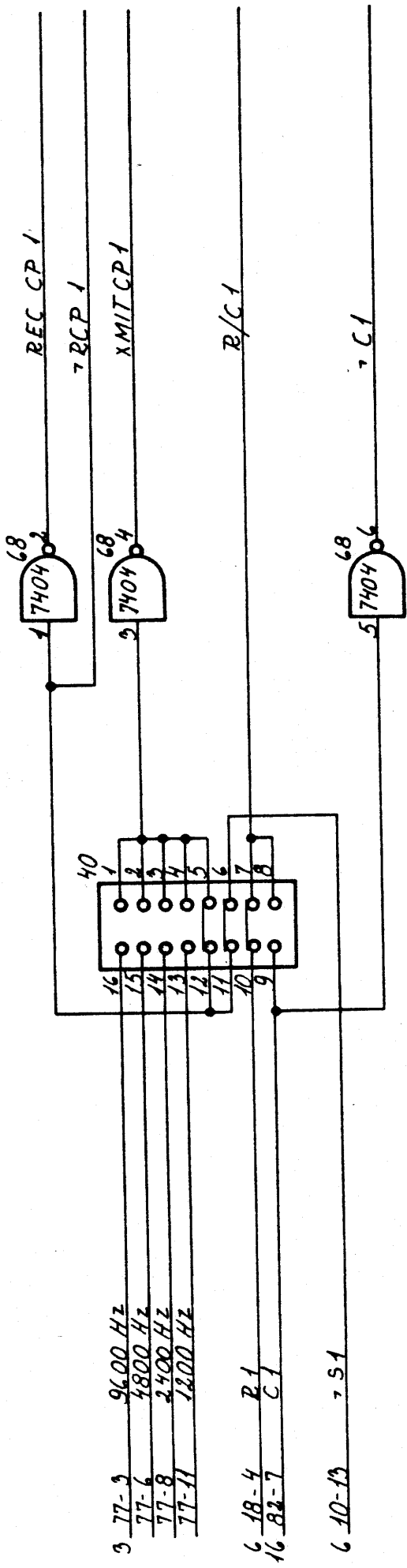


Signal	Destination	Description
-,PRESET 1	14,17	Byte synchronisation.
-,OR 1	14	FIFO output ready.
DATA LATE 1	28	Data late error.
BUSY XMT 1	3	Transmitter not ready for receiving new data.
T 1	6	Serial transmit data.

TRANSMITTER REGISTERS AND CONTROL CH1
LOGIC DIAGRAM

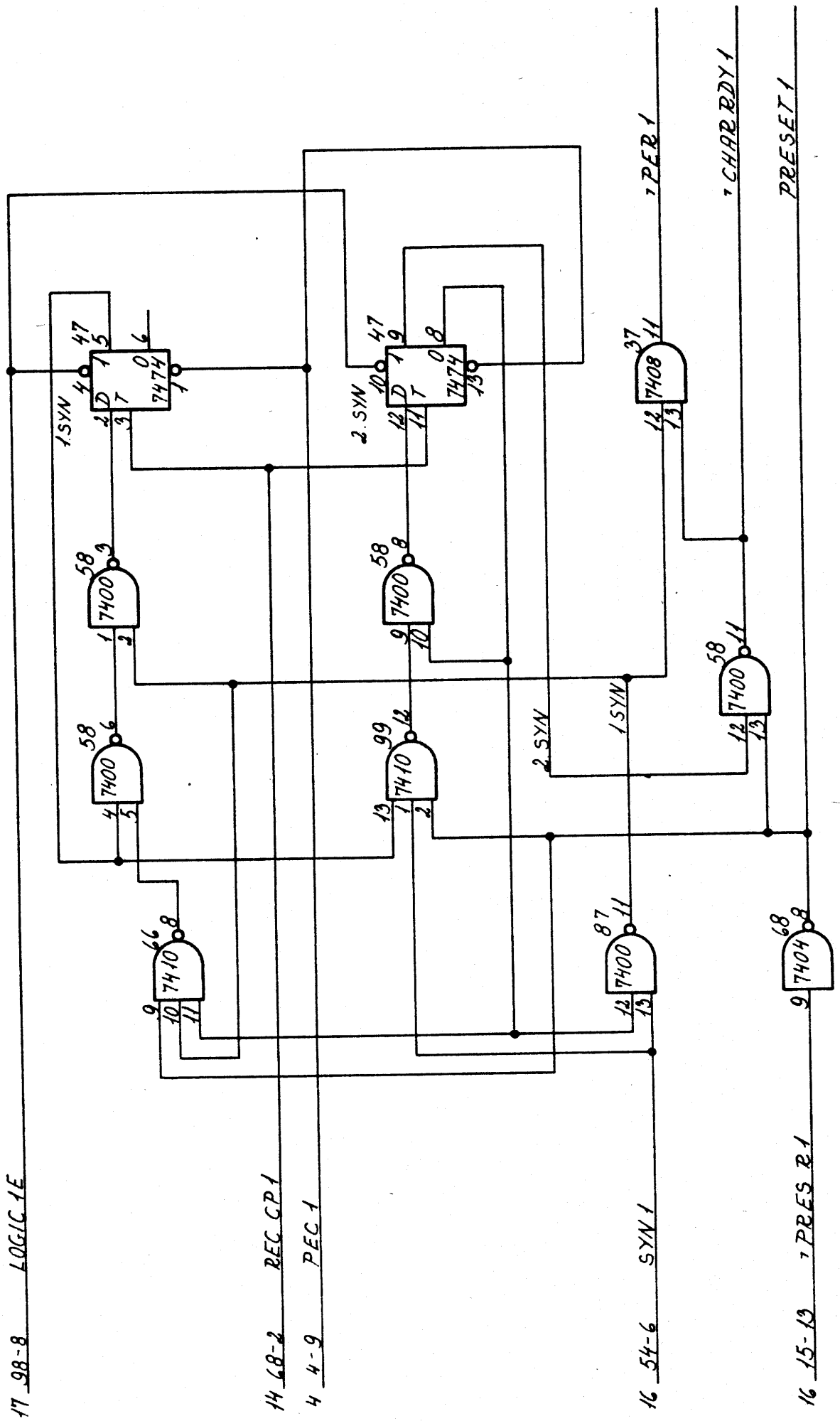


Signal	Destination	Description
REC CP 1	15,16	Receiver clock.
-,RCP 1	17	
XMT CP 1	13,14	Transmitter clock.
R/C 1	7	Status signal R. (test: C)
-,C 1	6	Modem control signal.
-,PE 1	13	Parallel enable. Byte synchronisation.

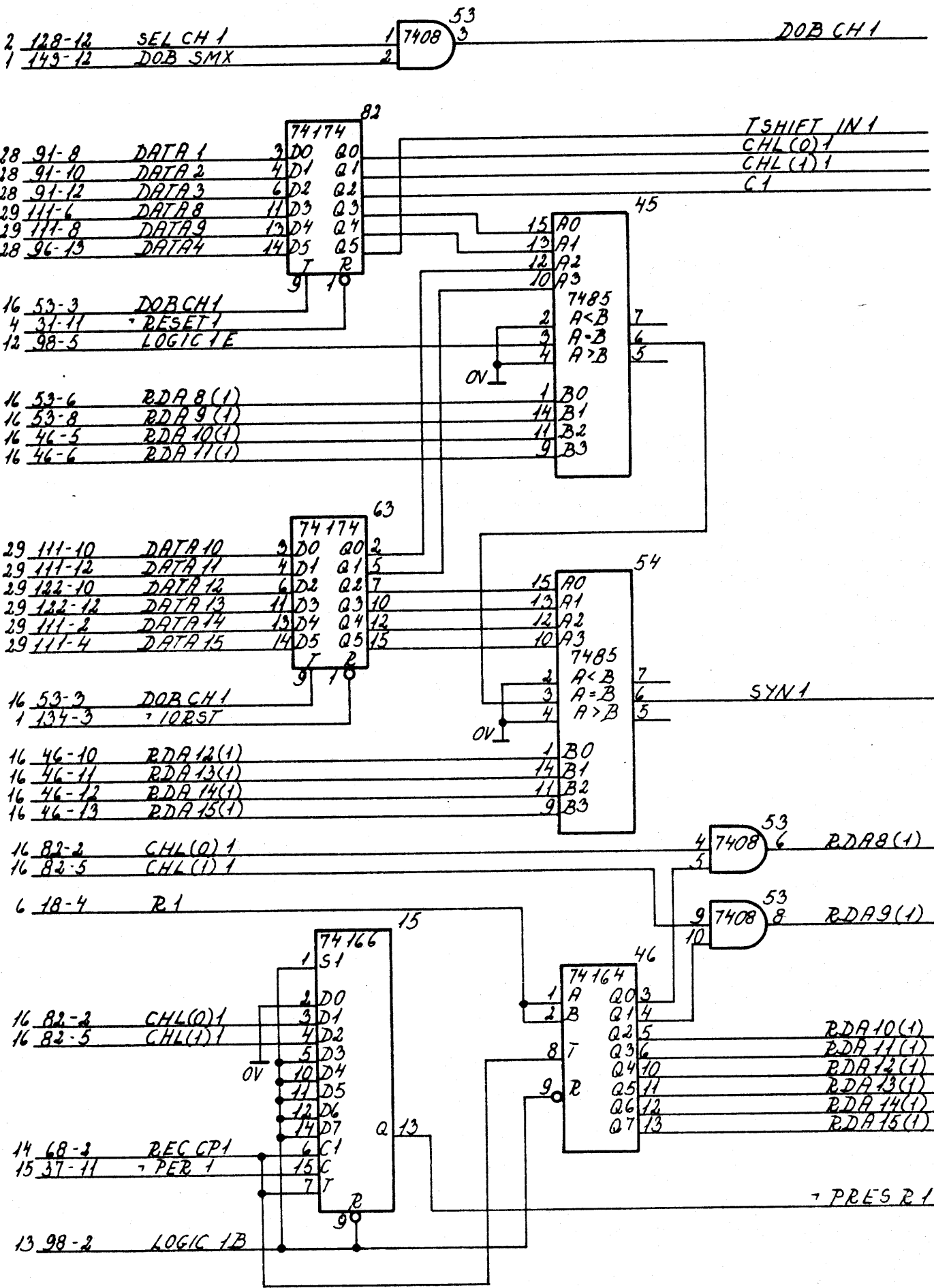


Signal	Destination	Description
-,PER 1	16	Receiver byte sunchronisation
CHARRDY 1	17	Character ready to be entered into the fifo.
PRESET 1	17	Receiver byte synchronization

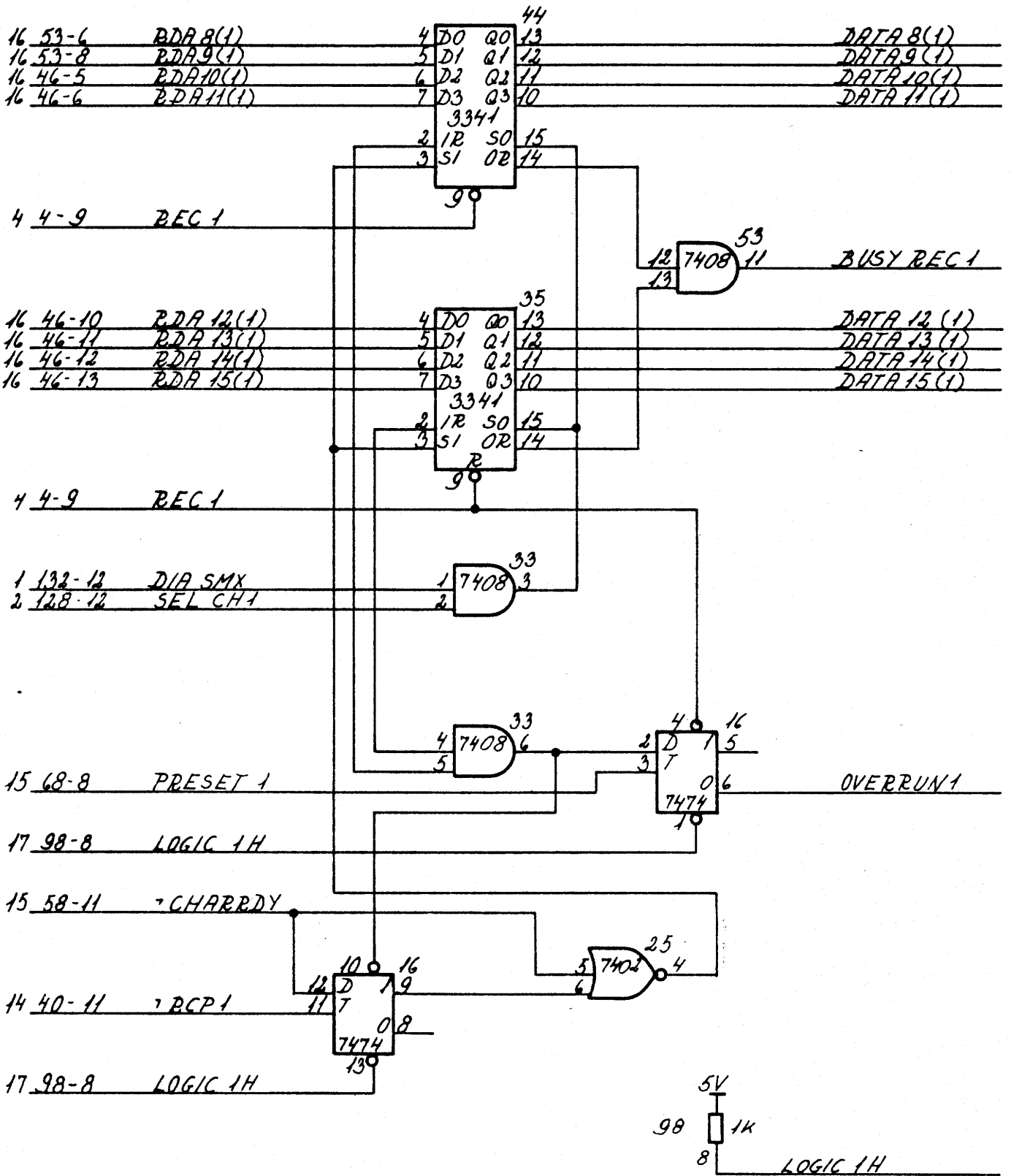
RECEIVER SYNC CONTROL CH1
LOGIC DIAGRAM



Signal	Destination	Description
DOB CH 1	16	Data out B, control register load.
TSHIFT IN 1	13	Transmitter level when not started.
CHL(0)-CHL(1) 1	16	Character length.
C 1	6	Modem control signal.
SYN 1	15	Sync byte found.
RDA (8:15) 1	16	Receiver data.
PRES R 1	15	Receiver byte synchronisation

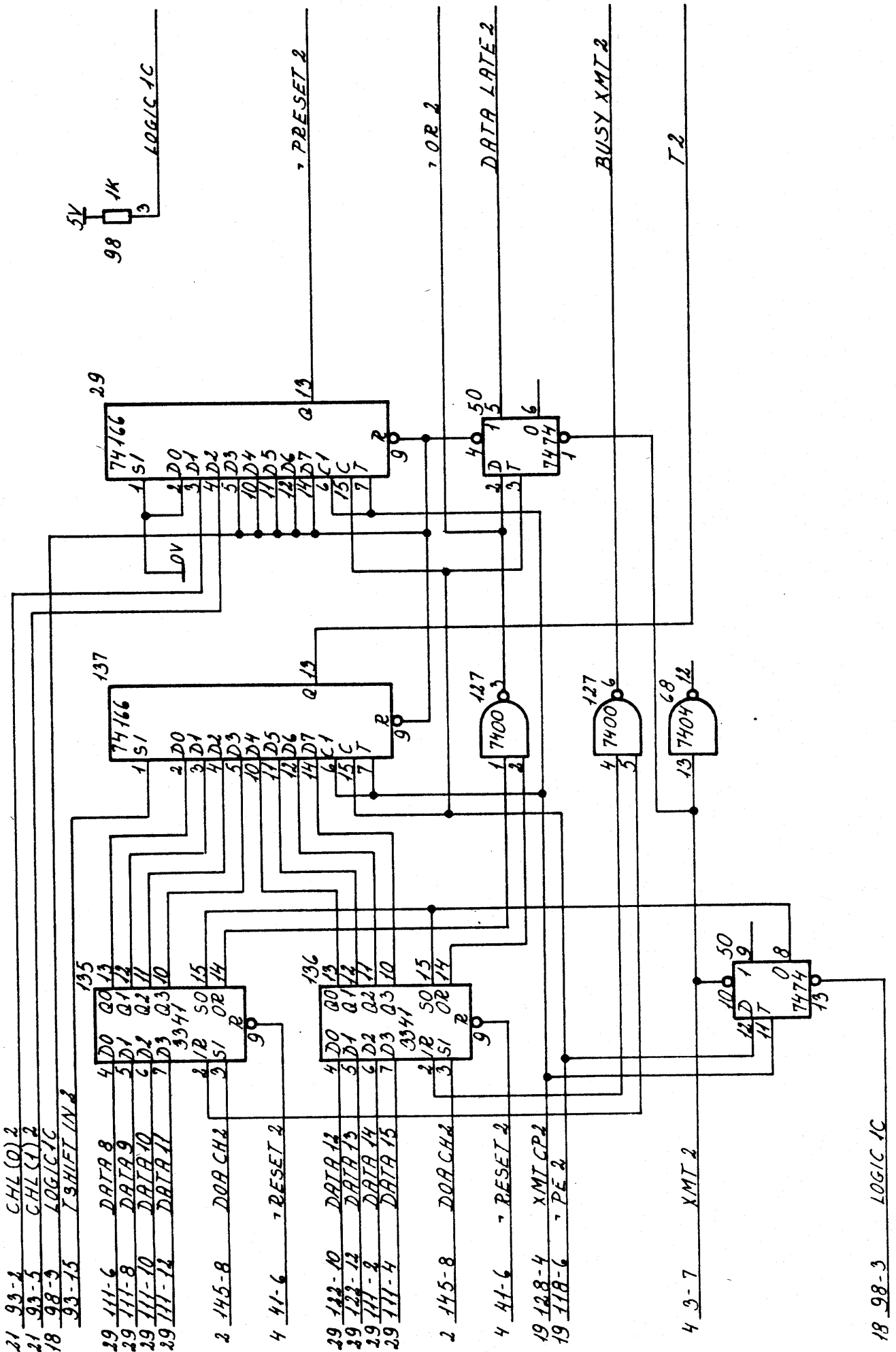


Signal	Destination	Description
DATA (8:15) 1	5	Receiver data to CPU.
BUSY REC 1	3	Receiver busy, no receiver data is ready.
OVERRUN 1	28	The fifo is not able to contain the incoming character.



Signal	Destination	Description
-,PRESET 2	19,22	Byte synchronisation.
-,OR 2	19	FIFO output ready.
DATA LATE 2	28	Data late error.
BUSY XMT 2	3	Transmitter not ready for receiving new data.
T 2	6	Serial transmit data.

TRANSMITTER REGISTERS & CONTROL CH2
LOGIC DIAGRAM



21 93-1 CHL(0)2

21 93-5 CHL(1)2

18 98-9 LOGIC IC

93-15 SHIFT IN 2

29 111-6 DATA 8

29 111-8 DATA 9

29 111-10 DATA 10

29 111-12 DATA 11

2 145-8 DOR CH2

4 41-6 RESET 2

29 122-10 DATA 12

29 122-12 DATA 13

29 111-8 DATA 14

29 111-4 DATA 15

2 145-8 DOR CH2

4 41-6 RESET 2

19 128-4 XMT CP2

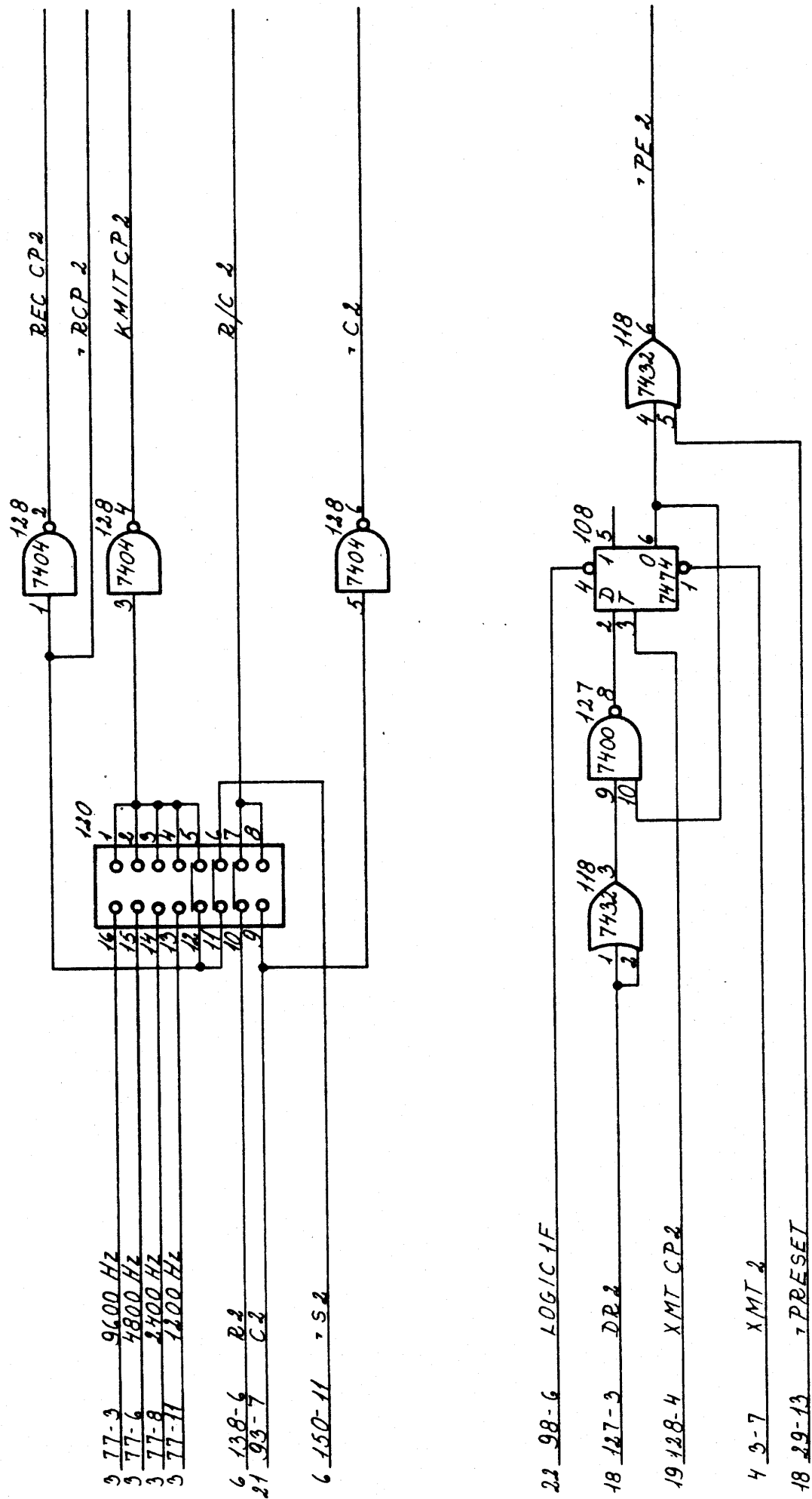
19 118-6 PE 2

4 9-7 XMT 2

4 9-7 XMT 2

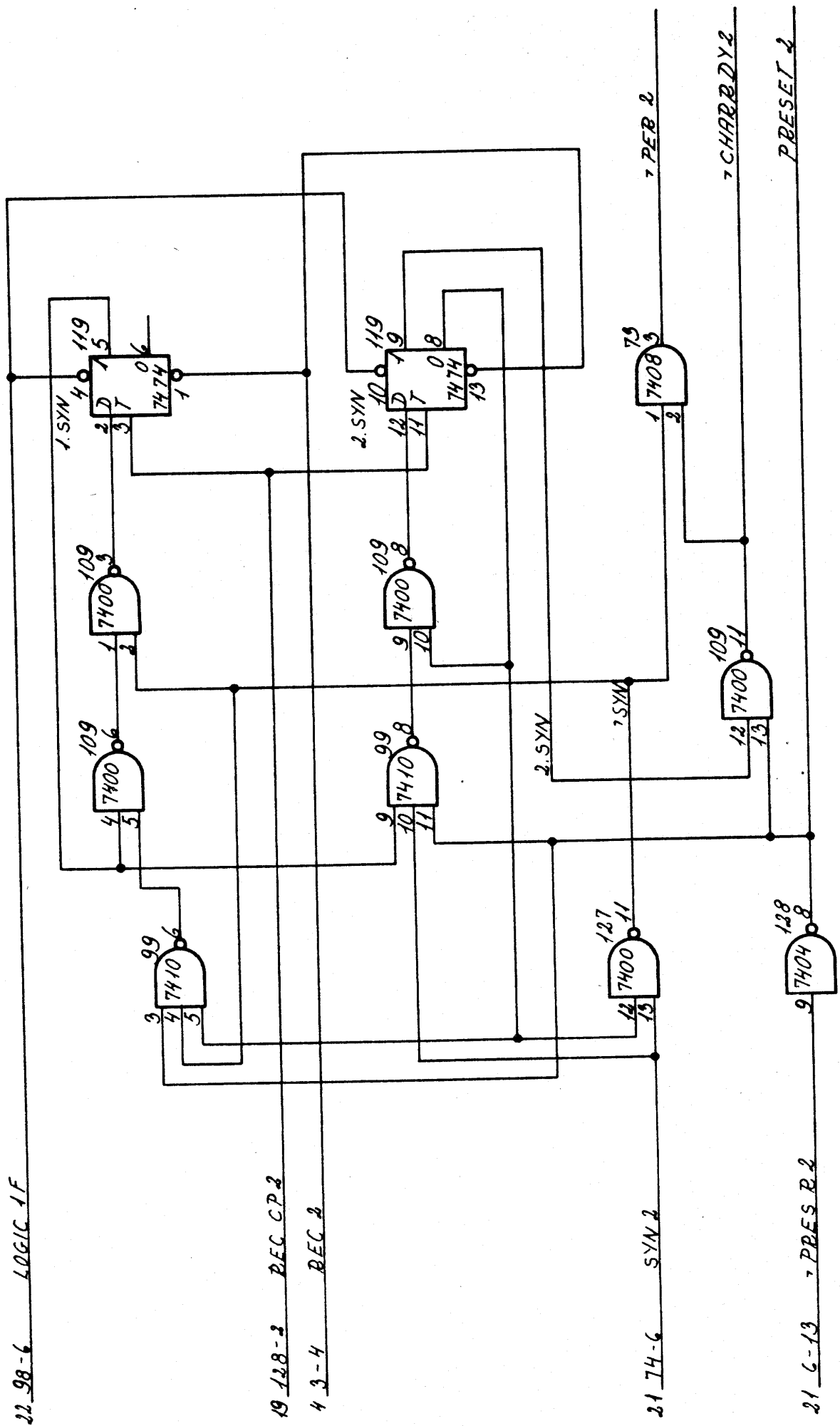
18 98-3 LOGIC IC

Signal	Destination	Description
REC CP 2	20,21	Receiver clock.
-,RCP 2	22	
XMT CP 2	18,19	Transmitter clock.
R/C 2	7	Status signal R. (test: C)
-,C 2	6	Modem control signal.
-,PE 2	18	Parallel enable. Byte synchronisation.



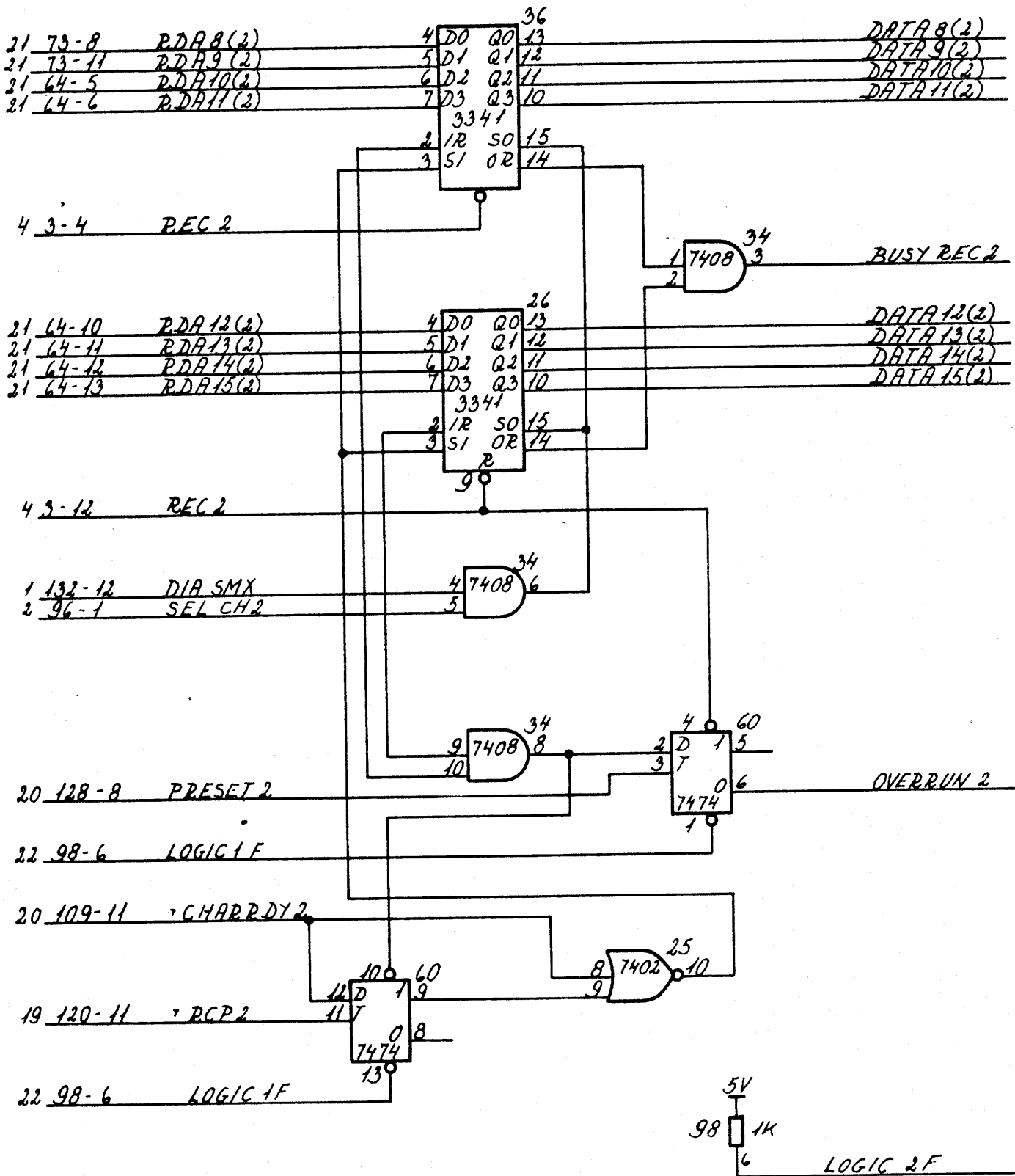
Signal	Destination	Description
-,PER 2	21	Receiver byte sunchronisation
CHARRDY 2	22	Character ready to be entered into the fifo.
PRESET 2	22	Receiver byte synchronisation

RECEIVER SYNC CONTROL CH2
LOGIC DIAGRAM



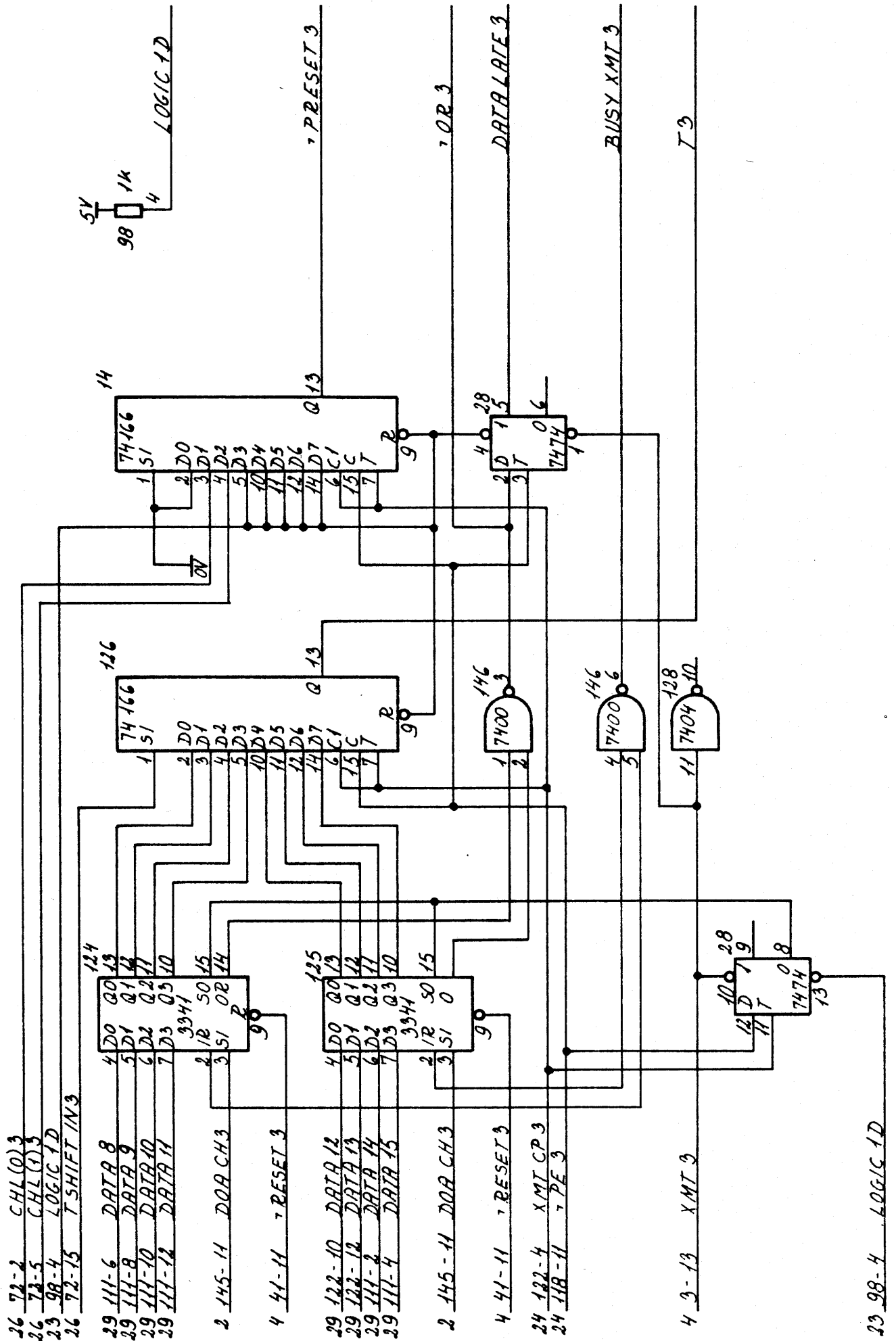
Signal	Destination	Description
DOB CH 2	21	Data out B, control register load.
TSHIFT IN 2	18	Transmitter level when not started.
CHL(0)-CHL(1) 2 21		Character length.
C 2	6	Modem control signal.
SYN 2	20	Sync byte found.
RDA (8:15) 2	21	Receiver data.
PRES R 2	20	Receiver byte synchronisation

Signal	Destination	Description
DATA (8:15) 2	5	Receiver data to CPU.
BUSY REC 2	3	Receiver busy, no receiver data is ready.
OVERRUN 2	28	The fifo is not able to contain the incoming character.



Signal	Destination	Description
-,PRESET 3	24,27	Byte synchronisation.
-,OR 3	24	Fifo output ready.
DATA LATE 3	28	Data late error.
BUSY XMT 3	3	Transmitter not ready for receiving new data.
T 3	6	Serial transmit data.

TRANSMITTER REGISTERS & CONTROL LOGIC DIAGRAM



26 72-2 CHL(0)3

26 72-5 CHL(A)3

23 98-4 LOGIC 1D

26 72-15 T SHIFT IN3

29 111-6 DATA 8

29 111-8 DATA 9

29 111-10 DATA 10

29 111-12 DATA 11

2 145-14 DOA CH3

4 41-11 RESET 3

29 122-10 DATA 12

29 122-12 DATA 13

29 111-2 DATA 14

29 111-4 DATA 15

2 145-14 DOA CH3

4 41-11 RESET 3

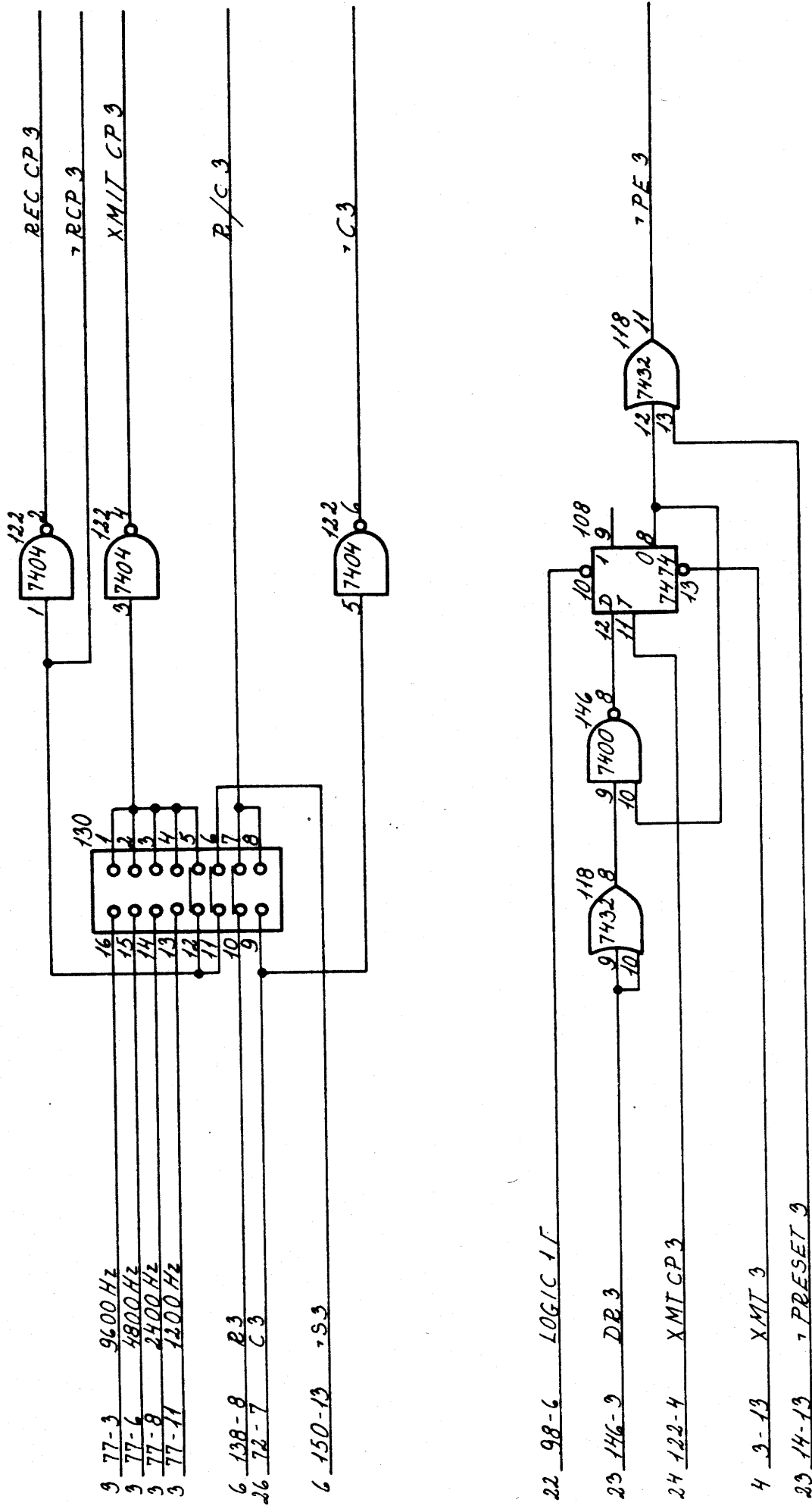
24 122-4 XMT CP 3

24 118-11 RESET 3

4 2-13 XMT 3

23 98-4 LOGIC 1D

Signal	Destination	Description
REC CP 3 -,RCP 3	25,26 27	Receiver clock.
XMT CP 3	23,24	transmitter clock.
R/C 3	7	Status signal R. (test: C)
-,C 3	6	Modem control signal.
-,PE 3	23	Parallel enable. Byte synchronisation.



Signal	Destination	Description
-,PER 3	26	Receiver byte synchronisation
CHARRDY 3	27	Character ready to be entered into the fifo.
PRESET 3	27	Receiver byte synchronisation

17 98-8 LOGIC 1H

24 122-2 REC CP 3

4 3-9 REC 3

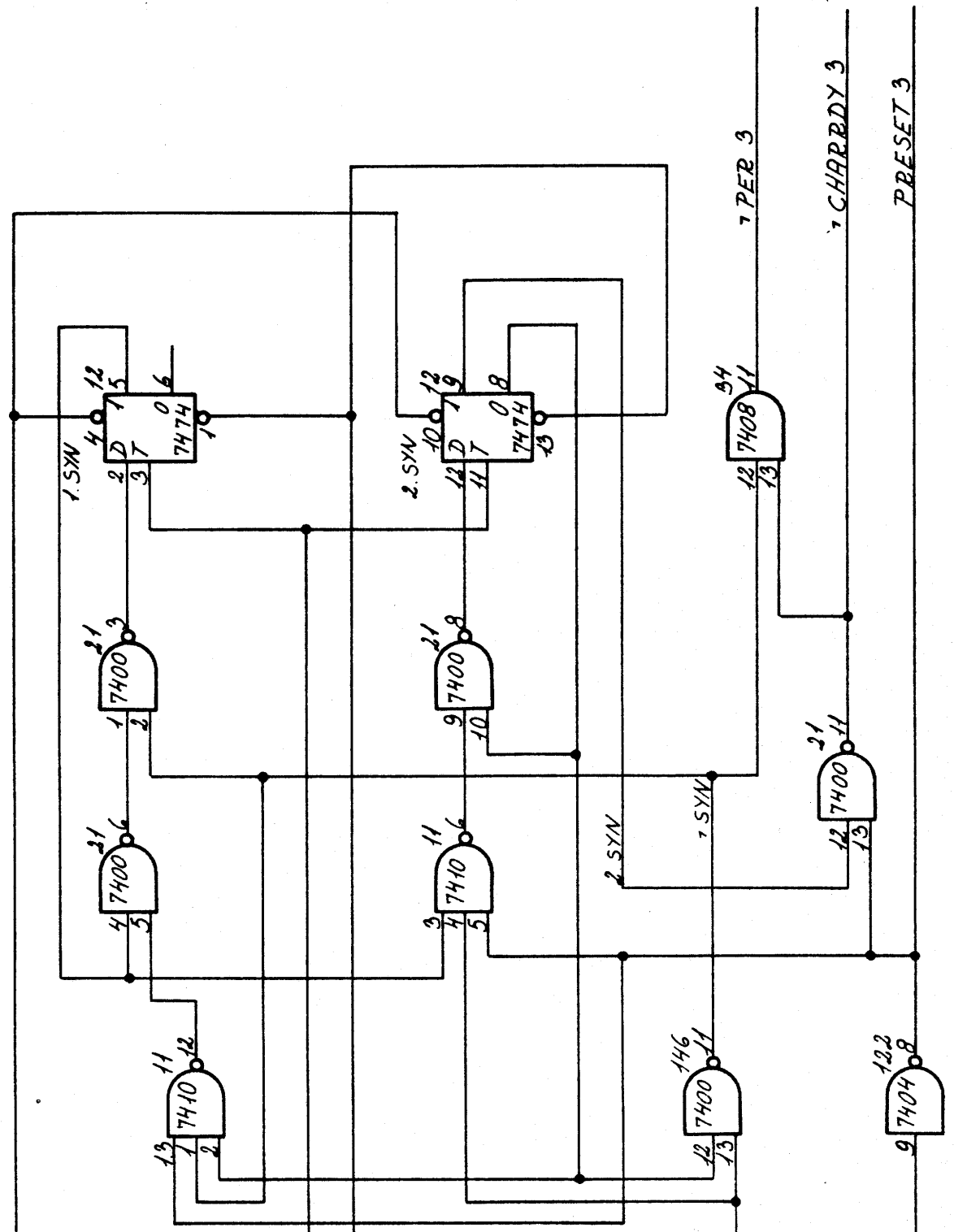
26 71-6 SYN 3

36 32-13 PRES B 3

7 PER 3

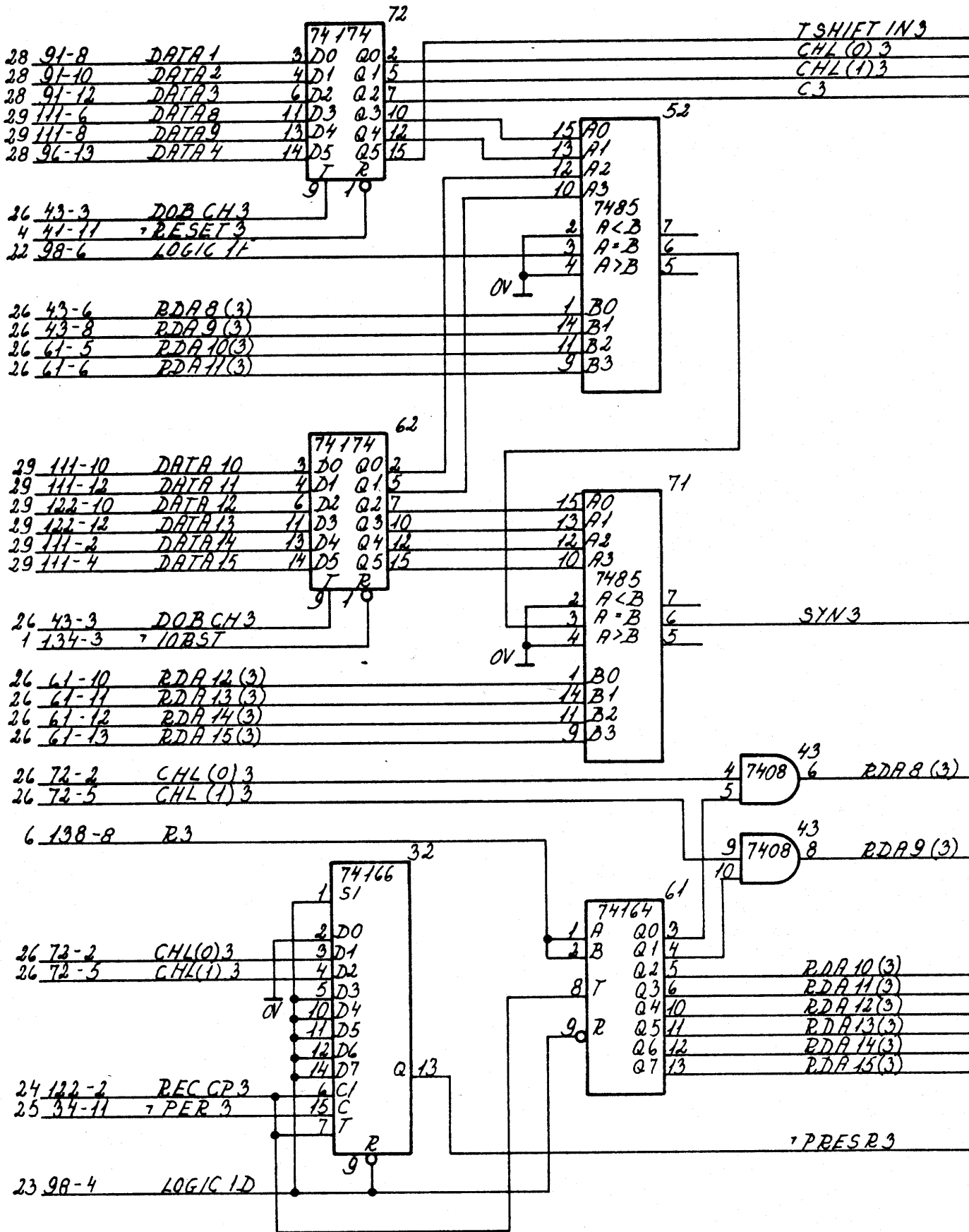
7 CHRRDY 3

PRESET 3

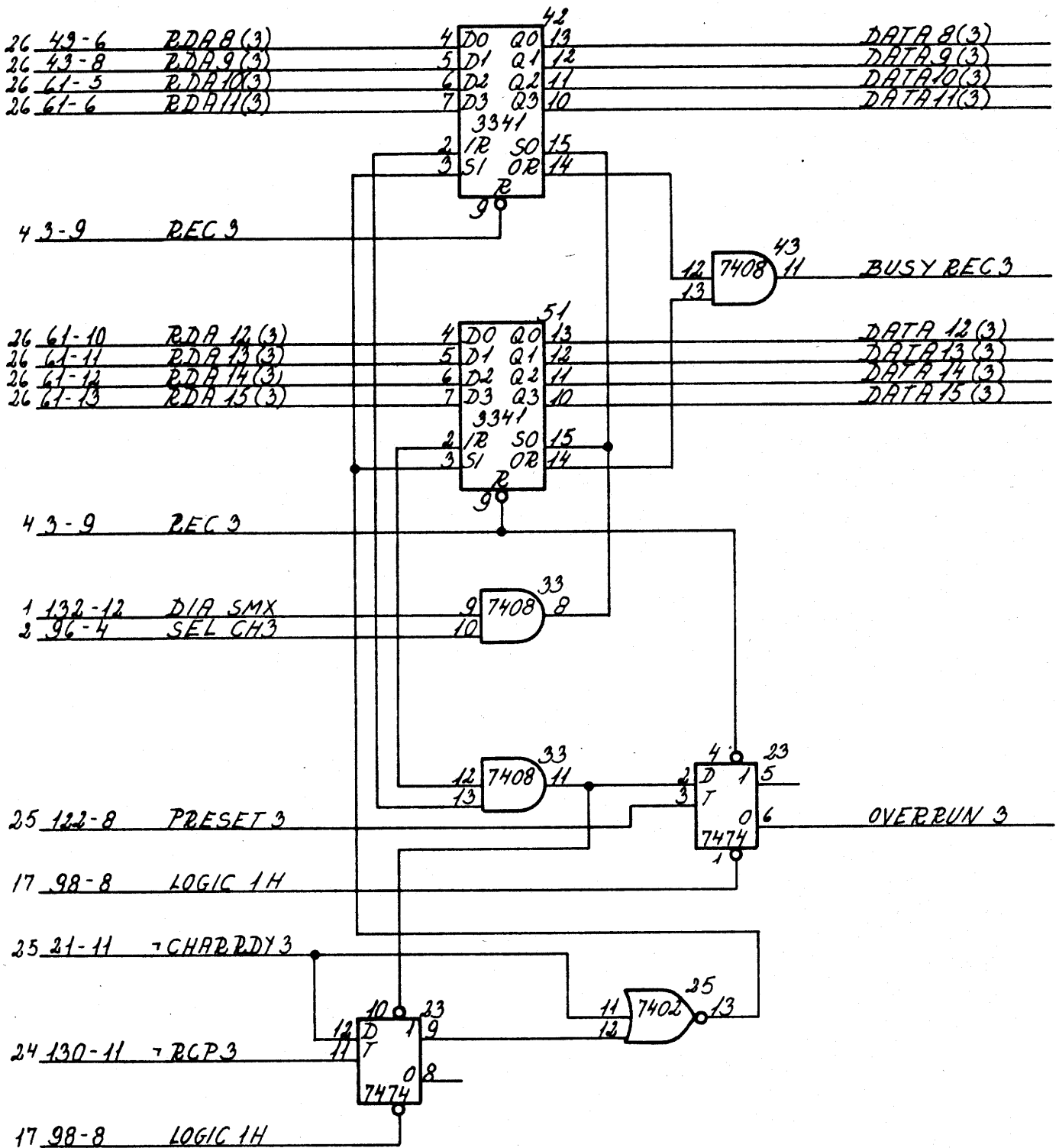


Signal	Destination	Description
DOB CH 3	26	Data out B, control register load.
TSHIFT IN 3	23	Transmitter level when not started.
CHL(0)-CHL(1) 3	26	Character length.
C 3	6	Modem control signal.
SYN 3	25	Sync byte found.
RDA (8:15) 3	26	Receiver data.
PRES R 3	25	Receiver byte synchronisation

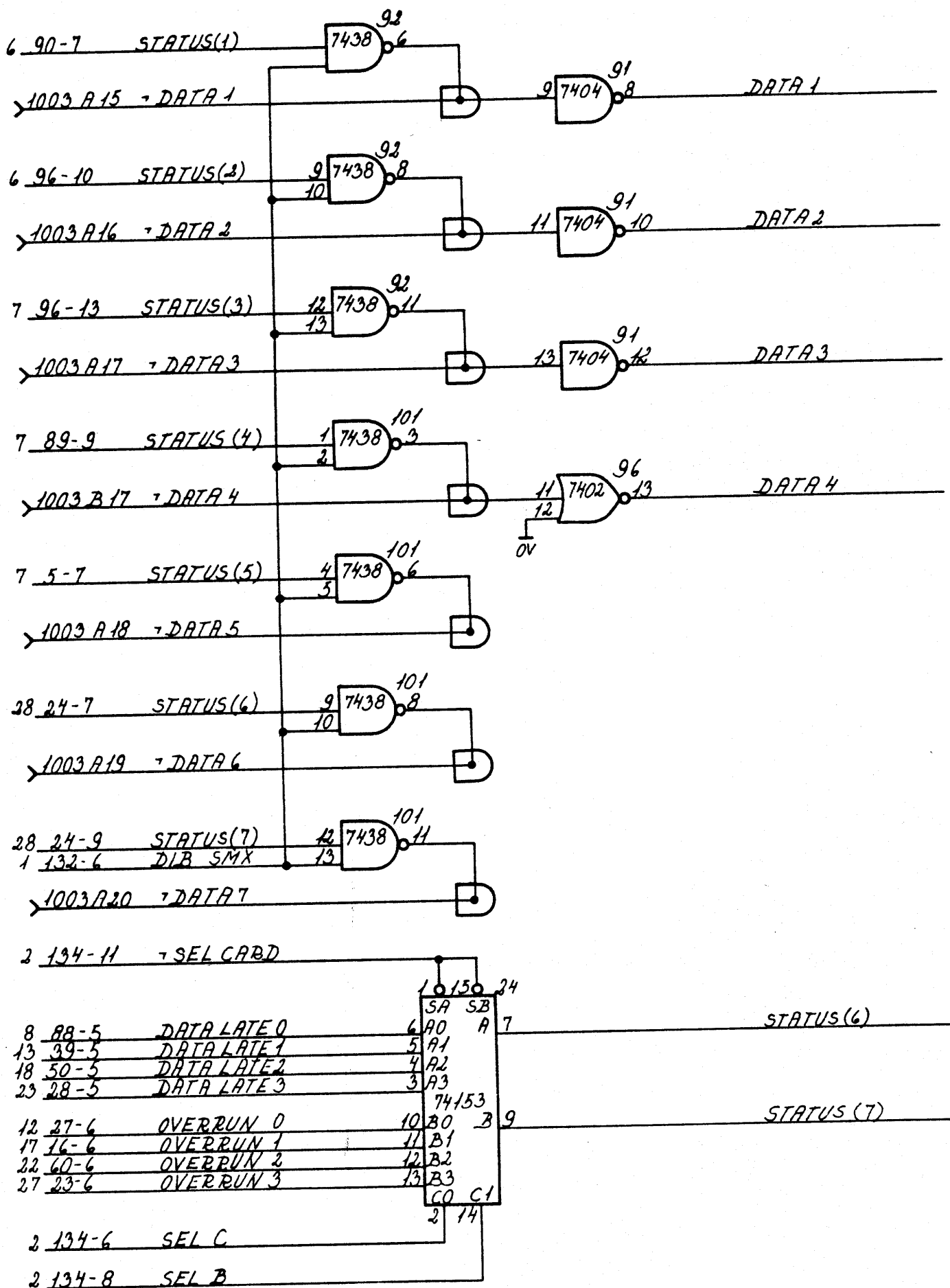
2 96-4 SEL CH 3 1 7408 43 3 DOB CH 3
 1 143-12 DOB SMX 2



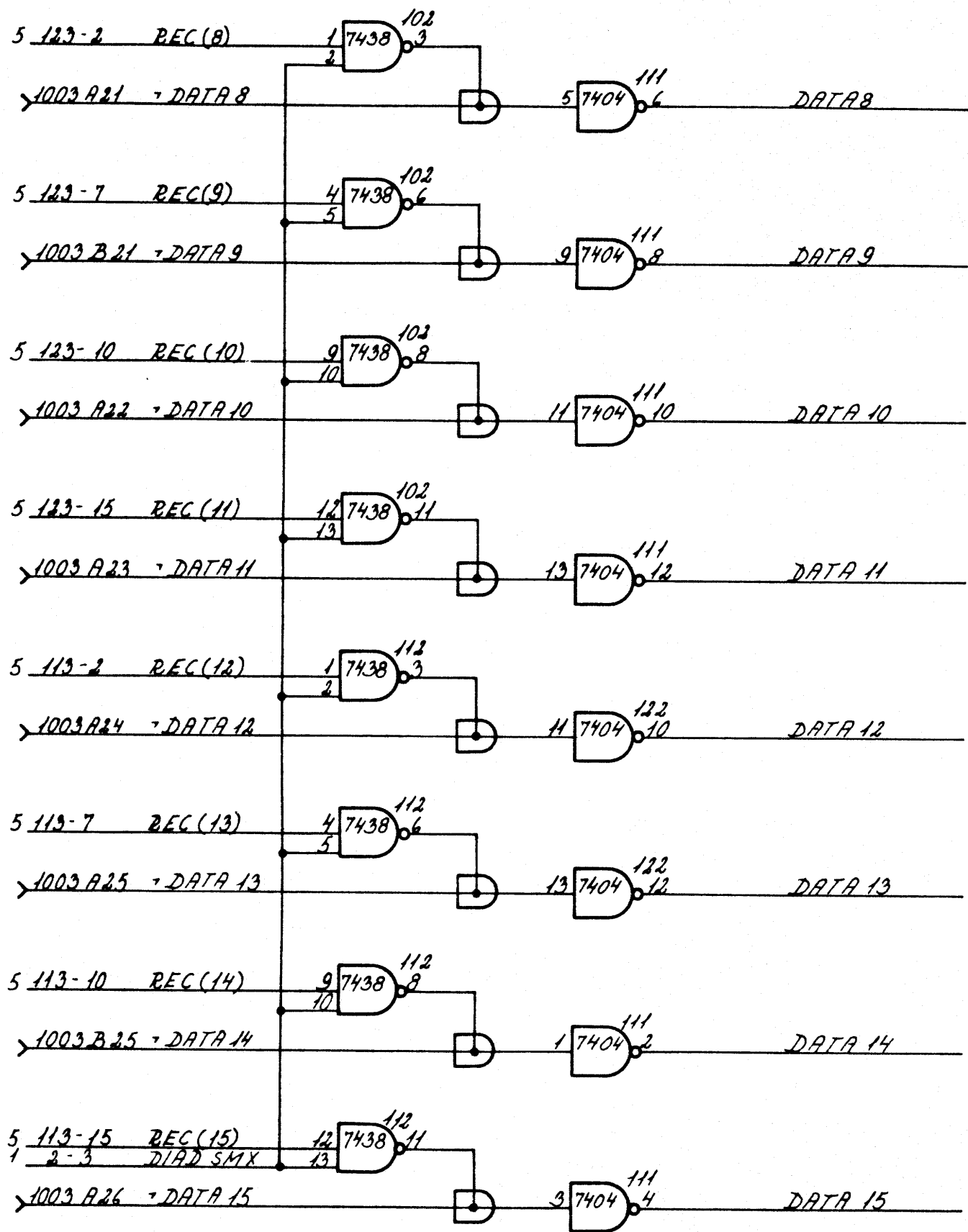
Signal	Destination	Description
DATA (8:15) 3	5	Receiver data to CPU.
BUSY REC 3	3	Receiver busy, no receiver data is ready.
OVERRUN 3	28	The fifo is not able to contain the incoming character.

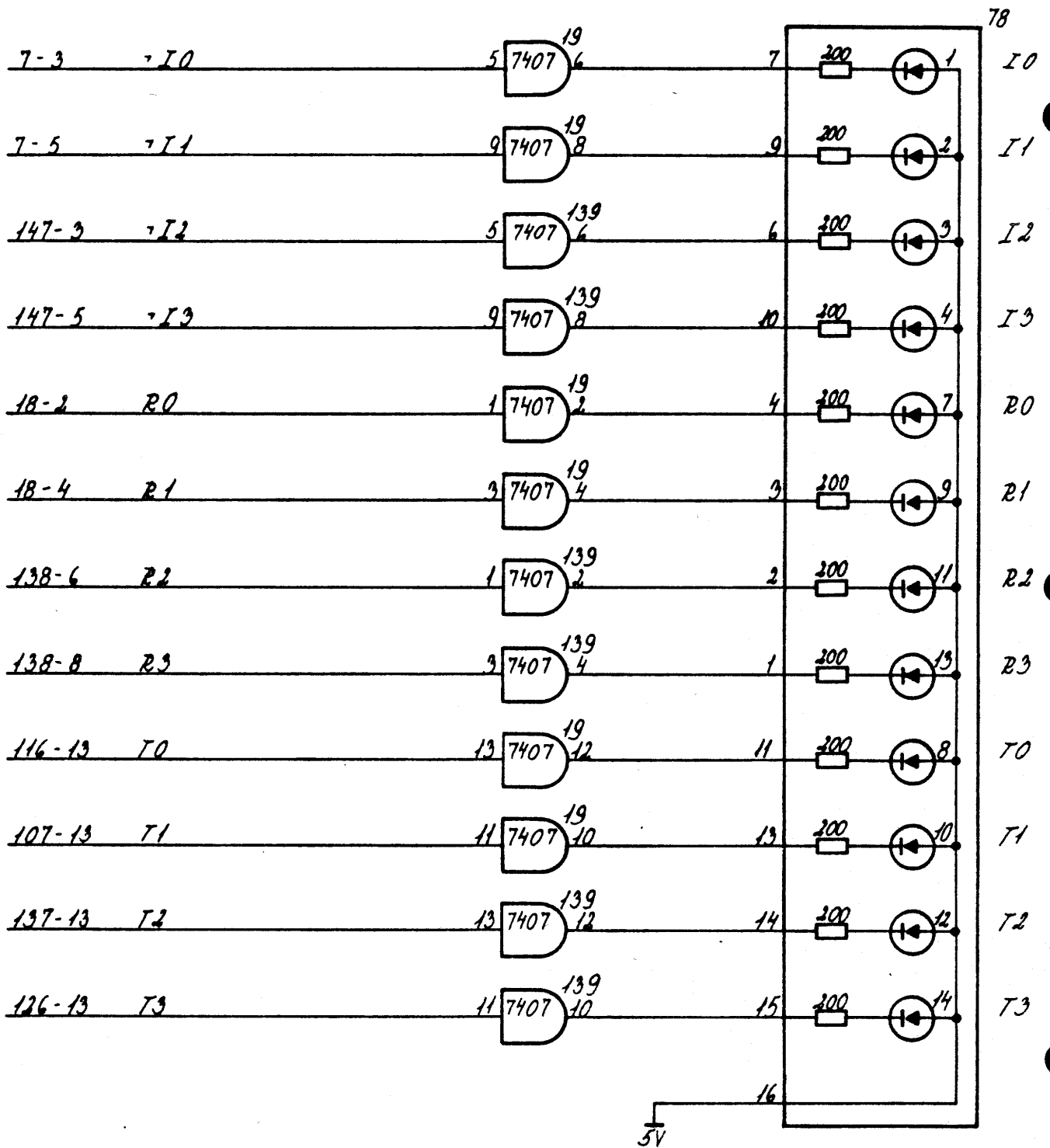


Signal	Destination	Description
DATA (1)-(3)	11,16,21,26	Data to control-register.
STATUS (6)-(7)	28	Status register.



Signal	Destination	Description
DATA (8)-(15)	2,8,13,18,23	Data to transmitter fifo, and channel selector.

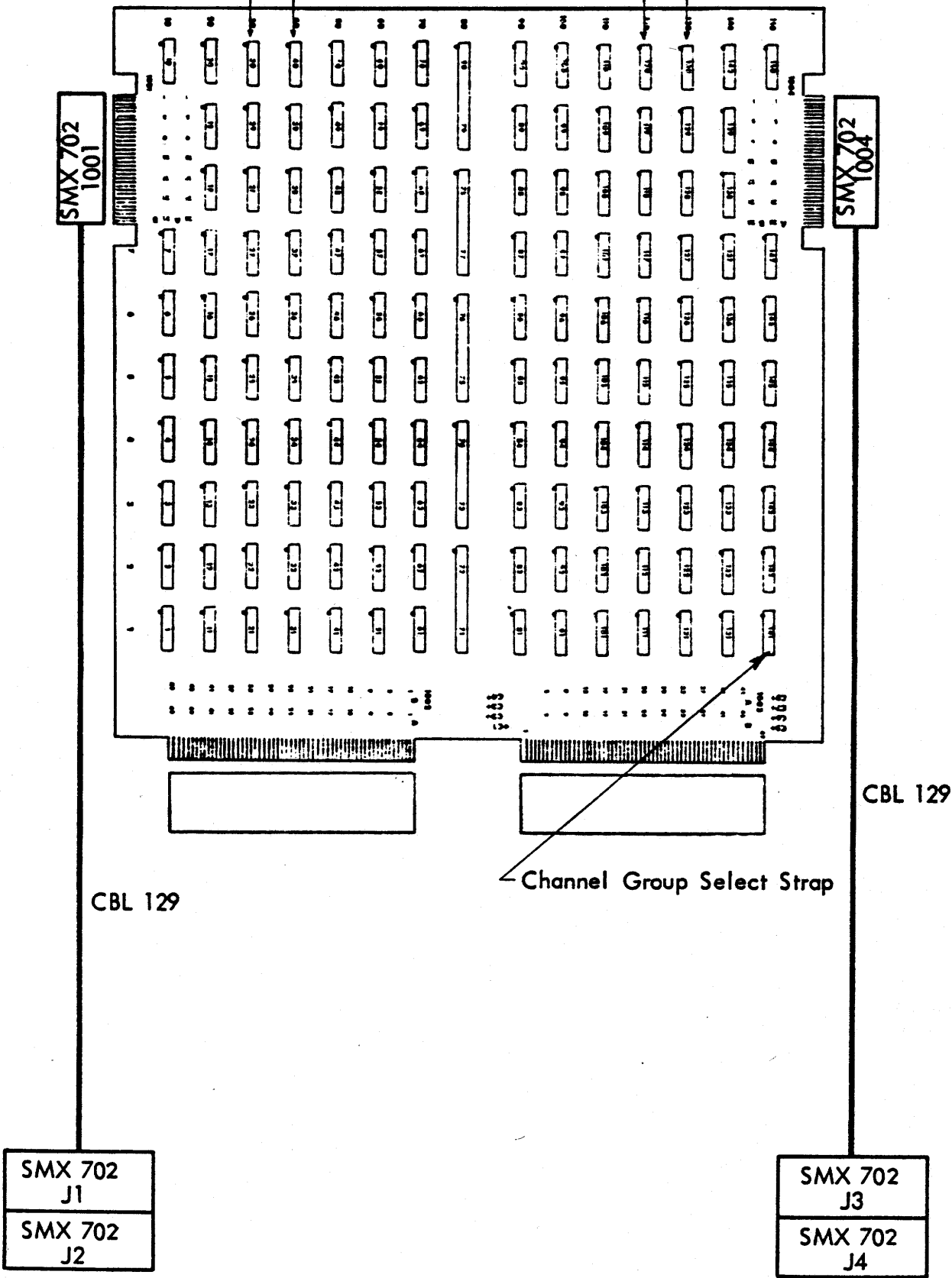




LMJ RGA
 820526 820526

Clock Select Straps

0 1 ← channel no. → 2 3



5. PLUG LISTS

5.

INTERNAL CABLE (CBL 129)

2 x 25 WAY

UPPER 19 WAY

EDGE CONNECTORCANNON CONNECTOR

A2	T(A)	2
A3	R(A)	3
A4	T(B)	4
A5	R(B)	5
A6	I(A)	6
A7	gnd	7
A8	I(B)	8
A9	S(B)	15
A10	S(A)	17
A11	C(A)	18
A12	C(B)	19

LOWER 19 WAY

CANNON CONNECTOR

A15	T(A)	2
A16	R(A)	3
A17	T(B)	4
A18	R(B)	5
A19	I(A)	6
A20	gnd	7
A21	I(B)	8
A22	S(B)	15
A23	S(A)	17
A24	C(A)	18
A25	C(B)	19

MODEM CABLE

SMX702		MODEM
J1 .J2 .J3 .J4		(ISO4903)
1	shield	1
2	T(A)	2
18	C(A)	3
3	R(A)	4
6	I(A)	5
17	S(A)	6
-	not used	7
7	gnd	8
4	T(B)	9
19	C(B)	10
5	R(B)	11
8	I(B)	12
15	S(B)	13
-	not used	14
-	not used	15



RETURN LETTER

SMX702, Binary Synchronous Communication

**Title: Multiplexer - X.21
Technical Manual**

RCSL No.: 44-RT2025

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