RCSL No: 44-RT2026

Edition: May 1982

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Title:

SMX702
Binary Synchronous Communications Multiplexer - X.21
Reference Manual

RCSL 42-i1905

A/S REGNECENTRALEN
af 1979

Keywords:

SMX702, BSC, synchronous communication, data transmission, Datex, X.21.

Abstract:

This paper describes the logical structure of the receivers and the transmitters in the binary synchronous communications controller SMX702.

(24 printed pages)

Printed by A/S Regnecentralen af 1979, Copenhagen

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1. MAIN CHARACTERISTICS

1.1 Description

The SMX702 is a binary synchronous communications multiplexer consisting of up to 32 channels, each containing a receiver and a transmitter.

The 32 channels are grouped in 4 channels on each hardware board, which is group-selected by solder straps.

Interfaces on all channels are X.24/X.27 which enables possibility for connection to the public data network (NPDN), using X.21 call and wait call procedures.

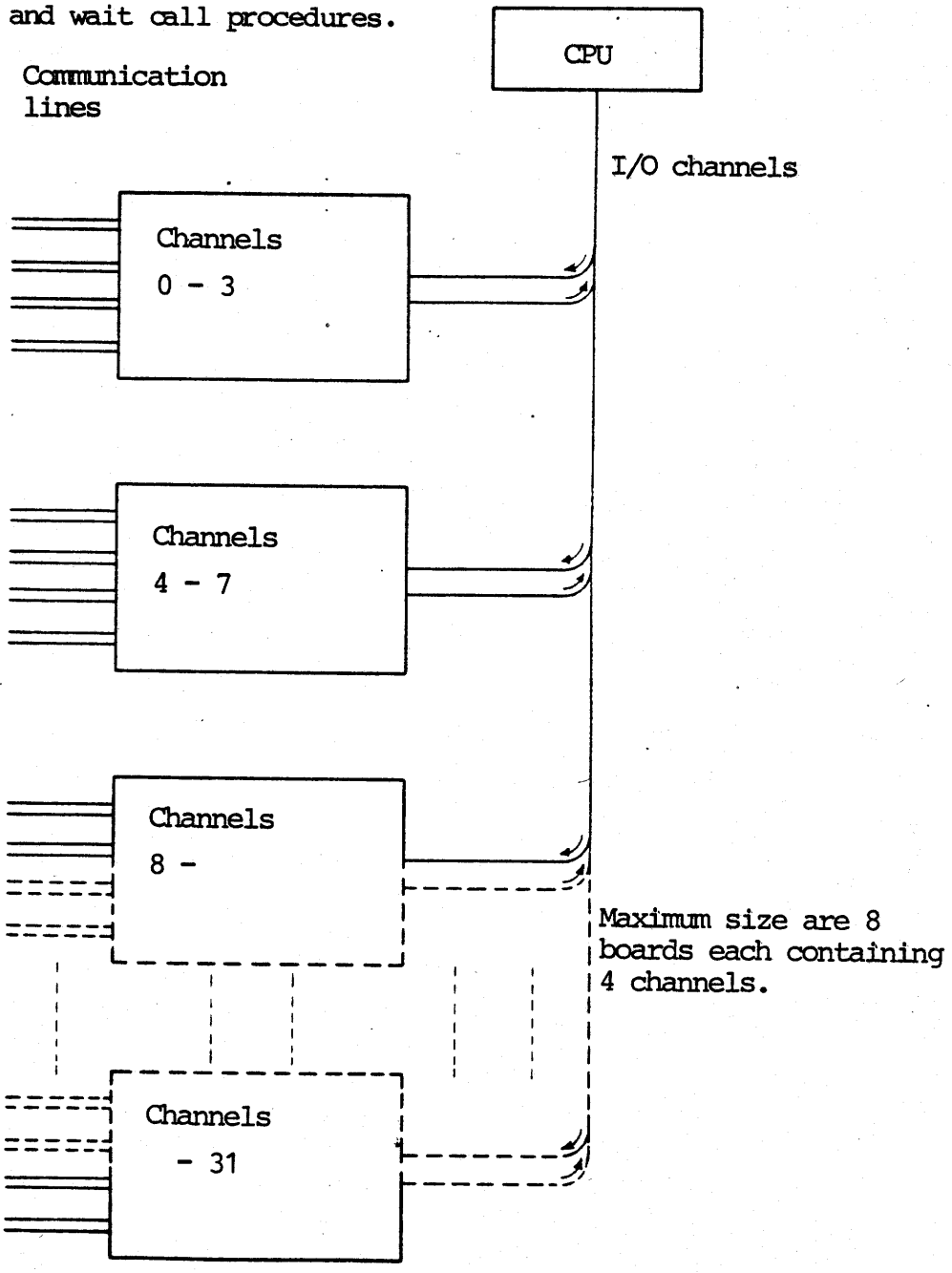


Figure 1: Expansion from 4 channels to 32 channels.

In all channels the receiver and the transmitter can be operated independently and simultaneously under full program control. This means that operation in full or half duplex mode is dependent only on the communications structure and the modem equipment in use.

1.2 Data Formats

1.2

The BSC multiplexer transfers information to the CPU through the normal I/O channel. The characters are right-justified in the data word and constist of 6, 7 or 8 bits. The characters are received from the communication line in serial way, bit by bit, with the least significant bit (LSB) received first. The characters are transmitted with the LSB first.

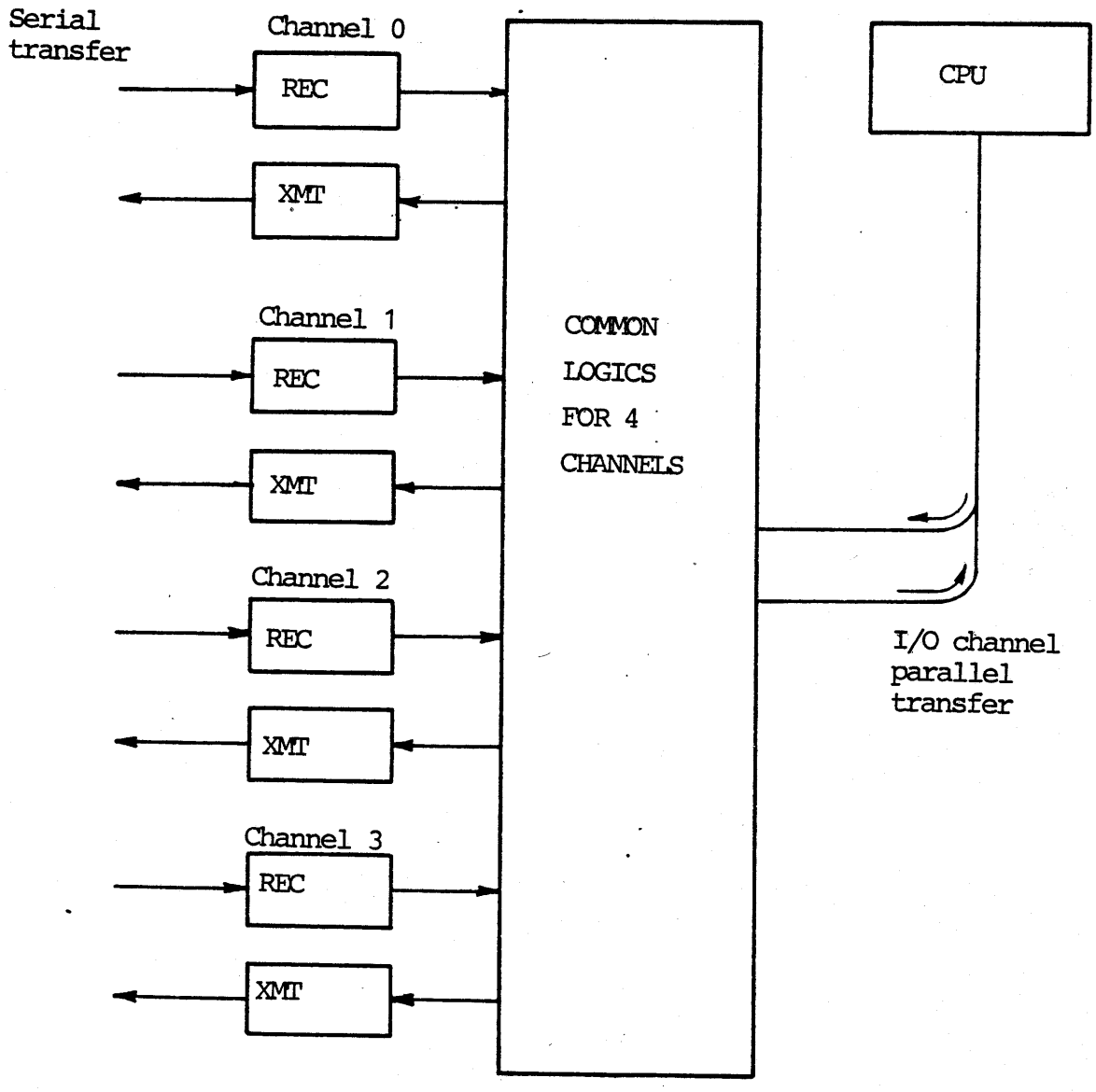


Figure 2. Data Formats.

2. PERFORMANCE SPECIFICATIONS 2.

2.1 Transmission Speed 2.1

When SMX702 is connected to a modem, this supplies the receive and transmit clocks to a channel.

The maximum transmission speed is 9600 bps. The clock from the SMX702 can be selected by solder straps to either 1200, 2400, 4800 or 9600 bps, each channel independently. For further information about the solder straps refer to 4.3.

2.2 Interface Specifications 2.2

All data and control signals between the SMX702 and the modem are in accordance with the CCITT recommendation X.24, which defines the interchange circuits

The following circuits are used:

G Signal ground
T Transmit
R Receive
C Control
I Indication
S Signal element timing

3. LOGIC SPECIFICATION

3.1 Channel Selection

The BSC multiplexer has the fixed device code 60 (octal) in all I/O instructions.

A DOC instruction will select and allocate one channel to the I/O bus, and all other instructions will be routed to this channel as shown in fig. 3. This will last until another channel is selected.

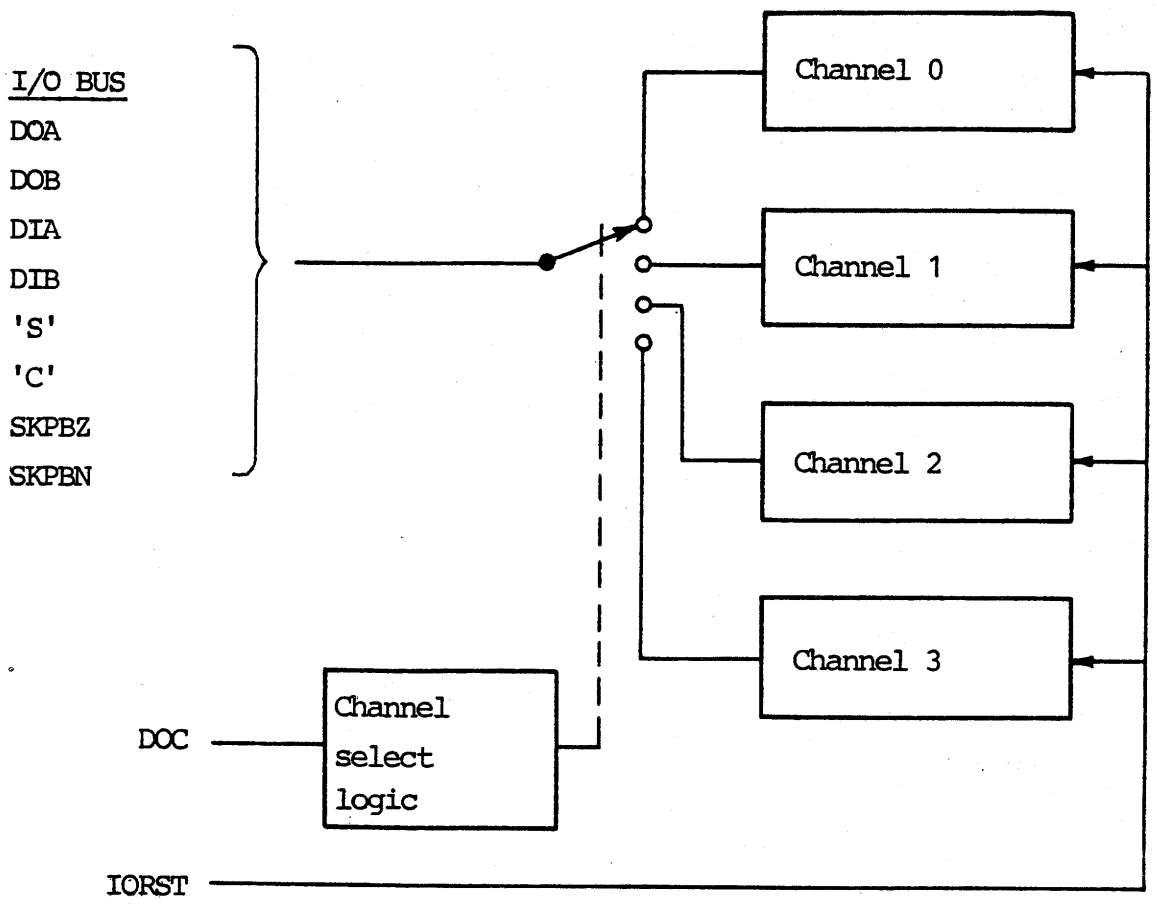


Figure 3: Channel selection.

The DOC instruction loads the channel select register with the contents of the specified accumulator.

DOC AC, SMX
AC

X	X	X	X	X	X	X	X	X	X	GROUP			CH		R/X
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

3.1.1 Select GROUP

The channel GROUP is solder strapped on a specified controller board.

BITS			ABSOLUTE CHANNEL NUMBERS
10	11	12	
0	0	0	0 - 3
0	0	1	4 - 7
0	1	0	8 - 11
0	1	1	12 - 15
1	0	0	16 - 19
1	0	1	20 - 23
1	1	0	24 - 27
1	1	1	28 - 31

3.1.2 Select Relative CHANNEL

The channel number is selected within one group. To get the absolute channel number add the first channel number in the selected group to the relative channel number.

BITS		ABSOLUTE CHANNEL NUMBERS
13	14	
0	0	0
0	1	1
1	0	2
1	1	3

3.1.3 Select R/X - Receiver/Transmitter

3.1.3

BIT 15	Selects:
0	Receiver
1	Transmitter

The last bit in the DOC instruction is used to start or stop a receiver or a transmitter in a channel by adding an 'S' or a 'C' modification to the DOC instruction, or to another instruction, if the receiver or the transmitter was selected in a previous instruction.

The same bit is used to select a receiver or a transmitter in SKIP BUSY instructions. This is used to sense room in the buffers (refer to 3.2 and 3.3).

An example will illustrate this channel selection:

Consider a BSC multiplexer consisting of 3 controller boards to make a total number of channels of 12.

For sensing on the BUSY flag in the transmitter in channel 5, the accumulator for the DOC instruction will look like this:

```
  DOC  AC, SMX
    AC
```

X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

The channel GROUP is 4-7, and bits 10, 11 and 12 are then 001.

The relative channel number within this group is 5 - 4 = 1, and bits 13 and 14 are then 01.

As the transmitter is selected, bit 15 is a logical 1.

Control of channel 10 by a DOB instruction must have this previous DOC instruction:

DOC AC, SMX

AC

X	X	X	X	X	X	X	X	X	X	0	1	0	1	0	X
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

The channel GROUP is 8-11, and bits 10, 11 and 12 are then 010.

The relative channel number within this group is 10 - 8 = 2, and bits 13 and 14 are then 10.

This DOB instruction goes for both the receiver and the transmitter, and then bit 15 is not used.

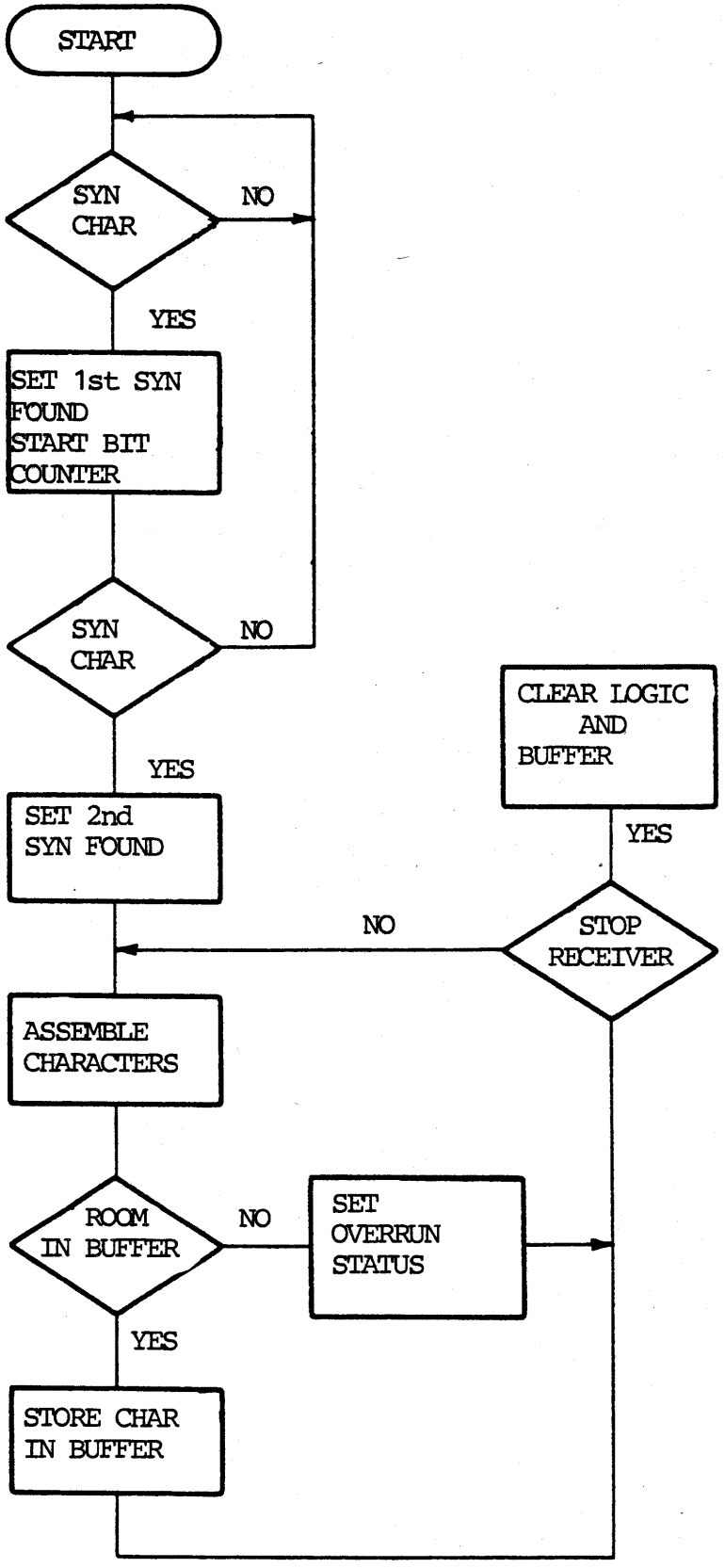


Figure 4: Receiver flow diagram.

A start command causes the receiver to monitor the incoming bit stream continuously until it meets two consecutive SYN-characters as specified by the program.

It then starts assembling the incoming bits into characters (6, 7 or 8 bits) and stores them in a buffer (first-in first-out memory: FIFO) which has room for 64 characters. As soon as a character is ready at the output of the buffer, the BUSY flag is set, and the program can transfer the character to an accumulator.

If the buffer runs empty, the BUSY flag remains low (zero).

The DIA instruction takes the character from the buffer and loads it into the specified accumulator, right-justified, and the next character in the input stream runs automatically upwards in the buffer.

3.3 Transmitter Operation

3.3

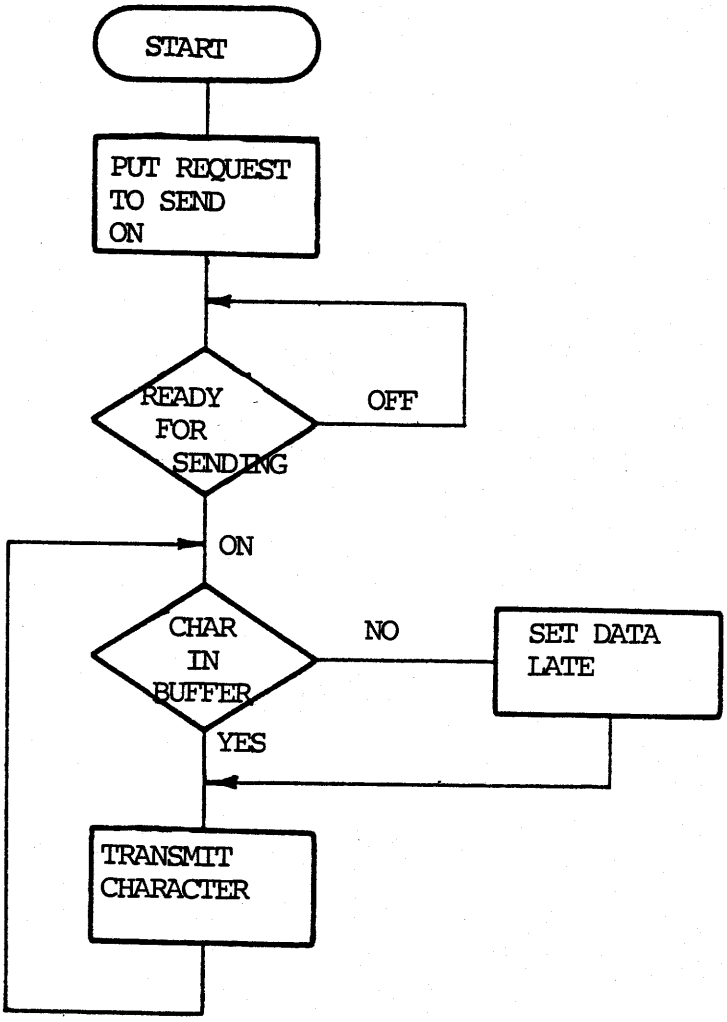


Figure 5: Transmitter flow diagram.

When the transmitter is started, it waits for there to be characters in the output buffer, which has room for 64 characters, like the receiver.

As soon as these conditions are fulfilled, the transmitter transfers the characters to a bit stream.

Characters are stored from the program into the buffer by a DOA command. If there is room in the buffer, the BUSY flag is zero '0', and if there is no room, the BUSY flag remains high '1'.

3.4 Control Registers

The data formats in the SMX702 are controlled by a DOB instruction. First the channel must be selected in a DOC instruction.

DOB AC, SMX

X	CHL	C	T	X	X	X	SYN - CHAR
0	1 2	3	4	5	6	7	8 9 10 11 12 13 14 15

3.4.1 Character Length

The channel can handle 6, 7 or 8 bit characters, i.e. the bits in a received character are right-justified in the hardware, and leading bits that are not used are always zero.

The transmitter will only transmit the number of bits in a character that is specified in the character length.

Leading bits are not transmitted if the character length is less than 8 bits.

BITS		CHARACTER	RECEIVED	TRANSMITTED
1	2	LENGTH	CHARACTER	CHARACTER
0	0	6 BITS	0 0 | 6 BIT CHAR 8 15	X X | 6 BIT CHAR 8 15
0	1	NOT USED		
1	0	7 BITS	0 | 7 BIT CHAR 8 15	X | 7 BIT CHAR 8 15
1	1	8 BITS	8 BIT CHAR 8 15	8 BIT CHAR 8 15

Figure 6: Handling of character length.

3.4.2 C (Control) 3.4.2

Bit 3 is the modem control signal C (control). When this bit is specified as a logical '1', the signal goes into ON condition. When taken to a logical '0', the signal goes into OFF condition.

3.4.3 T (Transmit) 3.4.3

Bit 4 defines the value of T (transmit data) when the transmitter is not started.

3.4.4 SYN-CHAR 3.4.4

Bits 8-15 specify the character at which the receiver should be synchronized. This character cannot be selected as all ones, as this character is the idle state of the line (PAD-character).

When 6 or 7 bit characters are used, the leading unused bits must be zero.

3.5 Channel Control

3.5.1 Receiver Control

The receiver is started by an 'S' (start) modification in an I/O instruction.

If the start modification is put on another instruction than DOC, the previously selected receiver (or transmitter) is started (refer to 3.2 and 3.3).

In the same way a receiver is stopped by applying a 'C' (clear) modification to an instruction. After a stop command the receiver logic goes into the idle state, and the input buffer is cleared.

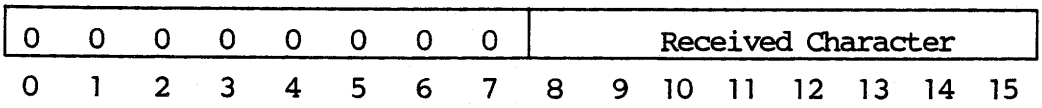
3.5.2 Received Data

When the receiver has started assembling characters, it stores them in the input buffer. As soon as the first character is ready at the buffer output, the BUSY flag is raised, and this character can be loaded into a specified accumulator by a DIA instruction.

If the BUSY flag is raised again, the next character is ready, etc.

DIA AC, SMX

AC



Example of program part:

```
DOC Ø, SMX ; Select Appropriate Receiver
SKPBN, SMX ; Character Ready?
JMP - - -  ; NO, Return
DIA 1, SMX ; YES, Load It
STA 1, MEM ; STORE It
SKPBN, SMX ; One More Ready
JMP - - -  ; NO, Return
DIA 1, SMX ; YES
          etc.
```

If the BUSY flag remains low, no more characters are in the buffer at this moment.

If the input buffer becomes completely full, an OVERRUN flag will be set at the next character that is collected from the input stream. Then this and the following characters are lost. OVERRUN is a status information that can be sensed by a DIB instruction (refer to 3.6).

3.5.3 Transmitter Control

3.5.3

The transmitter is started by an 'S' (start) modification in an I/O instruction.

If the start modification is put on another instruction than DOC, the previously selected transmitter (or receiver) is started (refer to 3.3 and 3.2).

When the transmitter is started, it waits for some characters in the output buffer.

As soon as this happens, the transmission starts.

In the same way a transmitter is stopped by applying a 'C' (clear) modification to an I/O instruction. After a stop command the transmitter logic goes into the idle state, the output buffer is cleared, and the transmitter sends the value defined by bit 4 in the control register (DOB).

The IORST instruction has the same effect as the stop command, but all receivers are cleared, and the control register is cleared.

3.5.4 Transmitted Data

3.5.4

When the program wants to start a transmitter, it is advisable to store some characters in the output buffer first, but it is no condition as the transmitter waits for the buffer to start the transmission. After a stop command the buffer is empty, and all 64 places can be filled.

The store character function is performed by a DOA instruction.

```
DOA   AC, SMX
  AC
```

X	X	X	X	X	X	X	X	Character to be transmitted							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Example of program part:

```
DOC Ø, SMX    ; Select Appropriate Transmitter
SKPBZ SMX     ; Is there room in the buffer?
JMP - - -     ; NO, Return
LDA 1, BUF    ; YES, Load the Character
DOA 1, SMX    ; and Store It
SKPBZ SMX     ; One more place?
JMP - - -     ; NO, Return
LDA 1, BUF+1  ; YES, Load It and
DOA 1, SMX    ; Store It
              etc.
```

If the BUSY flag remains high, no more places are free in the buffer at this moment.

If the output buffer becomes completely empty, a DATA LATE flag will be set when the transmitter starts to send the next character. DATA LATE is a status information that can be sensed by a DIB instruction (refer to 3.6).

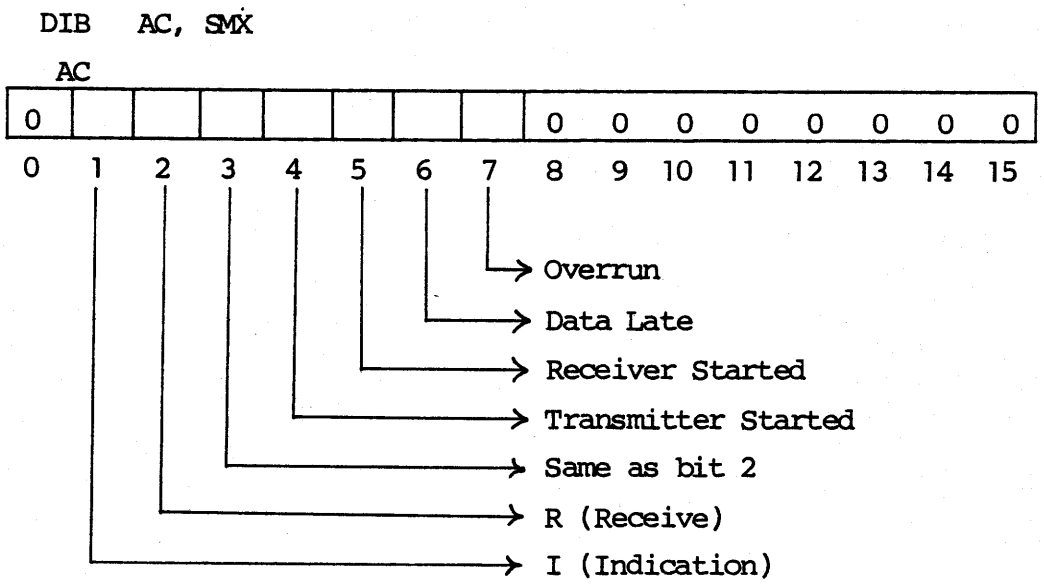
The transmitter will continue sending the last word until stopped, or until new data is filled in the buffer.

Note: The transmitted SYN-characters in the beginning of a block must be loaded into the transmit buffer by the program.

3.6 Status Word

3.6

The status of a selected channel can be loaded into an accumulator by a DIB instruction.



3.6.1 I (Indication) 3.6.1

If the modem control signal I (indication) changes from ON to OFF, this statusbit will be logical 1 as long as the OFF state remains.

3.6.2 R (Receive) 3.6.2

If the modem signal R (Receive) changes from 0 to 1, this statusbit will be logical 1 as long as the 1 state remains.

The signal has same level as the immediate bit level of the data receiver.

3.6.3 Transmitter Started, Bit 4 3.6.3

As soon as the specified transmitter has got a start command, this statusbit will be logical 1. When the transmitter is stopped, the statusbit will be logical 0.

3.6.4 Receiver Started, Bit 5 3.6.4

As soon as the specified receiver has got a start command, this statusbit will be logical 1. When the receiver is stopped, the statusbit will be logical 0.

3.6.5 Data Late, Bit 6 3.6.5

If the transmitter has been started and at least one character has been transmitted, this statusbit will be logical 1 if no characters are present in the output buffer. The statusbit can be cleared only by applying a stop command to the transmitter.

3.6.7 Overrun, Bit 7

If the receiver has been started and more than 64 characters are received after synchronization has been obtained and the program has not had time to take characters from the input buffer, this statusbit will be logical 1. The statusbit can be cleared only by applying a stop command to the transmitter.

RETURN LETTER

SMX702

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