Title:

FPA 705
Front End Processor Adapter
General Information

A/S REGNECENTRALEN

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Abstract:

This manual contains general information on the Front Processor Adapter, FPA 705.

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MAIN CHARACTERISTICS 1

Short Description. 1.1

The FPA 705 is an asynchronous controller intended for use as interconnecting media between the RC 3600 computer and RC 3600, RC 3500, or RC 8000 computers.

FPA705 contains two subdevices, called the TRANSMITTER and the RECEIVER. Refer to fig. 1.1. Basicly it is two separate controllers each with its own control logic, so transmission can take place in both directions simultaneously.

The two devices are controlled by the normal I/O instructions, but data-transport takes place through the data channel.

The transmission is more than 600K bytes/sec.

Communication with RC 3600. 1.2

Communication with the RC 3600 CPU takes place via the standard I/O bus. Operations are initiated in both the TRANSMITTER and the RECEIVER by using the normal I/O instructions.

Normally, the TRANSMITTER part of FPA 705 is used to transmit a data block to the remote controller, and to receive a single status byte as a response to the transmitted block.

The RECEIVER part of FPA 705 is used to receive a data block from the remote controller, and to transmit a single status byte as a response to the received data block.

Both the TRANSMITTER and the RECEIVER are connected to the Data Channel, so data transfer takes place directly between the FPA 705 and the core memory in RC 3600.

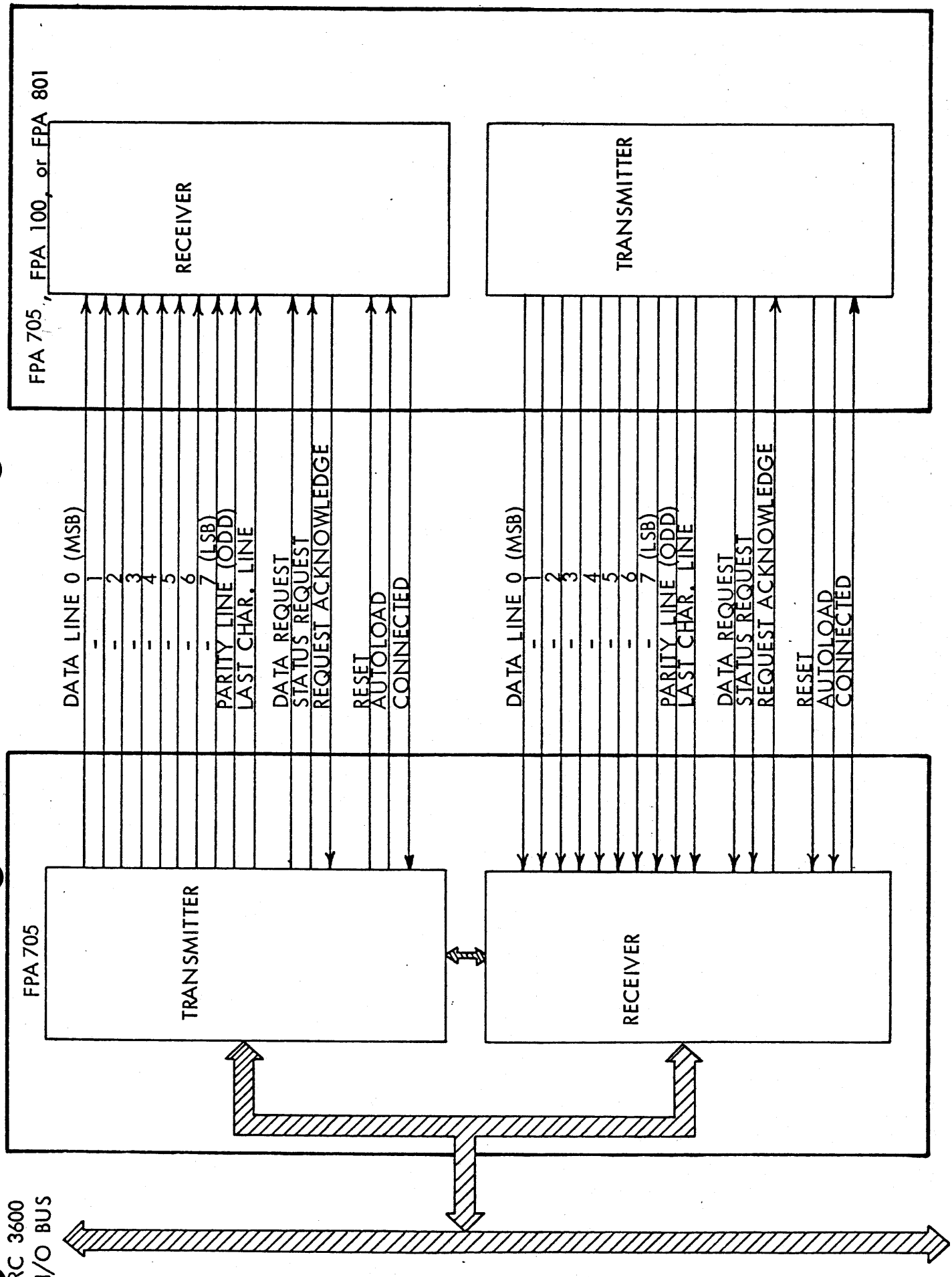

Fig. 1.1. FPA 705 Outline

The communication with the Remote Controller takes place via a set of output and a set of input lines. The output lines and input lines are completely symmetrical, each set consisting of:

9 Data lines, incl. a parity line, and
7 Control lines.

For further specification of the lines refer to section 4.

Included in the control lines is an autoload request line, which is necessary to be able to initiate an autoload procedure.

The communication is asynchronous on a byte by byte manner. Each byte consists of 9 bits: 8 databits + 1 parity bit (ODD parity).

The timing of the byte transfers are under control of two types of request signals and one request acknowledge signal.

The request signals are named:

DATA REQUEST and STATUS REQUEST.

The Data Request is used as a request signal when the Transmitter sends data to the remote controller, and the Status Request is used when the Receiver transmits status to the remote end.

The communication with the remote controller utilizes the asynchronous, fully interlocked technique. Each request signal from FPA 705 must be acknowledged to complete the transfer.

When FPA 705 wants to transmit a byte, the byte is placed on the data lines, and the data request signal is set. When the remote controller has stored the byte, it responds to the request by setting the request acknowledge signal, indicating the reception of the byte. Upon the reception of the acknowledge signal, FPA 705 lowers the request signal, which also causes the remote end to lower the acknowledge signal.

At FPA 705

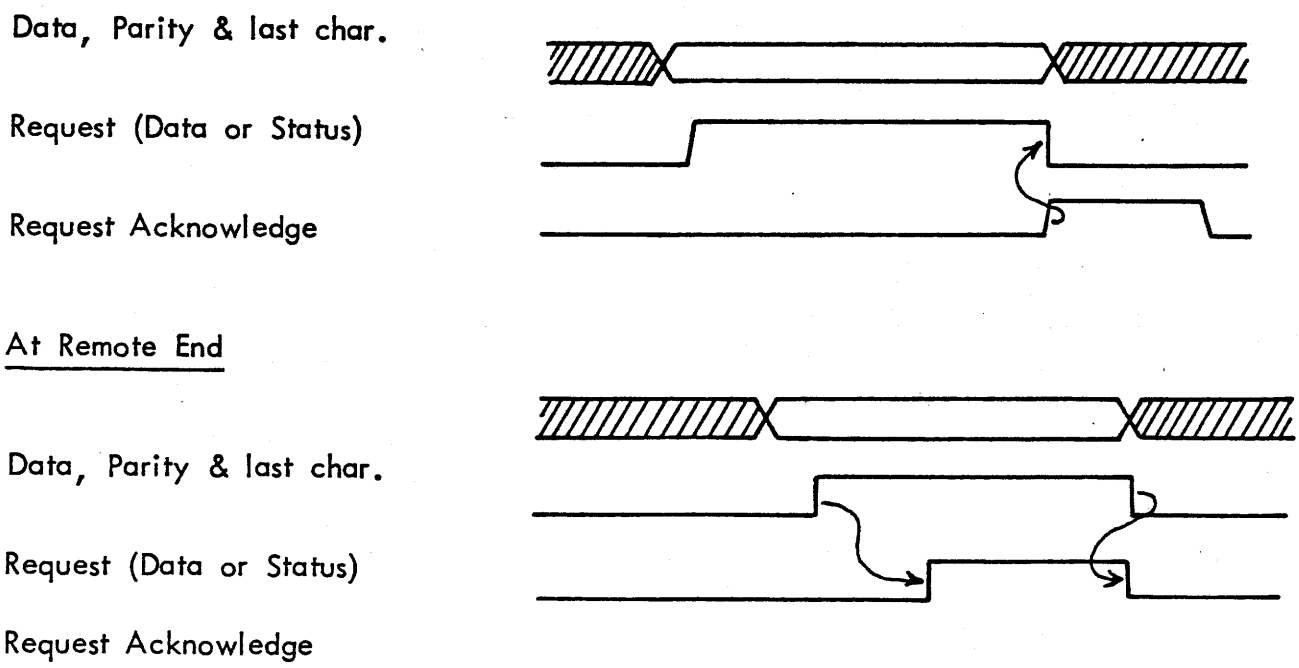

Fig. 1.2. Timing

Simultaneously with transmission of the last byte in a block, the LAST CHAR signal is sent.

Also provided in the control lines is a RESET signal, which notifies the receiver when the transmitter is reset.

The transmission can take place in both directions simultaneously. But if the receiver wants to transmit a STATUS Byte while the transmitter is in progress with transmitting a data block, the STATUS byte is not transmitted, before the transmitter has finished the previous data block, i.e. STATUS bytes are transmitted between data blocks.

Timing (Refer to Fig. 2.1). 2.1

As mentioned in section 1 "Main Characteristics", the communication with the front-end utilizes the handshake technique.

Note that the transmitting unit is allowed to rise the request signal, even if the request acknowledge signal is not lowered, which means that it is the rise of the leading edge of the request acknowledge that indicates the reception of the character.

This is done to speed up the transmission, since the transmitting unit does not need to wait for the propagation of the high to low transition of the acknowledge signal.

Upon the reception of the low to high transition of the request acknowledge signal the transmitting unit must lower the request signal. The request signal must be low for at least 100 ns.

The pulse width of request acknowledge must not be less than 30 ns.; however, the signal must not be lowered until the request signal has been lowered. The pulse width of request acknowledge depends on cable delay, driver/receiver propagation delays, and propagation delays in circuits, which utilizes the acknowledge signal. When using FPA 705 interface circuits and principle, the width of request acknowledge, measured at the output of the line driver, will not be less than 30 ns.

When measured at the outputs of line drivers, data must lead request with at least 20 ns., the same specification is valid for the last character signal. Data must not change as long as the request signal is true.

To compensate for max. cable and receiver skew, the receiving unit must delay the request signal at least 100 ns. before the character is stored.

The pulse width of RESET and AUTOLOAD signals shall be at least 300 ns.

Line Drivers and Receivers.

The following line drivers and receivers are recommended:

Drivers:

TEXAS	:	SN 75183
NATIONAL	:	DM 8830
FAIRCHILD	:	9612E

Receivers:

TEXAS	:	SN 75182
NATIONAL	:	DM 8820A
FAIRCHILD	:	9613

The line drivers provide differential output signals, and are used to drive a twisted pair line with an impedance of app. 120Ω . The drivers are single supplied and use only + 5V.

SN 75183 and DM 8830 are compatible and include gates, which are useful when it is necessary to gate the signals; therefore this type of driver is used for the control signals.

9612E is used for the data, parity, and last character signals since these signals need no gating.

The line receivers are designed to sense small differential signals in the presence of large common-mode noise; up to $\pm$ 15V. common mode input voltage can be tolerated. The receivers are single supplied and use only + 5V.

SN 75182 and DM 8820A are compatible and include strobe and terminating resistor (170Ω). The strobe input is used to strobe all of the control signal receivers with the disconnected signal from the opposite end. This assures that the output of the control signal receivers is always logical 0, if the opposite computer is disconnected (power off or no cable installed etc.).

9613 is used as receiver for the data parity and last character signals, since these signals need no gating. No terminating resistor is included in the 9613.

Cable Characteristics. 2.3

The cable to be used should have the following characteristics:

Type: Shielded cable,
min. 16 pairs of twisted wires 0.25 mm^2.

Impedance: App. 120Ω .

Max. length: 20 m.

The shield of the cable must be connected to the common zero voltage. Refer to fig. 4.2. The cable should only be terminated in the receiving unit.

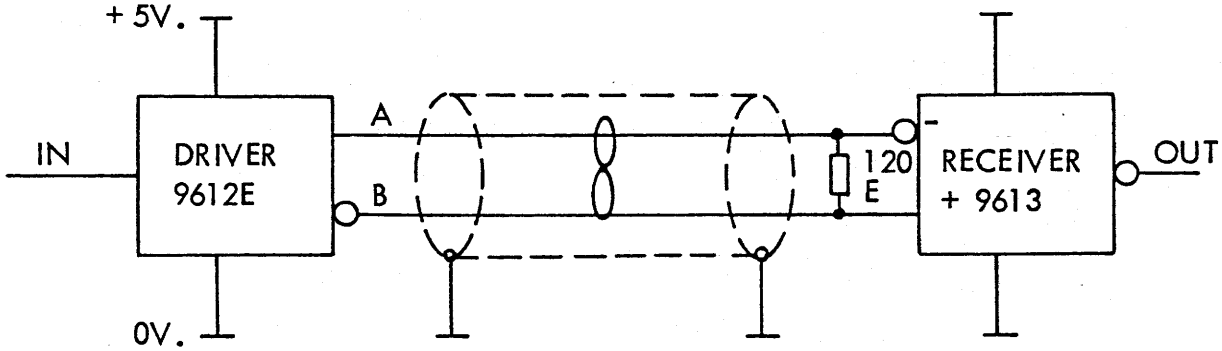

Fig. 2.2.

When a logical 1 exists on the line, A shall be positive in relation to B.

Signal Description. 2.4

DATA LINES 0 : 7 : Data line 0 is the most significant bit, and data line 7 the least significant bit.

PARITY LINE : This line is the parity line making the parity odd.

LAST CHAR LINE : When logical 1, this line indicates the end of the block. The LAST CHAR signal is generated simultaneously with the emission of the last character in the block and the STATUS BYTE.

DATA REQUEST LINE : This signal when logical 1 indicates to the receiving unit that a data character is ready on the data lines 0 : 7. The signal is generated by the transmitter in the transmitting unit.

STATUS REQUEST LINE : This signal when logical 1 indicates to the receiving unit that a status character is ready on the data lines 0 : 7. The signal is generated by the receiver in the transmitting unit.

REQUEST ACKNOWLEDGE LINE : When this signal changes from false to true state, it indicates to the transmitting unit that the character on the data lines has been stored in the receiving unit. Upon the reception of the rising edge of the acknowledge signal the transmitting unit is allowed to fetch the next character and place it on the data lines.

RESET LINE : This line when logical 1 indicates to the receiver in the receiving unit that the transmitter in the transmitting unit has been reset.

CONNECTED LINE : This line when logical 1 indicates to the receiving unit that power is on. The connected signal is used to strobe the following control signals:

RESET
REQUEST ACK
DATA REQUEST
STATUS REQUEST
AUTO LOAD

This assures that the output of these receivers is at logical 0 when power in the transmitting unit is turned off.

AUTOLOAD LINE : This line is necessary to be able to initiate an autoload procedure in the front end computer under RC 8000 program control.

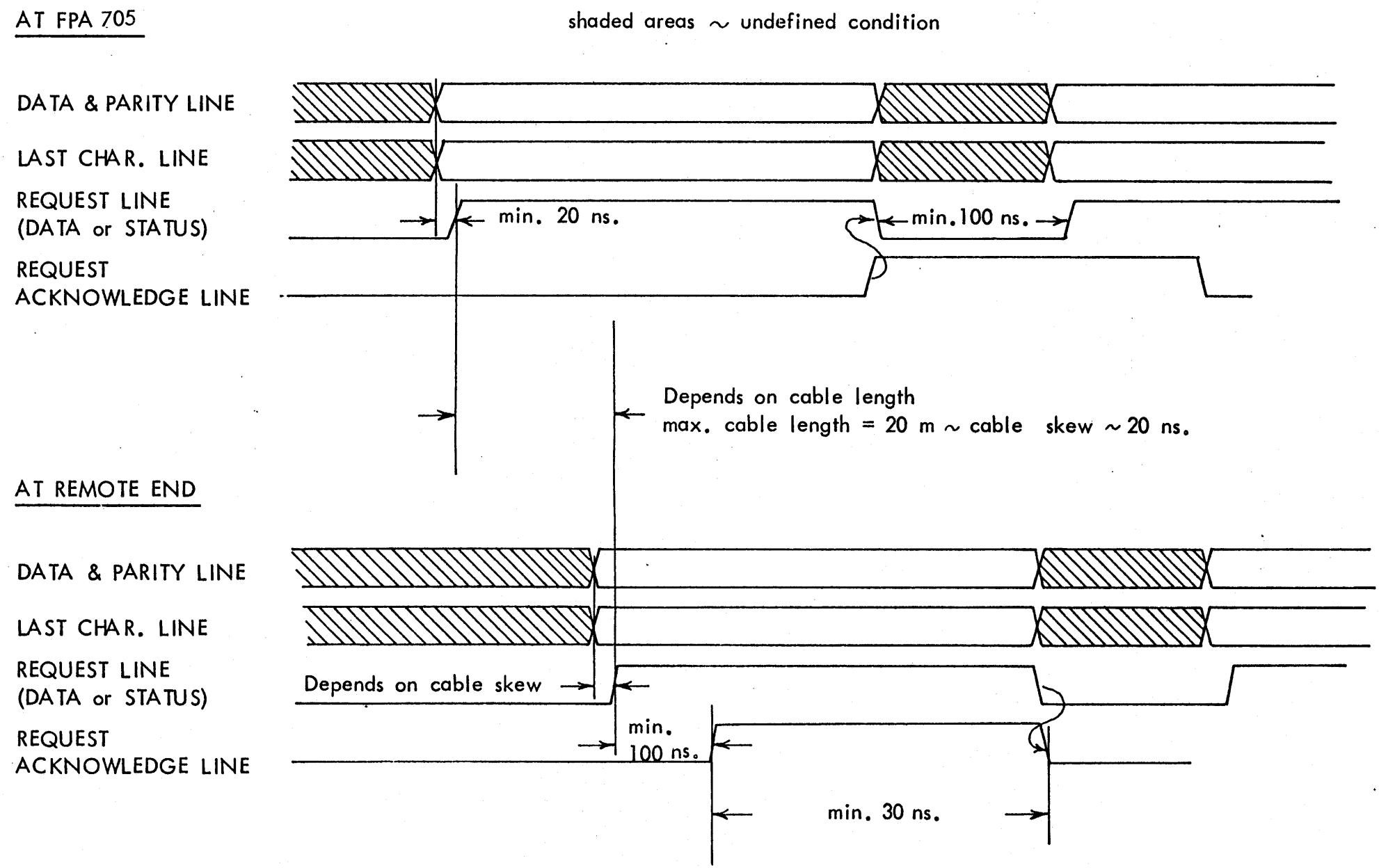

Fig. 2.1. Line Characteristics - Timing.

Refer to fig. 3.1-3.3.