INDHOLDSFORTEGNELSE	
1	[illegible] Memory Controller ME-131
2	[illegible] Memory System [illegible] / ME-111
3	[illegible] Logic diagram, [illegible] Register III STC, [illegible]
4	[illegible]
5	[illegible], modifikationer til [illegible] PROCESSOR incl. PCBA partlist for
6	[illegible] for [illegible] [illegible]
7	A. [illegible] Write Cycle Status [illegible] B. [illegible]

ECOM® F MEMORY CONTROLLER

MC-131

Standard Memories, Inc.
15130 West Ventura Boulevard
Sherman Oaks, California 91430

Phone: (213) 788-3010

standard memories

WARRANTY

All products manufactured by STANDARD MEMORIES, INC. are warranted to be free from defects in material and workmanship one year from date of delivery to the original purchaser.

STANDARD MEMORIES, INC's obligation under this warranty is limited to servicing or adjustment of any equipment returned to the factory for that purpose, and replacing any defective parts thereof. If the failure has been caused by misuse, operation in excess of specification guarantees, or modification by the customer, repairs will be billed at cost. In such cases, a cost estimate will be submitted before work is started.

This warranty is expressly in lieu of all other obligations or liabilities on the part of STANDARD MEMORIES, INC., and STANDARD MEMORIES, INC. neither assumes nor authorizes any other person to assume for them, any liability in connection with the sale of STANDARD MEMORIES, INC. products.

PROPRIETARY RIGHTS of STANDARD MEMORIES, INCORPORATED are involved in this subject matter and all manufacturing, reproduction, use and sales rights pertaining to such subject matter are expressly reserved. It is submitted in confidence for a specified purpose, and the recipient by accepting this material agrees that this material will not be used, copied or reproduced in whole or in part nor its contents revealed in any manner or to any person except to meet the purpose for which it was delivered.

TABLE OF CONTENTS

SECTION I

ECOM® F MEMORY CONTROLLER

MC-131

1.1 DESCRIPTION

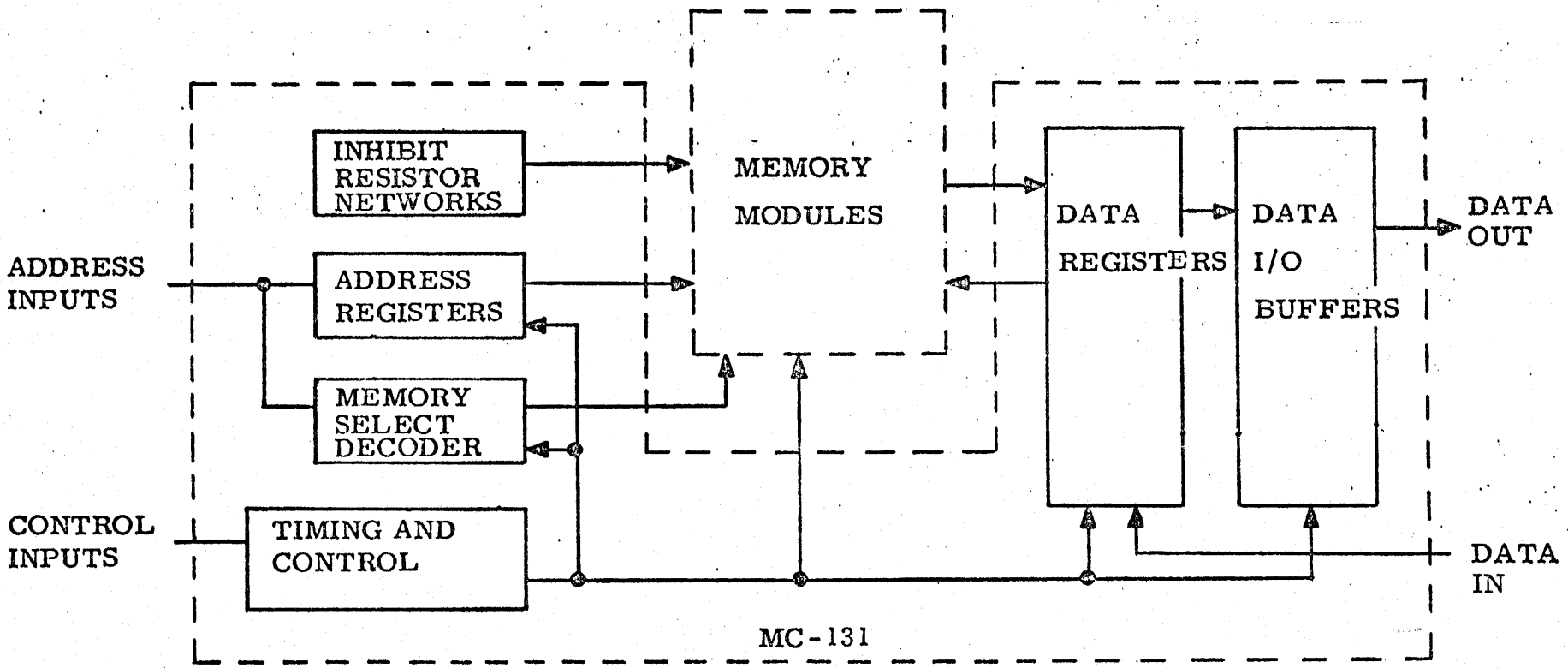
The Memory controller (MC-131) provides timing, control functions, address and data registe rs and the inhibit resistor networks for an 18 bit ECOM® F system of up to 131, 072 words. Expanded systems are possible by the parallel operation of memory controllers.

The MC-131 provides four operating modes: Full Cycle Read-Restore and Clear-Write, Split Cycle Read-Pause-Write and Clear-Pause-Write. Each word has been separated into two groups of nine bits which may be operated upon independently (Byte Control). Thus, the MC-131 can make a 131K X 18 bit ECOM® F system appear to contain 262, 144 nine bit words.

The input-output interface of the MC-131 is DTL/TTL compatible. All I/O terms originating on the memory controller, with the exception of a $\overline{\text{Memory Busy}}$ signal ($\overline{\text{Memory Busy}}$ is generated by an emitter follower to provide a low impedance or logic 0 signal during a power off condition) are generated by open collector TTL gates to provide compatibility with bussed systems. Either one way or bidirectional

bussing schemes may be used. Provision has been made for field installation of pull-up resistors, should it be desirable.

A power failure data protection circuit is provided on the memory controller. Upon a signal indicating that power is failing, the MC-131 will automatically conclude the cycle in progress, provide a "turn-off" signal to the memory module and then inhibit all commands to the memory module.



MC-131 FUNCTIONAL BLOCK DIAGRAM

1.2 SPECIFICATIONS

1.2.1 Operating Modes

Full Cycle	Read-Restore Clear-Write
Split Cycle	Read-Pause-Write Clear-Pause-Write

With Byte Control the ECOM® F system can perform any combination of two of the above functions. For example, it is possible to Read-Restore Byte$_1$ and Clear-Write Byte$_2$ or to Read-Pause-Write Byte$_1$ and Read-Restore Byte$_2$. In the latter case, both a full cycle and a split cycle function are requested. The system will perform both functions with the timing of the split cycle function.

Memory Mode	$R/\overline{C_1}$	$R/\overline{C_2}$	$R/\overline{M_1}$	$R/\overline{M_2}$
Full Cycle				
Read/Restore (R/R)	T	T	T	T
Clear/Write (C/W)	F	F	T	T
R/R Byte$_1$, C/W Byte$_2$	T	F	T	T
C/W Byte$_1$, R/R Byte$_2$	F	T	T	T
Split Cycle				
Read-Pause-Write (RPW)	T	T	F	F
Clear-Pause-Write (CPW)	F	F	F	F
RPW Byte$_1$, CPW Byte$_2$	T	F	F	F
CPW Byte$_1$, RPW Byte$_2$	F	T	F	F

1.2.2 Input/Output Interface.

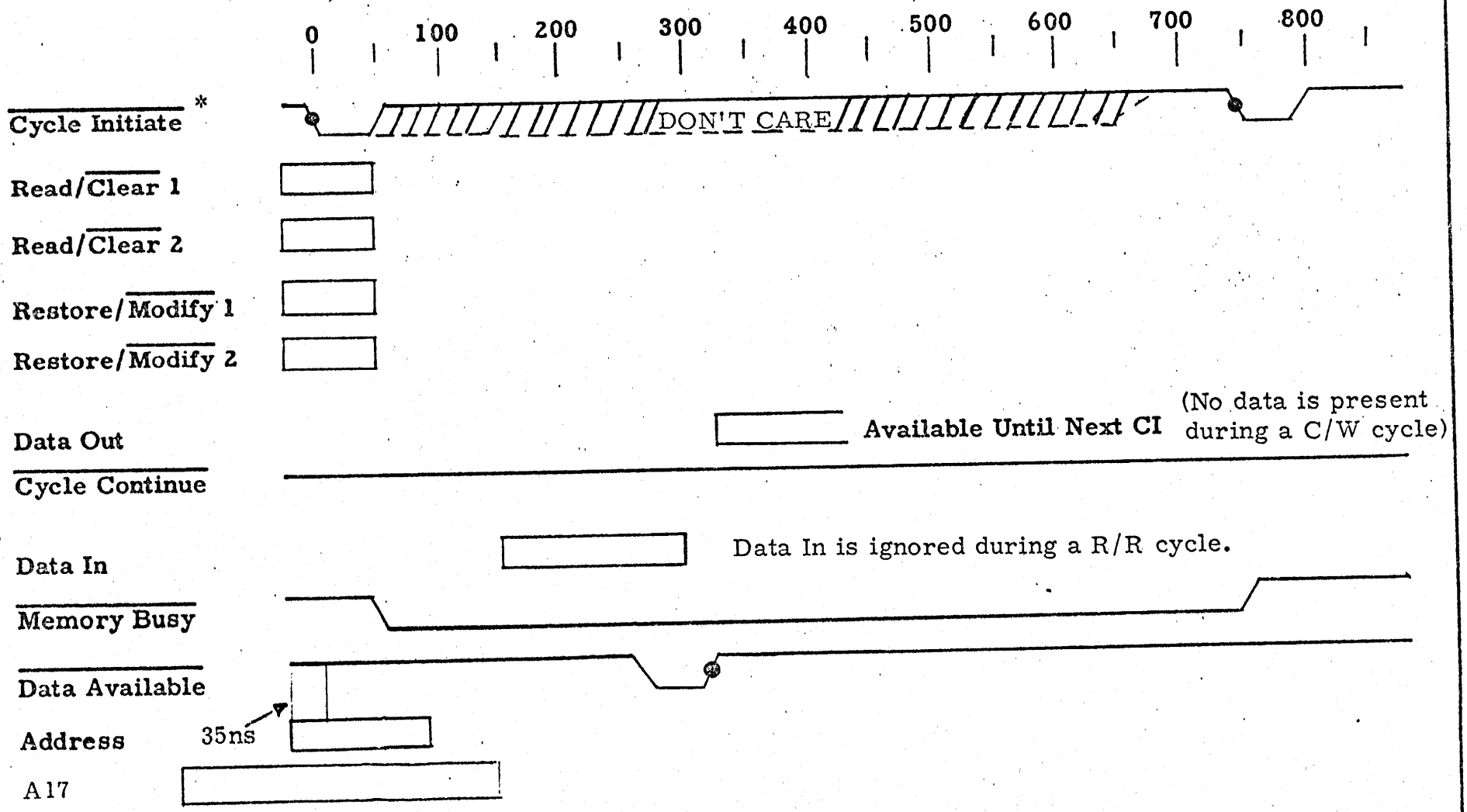
	Function	Lines	Loads	Signal
Input:				
	Address	18	2	Level
	Data In	18	2	Level
	$\overline{\text{Cycle Initiate}}$	1	2	Pulse
	Read/$\overline{\text{Clear}}$ 1	1	2	Level
	Read/$\overline{\text{Clear}}$ 2	1	2	Level
	Restore/$\overline{\text{Modify}}$ 1	1	2	Level
	Restore/$\overline{\text{Modify}}$ 2	1	2	Level
	Cycle Continue	1	2	Pulse
	Data Save P/S	1	2	Level
	Data Enable	2	1	Level
	Direct Data Save	1	5	Level

Note: When the power supply goes out of specification, the Data Save P/S line must be held true.

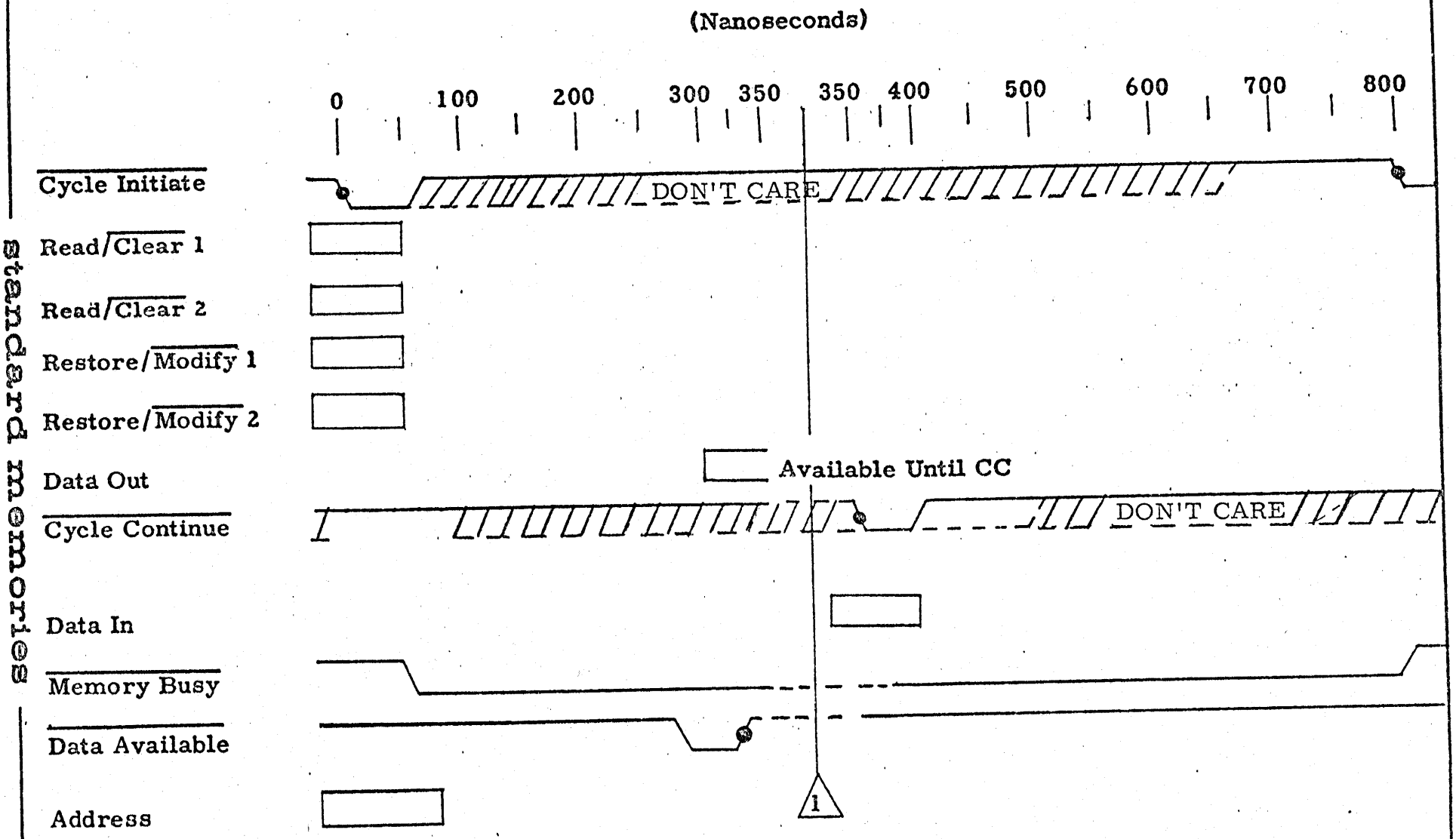
	Function	Lines	Loads	Signal
Output:				
	Data Out	18	10	Level
	Data Available	1	10	Pulse
	$\overline{\text{Memory Busy}}$	1	10	Level
	Data Save Sync	1	10	Level
	Data Save Active	1	10	Level

1.2.3 Input/Output Timing

Full Cycle (R/R or C/W) Timing



Split Cycle (Read-Pause-Write)



Note: 1 Insert Split Cycle Pause Here

= Required Stable Interval

* See full cycle diagram for $\overline{CI}$ specifications If CC is false at dot the split cycle will start there.

1.2.4 Memory Interface.

	Function	Lines	Signal
Input:			
	Data Ready	1	Pulse
	Memory Data	18	Pulse
Output:			
	Address	12	Level
	Selects	8	Level
	Control Data	18	Level
	Read	1	Pulse
	Write	1	Pulse
	Data Save	1	Level

All input and output lines are capable of operating with up to 16 memory modules.

1.2.5 Power Requirements.

Logic: +5V ± 5% 1.5 amperes

Inhibit Network: +15V ± 2%

Note: Current required by the inhibit network is a function of the data pattern and the cycle time. Calculations of average and peak current requirements are presented in the memory module specifications.

1.2.6 Environment.

Temperature: Operating 0°C to 50°C in free air when mounted vertically.

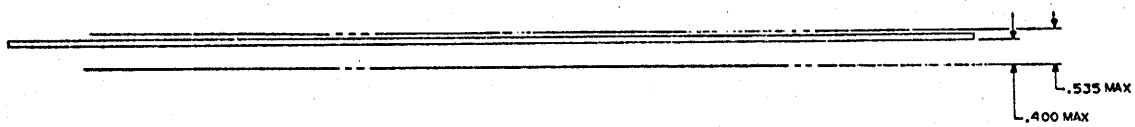
Operating 0°C to 50°C with 20 CFM air flow uniformally distributed over the inhibit resistors when mounted horizontally.

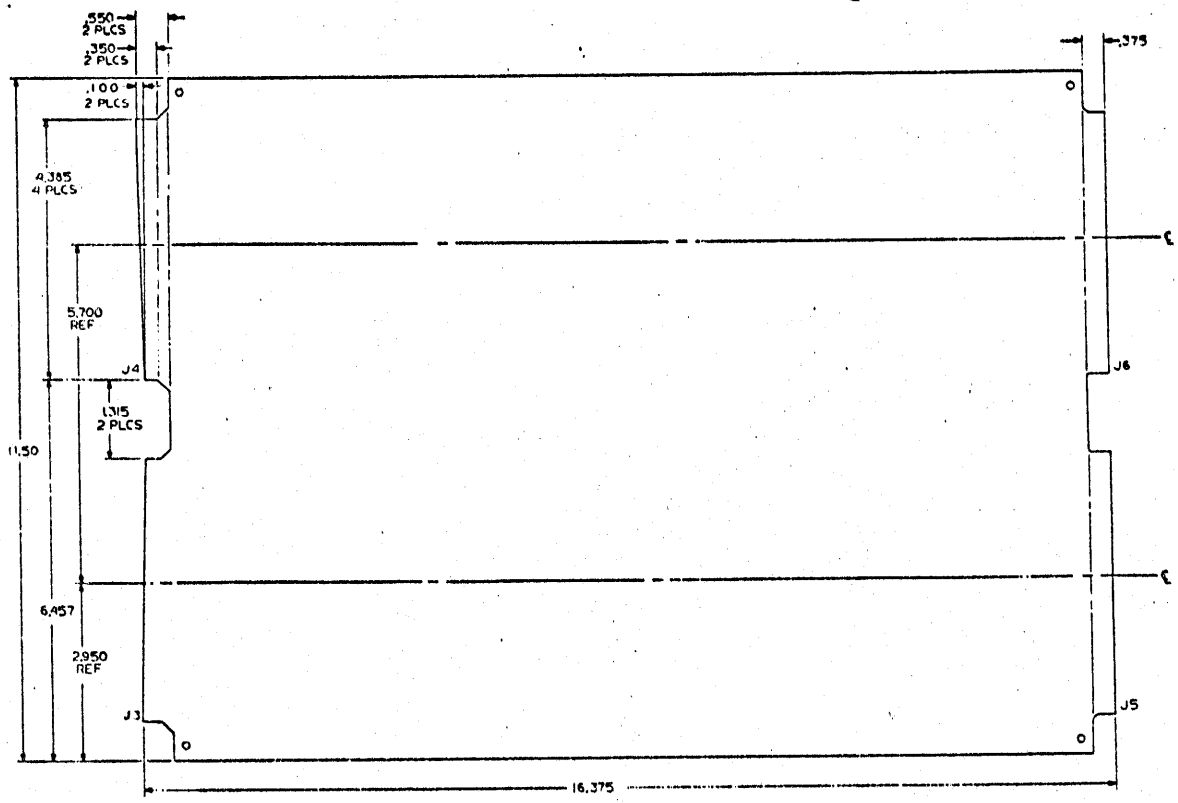
Storage, -40°C to +100°C

Humidity: To 95% relative, without condensation

1.2.7 Mechanical.

Board Size:	16.375" X 11.5" (Outline Diagram Page 1-11)
Mounting Centers:	0.75"
Connectors	86 pin card edge type with 0.025" sq. wire-wrap post on 0.100 centers.
I/O Connectors	86 pin card edge type with solder tabs on 0.100 centers.





COMPONENT SIDE

DRAWN		STANDARD MEMORIES, INC. SANTA ANA, CALIF.
CHECKED R. Swan	1-24-78	
APPROVED (illegible)	2-17-78	OUTLINE MC-131
		SIZE D · CODE ID 29737 · NUMBER SK-012172 · REV -
		SCALE 1/1 · SHEET 1 OF 1

CONNECTOR PIN ASSIGNMENTS

J3 Connector Type: Sylvania 7900-0261-4

Pin	Function	Pin	Function
1	Thru 1	2	Address Bit 11
3	Thru 2	4	Address Bit 10
5	Address Bit 9 Return	6	Address Bit 9
7	Address Bit 8 Return	8	Address Bit 8
9	Address Bit 7 Return	10	Address Bit 7
11	Address Bit 6 Return	12	Address Bit 6
13	Address Bit 5 Return	14	Address Bit 5
15	Address Bit 4 Return	16	Address Bit 4
17	Address Bit 3 Return	18	Address Bit 3
19	Address Bit 2 Return	20	Address Bit 2
21	Address Bit 1 Return	22	Address Bit 1
23	Address Bit 0 Return	24	Address Bit 0
25	Select B 4 Return	26	Select B 4
27	Select B 3 Return	28	Select B 3
29	Select B 2 Return	30	Select B 2
31	Select B 1 Return	32	Select B 1
33	Select A 4 Return	34	Select A 4
35	Select A 3 Return	36	Select A 3
37	Select A 2 Return	38	Select A 2
39	Select A 1 Return	40	Select A 1
41	Write Return	42	Write
43	Read Return	44	Read

DRAWN R. SLANE	2-4-72
CHECKED A. E	2-4-72
APPROVED [illegible]	2-29-72

SPECIFICATION CONTROL

MC-131 CONNECTOR PIN ASSIGNMENTS

STANDARD MEMORIES

SIZE	CODE IDENT	NUMBER	REV
A	29737	SC1622	A

Connector Pin Assignments - Continued

Pin	Function	Pin	Function
45	Data Ready Return	46	Data Ready
47	A17	48	$\overline{\text{CD}}$ Bit 1
49	Spare	50	$\overline{\text{MD}}$ Bit 1
51	$\overline{\text{CD}}$ Bit 2 Return	52	$\overline{\text{CD}}$ Bit 2
53	$\overline{\text{MD}}$ Bit 2 Return	54	$\overline{\text{MD}}$ Bit 2
55	$\overline{\text{CD}}$ Bit 3 Return	56	$\overline{\text{CD}}$ Bit 3
57	$\overline{\text{MD}}$ Bit 3 Return	58	$\overline{\text{MD}}$ Bit 3
59	$\overline{\text{CD}}$ Bit 4 Return	60	$\overline{\text{CD}}$ Bit 4
61	$\overline{\text{MD}}$ Bit 4 Return	62	$\overline{\text{MD}}$ Bit 4
63	$\overline{\text{CD}}$ Bit 5 Return	64	$\overline{\text{CD}}$ Bit 5
65	$\overline{\text{MD}}$ Bit 5 Return	66	$\overline{\text{MD}}$ Bit 5
67	$\overline{\text{CD}}$ Bit 6 Return	68	$\overline{\text{CD}}$ Bit 6
69	$\overline{\text{MD}}$ Bit 6 Return	70	$\overline{\text{MD}}$ Bit 6
71	$\overline{\text{CD}}$ Bit 7 Return	72	$\overline{\text{CD}}$ Bit 7
73	$\overline{\text{MD}}$ Bit 7 Return	74	$\overline{\text{MD}}$ Bit 7
75	$\overline{\text{CD}}$ Bit 8 Return	76	$\overline{\text{CD}}$ Bit 8
77	$\overline{\text{MD}}$ Bit 8 Return	78	$\overline{\text{MD}}$ Bit 8
79	$\overline{\text{CD}}$ Bit 9 Return	80	$\overline{\text{CD}}$ Bit 9
81	$\overline{\text{MD}}$ Bit 9 Return	82	$\overline{\text{MD}}$ Bit 9
83	$\overline{\text{CD}}$ Bit 10 Return	84	$\overline{\text{CD}}$ Bit 10
85	$\overline{\text{MD}}$ Bit 10 Return	86	$\overline{\text{MD}}$ Bit 10

CONNECTOR PIN ASSIGNMENTS

J4 Connector Type: Sylvania 7900-0261-4

Pin	Function	Pin	Function
1	$\overline{\text{CD}}$ Bit 11 Return	2	$\overline{\text{CD}}$ Bit 11
3	$\overline{\text{MD}}$ Bit 11 Return	4	$\overline{\text{MD}}$ Bit 11
5	$\overline{\text{CD}}$ Bit 12 Return	6	$\overline{\text{CD}}$ Bit 12
7	$\overline{\text{MD}}$ Bit 12 Return	8	$\overline{\text{MD}}$ Bit 12
9	$\overline{\text{CD}}$ Bit 13 Return	10	$\overline{\text{CD}}$ Bit 13
11	$\overline{\text{MD}}$ Bit 13 Return	12	$\overline{\text{MD}}$ Bit 13
13	$\overline{\text{CD}}$ Bit 14 Return	14	$\overline{\text{CD}}$ Bit 13
15	$\overline{\text{MD}}$ Bit 14 Return	16	$\overline{\text{MD}}$ Bit 14
17	$\overline{\text{CD}}$ Bit 15 Return	18	$\overline{\text{CD}}$ Bit 15
19	$\overline{\text{MD}}$ Bit 15 Return	20	$\overline{\text{MD}}$ Bit 15
21	$\overline{\text{CD}}$ Bit 16 Return	22	$\overline{\text{CD}}$ Bit 16
23	$\overline{\text{MD}}$ Bit 16 Return	24	$\overline{\text{MD}}$ Bit 16
25	$\overline{\text{CD}}$ Bit 17 Return	26	$\overline{\text{CD}}$ Bit 17
27	$\overline{\text{MD}}$ Bit 17 Return	28	$\overline{\text{MD}}$ Bit 17
29	$\overline{\text{CD}}$ Bit 18 Return	30	$\overline{\text{CD}}$ Bit 18
31	$\overline{\text{MD}}$ Bit 18 Return	32	$\overline{\text{MD}}$ Bit 18
33	$\overline{\text{Data Save}}$ Return	34	$\overline{\text{Data Save}}$
35	$\overline{\text{Data Save}}$ P/S Return	36	$\overline{\text{Data Save}}$ P/S
37	Address Bit 12 Return	38	Address Bit 12
39	Inhibit Bit 1 Return	40	Inhibit Bit 1
41	Inhibit Bit 2 Return	42	Inhibit Bit 2
43	Inhibit Bit 3 Return	44	Inhibit Bit 3
45	Inhibit Bit 4 Return	46	Inhibit Bit 4
47	Inhibit Bit 5 Return	48	Inhibit Bit 5
49	Inhibit Bit 6 Return	50	Inhibit Bit 6
51	Inhibit Bit 7 Return	52	Inhibit Bit 7
53	Inhibit Bit 8 Return	54	Inhibit Bit 8

Connector Pin Assignments - Continued

Pin	Function	Pin	Function
55	Inhibit Bit 9 Return	56	Inhibit Bit 9
57	Inhibit Bit 10 Return	58	Inhibit Bit 10
59	Inhibit Bit 11 Return	60	Inhibit Bit 11
61	Inhibit Bit 12 Return	62	Inhibit Bit 12
63	Inhibit Bit 13 Return	64	Inhibit Bit 13
65	Inhibit Bit 14 Return	66	Inhibit Bit 14
67	Inhibit Bit 15 Return	68	Inhibit Bit 15
69	Inhibit Bit 16 Return	70	Inhibit Bit 16
71	Inhibit Bit 17 Return	72	Inhibit Bit 17
73	Inhibit Bit 18 Return	74	Inhibit Bit 18
75	Select-C Return	76	Select C
77	+15V	78	+15V
79	P/S GND	80	P/S GND
81	+5V	82	+5V
83	Not Used	84	Not Used
85	Not Used	86	Not Used

CONNECTOR PIN ASSIGNMENTS

J5 Connector Type: Viking 2VH43/1JN5

Pin	Function	Pin	Function
B 1		A 1	
B 2	Address Bit 16+	A 2	Address Bit 16 Return
B 3	Address Bit 15+	A 3	Address Bit 15 Return
B 4	Address Bit 14+	A 4	Address Bit 14 Return
B 5	Address Bit 13+	A 5	Address Bit 13 Return
B 6	Address Bit 11+	A 6	Address Bit 11 Return
B 7	Address Bit 10+	A 7	Address Bit 10 Return
B 8	Address Bit 9+	A 8	Address Bit 9 Return
B 9	Address Bit 8+	A 9	Address Bit 8 Return
B10	Address Bit 7+	A10	Address Bit 7 Return
B11	Address Bit 6+	A11	Address Bit 6 Return
B12	Address Bit 5+	A12	Address Bit 5 Return
B13	Address Bit 4+	A13	Address Bit 4 Return
B14	Address Bit 3+	A14	Address Bit 3 Return
B15	Address Bit 2+	A15	Address Bit 2 Return
B16	Address Bit 1+	A16	Address Bit 1 Return
B17	Address Bit 0+	A17	Address Bit 0 Return
B18	$\overline{\text{Memory Busy}}$	A18	$\overline{\text{Memory Busy}}$ Return
B19	Data Available+	A19	Data Available Return
B20	$\overline{\text{CC}}$+	A20	$\overline{\text{CC}}$ Return
B21	$\overline{\text{CI}}$+	A21	$\overline{\text{CI}}$ Return
B22	Data Enable 2+	A22	Data Enable Return 2
B23	Data Enable 1+	A23	Data Enable Return 1
B24	Address Bit 12+	A24	Address Bit 12 Return
B25	Memory Select+	A25	Memory Select Return
B26	Address C+	A26	Address C Return

Connector Pin Assignments - Continued

Pin	Function	Pin	Function
B27	Thru 1	A27	Thru 1 Return
B28	Thru 2	A28	Thru 2 Return
B29		A29	
B30	$\overline{\text{CR}}$ (Cycle Restore)+	A30	$\overline{\text{CR}}$ Return
B31	Add. Enable+	A31	Add. Enable Return
B32		A32	
B33		A33	
B34		A34	
B35		A35	
B36		A36	
B37	Kickout 1 (Ver. -003 only)	A37	
B38	Kickout 2 (Ver. -003 only)	A38	
B39	Data Save Sync. (DSS)	A39	DSS Return
B40	$\overline{\text{Data Save Active}}$	A40	$\overline{\text{DSA}}$ Return
B41	Direct Data Save+	A41	DDS Return
B42		A42	
B43	+5V	A43	+5V

CONNECTOR PIN ASSIGNMENTS

J6 Connector Type: Viking 2VH43/1JN5

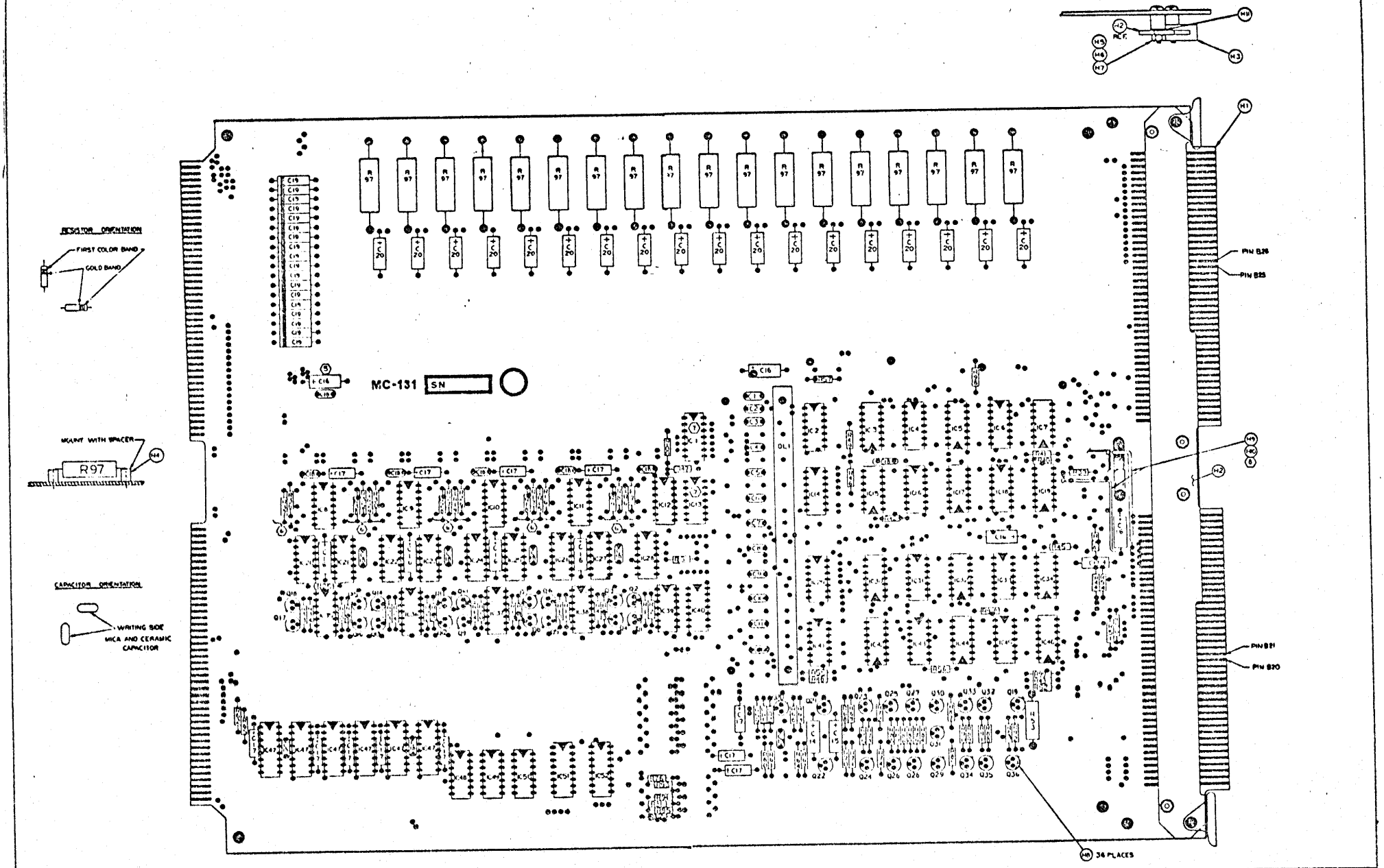
Pin	Function	Pin	Function
B 1	Data Save P/S *	A 1	Data Save P/S* Return
B 2	Data Save P/S	A 2	Data Save P/S Return
B 3		A 3	
B 4	Read/$\overline{\text{Clear}}_2$ +	A 4	Read/$\overline{\text{Clear}}_2$ Return
B 5	Read/$\overline{\text{Clear}}_1$ +	A 5	Read/$\overline{\text{Clear}}_1$ Return
B 6	Restore/$\overline{\text{Modify}}_1$ +	A 6	Restore/$\overline{\text{Modify}}_1$ Return
B 7	Restore/$\overline{\text{Modify}}_2$ +	A 7	Restore/$\overline{\text{Modify}}_2$ Retum
B 8	DI Bit 1 +	A 8	DI Bit 1 Return
B 9	DI Bit 2 +	A 9	DI Bit 2 Return
B10	DI Bit 3 +	A10	DI Bit 3 Return
B11	DI Bit 4 +	A11	DI Bit 4 Return
B12	DI Bit 5 +	A12	DI Bit 5 Return
B13	DI Bit 6 +	A13	DI Bit 6 Return
B14	DI Bit 7 +	A14	DI Bit 7 Return
B15	DI Bit 8 +	A15	DI Bit 8 Return
B16	DI Bit 9 +	A16	DI Bit 9 Return
B17	DI Bit 10 +	A17	DI Bit 10 Return
B18	DI Bit 11 +	A18	DI Bit 11 Return
B19	DI Bit 12 +	A19	DI Bit 12 Return
B20	DI Bit 13 +	A20	DI Bit 13 Return
B21	DI Bit 14 +	A21	DI Bit 14 Return
B22	DI Bit 15 +	A22	DI Bit 15 Return
B23	DI Bit 16 +	A23	DI Bit 16 Return
B24	DI Bit 17 +	A24	DI Bit 17 Return
B25	DI Bit 18 +	A25	DI Bit 18 Return
B26	DO Bit 1 #	A26	DO Bit 1 Return

Connector Pin Assignments - Continued

Pin	Function
B27	DO Bit 2 #
B28	DO Bit 3 #
B29	DO Bit 4 #
B30	DO Bit 5 #
B31	DO Bit 6 #
B32	DO Bit 7 #
B33	DO Bit 8 #
B34	DO Bit 9 #
B35	DO Bit 10 #
B36	DO Bit 11 #
B37	DO Bit 12 #
B38	DO Bit 13 #
B39	DO Bit 14 #
B40	DO Bit 15 #
B41	DO Bit 16 #
B42	DO Bit 17 #
B43	DO Bit 18 #

Pin	Function
A27	DO Bit 2 Return
A28	DO Bit 3 Return
A29	DO Bit 4 Return
A30	DO Bit 5 Return
A31	DO Bit 6 Return
A32	DO Bit 7 Return
A33	DO Bit 8 Return
A34	DO Bit 9 Return
A35	DO Bit 10 Return
A36	DO Bit 11 Return
A37	DO Bit 12 Return
A38	DO Bit 13 Return
A39	DO Bit 14 Return
A40	DO Bit 15 Return
A41	DO Bit 16 Return
A42	DO Bit 17 Return
A43	DO Bit 18 Return

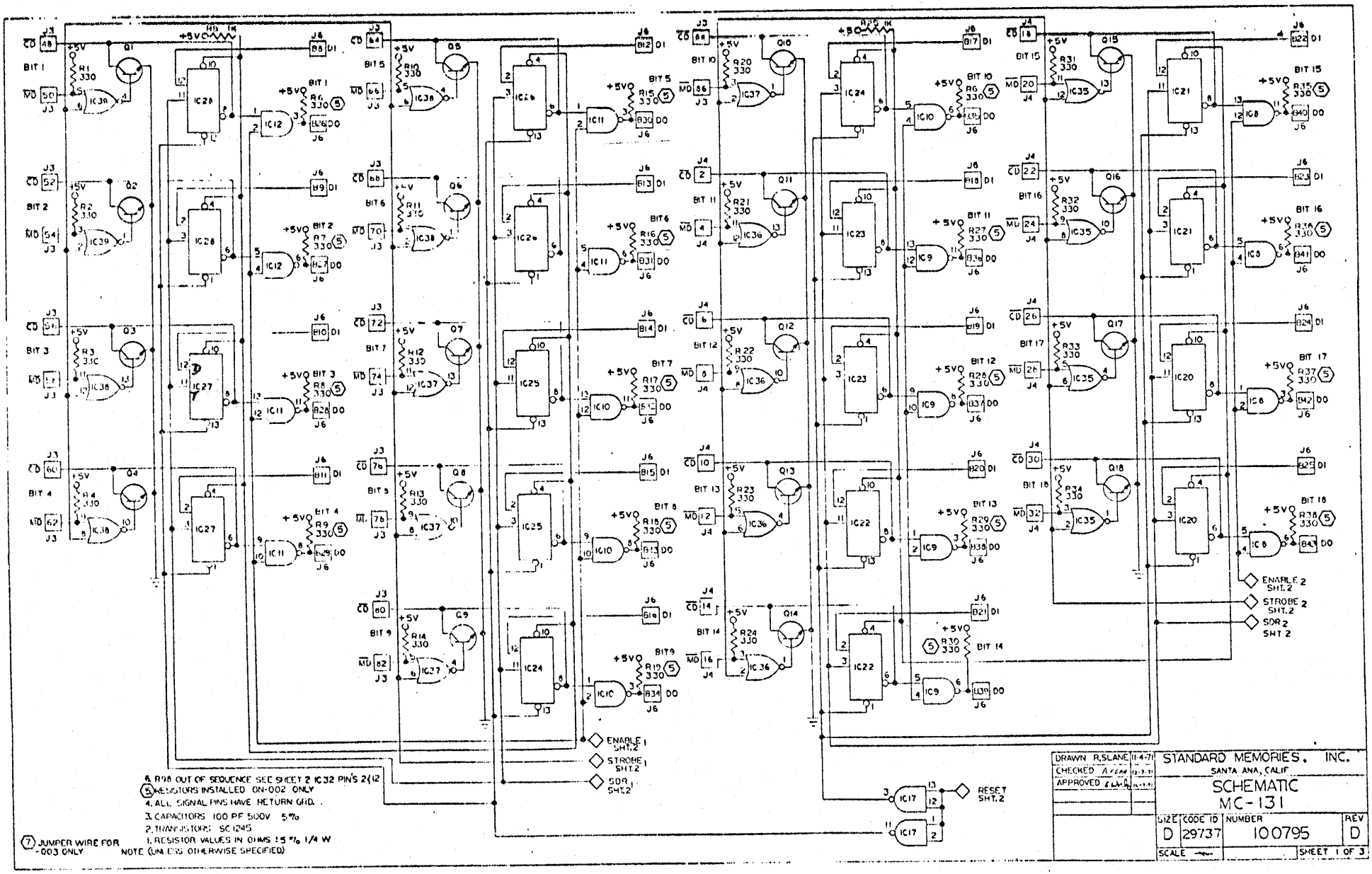
= Indicates space for pullup resistor only.
+ = Indicates space for termination on board.



(6) USED ONLY ON -003
(7) IC-1,13 NOT USED ON -001, 002, 003
(8) 16, 9, 15, 19, 26 - 30, 35 - 38 MC USED ON DASH 002 ONLY
(9) RUBBER STAMP ASSEMBLY DASH NUMBER AND REV. LET. APPROXIMATELY, WHERE SHOWN ON SOLDER SIDE

2. SCHEMATIC FOR ASSEMBLY IS STANDARD MEMORIES DRAWING 100790
1. MC 131 PARTS LIST FOR ASSEMBLY IS STANDARD MEMORIES DRAWING P/L 100819
NOTE: UNLESS OTHERWISE SPECIFIED

-003		ECOM F-11
-002		PULL UP RESISTORS ON DATA OUT
-001		DATA AND ERROR MEMORY CONTROL MODULE
DASH NO.	MINTEL	DESCRIPTION
DRAWN R. CLARK	2-11-77	STANDARD MEMORIES INC.
CHECKED A.E.	2-11-77	SANTA ANA, CALIF.
APPROVED E.W.	2-11-77	ASSEMBLY — MC-131
SIZE E	FSCM NO. 29737	NUMBER 100819
REV D		
SHT 2 OF 4		



6. R98 OUT OF SEQUENCE SEE SHEET 2 IC32 PINS 2 & 12
5. RESISTORS INSTALLED ON-002 ONLY
4. ALL SIGNAL PINS HAVE RETURN GRID.
3. CAPACITORS 100 PF 500V 5%
2. TRANSISTORS SC1245
1. RESISTOR VALUES IN OHMS ±5% 1/4 W
7. JUMPER WIRE FOR -003 ONLY

NOTE (UNLESS OTHERWISE SPECIFIED)

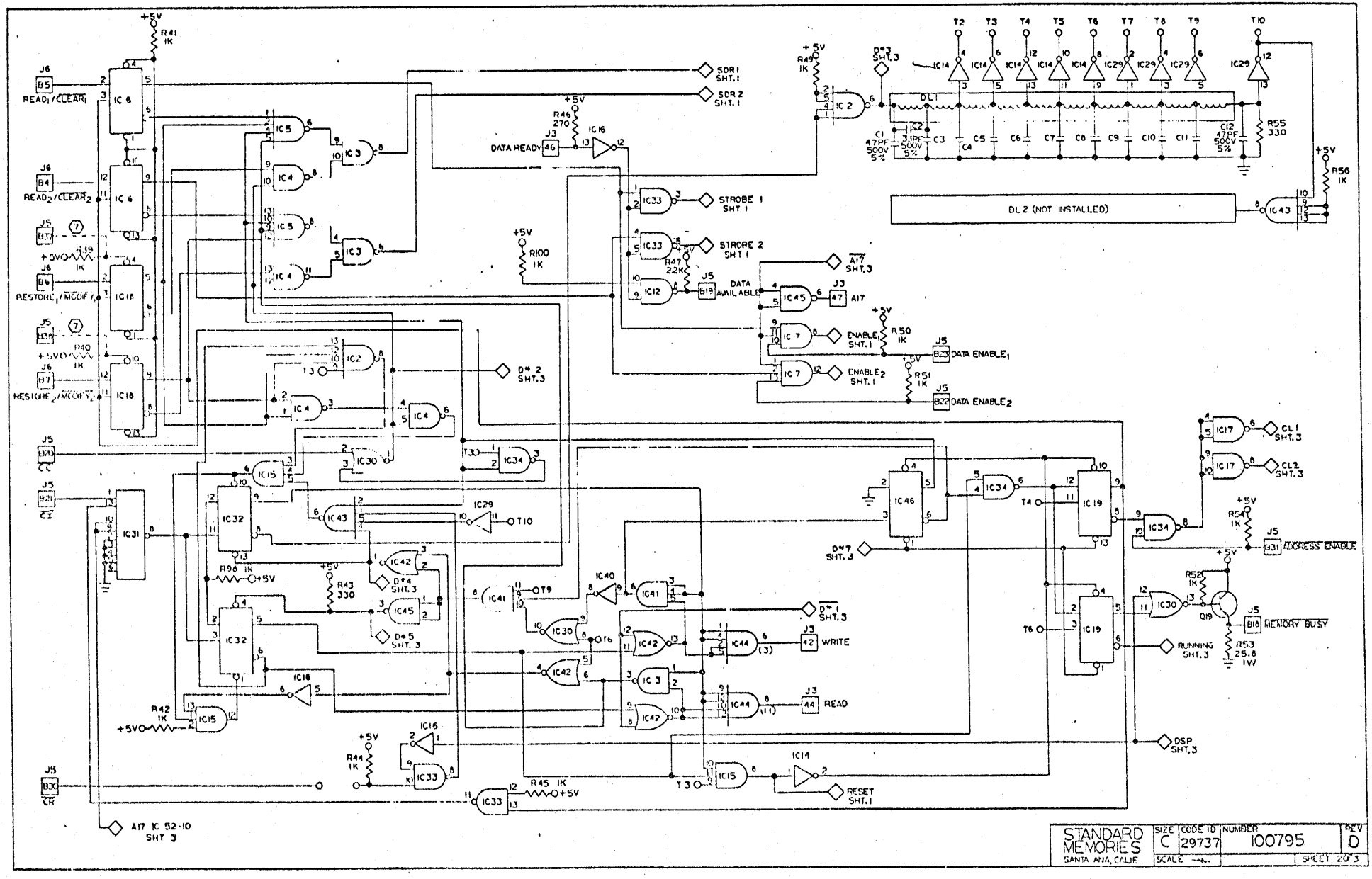
DRAWN	R.SLANE 11-4-71
CHECKED	A.CHAN 12-2-71
APPROVED	12-13-71

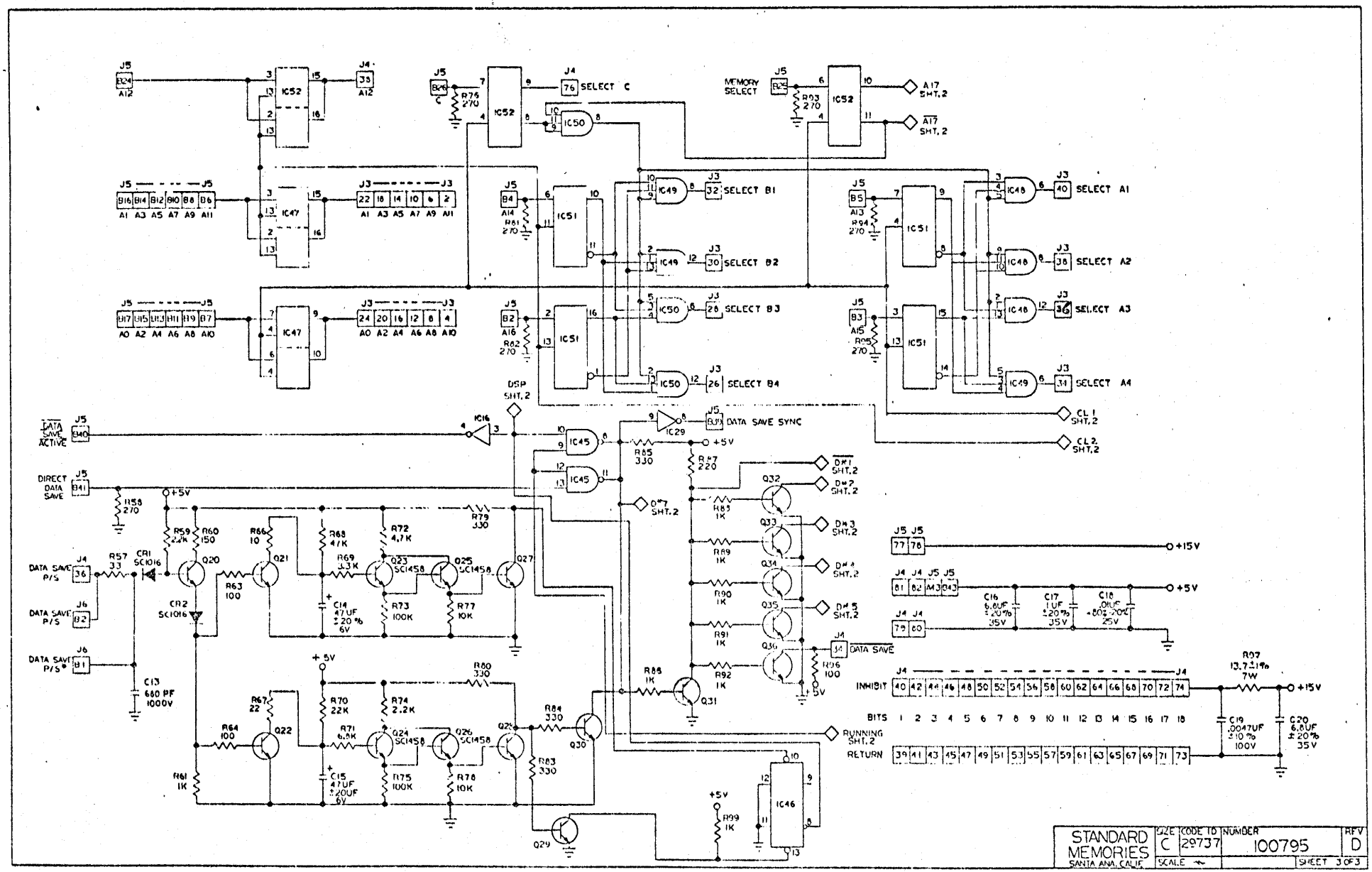
STANDARD MEMORIES, INC.
SANTA ANA, CALIF.

SCHEMATIC
MC-131

SIZE	CODE ID	NUMBER	REV
D	29737	100795	D

SCALE — SHEET 1 OF 3


+5V
R41 1K
J6 B5 READ1/CLEAR1
J6 B4 READ2/CLEAR2
J5 B11
J6 B6 RESTORE1/MODIF1
J5 B14
J6 B7 RESTORE2/MODIF2
J5 B13
J5 B21 CI
J5 B33 CR
IC 6
IC 18
IC 31
IC 32
IC 5
IC 4
IC 3
IC 2
IC 15
IC 16
IC 30
IC 33
IC 34
IC 43
IC 42
IC 41
IC 40
IC 44
IC 45
IC 12
IC 7
IC 46
IC 17
IC 19
IC 14
IC 29
SDR1 SHT.1
SDR2 SHT.1
DATA READY
J3 46
R46 270
STROBE 1 SHT 1
STROBE 2 SHT 1
R47 22K
J5 B19 DATA AVAILABLE
A17 SHT.3
J3 47 A17
ENABLE1 SHT.1
ENABLE2 SHT.1
R50 1K
R51 1K
J5 B23 DATA ENABLE1
J5 B22 DATA ENABLE2
R100 1K
D*2 SHT.3
D*4 SHT.3
D*5 SHT.3
D*7 SHT.3
D*1 SHT.3
R98 1K
R43 330
R42 1K
R44 1K
R45 1K
J3 42 WRITE
J3 44 READ
RESET SHT.1
A17 IC 52-10 SHT 3
T2 T3 T4 T5 T6 T7 T8 T9 T10
DL1
DL2 (NOT INSTALLED)
C1 47PF 500V 5%
C2 3PF 500V 5%
C12 47PF 500V 5%
R55 330
R56 1K
CL1 SHT.3
CL2 SHT.3
R54 1K
J5 B31 ADDRESS ENABLE
R52 1K
Q19
J5 B18 MEMORY BUSY
R53 25.8 1W
RUNNING SHT.3
DSP SHT.3
STANDARD MEMORIES
SANTA ANA, CALIF
SIZE C
CODE ID 29737
NUMBER 100795
REV D
SCALE
SHEET 2 OF 3


SELECT C
SELECT B1
SELECT B2
SELECT B3
SELECT B4
SELECT A1
SELECT A2
SELECT A3
SELECT A4
DATA SAVE SYNC
DATA SAVE
RUNNING
INHIBIT
BITS 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
RETURN
+5V
+15V
STANDARD MEMORIES
SANTA ANA, CALIF.
SIZE C
CODE ID 29737
NUMBER 100795
REV D
SCALE
SHEET 3 OF 3

		DATE
PREPARED	Al Egan	10/22/71
CHECKED	R.AS	11-22-71
PROJ ENGR	E. Worley	11-22-71
APPROVED	RJA	11/23/71

STANDARD MEMORIES, INC.

SANTA ANA, CALIF.
CODE IDENT 29737

PL 100819

PARTS LIST

ASSEMBLY TITLE
MC-131

REV E
REV DATE 6-21-72
REV AUTH
SHEET 1 OF 3

	-001	-002	-003	-	-	-	-
	REV E DATE 6-21-72	REV E DATE 6-21-72	REV D DATE 6-21-72	REV DATE	REV DATE	REV DATE	REV DATE
	QTY	QTY	QTY	QTY	QTY	QTY	QTY
ITEM	EACH EXT	EACH EXT	EACH EXT	EACH EXT	EACH EXT	EACH EXT	EACH EXT
1	1						
5	1						
10	8						
12	2						
14	1						
16	4						
18	14						
20	8						
22	7						
24	6						
26	8						
28	1						
30	1						
32	2						
35	4						
37	32						
42	2						
47	1						
49	1						
51	1						
52							
53	3						
55	1						

REFERENCE DESIGNATION	DESCRIPTION	SMI PART NO OR SPEC NO	
H1	Printed Circuit Bd.	100818	
H2	Ejector Mount	100811-001	
IC4, 33, 34	TTL Quad 2-in. NAND	SC1038	SN7400N
IC5, 43	TTL Dual 4-in NAND Buffer	SC1039-001	SN7440N
IC2	TTL Dual 4-in Hisp NAND Buf	SC1039-002	SN74H40
IC14, 16, 29 40	TTL Hex Inverter	SC1201	SN7404N
IC6, 18-28, 32, 46	TTL. Hi Speed Dual-D	SC1202	SN74H74N
IC47, 51, 52	TTL QUAD Latch	SC1203	SN7475N
IC30, -35-39 42	TTL Quad 2-in NOR	SC1204	SN7402N
IC7, 15, 41 48-50	TTL Triple 3-in AND	SC1047	SN74H11N
IC8-12, 45	TTL Quad 2-in NAND Buffer O.C.O.	SC1477	SN7438
IC31	2-2-2-3 and/or Invert	SC1505	SN74H53N
IC44	TTL Quad 2-in. Hi-Speed AND	SC1043-002	SN74H08N
IC3, 17	TTL Quad 2-In NAND Buffer	SC1478	SN7437N
Q23-26	NPN 2N930	SC1458	2N930
Q1-22, 27-36	NPN 2N2369	SC1245	2N2369
CR1, 2	Silicon Switching Diode	SC1016	FDH600
R66	10Ω 1/4W 5%	SC1249-001	
R67	22Ω 1/4W 5%	SC1249-002	
R57	33Ω 1/4W 5%	SC1249-003	
R68	68Ω 1/4W 5%	SC1249-005	
R63, 64, 96	100Ω 1/4W 5%	SC1249-007	
R59	150Ω 1/4W 5%	SC1249-009	

PROPRIETARY RIGHTS OF STANDARD MEMORIES INCORPORATED ARE INVOLVED IN THIS SUBJECT MATTER AND ALL MANUFACTURING, REPRODUCTION, USE AND SALES RIGHTS PERTAINING TO SUCH SUBJECT MATTER ARE EXPRESSLY RESERVED. IT IS SUBMITTED IN CONFIDENCE FOR A SPECIFIED PURPOSE, AND THE RECIPIENT BY ACCEPTING THIS MATERIAL AGREES THAT THIS MATERIAL WILL NOT BE USED, COPIED OR REPRODUCED IN WHOLE OR IN PART NOR ITS CONTENTS REVEALED IN ANY MANNER OR TO ANY PERSON EXCEPT TO MEET THE PURPOSE FOR WHICH IT WAS DELIVERED

		DATE
PREPARED	Al Egan	10/22/71
CHECKED	R.A.S.	11/22/71
PROJ ENGR		
APPROVED		

STANDARD MEMORIES, INC.

SANTA ANA, CALIF.
CODE IDENT 29737

PL 100819
PARTS LIST
ASSEMBLY TITLE
MC-131

REV E
REV DATE 6-21-72
REV AUTH
SHEET 2 OF 3

	– 001		– 002		– 003		–		–		–		–				
	REV E DATE 6-21-72		REV E DATE 6-21-72		REV D DATE 6-21-72		REV DATE		REV DATE		REV DATE		REV DATE				
	QTY		QTY		QTY		QTY		QTY		QTY		QTY				
ITEM	EACH	EXT	EACH	EXT	EACH	EXT	EACH	EXT	EACH	EXT	EACH	EXT	EACH	EXT	REFERENCE DESIGNATION	DESCRIPTION	SMI PART NO OR SPEC NO
58	1														R87	220Ω 1/4W 5%	SC1249-009
60	8														R46, 58, 76, 81, 82, 93, 94, 95	270Ω 1/4W 5%	SC1249-023
63	25														R1-4, 10-14, 20-24, 31-34, 43, 55, 79, 80, 83, 84, 85	330Ω 1/4W 5%	SC1249-010
67															R1-4, 6-24, 26-28, 43, 55, 79, 80, 84, 85, 65	330Ω 1/4 5%	SC1249-010
69															R70	470Ω 1/4 5%	SC1249-011
70	24														R5, 25, 38-42, 44, 45, 49-52, 54, 55, 61, 88, 88-92, 98-100	1K 1/4W 5%	SC1249-013
73	3														R47, 59, 74	2.2K 1/4W 5%	SC1249-015
75	1														R69	3.3K 1/4W 5%	SC1249-016
77	1														R72	4.7K 1/4W 5%	SC1249-017
79	1														R71	6.8K 1/4W 5%	SC1249-018
81	2														R77, 78	10K 1/4W 5%	SC1249-019
83	1														R70	22K 1/4W 5%	SC1249-020
85	1														R68	47K 1/4W 5%	SC1249-021
87	2														R73, 75	100K 1/4W 5%	SC1249-022
89	1														R53	25.5Ω 1W 2%	SC1253-001
91	18														R97	13.7Ω 7W 1%	SC1260-001
95	1														C2	33pf 500V 5%	SC1272-003
97	2														C1, 12	47pf 500V 5%	SC1272-004
99	9														C3-11	100pf 500V 5%	SC1272-006
101	1														C13	680pf 1KV 10%	SC1273-002
103	13														C18	.01μf +80 -20% 25V	SC1274-001
105	18														C19	.0047μf ±10% 100V	SC1275-006
107	13														C17	1μf ±20% 35V	SC1277-001
109	26														C16, 20	5.2μf ±20% 35V	SC1277-002
111	2														C14, 15	47μf ±20% 6V	SC1280-001

PROPRIETARY RIGHTS OF STANDARD MEMORIES INCORPORATED ARE INVOLVED IN THIS SUBJECT MATTER AND ALL MANUFACTURING, REPRODUCTION, USE AND SALES RIGHTS PERTAINING TO SUCH SUBJECT MATTER ARE EXPRESSLY RESERVED. IT IS SUBMITTED IN CONFIDENCE FOR A SPECIFIED PURPOSE, AND THE RECIPIENT BY ACCEPTING THIS MATERIAL AGREES THAT THIS MATERIAL WILL NOT BE USED, COPIED OR REPRODUCED IN WHOLE OR IN PART NOR ITS CONTENTS REVEALED IN ANY MANNER OR TO ANY PERSON EXCEPT TO MEET THE PURPOSE FOR WHICH IT WAS DELIVERED

		DATE
PREPARED	Al Egan	10/22/71
CHECKED	R.A.S	11-22-71
PROJ ENGR		
APPROVED		

STANDARD MEMORIES, INC.

SANTA ANA, CALIF.
CODE IDENT 29737

PL 100819	REV E
PARTS LIST	REV DATE 6-21-72
ASSEMBLY TITLE MC-131	REV ADTN
	SHEET 3 OF 3

	-001		-002		-003		-		-		-		-	
	REV E DATE 6-21-72		REV E DATE 6-21-72		REV D DATE 6-21-72		REV DATE		REV DATE		REV DATE		REV DATE	
	QTY		QTY		QTY		QTY		QTY		QTY		QTY	
ITEM	EACH	EXT	EACH	EXT	EACH	EXT	EACH	EXT	EACH	EXT	EACH	EXT	EACH	EXT
113	1													
118	2													
123	36													
125	4													
130	4													
132	4													
135	4													
140	36													
145														
147														

REFERENCE DESIGNATION	DESCRIPTION	SMI PART NO OR SPEC NO
DL1	Delay Line	SC1473-001
H3	Ejector	SC1385-001
H4	Spacer Phenolic	SC1084-001
H5	Spacer No. 4 1/4	SC1382-001
H6	Lock Screw (Pan Phil) No. 4-40 1/2	SC1405-006
H11	Washer, Flat No. 4	SC1369-002
H7	Nut, Hex 4-40	SC1373-001
H8	Transipad	SC1394-001
H9	Wire Tinned 26Ga.	SC1323-004
H10	Insulation Teflon #26	SC1324-004

Total Items -001 = 52
-002 = 52
-003 = 54

PROPRIETARY RIGHTS OF STANDARD MEMORIES INCORPORATED ARE INVOLVED IN THIS SUBJECT MATTER AND ALL MANUFACTURING, REPRODUCTION USE AND SALES RIGHTS PERTAINING TO SUCH SUBJECT MATTER ARE EXPRESSLY RESERVED. IT IS SUBMITTED IN CONFIDENCE FOR A SPECIFIED PURPOSE, AND THE RECIPIENT BY ACCEPTING THIS MATERIAL AGREES THAT THIS MATERIAL WILL NOT BE USED, COPIED OR REPRODUCED IN WHOLE OR IN PART NOR ITS CONTENTS REVEALED IN ANY MANNER OR TO ANY PERSON EXCEPT TO MEET THE PURPOSE FOR WHICH IT WAS DELIVERED

SECTION II

THEORY OF OPERATION

2.1 MODE CONTROL AND TIMING

A memory cycle in any mode is initiated by a $\overline{\text{Cycle Initiate}}$ ($\overline{\text{CI}}$) pulse. The mode control terms Read/$\overline{\text{Clear}}$ and Restore/$\overline{\text{Modify}}$ determine full or split cycle timing and the function to be performed. The four combinations of these terms and their definitions are:

Mode		Function	
Read	Restore	Full Cycle	Read-Restore
$\overline{\text{Clear}}$	Restore	Full Cycle	Clear-Write
Read	$\overline{\text{Modify}}$	Split Cycle	Read-Modify-Write
$\overline{\text{Clear}}$	$\overline{\text{Modify}}$	Split Cycle	Clear-Write

One complete memory cycle in any of these four combinations requires that a Read and then a Write command be presented to the memory. During the Read command, information will be taken from the memory and the cores will be "cleared". During the Write command, this information will either be restored or new information will be written into the cores.

By the use of Byte control, any pair of the above four combinations may be requested. When the mode control requests that one byte of memory perform a full cycle operation and the other a split cycle

operation, the memory controller will perform both requested operations with split cycle timing. For example, it is possible to Read-Pause-Write Byte $_2$. Data will be restored in Byte $_1$ and Data In will be written into Byte $_2$ at the conclusion of the pause.

Memory Mode	Read/$\overline{\text{Clear}}$ $R/\overline{C}_1$	$R/\overline{C}_2$	Restore/$\overline{\text{Modify}}$ $R/\overline{M}_1$	$R/\overline{M}_2$
Full Cycle:				
Read-Restore (R/R)	T	T	T	T
Clear-Write (C/W)	F	F	T	T
R/R Byte$_1$ C/W Byte$_2$	T	F	T	T
C/W Byte$_1$ R/R Byte$_2$	F	T	T	T
Split Cycle:				
Read-Modify-Write(RMW)	T	T	F	F
Clear- Pause-Write	F	F	F	F
RMW Byte$_1$ C/W Byte$_2$	T	F	F	F
C/W Byte$_1$ RMW Byte$_2$	F	T	F	F
--- etc. ---				

In the following descriptions of the MC-131 operation, positive logic notation is used. That is, a logic zero is ground or a low impedance, and a logic one is plus voltage or a high impedance. The MC-131 uses TTL logic, primarily the 7400 series.

The various manufacturers of this logic define a logic one as between +2.0 and +5.0 volts and a logic zero as between ground and +0.8 volts.

All internal timing in the MC-131 is obtained from a delay line. This

technique provides reliable and consistent timing with temperature and time. There are no significant differences in delays among paths propagating related signals, such as will be found between common asynchronous single shot multivibrators.

Two pulses are sent down the delay line to provide timing for the above functions. The first pulse is for the Read command, the second is for the Write command. Flip flop IC32 (pin 9) determines the width of the delay line pulse and the duration of the Read and Write commands. IC32 pins 5 and 6 provide control ; pin 5 is a logic one for a Write pulse, pin 6 is a logic one for a Read pulse.

In both the full cycle and split cycle modes $\overline{CI}$ clocks flip flop IC32 which starts the first pulse down the delay line. The flip flop will also initiate the Read command. When the leading edge of the pulse arrives at tap 6 of the delay line, it will reset the flip flop which in turn (a) terminates the Read command, (b) establishes the end of the pulse and (c) toggles IC32 pins 5 and 6.

In the full cycle modes, when the trailing edge of the pulse reaches delay line tap 3, it will set flip flop IC32 (pin 9) for the second time, thereby generating both the second delay line pulse and the Write command. When the leading edge of the second pulse arrives at

tap 6, it will again reset the flip flop terminating the Write command, establishing the end of the second pulse and toggling IC32 pins 5 and 6 back to their original state. As IC32 pin 6 had been returned to its original state, the trailing edge of the second pulse will not set the flip flop when it appears at tap 6. This pulse will continue down the delay line providing the signals to conclude the cycle.

In the split cycle modes, the first pulse will not reset flip flop IC32 when it arrives at tap 3 as IC2 pin 8 has been forced to a logic one state. The pulse will continue down the delay line without consequence. A $\overline{\text{Cycle Continue}}$ ($\overline{\text{CC}}$) command is required to complete the memory cycle. This command will set flip flop IC32 and thereby, start the Write command and the second delay line pulse. The logic will be reset, as above, when the trailing edge of the second pulse reaches tap 3.

2.2 ADDRESS AND MEMORY SELECT

The thirteen low order address bits A_0 through A_{12} are buffered by IC47 and 52, a Quad Latch Type flip flop used as a register. The output terms of the register go directly to the memory where they are decoded to select one of the up to 8192 words.

The clock terms to the register are normally a logic one allowing the output nodes, after one propagation delay, to follow the signal on the input nodes. When a $\overline{CI}$ command is received, the clock terms will go to a logic zero setting the register; therefore, it is required that the address terms be stable 25ns prior to, and remain stable 100ns after, the leading edge of $\overline{CI}$ (see section 1.2.3 for I/O Timing Diagrams). The clock terms will remain a logic zero until the memory cycle is completed. In addition, the $\overline{Address\ Enable}$ term can be used to externally set the register between cycles

The four high order address bits A_{13} through A_{16} are operated upon as above with the exception that two 1 of 4 decoding networks are between the output of the register and the memory. In a normal ECOM® F memory system, one term of each decoding network is connected to each memory module allowing the selection of one of a possible sixteen modules. The decoder truth tables are:

	Select		Select
A_{15} A_{13}	B_4 B_3 B_2 B_1	A_{14} A_{12}	A_4 A_3 A_2 A_1
0 0	0 0 0 1	0 0	0 0 0 1
0 1	0 0 1 0	0 1	0 0 1 0
1 0	0 1 0 0	1 0	0 1 0 0
1 1	1 0 0 0	1 1	1 0 0 0

The input nodes of address terms A_{13} through A_{16} are connected to ground through a 270Ω resistor to ensure a logical zero to the decoder when the address term is not connected on the I/O.

Two other address terms are present on the MC-131. "Memory Select" can be used as an extended address which will disable the MC-131 by blocking incoming $\overline{CI}$ and force all data out terms to a high level. As received from the factor "Memory Select" is forced low via a 270Ω so it will have no effect unless a signal is sent to J5B25. Also available is 'C', J5B26, which if forced high, will cause all A selects and B selects to go low, thereby selecting no memory but will cause 'Select C', J476, to go high. During a cycle with 'C' at a logical one all lower order address' and control and data functions are available. 'C' is forced low via a 270Ω for standard operation.

2.3 $\overline{\text{MEMORY BUSY}}$

When this term, driven by an emitter follower, is at a logic zero, the memory is either performing a cycle or is in a power shutdown condition.

When a $\overline{\text{CI}}$ command is given, it will clock flip flop IC-32 and turn off the emitter follower, and forcing $\overline{\text{Memory Busy}}$ to a logic zero. The transition from a logic one to a logic zero of the second pulse on the delay line will set the flip flop IC-19 and thereby, returning $\overline{\text{Memory Busy}}$ to the logic one state.

At the start of an AC power down condition, transistor Q33 will turn off, forcing IC30 (pin 13) to a logic zero and thereby, grounding the base of the emitter follower. As the DC power fails, the output node of IC45 will approach a high impedance and the emitter follower output will remain low. After the return of AC power, transistor Q33 will remain off for a time constant allowing DC power to return within tolerances and registers to be reset before allowing $\overline{\text{Memory Busy}}$ to return to a logic one.

2.4 DATA IN/DATA OUT

The MC-131 data circuitry has been divided into two identical, independent, nine bit Bytes under the control of the Read/$\overline{\text{Clear}}$ and Restore/$\overline{\text{Modify}}$ commands.

Data In is clocked into the data register by SDR. The inverting output of the register is provided to the memory modules as $\overline{\text{Control Data}}$ ($\overline{\text{CD}}$).

The Data Ready signal from the memory modules is inverted, gated with Read and used to strobe $\overline{\text{Memory Data}}$ ($\overline{\text{MD}}$) into the data register. Note that $\overline{\text{MD}}$ is inverted twice and is present at the output nodes of the register. During a restore cycle $\overline{\text{MD}}$ will be returned to the memory as $\overline{\text{CD}}$. The data register is connected to Data Out through a Nand gate, providing another inversion. Thus, there is an inversion of data from Data In to the memory module and an inversion of data from the memory module to Data Out. Data In and Data Out are of the same sense.

Data Enable 1 and 2 controls the connections of the data register to the Data Out bus. If Data Enable is a logic one, Data Out will be the complement of $\overline{\text{MD}}$ when the MC-131 is in a Read mode and will be a

high impedance when in a clear mode. When Data Enable is a logic zero, Data Out will be a high impedance. Thus, by controlling the modes and Data Enable; the MC-131 may be used with a common buss system. Provisions exist to Byte control Data Enable. If desired, Data In may be connected to Data Out for use with a two way buss. With Byte control, the data terms may be paralled in effect producing a nine bit memory of twice the number of words.

Each processing system is different. In an attempt to provide a "universal" interface, pull up resistors are not factory installed on the I/O. For those systems requiring them on the MC-131 provision has been made for the field installation of pull-up resistors to +5 volts. Plated through holes for the Data Out terms, are provided adjacent to IC8, IC9, IC10, IC11, and IC12. The hole pairs corresponding to Data Out bits 1 and 18 are indicated by the numbers 1 and 18 adjacent to IC8 and IC12 respectively. Provision is also made to terminate the signal inputs check the J5 & J6 pin list for the provision made on each signal.

2.5 INHIBIT NETWORK

The MC-131 contains the current determining resistors (R97), energy storage capacitors (C20), and pulse shaping capacitors (C19), for the memory modules inhibit circuitry. As only one memory module under the control of the MC-131 is active at any time, the inhibit

resistors are time shared.

2.6 $\overline{\text{DATA SAVE}}$

Data retention in the memory module during a power transient condition is accomplished by (1) not allowing Read or Write commands to be sent to the memory and (2) providing a $\overline{\text{Data Save}}$ term to the memory module which will be used to prevent operation of it's X-Y drive current source. When the input term Data Save P/S is at a logic zero, the memory will be allowed to operate; when it is at a logic one, the memory will not be allowed to operate.

On power turn-on the Data Save P/S signal must be a logic one until the +5 and ±15 volt power supplies approach their tolerances. When Data Save P/S returns to a logic zero, the MC-131 timing logic will have been reset and two time constants will start. The first to time out (R74-C15) will remove the reset commands and, by returning $\overline{\text{Data Save}}$ to a logic one, allow the memory module's current source to operate. The longer time constant (R68-C14) will return the $\overline{\text{Memory Busy}}$ signal to a logic one indicating that the memory is now stable and that $\overline{\text{CI}}$ commands will be accepted.

On power turn-off the Data Save P/S signal must go to a logic one. The power supplies must remain within tolerance for at least 20μs after Data Save P/S switches to allow the completion of any memory

cycles in progress. Data Save P/S will turn on transistor Q20 which provides base drive to Q21 and Q22. Transistor Q21 will discharge C14 through R16, thereby, turning off Q27. The collector of Q8 will become a logic one, (a) turning off Q19 providing a $\overline{\text{Memory Busy}}$ signal and (b) turning on IC43 (pin 6) forcing the concluding memory cycle in progress. The longer time constant C15 discharging through R67 and Q22 will provide time for the memory to conclude its cycle before Q36 provides a $\overline{\text{Data Save}}$ command to the memory.

A Data Save P/S signal is generated in the ECOM® F system power supply when the AC line drops below a preset value. This term is connected to connector J4 (pin 36) in all SMI chassis. The MC-131 connects this term directly to the I/O connector J6 pin B1 and through a 33Ω resistor (R57) to J6 pin B2 and the data retention circuitry. The memory's Data Save P/S signal can be used by the processor to control a shutdown sequence. If this is desired, R57 should be removed and the processor should provide the command to save data at J6 pin B2.

Three new signals are available to the MC-131 user. '$\overline{\text{Direct Data Save}}$' provides a direct, no time constant, way of forcing a Data Save action. $\overline{\text{Data Save Active}}$ is an output signal indicating that the Data Save is now fully in operation. Data Save Sync allows one MC-131 to operate as a master with any other MC-131's Data Save slaved to its operation.

SECTION III

INSTALLATION

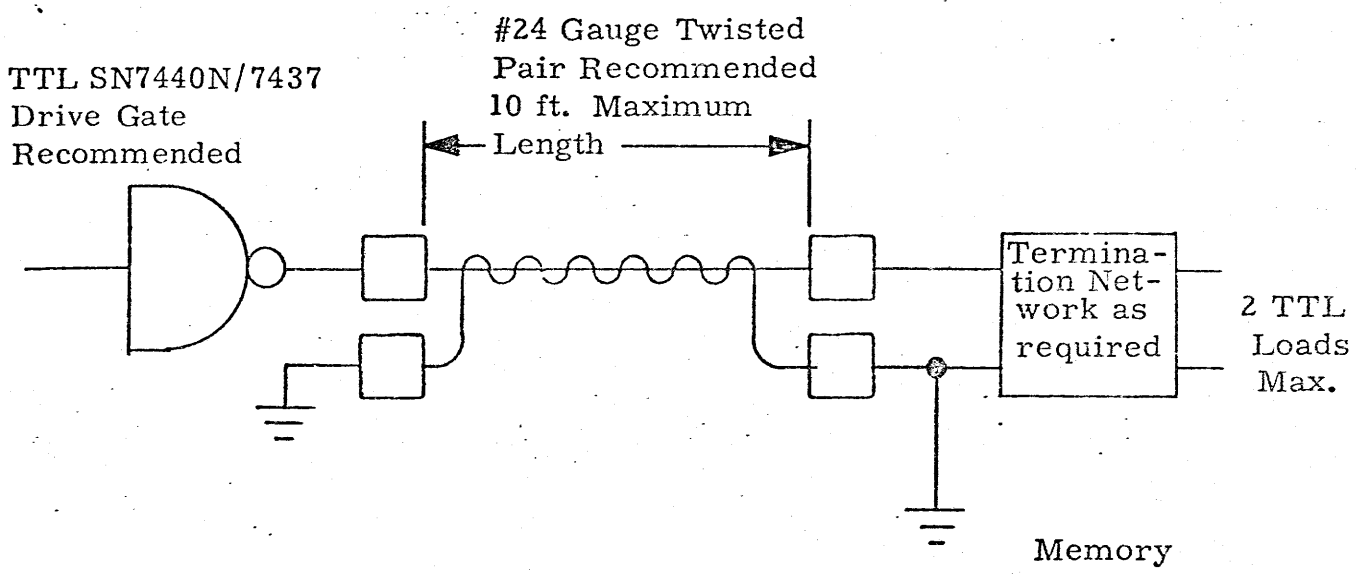
3.1 ELECTRICAL INTERFACE AND TERMINATIONS

All I/O signal connections to the MC-131 should be made with twisted pair. Number 24 insulated hookup wire twisted pair (24 TPF) is sufficient. All output lines, with the exception of $\overline{\text{Memory Busy}}$, are driven by open collector gates and should be terminated to +5 volts. It is recommended that these terminations be located at the receiving end of the line. (See recommended input and output interface, Figure 1). If the distance between the MC-131 and the receiving gates is short, it may be desirable to locate the pull-up resistors on the MC-131. Plated through holes are provided for this purpose. Provision has been made for termination of the address signals, Data In, and control signals.

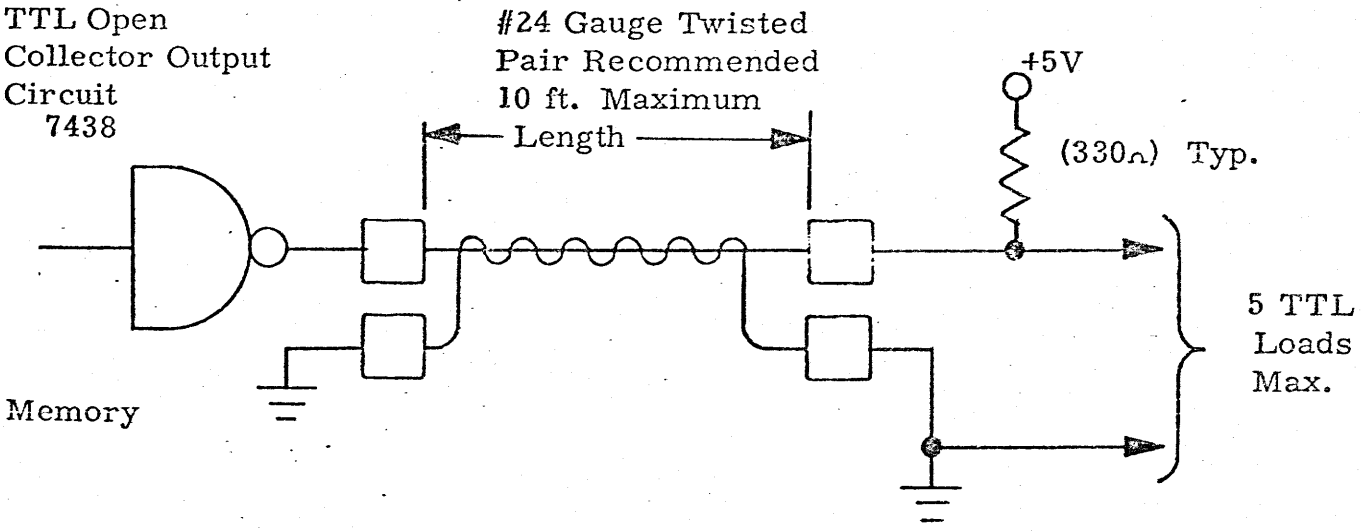
The MC-131 to memory module interface should not be in excess of three feet and must be twisted pair. The inhibit lines should not be bundled with lines carrying logic levels.

DC power supply lines should be of sufficient size to prevent the supply voltage at any module from going out of specification. The power supply shall be floating from earth ground.

FIGURE 1



Recommended Memory Input Interface



Recommended Memory Output Interface

3.2 MEMORY EXPANSION

The memory controller, with the use of Byte control, allows the 18 bit memory modules to be operated as a nine bit memory. In this mode of operation it is recommended that the two bytes be paralled (i.e., Data In and Data Out bits 1 and 10 tied together, bits 2 and 11 tied together, etc.). See section 2.1 for mode information.

Expansion of memory word length is possible by operating memory controllers in parallel. For example, a 36 bit word can be obtained by using two eighteen bit memory systems. Identical address and I/O control terms of the two memory controllers would be daisy-chained together. Data In and Data Out bits 1-18 should be connected to memory controller 1 and bits 19-36 should be connected to memory controller 2.

Field expansion of the number of words of memory is possible by the addition of memory modules to a maximum of 16 modules(131Kwords). Details of this expansion are included in the section on the memory module. Expansion to excess of 131K words is accomplished by the addition of memory controllers. Additional special MC configurations can be implemented using the MC-131. Please consult the factory if you need assistance.

Modified : Ballarup 4/10-72

ECOM® F MEMORY SYSTEM & ENCLOSURE

MINI MASS/ME-111

STANDARD MEMORIES, INC.
2801 E. Oakland Park Blvd., Suite 301
Ft. Lauderdale, Florida 33306

DRAWN AE	7/25/72	ECOM® F MEMORY SYSTEM & ENCLOSURE
CHECKED E. Dowell	8-7-72	MINI MASS/ME-111
APPROVED [illegible]	8/7/72	

STANDARD MEMORIES SANTA ANA, CALIF.	SIZE A	CODE IDENT	NUMBER SC1651	REV
	SCALE		Form F-011271	SHEET

PROPRIETARY RIGHTS of STANDARD MEMORIES, INCORPORATED are involved in this subject matter and all manufacturing, reproduction, use and sales rights pertaining to such subject matter are expressly reserved. It is submitted in confidence for a specified purpose, and the recipient by accepting this material agrees that this material will not be used, copied or reproduced in whole or in part nor its contents revealed in any manner or to any person except to meet the purpose for which it was delivered.

WARRANTY

All products manufactured by STANDARD MEMORIES, INC. are warranted to be free from defects in material and workmanship one year from date of delivery to the original purchaser.

STANDARD MEMORIES, INC's obligation under this warranty is limited to servicing or adjustment of any equipment returned to the factory for that purpose, and replacing any defective parts thereof. If the failure has been caused by misuse, operation in excess of specification guarantees, or modification by the customer, repairs will be billed at cost. In such cases, a cost estimate will be submitted before work is started.

This warranty is expressly in lieu of all other obligations or liabilities on the part of STANDARD MEMORIES, INC., and STANDARD MEMORIES, INC. neither assumes nor authorizes any other person to assume for them, any liability in connection with the sale of STANDARD MEMORIES, INC. products.

TABLE OF CONTENTS

SECTION I

ECOM® F MEMORY SYSTEM

SECTION I

ECOM® F MEMORY SYSTEM

1.1 DESCRIPTION

The ECOM® F memory system provides a low cost, modular approach to memory organization.

Features of the system include:

- 750ns Full Cycle Time
- 325ns Access Time
- Low Cost Field Expansion
- Power Failure Data Protection
- Wide Temperature Operation
- DTL/TTL Compatible Interface
- High Reliability Integrated Circuit Logic
- Byte Control Capability

A complete 18 bit system consists of an enclosure with power supply, a memory controller and one to sixteen memory modules. A 36 bit system would contain two memory controllers.

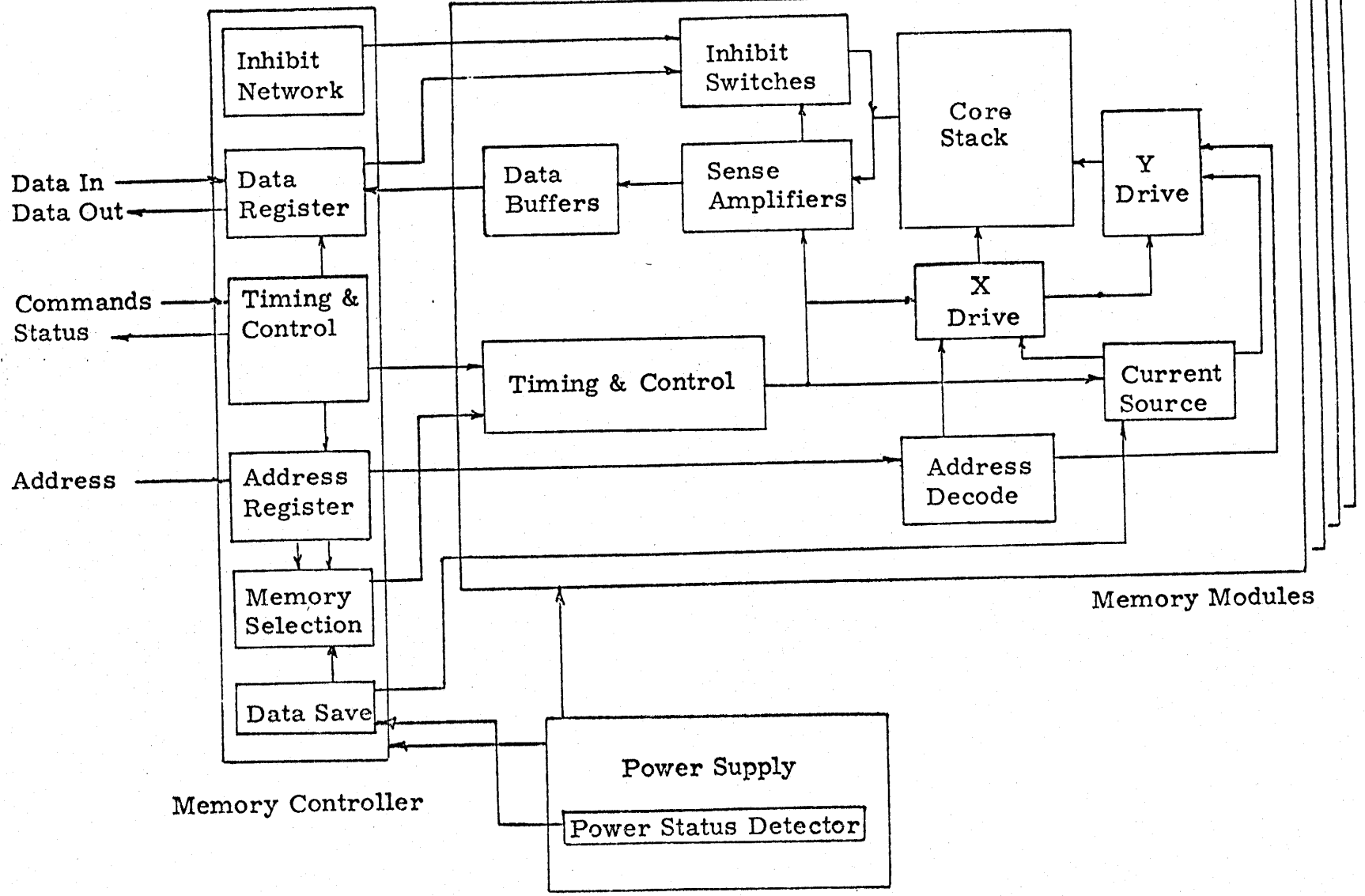
The memory system may be easily field expanded to 131K 18 bit words or 65K 36 bit words by the addition of memory modules. No additional interfacing or adjustments are required.

The memory module contains up to 8192 words with up to 18 bits per word. The core stack with the associated drive, sense and data buffering circuitry, is contained on a single 11 1/2 X 16 inch printed circuit card.

The memory controller provides the control functions, registers and inhibit networks for system users who do not wish to incorporate these functions within their own systems. Up to sixteen memory modules mayshare one controller.

Large memory systems may be obtained by the paralled operation of these modular ECOM® F components. For example, the 36 bit enclosure described in Section II is in essence two independent 18 bit memories of up to 65K words each operating in parallel in the same enclosure. Details of the modular components, their interface and theory of operation, are included as separate sections of this manual.

1.2 SYSTEM BLOCK DIAGRAM



ECOM® F MEMORY SYSTEM

SECTION II

ENCLOSURE

SECTION II

ENCLOSURE

2.1 DESCRIPTION

2.1.1 18 Bit word Length.

The ECOM® F memory enclosure is designed to accept up to sixteen memory modules, one memory controller, and a model PS-16-131 power supply. A complete memory system of up to 131,072 18 bit words can be contained in a 12 1/4 inch high standard RETMA rackmount enclosure.

Memory modules and controllers are inserted from the rear of the enclosure, thereby providing full access to all internal system connections by removing the "see through" front panel.

Figure 1 is an outline drawing of the enclosure showing the relative location of all components. Note that the memory controller is in position A. All remaining positions are reserved for memory modules. These positions are connected to the memory controller such that the memory module in position B will be selected by the first 8192 addresses. The memory module in position C will be selected by addresses between 8192 and 16383, etc.

2.1.2 36 Bit Word Length.

The ECOM® F memory enclosure is designed to accept up to sixteen memory modules, two memory controllers, and a model PS-16-131 power supply. A complete memory system of up to 65,536 36 bit words can be contained in a 12 1/4 inch high standard RETMA rackmount enclosure.

Figure 2 is an outline drawing of the enclosure showing the relative location of all components. Note that the memory controllers are in positions A and V. All remaining positions are reserved for memory modules. These positions are connected to the memory controllers such that the memory modules in positions B and U will be selected by the first 8192 addresses. The memory modules in positions C and T will be selected by addresses between 8192 and 16383, etc.

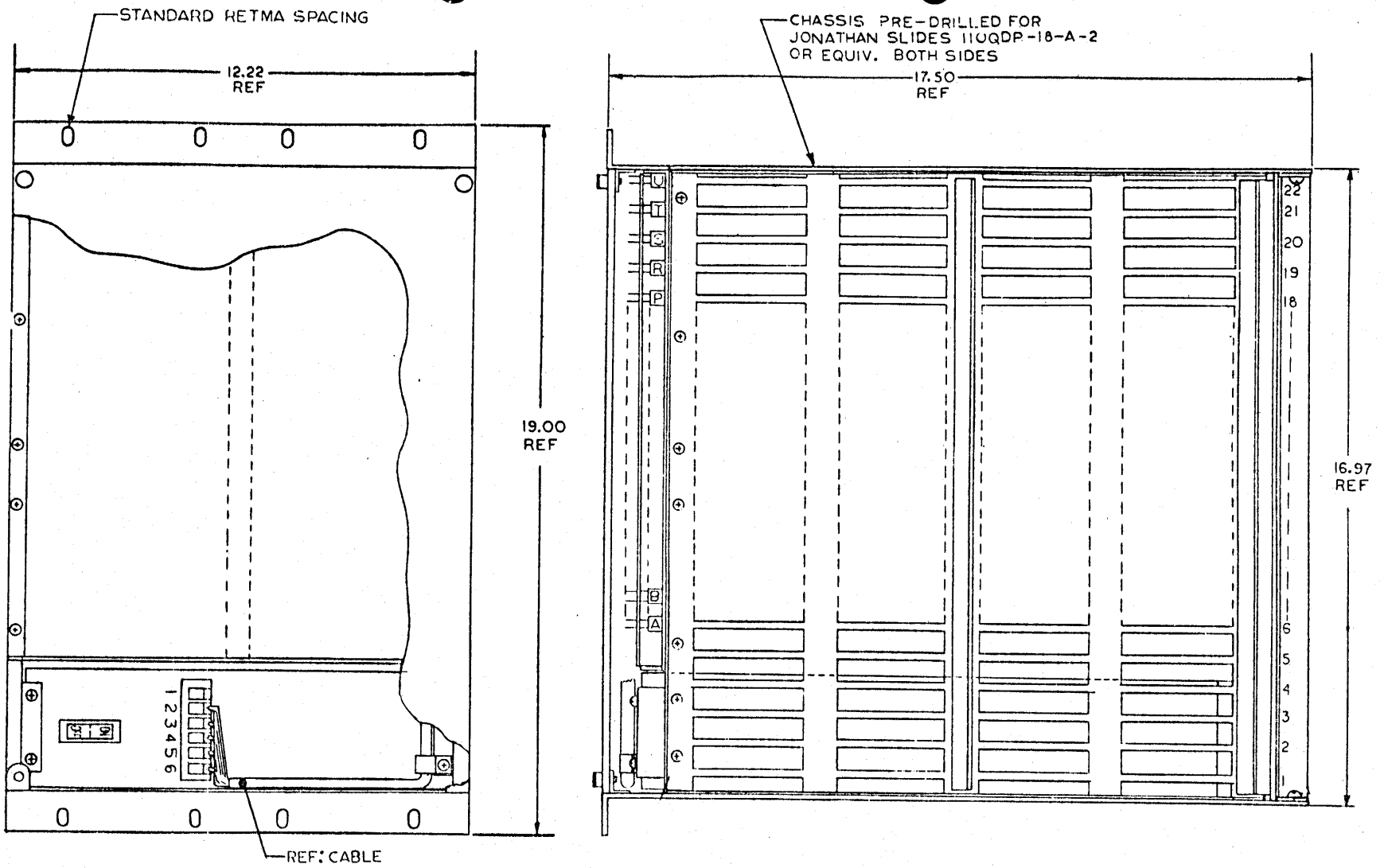


Figure 1

Note: 1. Ref P/L100984

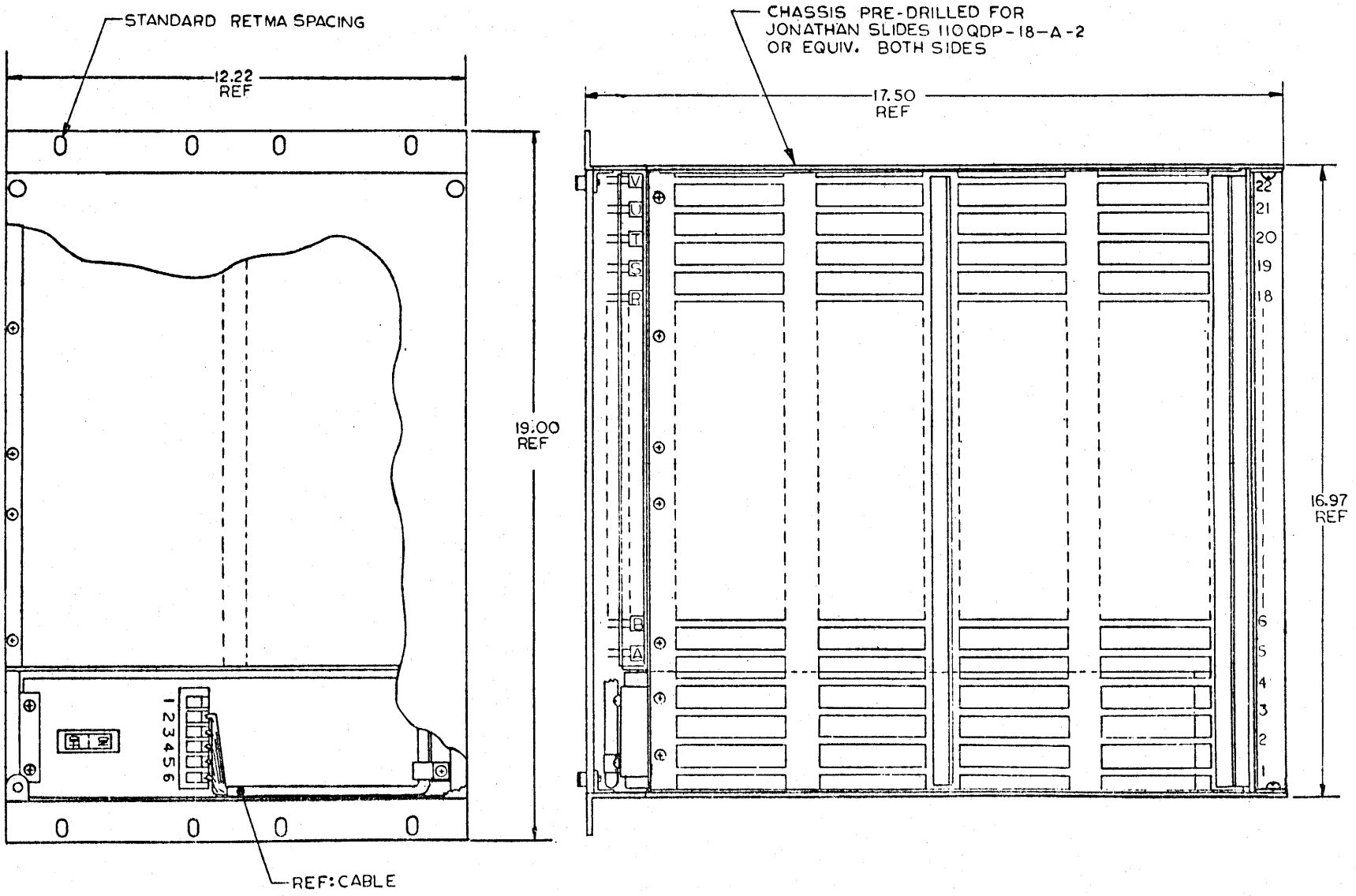


Figure 2

Note: 1. Ref P/L100984

RC 4005 LOGIC DIAGRAMS

~~CPU402, CPU404, CPU408~~ CPU 4&5

(MPC, STC, ITR, LCI, HCI)

Microprogram Controller (MPC)		Dwg. No.
MPC001	PRIMARY CLOCK PULSE GENERATOR	V10238
002	MAR(0) MICRO ADDRESS REGISTER	V10239
003	MAR(1) MICRO ADDRESS REGISTER	V10240
004	MAR(2) MICRO ADDRESS REGISTER	V10241
005	MAR(3) MICRO ADDRESS REGISTER	V10242
006	MAR(4) MICRO ADDRESS REGISTER	V10243
007	MAR(5) MICRO ADDRESS REGISTER	V10244
008	MAR(6) MICRO ADDRESS REGISTER	V10245
009	MAR(7) MICRO ADDRESS REGISTER	V10246
010	MAR(8) MICRO ADDRESS REGISTER	V10247
011	MAR(9) MICRO ADDRESS REGISTER	V10248
012	MC(1:10)	V10249
013	MC(11:20)	V10250
014	MC(21:30)	V10251
015	MC(31:40)	V10252
016	MC(41:50)	V10253
017	MC(51:60)	V10254
018	MC(61:70)	V10255
019	JS(71:80)	V10256
020	JS(81:90)	V10257
021	JS(91:100)	V10258
022	PARITY LOGIC	V10259
023	PARITY LOGIC	V10260
024	PARITY LOGIC	V10261
025	PARITY LOGIC	V10262
026	CLOCK PULSES	V10263
027	MAR Control	V10264
028	MANUAL MODE	V10265
029	NORMAL MODE AND RUNNING MODE	V10266
030	START STOP LOGIC	V10267

RCSL: ~~54-VB659-December 1969/A~~ 1972/308

Microprogram Controller (MPC)		Dwg. No.
MPC031	MPS PARITY CONTROL	V10268
032	CORE STORE PARITY CONTROL	V10269
033	OPERATOR MODE AND CONDITION RESET	V10270
034	START AND AUTOLOAD CONDITIONS	V10271
035	ARU DISPLAY CONTROL	V10272
036	POWER SUPPLY SUPERVISION	V10481
037	LAMP CONTROL	V10273
038	DISPLAY	V10274
050	+5 VOLT, 0 VOLT, AND CHASSIS CONNECTIONS	V11391

Store Controller (STC)		
STC001	PRIORITY SYSTEM	V10567
002	TIME BASE COUNTERS	V10568
003	BUFFER SECTION	V13516 ~~V10569~~
004	ADDRESS CONTROL	V10570 V13517
005	CORE STORE 1 CONTROL SIGNALS	~~V11396~~ V13518
006	READ AND WRITE CONTROL	~~V10572~~
007	READ AND WRITE CONTROL	V10573
008	ADDRESS GENERATION	V10574
009	ADDRESS GENERATION	V10575 V13519
010	STBUS(0:5)	~~V10576~~ V13520
011	STBUS(6:11)	~~V10577~~ V13521
012	STBUS(12:17)	~~V10578~~ V13522
013	STBUS(18:23)	~~V10579~~ ~~V13523~~
014	STBUS(24:27)	~~V10580~~
015	PARITY CHECK AND GENERATION	V10581
016	ADDRESS TRANSMISSION FROM CPU TO CORE STORE 1	V13511 ~~V10582~~
017	DATA TRANSMISSION FROM CPU TO CORE STORE 1	V13512 ~~V10583~~
018	DATA TRANSMISSION FROM CPU TO CORE STORE 1	V13513 ~~V10584~~

~~VD659~~

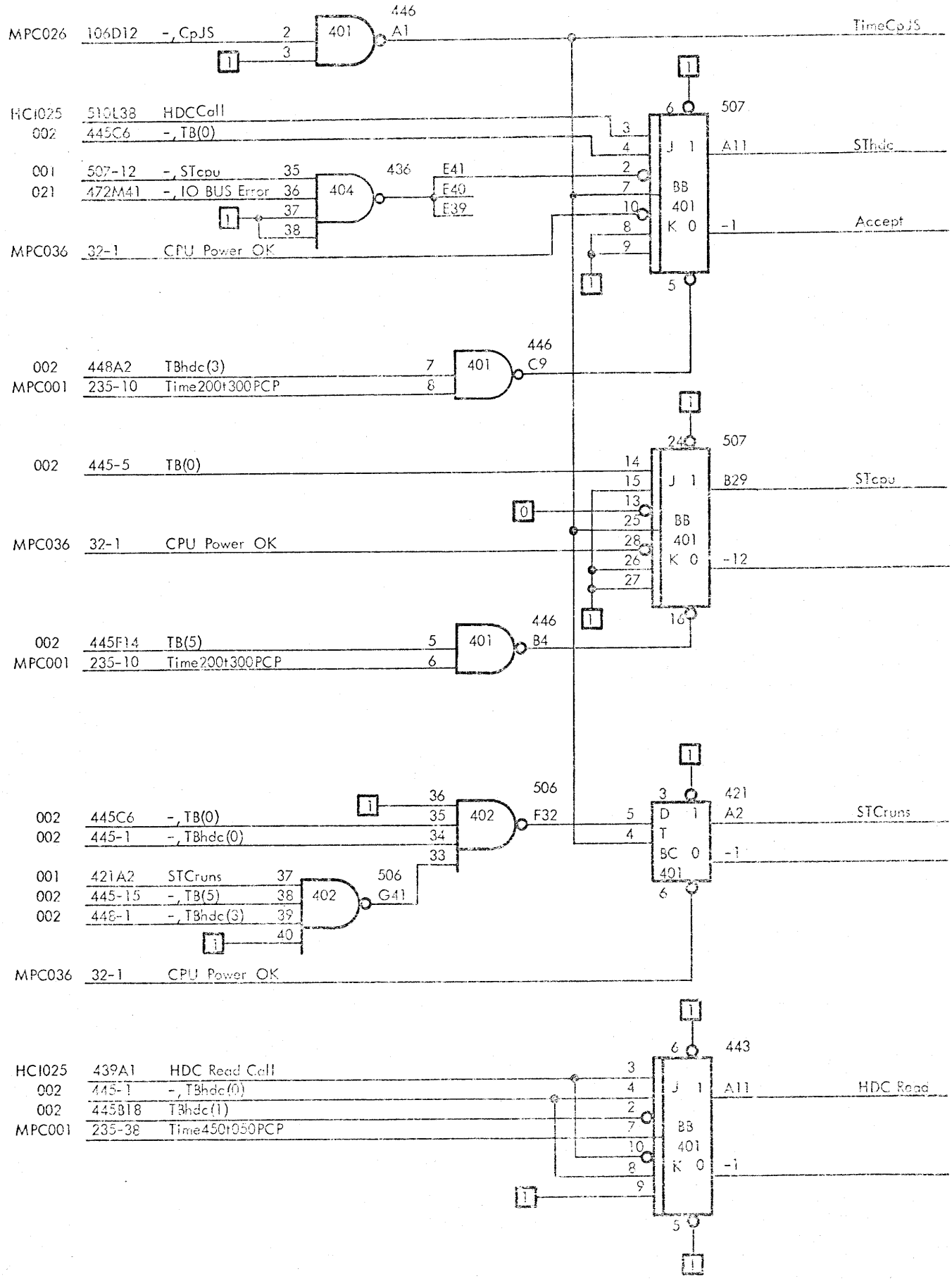
Store Controller (STC)		Dwg. No.
STC019	DATA TRANSMISSION FROM CORE STORE 1 TO CPU	V13514 ~~V10585~~
020	DATA TRANSMISSION FROM CORE STORE 1 TO CPU	V13515 ~~V10586~~
021	POWER SUPERVISION	V13521 ~~V10894~~
022	~~TERMINATION OF UNUSED WIRES~~ IN CORE STORE CABLES	✓13592 ~~V13525~~ ~~V11397~~
023	TERMINATION OF UNUSED WIRES IN CORE STORE CABLES	~~V13524~~ ~~V13592~~ V13526

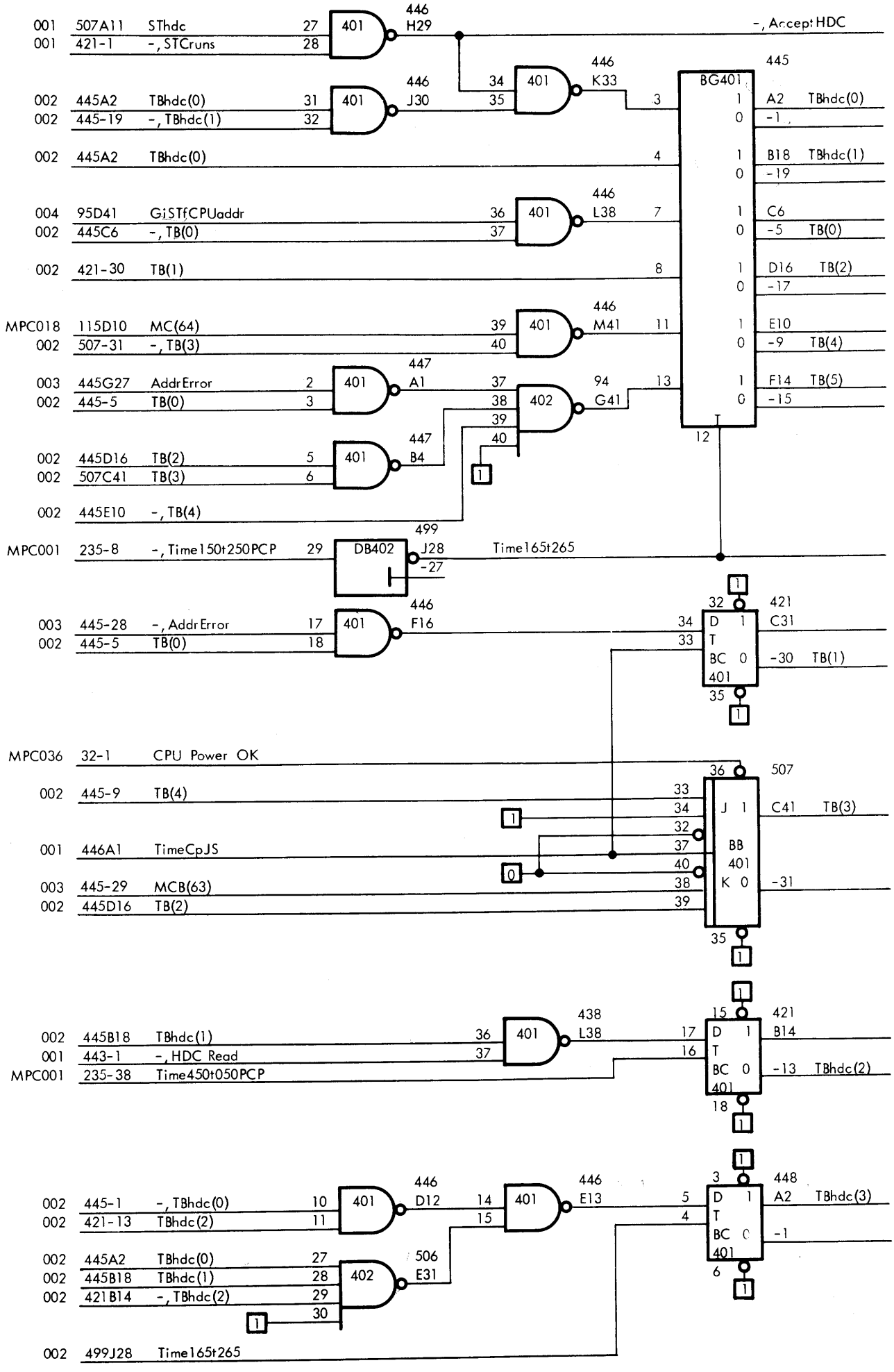
Interrupt Unit (ITR)		
ITR001	IR(0:3), IM(0:3), RM(0:3)	V10642
002	IR(4:7), IM(4:7), PR(4:7)	V10643
003	IR(8:11), IM(8:11), PR(8:11)	V10644
004	IR(12:15), IM(12:15), PR(12:15)	V10645
005	IR(16:19), IM(16:19), PR(16:19)	V10646
006	IR(20:23), IM(20:23), PR(20:23)	V10647
007	ITR REQUEST, GrSl(0:5)	V10648
008	ITRno(18:21), NOinGr(0:3)	V10649
009	ITRno(22)	V10650
010	CONTROL AND TIMING SIGNALS	V10651
011	INTERRUPT(3:11)	V11084
012	INTERRUPT(12:23)	V11085
013	CONNECTIONS BETWEEN INPUT CONNECTOR AND PLUG BOARD	V10654
014	INTERRUPTS FROM BASIC I/O UNITS	V11086

Low-Speed Data Channel Interface (LCI)		Dwg. No.
LCI001	SB(0:11)	V10601
002	SB(12:23)	V10602
003	LDC CONTROL SIGNALS	V10603
004	I/O CONNECTED AND I/O READY	V10604
008	DATA(0:7)	V10608
009	I/O DATA(8:15)	V10609
010	I/O DATA(16:23)	V10610
011	RPT CONTROL SIGNALS	V10611
012	RPT CONTROL SIGNALS, SB(16:23)	V10612
020	LDC CONTROL SIGNALS - BUS CABLE 1061	V11072
021	I/O BUS(0:5) - BUS CABLE 1061	V11073
022	I/O BUS(6:9) - BUS CABLE 1061	V11074
023	I/O BUS(10:15) - BUS CABLE 1061	V11075
024	I/O BUS(16:17) - BUS CABLE 1061	V11076
025	I/O BUS(18:23) - BUS CABLE 1061	V11077
026	LDC CONTROL SIGNALS - BUS CABLE 1062	V11078
027	I/O BUS(0:5) - BUS CABLE 1062	V11079
028	I/O BUS(6:9) - BUS CABLE 1062	V11080
029	I/O BUS(10:15) - BUS CABLE 1062	V11081
030	I/O BUS(16:17) - BUS CABLE 1062	V11082
031	I/O BUS(18:23) - BUS CABLE 1062	V11083

High-Speed Data Channel Interface (HCI)		
HCI001	CYS Request(0:7)	V10895
002	CYS Request(8:15)	V10896
003	RQ REGISTER	V10897
004	PRIORITY DECODING	V10898
005	PRIORITY DECODING	V10899
006	SelReqBf(0:15)	V10900
007	HDC GiAddr(0:11)	V10901
008	HDC GiData(0:11)	V10902
009	HDC GiAddr(12:15), HDC GiData(12:15)	V10903
010	HDC BUSout(0:9)	V10904

High-Speed Data Channel Interface (HCI)		Dwg. No.
HCI011	HDC BUSout(10:23)	V10905
012	HDC BUSin(0:11)	V10906
013	HDC BUSin(12:23)	V10907
014	BUFFER REGISTER FOR HDC ADDRESS AND INPUT DATA	V10908
015	BUFFER REGISTER FOR HDC ADDRESS AND INPUT DATA	V10909
016	TERMINATIONS FOR INPUT-OUTPUT CABLES	V10910
017	TERMINATIONS FOR INPUT-OUTPUT CABLES	V10911
018	TERMINATIONS FOR INPUT-OUTPUT CABLES	V10912
019	TERMINATIONS FOR INPUT-OUTPUT CABLES	V10913
020	TERMINATIONS FOR INPUT-OUTPUT CABLES	V10914
021	TERMINATIONS FOR INPUT-OUTPUT CABLES	V10915
022	HCI CONTROL	V10916
023	HCI CONTROL	V10917
024	HCI CONTROL	V10918
025	HCI CONTROL	V10919
026	HCI CONTROL	V10920
027	3<HDCBF WORD LIMIT ~~32K CORE STORE MODULE~~	V13527 ~~V11153~~


MPC026 106D12 -,CpJS
446 A1
401
TimeCpJS
HCI025 510L38 HDCCall
002 445C6 -,TB(0)
001 507-12 -,STcpu
021 472M41 -,IO BUS Error
436 E41 E40 E39
404
MPC036 32-1 CPU Power OK
507 A11 STHdc
J 1 BB 401 K 0
-1 Accept
002 448A2 TBhdc(3)
MPC001 235-10 Time200t300PCP
446 C9
401
507 B29 STcpu
002 445-5 TB(0)
MPC036 32-1 CPU Power OK
-12
002 445F14 TB(5)
MPC001 235-10 Time200t300PCP
446 B4
401
002 445C6 -,TB(0)
002 445-1 -,TBhdc(0)
001 421A2 STCruns
002 445-15 -,TB(5)
002 448-1 -,TBhdc(3)
506 G41
402
506 F32
421 A2 STCruns
D 1 T BC 0 401
-1
MPC036 32-1 CPU Power OK
HCI025 439A1 HDC Read Call
002 445-1 -,TBhdc(0)
002 445B18 TBhdc(1)
MPC001 235-38 Time450t050PCP
443 A11 HDC Read
-1



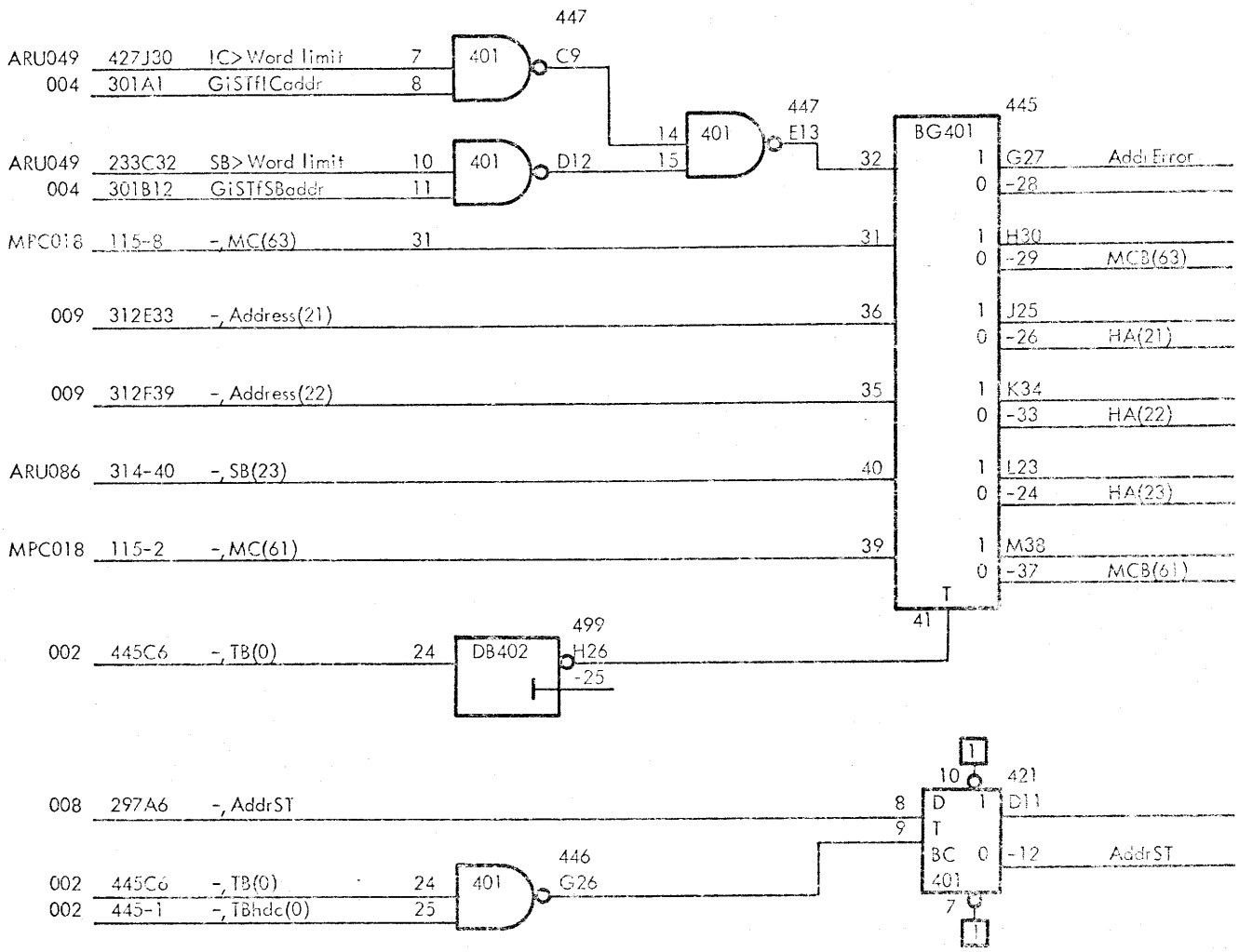
RC4000

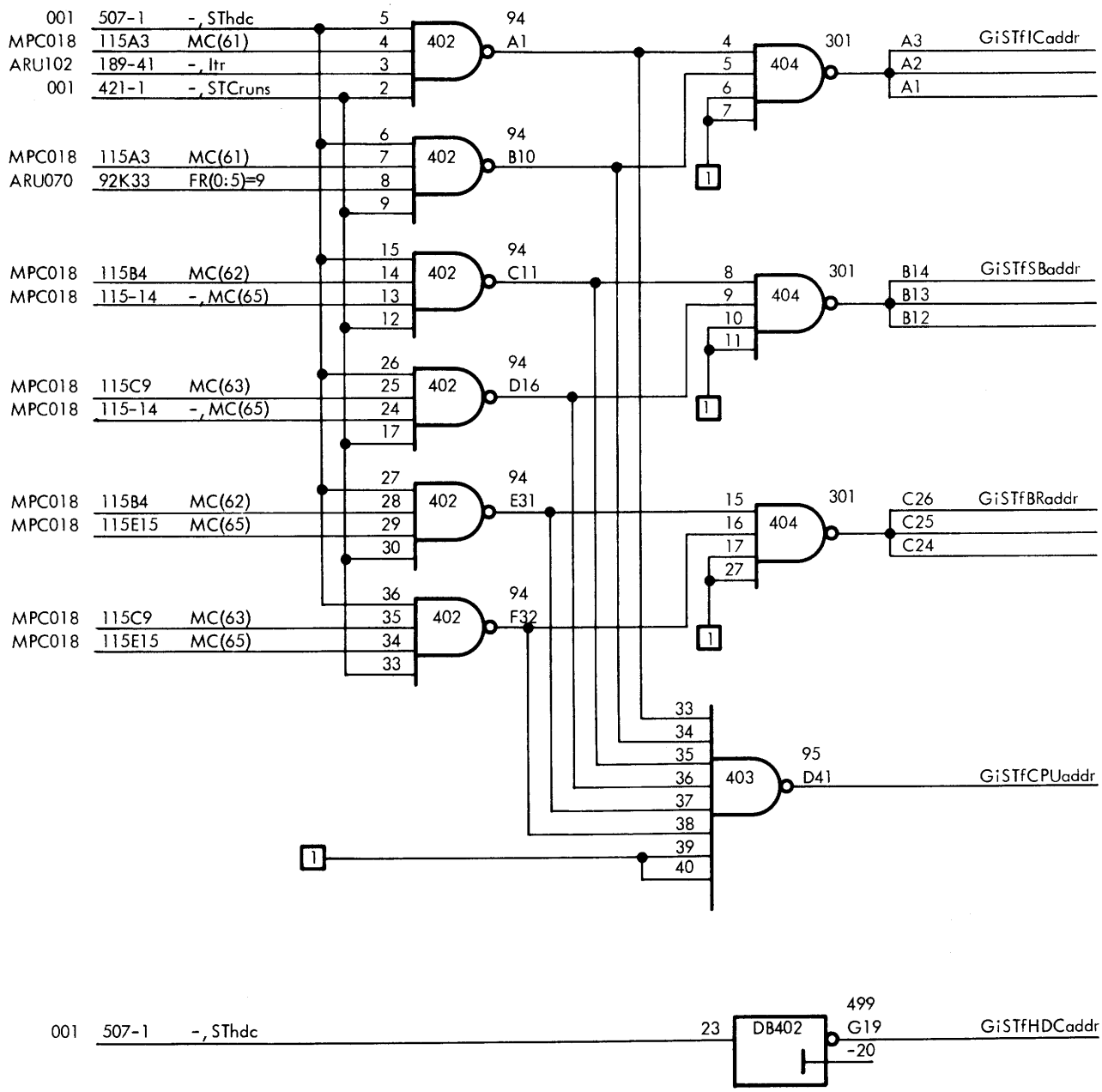
TIME BASE COUNTERS

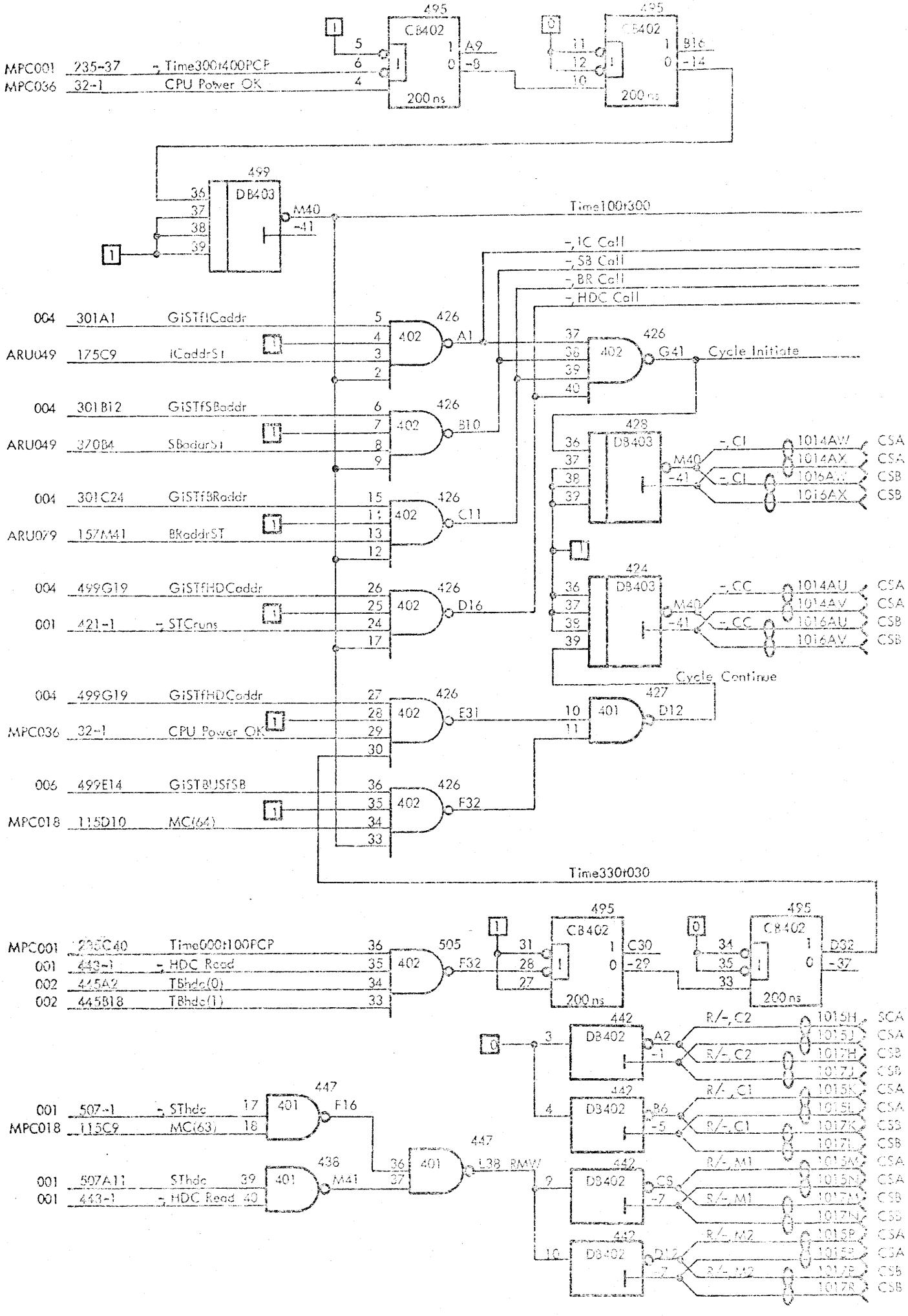
STC002

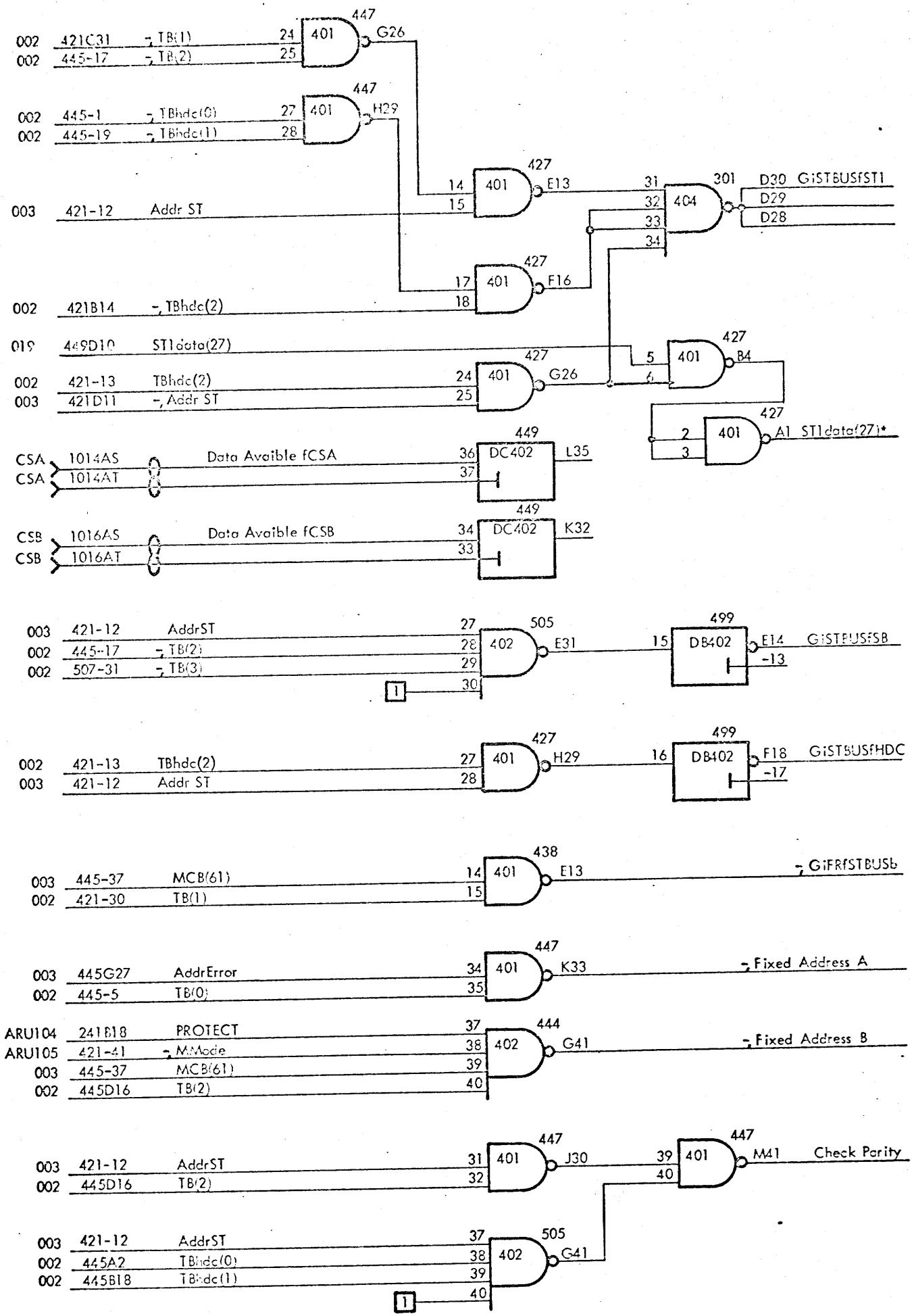
V10568

Logic Diagram


447
ARU049 004
427J30 301A1
IC>Word limit
GiSTfIC addr
7 8
401
C9
447
E13
14 15
401
ARU049 004
233C32 301B12
SB>Word limit
GiSTfSBaddr
10 11
401
D12
445
BG401
32
1 G27 Addr Error
0 -28
MPC018 115-8 -, MC(63) 31
31
1 H30
0 -29 MCB(63)
009 312E33 -, Address(21)
36
1 J25
0 -26 HA(21)
009 312F39 -, Address(22)
35
1 K34
0 -33 HA(22)
ARU086 314-40 -, SB(23)
40
1 L23
0 -24 HA(23)
MPC018 115-2 -, MC(61)
39
1 M38
0 -37 MCB(61)
T
41
499
002 445C6 -, TB(0) 24
DB402
H26
-25
1
10
421
008 297A6 -, AddrST
8
9
D 1 D11
T
BC 0 -12 AddrST
401
7
1
446
002 445C6 -, TB(0) 24
002 445-1 -, TBhdc(0) 25
401
G26

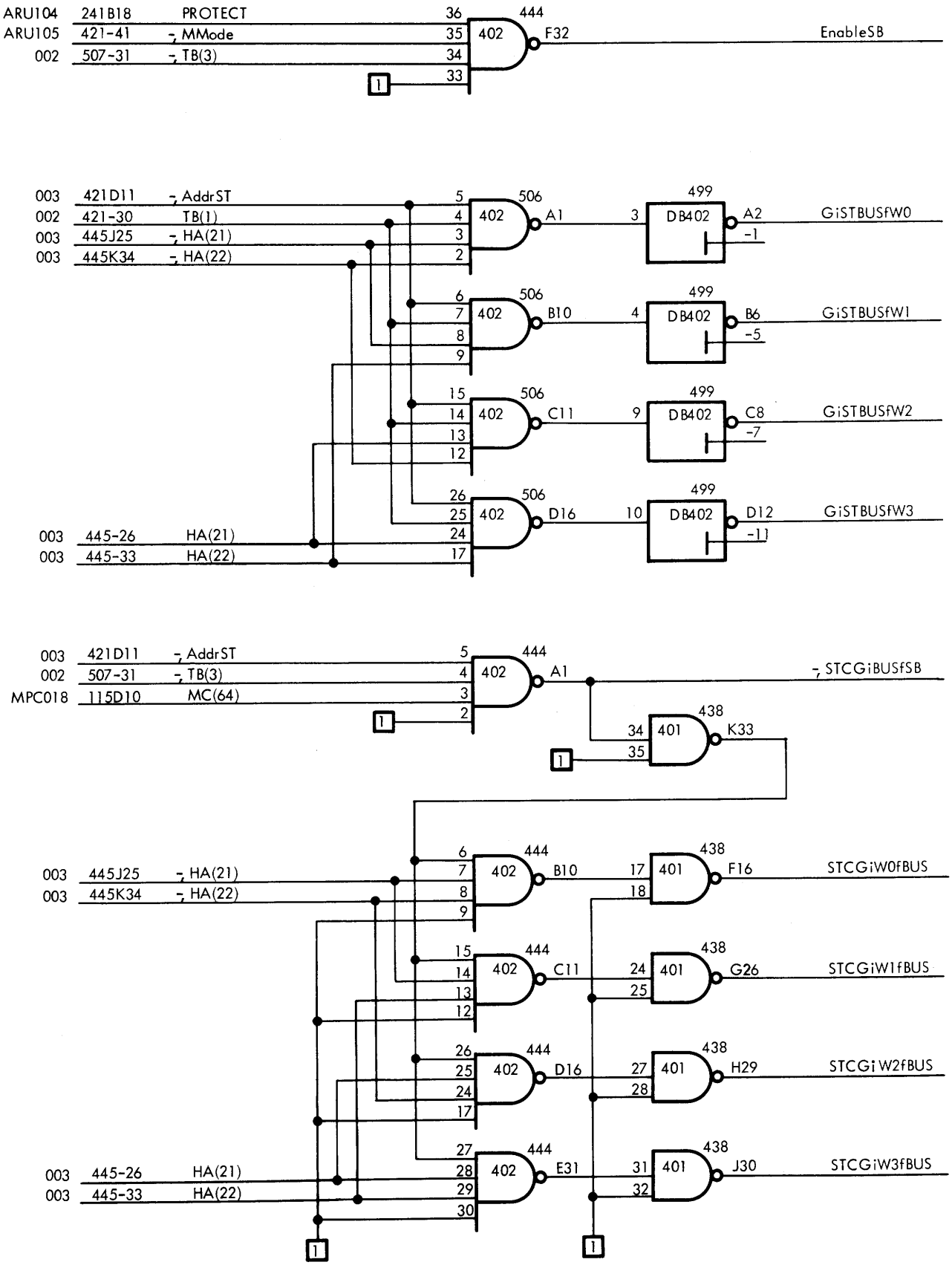

001 507-1 -,SThdc
MPC018 115A3 MC(61)
ARU102 189-41 -,Itr
001 421-1 -,STCruns
MPC018 115A3 MC(61)
ARU070 92K33 FR(0:5)=9
MPC018 115B4 MC(62)
MPC018 115-14 -,MC(65)
MPC018 115C9 MC(63)
MPC018 115-14 -,MC(65)
MPC018 115B4 MC(62)
MPC018 115E15 MC(65)
MPC018 115C9 MC(63)
MPC018 115E15 MC(65)
402
A1
B10
C11
D16
E31
F32
404
A3
A2
A1
GiSTfICaddr
B14
B13
B12
GiSTfSBaddr
C26
C25
C24
GiSTfBRaddr
403
D41
GiSTfCPUaddr
001 507-1 -,SThdc
DB402
G19
-20
GiSTfHDCaddr

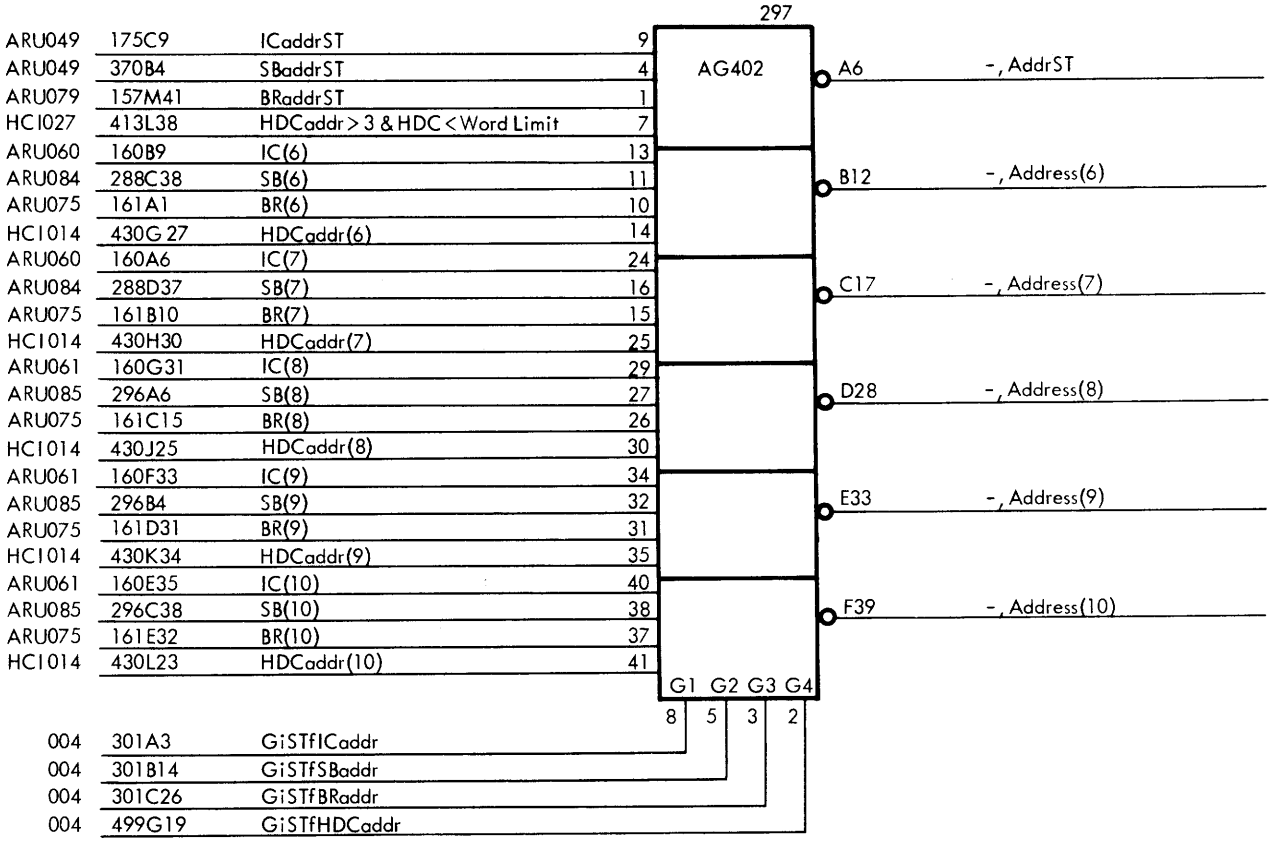

MPC001 235-37 -, Time300t400PCP
MPC036 32-1 CPU Power OK
CB402
200 ns
A9
-8
B16
-14
DB403
M40
-41
Time100t300
-, IC Call
-, SB Call
-, BR Call
-, HDC Call
004 301A1 GiSTfICaddr
ARU049 175C9 ICaddrST
004 301B12 GiSTfSBaddr
ARU049 370B4 SBaddrST
004 301C24 GiSTfBRaddr
ARU079 157M41 BRaddrST
004 499G19 GiSTfHDCaddr
001 421-1 -, STCruns
004 499G19 GiSTfHDCaddr
MPC036 32-1 CPU Power OK
006 499E14 GiSTBUSfSB
MPC018 115D10 MC(64)
402
426
A1
B10
C11
D16
E31
F32
401
427
D12
Cycle Initiate
Cycle Continue
428
424
-, CI
-, CC
1014AW
1014AX
1016AW
1016AX
1014AU
1014AV
1016AU
1016AV
CSA
CSB
Time330t030
MPC001 235C40 Time000t100FCP
001 443-1 -, HDC Read
002 445A2 TBhdc(0)
002 445B18 TBhdc(1)
505
C30
-22
D32
-37
442
A2
B6
C8
D12
R/-, C2
R/-, C1
R/-, M1
R/-, M2
1015H
1015J
1017H
1017J
1015K
1015L
1017K
1017L
1015M
1015N
1017M
1017N
1015P
1015R
1017P
1017R
SCA
447
F16
L38 RMW
436
M41
001 507-1 -, STbdc
MPC018 115C9 MC(63)
001 507A11 STbdc
001 443-1 -, HDC Read

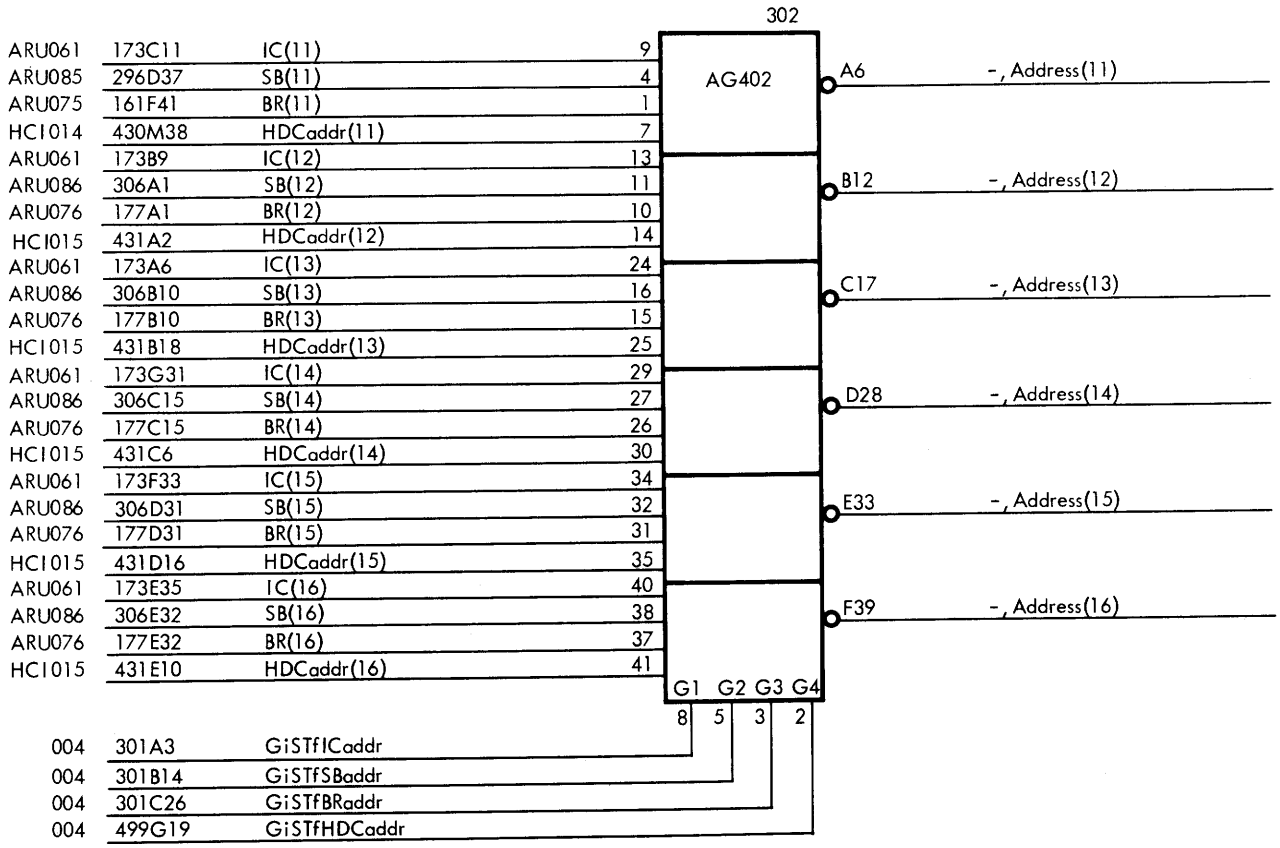


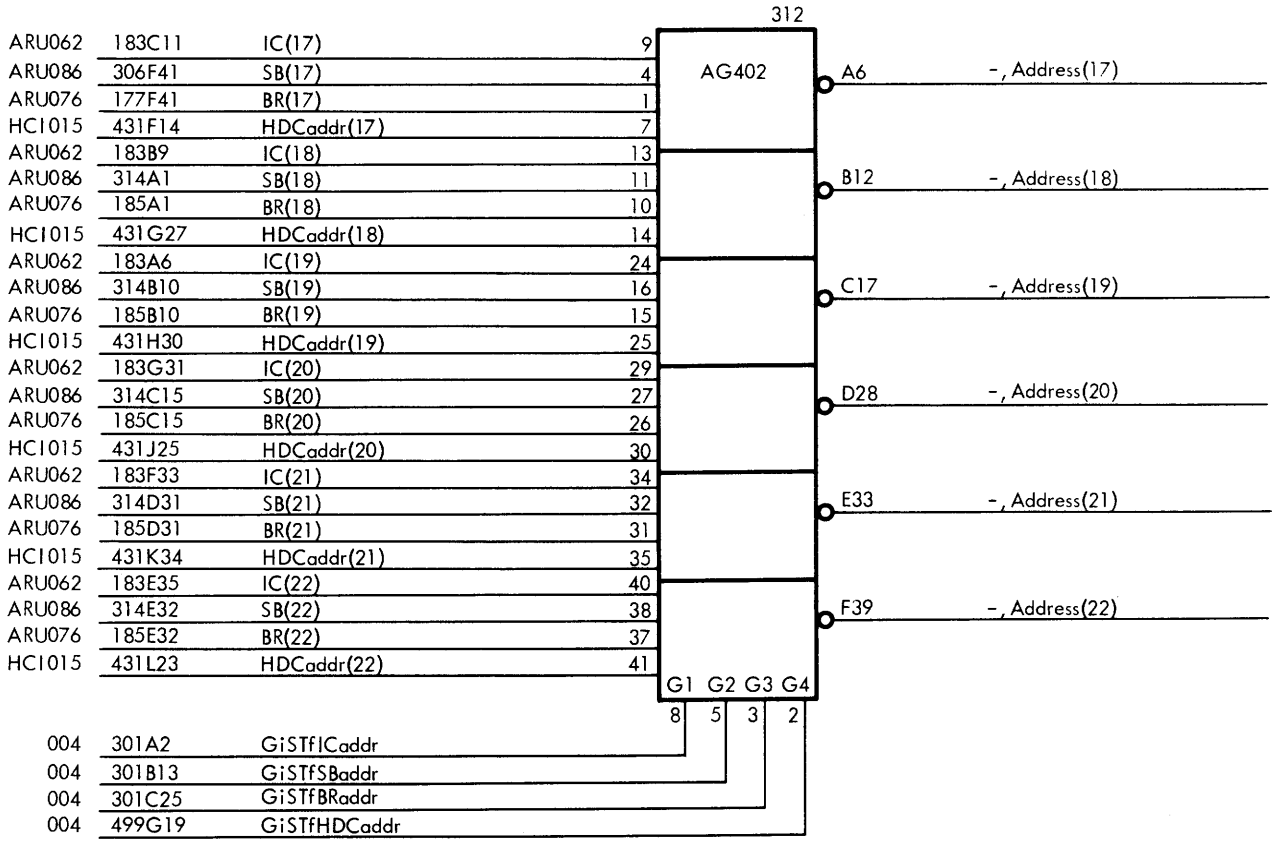
RC4000 READ AND WRITE CONTROL STC036

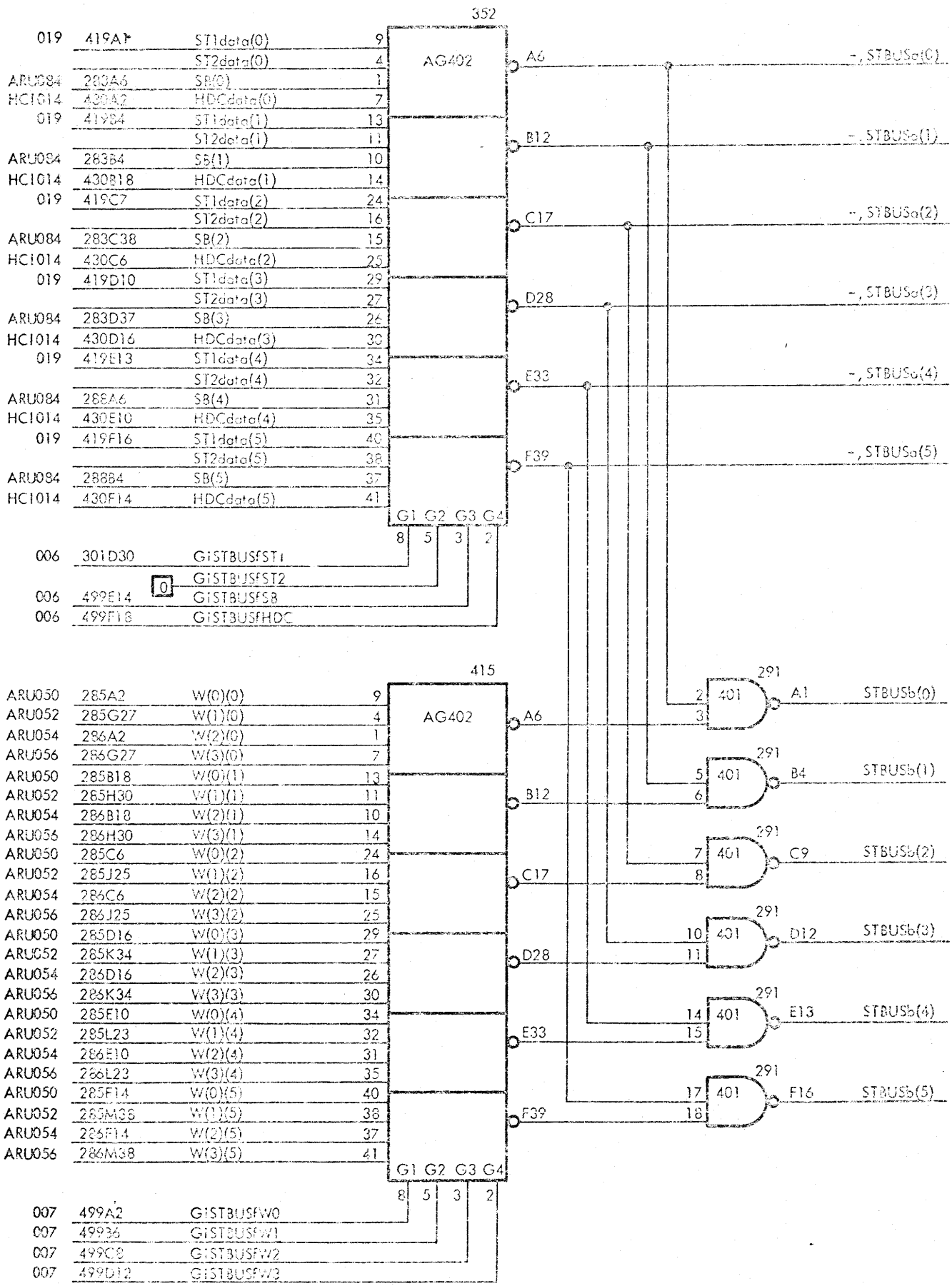
V13590 Logic Diagram

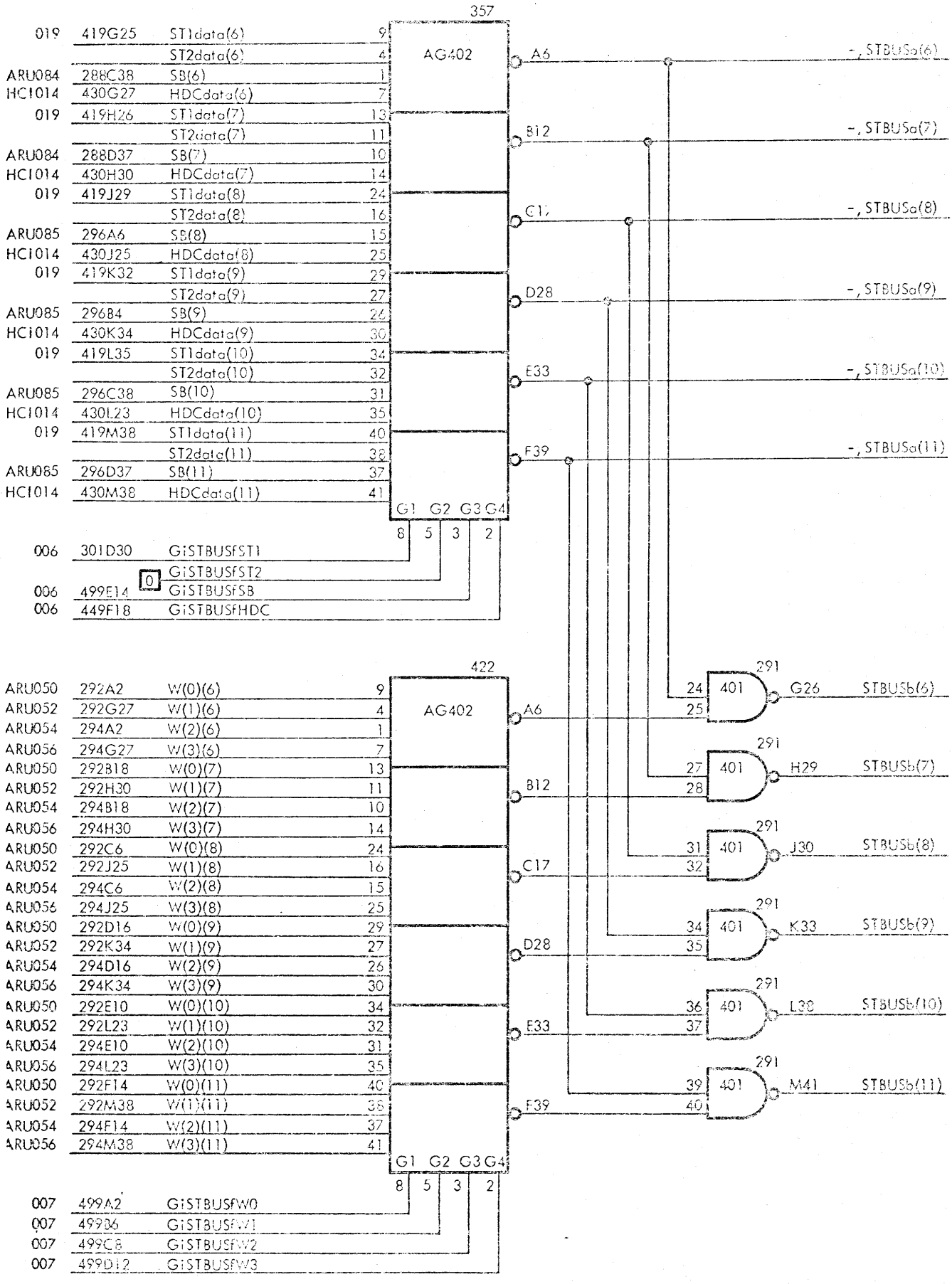

ARU104 241B18 PROTECT
ARU105 421-41 ⁻, MMode
002 507-31 ⁻, TB(3)
36
35
34
33
444
402
F32
EnableSB
003 421D11 ⁻, AddrST
002 421-30 TB(1)
003 445J25 ⁻, HA(21)
003 445K34 ⁻, HA(22)
003 445-26 HA(21)
003 445-33 HA(22)
506
499
DB402
A1
A2
-1
B10
B6
-5
C11
C8
-7
D16
D12
-11
GiSTBUSfW0
GiSTBUSfW1
GiSTBUSfW2
GiSTBUSfW3
003 421D11 ⁻, AddrST
002 507-31 ⁻, TB(3)
MPC018 115D10 MC(64)
⁻, STCGiBUSfSB
438
401
K33
003 445J25 ⁻, HA(21)
003 445K34 ⁻, HA(22)
003 445-26 HA(21)
003 445-33 HA(22)
B10
C11
D16
E31
F16
G26
H29
J30
STCGiW0fBUS
STCGiW1fBUS
STCGiW2fBUS
STCGiW3fBUS

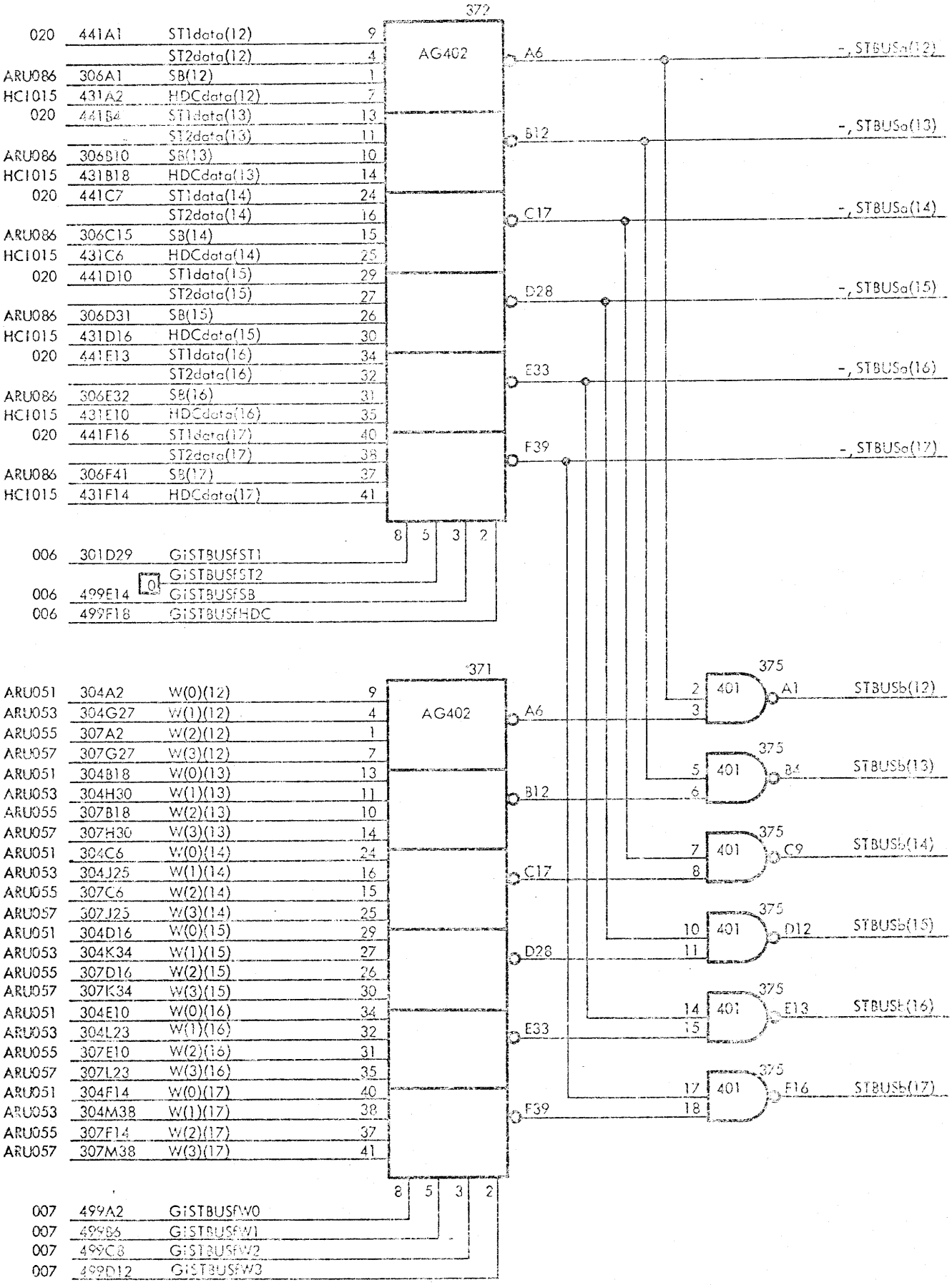

297
ARU049 175C9 ICaddrST 9
ARU049 370B4 SBaddrST 4
ARU079 157M41 BRaddrST 1
HCI027 413L38 HDCaddr > 3 & HDC < Word Limit 7
ARU060 160B9 IC(6) 13
ARU084 288C38 SB(6) 11
ARU075 161A1 BR(6) 10
HCI014 430G 27 HDCaddr(6) 14
ARU060 160A6 IC(7) 24
ARU084 288D37 SB(7) 16
ARU075 161B10 BR(7) 15
HCI014 430H30 HDCaddr(7) 25
ARU061 160G31 IC(8) 29
ARU085 296A6 SB(8) 27
ARU075 161C15 BR(8) 26
HCI014 430J25 HDCaddr(8) 30
ARU061 160F33 IC(9) 34
ARU085 296B4 SB(9) 32
ARU075 161D31 BR(9) 31
HCI014 430K34 HDCaddr(9) 35
ARU061 160E35 IC(10) 40
ARU085 296C38 SB(10) 38
ARU075 161E32 BR(10) 37
HCI014 430L23 HDCaddr(10) 41
AG402
A6 -, AddrST
B12 -, Address(6)
C17 -, Address(7)
D28 -, Address(8)
E33 -, Address(9)
F39 -, Address(10)
G1 G2 G3 G4
8 5 3 2
004 301A3 GiSTfICaddr
004 301B14 GiSTfSBaddr
004 301C26 GiSTfBRaddr
004 499G19 GiSTfHDCaddr


302
ARU061 173C11 IC(11) 9
ARU085 296D37 SB(11) 4
ARU075 161F41 BR(11) 1
HCI014 430M38 HDCaddr(11) 7
ARU061 173B9 IC(12) 13
ARU086 306A1 SB(12) 11
ARU076 177A1 BR(12) 10
HCI015 431A2 HDCaddr(12) 14
ARU061 173A6 IC(13) 24
ARU086 306B10 SB(13) 16
ARU076 177B10 BR(13) 15
HCI015 431B18 HDCaddr(13) 25
ARU061 173G31 IC(14) 29
ARU086 306C15 SB(14) 27
ARU076 177C15 BR(14) 26
HCI015 431C6 HDCaddr(14) 30
ARU061 173F33 IC(15) 34
ARU086 306D31 SB(15) 32
ARU076 177D31 BR(15) 31
HCI015 431D16 HDCaddr(15) 35
ARU061 173E35 IC(16) 40
ARU086 306E32 SB(16) 38
ARU076 177E32 BR(16) 37
HCI015 431E10 HDCaddr(16) 41
AG402
A6 -, Address(11)
B12 -, Address(12)
C17 -, Address(13)
D28 -, Address(14)
E33 -, Address(15)
F39 -, Address(16)
G1 G2 G3 G4
8 5 3 2
004 301A3 GiSTfICaddr
004 301B14 GiSTfSBaddr
004 301C26 GiSTfBRaddr
004 499G19 GiSTfHDCaddr


312
ARU062 183C11 IC(17) 9
ARU086 306F41 SB(17) 4
ARU076 177F41 BR(17) 1
HC1015 431F14 HDCaddr(17) 7
ARU062 183B9 IC(18) 13
ARU086 314A1 SB(18) 11
ARU076 185A1 BR(18) 10
HC1015 431G27 HDCaddr(18) 14
ARU062 183A6 IC(19) 24
ARU086 314B10 SB(19) 16
ARU076 185B10 BR(19) 15
HC1015 431H30 HDCaddr(19) 25
ARU062 183G31 IC(20) 29
ARU086 314C15 SB(20) 27
ARU076 185C15 BR(20) 26
HC1015 431J25 HDCaddr(20) 30
ARU062 183F33 IC(21) 34
ARU086 314D31 SB(21) 32
ARU076 185D31 BR(21) 31
HC1015 431K34 HDCaddr(21) 35
ARU062 183E35 IC(22) 40
ARU086 314E32 SB(22) 38
ARU076 185E32 BR(22) 37
HC1015 431L23 HDCaddr(22) 41
AG402
A6 -, Address(17)
B12 -, Address(18)
C17 -, Address(19)
D28 -, Address(20)
E33 -, Address(21)
F39 -, Address(22)
G1 G2 G3 G4
8 5 3 2
004 301A2 GiSTfICaddr
004 301B13 GiSTfSBaddr
004 301C25 GiSTfBRaddr
004 499G19 GiSTfHDCaddr


352
019 419A1 ST1data(0) 9
ST2data(0) 4
ARU084 283A6 SB(0) 1
HC1014 430A2 HDCdata(0) 7
019 419B4 ST1data(1) 13
ST2data(1) 11
ARU084 283B4 SB(1) 10
HC1014 430B18 HDCdata(1) 14
019 419C7 ST1data(2) 24
ST2data(2) 16
ARU084 283C38 SB(2) 15
HC1014 430C6 HDCdata(2) 25
019 419D10 ST1data(3) 29
ST2data(3) 27
ARU084 283D37 SB(3) 26
HC1014 430D16 HDCdata(3) 30
019 419E13 ST1data(4) 34
ST2data(4) 32
ARU084 288A6 SB(4) 31
HC1014 430E10 HDCdata(4) 35
019 419F16 ST1data(5) 40
ST2data(5) 38
ARU084 28884 SB(5) 37
HC1014 430F14 HDCdata(5) 41
AG402
A6
B12
C17
D28
E33
F39
-,STBUSa(0)
-,STBUSa(1)
-,STBUSa(2)
-,STBUSa(3)
-,STBUSa(4)
-,STBUSa(5)
G1 G2 G3 G4
8 5 3 2
006 301D30 GiSTBUSfST1
0
GiSTBUSfST2
006 499E14 GiSTBUSfSB
006 499F18 GiSTBUSfHDC
415
ARU050 285A2 W(0)(0) 9
ARU052 285G27 W(1)(0) 4
ARU054 286A2 W(2)(0) 1
ARU056 286G27 W(3)(0) 7
ARU050 285B18 W(0)(1) 13
ARU052 285H30 W(1)(1) 11
ARU054 286B18 W(2)(1) 10
ARU056 286H30 W(3)(1) 14
ARU050 285C6 W(0)(2) 24
ARU052 285J25 W(1)(2) 16
ARU054 286C6 W(2)(2) 15
ARU056 286J25 W(3)(2) 25
ARU050 285D16 W(0)(3) 29
ARU052 285K34 W(1)(3) 27
ARU054 286D16 W(2)(3) 26
ARU056 286K34 W(3)(3) 30
ARU050 285E10 W(0)(4) 34
ARU052 285L23 W(1)(4) 32
ARU054 286E10 W(2)(4) 31
ARU056 286L23 W(3)(4) 35
ARU050 285F14 W(0)(5) 40
ARU052 285M38 W(1)(5) 38
ARU054 286F14 W(2)(5) 37
ARU056 286M38 W(3)(5) 41
AG402
A6
B12
C17
D28
E33
F39
G1 G2 G3 G4
8 5 3 2
007 499A2 GiSTBUSfW0
007 499B6 GiSTBUSfW1
007 499C8 GiSTBUSfW2
007 499D12 GiSTBUSfW3
291
401
2 3 A1 STBUSb(0)
5 6 B4 STBUSb(1)
7 8 C9 STBUSb(2)
10 11 D12 STBUSb(3)
14 15 E13 STBUSb(4)
17 18 F16 STBUSb(5)


357
AG402
019 419G25 ST1data(6) 9
ST2data(6) 4
ARU084 288C38 SB(6) 1
HCI014 430G27 HDCdata(6) 7
019 419H26 ST1data(7) 13
ST2data(7) 11
ARU084 288D37 SB(7) 10
HCI014 430H30 HDCdata(7) 14
019 419J29 ST1data(8) 24
ST2data(8) 16
ARU085 296A6 SB(8) 15
HCI014 430J25 HDCdata(8) 25
019 419K32 ST1data(9) 29
ST2data(9) 27
ARU085 29684 SB(9) 26
HCI014 430K34 HDCdata(9) 30
019 419L35 ST1data(10) 34
ST2data(10) 32
ARU085 296C38 SB(10) 31
HCI014 430L23 HDCdata(10) 35
019 419M38 ST1data(11) 40
ST2data(11) 38
ARU085 296D37 SB(11) 37
HCI014 430M38 HDCdata(11) 41
G1 G2 G3 G4
8 5 3 2
006 301D30 GiSTBUSfST1
0 GiSTBUSfST2
006 499E14 GiSTBUSfSB
006 449F18 GiSTBUSfHDC
A6
B12
C17
D28
E33
F39
-, STBUSa(6)
-, STBUSa(7)
-, STBUSa(8)
-, STBUSa(9)
-, STBUSa(10)
-, STBUSa(11)
422
AG402
ARU050 292A2 W(0)(6) 9
ARU052 292G27 W(1)(6) 4
ARU054 294A2 W(2)(6) 1
ARU056 294G27 W(3)(6) 7
ARU050 292B18 W(0)(7) 13
ARU052 292H30 W(1)(7) 11
ARU054 294B18 W(2)(7) 10
ARU056 294H30 W(3)(7) 14
ARU050 292C6 W(0)(8) 24
ARU052 292J25 W(1)(8) 16
ARU054 294C6 W(2)(8) 15
ARU056 294J25 W(3)(8) 25
ARU050 292D16 W(0)(9) 29
ARU052 292K34 W(1)(9) 27
ARU054 294D16 W(2)(9) 26
ARU056 294K34 W(3)(9) 30
ARU050 292E10 W(0)(10) 34
ARU052 292L23 W(1)(10) 32
ARU054 294E10 W(2)(10) 31
ARU056 294L23 W(3)(10) 35
ARU050 292F14 W(0)(11) 40
ARU052 292M38 W(1)(11) 38
ARU054 294F14 W(2)(11) 37
ARU056 294M38 W(3)(11) 41
G1 G2 G3 G4
8 5 3 2
007 499A2 GiSTBUSfW0
007 499B6 GiSTBUSfW1
007 499C8 GiSTBUSfW2
007 499D12 GiSTBUSfW3
A6
B12
C17
D28
E33
F39
291
401
24 25 G26 STBUSb(6)
27 28 H29 STBUSb(7)
31 32 J30 STBUSb(8)
34 35 K33 STBUSb(9)
36 37 L38 STBUSb(10)
39 40 M41 STBUSb(11)



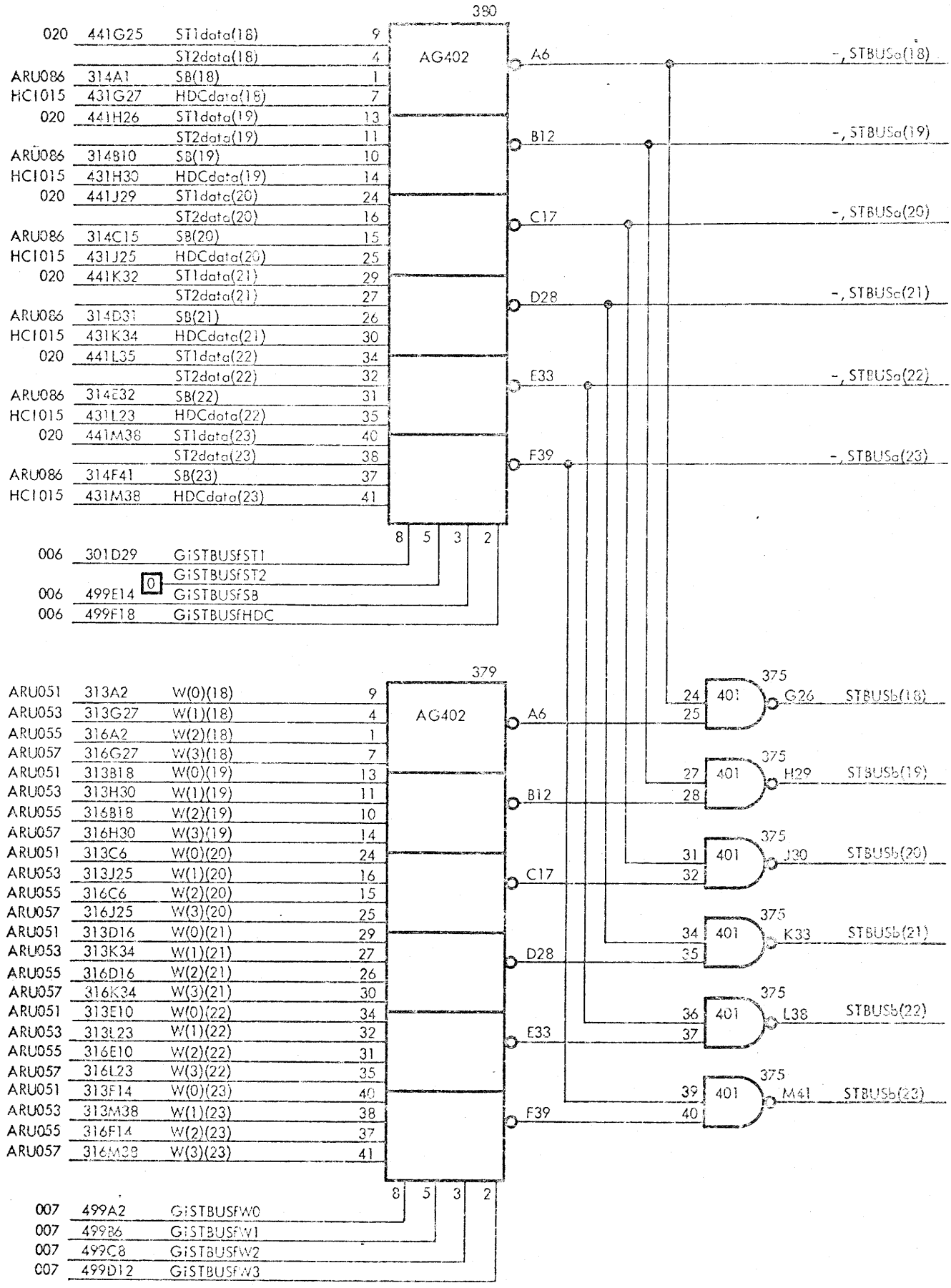
RC4000

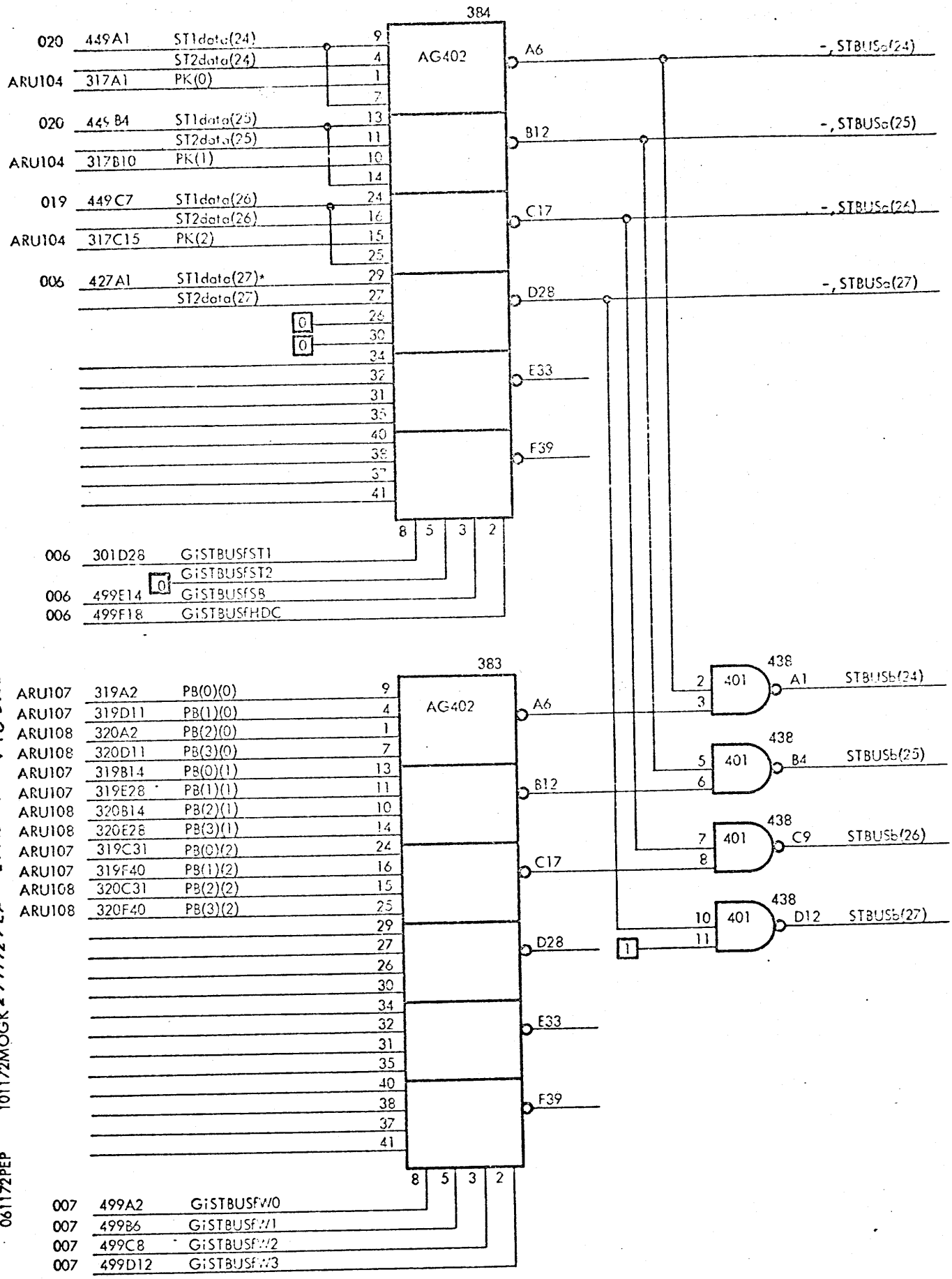
STBUS(12:17)

STC012

V13521

Logic Diagram

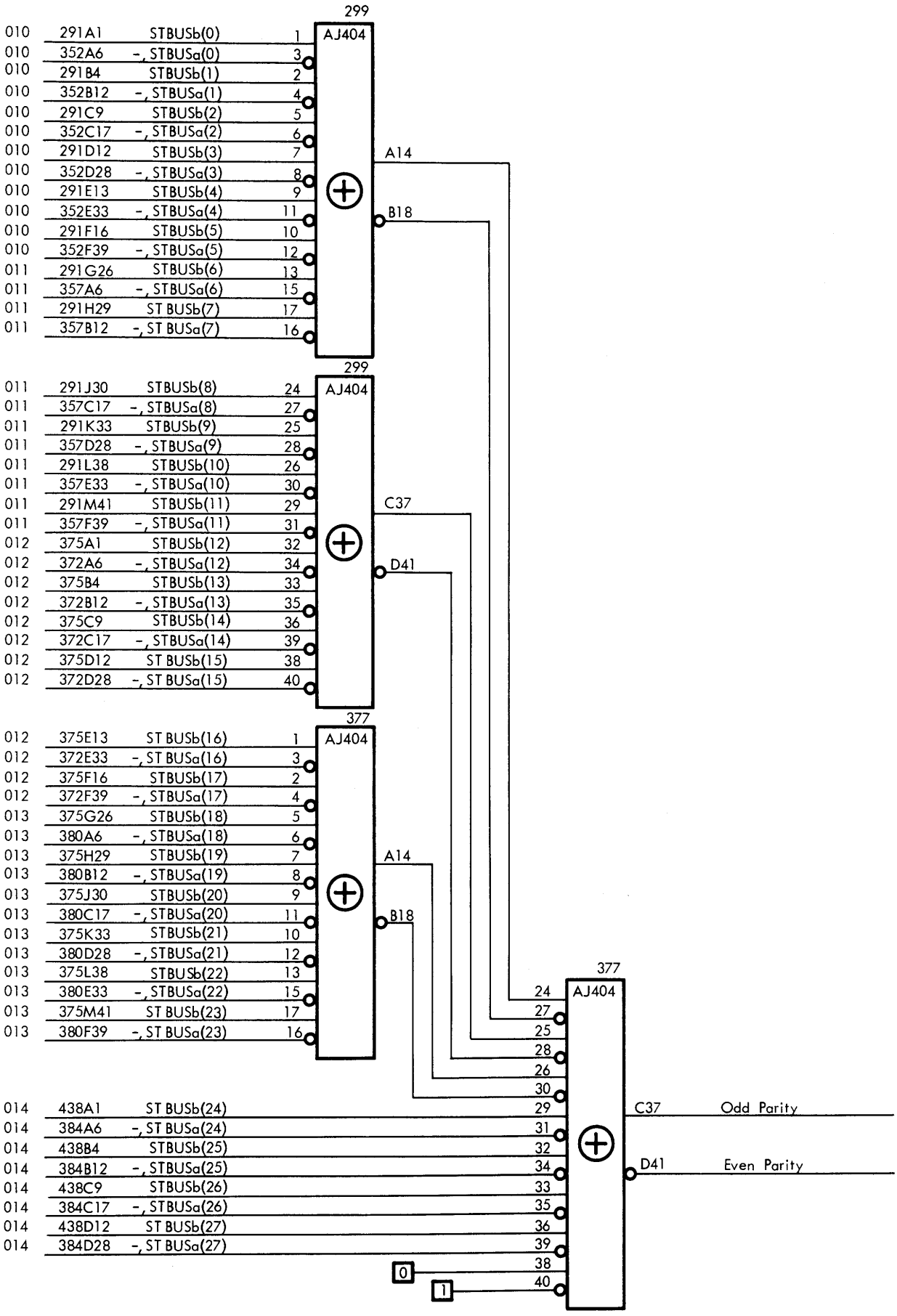

380
AG402
020 441G25 ST1data(18) 9
ST2data(18) 4
ARU086 314A1 SB(18) 1
HC1015 431G27 HDCdata(18) 7
020 441H26 ST1data(19) 13
ST2data(19) 11
ARU086 314B10 SB(19) 10
HC1015 431H30 HDCdata(19) 14
020 441J29 ST1data(20) 24
ST2data(20) 16
ARU086 314C15 SB(20) 15
HC1015 431J25 HDCdata(20) 25
020 441K32 ST1data(21) 29
ST2data(21) 27
ARU086 314D31 SB(21) 26
HC1015 431K34 HDCdata(21) 30
020 441L35 ST1data(22) 34
ST2data(22) 32
ARU086 314E32 SB(22) 31
HC1015 431L23 HDCdata(22) 35
020 441M38 ST1data(23) 40
ST2data(23) 38
ARU086 314F41 SB(23) 37
HC1015 431M38 HDCdata(23) 41
A6
B12
C17
D28
E33
F39
-,STBUSa(18)
-,STBUSa(19)
-,STBUSa(20)
-,STBUSa(21)
-,STBUSa(22)
-,STBUSa(23)
8 5 3 2
006 301D29 GiSTBUSfST1
0
GiSTBUSfST2
006 499E14 GiSTBUSfSB
006 499F18 GiSTBUSfHDC
379
AG402
ARU051 313A2 W(0)(18) 9
ARU053 313G27 W(1)(18) 4
ARU055 316A2 W(2)(18) 1
ARU057 316G27 W(3)(18) 7
ARU051 313B18 W(0)(19) 13
ARU053 313H30 W(1)(19) 11
ARU055 316B18 W(2)(19) 10
ARU057 316H30 W(3)(19) 14
ARU051 313C6 W(0)(20) 24
ARU053 313J25 W(1)(20) 16
ARU055 316C6 W(2)(20) 15
ARU057 316J25 W(3)(20) 25
ARU051 313D16 W(0)(21) 29
ARU053 313K34 W(1)(21) 27
ARU055 316D16 W(2)(21) 26
ARU057 316K34 W(3)(21) 30
ARU051 313E10 W(0)(22) 34
ARU053 313L23 W(1)(22) 32
ARU055 316E10 W(2)(22) 31
ARU057 316L23 W(3)(22) 35
ARU051 313F14 W(0)(23) 40
ARU053 313M38 W(1)(23) 38
ARU055 316F14 W(2)(23) 37
ARU057 316M38 W(3)(23) 41
A6
B12
C17
D28
E33
F39
8 5 3 2
007 499A2 GiSTBUSfW0
007 499B6 GiSTBUSfW1
007 499C8 GiSTBUSfW2
007 499D12 GiSTBUSfW3
375
401
24
25
G26
STBUSb(18)
27
28
H29
STBUSb(19)
31
32
J30
STBUSb(20)
34
35
K33
STBUSb(21)
36
37
L38
STBUSb(22)
39
40
M41
STBUSb(23)



V13523 271172PEP 101172MOGK 271172PEP 061172PEP

RC4000 STBUS(24:27) STC014

V13591 Logic Diagram



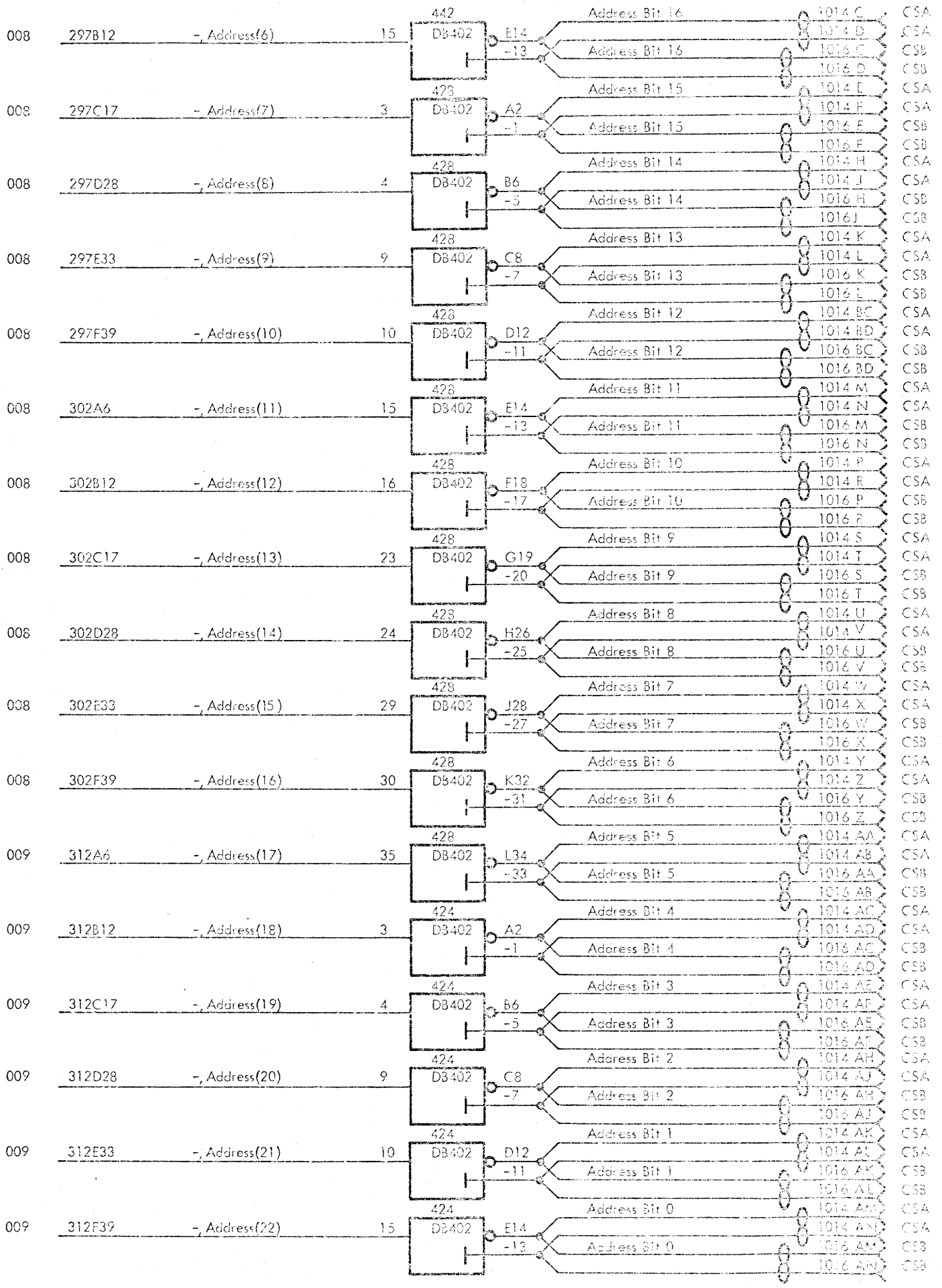
RC4000

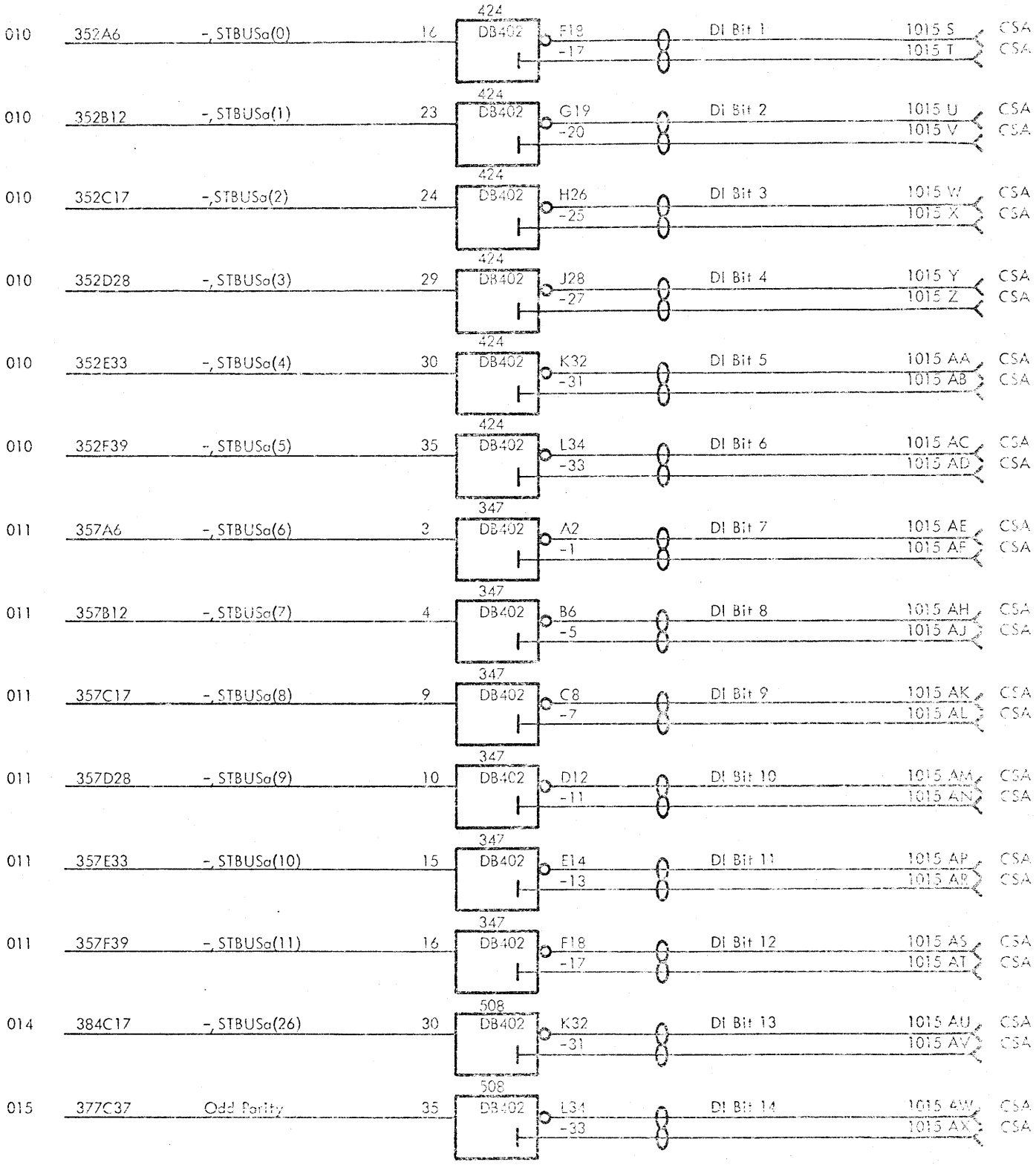
PARITY CHECK AND GENERATION

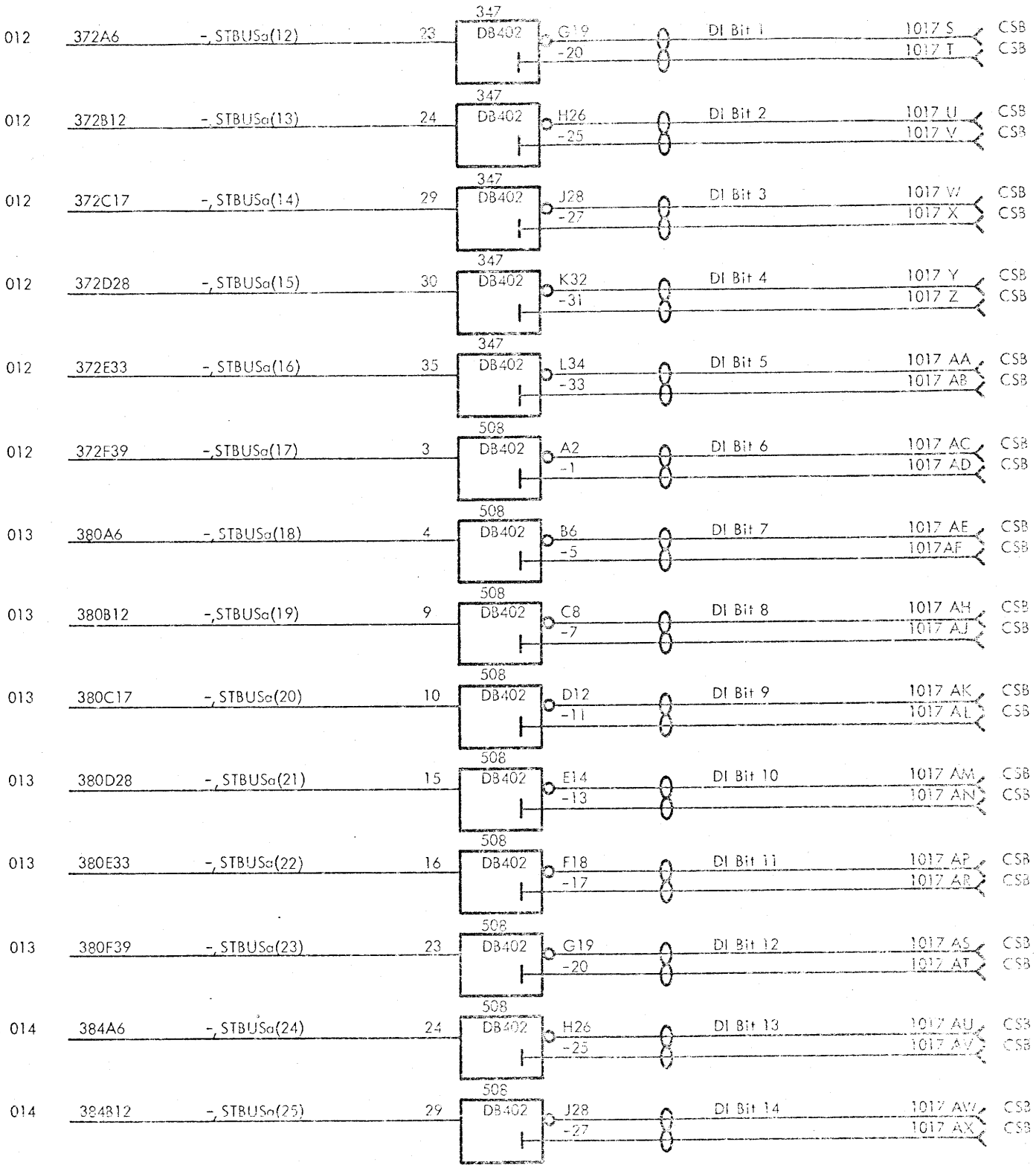
STC015

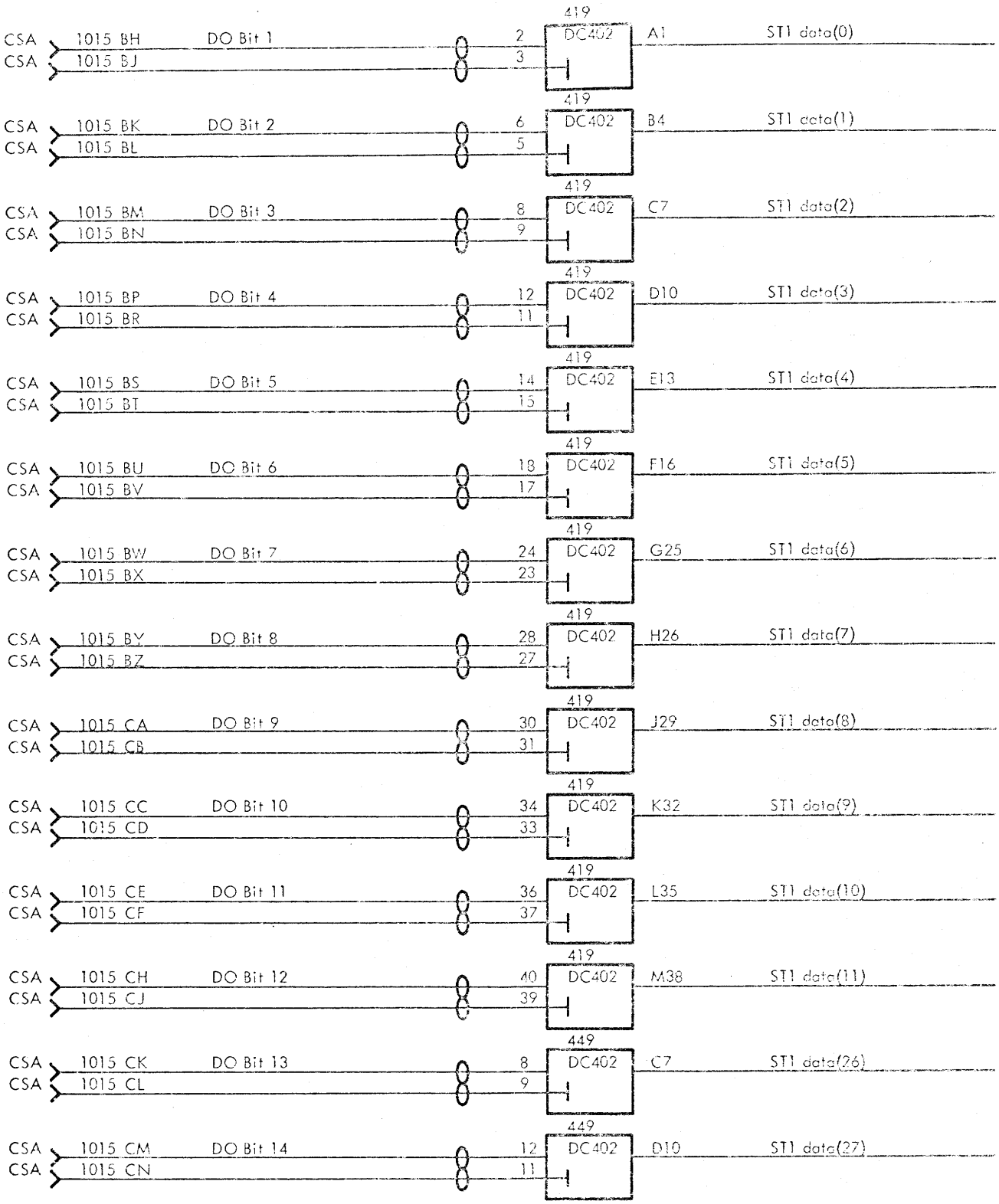
V10581

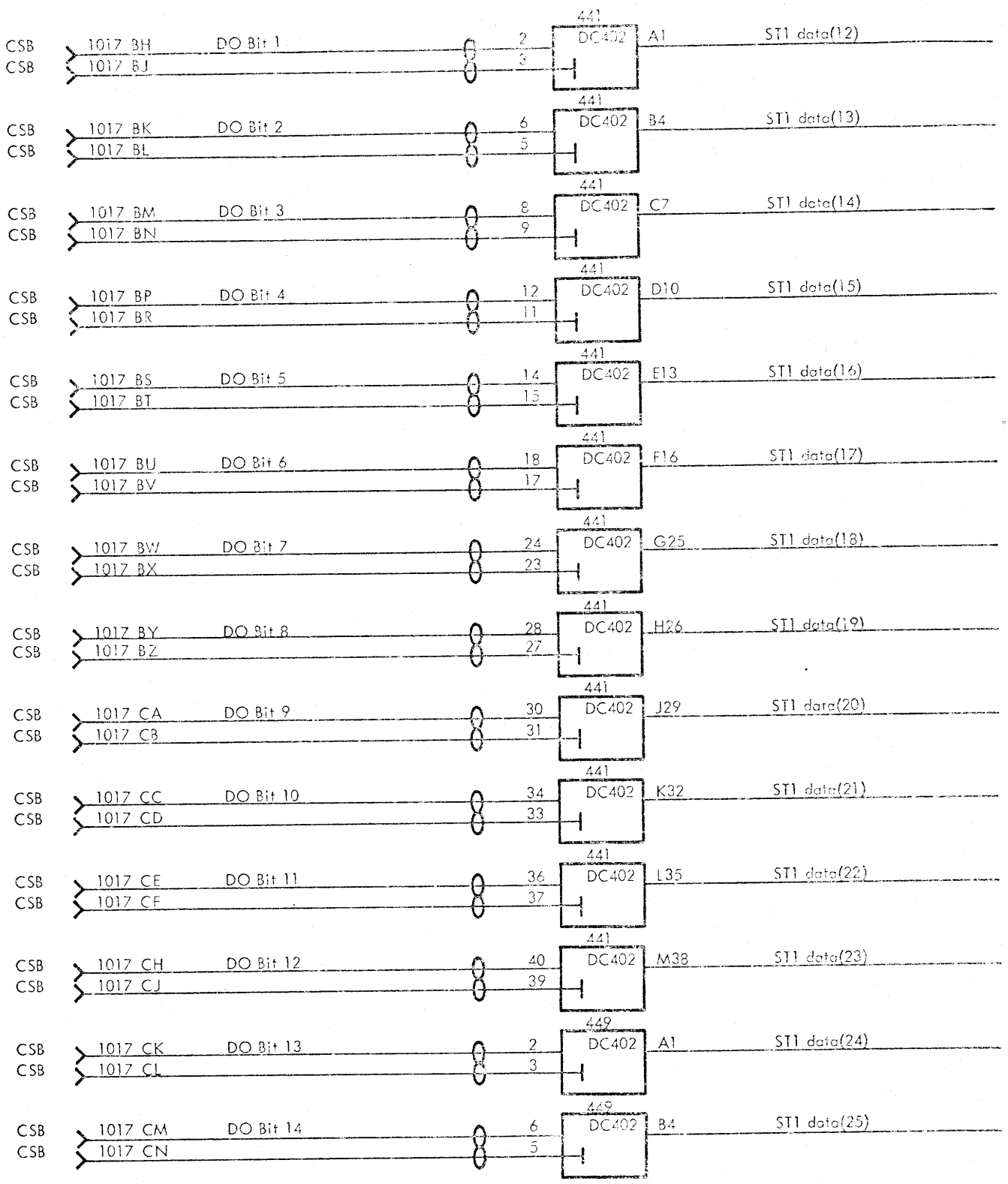
Logic Diagram

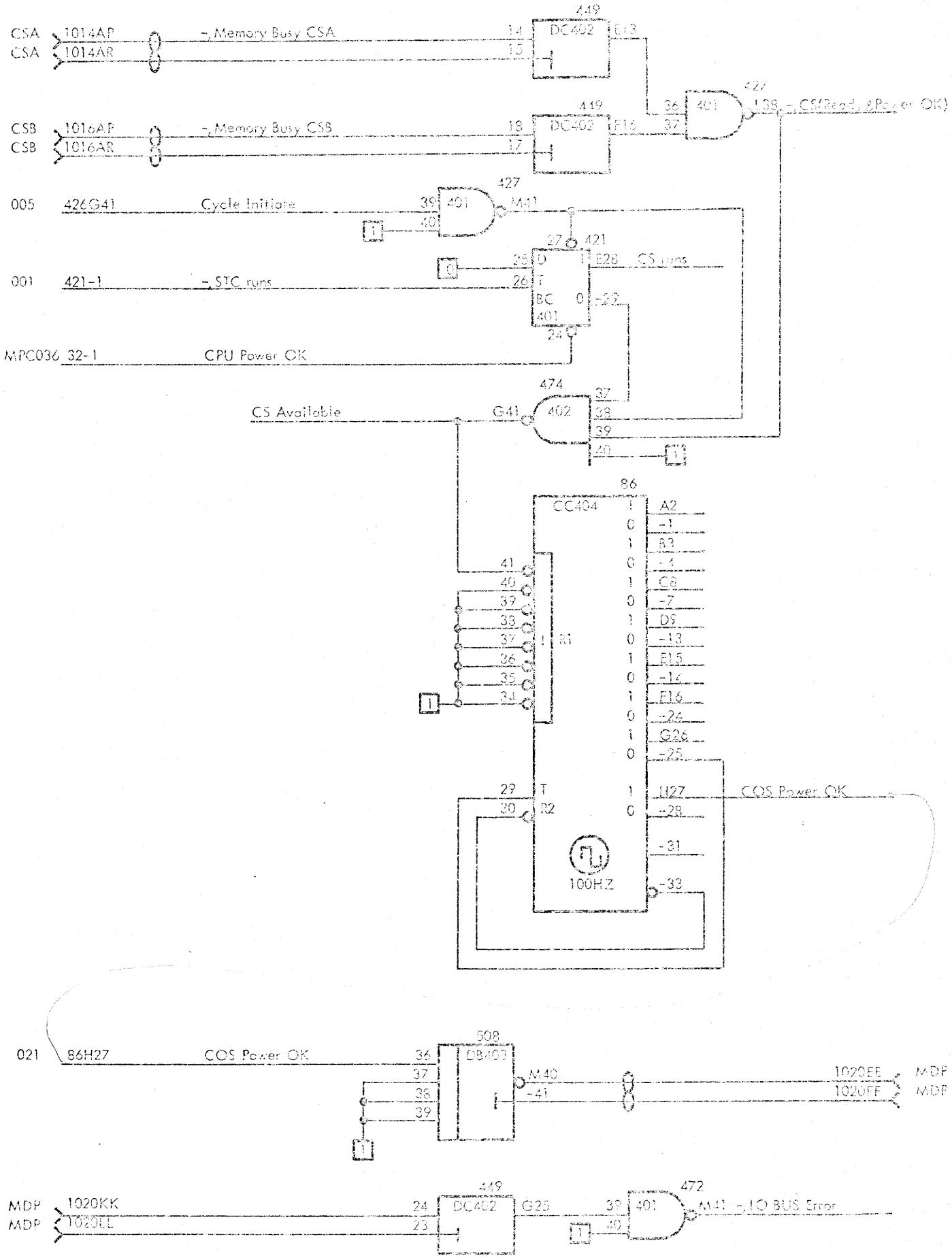

008 297B12 -, Address(6) 15 442 DB402 E14 -13 Address Bit 16 1014 C CSA 1014 D CSA 1016 C CSB 1016 D CSB
008 297C17 -, Address(7) 3 428 DB402 A2 -1 Address Bit 15 1014 E CSA 1014 F CSA 1016 E CSB 1016 F CSB
008 297D28 -, Address(8) 4 428 DB402 B6 -5 Address Bit 14 1014 H CSA 1014 J CSA 1016 H CSB 1016 J CSB
008 297E33 -, Address(9) 9 428 DB402 C8 -7 Address Bit 13 1014 K CSA 1014 L CSA 1016 K CSB 1016 L CSB
008 297F39 -, Address(10) 10 428 DB402 D12 -11 Address Bit 12 1014 BC CSA 1014 BD CSA 1016 BC CSB 1016 BD CSB
008 302A6 -, Address(11) 15 428 DB402 E14 -13 Address Bit 11 1014 M CSA 1014 N CSA 1016 M CSB 1016 N CSB
008 302B12 -, Address(12) 16 428 DB402 E18 -17 Address Bit 10 1014 P CSA 1014 R CSA 1016 P CSB 1016 R CSB
008 302C17 -, Address(13) 23 428 DB402 G19 -20 Address Bit 9 1014 S CSA 1014 T CSA 1016 S CSB 1016 T CSB
008 302D28 -, Address(14) 24 428 DB402 H26 -25 Address Bit 8 1014 U CSA 1014 V CSA 1016 U CSB 1016 V CSB
008 302E33 -, Address(15) 29 428 DB402 J28 -27 Address Bit 7 1014 W CSA 1014 X CSA 1016 W CSB 1016 X CSB
008 302F39 -, Address(16) 30 428 DB402 K32 -31 Address Bit 6 1014 Y CSA 1014 Z CSA 1016 Y CSB 1016 Z CSB
009 312A6 -, Address(17) 35 428 DB402 L34 -33 Address Bit 5 1014 AA CSA 1014 AB CSA 1016 AA CSB 1016 AB CSB
009 312B12 -, Address(18) 3 424 DB402 A2 -1 Address Bit 4 1014 AC CSA 1014 AD CSA 1016 AC CSB 1016 AD CSB
009 312C17 -, Address(19) 4 424 DB402 B6 -5 Address Bit 3 1014 AE CSA 1014 AF CSA 1016 AE CSB 1016 AF CSB
009 312D28 -, Address(20) 9 424 DB402 C8 -7 Address Bit 2 1014 AH CSA 1014 AJ CSA 1016 AH CSB 1016 AJ CSB
009 312E33 -, Address(21) 10 424 DB402 D12 -11 Address Bit 1 1014 AK CSA 1014 AL CSA 1016 AK CSB 1016 AL CSB
009 312F39 -, Address(22) 15 424 DB402 E14 -13 Address Bit 0 1014 AM CSA 1014 AN CSA 1016 AM CSB 1016 AN CSB

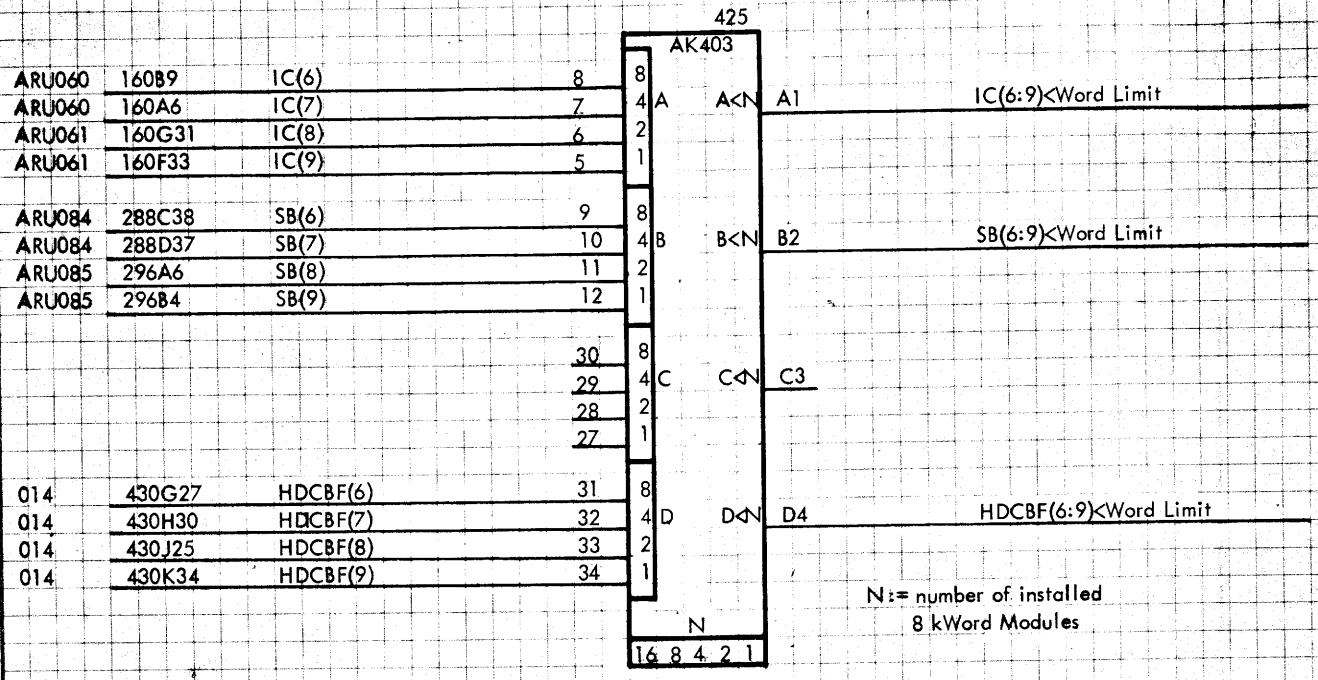

010 352A6 -,STBUSa(0) 16 424 DB402 F18 -17 DI Bit 1 1015 S CSA 1015 T CSA
010 352B12 -,STBUSa(1) 23 424 DB402 G19 -20 DI Bit 2 1015 U CSA 1015 V CSA
010 352C17 -,STBUSa(2) 24 424 DB402 H26 -25 DI Bit 3 1015 W CSA 1015 X CSA
010 352D28 -,STBUSa(3) 29 424 DB402 J28 -27 DI Bit 4 1015 Y CSA 1015 Z CSA
010 352E33 -,STBUSa(4) 30 424 DB402 K32 -31 DI Bit 5 1015 AA CSA 1015 AB CSA
010 352F39 -,STBUSa(5) 35 424 DB402 L34 -33 DI Bit 6 1015 AC CSA 1015 AD CSA
011 357A6 -,STBUSa(6) 3 347 DB402 A2 -1 DI Bit 7 1015 AE CSA 1015 AF CSA
011 357B12 -,STBUSa(7) 4 347 DB402 B6 -5 DI Bit 8 1015 AH CSA 1015 AJ CSA
011 357C17 -,STBUSa(8) 9 347 DB402 C8 -7 DI Bit 9 1015 AK CSA 1015 AL CSA
011 357D28 -,STBUSa(9) 10 347 DB402 D12 -11 DI Bit 10 1015 AM CSA 1015 AN CSA
011 357E33 -,STBUSa(10) 15 347 DB402 E14 -13 DI Bit 11 1015 AP CSA 1015 AR CSA
011 357F39 -,STBUSa(11) 16 347 DB402 F18 -17 DI Bit 12 1015 AS CSA 1015 AT CSA
014 384C17 -,STBUSa(26) 30 508 DB402 K32 -31 DI Bit 13 1015 AU CSA 1015 AV CSA
015 377C37 Odd Parity 35 508 DB402 L34 -33 DI Bit 14 1015 AW CSA 1015 AX CSA

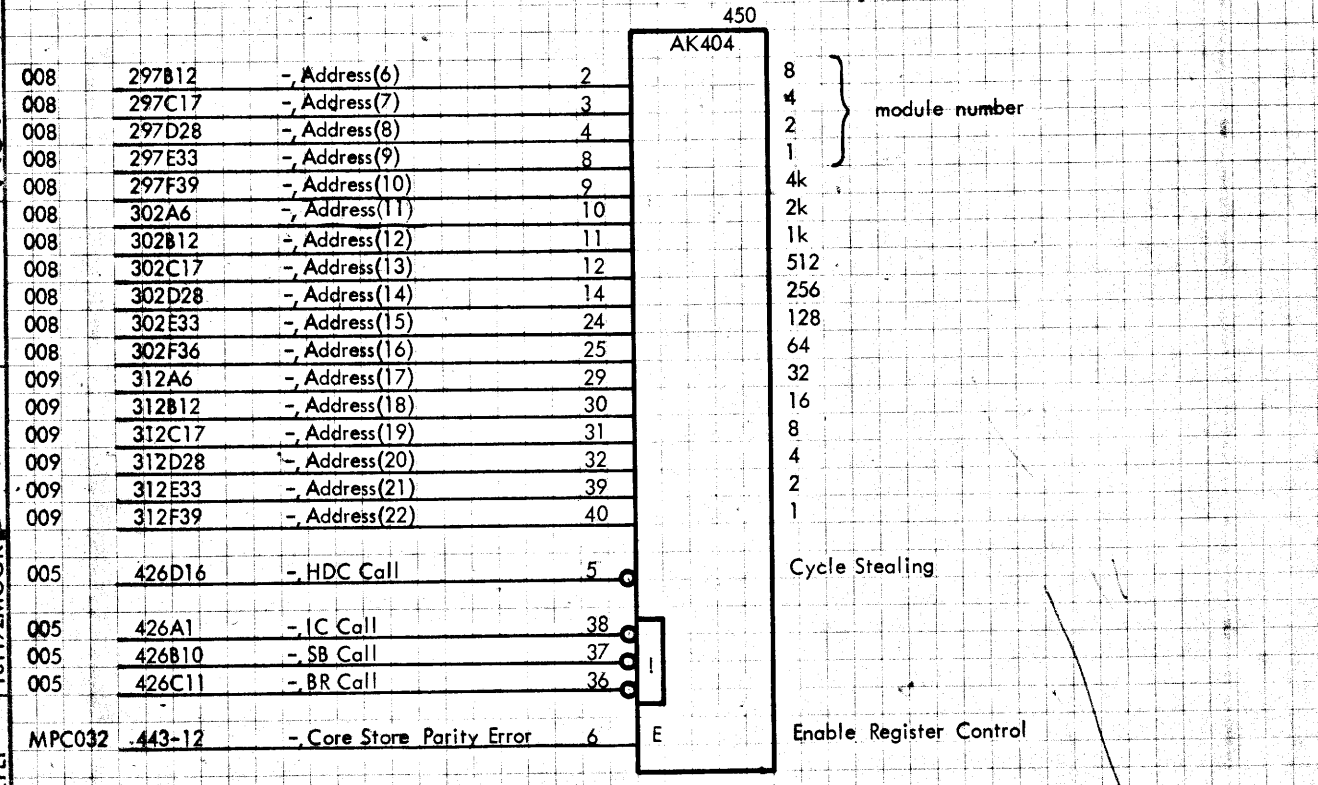

012 372A6 -,STBUSa(12) 23 347 DB402 G19 -20 DI Bit 1 1017 S 1017 T CSB CSB
012 372B12 -,STBUSa(13) 24 347 DB402 H26 -25 DI Bit 2 1017 U 1017 V CSB CSB
012 372C17 -,STBUSa(14) 29 347 DB402 J28 -27 DI Bit 3 1017 W 1017 X CSB CSB
012 372D28 -,STBUSa(15) 30 347 DB402 K32 -31 DI Bit 4 1017 Y 1017 Z CSB CSB
012 372E33 -,STBUSa(16) 35 347 DB402 L34 -33 DI Bit 5 1017 AA 1017 AB CSB CSB
012 372F39 -,STBUSa(17) 3 508 DB402 A2 -1 DI Bit 6 1017 AC 1017 AD CSB CSB
013 380A6 -,STBUSa(18) 4 508 DB402 B6 -5 DI Bit 7 1017 AE 1017AF CSB CSB
013 380B12 -,STBUSa(19) 9 508 DB402 C8 -7 DI Bit 8 1017 AH 1017 AJ CSB CSB
013 380C17 -,STBUSa(20) 10 508 DB402 D12 -11 DI Bit 9 1017 AK 1017 AL CSB CSB
013 380D28 -,STBUSa(21) 15 508 DB402 E14 -13 DI Bit 10 1017 AM 1017 AN CSB CSB
013 380E33 -,STBUSa(22) 16 508 DB402 F18 -17 DI Bit 11 1017 AP 1017 AR CSB CSB
013 380F39 -,STBUSa(23) 23 508 DB402 G19 -20 DI Bit 12 1017 AS 1017 AT CSB CSB
014 384A6 -,STBUSa(24) 24 508 DB402 H26 -25 DI Bit 13 1017 AU 1017 AV CSB CSB
014 384B12 -,STBUSa(25) 29 508 DB402 J28 -27 DI Bit 14 1017 AW 1017 AX CSB CSB


CSA 1015 BH
CSA 1015 BJ
DO Bit 1
2
3
419
DC402
A1
ST1 data(0)
CSA 1015 BK
CSA 1015 BL
DO Bit 2
6
5
419
DC402
B4
ST1 data(1)
CSA 1015 BM
CSA 1015 BN
DO Bit 3
8
9
419
DC402
C7
ST1 data(2)
CSA 1015 BP
CSA 1015 BR
DO Bit 4
12
11
419
DC402
D10
ST1 data(3)
CSA 1015 BS
CSA 1015 BT
DO Bit 5
14
15
419
DC402
E13
ST1 data(4)
CSA 1015 BU
CSA 1015 BV
DO Bit 6
18
17
419
DC402
F16
ST1 data(5)
CSA 1015 BW
CSA 1015 BX
DO Bit 7
24
23
419
DC402
G25
ST1 data(6)
CSA 1015 BY
CSA 1015 BZ
DO Bit 8
28
27
419
DC402
H26
ST1 data(7)
CSA 1015 CA
CSA 1015 CB
DO Bit 9
30
31
419
DC402
J29
ST1 data(8)
CSA 1015 CC
CSA 1015 CD
DO Bit 10
34
33
419
DC402
K32
ST1 data(9)
CSA 1015 CE
CSA 1015 CF
DO Bit 11
36
37
419
DC402
L35
ST1 data(10)
CSA 1015 CH
CSA 1015 CJ
DO Bit 12
40
39
419
DC402
M38
ST1 data(11)
CSA 1015 CK
CSA 1015 CL
DO Bit 13
8
9
449
DC402
C7
ST1 data(26)
CSA 1015 CM
CSA 1015 CN
DO Bit 14
12
11
449
DC402
D10
ST1 data(27)


CSB 1017 BH DO Bit 1
CSB 1017 BJ
441 DC402 2 3 A1 ST1 data(12)
CSB 1017 BK DO Bit 2
CSB 1017 BL
441 DC402 6 5 B4 ST1 data(13)
CSB 1017 BM DO Bit 3
CSB 1017 BN
441 DC402 8 9 C7 ST1 data(14)
CSB 1017 BP DO Bit 4
CSB 1017 BR
441 DC402 12 11 D10 ST1 data(15)
CSB 1017 BS DO Bit 5
CSB 1017 BT
441 DC402 14 15 E13 ST1 data(16)
CSB 1017 BU DO Bit 6
CSB 1017 BV
441 DC402 18 17 F16 ST1 data(17)
CSB 1017 BW DO Bit 7
CSB 1017 BX
441 DC402 24 23 G25 ST1 data(18)
CSB 1017 BY DO Bit 8
CSB 1017 BZ
441 DC402 28 27 H26 ST1 data(19)
CSB 1017 CA DO Bit 9
CSB 1017 CB
441 DC402 30 31 J29 ST1 data(20)
CSB 1017 CC DO Bit 10
CSB 1017 CD
441 DC402 34 33 K32 ST1 data(21)
CSB 1017 CE DO Bit 11
CSB 1017 CF
441 DC402 36 37 L35 ST1 data(22)
CSB 1017 CH DO Bit 12
CSB 1017 CJ
441 DC402 40 39 M38 ST1 data(23)
CSB 1017 CK DO Bit 13
CSB 1017 CL
449 DC402 2 3 A1 ST1 data(24)
CSB 1017 CM DO Bit 14
CSB 1017 CN
449 DC402 6 5 B4 ST1 data(25)


CSA 1014AP
CSA 1014AR
-, Memory Busy CSA
449
DC402
CSB 1016AP
CSB 1016AR
-, Memory Busy CSB
427
401
-, CS(Read) & Power OK)
005 426G41
Cycle Initiate
421
CS runs
001 421-1
-, STC runs
MPC036 32-1
CPU Power OK
474
402
CS Available
G41
86
CC404
A2
B3
C8
D5
E15
F16
G26
H27
COS Power OK
R1
R2
100HZ
021 86H27
COS Power OK
508
DB403
M40
-41
1020EE
1020FF
MDP
MDP
1020KK
1020LL
472
M41 -, IO BUS Error
G25





Replaced by Dwg. No.

due to ECN

Replaces Dwg. No. V13525

Design Check 271172 PEP

Dwg. Office Check 271172 PEP

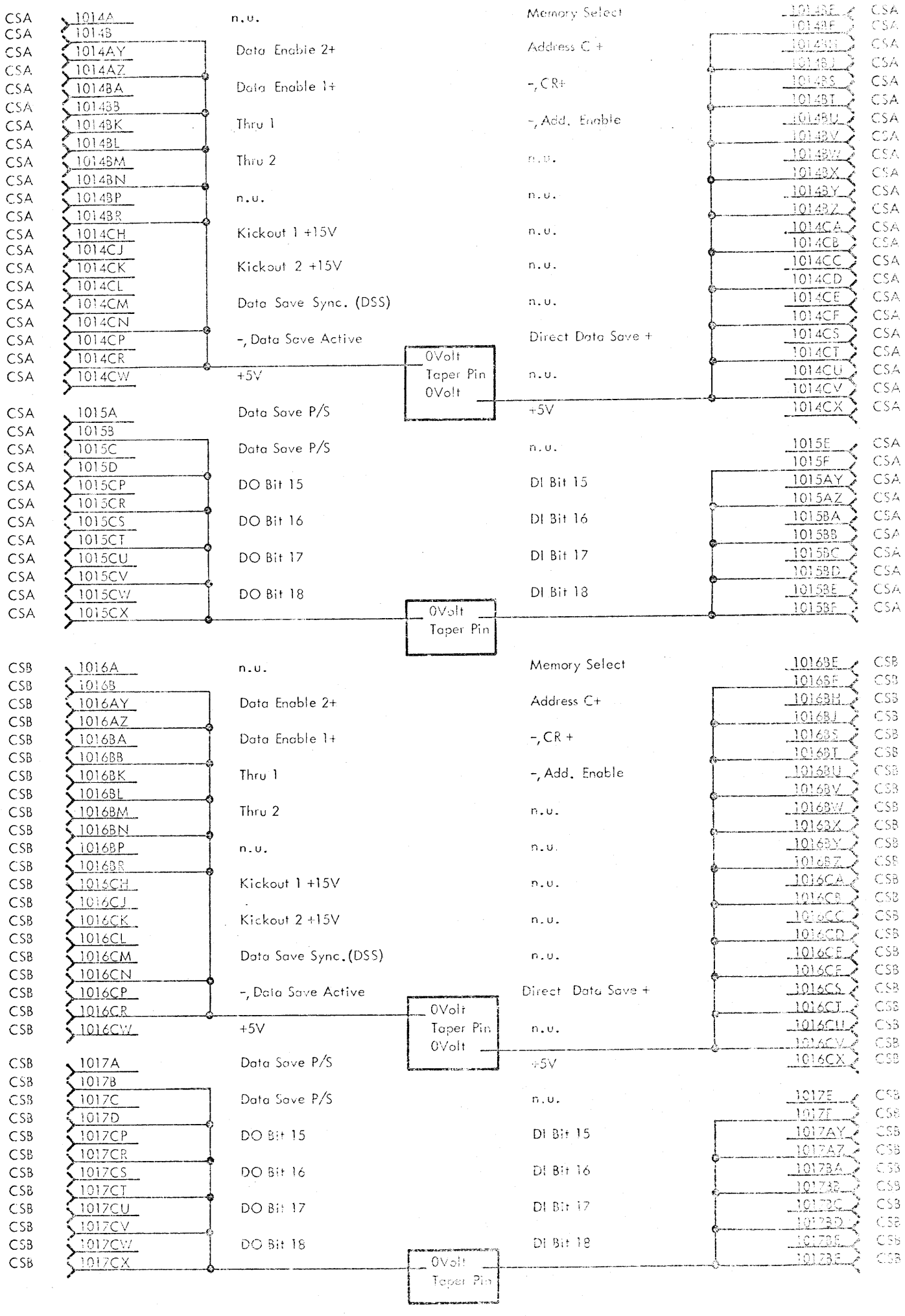
Drawn by 101172MOGK

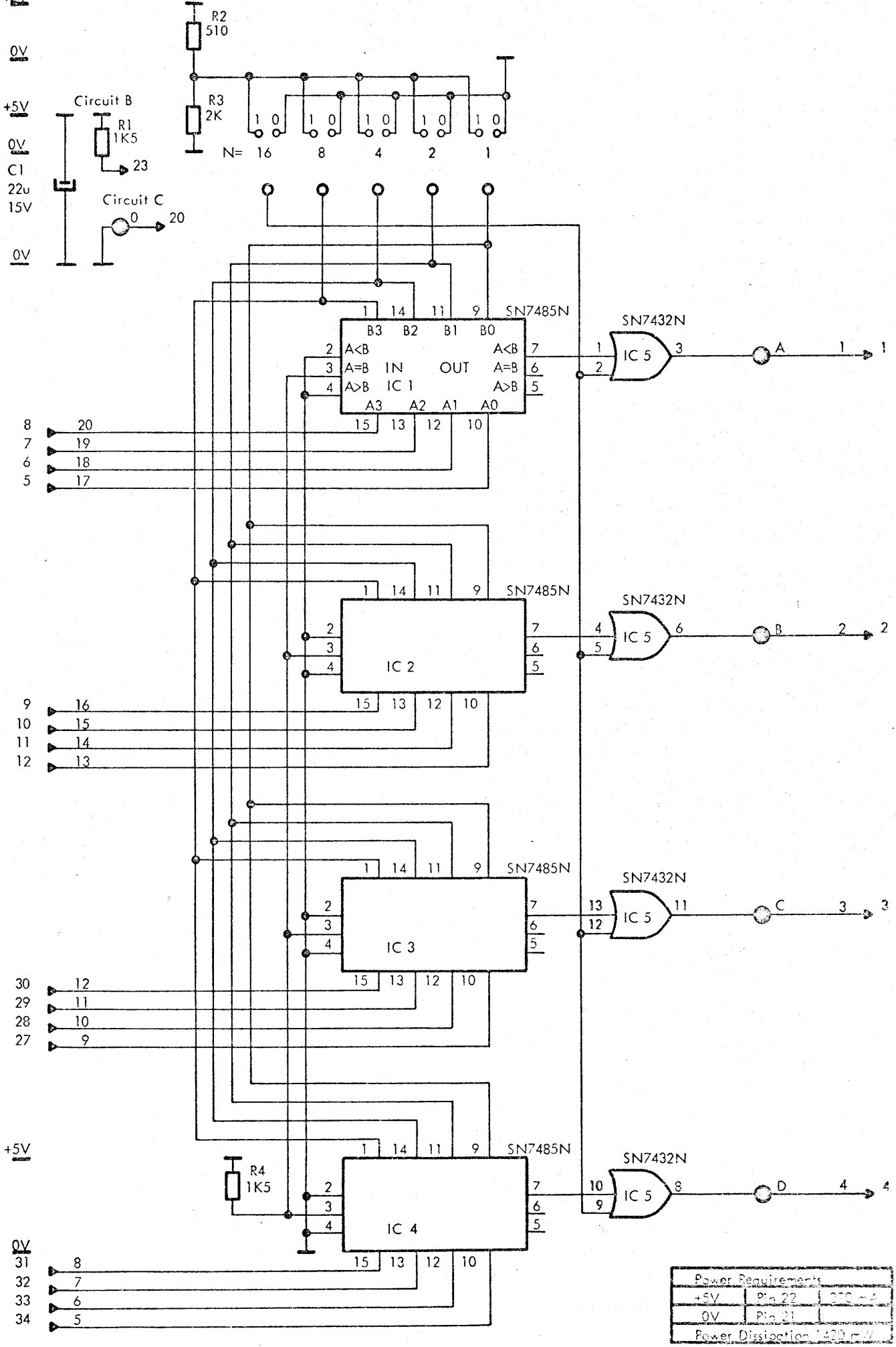
Designed by 061172PEP

CENTRALEN

Unit		
RC4000	CORE STORE SIZE AND ADDRESS DISPLAY	STC022
Dwg. No. V13592	Logic Diagram	

A/S


CSA 1014A n.u.
CSA 1014B
CSA 1014AY Data Enable 2+
CSA 1014AZ
CSA 1014BA Data Enable 1+
CSA 1014BB
CSA 1014BK Thru 1
CSA 1014BL
CSA 1014BM Thru 2
CSA 1014BN
CSA 1014BP n.u.
CSA 1014BR
CSA 1014CH Kickout 1 +15V
CSA 1014CJ
CSA 1014CK Kickout 2 +15V
CSA 1014CL
CSA 1014CM Data Save Sync. (DSS)
CSA 1014CN
CSA 1014CP -, Data Save Active
CSA 1014CR
CSA 1014CW +5V
0Volt Taper Pin 0Volt
Memory Select
Address C +
-, CR+
-, Add. Enable
n.u.
n.u.
n.u.
n.u.
Direct Data Save +
n.u.
+5V
1014BE CSA
1014BF CSA
1014BH CSA
1014BJ CSA
1014BS CSA
1014BT CSA
1014BU CSA
1014BV CSA
1014BW CSA
1014BX CSA
1014BY CSA
1014BZ CSA
1014CA CSA
1014CB CSA
1014CC CSA
1014CD CSA
1014CE CSA
1014CF CSA
1014CS CSA
1014CT CSA
1014CU CSA
1014CV CSA
1014CX CSA
CSA 1015A Data Save P/S
CSA 1015B
CSA 1015C Data Save P/S
CSA 1015D
CSA 1015CP DO Bit 15
CSA 1015CR
CSA 1015CS DO Bit 16
CSA 1015CT
CSA 1015CU DO Bit 17
CSA 1015CV
CSA 1015CW DO Bit 18
CSA 1015CX
0Volt Taper Pin
n.u.
DI Bit 15
DI Bit 16
DI Bit 17
DI Bit 18
1015E CSA
1015F CSA
1015AY CSA
1015AZ CSA
1015BA CSA
1015BB CSA
1015BC CSA
1015BD CSA
1015BE CSA
1015BF CSA
CSB 1016A n.u.
CSB 1016B
CSB 1016AY Data Enable 2+
CSB 1016AZ
CSB 1016BA Data Enable 1+
CSB 1016BB
CSB 1016BK Thru 1
CSB 1016BL
CSB 1016BM Thru 2
CSB 1016BN
CSB 1016BP n.u.
CSB 1016BR
CSB 1016CH Kickout 1 +15V
CSB 1016CJ
CSB 1016CK Kickout 2 +15V
CSB 1016CL
CSB 1016CM Data Save Sync.(DSS)
CSB 1016CN
CSB 1016CP -, Data Save Active
CSB 1016CR
CSB 1016CW +5V
0Volt Taper Pin 0Volt
Memory Select
Address C+
-, CR +
-, Add. Enable
n.u.
n.u.
n.u.
n.u.
Direct Data Save +
n.u.
+5V
1016BE CSB
1016BF CSB
1016BH CSB
1016BJ CSB
1016BS CSB
1016BT CSB
1016BU CSB
1016BV CSB
1016BW CSB
1016BX CSB
1016BY CSB
1016BZ CSB
1016CA CSB
1016CB CSB
1016CC CSB
1016CD CSB
1016CE CSB
1016CF CSB
1016CS CSB
1016CJ CSB
1016CU CSB
1016CV CSB
1016CX CSB
CSB 1017A Data Save P/S
CSB 1017B
CSB 1017C Data Save P/S
CSB 1017D
CSB 1017CP DO Bit 15
CSB 1017CR
CSB 1017CS DO Bit 16
CSB 1017CT
CSB 1017CU DO Bit 17
CSB 1017CV
CSB 1017CW DO Bit 18
CSB 1017CX
0Volt Taper Pin
n.u.
DI Bit 15
DI Bit 16
DI Bit 17
DI Bit 18
1017E CSB
1017F CSB
1017AY CSB
1017AZ CSB
1017BA CSB
1017BB CSB
1017BC CSB
1017BD CSB
1017BE CSB
1017BF CSB

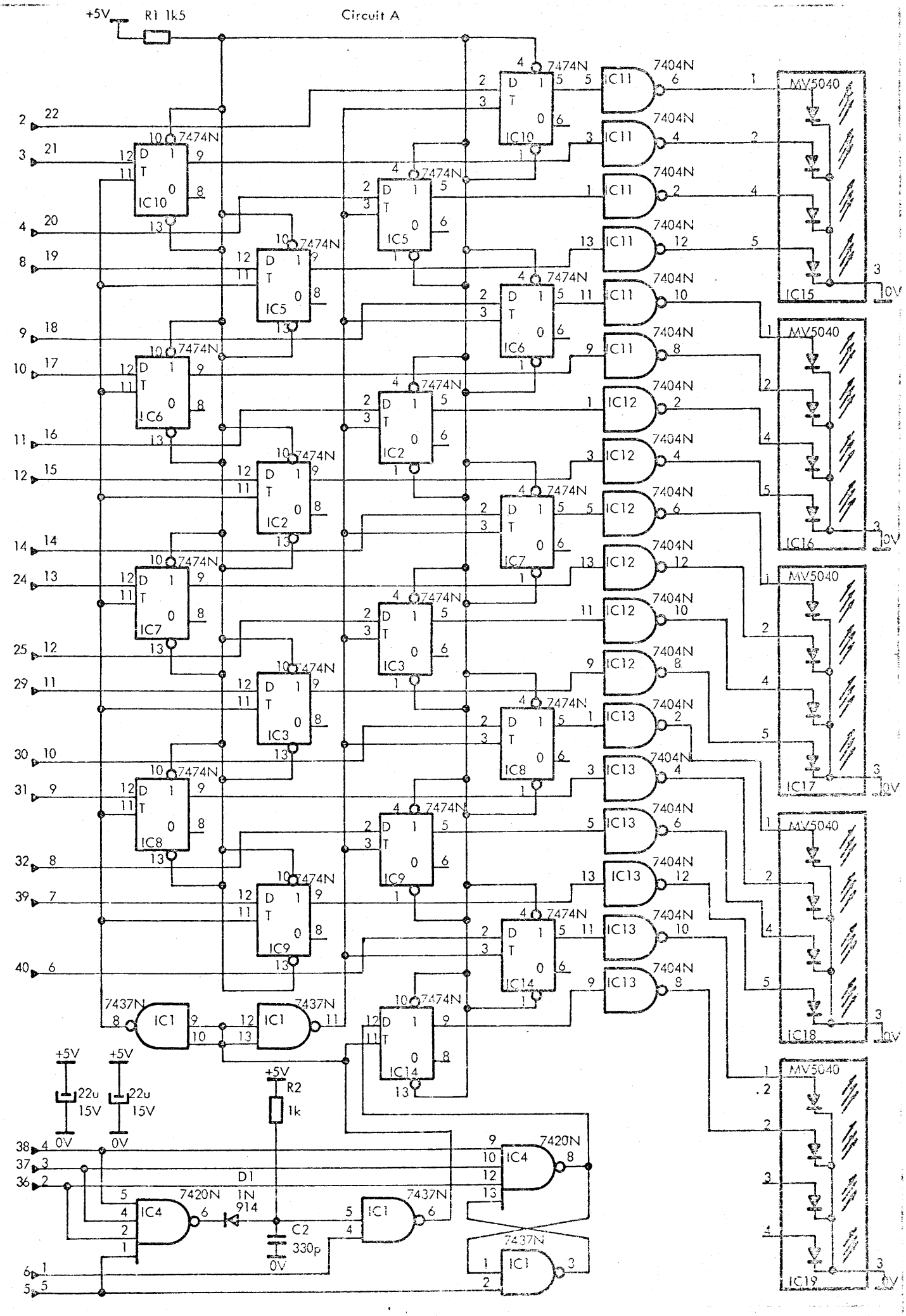


Power Requirements		
+5V	Pin 22	270 mA
0V	Pin 21	
Power Dissipation 1620 mW		

061172 PEP 73 01 03 BA

RCLM400 1 AK 403 RC2052-1

V13575 PCBA Circuit Diagram



090173BA

151272AL

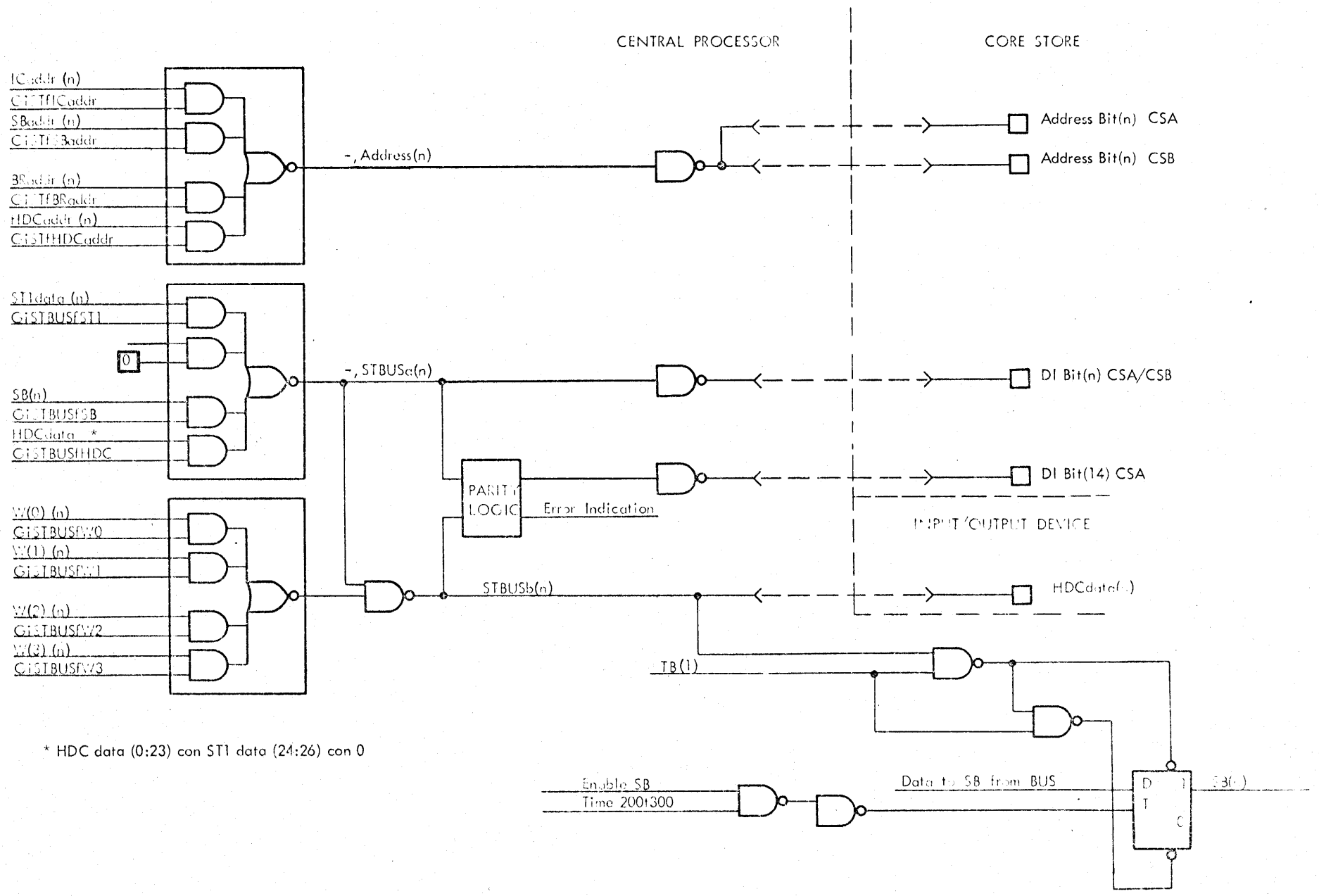
010572PEP

RCLM400 1AK404 RC2073 - 1

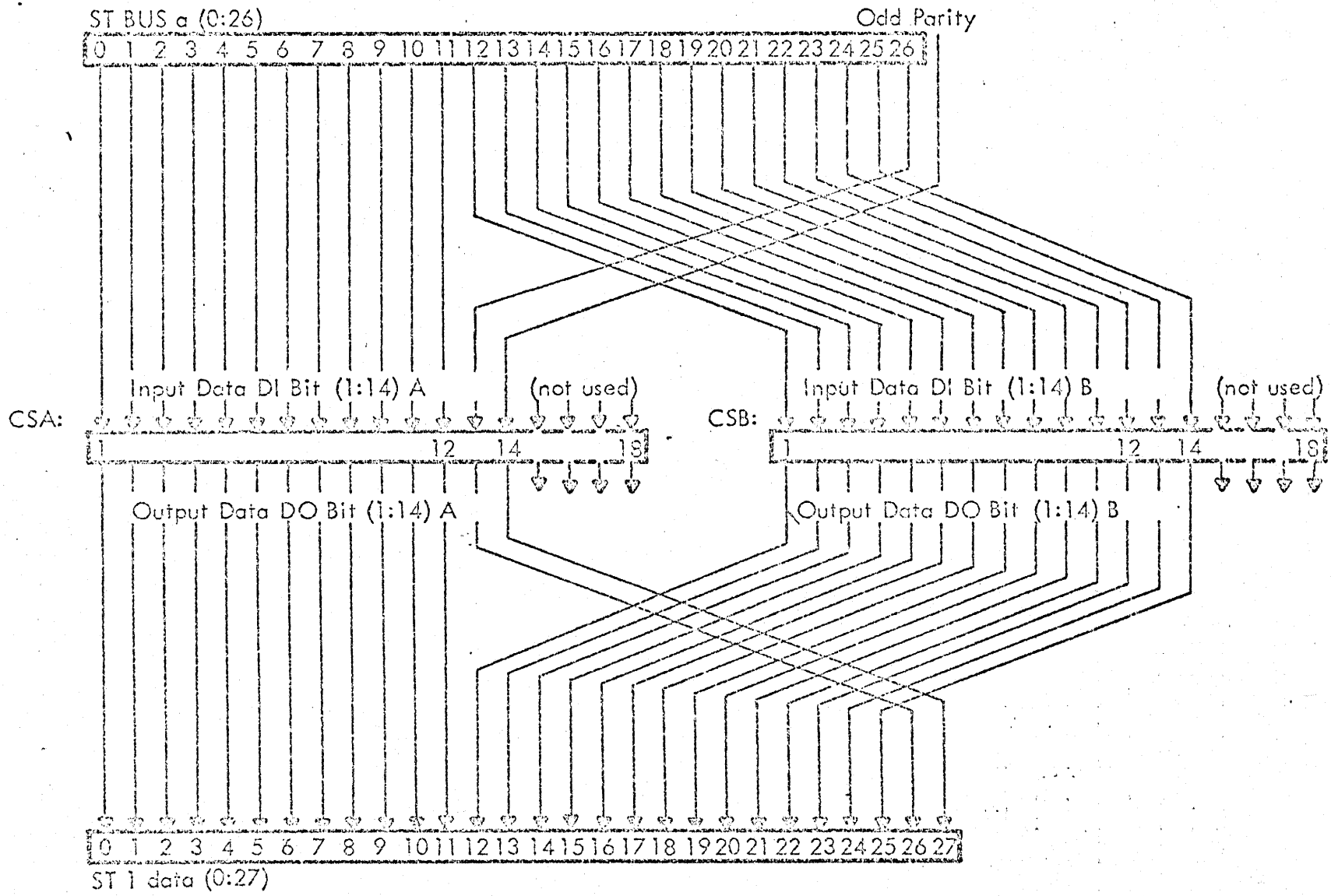
V13572 PCBA Circuit Diagram

DATA PATHS CONTROLLED BY THE STC

Block Diagram

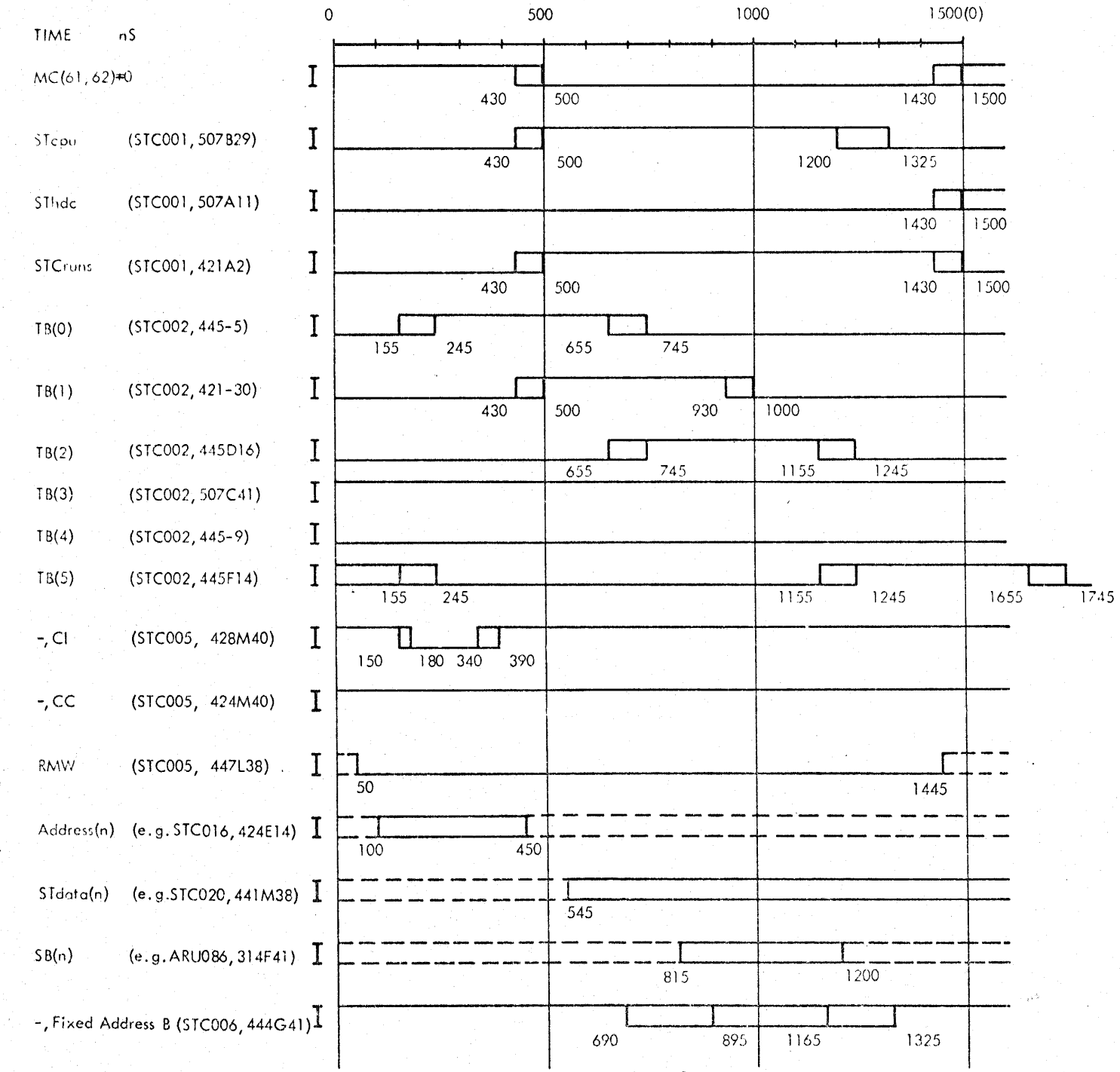


* HDC data (0:23) con ST1 data (24:26) con 0


ST BUS a (0:26)
Odd Parity
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
CSA:
Input Data DI Bit (1:14) A
(not used)
1 12 14 18
CSB:
Input Data DI Bit (1:14) B
(not used)
1 12 14 18
Output Data DO Bit (1:14) A
Output Data DO Bit (1:14) B
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
ST 1 data (0:27)

V13565 RC4000

061172PEP 291172MOGK 291172 PEP

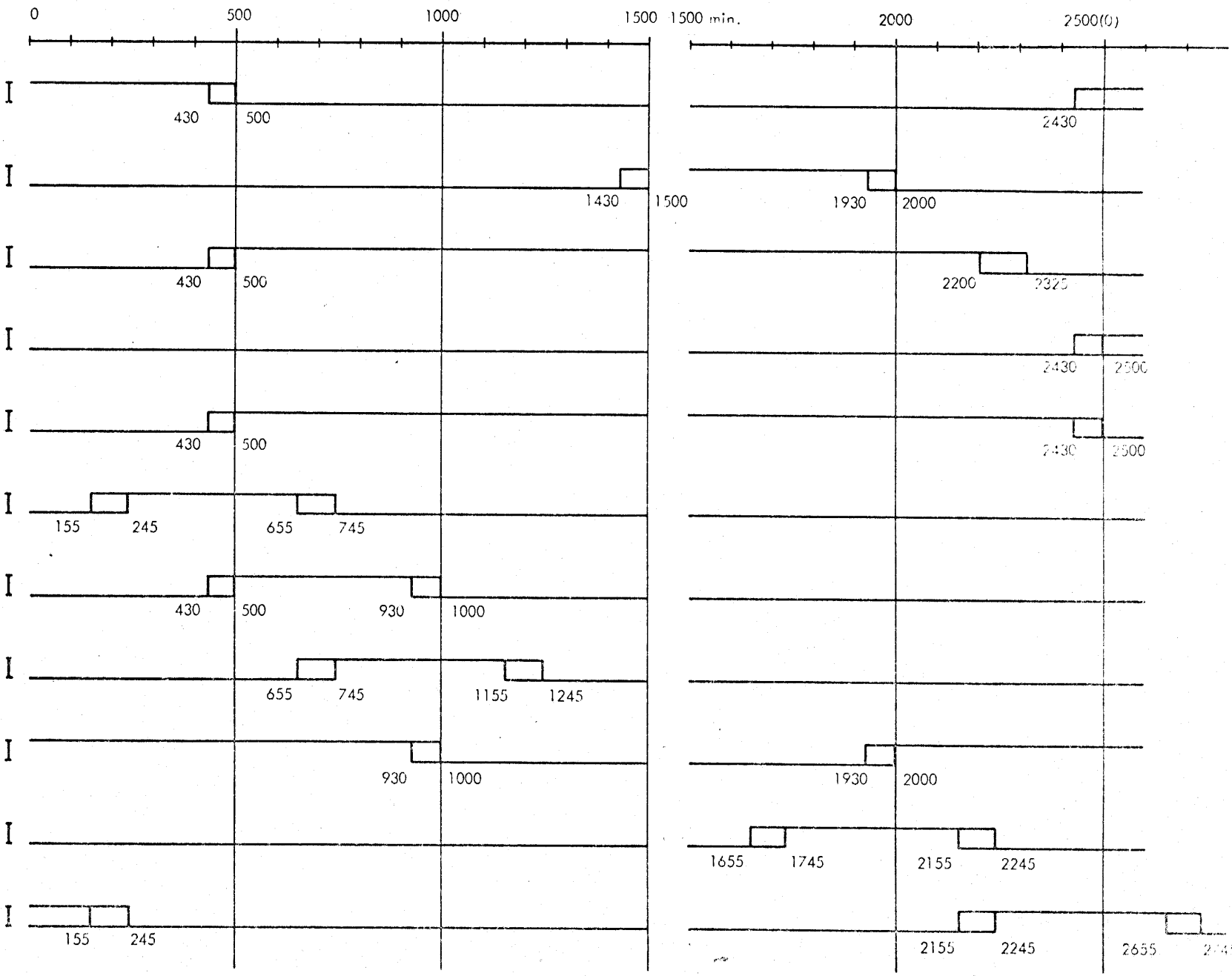


RAPID CORE STORE TIMING FOR READ INSTRUCTION AND READ DATA (DOUBLE)
6 < ADDRESS < WORD LIMIT
Timing Chart

RC4000

V13566

TB AND CORE STORE TIMING FOR READ SPLIT - SPLIT WRITE
6 < ADDRESS < WORD LIMIT
Timing Chart

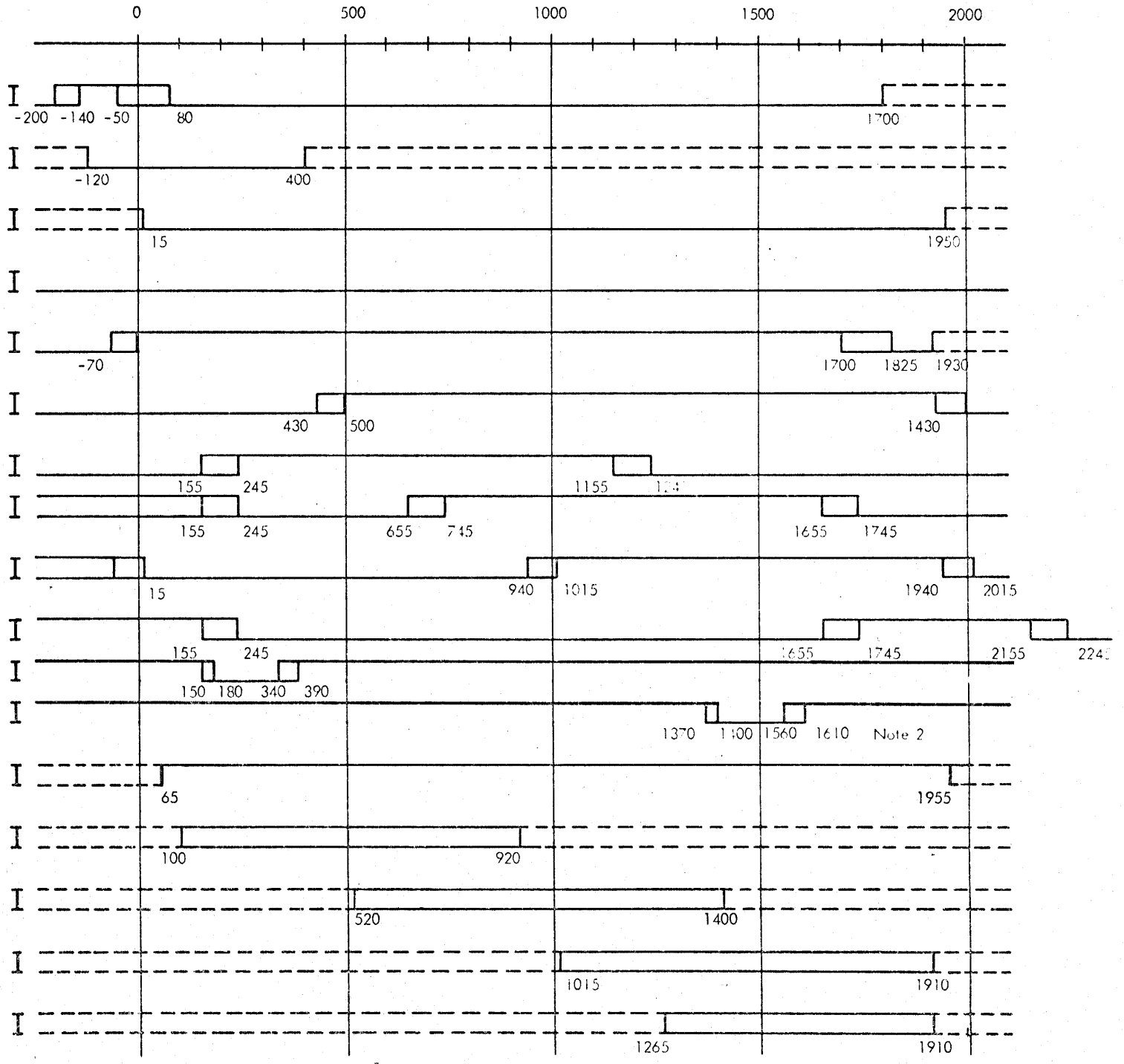


V13570 RC4000

061172PEP 291172MOGK 291172 PEP

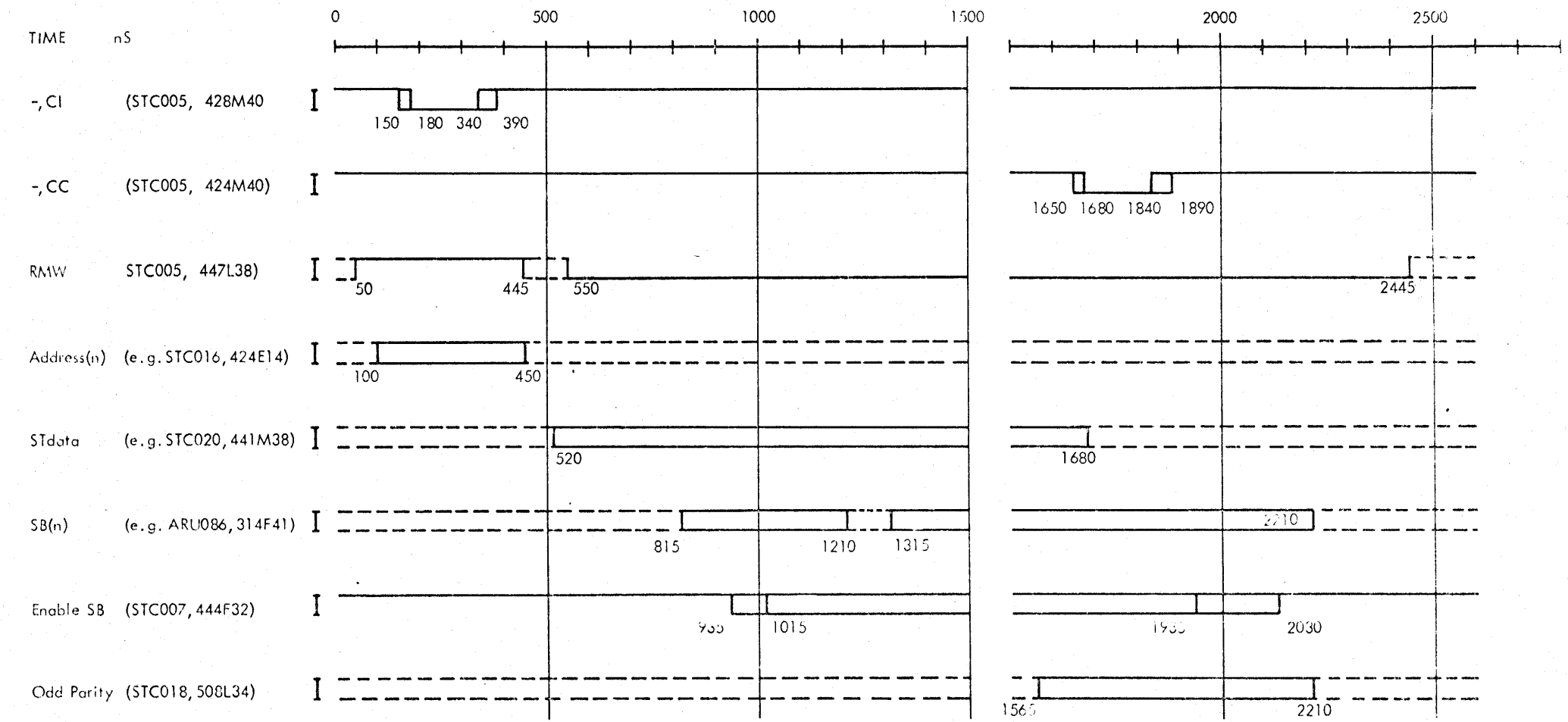
TBhdc AND CORE STORE TIMING FOR HDC WRITE

Timing Chart



V13567 RC4090

TB AND CORE STORE TIMING FOR READ SPLIT - SPLIT WRITE
6 < ADDRESS ≤ WORD LIMIT
Timing Chart



061172PEP 291172MOGK 291172 PEP

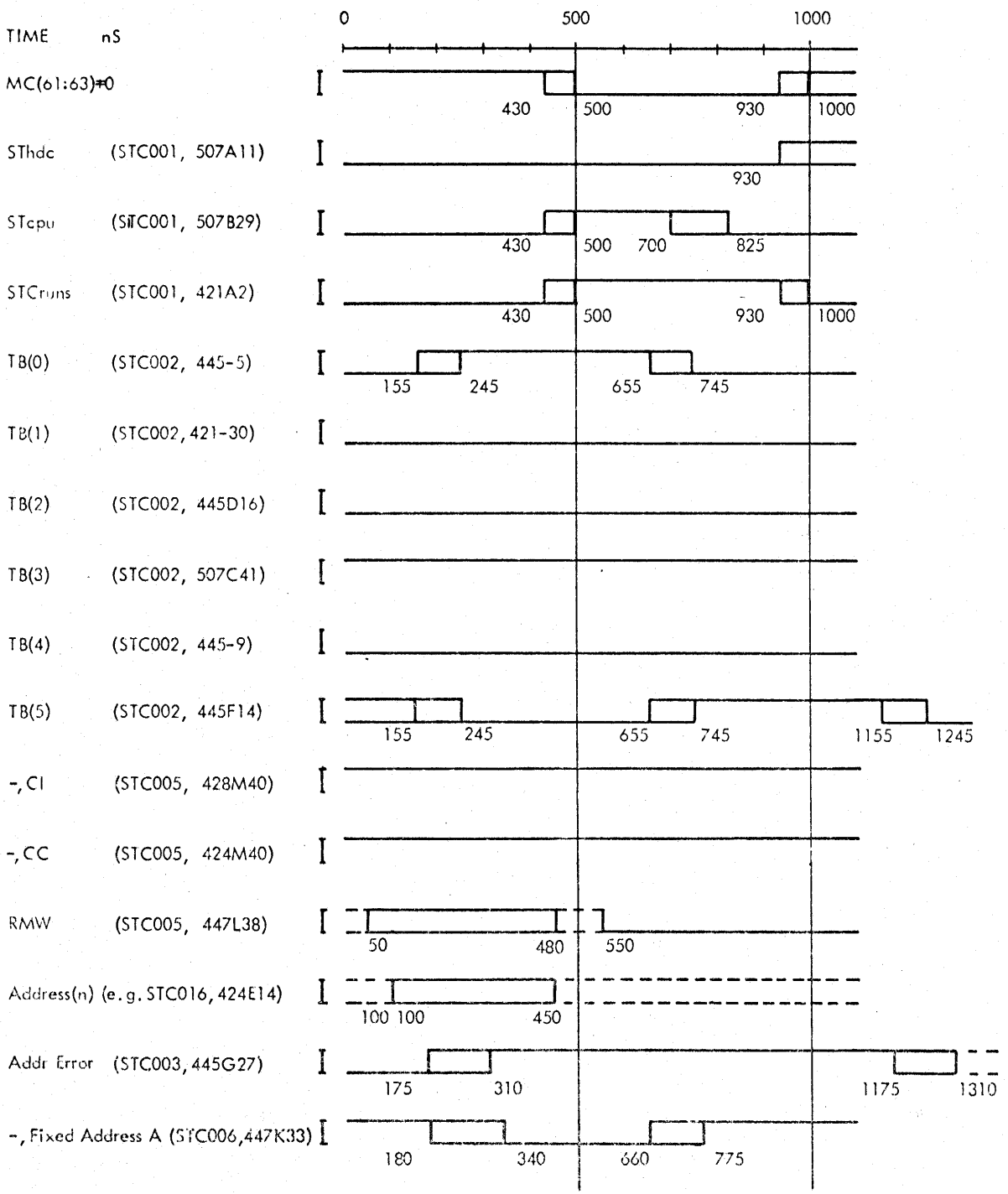
RC4000

V13568

TB AND CORE STORE TIMING FOR READ INSTRUCTION, READ DATA, AND READ SPLIT

ADDRESS > WORD-LIMIT

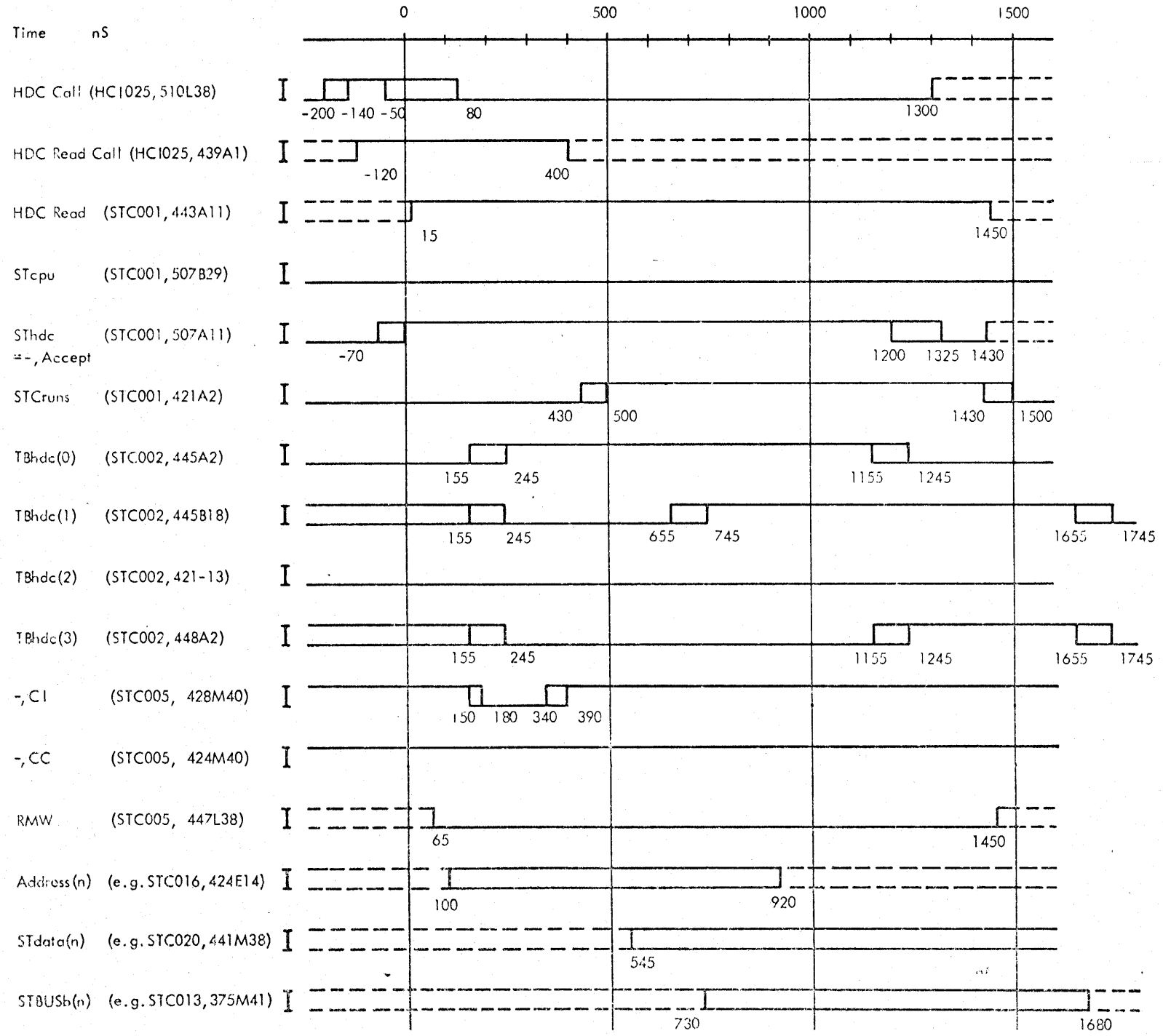
Timing Chart



061172PEP 291172MOGK 291172 PEP

RC4000 V13569 Timing Chart

TBhdc AND CORE STORE TIMING FOR HDC READ



RC 4005 B CENTRAL PROCESSOR

TEGN. Nr.: Dato:

1 RC 4005 B. CENTRAL PROCESSOR:

Interconnection plan:

Basic System with Mini Mass core Store RCSL: 31-D225

Definition af RC 4005 V23399 181272

Part liste

2 CPU 425 kortramme 51-VB1059 ??

* Mekaniske tegninger RCSL: ~~[illegible]~~

* Stregtrådningsplan RCSL:

~~[illegible]~~ RCSL: 31-V1201

Spændingstraadning	V11215	110870
Spændingstraadning 0V og +5V	V1~~[illegible]~~ 13529	120870
Spændingstraadning 0V og +5V	V20970	120870
Spændingstraadning +12V og -6V	V20971	120870
Spændingstrådning 90 Pol Elco	V23397	141272
Spændingstraadning 90 Pol. Elco	V20884	120870
Spændingstraadning 38 Pol. Elco	V20972	120870
Spændingstraadning Stik 1084	V20021	120870

0 Voltledning stik 1014, 1015, 1016, 1017 V23396 141272

Kabelstikplacering CPU 425 V23398 141272

Part liste.

3 CPU 425 PCBA:

PCBA Position List RCSL: 31-D226

Varianter:

RC0888 1/3	V20893	150669
RC090-1/2	V20894	150669
RC0909-1/1	V20895	150669
RC0909 1/2	V20896	150669

* selvstændig mappe

Tegn. Nr.: Dato

4 RC 4005 B Kabler :

Markning V
Partliste

5 MiNi MASS Fanitlager :

Udskiftning af
220V netledning V 23403 171172

Opsparing af kabler
til Mini Mass Core Store V.

6 RC 4005 B Kabinet :

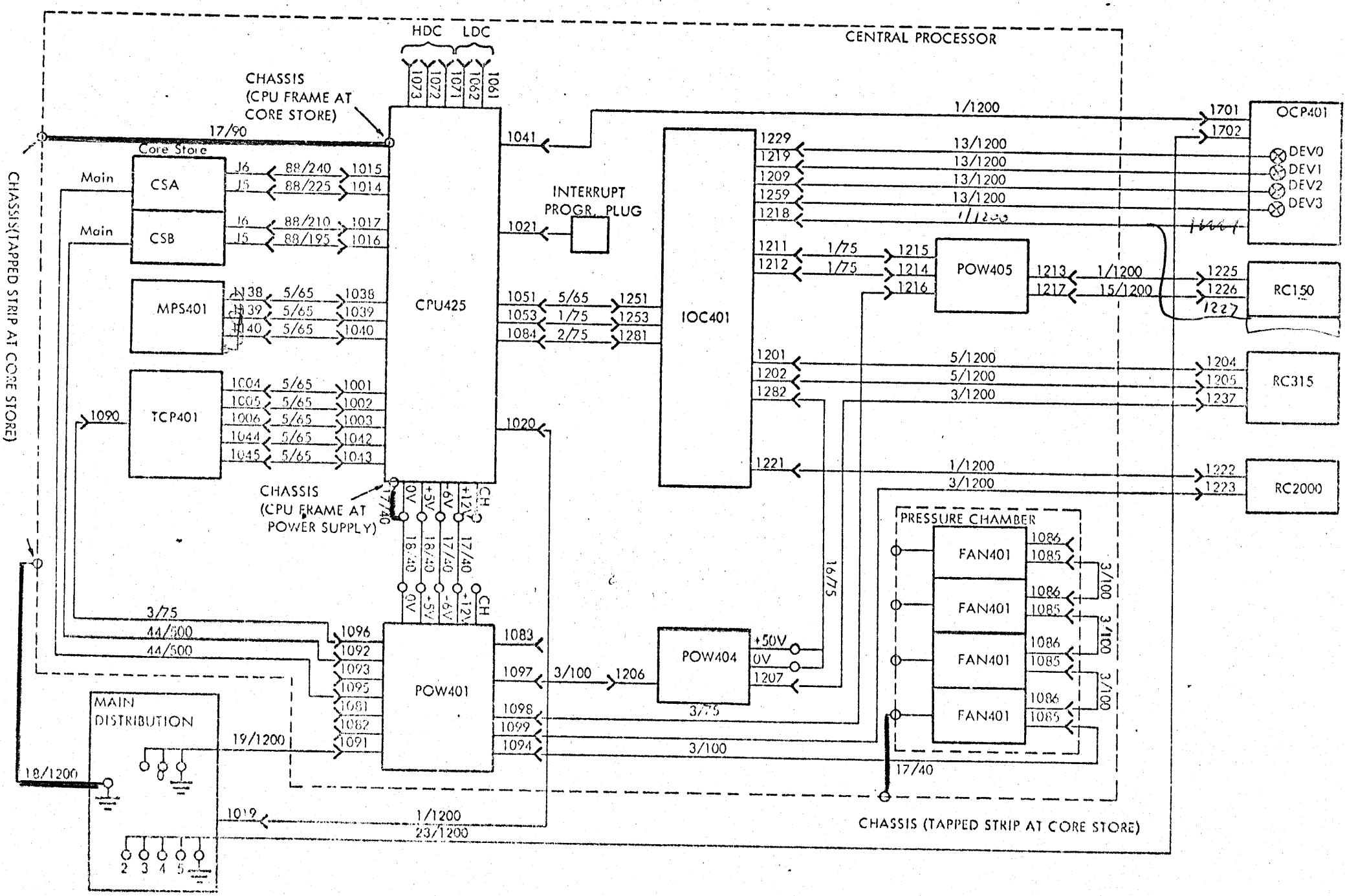
Materialeliste V21443 050570

Opsparingsvinkel for
Mini Mass Core Store V 13573 071272

Placeringstegning for RC 4005 B V
Placeringstegning for RC 4005 B V
Placeringstegning for RC 4005 B V

Dwg No.

INTERCONNECTION PLAN FOR RC 4000 - BASIC SYSTEM WITH MINI-MASS CORE STORE
RC 4000 INSTALLATION:



RC 4005 CENTRAL PROCESSOR

Der eksisterer i dag to udgaver af RC 4005.

RC 4005 A med AMPEX Ferritlager

RC 4005 B med MINI-MASS Ferritlager

Til at producere disse findes følgende produktionsmapper:

RC 4005 CENTRAL PROCESSOR for RC 4005 A (herefter kaldet mappe 1)og

RC 4005 B CENTRAL PROCESSOR for RC 4005 B (herefter kaldet mappe 2).

Produktionsmappen for RC 4005 B (mappe 2) indeholder kun de afsnit fra mappe 1, der er sket ændringer i, samt et afsnit omhandlende ombygning af en RC 4005 A til RC 4005 B.
Følgende opskrift anvendes ved produktion af de forskellige udgaver:

RC 4005 A produceres udelukkende efter papirerne i mappe 1.
RC 4005 B produceres efter papirerne i mappe 1 og 2, således at følgende afsnit i mappe 1 erstattes af følgende afsnit i mappe 2.

Mappe 1	Mappe 2
RC 4005 CENTRAL PROCESSOR	RC 4005 B CENTRAL PROCESSOR
CPU 401 - 408 Kortramme	CPU 425 Kortramme
CPU 401 PCBA	CPU 425 PCBA
RC 4005 Kabler	RC 4005 B Kabler
AMPEX RC ferritlager	MINI-MASS ferritlager
RC 4005 Kabinet	RC 4005 B Kabinet

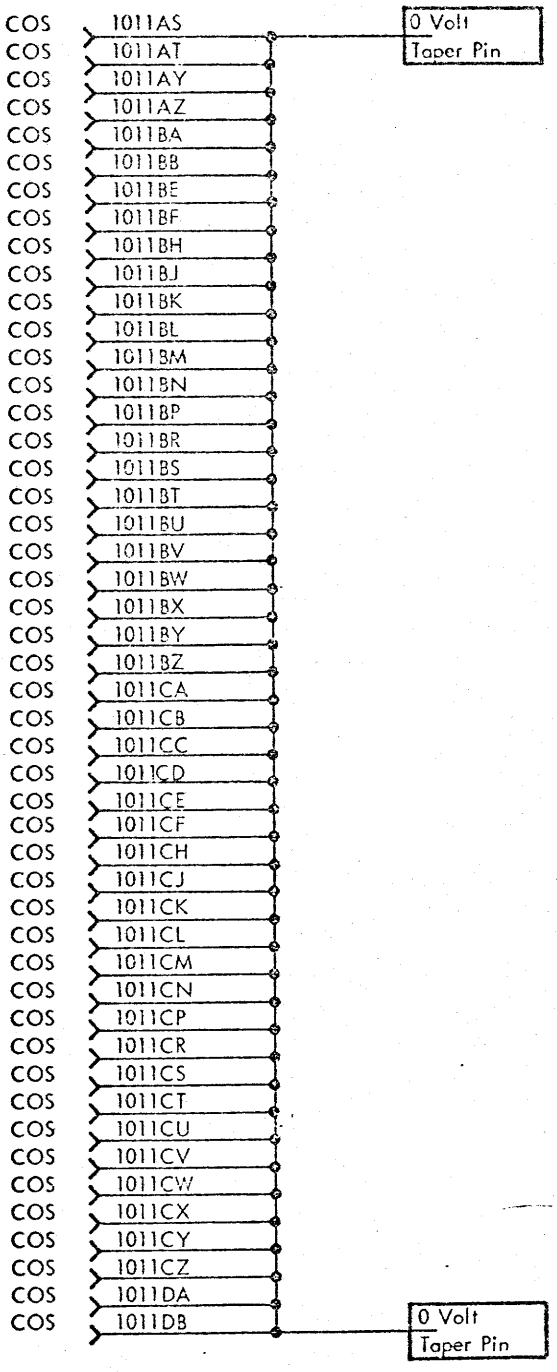
RC 4005 A og RC 4005 B er en produktionsbetegnelse for de to udgaver.
Salgsmæssigt hedder de begge RC 4005 CENTRAL PROCESSOR (ingen ændring).

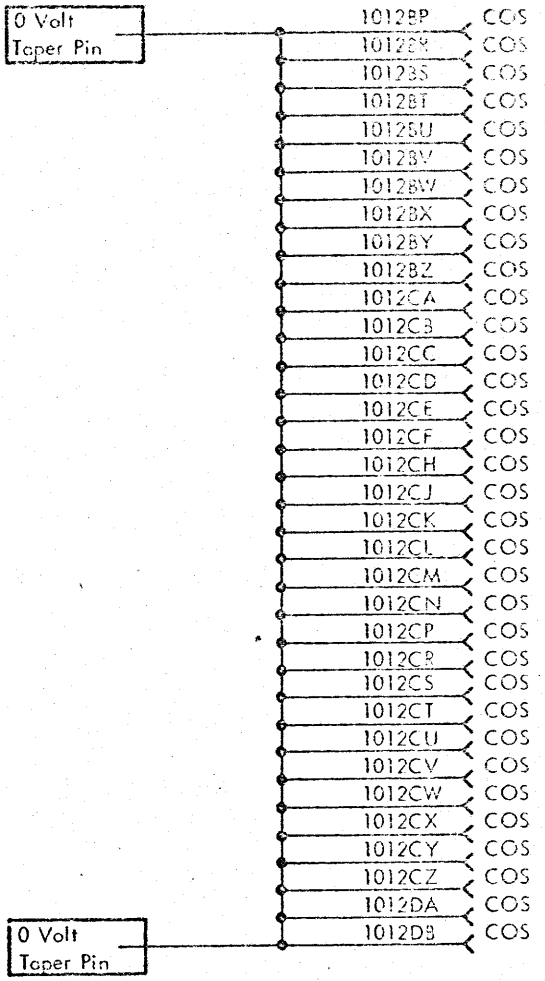
MODIFIKATION AF CPU402/408 TIL CPU425

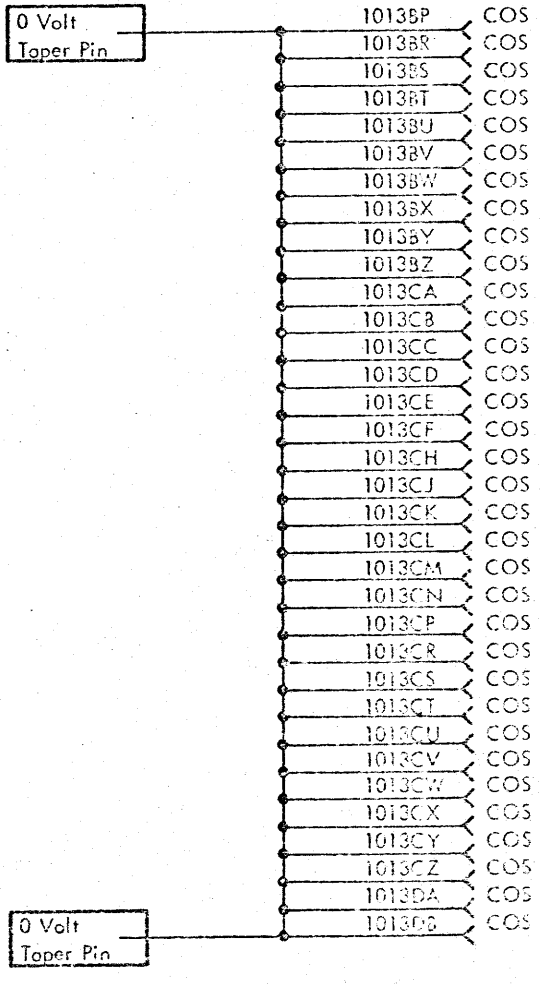
ARBEJDSPLAN

1. Tøm stik 1011, 1012 og 1013 for spændings- og logiktrådning.
   Se tegning V23455
2. Monter ekstra Elco stik, flyt og omnummerer de andre Elco. stik.
   Se tegning V23401 og V23398
3. Foretag spændingstrådning af stik 1014, 1015, 1016 og 1017.
   Se tegning V23396
4. Fjern strengene fra tillægstrådningsplanen til det pågældne anlæg (det afhænger af ferritlagerstørrelsen, hvilken der skal bruges).
5. Foretag trådningsændringer ifølge rettelsestrådningsplan for ombygning af CPU 402/408 til CPU 425.
6. Indsæt de nye printkort i CPU-rammen.
   Se tegning V23400

V23416





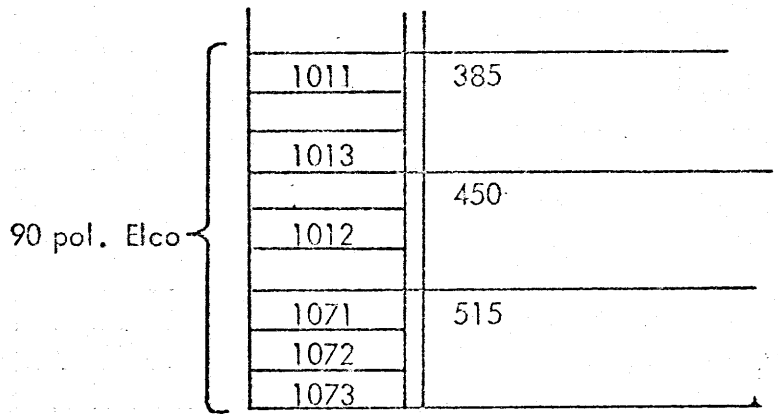


Disse stenge fjernes

CPU 401/408 → CPU 425

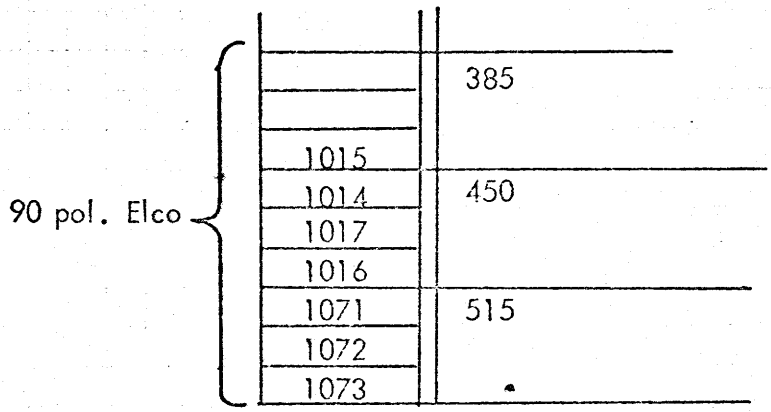
181272 Mos

CPU 401-408



Rammerne er set fra trådsiden.

CPU 425

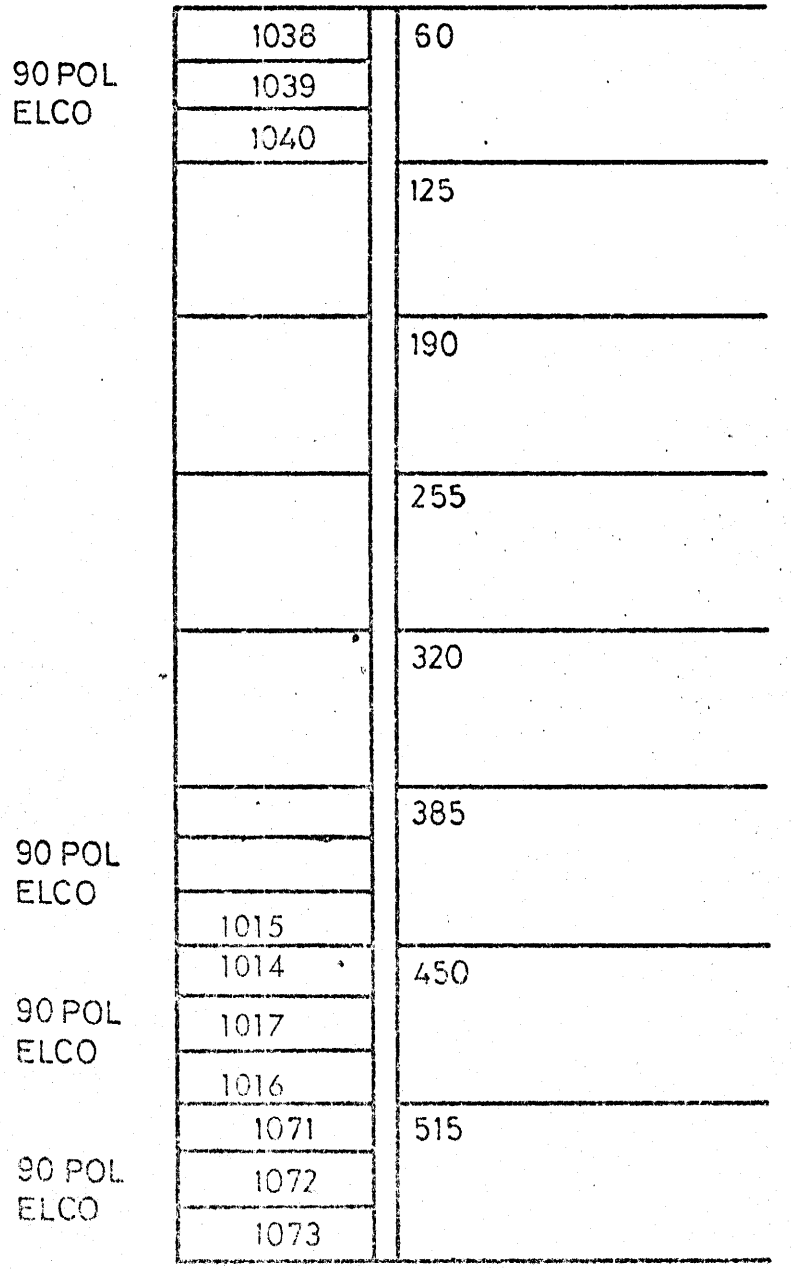


181272 MOJ

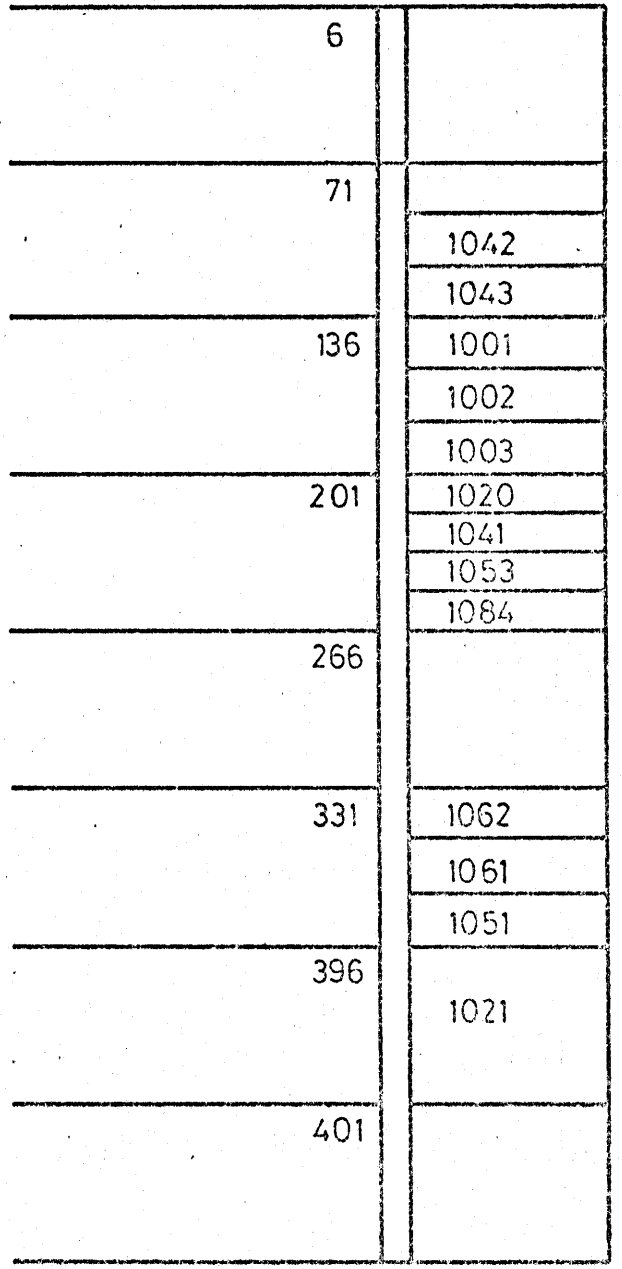
141272 MOJ

RC 4000 KABELSTIKPLACERING CPU 425

V23398



RAMMEN SET FRA TRÅDSIDEN



RC 4000
V2339%

0 Volt trådning i stik 1014, 1015, 1016 og 1017
i CPU425

STIK 1014:

0V	B	AZ	BB	BL	BN	BR	CN	CR			
0V	BF	BJ	BT	BV	BX	BZ	CB	CD	CF	CT	CV

STIK 1015:

0V	B	D	CR	CT	CV	CX
0V	F	AZ	BB	BD	BF	

STIL 1016:

0V	B	AZ	BB	BL	BN	BR	CN	CR			
0V	BF	BJ	BT	BV	BX	BZ	CB	CD	CF	CT	CV

STIK 1017:

0V	B	D	CR	CT	CV	CX
0V	F	AZ	BB	BD	BF	

Forbindelse til 0 Volt sker ved Taper pin til 0 Volt taper pin skinne.
Trådning lægges i 0.25 mm^2 blød tråd
Trådlængde: 0V til kabelstikben 150 mm
kabelstikben til kabelstikben 10 mm

	Ben nr.					
Stik nr.	CW	CX	CY	CZ	DA	DB
1001	0V	0V	+5V	+5V	CH.	CH.
1002					CH.	CH.
1003	0V	0V	+5V	+5V	CH.	CH.
1038	+5V	+5V	+5V	+5V	CH.	CH.
1039	+5V	+5V	+5V	+5V	CH.	CH.
1040	+5V	+5V	+5V	+5V	CH.	CH.
1042	0V	0V	0V	0V	CH.	CH.
1043	0V	0V	0V	0V	CH.	CH.
1051	0V	0V	0V	0V	CH.	CH.
1061	0V	0V	0V	0V	CH.	CH.
1062	0V	0V	0V	0V	CH.	CH.
1071	0V	0V	0V	0V	CH.	CH.
1072	0V	0V	0V	0V	CH.	CH.
1073	0V	0V	0V	0V	CH.	CH.

141272 MOJ

Al trådning lægges i 0,25mm^2 grå/hvid tråd

Forbindelse til 0V sker ved taper pin

Forbindelse til +5V sker ved lodning til +5V plan

Forbindelse til CH (stel sker ved kabelsko Amp rød som forbindes til nærmeste stag til opspænding af 41 pol Elco stik. DA og DB klemmes i samme kabelsko for hvert stik.

Spændingstrådning af 90 pol. Elco stik i CPU425

Følgende ekstra printkort skal benyttes ved ombygning af CPU 401-408 til CPU 425

Pos.	PCBA
CPU425	RC2072-1
CPU427	RC0834-1
CPU442	RC0890-1
CPU450	RC2073-1

181272 MOJ

UDSKIFTNING AF AMPEX CORE STORE MED MINI-MASS CORE STORE.

ARBEJDSPLAN.

1. Udskift powerkabel i MINI-MASS CORE STORE power supply. Se tegning V23403
2. Fjern alle kabler i forbindelse med CORE STORE (AMPEX).
3. Udtag Ampex power supply og core store modul(er).
4. Fjern teleskopskinner.
5. Monter opspændingsvinkler for MINI-MASS CORE STORE så højt oppe som muligt.
6. Monter MINI-MASS skufferne.
7. Opspænd kabler i kabelaflastninger.

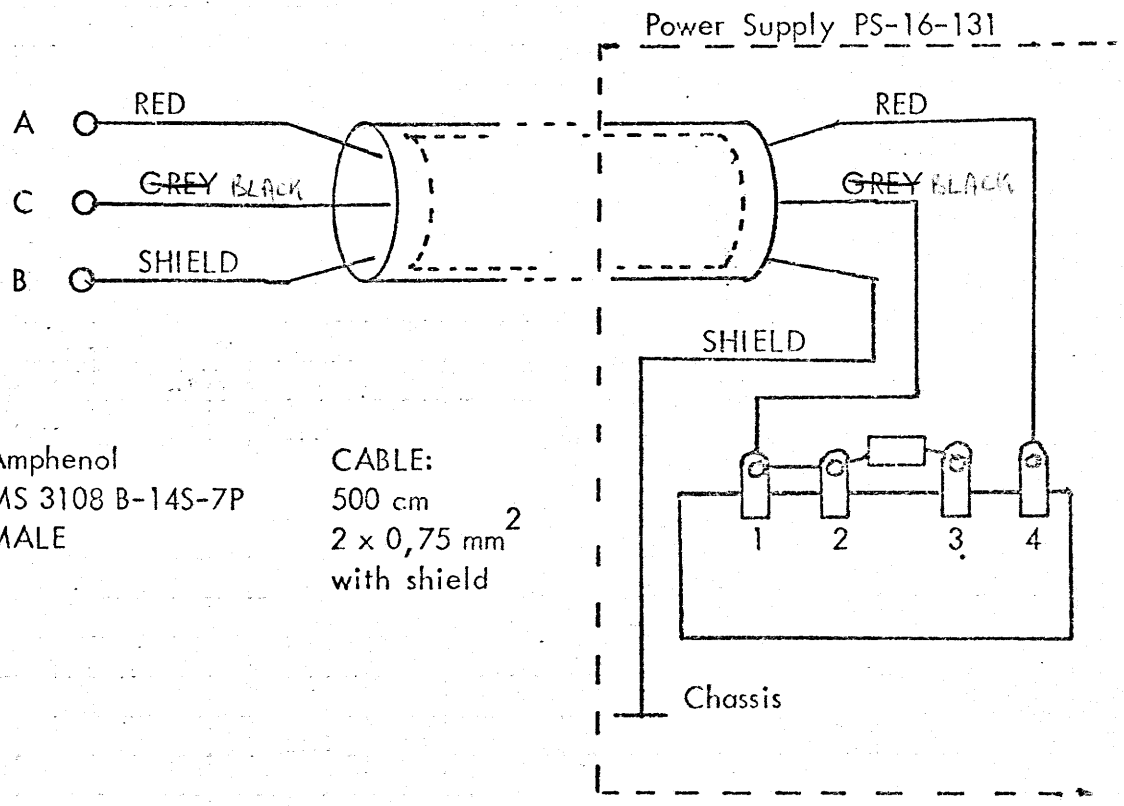
} Se tegning V23454

8. Kablerne kan nu forbindes og core store modulerne indsættes. Se tegning V23402

UDSKIFTNING AF 220 VOLT NETLEDNING I MINI-MASS CORE STORE

Fra producentens side er hvert lager forsynet med en ca. 1.5 m lang netledning afsluttet med et specielt amerikansk stik med flade ben. Denne netledning fjernes ved demontering i power supply boksen og gemmes i den tomme emballage.

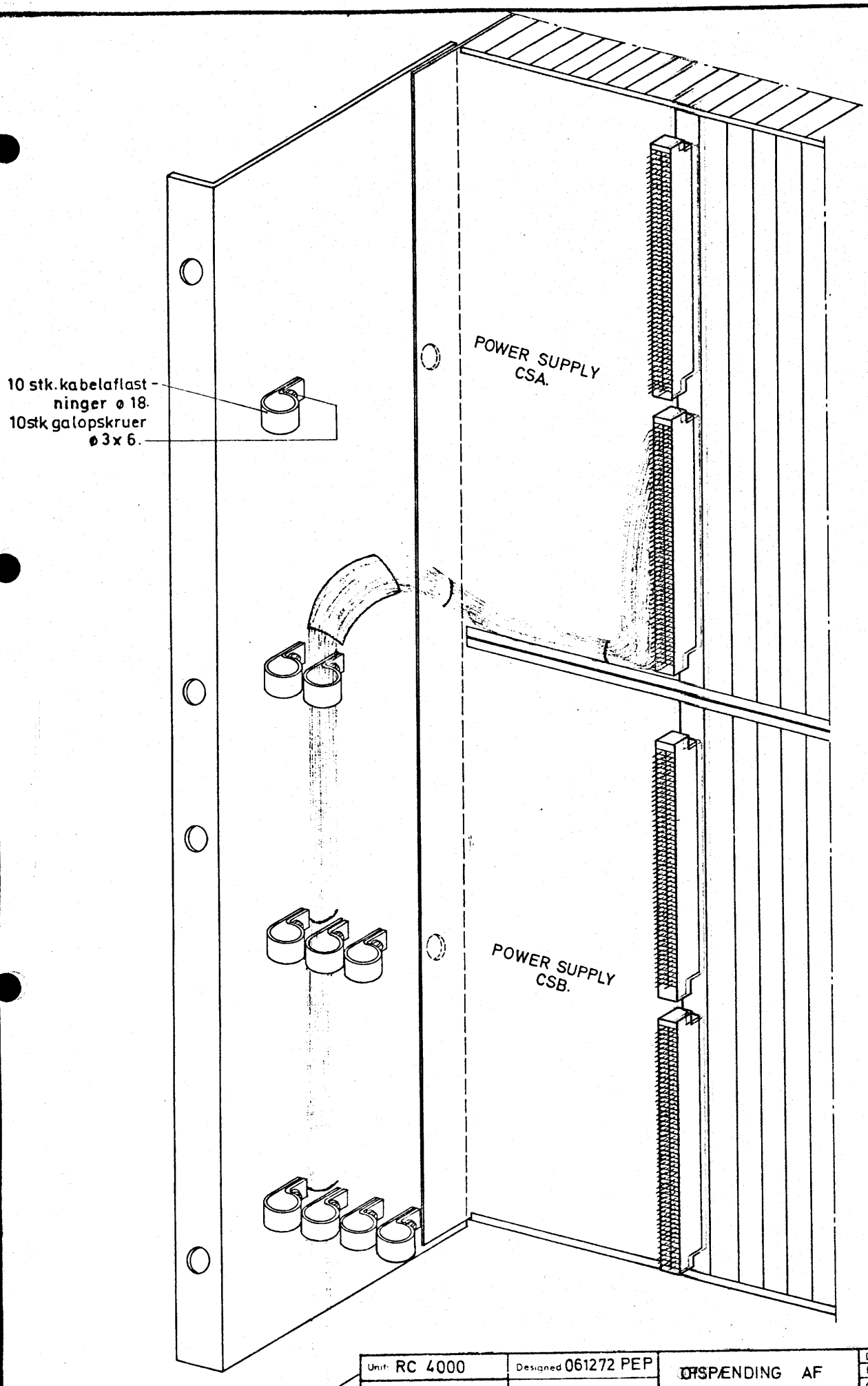
Herefter tilsluttes en ny netledning, type 44, efter følgende trådningsdiagram:



Amphenol
MS 3108 B-14S-7P
MALE

CABLE:
500 cm
2 x 0,75 mm^2
with shield

171172 PEP 181272 MOJ



Unit: RC 4000	Designed 061272 PEP	OPSPÆNDING AF KABLER TIL MINI-MASS FERRITLAGER.	Drawing No V 2245A
REGNECENTRALEN	Approved		Drawn by SA
	Checked		Checked 030473
	Last Revision		1 Sheets | Sheet 1

Følgende kabler skal anvendes i forbindelse med MINI-MASS Core Store. Kablerne skal mærkes som her anført.

Kabeltype	Connector 1	Connector 2
88/195 cm	1016 (Elco)	J5 CSB (Viking)
88/210 cm	1017 (Elco)	J6 CSB (Viking)
88/225 cm	1014 (Elco)	J5 CSA (Viking)
88/240 cm	1015 (Elco)	J6 CSA (Viking)

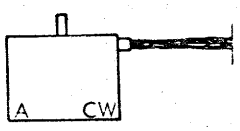
Følgende kabler skal ikke benyttes mere.

1 stk.	11/500	Powerkabel
3 stk.	12/300	Datakabler

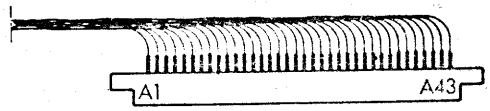
181272 MOJ

Connector I. Elco plug 8016-090-704
Connector II: Viking ~~2~~ 3VH43/1JN5
Cable :

I PIN	WIRE	II PIN	I PIN	WIRE	II PIN	I PIN	WIRE	PIN
A	rød	B1	AM	rød	B17	BY	rød	B33
B	blå	A1	AN	blå	A17	BZ	blå	A33
C	rød	B2	AP	rød	B18	CA	rød	B34
D	blå	A2	AR	blå	A18	CB	blå	A34
E	rød	B3	AS	rød	B19	CC	rød	B35
F	blå	A3	AT	blå	A19	CD	blå	A35
H	rød	B4	AU	rød	B20	CE	rød	B36
J	blå	A4	AV	blå	A20	CF	blå	A36
K	rød	B5	AW	rød	B21	CH	rød	B37
L	blå	A5	AX	blå	A21	CJ	blå	A37
M	rød	B6	AY	rød	B22	CK	rød	B38
N	blå	A6	AZ	blå	A22	CL	blå	A38
P	rød	B7	BA	rød	B23	CM	rød	B39
R	blå	A7	BB	blå	A23	CN	blå	A39
S	rød	B8	BC	rød	B24	CP	rød	B40
T	blå	A8	BD	blå	A24	CR	blå	A40
U	rød	B9	BE	rød	B25	CS	rød	B41
V	blå	A9	BF	blå	A25	CT	blå	A41
W	rød	B10	BH	rød	B26	CU	rød	B42
X	blå	A10	BJ	blå	A26	CV	blå	A42
Y	rød	B11	BK	rød	B27	CW	rød	B43
Z	blå	A11	BL	blå	A27	CX	blå	A43
AA	rød	B12	BM	rød	B28	CY		
AB	blå	A12	BN	blå	A28	CZ		
AC	rød	B13	BP	rød	B29	DA		
AD	blå	A13	BR	blå	A29	DB		
AE	rød	B14	BS	rød	B30			
AF	blå	A14	BT	blå	A30			
AH	rød	B15	BU	rød	B31			
AJ	blå	A15	BV	blå	A31			
AK	rød	B16	BW	rød	B32			
AL	blå	A16	BX	blå	A32			



Connector I



Connector II

Kabeltype 88/ cm.

091072PEP 061172MOGK

V13509

CP425

PCBA Position List

Pos.	PCBA
CPU25	RC0839-1
CPU26	RC0839-1
CPU27	RC0839-1
CPU28	RC0839-1
CPU30	RC0861-1
CPU31	RC0861-1
CPU32	RC0893-3
CPU34	RC0852-1
CPU36	RC0837-1
CPU37	RC0900-1/2
CPU38	RC0837-1
CPU39	RC0837-1
CPU40	RC0872-1
CPU41	RC0860-2
CPU42	RC0860-2
CPU43	RC0872-1
CPU44	RC0872-1
CPU45	RC0834-1
CPU46	RC0837-1
CPU47	RC0834-1
CPU48	RC0839-1
CPU49	RC0872-1
CPU50	RC0834-1
CPU51	RC0846-1
CPU52	RC0872-1
CPU53	RC0846-1
CPU54	RC0846-1
CPU55	RC0854-1
CPU56	RC0846-1
CPU57	RC0854-1
CPU58	RC0872-1
CPU59	RC0872-1
CPU60	RC0854-1
CPU86	RC0888-1/3
CPU87	RC0909-1/1
CPU88	RC0839-1
CPU89	RC0834-1
CPU90	RC0839-1
CPU91	RC0836-1
CPU92	RC0834-1
CPU93	RC0861-1
CPU94	RC0839-1
CPU95	RC0838-1
CPU96	RC0861-1
CPU97	RC0861-1
CPU99	RC0837-1
CPU100	RC0837-1

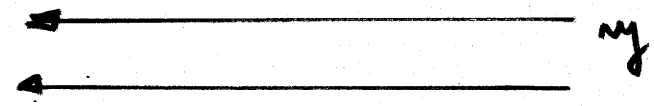
Pos.	PCBA
CPU101	RC0837-1
CPU102	RC0839-1
CPU103	RC0834-1
CPU104	RC0846-1
CPU106	RC0834-1
CPU107	RC0854-1
CPU108	RC0854-1
CPU109	RC0846-1
CPU110	RC0854-1
CPU111	RC0846-3
CPU112	RC0854-1
CPU113	RC0854-1
CPU114	RC0854-1
CPU115	RC0854-1
CPU116	RC0870-1
CPU117	RC0870-1
CPU118	RC0870-1
CPU119	RC0870-1
CPU120	RC0870-1
CPU121	RC0870-1
CPU122	RC0870-1
CPU123	RC0870-1
CPU124	RC0870-1
CPU125	RC0870-1
CPU146	RC0835-1
CPU147	RC0834-1
CPU148	RC0861-1
CPU149	RC0836-1
CPU150	RC0834-1
CPU151	RC0839-1
CPU152	RC0835-1
CPU153	RC0845-1
CPU154	RC0861-1
CPU155	RC0845-1
CPU156	RC0845-1
CPU157	RC0834-1
CPU158	RC0835-1
CPU159	RC0835-1
CPU160	RC0862-1
CPU161	RC0845-1
CPU162	RC0834-1
CPU164	RC0845-1
CPU165	RC0845-1
CPU166	RC0862-1
CPU167	RC0872-1
CPU168	RC0838-1
CPU169	RC0836-1
CPU170	RC0879-1
CPU171	RC0836-1
CPU172	RC0835-1
CPU173	RC0862-1
CPU174	RC0836-1

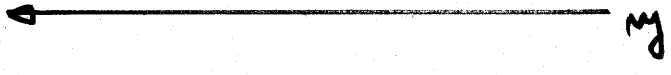
Pos.	PCBA
CPU175	RC0834-1
CPU176	RC0839-1
CPU177	RC0845-1
CPU178	RC0862-1
CPU179	RC0847-1
CPU180	RC0838-1
CPU181	RC0835-1
CPU182	RC0835-1
CPU183	RC0862-1
CPU184	RC0847-1
CPU185	RC0845-1
CPU186	RC0862-1
CPU187	RC0834-1
CPU188	RC0839-1
CPU189	RC0835-1
CPU190	RC0834-1
CPU206	RC0834-1
CPU207	RC0861-1
CPU208	RC0838-1
CPU209	RC0834-1
CPU210	RC0839-1
CPU211	RC0838-1
CPU212	RC0836-1
CPU213	RC0839-1
CPU214	RC0839-1
CPU215	RC0857-1
CPU216	RC0857-1
CPU217	RC0857-1
CPU218	RC0836-1
CPU219	RC0857-1
CPU220	RC0857-1
CPU221	RC0857-1
CPU222	RC0847-1
CPU223	RC0857-1
CPU224	RC0857-1
CPU225	RC0857-1
CPU226	RC0847-1
CPU227	RC0857-1
CPU229	RC0857-1
CPU230	RC0857-1
CPU231	RC0834-1
CPU232	RC0834-1
CPU233	RC0838-1
CPU234	RC0836-1
CPU235	RC0929-1
CPU236	RC0836-1
CPU237	RC0836-1
CPU238	RC0857-1
CPU239	RC0857-1
CPU240	RC0857-1
CPU241	RC0838-1
CPU242	RC0857-1

Pos.	PCBA
CPU243	RC0857-1
CPU244	RC0857-1
CPU245	RC0834-1
CPU246	RC0857-1
CPU247	RC0857-1
CPU248	RC0857-1
CPU249	RC0839-1
CPU250	RC0857-1
CPU251	RC0857-1
CPU252	RC0857-1
CPU253	RC0839-1
CPU254	RC0858-1
CPU255	RC0834-1
CPU266	RC0899-1
CPU267	RC0899-1
CPU268	RC0899-1
CPU271	RC0899-1
CPU272	RC0836-1
CPU275	RC0894-1
CPU276	RC0894-1
CPU278	RC0886-1
CPU279	RC0872-1
CPU280	RC0834-1
CPU281	RC0836-1
CPU282	RC0868-1
CPU283	RC0859-1
CPU284	RC0868-1
CPU285	RC0844-1
CPU286	RC0844-1
CPU287	RC0834-1
CPU288	RC0859-1
CPU289	RC0868-1
CPU290	RC0844-1
CPU291	RC0834-1
CPU292	RC0844-1
CPU294	RC0844-1
CPU295	RC0868-1
CPU296	RC0859-1
CPU297	RC0858-1
CPU298	RC0838-1
CPU299	RC0846-3
CPU300	RC0834-1
CPU301	RC0836-1
CPU302	RC0858-1
CPU303	RC0836-1
CPU304	RC0844-1
CPU305	RC0868-1
CPU306	RC0845-1
CPU307	RC0844-1
CPU308	RC0847-1
CPU309	RC0844-1
CPU310	RC0868-1

Pos.	PCBA
CPU311	RC0836-1
CPU312	RC0858-1
CPU313	RC0844-1
CPU314	RC0845-1
CPU315	RC0868-1
CPU316	RC0844-1
CPU317	RC0845-1
CPU318	RC0861-1
CPU319	RC0835-1
CPU320	RC0835-1
CPU333	RC0897-1
CPU334	RC0897-1
CPU335	RC0839-1
CPU336	RC0897-1
CPU338	RC0838-1
CPU339	RC0834-1
CPU341	RC0858-1
CPU342	RC0897-1
CPU343	RC0839-1
CPU344	RC0858-1
CPU345	RC0834-1
CPU347	RC0890-1
CPU349	RC0859-1
CPU350	RC0868-1
CPU351	RC0845-1
CPU352	RC0858-1
CPU353	RC0858-1
CPU354	RC0859-1
CPU355	RC0868-1
CPU356	RC0838-1
CPU357	RC0858-1
CPU359	RC0845-1
CPU360	RC0859-1
CPU361	RC0868-1
CPU362	RC0858-1
CPU363	RC0836-1
CPU364	RC0834-1
CPU365	RC0834-1
CPU366	RC0834-1
CPU367	RC0859-1
CPU368	RC0868-1
CPU369	RC0845-1
CPU370	RC0834-1
CPU371	RC0858-1
CPU372	RC0858-1
CPU373	RC0839-1
CPU374	RC0836-1
CPU375	RC0834-1
CPU376	RC0834-1
CPU377	RC0846-3
CPU378	RC0839-1
CPU379	RC0858-1

Pos.	PCBA
CPU380	RC0858-1
CPU381	RC0861-1
CPU382	RC0834-1
CPU383	RC0858-1
CPU384	RC0858-1
CPU385	RC0836-1
CPU396	RC0834-1
CPU397	RC0839-1
CPU398	RC0839-1
CPU399	RC0839-1
CPU400	RC0869-1
CPU401	RC0869-1
CPU402	RC0869-1
CPU403	RC0869-1
CPU404	RC0869-1
CPU405	RC0869-1
CPU406	RC0869-1
CPU407	RC0869-1
CPU408	RC0869-1
CPU409	RC0869-1
CPU410	RC0869-1
CPU411	RC0869-1
CPU412	RC0836-1
CPU413	RC0834-1
CPU414	RC0838-1
CPU415	RC0858-1
CPU416	RC0839-1
CPU418	RC0894-1
CPU419	RC0891-1
CPU421	RC0835-1
CPU422	RC0858-1
CPU425	RC2072-1
CPU424	RC0890-1
CPU427	RC0834-1
CPU426	RC0839-1
CPU428	RC0890-1
CPU430	RC0844-1
CPU431	RC0844-1
CPU432	RC0836-1
CPU433	RC0834-1
CPU434	RC0839-1
CPU435	RC0834-1
CPU436	RC0836-1
CPU437	RC0847-1
CPU438	RC0834-1
CPU439	RC0847-1
CPU440	RC0835-1
CPU441	RC0891-1
CPU442	RC0890-1
CPU443	RC0837-1
CPU444	RC0839-1
CPU445	RC0844-1





Pos.	PCBA
CPU446	RC0834-1
CPU447	RC0834-1
CPU448	RC0835-1
CPU449	RC0891-1
CPU450	RC2073-1
CPU461	RC0899-1
CPU462	RC0899-1
CPU463	RC0899-1
CPU465	RC0897-1
CPU466	RC0834-1
CPU467	RC0844-1
CPU468	RC0899-1
CPU469	RC0897-1
CPU470	RC0897-1
CPU471	RC0890-1
CPU472	RC0834-1
CPU473	RC0839-1
CPU474	RC0839-1
CPU475	RC0838-1
CPU476	RC0838-1
CPU477	RC0894-1
CPU478	RC0894-1
CPU479	RC0844-1
CPU480	RC0897-1
CPU481	RC0897-1
CPU482	RC0834-1
CPU483	RC0897-1
CPU484	RC0839-1
CPU485	RC0899-1
CPU486	RC0894-1
CPU487	RC0894-1
CPU489	RC0834-1
CPU490	RC0844-1
CPU491	RC0835-1
CPU492	RC0894-1
CPU493	RC0899-1
CPU494	RC0894-1
CPU495	RC0909-1/2
CPU496	RC0894-1
CPU497	RC0897-1
CPU498	RC0894-1
CPU499	RC0890-1
CPU500	RC0897-1
CPU501	RC0836-1
CPU502	RC0836-1
CPU503	RC0834-1
CPU504	RC0894-1
CPU505	RC0839-1
CPU506	RC0839-1
CPU507	RC0837-1
CPU508	RC0890-1
CPU510	RC0834-1
CPU511	RC0839-1

Pos.	PCBA
CPU512	RC0837-1
CPU513	RC0837-1
CPU514	RC0838-1
CPU515	RC0838-1

PARTLISTE

benævnelse	antal	nr
TRÅD 0.25mm² GRÅ/HVID	1600	11915
KABEL 4,0 MM² SORT	12	12019
KABEL 6,0 MM² SORT	3	12100
TRÅD PFR 2 × 0.22 MM² RØD/BLÅ	800	12116
AMP KABELSKO 31890 (0.25 - 1.6)	40	13301
AMP KABELSKO 130171 (2.7 - 6.6)	15	13307
ELCO RECEPT 8016-038-000-007	4	13712
ELCO RECEPT 8017-130-000-007	1	13718
ELCO RECEPT M. LANGE STYR 7052-41	432	13807
ELCO CRIMP (BÅND) 8017-0323	9	13808
AMP TAPER PIN 41662 FORSØLVET	2500	14912
ELCO RECEPT 8016-090-707	18	36406

DEMO. 22/3-73 HØJ

benævnelse			blad
CPU 425 KORTRAMME	DKA Nr.	V 23452	

STANDARD MEMORIES
INCORPORATED
SUBSIDIARY OF APPLIED MAGNETICS CORP.

Telephone (714) 540-3605 2221 South Anne Street • Santa Ana, California • 92704

September 26, 1972

Mr. P. E. Pedersen
Regnencentralen A. G.

c/o Roger Laureys
Applied Magnetics Belgium
Industriezone-Raadsherenstraat
2300 Turnhout
Belgium

Dear Mr. Pedersen:

Per your request, I will define the selection criteria for all unspecified resistor values in the Standard Memories ECOM® F Memory System. Attached to this letter are the MM-110 Test Specification, a typical MM-110 Test Report, the CM10 Schematic, and the PS4-32 Schematic to clarify the discussion.

1. MM-110

a) R8 and R13, located in the sense amplifier threshold circuit, were provided for early in the MM-110 design phase to permit compensation for sense amplifier lot variations. This has since proven not to be necessary. Note that the MM-110 Test Spec., sheet 2, para. 5.5, specifies that the voltage at the threshold adj. test point, J1 pin 48, shall be +2.21 ±.05V for all memory modules.

R10 is used to hold the sense amp threshold constant as a function of the number of bit circuits present on each MM-110 version. See the CM-10 Schematic, sheet 1, "Assy. Dash No. Table" (upper right corner of page) for the R10 value. Note that the 18 bit version does not use R10.

b) R71 and R74 determine sense amplifier strobe position and duration, respectively. R71 is adjusted to optimize the signal to noise or "1" to "0" operating margin. R71 is selected in the SMI Test Dept. such that the requirements of the MM-110 Test Spec., para. 5.8.1, are exceeded. R71 values are typically between 4.7K and 15K.

b) (cont'd.)

R74 is selected to meet the requirements of para. 5.3. Typical values are 6.8K, 10K or not installed.

c) R39, R40, R41, and R42 are provided in the XY drive current source temperature compensation network to accommodate variations in core type and lot characteristics. Since all 18 mil cores used by SMI have the same temperature coefficient, trim resistors are seldom required (less than 5% of all new modules shipped). The MM-110 Test Spec., para. 5.6, lists the nominal temperature tracking characteristic. The current margin requirements of para. 5.9 must be exceeded by all memory modules.

Designation	Function	Type Value, If Required
R39	Lowers drive, all temps.	33K, 47K
R40	Raises drive, all temps.	33K, 47K
R41	Lowers high temp. drive	1K, 2.2K
R42	Lowers low temp. drive	1K, 2.2K

2. PS4-32

a) R11, R20, R21, and R28 are provided to permit adjustment of the current limit points for each power supply output. The power supply is tested to the following current limit criteria:

Output	Resistor	Current Limit
+5V	R11	17A to 20A
+15V	R20, R21	15A to 17.5A
-15V	R28	1.7A to 2.0A

I sincerely hope the above information meets your requirements. If not, we at Standard Memories, Inc. would welcome any further questions.

Respectfully yours,

STANDARD MEMORIES, INC.

Ernest F. Worley

Ernest F. Worley, Manager
Memory Products Engineering

EFW/dce

Attach.

cc: J. DeVine - SMI, Florida
D. Ray - SMI- Florida

1.0 TITLE

1.1 Test Specification MM-110 ECOM® F Memory Module

2.0 SCOPE

2.1 This document establishes the electrical test requirements of the ECOM® F memory module, MM-110.

3.0 GENERAL REQUIREMENTS

3.1 Test results for all units subject to this specification shall be recorded in sufficient detail to certify compliance to this specification.

3.2 All parameters not specifically defined herein shall be controlled to current best commercial standards.

3.3 The test conditions and signal response limits are stated as absolute values. In an actual testing situation, test equipment characteristics must be taken into consideration.

3.4 All logic pulse timing measurements shall be referenced to the +1.5 volt level of the logic pulse edge.

4.0 TEST CONDITIONS

4.1 The test conditions listed below are nominal for the module and are applicable unless otherwise specified in paragraph 5.0.

4.1.1 Ambient Temperature: 25° C

4.1.2 Test Cycle Time: 750ns

4.1.3 Supply Voltages: +15V, -15V, +5V

DRAWN E. Worley	11/12/71	TEST SPECIFICATION MM-110 ECOM® F MEMORY MODULE			
CHECKED A. EGAN	11/12/71				
APPROVED	11/12/71				
STANDARD MEMORIES SANTA ANA, CALIF.		SIZE A	CODE IDENT 29737	NUMBER SC1523	REV A
		SCALE	Form F-011271	SHEET 1 of 4	

4.1.4 Test data patterns shall include: All Ones, All Zeros, Worst Pattern, Compliment of Worst Pattern, and Address. Worst Pattern address for the MM-110 is characterized by the input address relationship Address 0 ⊕ Address 8.

4.1.5 SA, SB, and $\overline{\text{DATA}}$ $\overline{\text{SAVE}}$ inputs: +5V.

4.1.6 READ pulse input: 200ns duration.

4.1.7 WRITE pulse input: 200ns duration, leading edge of WRITE to be 100ns later than trailing edge of READ.

4.1.8 $\overline{\text{MD}}$ and $\overline{\text{DATA READY}}$ termination: 220Ω to 330Ω pull-up to +5V.

5.0 PERFORMANCE REQUIREMENTS

5.1 The $\overline{\text{MD}}$ output pulse ("1" output) duration shall be 100ns minimum for all bits.

5.2 Access time, measured from the leading edge of the READ pulse to the leading edge of the $\overline{\text{MD}}$ pulse, shall be 250ns maximum for all bits.

5.3 The $\overline{\text{DATA READY}}$ pulse duration shall be 50ns ± 5ns.

5.4 With worst pattern stored in memory, attempt to write the complement of worst pattern into memory with the SA, SB, and $\overline{\text{DATA SAVE}}$ inputs grounded (each, one at a time). Worst pattern shall then be read from memory without error.

5.5 The THRESHOLD ADJ. output shall be + 2.21V ±0.05V.

5.6 The I ADJUST output shall be as listed below:

25° C: 2.65V ±0.1V
0° C: 3.0V ±0.1V
60° C: 2.3V ±0.1V

5.7 The memory shall operate without error with the +5V supply varied between +4.5V and 5.5V at 25° C, 0° C and 60° C.

5.8 Signal/Noise Margin

5.8.1 The memory shall operate without error with the THRESHOLD ADJ. input varied externally as indicated below:

25^{o} C: 1.3V to 3.1V
0^{o} C: 1.5V to 2.9V
60^{o} C: 1.5V to 2.9V

5.9 Current Margin (Shmoo) Tests:

5.9.1 Shmoo tests shall be conducted by varying the XY* and INHIBIT supply voltages at 25^{o}C, 0^{o}C, and 60^{o}C. The error point plots shall be everywhere outside the shaded areas shown in Fig. 1.

* The +15V and -15V XY supplies must be varied together in absolute magnitude.

5.10 The memory shall, while operating, be subjected to mechanical vibration of suffiecient intensity to determine if intermittent conditions exist.

5.11 The memory shall be tested in accordance with "Temperature Cycle/Burn-In Requirements, SC1233" paragraph 4.0.

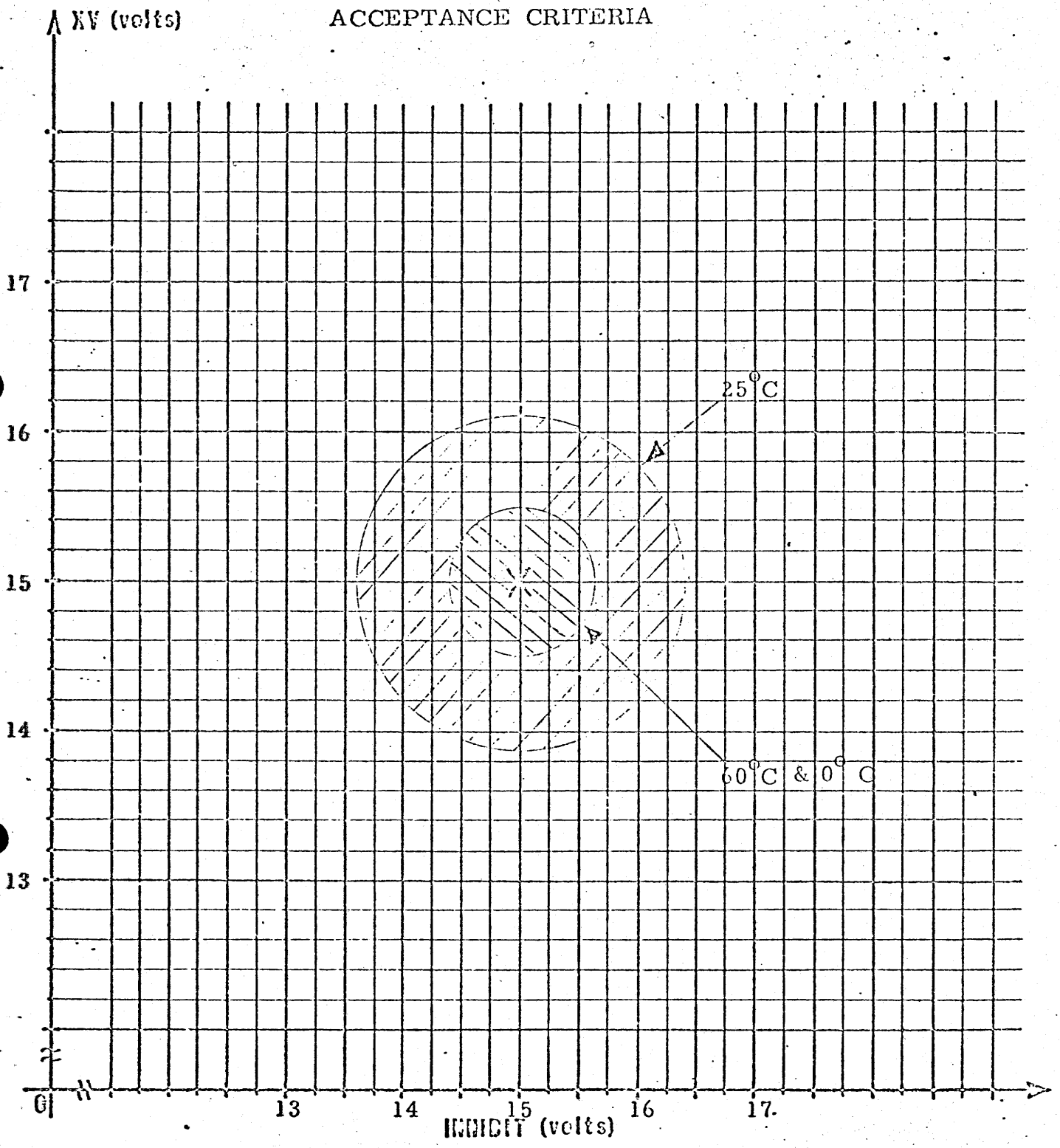
SHMOO DIAGRAM

Fig. I

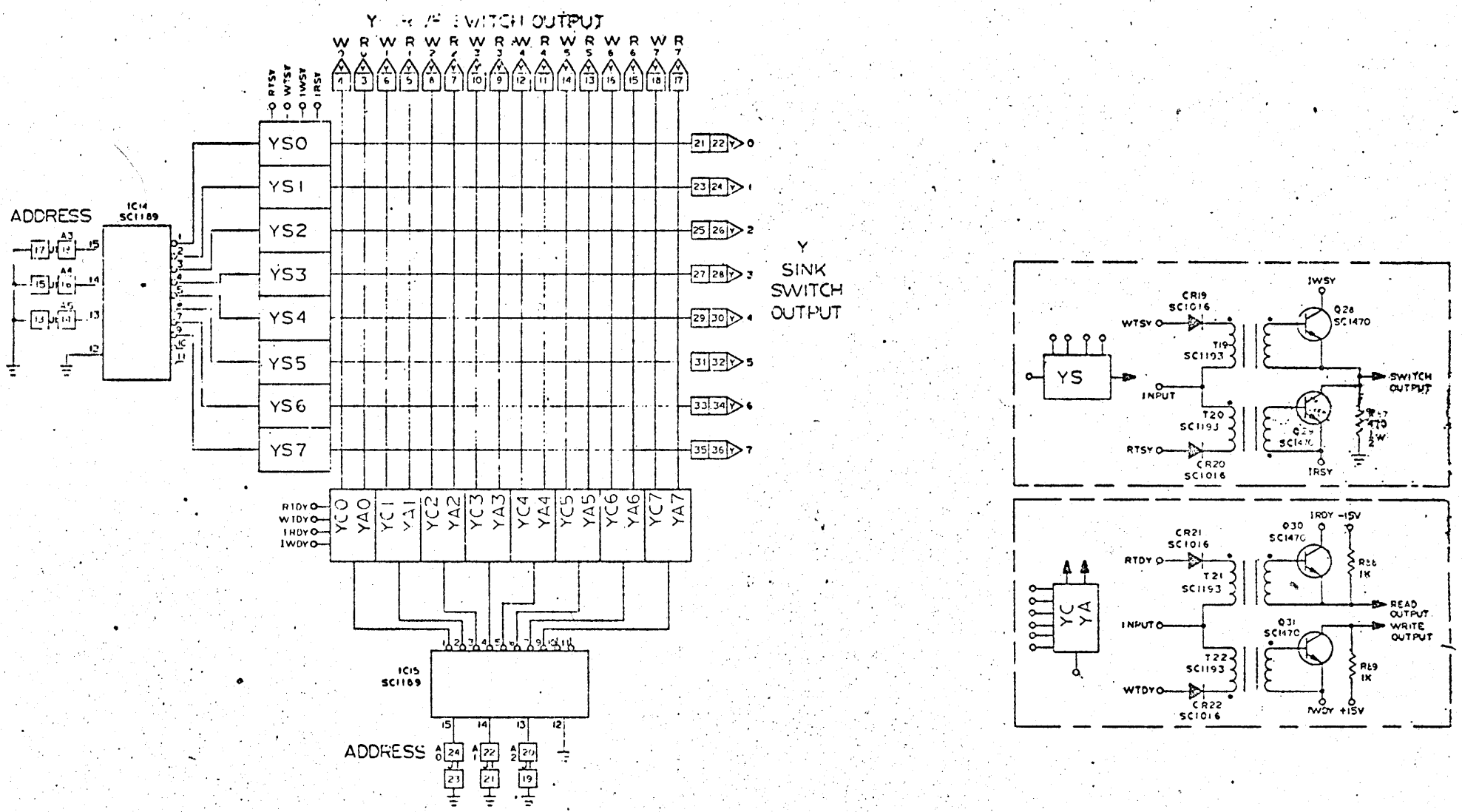
MODEL MM-110

CURRENT MARGIN

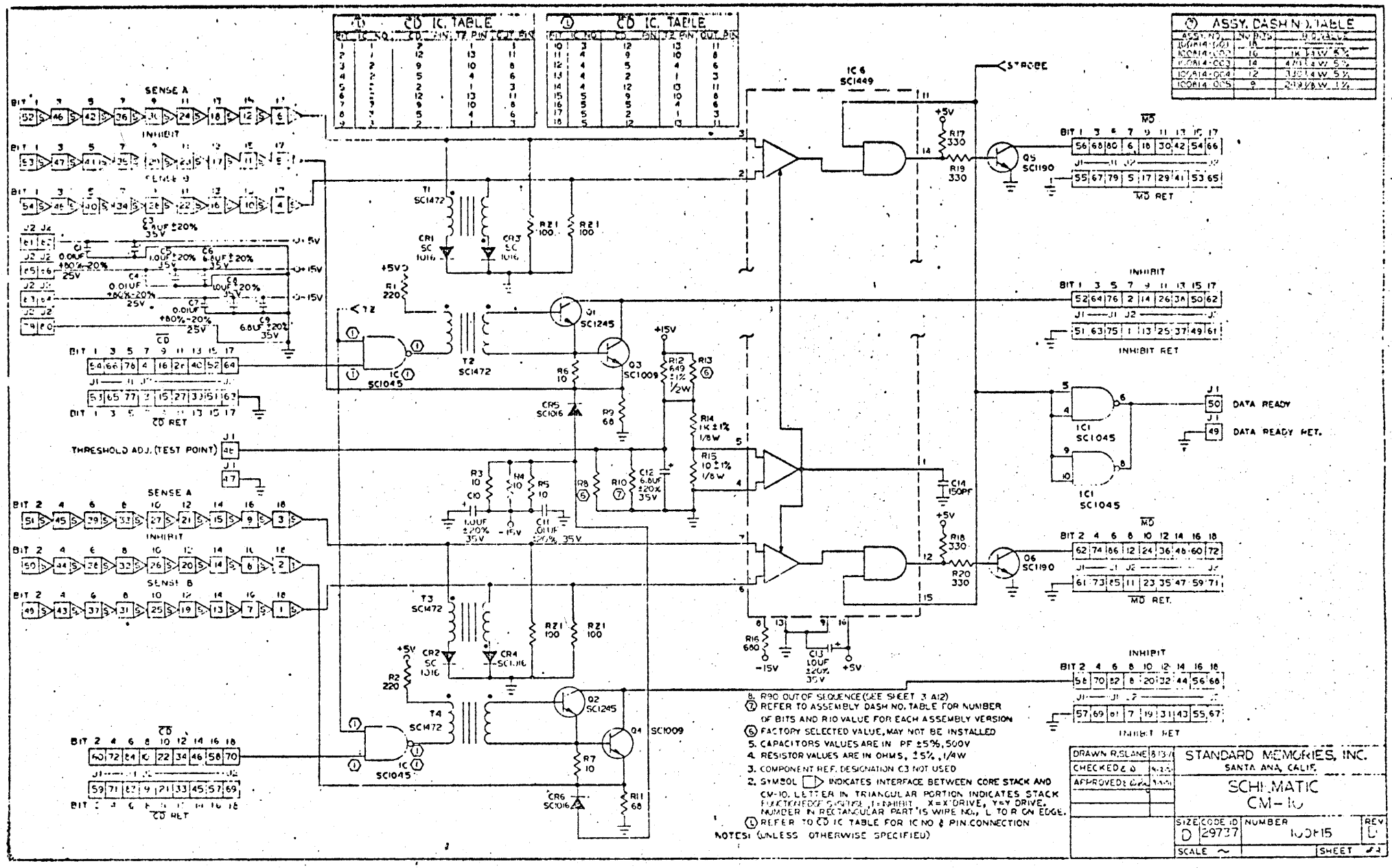
ACCEPTANCE CRITERIA



STANDARD MEMORIES SANTA ANA, CALIF.	SIZE A	CODE IDENT	NUMBER SC 1523	REV A
	SCALE		Form F-120367	SHEET 4 of 4



STANDARD MEMORIES INC	SIZE D	CODE ID 29737	NUMBER 101815	REV.
	SCALE ~		SHEET 4	

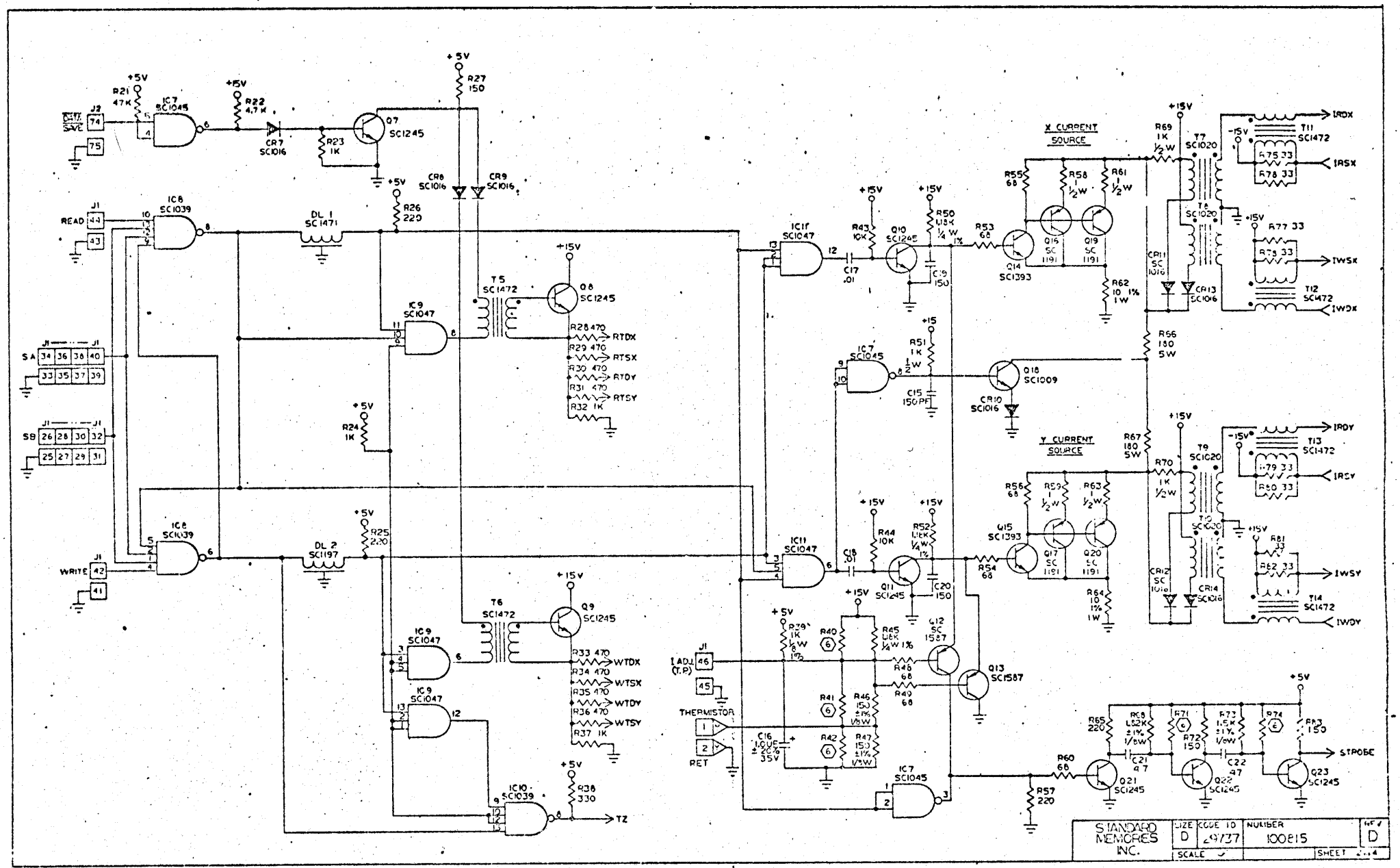


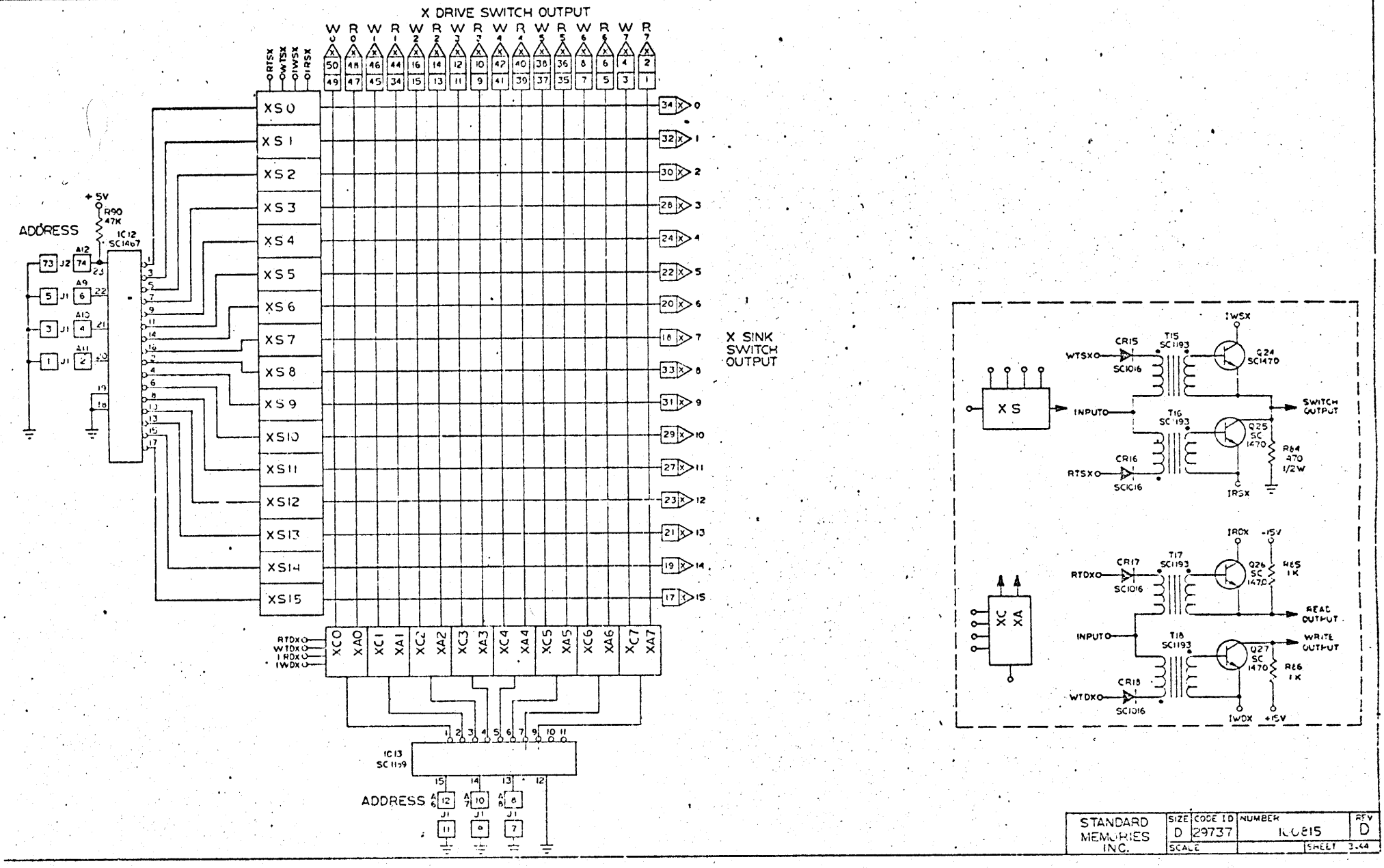
ASSY. DASH NO. TABLE		
ASSY NO.	NO. PINS	R 5% 1/4W
100A14-001	18	
100A14-002	16	1K 1/4W 5%
100A14-003	14	470 1/4W 5%
100A14-004	12	330 1/4W 5%
100A14-005	9	249 1/8W 1%

8. R90 OUT OF SEQUENCE (SEE SHEET 3 A12)
7. REFER TO ASSEMBLY DASH NO. TABLE FOR NUMBER OF BITS AND R10 VALUE FOR EACH ASSEMBLY VERSION
6. FACTORY SELECTED VALUE, MAY NOT BE INSTALLED
5. CAPACITORS VALUES ARE IN PF ±5%, 500V
4. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W
3. COMPONENT REF. DESIGNATION C3 NOT USED
2. SYMBOL ▷ INDICATES INTERFACE BETWEEN CORE STACK AND CM-10. LETTER IN TRIANGULAR PORTION INDICATES STACK FUNCTION EDGE S=STROBE, I=INHIBIT, X=X DRIVE, Y=Y DRIVE. NUMBER IN RECTANGULAR PART IS WIRE NO., L TO R ON EDGE.
1. REFER TO CD IC TABLE FOR IC NO & PIN CONNECTION

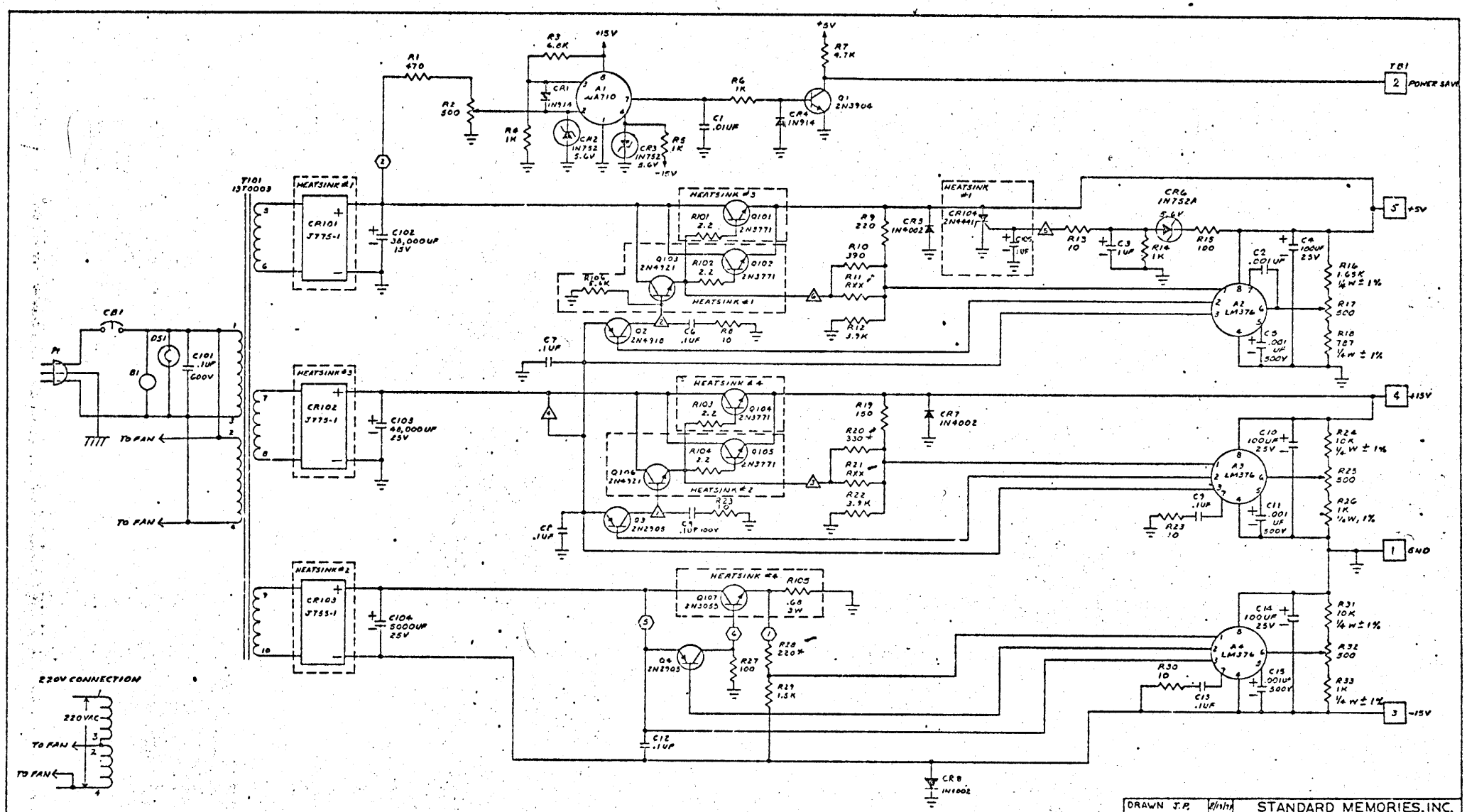
NOTES: (UNLESS OTHERWISE SPECIFIED)

DRAWN R.SLANE	8/13/	STANDARD MEMORIES, INC. SANTA ANA, CALIF.
CHECKED		SCHEMATIC CM-10
APPROVED		SIZE D, CODE ID 29737, NUMBER 100H15, REV D, SCALE ~, SHEET #3


+5V
R21 47K
IC7 SC1045
J2
74
75
+15V
R22 4.7K
CR7 SC1016
R23 1K
Q7 SC1245
R27 150
CR8 SC1016
CR9 SC1016
R26 220
J1
READ
44
43
IC8 SC1039
DL 1 SC1471
IC9 SC1047
T5 SC1472
Q8 SC1245
R28 470 RTDX
R29 470 RTSX
R30 470 RTDY
R31 470 RTSY
R32 1K
R24 1K
SA
34 36 38 40
33 35 37 39
SB
26 28 30 32
25 27 29 31
WRITE
42
41
IC6 SC1039
DL 2 SC1197
R25 220
IC9 SC1047
T6 SC1472
Q9 SC1245
R33 470 WTDX
R34 470 WTSX
R35 470 WTDY
R36 470 WTSY
R37 1K
IC10 SC1039
R38 330
TZ
IC11F SC1047
C17 .01
R43 10K
Q10 SC1245
R50 18K ¼W 1%
R53 68
X CURRENT SOURCE
R55 68
R58 1 ½W
R61 1 ½W
Q14 SC1393
Q15 SC 1191
Q19 SC 1191
R62 10 1% 1W
R69 1K ½W
T7 SC1020
T11 SC1472
R75 33
R78 33
IRDX
IRSX
CR11 SC 1016
CR13 SC1016
R77 33
R79 33
T12 SC1472
IWDX
R66 180 5W
IC7 SC1045
R51 1K ½W
C15 150PF
Q18 SC1009
CR10 SC1016
Y CURRENT SOURCE
R67 180 5W
R70 1K ½W
T9 SC1020
T13 SC1472
R79 33
R80 33
IRDY
IRSY
R56 68
R59 1 ½W
R63 1 ½W
Q15 SC1393
Q17 SC 1191
Q20 SC 1191
R64 10 1% 1W
CR12 SC 1016
CR14 SC1016
R81 33
R82 33
T14 SC1472
IWDY
IC11 SC1047
C18 .01
R44 10K
R52 18K ¼W 1%
R54 68
Q11 SC1245
C20 150
Q12 SC 1587
Q13 SC1587
R78 1K ¼W 1%
R40
R45 18K ¼W 1%
R48 68
R49 68
R41
R46 150 ±1% ⅛W
R42
R47 150 ±1% ⅛W
C16 100E ±20% 35V
J1
I ADJ (T.P.)
46
45
THERMISTOR
RET
1
2
IC7 SC1045
R60 68
R57 220
R65 220
R68 1.62K ±1% ⅛W
R71
R72 150
R73 1.5K ±1% ⅛W
R74
R83 150
C21 47
C22 .47
Q21 SC1245
Q22 SC1245
Q23 SC1245
STROBE
STANDARD MEMORIES INC.
SIZE D
CODE ID 49737
NUMBER 100815
REV D
SCALE
SHEET



STANDARD MEMORIES INC.	SIZE D	CODE ID 29737	NUMBER 100815	REV D
	SCALE			SHEET 3-44



DRAWN J.P.	2/15/71	STANDARD MEMORIES, INC.	
CHECKED R.M.P.	2/16/71	SANTA ANA, CALIF.	
APPROVED [illegible]	2/16/71	SCHEMATIC- P.S. 4-32	
	2/17/71		
		SIZE D / CODE ID 29737 / NUMBER 100776 / REV C	
		SCALE: NONE	SHEET 1 OF 1

S.M. DENOTES FATORY SELECTED PART. NOMINAL VALUE SHOWN.

4. □ INDICATES PINS ON TB1
3. ⬡ INDICATES PADS ON P2
2. △ INDICATES PADS ON P1
1. ALL RESISTORS ARE IN OHMS, 1/2 W ± 5%

NOTE: UNLESS OTHERWISE SPECIFIED

TEST REPORT

ECOM® F MEMORY MODULE 8K

Model No. MM-110-1 CM-10 Serial No. 1506

MM-110 Serial No. 1525 CF-10 Serial No. 1298

1. Ambient Temperature 25 °C
2. Full Cycle Test Time 750 ns
3. +5V Margin ± 10% Ok
4. Data Save Operation Ok
5. Access Time Ok
6. Signal to Noise Ratio 3.40 / 1.89
7. Shmoo Data

XY Volts	Inhibit Volts
13.0 / 15.9	13.0
13.1 / 16.5	14.0
13.0 / 17.1	15.0
13.1 / 17.5	16.0
13.1 / 18.0	17.0

8. Low Temperature Operation 0°C Ok
9. High Temperature Operation 60°C Ok

Workmanship Inspection SMI 3 SEP 1 1973 Approved RSL

Functional Test Clark Date 8-31-72

standard memories

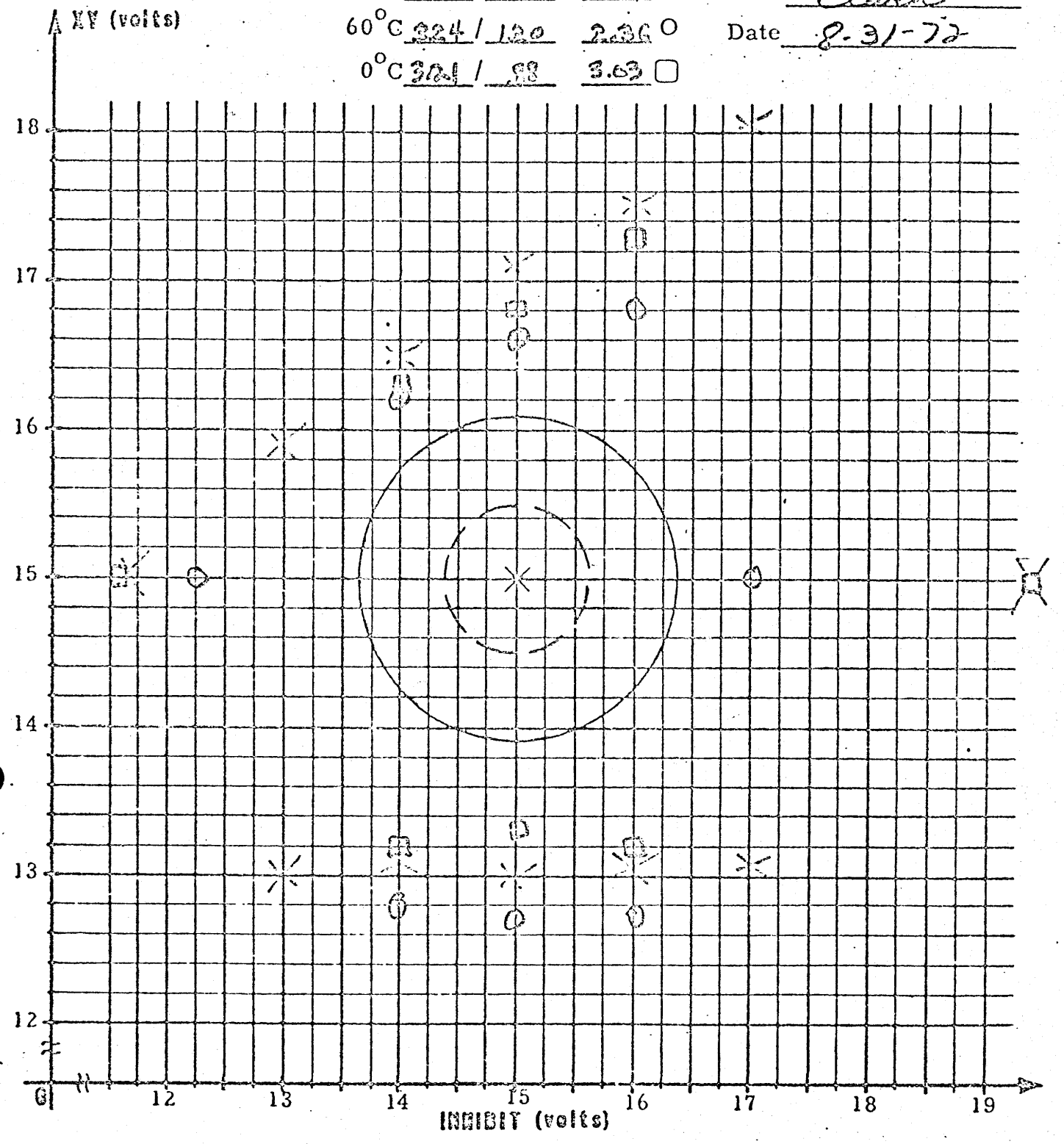
SHMOO DIAGRAM

MODEL NO. MM-110-1 | E-F MEMORY MODULE SC1238 | SERIAL NO. 1525

	S/N	I Adj.	
25°C	3.401 / .89	2.69	X
60°C	324 / 120	2.36	O
0°C	304 / .88	3.03	□

Tech. Clarke

Date 8-31-72



STANDARD MEMORIES SANTA ANA, CALIF.	SIZE A	CODE IDENT	NUMBER	REV
	SCALE	Form F-122870	SHEET	

RCSL: 51-VB620
Author: Allan Giese
Edited: November 1969

RC 4000

CORE STORE TEST

A/S REGNECENTRALEN
Falkoneralle 1
2000 Copenhagen F

CONTENTS:

CORE STORE TEST

1. INITIATION OF PROGRAMS

The core store test program is loaded by means of either the fixed or the relocatable loader in exactly the same way as the testprograms for the peripheral devices.

When the program writes:

device no. =

and later

channel no. =

the operator should respond by typing a <NL> character. He may also type a number terminated by <NL>, but the number has no influence at all on the core store programs.

When the program asks:

error messages:

the operator types y or n for yes and no, respectively, whereafter the program supplies the text with the missing characters es (yes) or o (no).

The next message informs the operator about the free areas of the core store (i.e. the areas not occupied by the program) by writing:

free areas: <area specification>

where <area specification>::= <k number>-<k number> |
<k number>-<k number>,<k number>-<k number>

<k number>::= <positive number>k<positive number>

As an example, the k number 2k15 denotes word number 2 × 1024 + 15 = 2063. The corresponding byte numbers are, of course, 4126 and 4127.

The program writes now:

test areas: <area specification>

and the operator can type the area specification he wants within the stated free areas. The specification is terminated by a <NL> character. If the test areas are outside the free areas, the program will once again write test areas and this is repeated until agreement has been achieved.

Remember to switch off the core store parity control, otherwise the program is stopped whenever a parity error occurs.

2. ADDRESS SELECTION TEST

Purpose

This program tests that every word in the test areas of the core store can be selected. In other words, the test guarantees that two different addresses will not select the same word.

Test

The program works by loading into each word the number of the word, i.e. core store (n):= n. When this is accomplished for every word, the program checks whether the core store contents are correct or not.

Error Messages

An error causes the program to issue the following message:

address <k number>

received <received data, 24 bits>

expected <expected data, 24 bits>

3. BIT SELECTION TEST

Purpose

This program tests that every bit in the test areas of the core store can be set and reset.

Test

The program works by loading into each word the following bitpatterns consisting of 27 bits:

000 ... 000 001
000 ... 000 010

100 ... 000 000
000 ... 000 000

When a bitpattern is stored in core store, it is read out again to be checked against the original bitpattern.

Error Messages

An error causes the program to issue the following message:

address <k number>

received <received data, 27 bits>

expected <expected data, 27 bits>

4. WORST CASE TEST

Purpose

This program checks that the contents of the test areas of the core store are not changed due to noise introduced by the worst case pattern.

Test

The program starts by loading into each word the worst case word, belonging to the worst case pattern; this is done only in run No. 1. Then it continues to read those words repeatedly.

The worst case pattern is an array of worst case words and the contents of those words are chosen so that maximum resultant noise will be produced at the output of the sense windings. The contents of the worst case word are either all ones or all zeroes depending on the address bits 15 (core address 128), 16 (core address 64), and 21 (core address 2) as seen below:

Contents:= all ones for odd Address (15,16,21) = 0
Contents:= all zeroes for odd Address (15,16,21) = 1

Error Messages

An error causes the program to issue the following message:

address <k number>
received <received data, 27 bits>
expected <0 or 1>

where <0 or 1>::= 0|1

0 stands for all zeroes and 1 for all ones.

5. WORST CASE COMPLEMENT TEST

Purpose

This program checks that the contents of the test areas of the core store are not changed due to noise introduced by the worst case complement pattern.

Test

The program works as the worst case test program, the only exception being that the contents of the words under test are complemented, i.e.

Contents:= all ones	for	odd Address (15,16,21) = 1
Contents:= all zeroes	for	odd Address (15,16,21) = 0

Error Messages

The error messages are identical to those of the worst case test.

RCSL: 51-VB335
Author: Allan Giese
Edited: February 1969

PROGRAM DESCRIPTION FOR CLEARING

THE CORE STORE FOR PARITY ERRORS

ABSTRACT.

The purpose of this program is to cancel the stop of the micro-program caused by a parity error and to re-enter the NORMAL operation mode.

A/S REGNECENTRALEN
Falkoneralle 1
Copenhagen F.

The operator must carry out the following procedure:

PAPER TAPE READER:

1. Insert the program in the paper tape reader and press the RESET button

CENTRAL PROCESSOR, TECHNICAL PANEL:

2. Switch the MODE SELECTOR key to TECHNICAL position
3. Deactivate CORE STORE CONTROL
4. Press the button named: MAR MANUAL CONTROLLED and insert in MAR the address x4y2
5. Press the button named: MAR COMPUTER CONTROLLED
6. Press the button named: CONTINUE
7. Press the button named: MAR MANUAL CONTROLLED and insert in MAR the address x20y4
8. Press the button named: MAR COMPUTER CONTROLLED
9. Press the button named: CONTINUE

When the typewriter writes:

switch to NORMAL position

then

10. Switch the MODE SELECTOR key to NORMAL position

INPUT/OUTPUT TYPEWRITER:

11. Press the New Line (NL) key on the typewriter

When the typewriter writes:

core store cleared for parity error

then the computer is ready for normal program execution.

PROGRAM EXPLANATION.

When the program issues its first message, the program has stored in each word of the core store its own word number; - the only exception being the words occupied by the program itself. After the NL key has been depressed, the program will once more activate all words of the store, but now under supervision of the parity control circuit.

Register w1 equals the address of the core store word to be tested.

```
s. a100, b100,

;   procedure Standard heading for autoload key;
                                        ; begin
w.      aw          2                   ;   comment       w0: aw          2
        aw          4                   ;                 w1: aw          4
        jl          0                   ;                 w2: jl          0
        aw          94                  ;                 w1: aw          94
        aw      x1  2                   ;                a94: aw      x1  2
        aw          96                  ;                 w1: aw          96
        al  w1  x1  2                   ;                a96: al  w1  x1  2
        aw          98                  ;                 w1: aw          98
        jl.        -4                   ;                a98: jl.        -4
        jl  w1      94                  ;                 w1: jl  w1      94
                                        ;   w1:= 4;
                                        ; end Standard heading for autoload key;

                    0                   ;   w3:= 0;
                    0                   ;   ST[8]:= 0;
                    0                   ;   ST[10]:= 0;
                    24                  ;   Service addr:= 24;
                                        ; Start location 1:
                                        ;   w1:= 94;
  a14:  al  w2     -1                   ;
        pl          5                   ;   PR:= b 1111 1111;
  a18:  al  w1  x1  2                   ;   for w1:= 96 step 2 until store limit
        rs  w1  x1  0                   ;     do ST[w3]:= w3;
        jl.        -4                   ;


;   procedure Type text 1;
                                        ; begin
  a24: al. w2       a42.
  a26: bz  w0  x2   0                   ;   char:= w0;
       sn  w0       0                   ;   if char = 0
       jl.          a70.                ;     then goto Wait for NL;
  a32: io  w0       2<6+3               ;   io( w0, IO tpw, write);
       sx  w1       3                   ;   if busy ∨ disconnected
       jl.         -4                   ;     then goto a32;
       al  w2  x2   1                   ;   pointer:= pointer + 1;
       jl.          a26.


;   Data for text 1;
h.a42:          10 , 115                ;   comment
                119, 105                ;   < switch to NORMAL position>
                116, 99
                104, 32
                116, 111
                32 , 78
                79 , 82
                77 , 65
                76 , 32
                112, 111
                115, 105
                116, 105
                111, 110
                0  , 0                  ;     the endmark is the character 0;
                                        ; end Type text 1;
```

```
                                        ; Wait for NL:
w.a70: io  w0        2<6+2              ;   io( w0, IO tpw, read);
  a72: io  w0        2<6+0              ;   io( w0, IO tpw, sense);
       sx            3                  ;   if busy ∨ disconnected
       jl.          -4                  ;     then goto a72;
       se  w0        10                 ;   if char < > NL
       jl.           a70.               ;    then goto a70;
       al  w1        6                  ;   w1:= 6;
       al  w1  x1    2                  ;   for w1:= 8 step 2 until 72
       aw      x1    0                  ;     do ST[w1]:= 4 characters;
       se  w1        72                 ;
       jl.          -6
       jl            14                 ;   goto Start location 2;
  a94: jl.           a14.               ;   goto Start location 1;
; a96:
; a98:

                     0                  ;   ST[8]:= 0;
                     0                  ;   ST[10]:= 0;
                     20                 ;   Service addr:= 20;
                                        ; Start location 2:
  b14: al  w1  x1    2                  ;   for w1:= 74 step 2 until store limit;
       rs  w1  x1    0                  ;     do ST[w1]:= w1;
       jl.          -4                  ;

;   procedure Type text 2;
                                        ; begin
  b20: al. w2        b38.
  b22: bz  w0  x2    0                  ;   char:= w0;
       sn  w0        0                  ;   if char = 0
  b26: jl.           0                  ;     then goto b26;
  b28: io  w0        2<6+3              ;   io( w0, IO tpw, write);
       sx            3                  ;   if busy ∨ disconnected
       jl.          -4                  ;     then goto b28;
       al  w2  x2    1                  ;   pointer:= pointer + 1;
       jl.           b22.               ;

;   Data for text 2;
h.b38:             99 , 111             ;   comment
                   114, 101             ;   < core store cleared for
                   32 , 115             ;    parity error>
                   116, 111
                   114, 101
                   32 , 99
                   108, 101
                   97 , 114
                   101, 100
                   32 , 102
                   111, 114
                   32 , 112
                   97 , 114
                   105, 116
                   121, 32
                   101, 114
                   114, 111
  b72:             114, 0               ;   the endmark is the character 0;
                                        ; end Type text 2;
e.
```

A/S REGNECENTRALEN
SCANDINAVIAN INFORMATION PROCESSING SYSTEMS

FALKONERALLE 1 · DK 2000 COPENHAGEN F
DENMARK – TELEPHONE: (01) 10 53 66
CABLES: REGNECENTRALEN · TELEX: 6282 RC HQ DK