
DATAMATICS

SECTION I

ECOM® F MEMORY SYSTEM

1.1 DESCRIPTION

The ECOM® F memory system provides a low cost, modular approach to memory organization.

Features of the system include:

- 750ns Full Cycle Time
- 325ns Access Time
- Low Cost Field Expansion
- Power Failure Data Protection
- Wide Temperature Operation
- DTL/TTL Compatible Interface
- High Reliability Integrated Circuit Logic
- Byte Control Capability

A complete 18 bit system consists of an enclosure with power supply, a memory controller and one to sixteen memory modules. A 36 bit system would contain two memory controllers.

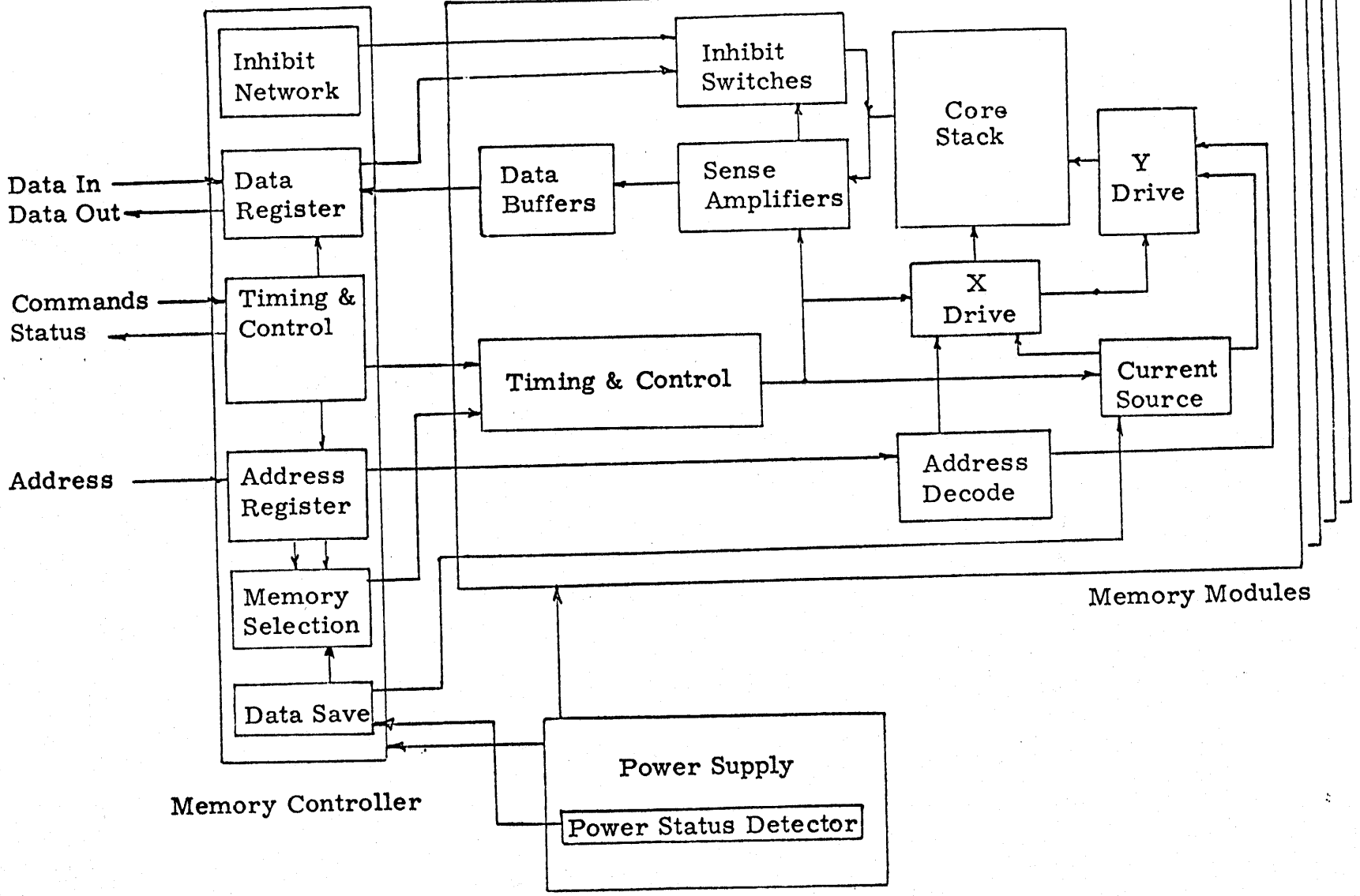
The memory system may be easily field expanded to 131K 18 bit words or 65K 36 bit words by the addition of memory modules. No additional interfacing or adjustments are required.

The memory module contains up to 8192 words with up to 18 bits per word. The core stack with the associated drive, sense and data buffering circuitry, is contained on a single 11 1/2 X 16 inch printed circuit card.

The memory controller provides the control functions, registers and inhibit networks for system users who do not wish to incorporate these functions within their own systems. Up to sixteen memory modules mayshare one controller.

Large memory systems may be obtained by the paralled operation of these modular ECOM® F components. For example, the 36 bit enclosure described in Section II is in essence two independent 18 bit memories of up to 65K words each operating in parallel in the same enclosure. Details of the modular components, their interface and theory of operation, are included as separate sections of this manual.

1.2 SYSTEM BLOCK DIAGRAM



ECOM® F MEMORY SYSTEM

SECTION III

POWER SUPPLY

3.1 DESCRIPTION

The model PS-16-131 power supply is intended for service with the Standard Memories ECOM® F series of core memory systems. The power supply provides regulated +5 volts, +15 volts, -15 volts, and a line voltage status detector.

Power on/off control and fault protection for the transformer circuitry is provided by circuit breaker CB1. Over-current protection for the regulated D. C. outputs is provided by current limiting circuitry within each regulator. Over-voltage protection is provided on the +5 volt supply.

3.2 SPECIFICATIONS

3.2.1 Input.

Voltage	105 to 125V RMS*
Current	6A RMS
Frequency	47 to 440 H_z **

*- The unit may be operated on 210/250V RMS service. The unit is supplied wired for 105/125V service, therefore, before operating the unit on 210/250V service, the transformer must be reconnected. Wiring for both voltage levels is shown on the power supply schematic.

** - Requires special fan for 440H_z operation.

3.2.2	Output	
	Voltage	+5.0V +15.0V -15.0V
	Range	±0.5V ±1.5V ±1.5V
	Current	19 amps. 15 amps. 3 amps.
3.2.3	Power Status Output	
	Normal Line Voltage	0V nominal
	Low Line Voltage	+5V nominal
	Fan Out	4 TTL Loads
	Threshold Range	90V to 120V RMS (Adjustable)
3.2.4	Environment	
	Temperature	0^{o}C to 70^{o}C
	Humidity	to 95% RH without condensation
	Physical Size	3-1/8" X 17-1/4" X 10-3/4"

3.3 THEORY OF OPERATION

3.3.1 Regulator Circuits.

The regulators for all three voltages are on one printed circuit card and are very similar in operation. All are series regulators. Operation of the +5 volt regulator is typical.

Capacitor C1 supplies bulk energy storage. Energy flows from the capacitor through the series regulating transistors Q1 thru Q5 to the memory system. Integrated circuit regulator IC1 provides: Voltage regulator control to the external driver Q6 and the over current fold back. Zener diode CR-11 provides over voltage protection for the +5 supply only.

3.3.2 Power Status

This circuit controls the data save function of the memory system. The output node of this circuit is switched to ground when the A.C. line voltage is normal. The output is +5 volts, or a high impedance, when the A.C. line voltage is low.

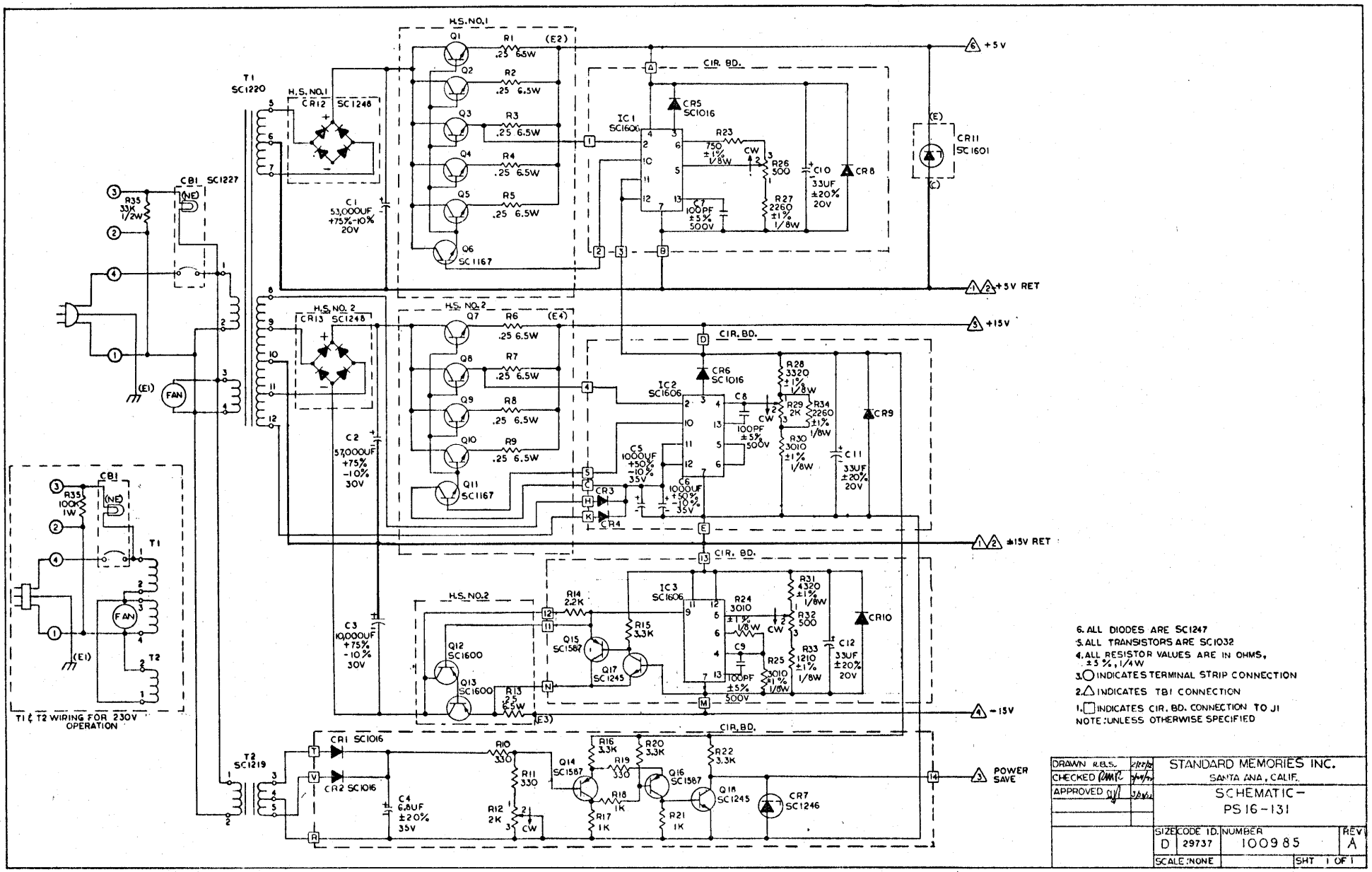
Transformer T2 drives diode bridge CR2 to charge capacitor C4 as a function of peak line voltage. Shunt resistor network (R11-R12) bleeds the charge out of C4 at a fixed rate. Schmitt trigger Q14, 16 monitors the state of charge. When the capacitor voltage drops below a predetermined point, the schmitt trigger will switch providing the 'Data Save P/S' term to the memory.

The value of the A.C. line at which the trigger will switch is factory set at 103V (nominal RMS). This value may be changed by a screwdriver adjustment on the front panel of the memory enclosure. A clockwise turn will lower the threshold voltage.

3.4 TERMINAL ASSIGNMENTS

3.4.1

TB1	Position
Ground	1
Ground	2
Data Save P/S	3
-15	4
+15	5
+5	6


H.S. NO.1
Q1
R1 .25 6.5W (E2)
Q2
R2 .25 6.5W
Q3
R3 .25 6.5W
Q4
R4 .25 6.5W
Q5
R5 .25 6.5W
Q6 SC1167
T1 SC1220
H.S. NO.1 CR12 SC1248
C1 53,000UF +75%-10% 20V
CB1 SC1227
R35 33K 1/2W
(NE)
(E1)
FAN
CIR. BD.
IC1 SC1606
CR5 SC1016
R23 750 ±1% 1/8W CW
R26 500
C10 33UF ±20% 20V
CR8
R27 2260 ±1% 1/8W
100PF ±5% 500V
(E) CR11 SC1601 (C)
+5V
+5V RET
H.S. NO.2
CR13 SC1248
Q7
R6 .25 6.5W (E4)
Q8
R7 .25 6.5W
Q9
R8 .25 6.5W
Q10
R9 .25 6.5W
Q11 SC1167
C2 57,000UF +75% -10% 30V
+15V
IC2 SC1606
CR6 SC1016
C8 100PF ±5% 500V
R28 3320 ±1% 1/8W
R29 2K
R34 2260 ±1% 1/8W
R30 3010 ±1% 1/8W
CR9
C11 33UF ±20% 20V
C5 1000UF +50% -10% 35V
C6 1000UF +50% -10% 35V
CR3
CR4
±15V RET
CB1
R35 100K 1W
T1
T2
FAN
(E1)
T1 & T2 WIRING FOR 230V OPERATION
C3 10,000UF +75% -10% 30V
H.S. NO.2
Q12 SC1600
Q13 SC1600
R13 .25 6.5W (E3)
R14 2.2K
Q15 SC1587
R15 3.3K
Q17 SC1245
IC3 SC1606
R24 3010 ±1% 1/8W CW
R31 4320 ±1% 1/8W
R32 500
R33 1210 ±1% 1/8W
R25 3010 ±1% 1/8W
C9 100PF ±5% 500V
CR10
C12 33UF ±20% 20V
-15V
T2 SC1219
CR1 SC1016
CR2 SC1016
C4 6.8UF ±20% 35V
R10 330
R11 330
R12 2K CW
R16 3.3K
R19 330
R18 1K
R17 1K
Q14 SC1587
Q16 SC1587
R20 3.3K
R21 1K
R22 3.3K
Q18 SC1245
CR7 SC1246
POWER SAVE
6. ALL DIODES ARE SC1247
5. ALL TRANSISTORS ARE SC1032
4. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W
3. ○ INDICATES TERMINAL STRIP CONNECTION
2. △ INDICATES TB1 CONNECTION
1. □ INDICATES CIR. BD. CONNECTION TO J1
NOTE: UNLESS OTHERWISE SPECIFIED
DRAWN R.B.S.
CHECKED
APPROVED
STANDARD MEMORIES INC.
SANTA ANA, CALIF.
SCHEMATIC-
PS16-131
SIZE D
CODE ID. 29737
NUMBER 100985
REV A
SCALE: NONE
SHT 1 OF 1

SECTION I
ECOM® F MEMORY CONTROLLER
MC-131

1.1 DESCRIPTION

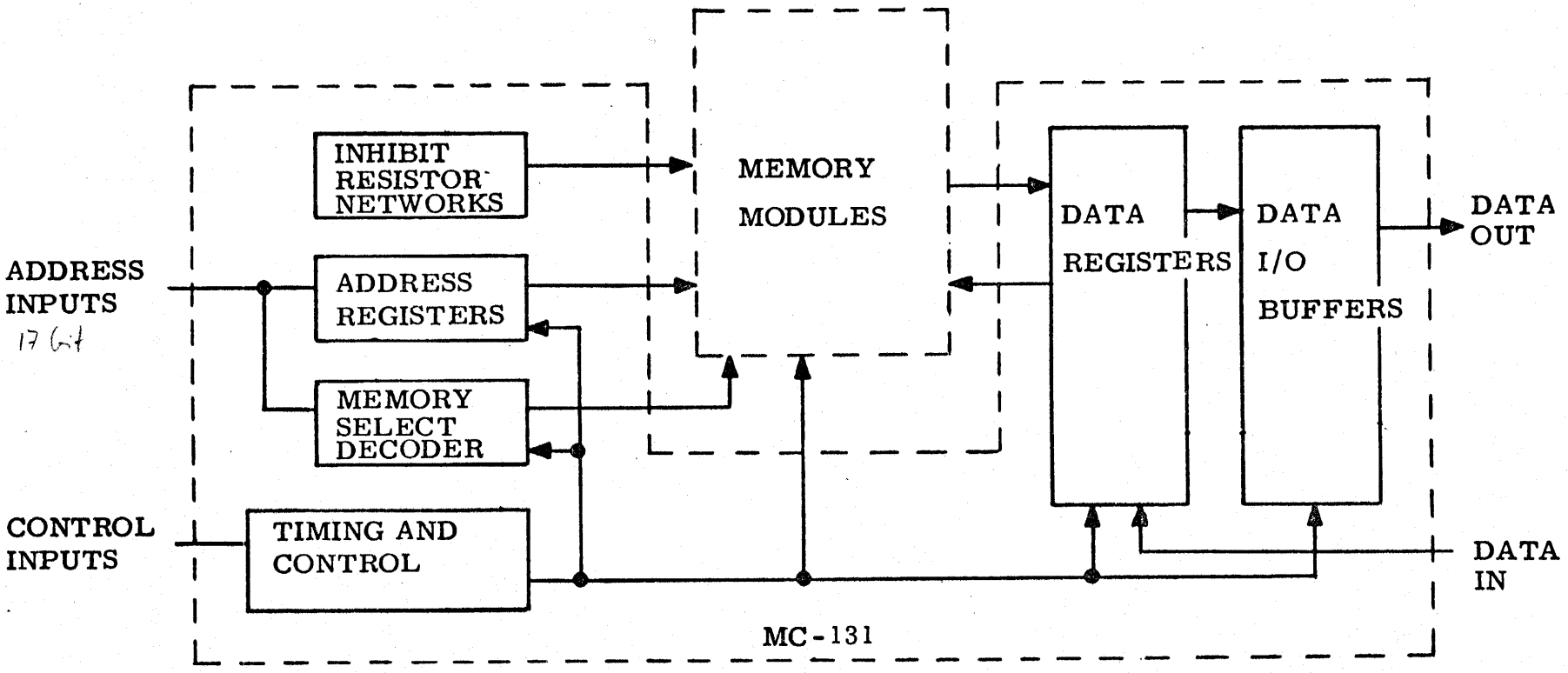
The Memory controller (MC-131) provides timing, control functions, address and data registe rs and the inhibit resistor networks for an 18 bit ECOM® F system of up to 131,072 words. Expanded systems are possible by the parallel operation of memory controllers.

The MC-131 provides four operating modes: Full Cycle Read-Restore and Clear-Write, Split Cycle Read-Pause-Write and Clear-Pause-Write. Each word has been separated into two groups of nine bits which may be operated upon independently (Byte Control). Thus, the MC-131 can make a 131K X 18 bit ECOM® F system appear to contain 262,144 nine bit words.

The input-output interface of the MC-131 is DTL/TTL compatible. All I/O terms originating on the memory controller, with the exception of a $\overline{\text{Memory Busy}}$ signal ($\overline{\text{Memory Busy}}$ is generated by an emitter follower to provide a low impedance or logic 0 signal during a power off condition) are generated by open collector TTL gates to provide compatibility with bussed systems. Either one way or bidirectional

bussing schemes may be used. Provision has been made for field installation of pull-up resistors, should it be desirable.

A power failure data protection circuit is provided on the memory controller. Upon a signal indicating that power is failing, the MC-131 will automatically conclude the cycle in progress, provide a "turn-off" signal to the memory module and then inhibit all commands to the memory module.



MC-131 **FUNCTIONAL BLOCK DIAGRAM**

1.2 SPECIFICATIONS

1.2.1 Operating Modes

Full Cycle	Read-Restore Clear-Write
Split Cycle	Read-Pause-Write Clear-Pause-Write

With Byte Control the ECOM® F system can perform any combination of two of the above functions. For example, it is possible to Read-Restore Byte$_1$ and Clear-Write Byte$_2$ or to Read-Pause-Write Byte$_1$ and Read-Restore Byte$_2$. In the latter case, both a full cycle and a split cycle function are requested. The system will perform both functions with the timing of the split cycle function.

Memory Mode	R/$\overline{C_1}$	R/$\overline{C_2}$	R/$\overline{M_1}$	R/$\overline{M_2}$
Full Cycle				
Read/Restore (R/R)	T	T	T	T
Clear/Write (C/W)	F	F	T	T
R/R Byte$_1$, C/W Byte$_2$	T	F	T	T
C/W Byte$_1$, R/R Byte$_2$	F	T	T	T
Split Cycle				
Read-Pause-Write (RPW)	T	T	F	F
Clear-Pause-Write (CPW)	F	F	F	F
RPW Byte$_1$, CPW Byte$_2$	T	F	F	F
CPW Byte$_1$, RPW Byte$_2$	F	T	F	F

1.2.2 Input/Output Interface.

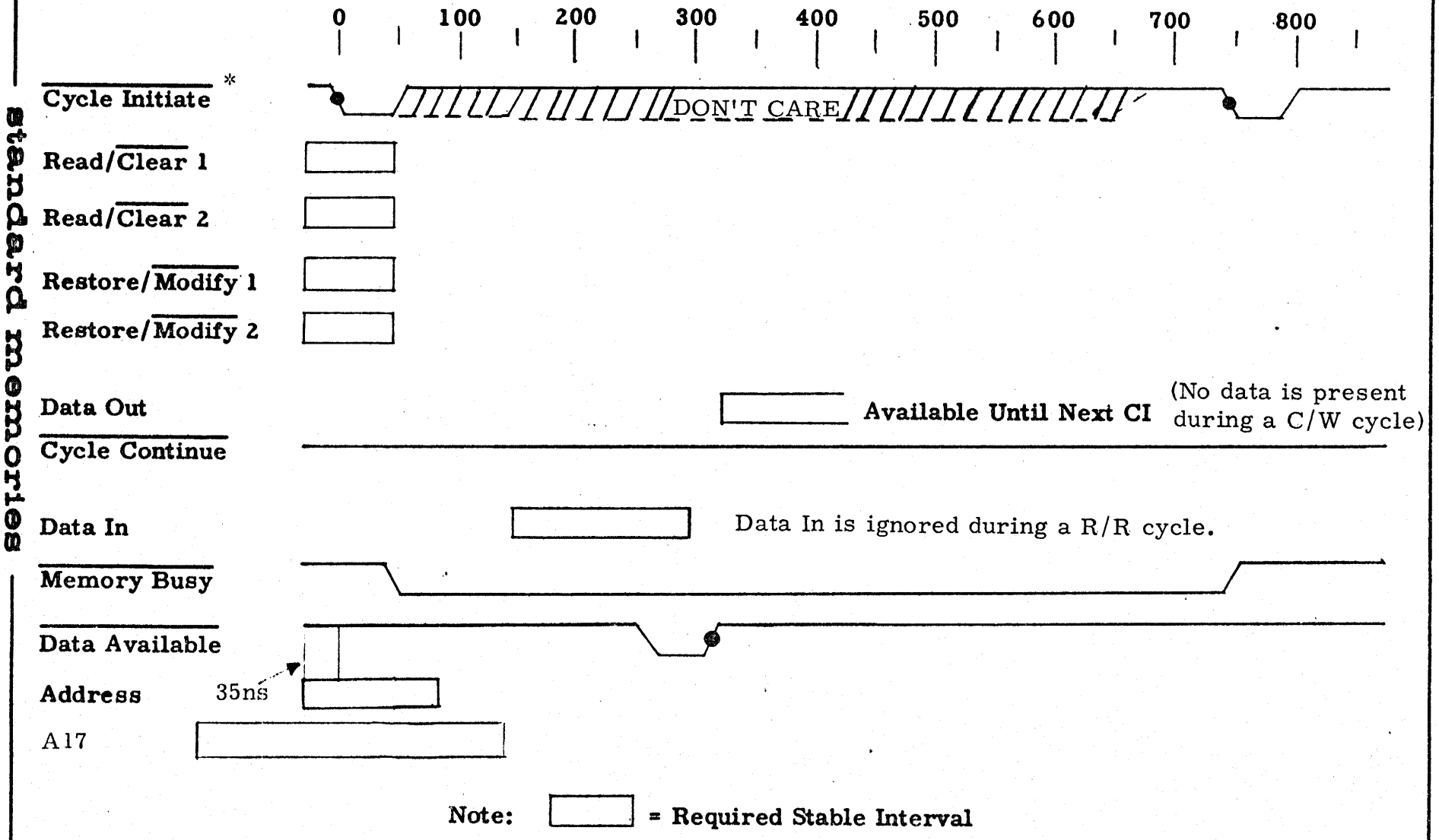
Function	Lines	Loads	Signal
Input:			
Address	18	2	Level
to MC-131 Data In	(18) 14	2	Level
$\overline{\text{Cycle Initiate}}$	1	2	Pulse
Read/$\overline{\text{Clear}}$ 1	1	2	Level
Read/$\overline{\text{Clear}}$ 2	1	2	Level
Restore/$\overline{\text{Modify}}$ 1	1	2	Level
Restore/$\overline{\text{Modify}}$ 2	1	2	Level
Cycle Continue	1	2	Pulse
Data Save P/S	1	2	Level
Data Enable	2	1	Level
Direct Data Save	1	5	Level
	46		

Note: When the power supply goes out of specification, the Data Save P/S line must be held true.

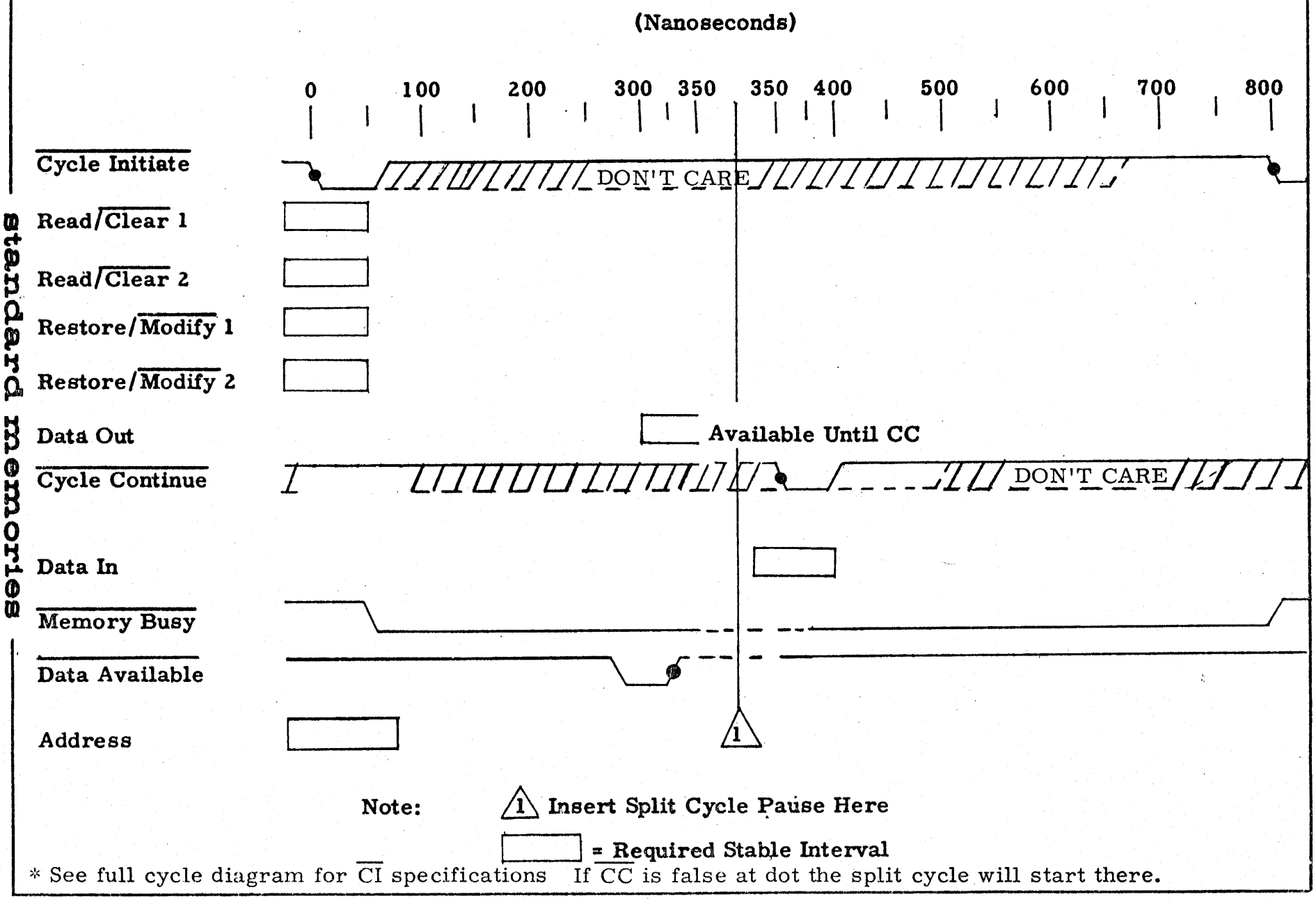
Function	Lines	Loads	Signal
Output:			
from MC-131 Data Out	18	10	Level
Data Available	1	10	Pulse
$\overline{\text{Memory Busy}}$	1	10	Level
Data Save Sync	1	10	Level
Data Save Active	1	10	Level
	22		

1.2.3 Input/Output Timing

Full Cycle (R/R or C/W) Timing



Split Cycle (Read-Pause-Write)



Note: 1 Insert Split Cycle Pause Here

= Required Stable Interval

* See full cycle diagram for CI specifications If CC is false at dot the split cycle will start there.

1.2.4 Memory Interface.

Function	Lines	Signal
Input:		
Data Ready	1	Pulse
Memory Data	18	Pulse
Output:		
Address	12	Level
Selects	8	Level
Control Data	18	Level
Read	1	Pulse
Write	1	Pulse
Data Save	1	Level

All input and output lines are capable of operating with up to 16 memory modules.

1.2.5 Power Requirements.

Logic: +5V ± 5% 1.5 amperes

Inhibit Network: +15V ± 2%

Note: Current required by the inhibit network is a function of the data pattern and the cycle time. Calculations of average and peak current requirements are presented in the memory module specifications.

1.2.6 Environment.

Temperature: Operating 0°C to 50°C in free air when mounted vertically.

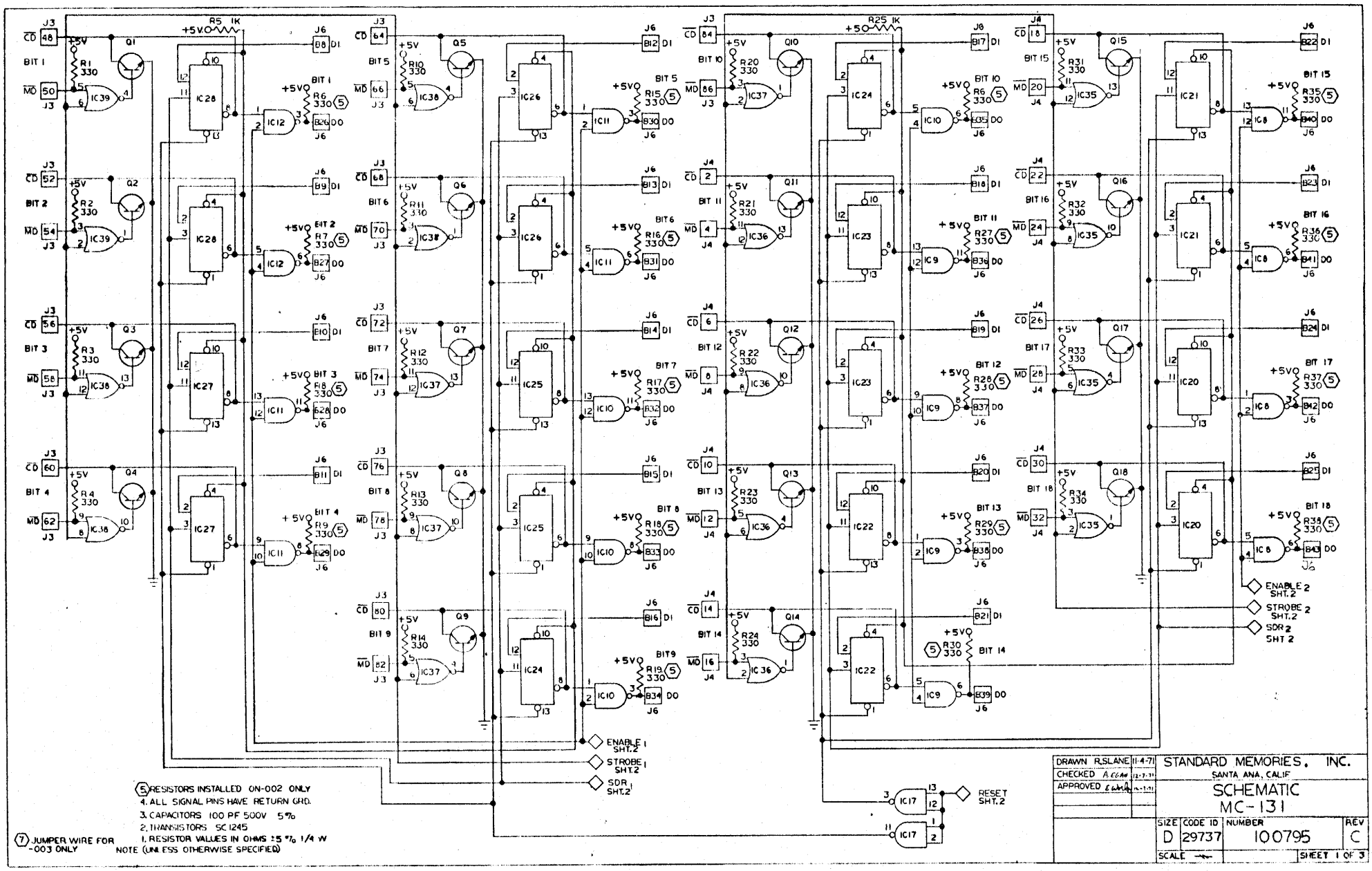
Operating 0°C to 50°C with 20 CFM air flow uniformally distributed over the inhibit resistors when mounted horizontally.

Storage, -40°C to $+100^{\circ}$C

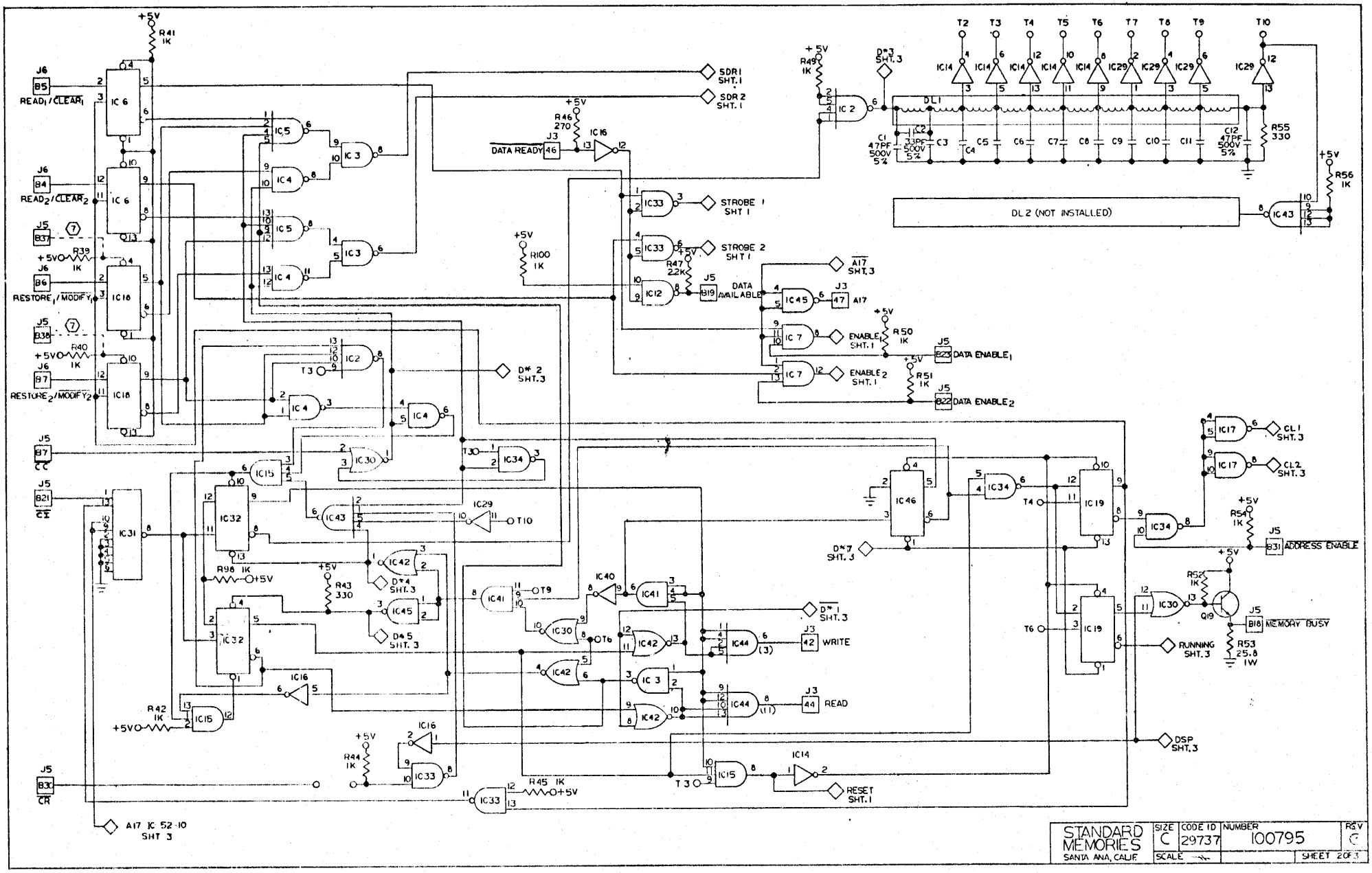
Humidity: To 95% relative, without condensation

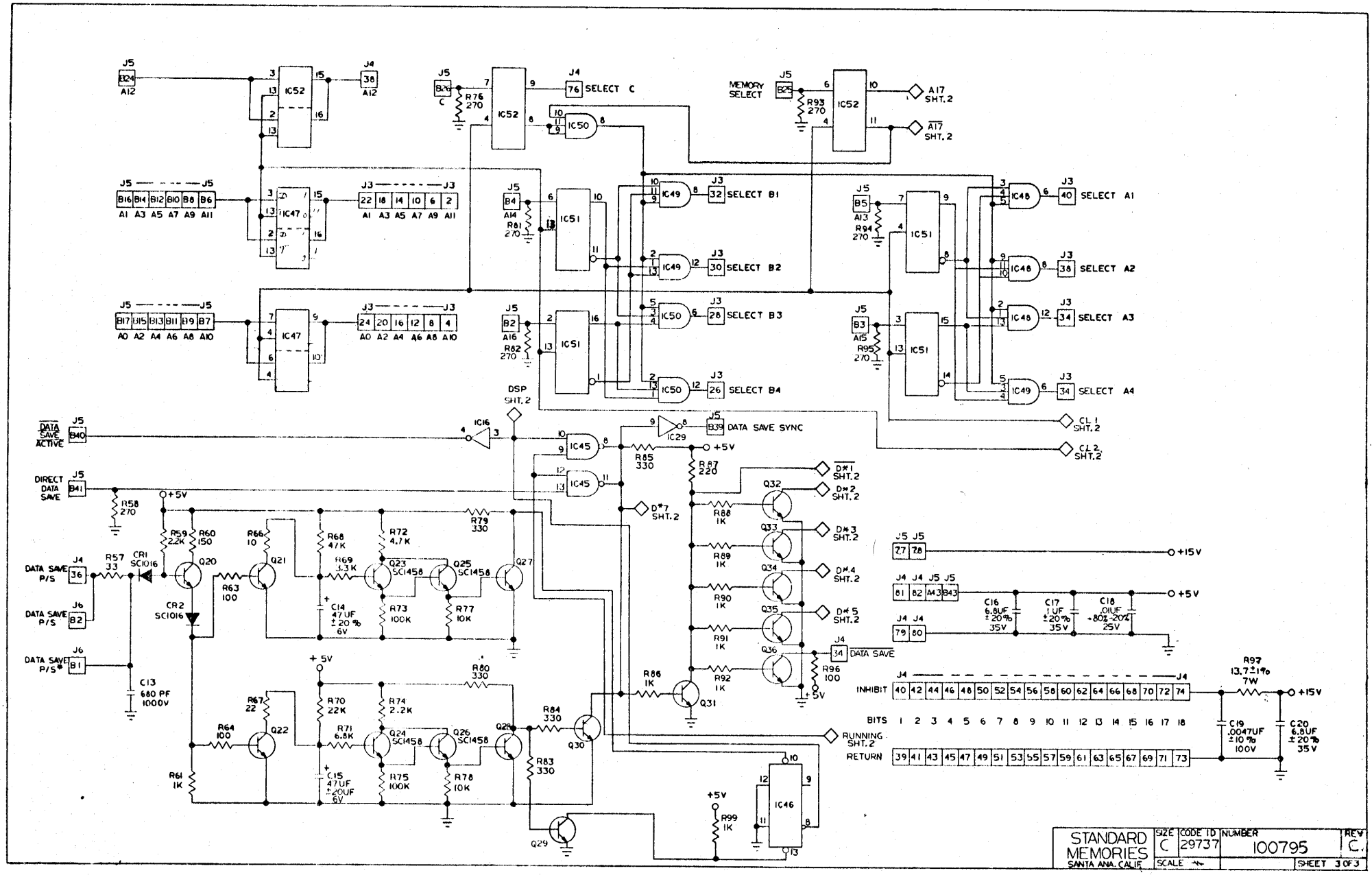
1.2.7 Mechanical.

Board Size:	16.375" X 11.5" (Outline Diagram Page 1-11)
Mounting Centers:	0.75"
Connectors	86 pin card edge type with 0.025" sq. wire-wrap post on 0.100 centers.
I/O Connectors	86 pin card edge type with solder tabs on 0.100 centers.



memory controller


+5V
R41 1K
J6 B5 READ1/CLEAR1
J6 B4 READ2/CLEAR2
J5 B37
J6 B6 RESTORE1/MODIFY1
J5 B38
J6 B7 RESTORE2/MODIFY2
J5 B7 CC
J5 B21 CI
J5 B30 CR
R39 1K
R40 1K
IC 6
IC 18
IC 31
IC 32
IC 15
IC 16
R42 1K
R98 1K
R43 330
R44 1K
R45 1K
R46 270
R47 22K
R100 1K
R49 1K
R50 1K
R51 1K
R54 1K
R52 1K
R53 25.8 1W
Q19
SDR1 SHT.1
SDR2 SHT.1
DATA READY J3 46
STROBE 1 SHT 1
STROBE 2 SHT 1
DATA AVAILABLE J5 B19
A17 SHT.3
J3 47 A17
ENABLE1 SHT.1
ENABLE2 SHT.1
J5 B23 DATA ENABLE1
J5 B22 DATA ENABLE2
D* 2 SHT.3
D*3 SHT.3
D*4 SHT.3
D*5 SHT.3
D*7 SHT.3
D* 1 SHT.3
J3 42 WRITE
J3 44 READ
T10
T9
T6
T3
T4
DL1
DL2 (NOT INSTALLED)
C1 47PF 500V 5%
C2 330PF 500V 5%
C12 47PF 500V 5%
R55 330
R56 1K
CL1 SHT.3
CL2 SHT.3
J5 B31 ADDRESS ENABLE
J5 B18 MEMORY BUSY
RUNNING SHT.3
DSP SHT.3
RESET SHT.1
A17 IC 52-10 SHT 3
STANDARD MEMORIES
SANTA ANA, CALIF
SIZE C
CODE ID 29737
NUMBER 100795
REV C
SCALE
SHEET 2 OF 3


SELECT C
SELECT B1
SELECT B2
SELECT B3
SELECT B4
SELECT A1
SELECT A2
SELECT A3
SELECT A4
DATA SAVE SYNC
DATA SAVE
INHIBIT
RUNNING
RETURN
BITS 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
+5V
+15V
STANDARD MEMORIES
SANTA ANA, CALIF.
SIZE C
CODE ID 29737
NUMBER 100795
REV C
SCALE
SHEET 3 OF 3

SECTION II

THEORY OF OPERATION

2.1 MODE CONTROL AND TIMING

A memory cycle in any mode is initiated by a $\overline{\text{Cycle Initiate}}$ ($\overline{\text{CI}}$) pulse. The mode control terms Read/$\overline{\text{Clear}}$ and Restore/$\overline{\text{Modify}}$ determine full or split cycle timing and the function to be performed. The four combinations of these terms and their definitions are:

Mode		Function	
Read	Restore	Full Cycle	Read-Restore
$\overline{\text{Clear}}$	Restore	Full Cycle	Clear-Write
Read	$\overline{\text{Modify}}$	Split Cycle	Read-Modify-Write
$\overline{\text{Clear}}$	$\overline{\text{Modify}}$	Split Cycle	Clear-Write

One complete memory cycle in any of these four combinations requires that a Read and then a Write command be presented to the memory. During the Read command, information will be taken from the memory and the cores will be "cleared". During the Write command, this information will either be restored or new information will be written into the cores.

By the use of Byte control, any pair of the above four combinations may be requested. When the mode control requests that one byte of memory perform a full cycle operation and the other a split cycle

operation, the memory controller will perform both requested operations with split cycle timing. For example, it is possible to Read-Pause-Write Byte $_2$. Data will be restored in Byte $_1$ and Data In will be written into Byte $_2$ at the conclusion of the pause.

Memory Mode	Read/$\overline{\text{Clear}}$ $R/\overline{C}_1$	$R/\overline{C}_2$	Restore/$\overline{\text{Modify}}$ $R/\overline{M}_1$	$R/\overline{M}_2$
Full Cycle:				
Read-Restore (R/R)	T	T	T	T
Clear-Write (C/W)	F	F	T	T
R/R Byte$_1$ C/W Byte$_2$	T	F	T	T
C/W Byte$_1$ R/R Byte$_2$	F	T	T	T
Split Cycle:				
Read-Modify-Write(RMW)	T	T	F	F
Clear-Pause-Write	F	F	F	F
RMW Byte$_1$ C/W Byte$_2$	T	F	F	F
C/W Byte$_1$ RMW Byte$_2$	F	T	F	F
--- etc. ---				

In the following descriptions of the MC-131 operation, positive logic notation is used. That is, a logic zero is ground or a low impedance, and a logic one is plus voltage or a high impedance. The MC-131 uses TTL logic, primarily the 7400 series.

The various manufacturers of this logic define a logic one as between +2.0 and +5.0 volts and a logic zero as between ground and +0.8 volts.

All internal timing in the MC-131 is obtained from a delay line. This

technique provides reliable and consistent timing with temperature and time. There are no significant differences in delays among paths propagating related signals, such as will be found between common asynchronous single shot multivibrators.

Two pulses are sent down the delay line to provide timing for the above functions. The first pulse is for the Read command, the second is for the Write command. Flip flop IC32 (pin 9) determines the width of the delay line pulse and the duration of the Read and Write commands. IC32 pins 5 and 6 provide control ; pin 5 is a logic one for a Write pulse, pin 6 is a logic one for a Read pulse.

In both the full cycle and split cycle modes $\overline{CI}$ clocks flip flop IC32 which starts the first pulse down the delay line. The flip flop will also initiate the Read command. When the leading edge of the pulse arrives at tap 6 of the delay line, it will reset the flip flop which in turn (a) terminates the Read command, (b) establishes the end of the pulse and (c) toggles IC32 pins 5 and 6.

In the full cycle modes, when the trailing edge of the pulse reaches delay line tap 3, it will set flip flop IC32 (pin 9) for the second time, thereby generating both the second delay line pulse and the Write command. When the leading edge of the second pulse arrives at

tap 6, it will again reset the flip flop terminating the Write command, establishing the end of the second pulse and toggling IC32 pins 5 and 6 back to their original state. As IC32 pin 6 had been returned to its original state, the trailing edge of the second pulse will not set the flip flop when it appears at tap 6. This pulse will continue down the delay line providing the signals to conclude the cycle.

In the split cycle modes, the first pulse will not reset flip flop IC32 when it arrives at tap 3 as IC2 pin 8 has been forced to a logic one state. The pulse will continue down the delay line without consequence. A $\overline{\text{Cycle Continue}}$ ($\overline{\text{CC}}$) command is required to complete the memory cycle. This command will set flip flop IC32 and thereby, start the Write command and the second delay line pulse. The logic will be reset, as above, when the trailing edge of the second pulse reaches tap 3.

2.2 ADDRESS AND MEMORY SELECT

The thirteen low order address bits A_0 through A_{12} are buffered by IC47 and 52, a Quad Latch Type flip flop used as a register. The output terms of the register go directly to the memory where they are decoded to select one of the up to 8192 words.

The clock terms to the register are normally a logic one allowing the output nodes, after one propagation delay, to follow the signal on the input nodes. When a $\overline{CI}$ command is received, the clock terms will go to a logic zero setting the register; therefore, it is required that the address terms be stable 25ns prior to, and remain stable 100ns after, the leading edge of $\overline{CI}$ (see section 1.2.3 for I/O Timing Diagrams). The clock terms will remain a logic zero until the memory cycle is completed. In addition, the $\overline{\text{Address Enable}}$ term can be used to externally set the register between cycles.

The four high order address bits A_{13} through A_{16} are operated upon as above with the exception that two 1 of 4 decoding networks are between the output of the register and the memory. In a normal ECOM® F memory system, one term of each decoding network is connected to each memory module allowing the selection of one of a possible sixteen modules. The decoder truth tables are:

	Select		Select
A_{15} A_{13}	B_4 B_3 B_2 B_1	A_{14} A_{12}	A_4 A_3 A_2 A_1
0 0	0 0 0 1	0 0	0 0 0 1
0 1	0 0 1 0	0 1	0 0 1 0
1 0	0 1 0 0	1 0	0 1 0 0
1 1	1 0 0 0	1 1	1 0 0 0

The input nodes of address terms A_{13} through A_{16} are connected to ground through a 270Ω resistor to ensure a logical zero to the decoder when the address term is not connected on the I/O.

Two other address terms are present on the MC-131. "Memory Select" can be used as an extended address which will disable the MC-131 by blocking incoming $\overline{CI}$ and force all data out terms to a high level. As received from the factor "Memory Select" is forced low via a 270Ω so it will have no effect unless a signal is sent to J5B25. Also available is 'C', J5B26, which if forced high, will cause all A selects and B selects to go low, thereby selecting no memory but will cause 'Select C', J476, to go high. During a cycle with 'C' at a logical one all lower order address' and control and data functions are available. 'C' is forced low via a 270Ω for standard operation.

2.3 $\overline{\text{MEMORY BUSY}}$

When this term, driven by an emitter follower, is at a logic zero, the memory is either performing a cycle or is in a power shutdown condition.

When a $\overline{\text{CI}}$ command is given, it will clock flip flop IC-32 and turn off the emitter follower, and forcing $\overline{\text{Memory Busy}}$ to a logic zero. The transition from a logic one to a logic zero of the second pulse on the delay line will set the flip flop IC-19 and thereby, returning $\overline{\text{Memory Busy}}$ to the logic one state.

At the start of an AC power down condition, transistor Q33 will turn off, forcing IC30 (pin 13) to a logic zero and thereby, grounding the base of the emitter follower. As the DC power fails, the output node of IC45 will approach a high impedance and the emitter follower output will remain low. After the return of AC power, transistor Q33 will remain off for a time constant allowing DC power to return within tolerances and registers to be reset before allowing $\overline{\text{Memory Busy}}$ to return to a logic one.

2.4 DATA IN/DATA OUT

The MC-131 data circuitry has been divided into two identical, independent, nine bit Bytes under the control of the Read/$\overline{\text{Clear}}$ and Restore/$\overline{\text{Modify}}$ commands.

Data In is clocked into the data register by SDR. The inverting output of the register is provided to the memory modules as $\overline{\text{Control Data}}$ ($\overline{\text{CD}}$).

The Data Ready signal from the memory modules is inverted, gated with Read and used to strobe $\overline{\text{Memory Data}}$ ($\overline{\text{MD}}$) into the data register. Note that $\overline{\text{MD}}$ is inverted twice and is present at the output nodes of the register. During a restore cycle $\overline{\text{MD}}$ will be returned to the memory as $\overline{\text{CD}}$. The data register is connected to Data Out through a Nand gate, providing another inversion. Thus, there is an inversion of data from Data In to the memory module and an inversion of data from the memory module to Data Out. Data In and Data Out are of the same sense.

Data Enable 1 and 2 controls the connections of the data register to the Data Out bus. If Data Enable is a logic one, Data Out will be the complement of $\overline{\text{MD}}$ when the MC-131 is in a Read mode and will be a

high impedance when in a clear mode. When Data Enable is a logic zero, Data Out will be a high impedance. Thus, by controlling the modes and Data Enable; the MC-131 may be used with a common buss system. Provisions exist to Byte control Data Enable. If desired, Data In may be connected to Data Out for use with a two way buss. With Byte control, the data terms may be paralled in effect producing a nine bit memory of twice the number of words.

Each processing system is different. In an attempt to provide a "universal" interface, pull up resistors are not factory installed on the I/O. For those systems requiring them on the MC-131 provision has been made for the field installation of pull-up resistors to +5 volts. Plated through holes for the Data Out terms, are provided adjacent to IC8, IC9, IC10, IC11, and IC12. The hole pairs corresponding to Data Out bits 1 and 18 are indicated by the numbers 1 and 18 adjacent to IC8 and IC12 respectively. Provision is also made to terminate the signal inputs check the J5&J6 pin list for the provision made on each signal.

2.5 INHIBIT NETWORK

The MC-131 contains the current determining resistors (R97), energy storage capacitors (C20), and pulse shaping capacitors (C19), for the memory modules inhibit circuitry. As only one memory module under the control of the MC-131 is active at any time, the inhibit

resistors are time shared.

2.6 $\overline{\text{DATA SAVE}}$

Data retention in the memory module during a power transient condition is accomplished by (1) not allowing Read or Write commands to be sent to the memory and (2) providing a $\overline{\text{Data Save}}$ term to the memory module which will be used to prevent operation of it's X-Y drive current source. When the input term Data Save P/S is at a logic zero, the memory will be allowed to operate; when it is at a logic one, the memory will not be allowed to operate.

On power turn-on the Data Save P/S signal must be a logic one until the +5 and ±15 volt power supplies approach their tolerances. When Data Save P/S returns to a logic zero, the MC-131 timing logic will have been reset and two time constants will start. The first to time out (R74-C15) will remove the reset commands and, by returning $\overline{\text{Data Save}}$ to a logic one, allow the memory module's current source to operate. The longer time constant (R68-C14) will return the $\overline{\text{Memory Busy}}$ signal to a logic one indicating that the memory is now stable and that $\overline{\text{CI}}$ commands will be accepted.

On power turn-off the Data Save P/S signal must go to a logic one. The power supplies must remain within tolerance for at least 20μs after Data Save P/S switches to allow the completion of any memory

cycles in progress. Data Save P/S will turn on transistor Q20 which provides base drive to Q21 and Q22. Transistor Q21 will discharge C14 through R16, thereby, turning off Q27. The collector of Q8 will become a logic one, (a) turning off Q19 providing a $\overline{\text{Memory Busy}}$ signal and (b) turning on IC43 (pin 6) forcing the concluding memory cycle in progress. The longer time constant C15 discharging through R67 and Q22 will provide time for the memory to conclude its cycle before Q36 provides a $\overline{\text{Data Save}}$ command to the memory.

A Data Save P/S signal is generated in the ECOM® F system power supply when the AC line drops below a preset value. This term is connected to connector J4 (pin 36) in all SMI chassis. The MC-131 connects this term directly to the I/O connector J6 pin B1 and through a 33Ω resistor (R57) to J6 pin B2 and the data retention circuitry. The memory's Data Save P/S signal can be used by the processor to control a shutdown sequence. If this is desired, R57 should be removed and the processor should provide the command to save data at J6 pin B2.

Three new signals are available to the MC-131 user. '$\overline{\text{Direct Data Save}}$' provides a direct, no time constant, way of forcing a Data Save action. $\overline{\text{Data Save Active}}$ is an output signal indicating that the Data Save is now fully in operation. Data Save Sync allows one MC-131 to operate as a master with any other MC-131's Data Save slaved to its operation.

SECTION I

ECOM® F MEMORY MODULE, MM-110

1.1 DESCRIPTION

ECOM® F series memory modules are designed for service in general systems and computer main frame applications requiring submicrosecond random access to large banks of digital data. The module consists of a core stack with associated drive, sense, and data buffer circuitry. The module is available in capacities of 8192 words with up to 18 bits per word.

Standard features for the module include:

- 750 nanosecond Full Cycle Time
- 250 nanosecond Access Time
- Low Cost Field Expansion (8192 Word Modules)
- Data Saver (Power Fail Data Protect)
- Wide Temperature Lithium Nickel Cores
- Integrated Circuit Logic
- DTL/TTL Compatible Interface
- Internal Temperature Compensation
- 3D, 3 Wire Organization
- Byte Control Capability
- 0.75" Mounting Centers in Multiple Module Applications

The modular approach to memory organization permits low cost memory expansion to 131,072 words with the simple installation of additional memory module cards. Up to sixteen 8K word modules may time share one interface via the party-line interconnect technique where all address, control, data and inhibit current source lines are bussed in parallel to all modules in the system, providing up to 18 bits per word.

The interface required to service one to sixteen memory modules consists of a data register, address register, read/write timing generator and a set of inhibit resistors.

The 8K MM-110 ECOM®F module is electrically and mechanically interchangeable with the 4K MM-108 ECOM® F module with the exception of one added address input and slightly different supply current requirements.

Standard Memories makes a complete analysis of each module produced to insure that adequate margin is available in all critical parameters for reliable operation over extended periods without adjustment. The results of this analysis for each module are available to the customer in the form of a test report.

1.2 OPTIONAL ECOM® F SERIES COMPONENTS

1.2.1 Memory Controllers.

ECOM® F Memory Controllers are PC cards with dimensions equivalent to those of the ECOM® F memory module, which provide the balance of circuitry for module users that do not wish to integrate address and data registers and inhibit resistors within their own systems. Capabilities of typical Memory Controllers include:

131K X 18 Control Capacity

750ns Full Cycle Read-Restore and Clear-Write

Split Cycle Read-Pause-Write

325ns Access Time

Byte Control

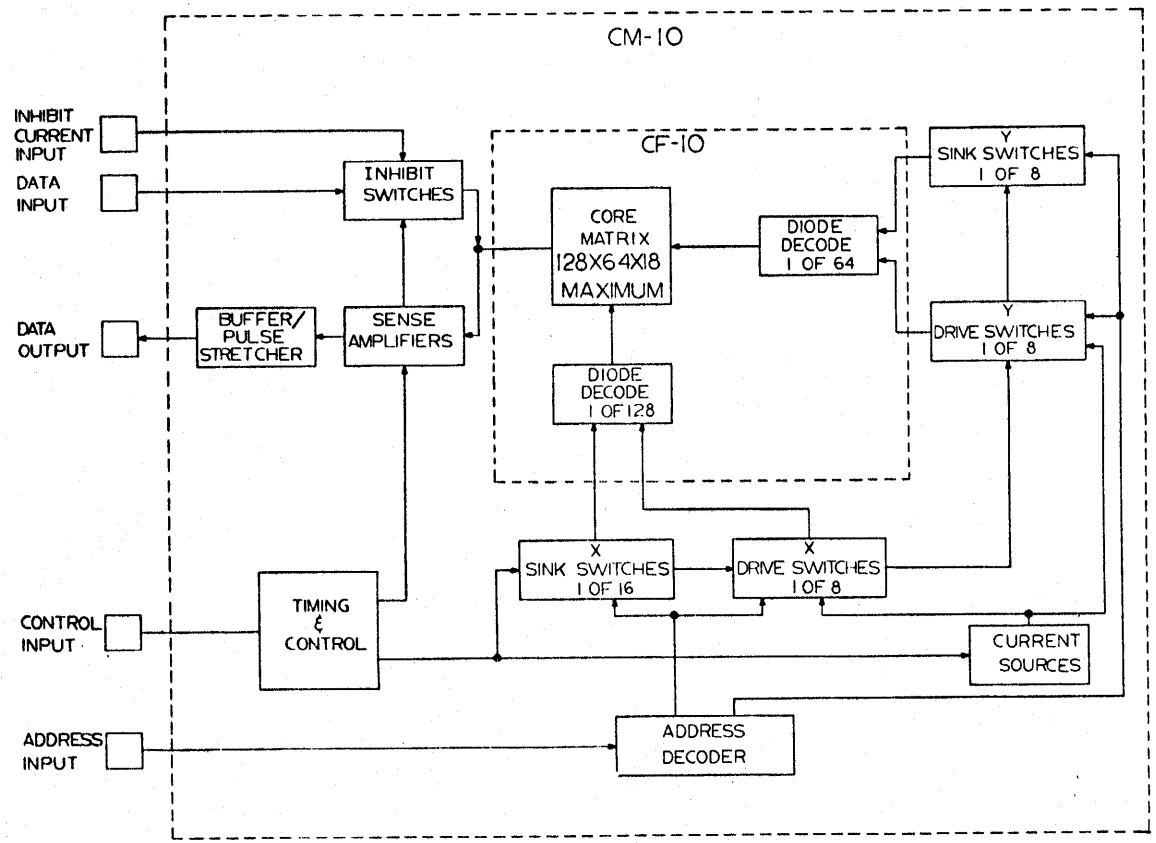
Data Saver Control

1.2.2 Memory Enclosures.

5 1/4 inch high rack mount enclosures with fan and optional power supply. The enclosure may house up to four memory modules and one optional controller yielding 32K X 18 bit maximum memory capacity.

12 1/4 inch high rack mount enclosures with optional power supply. The enclosure may house up to 16

memory modules and either one or two optional controller cards to yield 131K X 18 or 65K X 36 bit maximum memory capacity, respectively.



DRAWN J.P.	10/25/71	STANDARD MEMORIES INC. SANTA ANA, CALIF.
CHECKED [illegible]	10/25/71	
APPROVED [illegible]	10/25/71	BLOCK DIAGRAM - MM-110 ECOM F MEMORY MODULE
		SIZE D · CODE ID 29737 · NUMBER 100899 · REV.
		SCALE —— · SHEET 1 of 1

1.4 SPECIFICATIONS

1.4.1 Memory Type

3D, 3 Wire Coincident Current

1.4.2 Storage Capacity

Words	8192 per module
Bits/Word	Up to 18

1.4.3 Operating Modes

Full Cycle	Read-Restore or Clear-Write
Split Cycle	Read-Pause-Write

1.4.4 Operating Speed

Full Cycle	750 nanoseconds
Split Cycle	750 nanoseconds + pause
Access Time	250 nanoseconds

1.4.5 Input Interface

Function	Lines	TTL Loads	Signal
Address	13	1	Level
Select	2	2	Level
Data Save	1	1	Level
Control Data	18	1	Level
Read	1	1	Pulse
Write	1	1	Pulse

Note - When the power supply goes out of specification, the Data Save line must be held false (0V).

1.4.6 Output Interface (Open Collectors)

Function	Lines	TTL Loads	Signal
Memory Data	18	10	Level
Data Ready	1	8	Pulse

1.4.7 Power Supplies (Current in Amperes)

Worst case requirement for 18 bit word with full cycle time of 750ns:

		Operate					Stand By				
	Voltage	8K	16K	32K	65K	131K	8K	16K	32K	65K	131K
	+5V±5%	1.1	2.1	3.9	7.3	14.7	0.9	1.8	3.6	7.2	14.5
*	+15V±2%	6.1	6.2	6.4	6.8	7.6	0.1	0.2	0.4	0.8	1.6
	-15V±2%	0.5	0.6	0.9	1.4	2.5	0.2	0.3	0.6	1.1	2.2

*Note: +15V current drain includes current for external inhibit resistors.

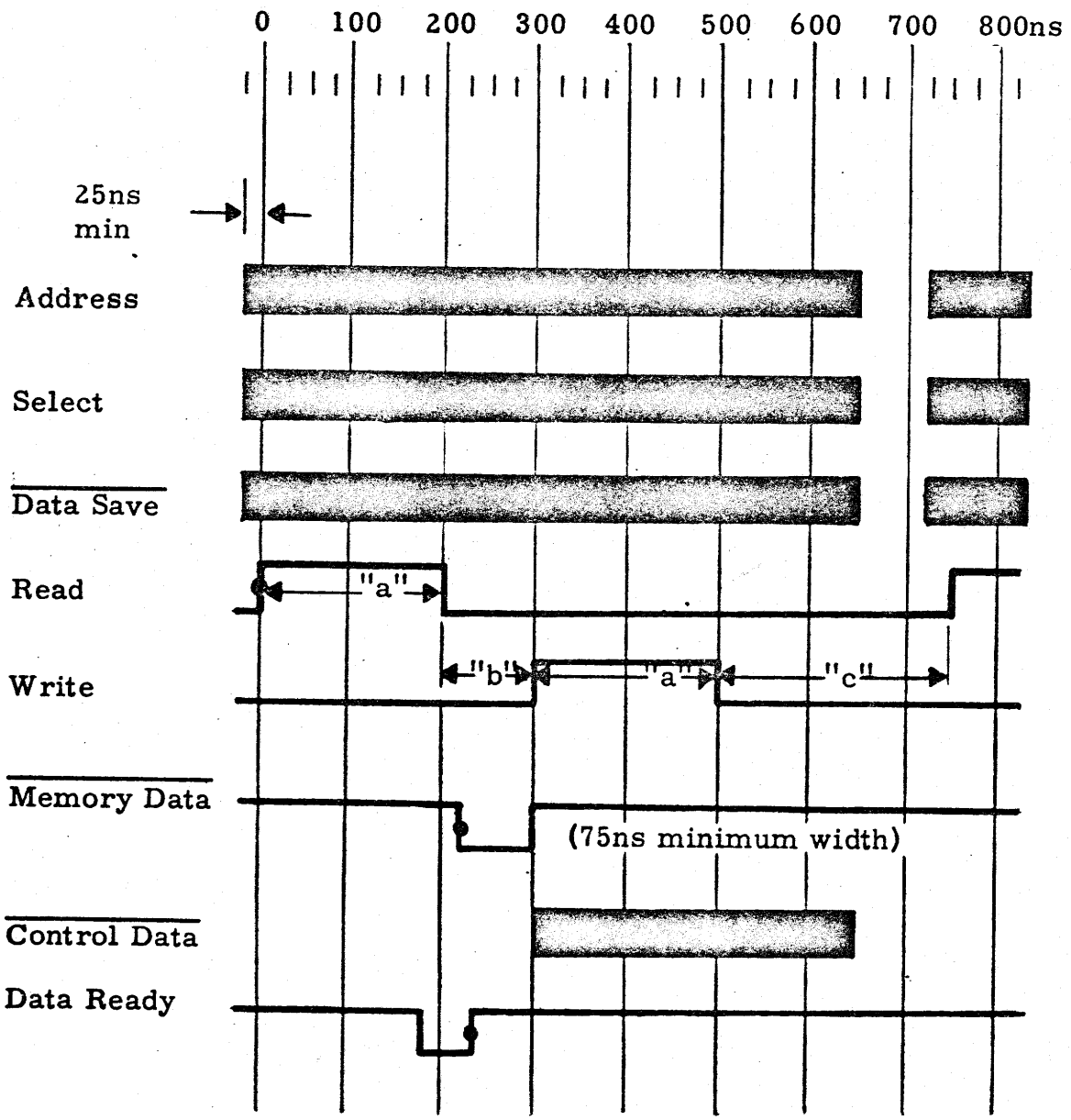
1.4.8 Environment.

Temperature	Operating, 0^{o}C to 50^{o}C in free air when mounted vertically.
	0^{o}C to 50^{o}C with 20 CFM when mounted horizontally.
	Storage, -40^{o}C to $+100^{o}$C
Humidity	To 95% relative, without condensation.

1.4.9 Mechanical.

Board Size	16.0" X 11.5"
Mounting Centers	0.75"
Connectors	86 pin card edge type with 0.025" sq. wire-wrap post on 0.100 centers.

1.5 MODULE INTERFACE TIMING



NOTE:
- = Indicates required settled period
- = Dot indicates significant transition
- "a" = 200ns nominal, 180ns min, 240ns max.
- "b" = 100ns nominal, 80ns min
- "c" = 250ns nominal, 230ns min

1.6 TYPICAL POWER SUPPLY CURRENT DRAIN (AMPERES)

The equations given below are valid for 1 to 16 memory modules time-sharing one interface (131K X 18 maximum). For applications exceeding either 131K words or 18 bits per word or both, calculate the current drains separately for each group of modules serviced by one party line interface and sum the results.

5.1 $I(+5V) = 0.026N(b+13.5) + 0.0075bf$

5.2 $I(+15V)^{*} = 0.09N + 0.21(b + 2.7)f$

5.3 $I(-15V) = 0.0068(Nb + 33f)$

5.4 Definitions:

N = Number of 8K modules (1 to 16)

b = Number of bits/word (9, 12, 14, 16 or 18)

f = Full cycle frequency in Mhz (in standby, f = 0)

* Data pattern "All Zeros" which is the worst case +15V inhibit current demand condition. For normal operating conditions (50% "one" and 50% "zero" data mix) divide "b" by two.

SECTION II

MAGNETICS, CORE STACK

2.1 DESCRIPTION

The core stack assembly, mounted centrally on the electronics board (CM-10), contains the lithium-nickel ferrite core arrays positioned between two hinged P. C. boards. The core arrays are affixed to ground planes between the two boards to minimize thermal gradients in the core area. Diode decode matrices for the X and Y axes are located at the core stack periphery.

A thermistor is provided to sense core temperatures. The thermistor becomes a part of a servo loop in the stack drive electronics to compensate for variations in core characteristics with temperature changes.

2.2 THEORY OF OPERATION

The core stack is electrically organized as a 3D, 3 wire coincident current core stack. A memory data word is addressed for read or write by applying one half of core switching current each on one selected X line and one half on one selected Y line. There are 128 X axis and 64 Y axis drive lines for a total of 8192 word intersections.

The third line through the memory cores is used as a common sense-inhibit line. During read time the sense-inhibit line is used to sense the flux reversal in the core. During write time the sense-inhibit line is used to inhibit the X and Y currents from setting a core to the "1" state, if "0" is to be written. When "1" is to be written, the inhibit line is not energized during the write operation.

The above method of read and write selection is possible only because of the well controlled magnetic threshold of the lithium-nickel ferrite cores used. The core performs the AND logic function in the address selection process, since only when X and Y currents are present in the core aperture will the core be selected. This requirement for the core to perform the AND function places tight limits on the shape of the core hysteresis loop. The half-select current must be less than the knee on the hysteresis loop while the full select current (twice the half-select current) must be greater than the full switching value.

2.3 PARTS REPLACEMENT

No field repairs to the core stack should be attempted. Any service required should be referred to the factory.

SECTION III

ELECTRONICS, CM-10 BOARD

3.1 DESCRIPTION

The CM-10 board contains the circuitry required to drive and sense the core stack.

The CM-10 requires Read and Write pulse inputs to generate read and write memory half cycles, respectively. Timing signals generated within the CM-10 are factory set and should not require readjustment for the life of the equipment.

Operating modes (full cycle Read-Restore and Clear-Write, split cycle Read-Pause-Write) for the module are controlled by Read and Write pulse timing and data inputs to the CM-10. Byte control, if desired, may be provided for in an external data register.

3.2 THEORY OF OPERATION

3.2.1 Timing and Control.

Timing and control signals generated internally on the CM-10 are explained below:

a. RTD and RTS are current pulses of durations approximately equal to that of the Read timing

pulse input, plus the delay of DL1 (50ns) and are used to close selected drive and sink switches in the X and Y stack drive circuits. For example, RTDX closes 1 of 8 read-drive floating switches composed of CR17, T17 and Q26. Address decoder IC13 performs the 1 of 8 switch selection. RTSX, RTDY and RTSY perform in a similar manner.

b. WTD and WTS perform the same function as RTD and RTS but occur during a write half cycle.

c. STROBE is a short positive pulse to the sense amplifiers which occurs approximately at core peaking time during a read half cycle. Strobe is generated by the timing circuits associated with Q21, Q22 and Q23.

d. TZ is a timing pulse enabling input data to control the inhibit current switches. The duration of TZ is approximately equal to that of the Write pulse input plus 70ns, the delay time of DL2.

3.2.2 X and Y Drive Circuits.

X and Y drive currents to the core stack are controlled in magnitude and rise time by a two linear, active current sources. For example, the X current source is composed of Q14, Q16 and Q19 and

associated components. R50 and C19 form an R-C integrator to control current rise times. Q12 clamps the current magnitudes to a value established by the core stack thermistor to provide current versus temperature compensation. Current source outputs are routed to stack drive and sink switch transistors at the core stack periphery by a four transformer distribution matrix.

The Y current source performs in a similar manner except that the Y read current leads the X read current by 50ns, the delay of DL1.

The $\overline{\text{Data Save}}$ input, when held low (0V) will disable all X and Y stack drive and sink switches. Should the power supply voltages go out of specification, the module should be permitted to complete any memory cycle in process before $\overline{\text{Data Save}}$ is forced to ground.

3.2.3 Data Circuits.

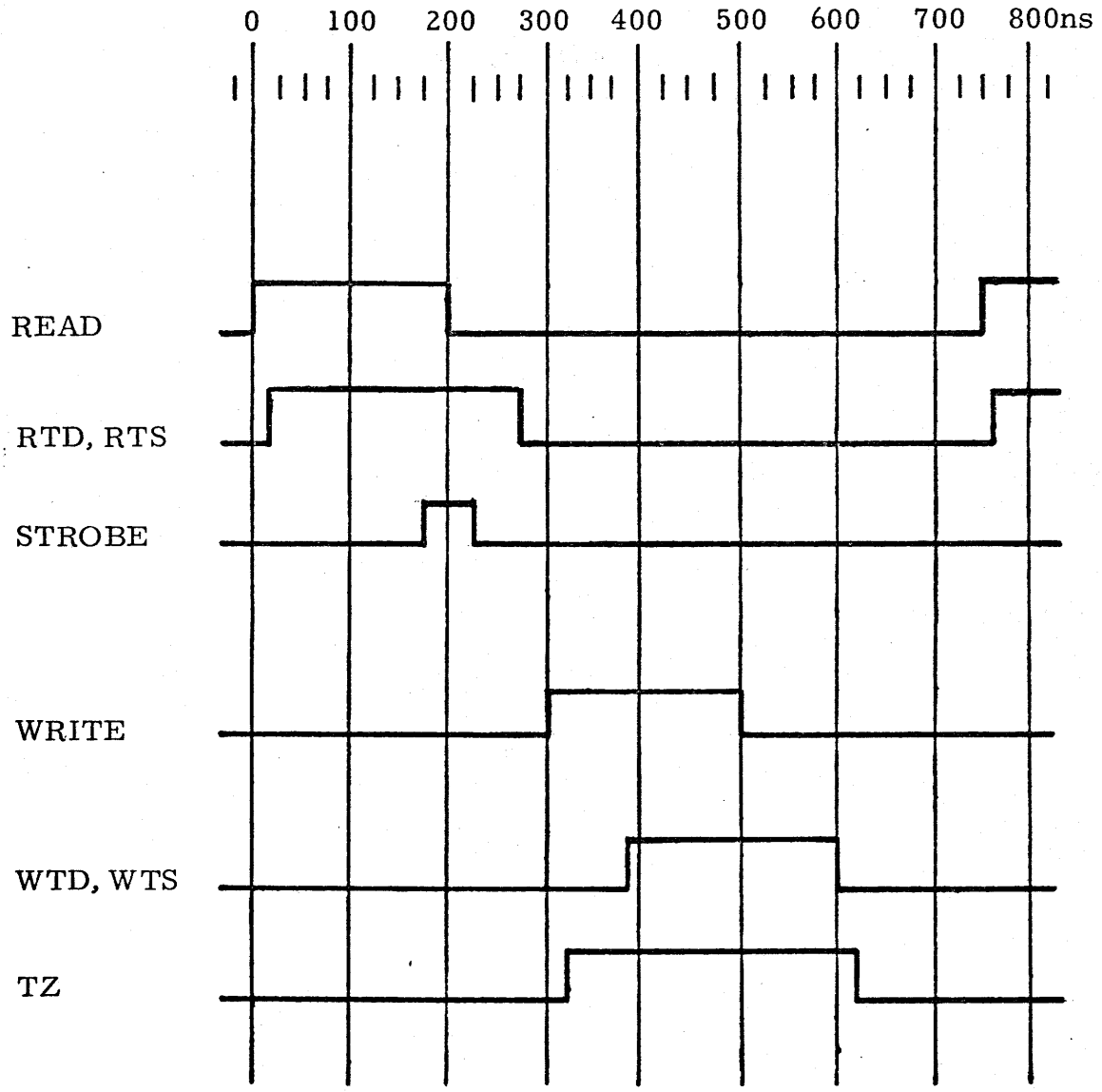
Core stack signal sensing is performed by a dual-channel integrated circuit sense amplifier (IC6). The sense lines are terminated by RZ1. Pins

4 and 5 of IC6 are inputs to a reference amplifier which sets the threshold for identical amplifiers at pins 2-3 and 6-7 of the same IC. Signal threshold is developed across R15 by a precision voltage divider network.

The strobe pulse to the sense amplifier gates the sense amplifier at read time and enables data read-out of the core stack to be transferred to the data output buffers, Q5 and Q6. Q5 and Q6 are fast-on, slow-off devices to effectively stretch the $\overline{\text{Memory Data}}$ ($\overline{\text{MD}}$) output pulse width.

Inhibit switches (Darlington pairs Q_1 -Q_3 and Q_2 -Q_4) supply inhibit currents from remote inhibit resistors to the center-tapped sense/inhibit lines. The inhibit switches are controlled by input data, $\overline{\text{Control Data}}$ ($\overline{\text{CD}}$), as timed by TZ during a write cycle.

3.3 INTERNAL TIMING (Typical)



(SC 1449)

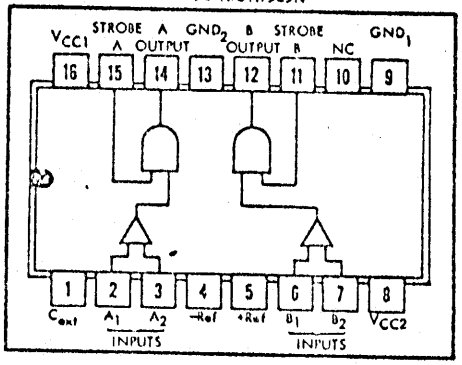
logic

POSITIVE LOGIC

OUTPUT A = $S_A \cdot IN_A$
OUTPUT B = $S_B \cdot IN_B$

Where: S_A = STROBE A ≥ 2 V
IN_A = (V_{inD} or INPUTS A_1 and A_2) > V_T
S_B = STROBE B ≥ 2 V
IN_B = (V_{inD} or INPUTS B_1 and B_2) > V_T

SN7524N/SN7525N



electrical characteristics (unless otherwise noted V_{CC1} = 5 V, V_{CC2} = -5 V, T_A = 0°C to 70°C)

	PARAMETER	TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_T	Differential-input threshold voltage (See Note 1)	12	V_{ref} = 15 mV	SN7524N	11	15	19	mV
				SN7525N	8	15	22	mV
			V_{ref} = 40 mV	SN7524N	36	40	44	mV
				SN7525N	33	40	47	mV
V_{CMF}	Common-mode input firing voltage (See Note 2)	none	Strobe Input: $V_{inS} = V_{in(1)}$ Common-Mode Input Pulse: $t_r = t_f$ = 15 ns, $t_{p(in)}$ = 50 ns, T_A = 25°C			±3		V
I_{in}	Differential-input bias current	2	V_{CC1} = 5.25 V, V_{CC2} = -5.25 V, V_{inD} = 0 mV			30	75	μA
I_{DI}	Differential-input offset current	2	V_{CC1} = 5.25 V, V_{CC2} = -5.25 V			0.5		μA
z_{inD}	Differential-input impedance	none	f = 1 kHz			2		kΩ
$V_{in(1)}$	Logical 1 input voltage (strobe inputs)	13	V_{CC1} = 4.75 V, V_{CC2} = -4.75 V, $V_{in(0)}$ = 0.8 V		2			V
$V_{in(0)}$	Logical 0 input voltage (strobe inputs)	13	V_{CC1} = 4.75 V, V_{CC2} = -4.75 V, $V_{in(1)}$ = 2 V				0.8	V
$I_{in(0)}$	Logical 0 level input current (strobe inputs)	13	V_{CC1} = 5.25 V, V_{CC2} = -5.25 V, $V_{in(0)}$ = 0.4 V			-1	-1.6	mA
$I_{in(1)}$	Logical 1 level input current (strobe inputs)	13	V_{CC1} = 5.25 V, V_{CC2} = -5.25 V, $V_{in(1)}$ = 2.4 V				40	μA
			V_{CC1} = 5.25 V, V_{CC2} = -5.25 V, $V_{in(1)} = V_{CC1}$				1	mA
$V_{out(1)}$	Logical 1 output voltage	14	V_{CC1} = 4.75 V, V_{CC2} = -4.75 V, I_{load} = -400 μA, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V		2.4	3.9		V
$V_{out(0)}$	Logical 0 output voltage	14	V_{CC1} = 4.75 V, V_{CC2} = -4.75 V, I_{sink} = 16 mA, $V_{in(0)}$ = 0.8 V			0.25	0.4	V
I_{OS}	Output short-circuit current	15	V_{CC1} = 5.25 V, V_{CC2} = -5.25 V		-2.1		-3.5	mA
I_{CC1}	V_{CC1} supply current	6	T_A = 25°C			25		mA
I_{CC2}	V_{CC2} supply current	6	T_A = 25°C			-15		mA

NOTES: 1. The differential-input threshold voltage (V_T) is defined as the d-c input voltage (V_{in}) required to force the output of the sense amplifier to the logic gate threshold voltage level.

2. Common-mode input firing voltage is the common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable signal present.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = -5 V, T_A = 25°C (see figure 18)

PROPAGATION DELAY TIMES						
SYMBOL	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(1)D}$	A_1-A_2 or B_1-B_2	A or B			75	40	ns
$t_{pd(0)D}$					20		ns
$t_{pd(1)S}$	STROBE A or B	A or B			15	30	ns
$t_{pd(0)S}$					20		ns

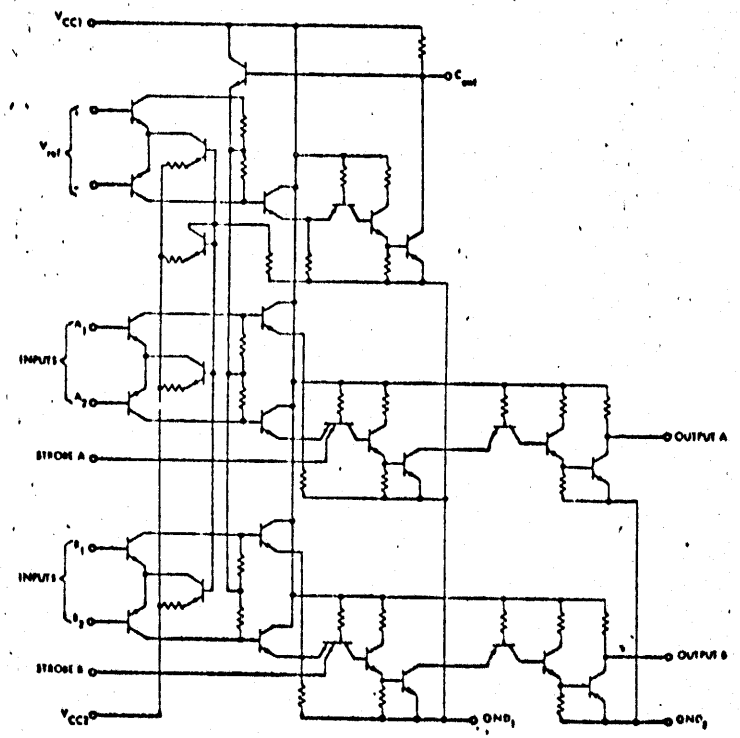
typical recovery and cycle times, V_{CC1} = 5 V, V_{CC2} = -5 V, T_A = 25°C

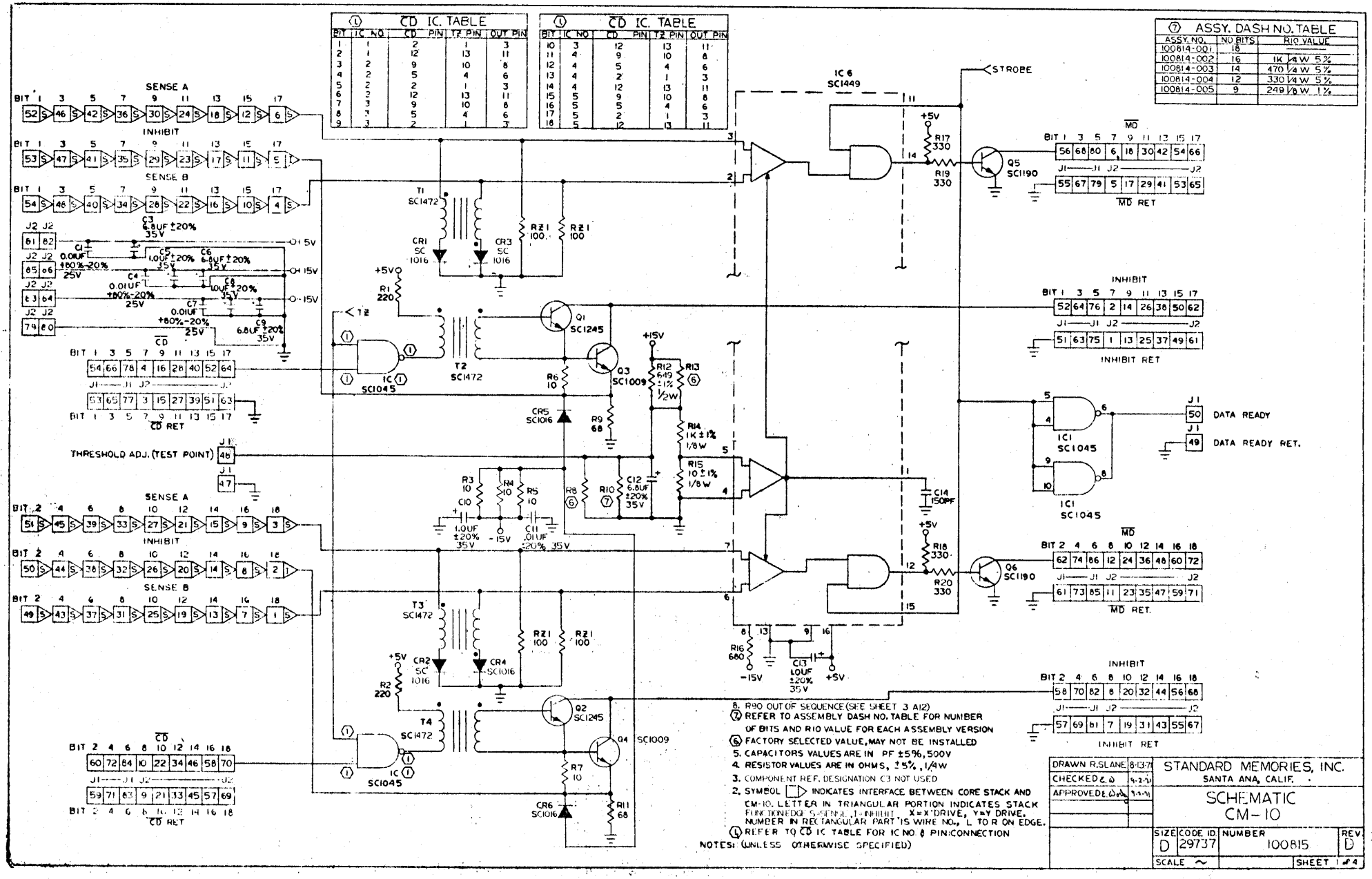
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (See Note 3)	V_{inD} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orCM}	Common-mode-input overload recovery time (See Note 4)	V_{inCM} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

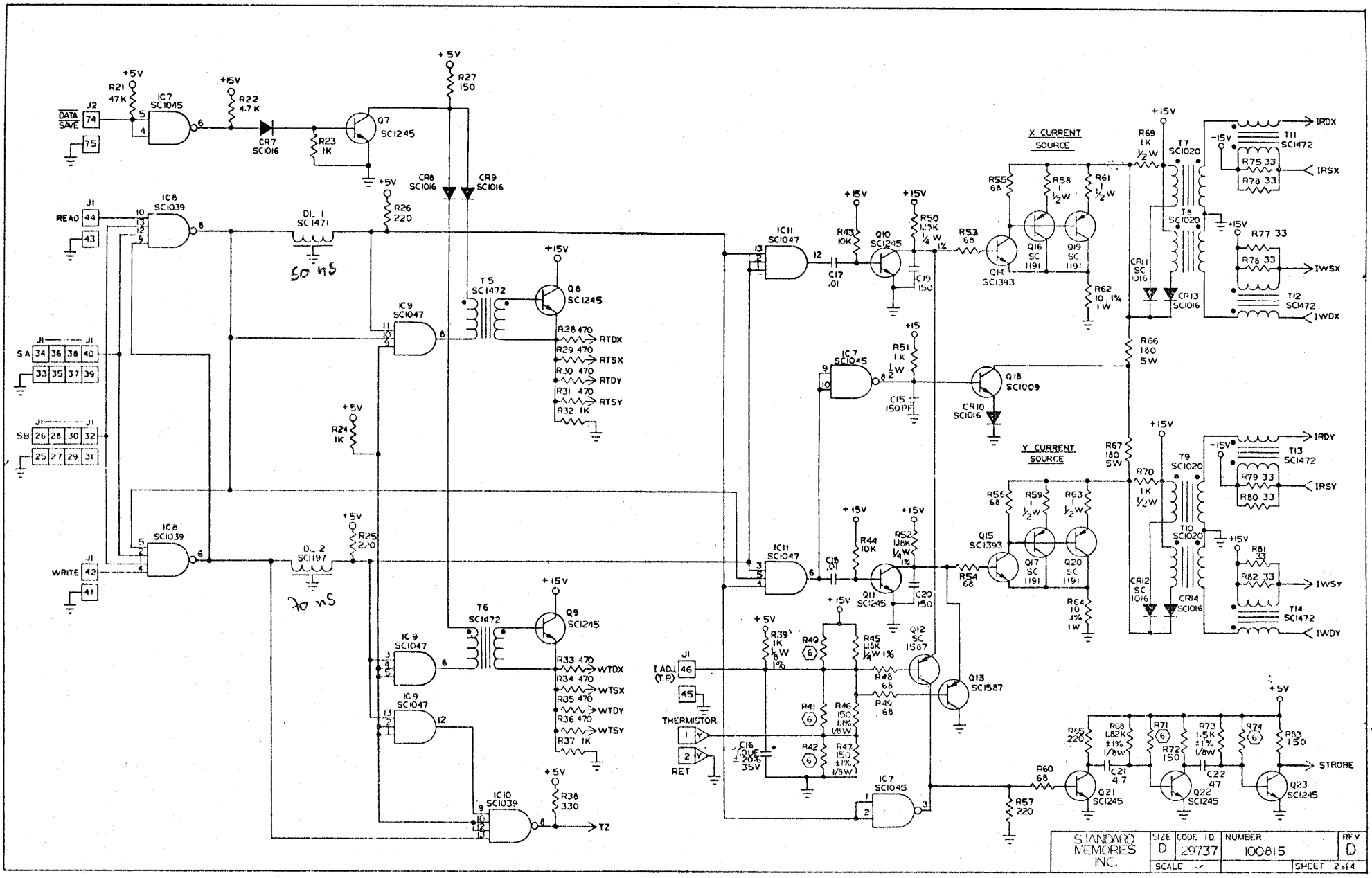
NOTES: 3. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.

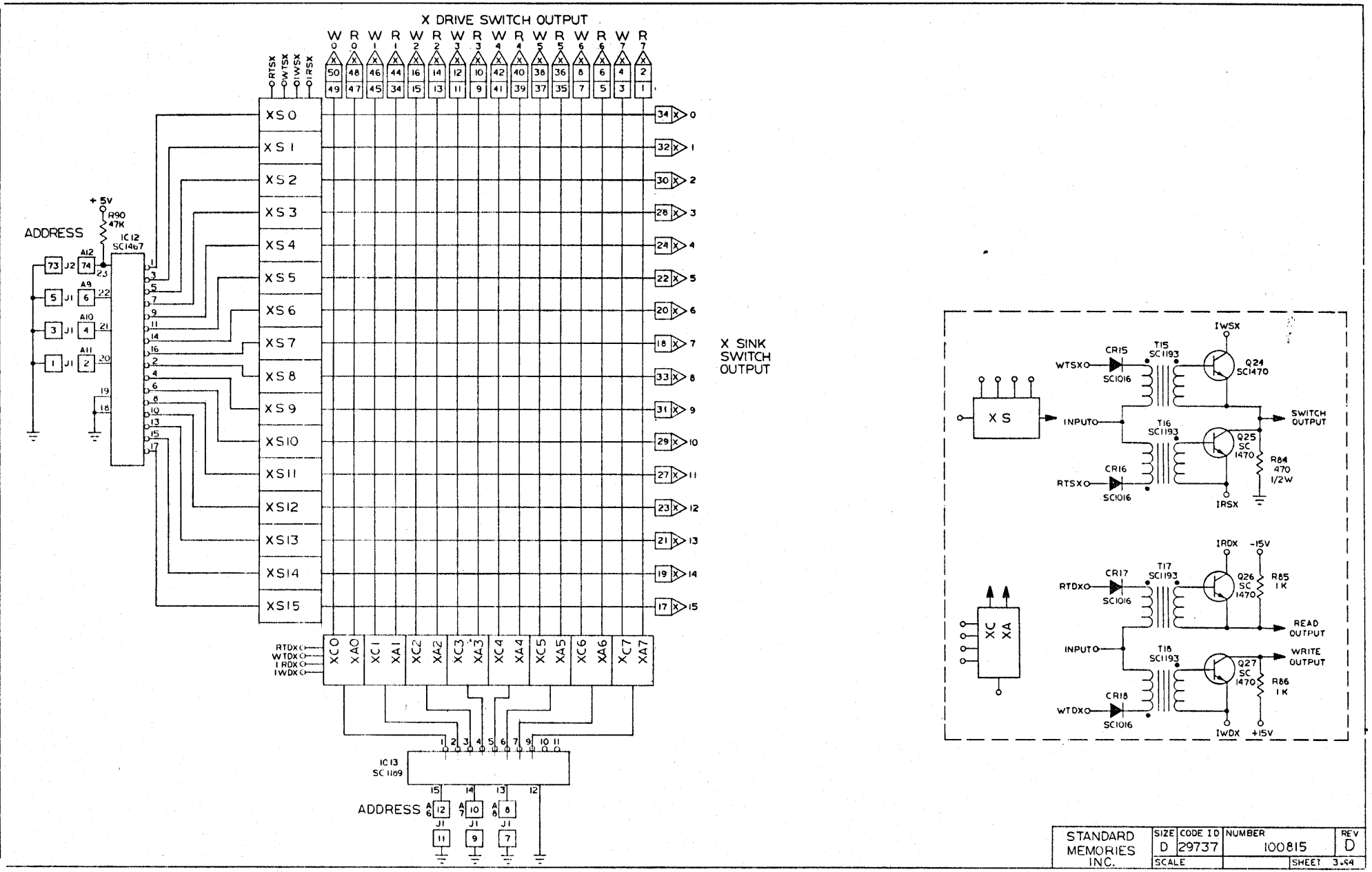
4. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic diagram

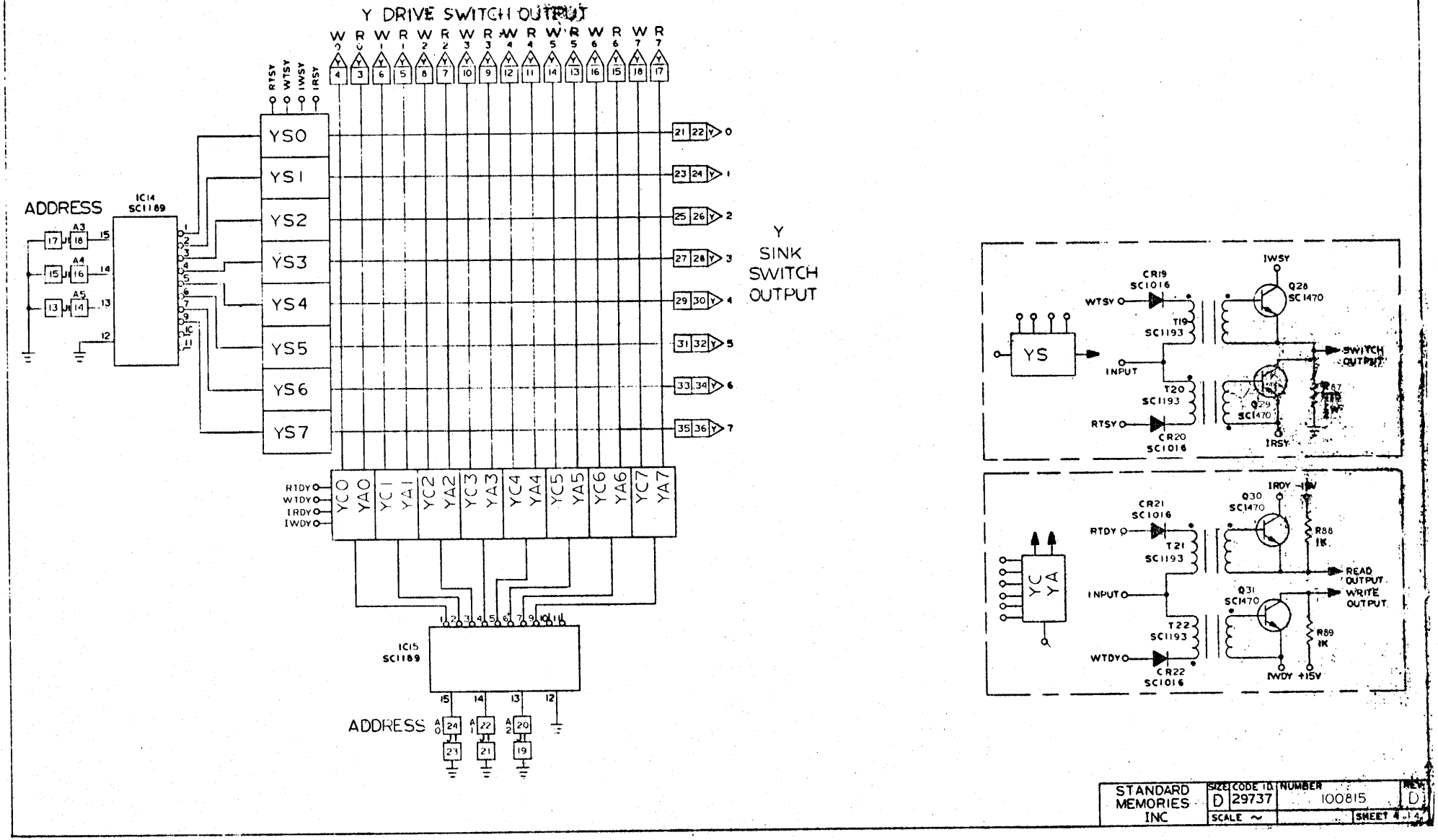



① CD IC. TABLE
BIT | IC NO | CD PIN | T2 PIN | OUT PIN
1 | 1 | 2 | 1 | 3
2 | 1 | 12 | 13 | 11
3 | 2 | 9 | 10 | 8
4 | 2 | 5 | 4 | 6
5 | 3 | 2 | 1 | 3
6 | 3 | 12 | 13 | 11
7 | 3 | 9 | 10 | 8
8 | 3 | 5 | 4 | 6
9 | 3 | 2 | 1 | 3
① CD IC. TABLE
BIT | IC NO | CD PIN | T2 PIN | OUT PIN
10 | 3 | 12 | 13 | 11
11 | 4 | 9 | 10 | 8
12 | 4 | 5 | 4 | 6
13 | 4 | 2 | 1 | 3
14 | 4 | 12 | 13 | 11
15 | 5 | 9 | 10 | 8
16 | 5 | 5 | 4 | 6
17 | 5 | 2 | 1 | 3
18 | 5 | 12 | 13 | 11
⑦ ASSY. DASH NO. TABLE
ASSY. NO. | NO BITS | R10 VALUE
100814-001 | 18 |
100814-002 | 16 | 1K 1/4W 5%
100814-003 | 14 | 470 1/4W 5%
100814-004 | 12 | 330 1/4W 5%
100814-005 | 9 | 249 1/8W 1%
SENSE A
INHIBIT
SENSE B
INHIBIT
SENSE A
INHIBIT
SENSE B
CD
CD RET
MD
MD RET
INHIBIT
INHIBIT RET
MD
MD RET
INHIBIT
INHIBIT RET
IC 6 SC1449
STROBE
T1 SC1472
T2 SC1472
T3 SC1472
T4 SC1472
IC ① SC1045
IC ① SC1045
IC ① SC1045
IC ① SC1045
Q1 SC1245
Q2 SC1245
Q3 SC1009
Q4 SC1009
Q5 SC1190
Q6 SC1190
CR1 SC 1016
CR2 SC 1016
CR3 SC 1016
CR4 SC1016
CR5 SC1016
CR6 SC1016
THRESHOLD ADJ. (TEST POINT)
DATA READY
DATA READY RET.
+5V
+15V
-15V
R1 220
R2 220
R3 10
R4 10
R5 10
R6 10
R7 10
R8
R9 68
R10
R11 68
R12 649 ±1% 1/2W
R13
R14 1K ±1% 1/8W
R15 10 ±1% 1/8W
R16 680
R17 330
R18 330
R19 330
R20 330
RZ1 100
RZ1 100
RZ1 100
C1 0.01UF +80%-20% 25V
C2 0.01UF +80%-20% 25V
C3 6.8UF ±20% 35V
C4 0.01UF +80%-20% 25V
C5 1.0UF ±20% 35V
C6 6.8UF ±20% 35V
C7 0.01UF +80%-20% 25V
C8 1.0UF ±20% 35V
C9 6.8UF ±20% 35V
C10 1.0UF ±20% 35V
C11 .01UF ±20% 35V
C12 6.8UF ±20% 35V
C13 1.0UF ±20% 35V
C14 150PF
8. R90 OUT OF SEQUENCE (SEE SHEET 3 A12)
⑦ REFER TO ASSEMBLY DASH NO. TABLE FOR NUMBER OF BITS AND R10 VALUE FOR EACH ASSEMBLY VERSION
⑥ FACTORY SELECTED VALUE, MAY NOT BE INSTALLED
5. CAPACITORS VALUES ARE IN PF ±5%, 500V
4. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W
3. COMPONENT REF. DESIGNATION C3 NOT USED
2. SYMBOL INDICATES INTERFACE BETWEEN CORE STACK AND CM-10. LETTER IN TRIANGULAR PORTION INDICATES STACK FUNCTION EDGE S=SENSE, I=INHIBIT, X=X DRIVE, Y=Y DRIVE, NUMBER IN RECTANGULAR PART IS WIRE NO., L TO R ON EDGE.
① REFER TO CD IC TABLE FOR IC NO & PIN CONNECTION
NOTES: (UNLESS OTHERWISE SPECIFIED)
DRAWN R.SLANE 8-13-71
CHECKED
APPROVED
STANDARD MEMORIES, INC.
SANTA ANA, CALIF.
SCHEMATIC
CM-10
SIZE D
CODE ID 29737
NUMBER 100815
REV D
SCALE ~
SHEET 1 of 4


+5V
+15V
-15V
R21 47K
IC7 SC1045
R22 4.7K
CR7 SC1016
R23 1K
Q7 SC1245
R27 150
CR8 SC1016
CR9 SC1016
R26 220
DATA SAVE
J2
74
75
J1
READ
44
43
IC8 SC1039
DL 1 SC1471
50 nS
IC9 SC1047
T5 SC1472
Q8 SC1245
R28 470 RTDX
R29 470 RTSX
R30 470 RTDY
R31 470 RTSY
R32 1K
R24 1K
SA
34 36 38 40
33 35 37 39
SB
26 28 30 32
25 27 29 31
WRITE
42
41
DL 2 SC1197
70 nS
R25 220
T6 SC1472
Q9 SC1245
R33 470 WTDX
R34 470 WTSX
R35 470 WTDY
R36 470 WTSY
R37 1K
IC10 SC1039
R38 330
TZ
IC11 SC1047
R43 10K
Q10 SC1245
R50 1.5K 1/4W 1%
R52 68
C17 .01
C19 150
X CURRENT SOURCE
R55 68
R58 1/2W
R61 1/2W
Q14 SC1393
Q16 SC 1191
Q19 SC 1191
R62 10, 1% 1W
R69 1K 1/2W
T7 SC1020
T8 SC1020
T11 SC1472
R75 33
R76 33
R77 33
R78 33
T12 SC1472
CR11 SC 1016
CR13 SC1016
IRDX
IRSX
IWSX
IWDX
R66 180 5W
R51 1K 1/2W
C15 150PF
Q18 SC1009
CR10 SC1016
Y CURRENT SOURCE
R56 68
R59 1/2W
R63 1/2W
Q15 SC1393
Q17 SC 1191
Q20 SC 1191
R64 10 1% 1W
R67 180 5W
R70 1K 1/2W
T9 SC1020
T10 SC1020
T13 SC1472
R79 33
R80 33
R81 33
R82 33
T14 SC1472
CR12 SC 1016
CR14 SC1016
IRDY
IRSY
IWSY
IWDY
R44 10K
R52 1.8K 1/4W 1%
C18 .01
C20 150
Q11 SC1245
R54 68
R39 1K 1/8W 1%
R40 6
R45 1.5K 1/4W 1%
Q12 SC 1587
Q13 SC1587
R48 68
R49 68
R41 6
R46 150 ±1% 1/8W
R42 6
R47 150 ±1% 1/8W
J1
I ADJ (T.P.)
46
45
THERMISTOR
1
2
RET
C16 .OUE ±20% 35V
IC7 SC1045
R60 68
R57 220
R65 220
R68 1.82K ±1% 1/8W
R71 6
R72 150
R73 1.5K ±1% 1/8W
R74 6
R83 150
C21 47
C22 47
Q21 SC1245
Q22 SC1245
Q23 SC1245
STROBE
STANDARD MEMORIES INC.
SIZE D
CODE ID 29737
NUMBER 100815
REV D
SCALE
SHEET 2 of 4



STANDARD MEMORIES INC.	SIZE	CODE ID	NUMBER	REV
	D	29737	100815	D
	SCALE			SHEET 3 of 4



STANDARD MEMORIES INC	SIZE D	CODE ID 29737	NUMBER 100815	REV D
	SCALE ~		SHEET 4 of 4	

FIG. 4

MODULE SELECTION

Selection of a module is accomplished by satisfying the "AND" condition of it's two select inputs, SA and SB. Four pins each at the I/O connector are assigned to SA and SB to facilitate an externally wired 4 X 4 selection matrix at the connector interface. Unique selection of one module with up to 16 modules tied together via party line is thereby accomplished.

A typical 1 of 16 selection truth table is listed below.

	Select A				Select B				Selected Module																			
J1 Pin	40	38	36	34	32	30	28	26	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16				
	1				1				1																			
		1			1					1																		
			1		1						1																	
				1	1							1																
1						1							1															
	1					1								1														
		1				1									1													
			1			1										1												
1							1										1											
	1						1											1										
		1					1												1									
			1				1													1								
1								1													1							
	1							1														1						
		1						1															1					
			1					1																1				

NOTE: If either SA or SB inputs are not actively used, tie up to +5V through a 1KΩ resistor.

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