Der mangler

BCT 401 og

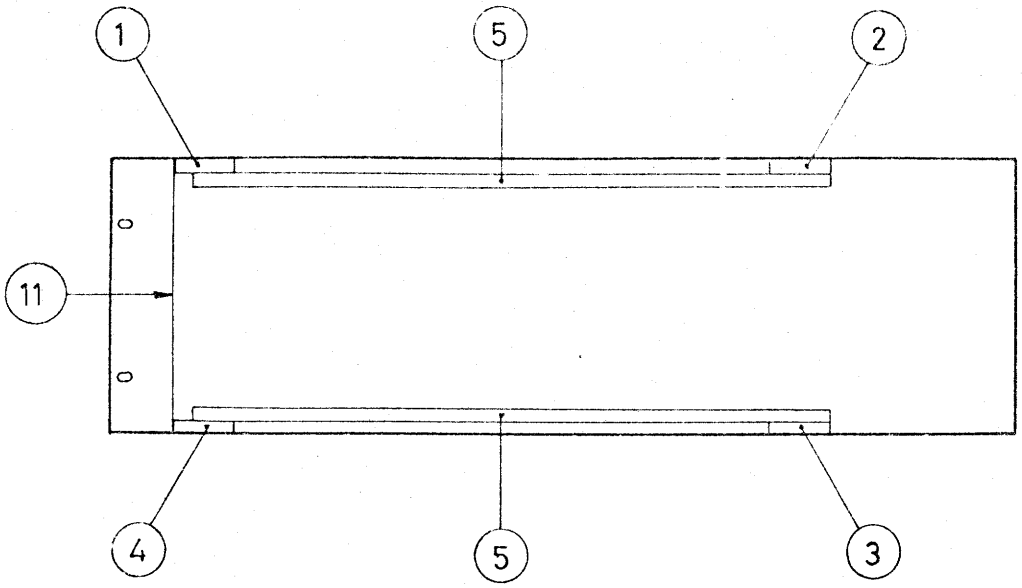
PPG

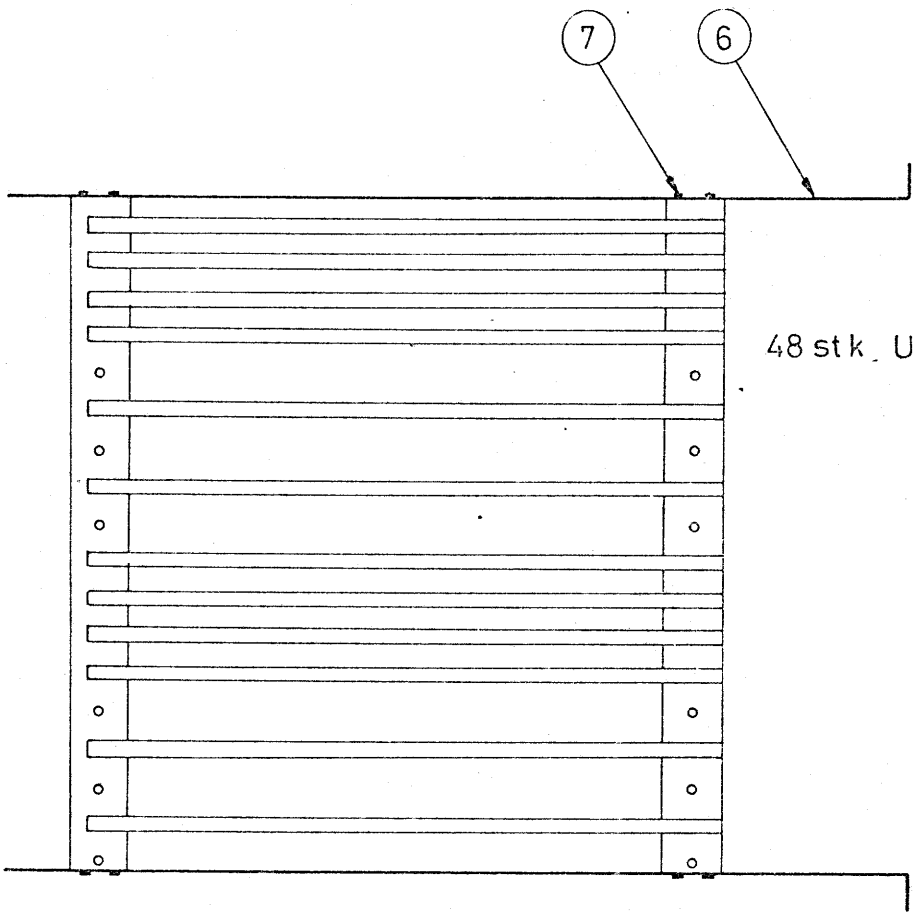
og

HSAI, MCS

i mappen

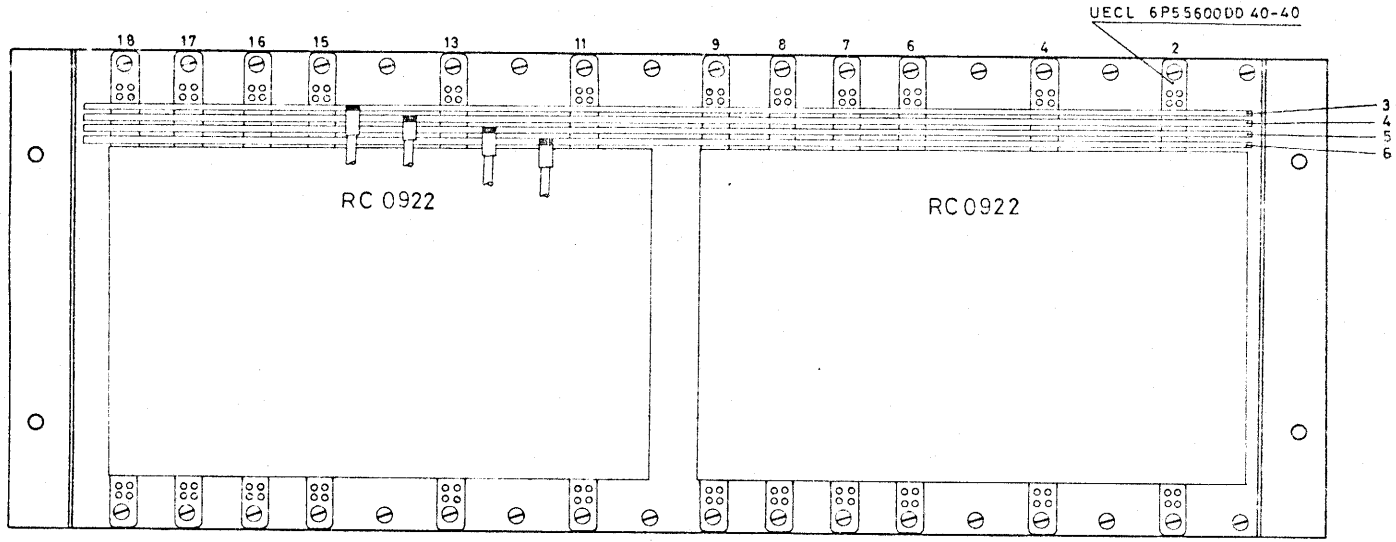
DATAMATICS



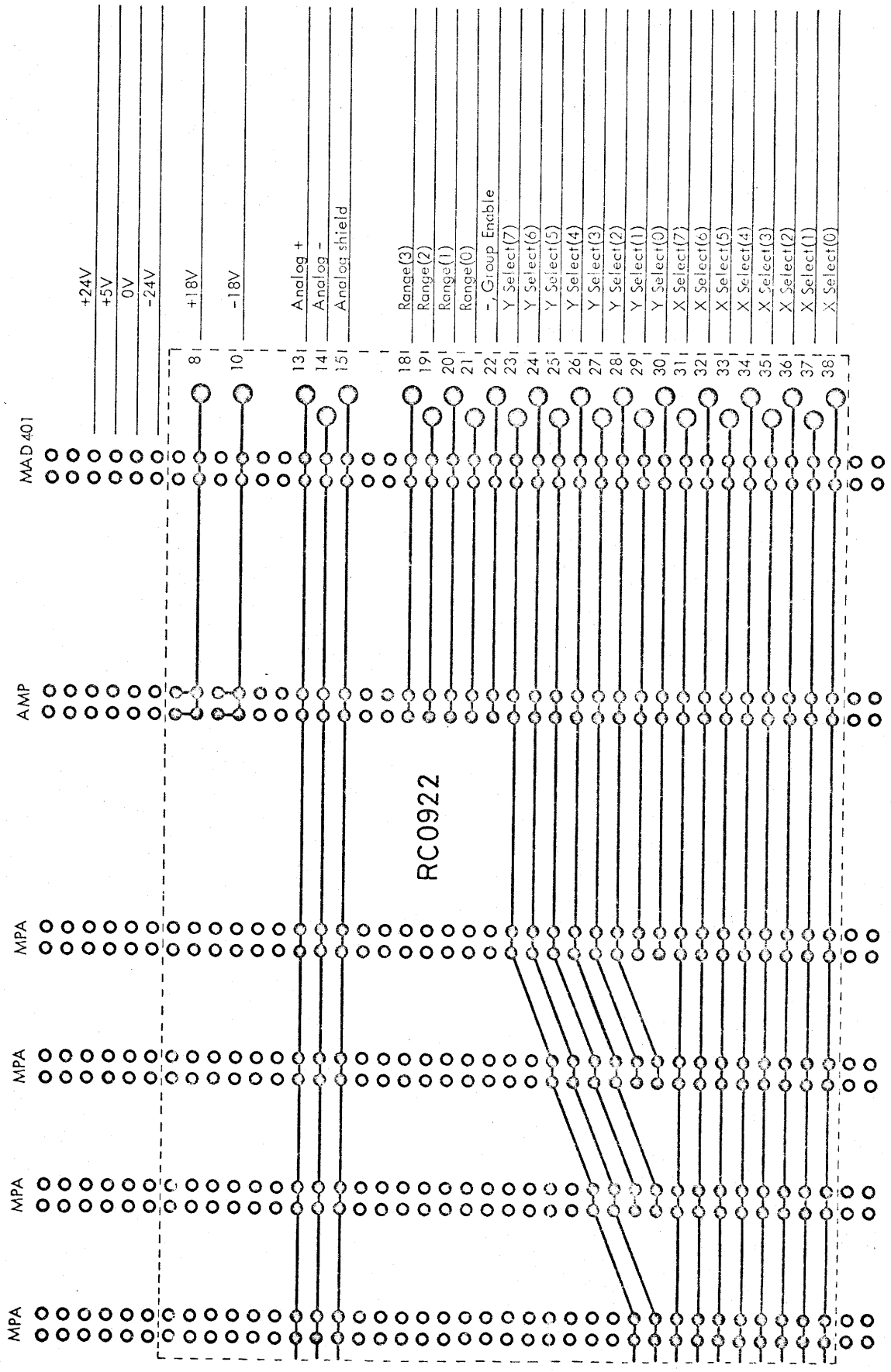


48 stk. UHJ M4x8

Unit	Designed 190370SK	CHS 401 MEKANISK SAMLINGSTEGNING	Drawing No V21334
ASEA	Approved		Drawn by 190370MK
	Checked 23.11.70 SK		Checked
			Sheets / Sheet



Unit: CENTRALE	Designed 170370SK Approved Checked 23.11.70SK Last Revision	CHS 401 EL MONTERINGSTEGN.	Drawing No V[illegible] Drawn by 160470MK Checked Sheet

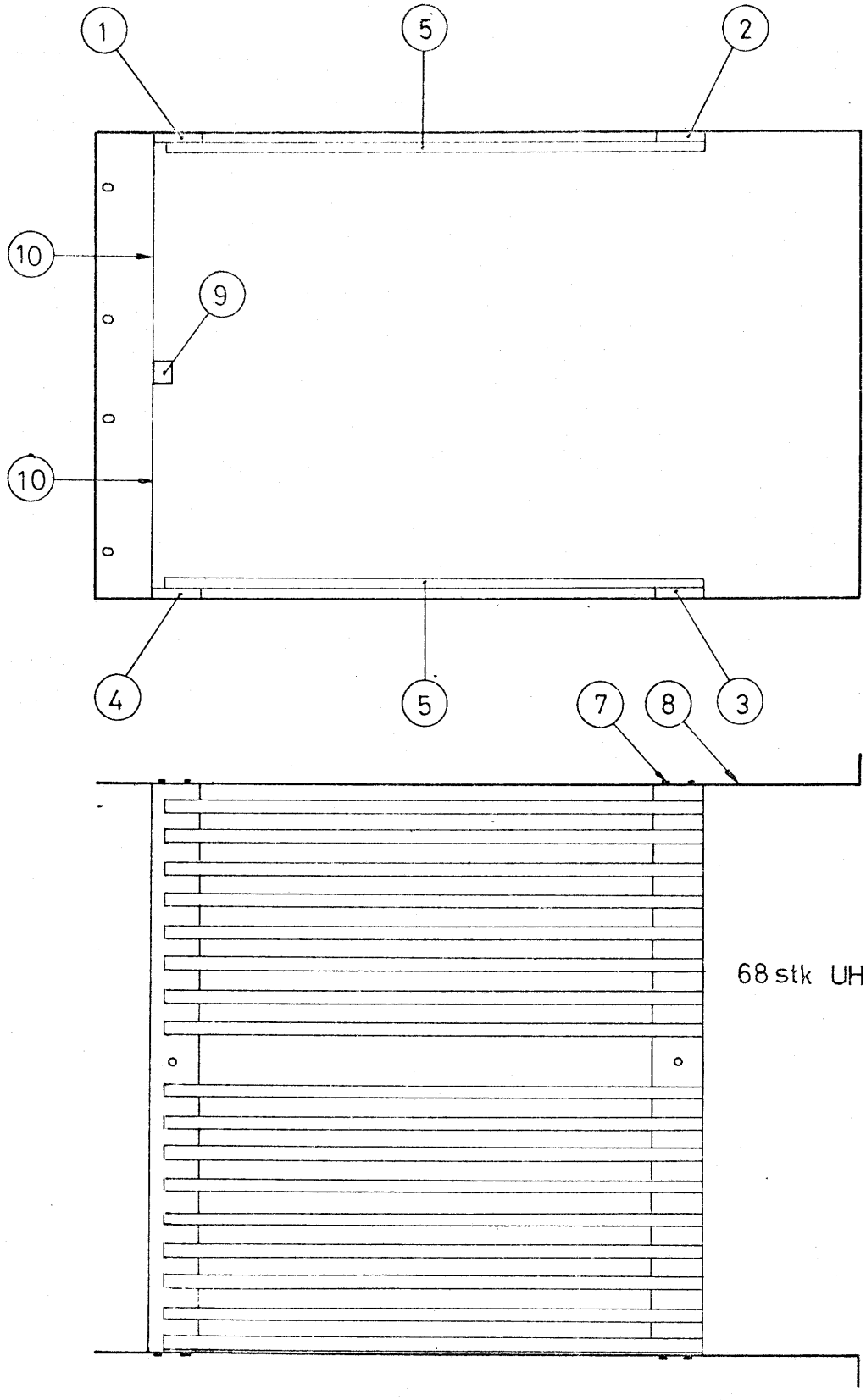


RC 4000

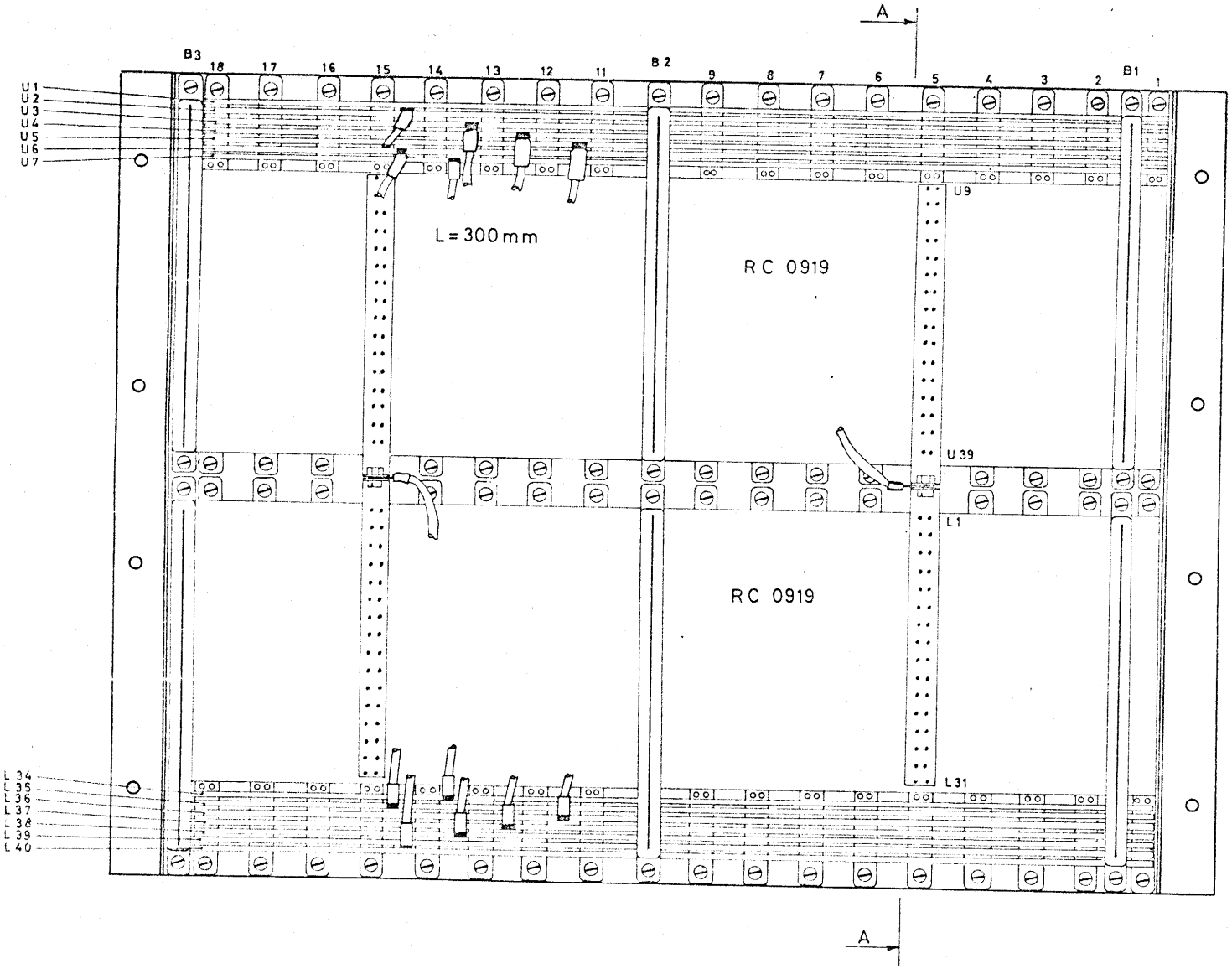
V12165

Motherboard for MPA, AMP and MAD

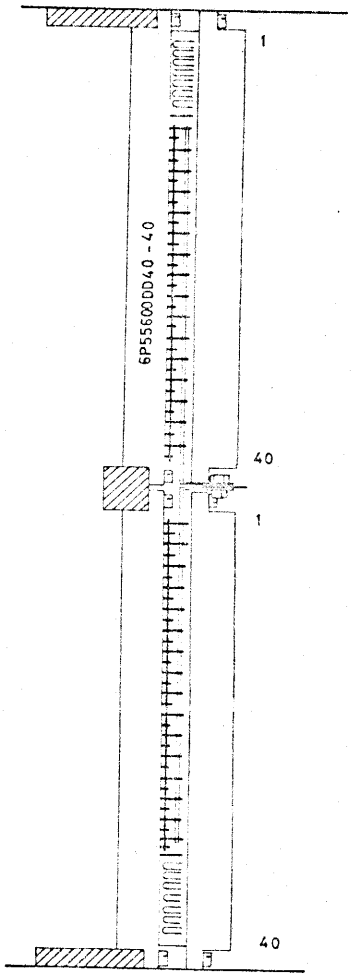
PCBA Circuit Diagram



Unit:	Designed 190370SK	CHS 404 MEKANISK SAMLINGSTEGNING	Drawing No V2:336
SBCNE CENTRALEN	Approved		Drawn by 1903 0MK
	Checked 23.11.70SK		Checked
	Last Revision		Sheets / Sheet



snit A-A



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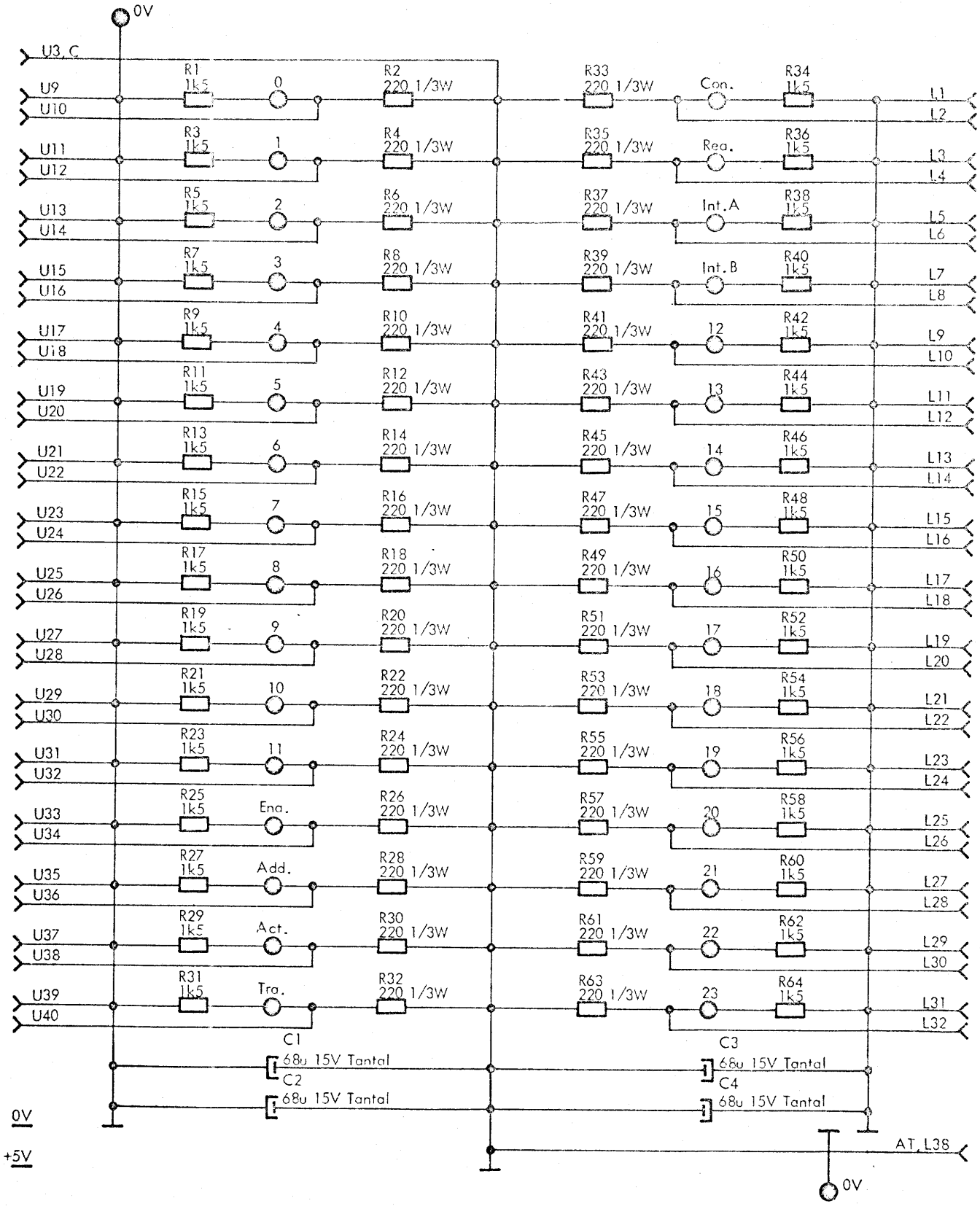
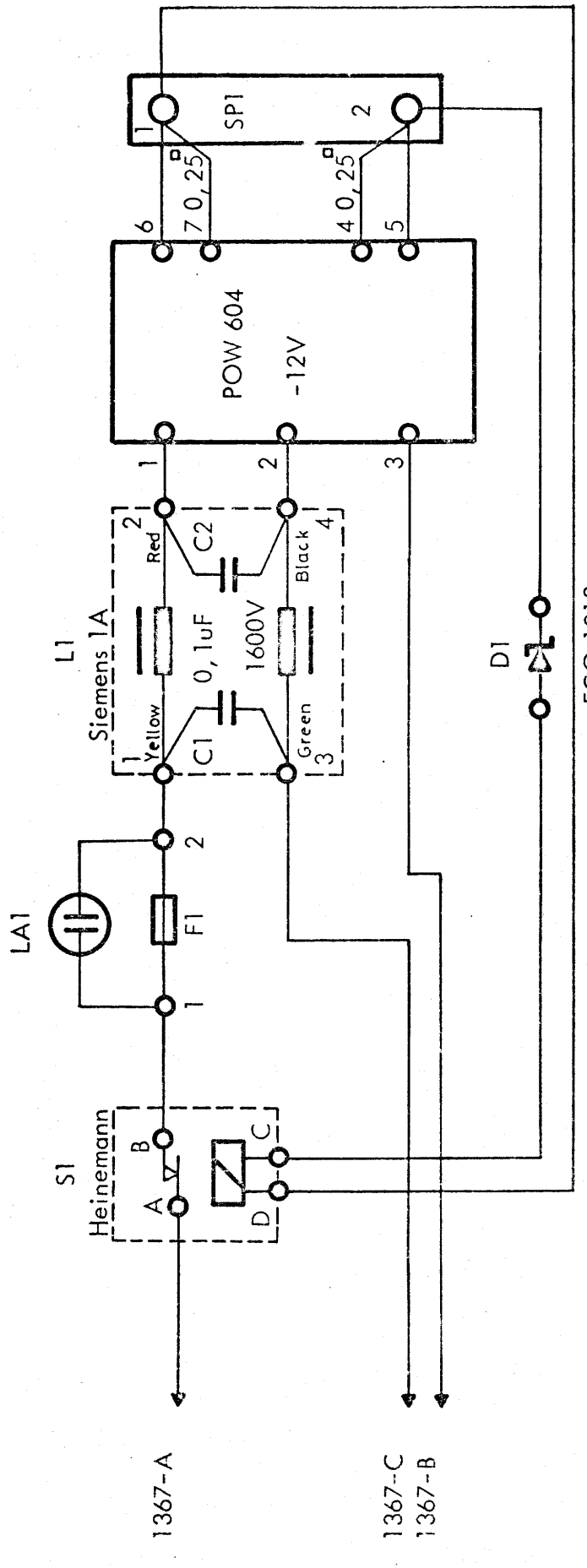


RC 4000

Termination board for CHS 404

V12145

PCBA Circuit Diagram



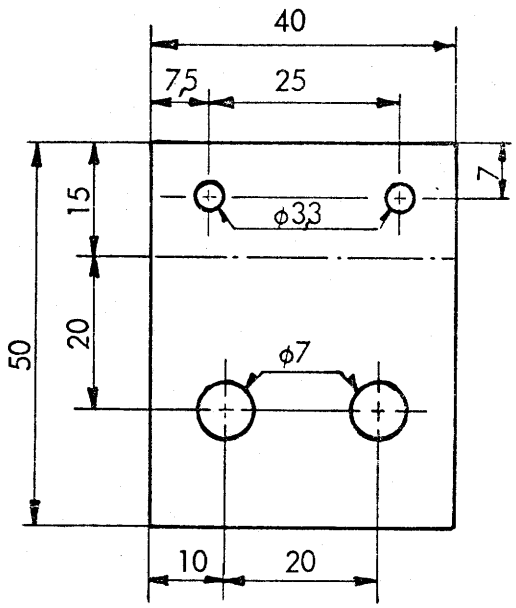
Ikke angivne tværsnit: 1 □
Trådtype overalt: soflex type TK varmebestandig

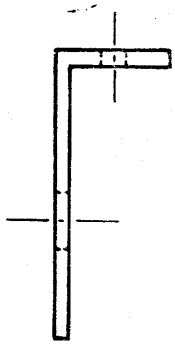
POW 411

V21304

POW 411 Power Supply

Circuit Diagram





Pos.	4	Materiale	2 mm Alu
Målforhold	1:1	Overflade	Lakeres sort
Tol. i koordinatet		Bemærkt	

Unit:	Designed 200270AL	OPSPÆNDINGSVINKEL	Drawing No V21305
§ BEGNB CENTRALEN	Approved	for ZENERDIODER	Drawn by AL
	Checked		Checked
	Last Revision		Sheets / Sheet

Form 308-AA-3-3

TEGN NR	POS	BESKRIVELSE	FREMSTILLES AF	
V11778	1	FORPLADE	3mm ALU. PLADE	1
V11776	2	BAGPLADE	1mm JERNPLADE	1
V11772	3	TOPPLADE	PERFORERET JERNPLADE no1155F	1
V21305	4	OPSPÆNDINGSVINKEL	2mm ALU. PLADE	1
	5	TPP 20 PART NO16517.4MGTUBTARA		4

Unit: POW 411

ASCONE CENTRALEN

Designed 250270PTN

Approved

Checked

Last Revision

MATERIALELISTE.

Drawing No V21308

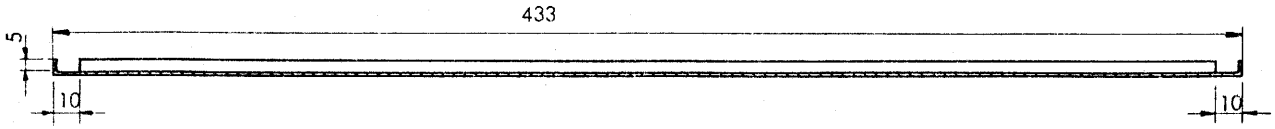
Drawn by

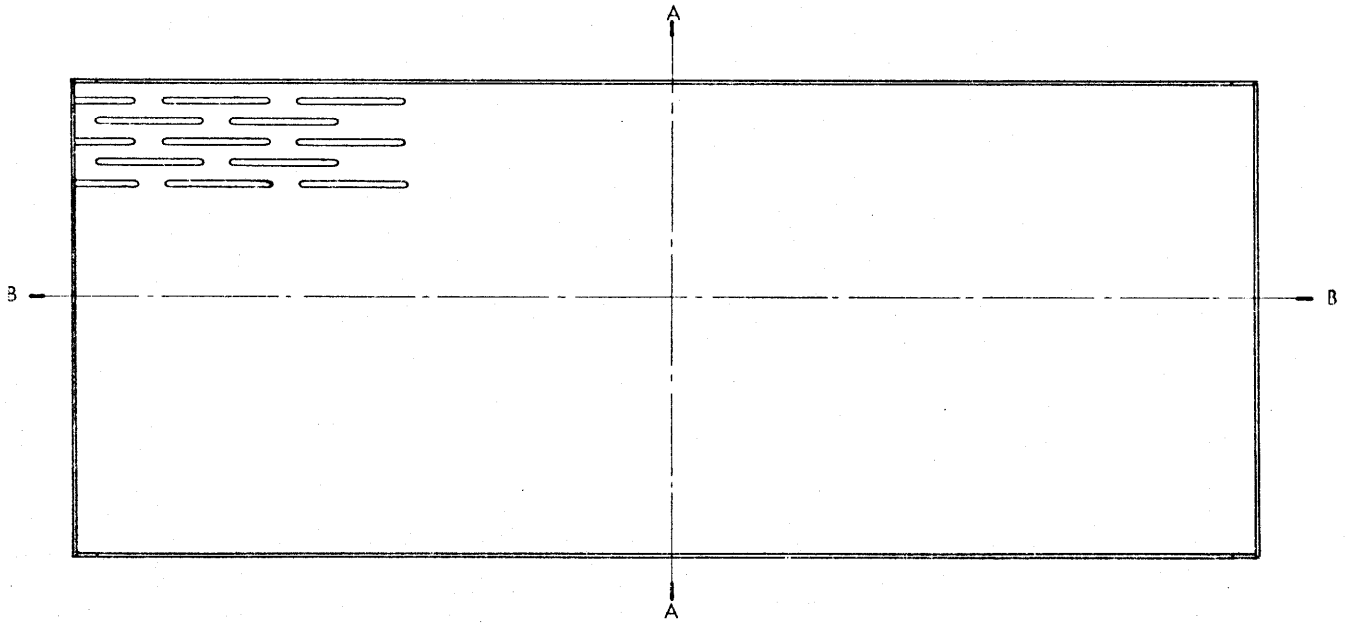
Checked

Sheets | Sheet

Form 3084-A 2.74

Snit BB

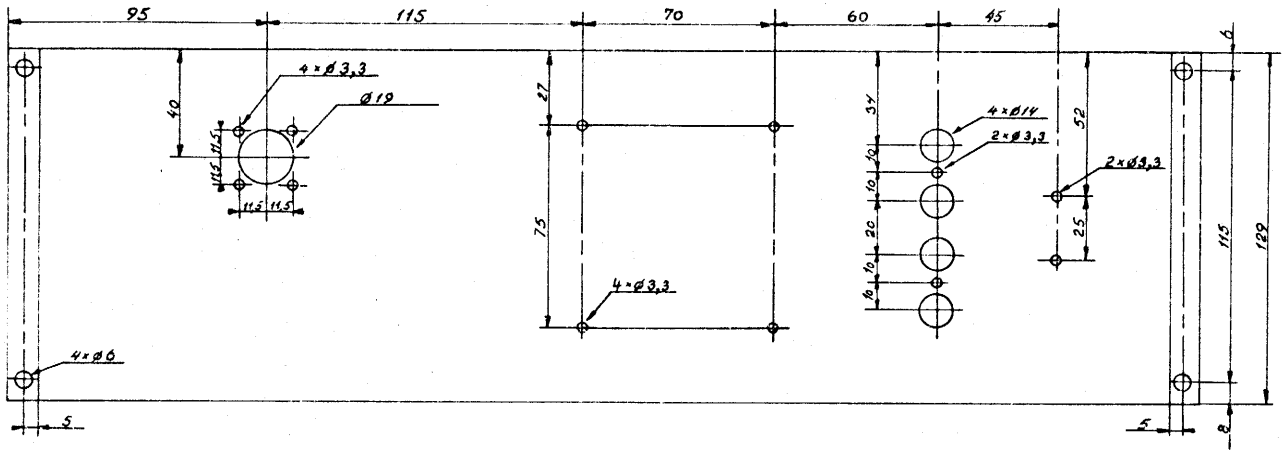


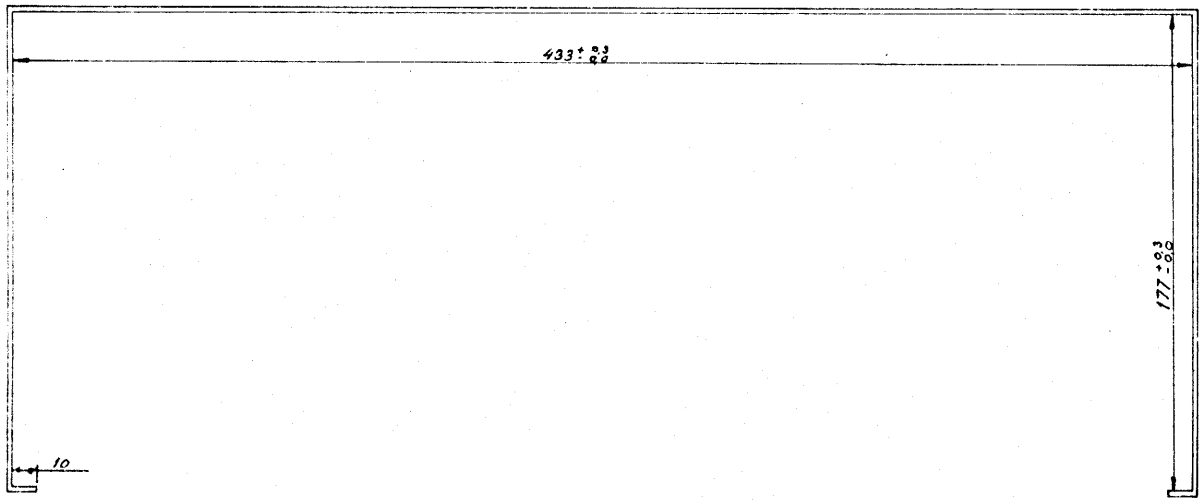


Snit AA

Pos.	3	Materiale	1 mm perforeret jernplade. Nr. 1155F
Målforhold	1:2	Overflade	(Efter sammensvejsning med bagplade) Sortlakeres
Tol. i koordinat	+00 / -03	Bemærk!	

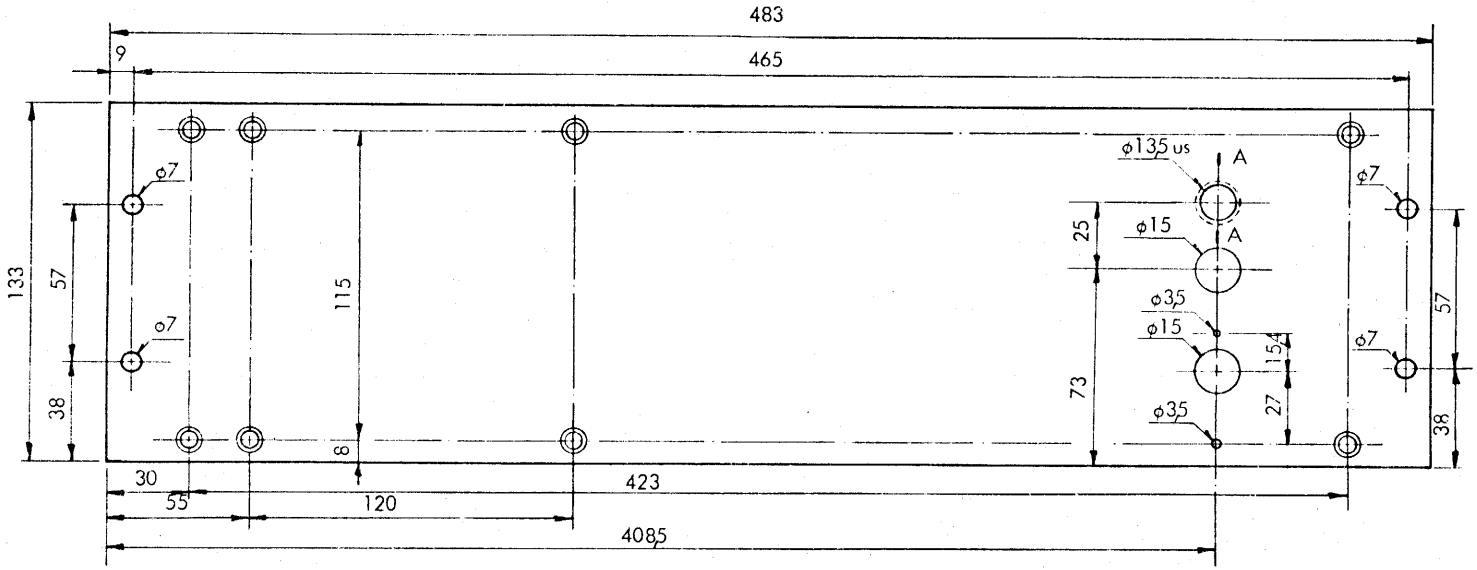
Unit:	Designed 190270AL	TOPPLADE	Drawing No V11772
	Approved		Drawn by AL
CENTRALEN	Checked		Checked
	Last Revision		Sheets / Sheet



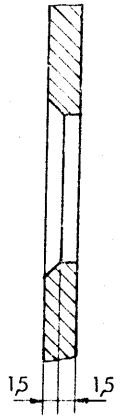


Pos.	2	Materiale	1mm Jernplade
Målforhold	1 : 2	Overflade	(efter sammensvejsning med topplade) Sortlakeres.
Tol. i koordinatmål	02	Bemærk!	Huller mrk. Ø6 monteres med Tubtara gevindnitte TPP20

Unit:	Designed 230270SB	BAGPLADE.	Drawing No V11776
CENTRALEN	Approved		Drawn by
	Checked		Checked
	Last Revision 310770HC		Sheets / Sheet

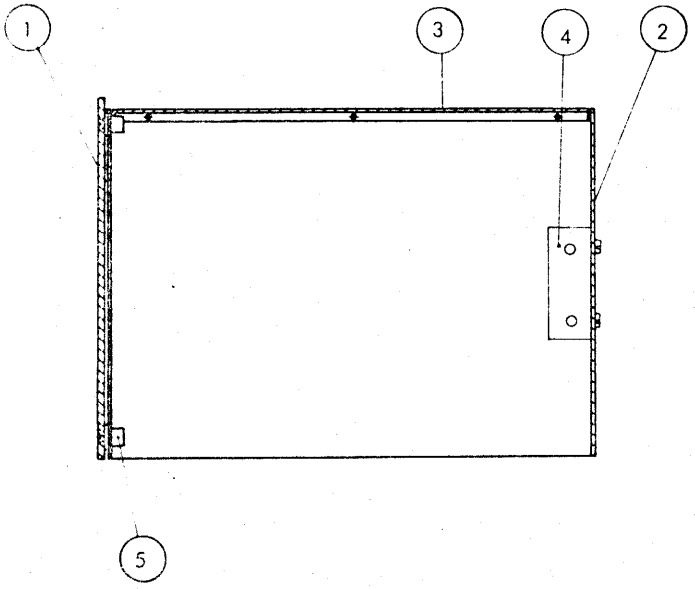


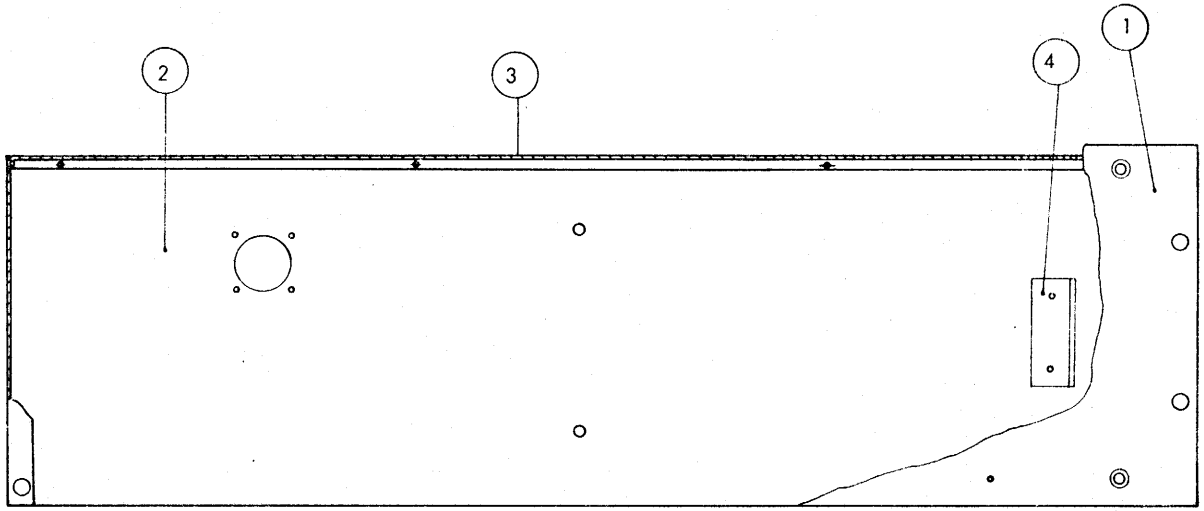
Snit AA



Pos.	1	Materiale	3 mm Alu
Målforhold	1:2	Overflade	Pudses og eloxeres hvid
Tol. i koordinatet	± 0,2	Bemærkl	Ubenævnte huller ø4 us

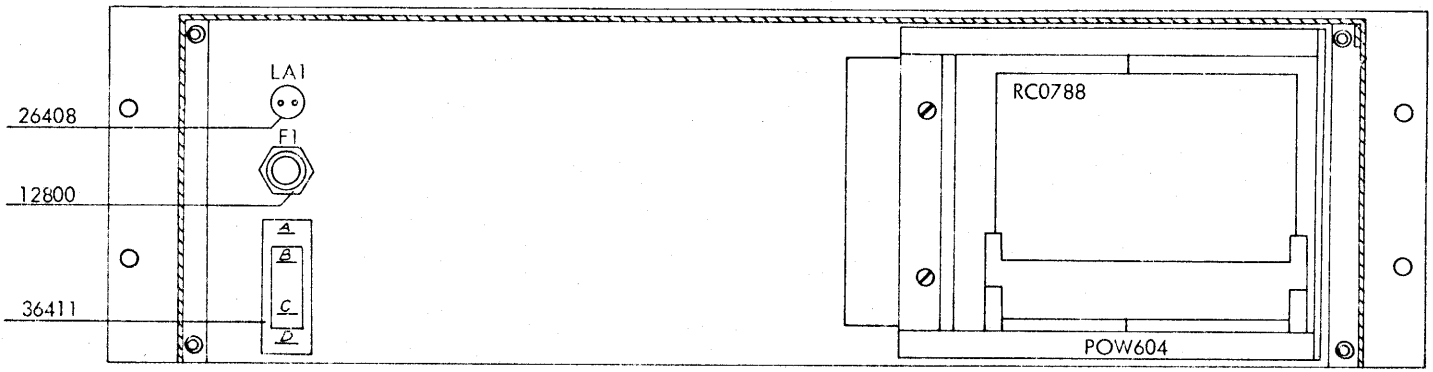
Unit: POW 411	Designed 200270AL	FORPLADE.	Drawing No. 11778
BBGNB CENTRALEN	Approved		Drawn by
	Checked		Checked
	Last Revision		Sheets / Sheet



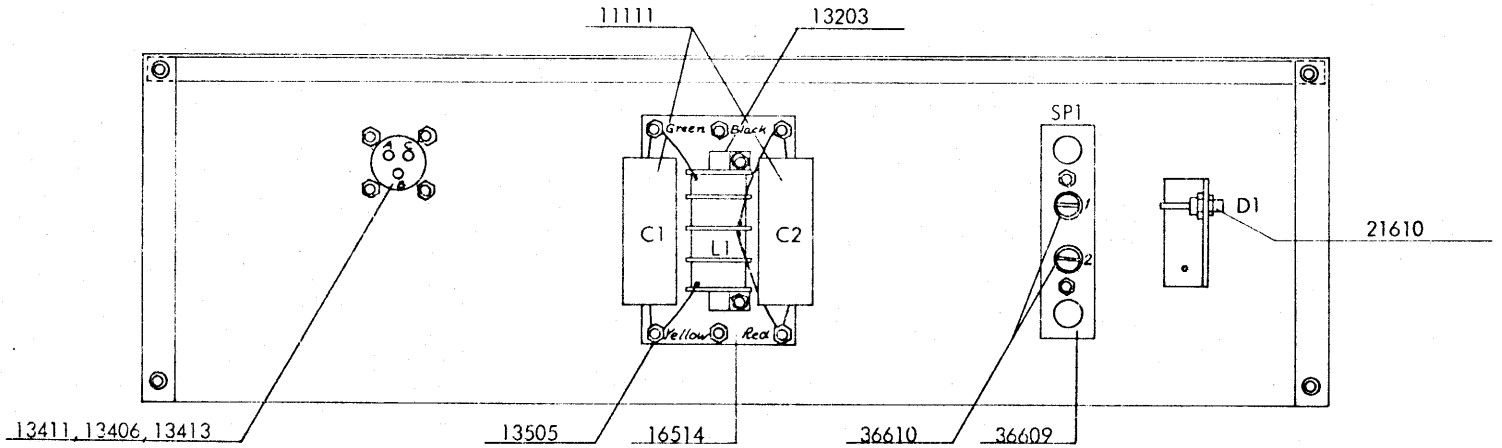


Unit. ELCONE CENTRALEN	Designed 200270AL Approved Checked Last Revision	SAMLINGSTEGNING.	Drawing No V11777 Drawn by Checked Sheets / Sheet

FORPLADE SET BAGFRA.



BAGPLADE SET BAGFRA.

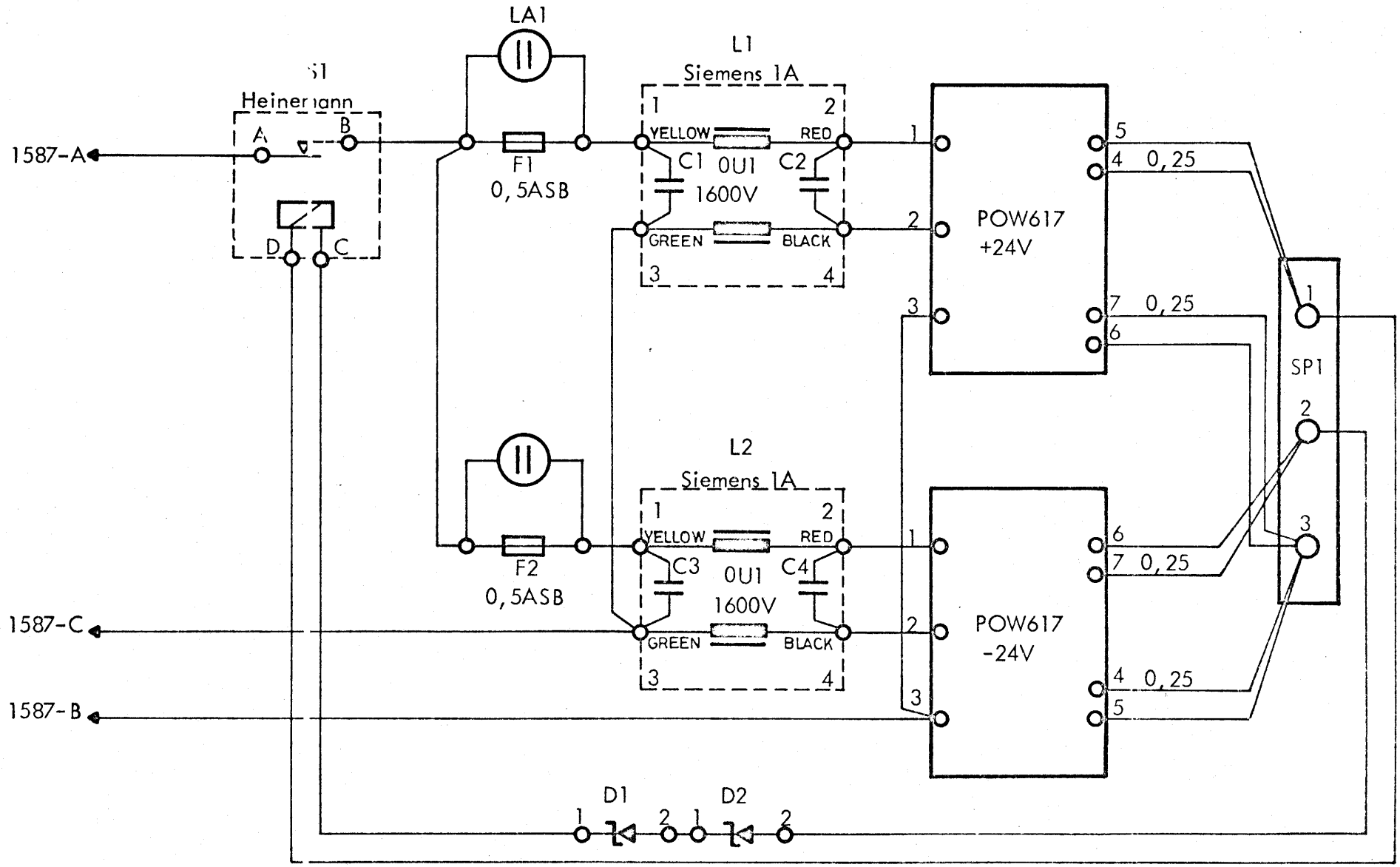


Unit POW 411	Designed 200270SB	KOMPONENTPLACERINGS TEGNING.	Drawing No V11773
RØNNE CENTRALEN	Approved		Drawn by
	Checked		Checked
	Last Revision		Sheets / Sheet

V21544

POW413-24V +24V 1A.

270170S 3

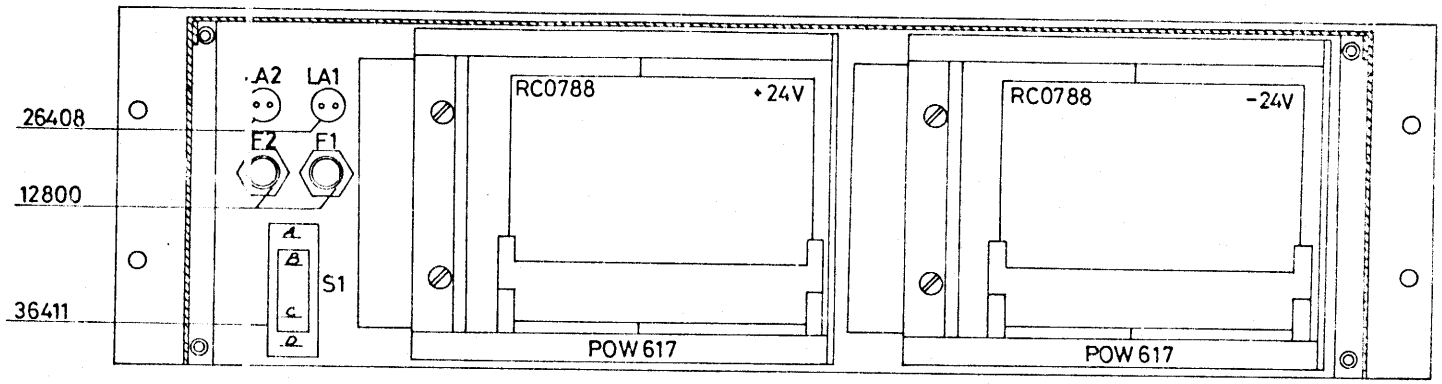


Ikke angivne tværsnit 1□

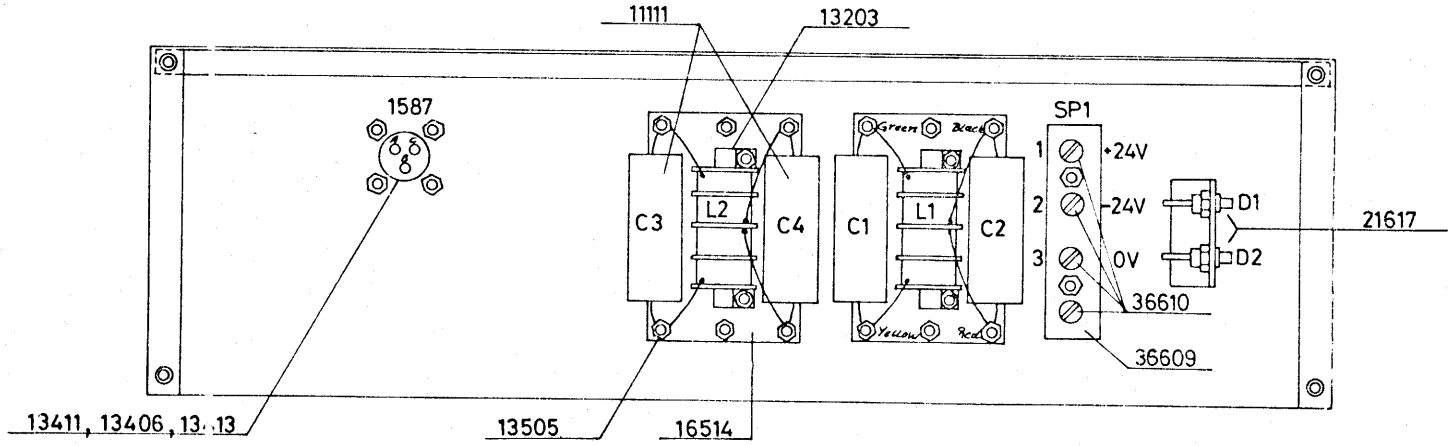
2 x ECO 1227

Trådtype overalt : Soflex type TK varmebestandig.

FRONTPANEL SEEN FROM THE BACK

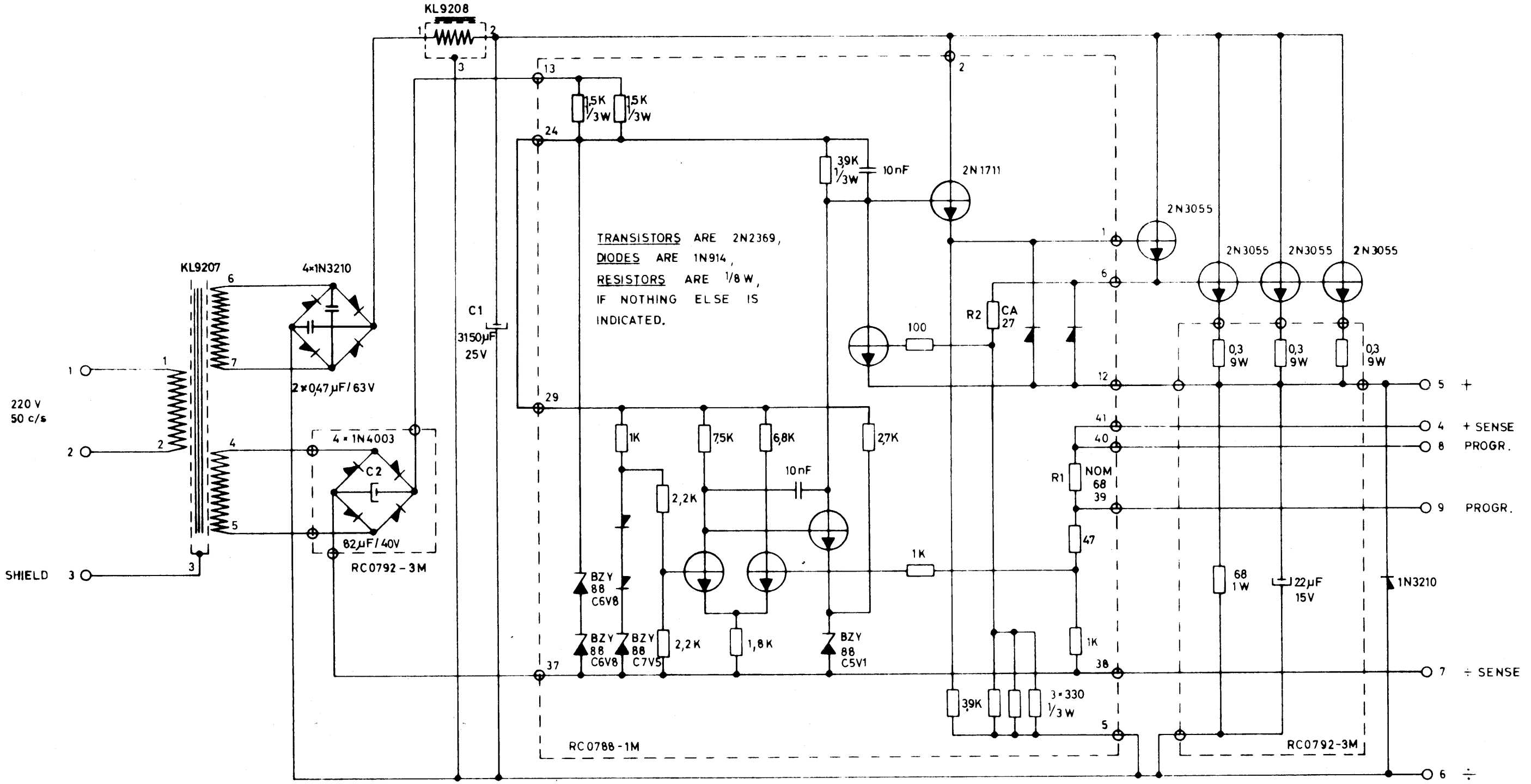


BACKPANEL SEEN FROM THE INNER SIDE



Unit: POW 413	Designed 180870 SSL	ASSEMBLY DRAWING	Drawing No V11993
A/S REGNE CENTRALEN	Approved		Drawn by
	Checked		Checked
	Last Revision		Sheets / Sheet

A3



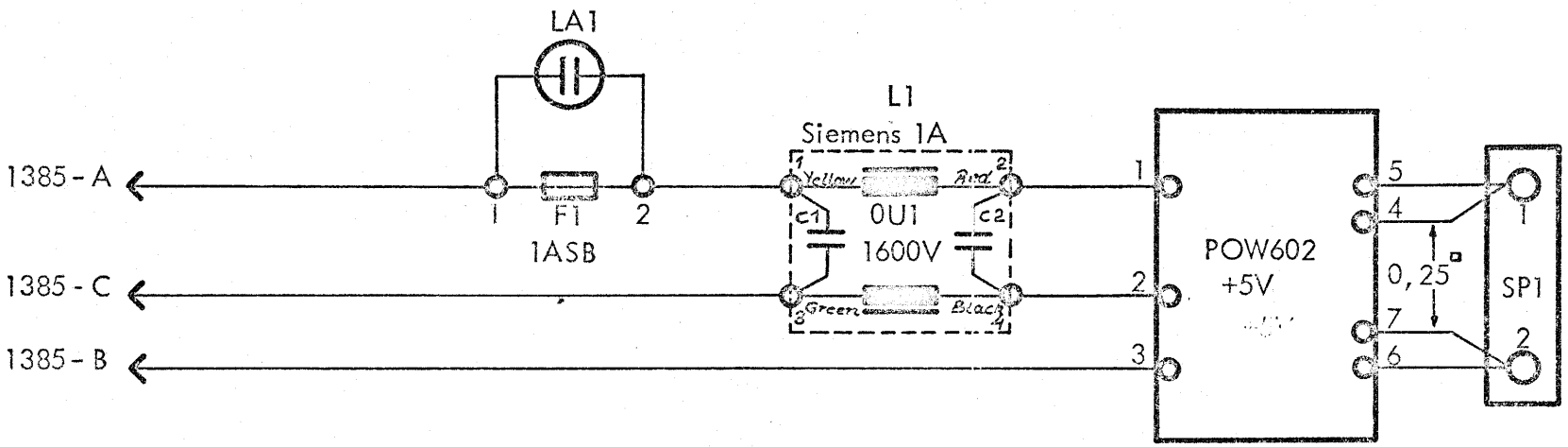
I-SEKTOR

Unit POW 602	Designed 1-9-66 JAK	POW 602	Drawing No V 2902
REGNE CENTRALEN	Approved		Drawn by AL 23-2-67
	Checked 1/3-67 JAK	5V, 9A	Checked
	Last Revision 250969 HC		Sheets · Sheet

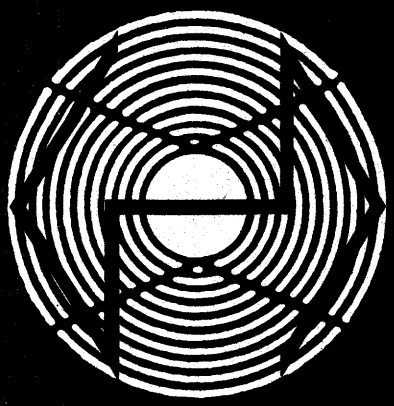
080970JAK

V21555

POW417 Power Supply
Circuit Diagram



Ikke angivne tværsnit 1mm^2
Trådtype: Soflex type TK varmebestandig.



RCSL No:

Edition:

Author:

Title:

Keywords:

Abstract:

MAIN CHARACTERISTICS

The AIC401 Analog Input Controller is connected to the low-speed data channel by means of a buffer register.

It selects the requested analog input channel within max. 1024 channels by means of an analog multiplexer, and converts the analog data to digital form by means of a 12-bit A/D-converter. Additionally it selects the requested analog input range, within max. 4 fixed ranges, simultaneously with the channel selection.

AIC401 will always be under remote control.

COMMANDS:

For the AIC401-device the control command and the sense command are available. The value of the modifier-field, bit 18:21 in the effective address of the i/o-instruction is irrelevant as it has no influence on the operation of the device.

1. CONTROL COMMAND:

A control command initiates an analog input operation during which the device is not ready. During the execution of the control command the contents of the working register is transferred to the device buffer register and the value is interpreted as follows:

Bit (0:11): Irrelevant

Bit (12,13): Analog range field where
Bit (12,13) = 00 selects range No. 0 (lowest range)
Bit (12,13) = 01 selects range No. 1
Bit (12,13) = 10 selects range No. 2
Bit (12,13) = 11 selects range No. 3 (highest range)

Bit (14:23): Analog input channel address (integers 0-1023)

The range and channel selection takes place immediately after the transfer of control information, and [130 + 5 : analog range (volts)] microseconds later the analog input operation is finished. This is indicated by the change of the device ready signal from 0 to 1.

2. SENSE COMMAND, STATUS, INTERRUPT:

When an analog input operation is not in progress, a status- and data word may be transferred from the buffer register to a working register by means of a sense command. The status- and data word is undefined after a power turn-on until the first accepted control command.

The contents of the buffer register has the following meaning:

Bit (0):	Not used (=0)
Bit (1):	Parity error
Bit (2):	Timer
Bit (3:11):	Not used (=0)
Bit (12:23):	Converted analog value (A/D value)

Converted analog value is given as a signed integer where the numerical value 2048 corresponds to a full scale analog input signal.

Parity error = 1 if an overload condition has been present during the preceding analog input operation.

When an overload condition occurs, it may not be possible to achieve valid A/D values within the following 50 milliseconds. Due to this a 50-millisecond timer in the device is started as soon as an overload is detected. This time interval is terminated by an interrupt signal, indicating that the device is available for valid analog input operations.

Timer = 1 reestablish program control of the AIC401 if the last initiated analog input operation is not terminated within 2 milliseconds. The measured A/D value is undefined.

The status bit(1:2) are cleared by an accepted control command.

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Timer = 1 reestablish program control of the AIC401 if the last initiated analog input operation is not terminated within 2 milliseconds. The measured A/D value is undefined.

The status bit(1:2) are cleared by an accepted control command.

ANALOG INPUT CONVERTER AND CONTROLLER, AIC401

Analog Input Converter and Controller, AIC401, form the connection between the Low-Speed Data Channel of RC 4000 and the Analog Input Units, MAD401, AMP401, and MPA401. In order to do this the following functions are performed:

- Receiving, transmitting and buffering of data from/to the Low-Speed Data Channel of RC 4000.
- Selection of required input channel and measuring range in suitable time intervals, all according to received Control Command.
- Analog-to-digital Conversion.
- Generation of 'ready' and 'interrupt' signals.
- Generation of status information.

Specifications:

AIC401:

Max. Number of Analog Input Channels:	1024
Max. Number of Measuring Ranges Controlled by AIC401:	4
A/D Converter:	Raytheon, model MADC 1204-16
Connection to RC 4000:	via Low-Speed Data Channel (I/O instruction with predetermined device address)
I/O Commands:	Control: Range and Channel address Sense: Status and converted analog signal

Format of Control Information (Control Command):	1 byte transferred from selected W-register, bit 12:23. Value given by: ax 1024 + b, where a = range No. (0 thru 3) b = channel address (0 thru 1023)
Format of Status Information (Sense Command):	1 word transferred to selected W-register, bit 0:23. Bit 0 = 0 Bit 1 = Parity Error (amplifier overload) Bit 2:11 = 0 Bit 12:23 = Converted analog value.
Timeinterval from Control Command to End of A/D Conversion:	[130 + 5: analog range (volts)] microseconds.
Connection to Sub-Modules:	max. 16 amplifiers AMP401 or equivalent analog signal sources, + max. 16 multiplexer address decoders, MAD401, + max. 64 analog multiplexer modules, MPA401.
Control Signals to Sub-Modules:	13 bits busline system: 10 bits binary multiplexer channel address 2 bits binary range address 1 bit multiplexer enable
Dimensions:	Height: 127 mm Width: 525 mm Depth: 210 mm
Supply Voltages:	+ 5 V ±5 per cent, 3500 mA - 6 V ±5 per cent, 110 mA +12 V ±5 per cent, 140 mA
Ambient Air:	Temperature: 0 to 45 degrees C Relative Humidity: 30 to 70 per cent
Weight:	6.0 kg

RCSL: 51-VB474
Author: V. Toft Pedersen
Edited: June 1969

RC 4000 PERIPHERAL DEVICES

AIC401, ANALOG INPUT CONTROLLER

PRELIMINARY SPECIFICATIONS

Abstract

This report describes the logical structure of the AIC401, ANALOG INPUT CONTROLLER when used as ANALOG INPUT UNIT in connection with the RC 4000 computer.

A/S REGNECENTRALEN
Falkoneralle 1
2000 Copenhagen F

MAIN CHARACTERISTICS

The AIC401 Analog Input Controller is connected to the low-speed data channel by means of a buffer register.

It selects the requested analog input channel within max. 1024 channels by means of an analog multiplexer, and converts the analog data to digital form by means of a 12-bit A/D-converter. Additionally it selects the requested analog input range, within max. 4 fixed ranges, simultaneously with the channel selection.

AIC401 will always be under remote control.

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For the AIC401-device the control command and the sense command are available. The value of the modifier-field, bit 18:21 in the effective address of the i/o-instruction is irrelevant as it has no influence on the operation of the device.

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Bit (14:23): Analog input channel address (integers 0-1023)

The range and channel selection takes place immediately after the transfer of control information, and [130 + 5 : analog range (volts)] microseconds later the analog input operation is finished. This is indicated by the change of the device ready signal from 0 to 1.

2. SENSE COMMAND, STATUS, INTERRUPT:

When an analog input operation is not in progress, a status- and data word may be transferred from the buffer register to a working register by means of a sense command.

The contents of the buffer register has the following meaning:

Bit (0): Not used (= 0)

Bit (1): Parity error

Bit (2:11): Not used (= 0)

Bit (12:23): Converted analog value (A/D value)

Converted analog value is given as a signed integer where the numerical value 2048 corresponds to a full scale analog input signal.

Parity error = 1 if an overload condition has been present during the preceding analog input operation.

When an overload condition occurs, it may not be possible to achieve valid A/D values within the following 50 milliseconds. Due to this a 50-millisecond timer in the device is started as soon as an overload is detected. This time interval is terminated by an interrupt signal, indicating that the device is available for valid analog input operations.

RCSL: 51-VB881
Author: V. Toft Pedersen
Edited: May 1970

OVERALL SPECIFICATIONS FOR

MEDIUM-SPEED, DIFFERENTIAL ANALOG INPUT UNIT

(Preliminary)

A/S REGNECENTRALEN
Falkoneralle 1
DK 2000 Copenhagen F

CONTENTS

pp.: 1:5

1. GENERAL

The ANALOG INPUT UNIT accomplishes the connection between the RC 4000 DATA PROCESSING EQUIPMENT and the process parameters represented by analog voltages from different kinds of transducers.
It includes the following types of equipment, the scope of which is defined in the relevant configuration-description:

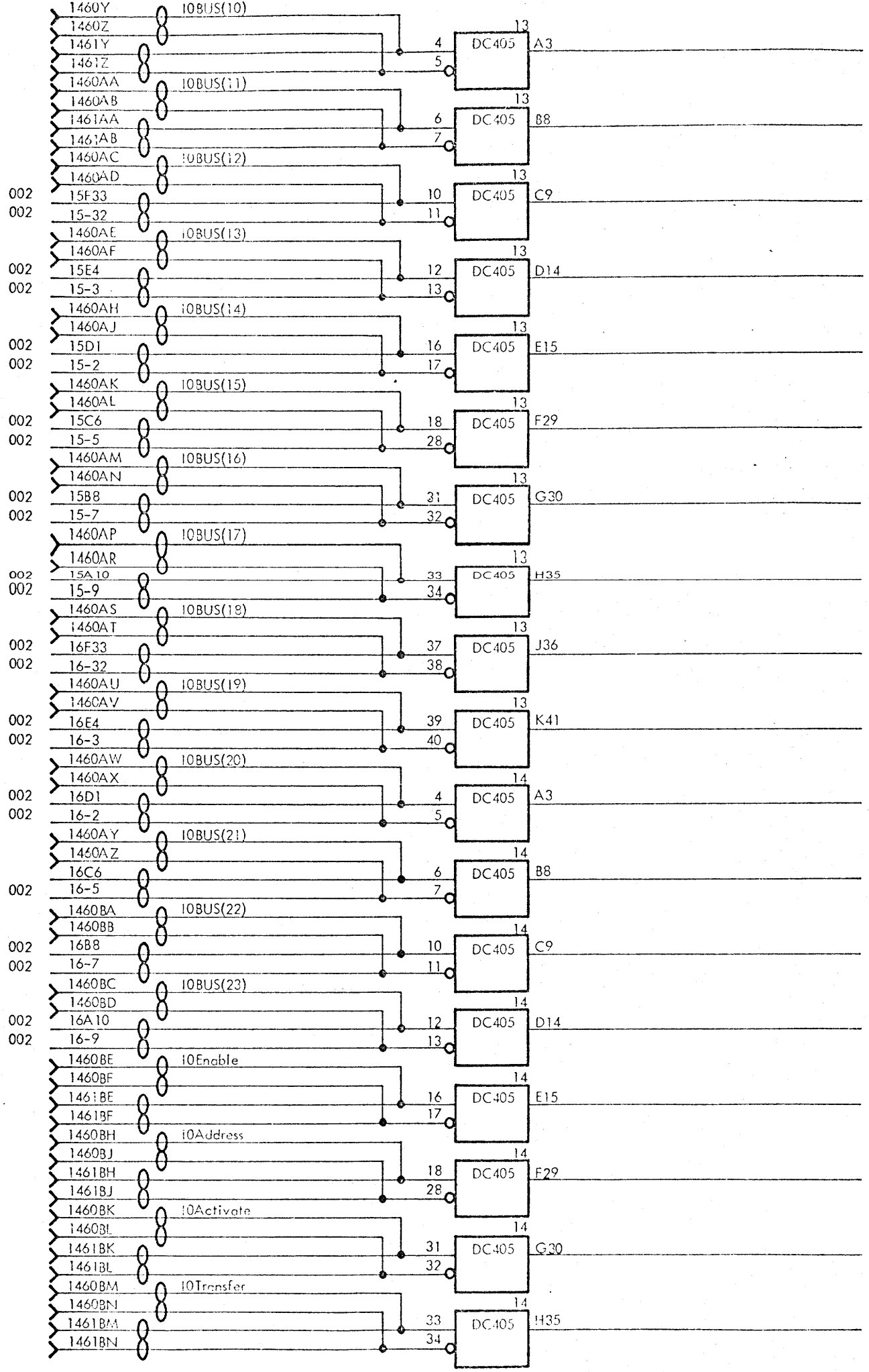
- Analog Input Controller and A/D-Converter, AIC 401
- Multiplexer Address Decoder, MAD 401
- Multigain Amplifier, AMP 402
- Analog Multiplexer, MPA 401

2. OVERALL SPECIFICATIONS FOR ANALOG INPUT UNIT

Max. Number of Analog Input Channels within one Analog Input Unit:	1024	
Type of Input Channels:	Voltage, differential	
Input Impedance:	Differential mode:	min. 10,000 Mohms
	Common mode:	min. 10,000 Mohms
Input Current:	Differential mode:	max. 0.5 nA
	Common mode:	max. 1.0 nA
Common Mode Rejection Ratio at 50 cps:	[60 dB + 20 log (10/analog range (volts))] or 110 dB, whichever is less	

Normal Mode Noise Rejection:	One low-pass filter per input channel required for input ranges of ±1 volt or lower. For detailed specification, see separate specification sheet.
Max. Input Voltage with specified Common Mode Rejection (ref. to system ground):	±13.5 volts, peak (either side)
Overvoltage Protection for max. 220 V rms.:	2 fuses and 4 diodes per channel
Max. Number of Analog Input Ranges:	4 within ±10 volts full scale thru ±10 mV full scale (must be selected by the customer in due time)
Range Identification:	Range address No. 0 thru 3, where 0 identifies lowest range and 3 highest range.
Connection to RC 4000, CPU:	via low-speed Data Channel (I/O- instruction with predetermined device address)
I/O Commands used for Data-Transfer:	Control: Range and Channel address Sense: Status and converted analog signal
Format of Control Information: (Control command)	1 byte transferred from selected W-register, bit 12:23. Integer given by: $a \times 1024 + b$, where a = range No. (0 thru 3) b = channel address (0 thru 1023)

Format of Status/Data Information: (Sense command)	1 word transferred to selected W-register bit 0:23 : Bit 0 = 0 Bit 1 = Parity Error (amplifier overload) Bit 2:11 = 0 Bit 12:23 = Converted analog value
Time-Interval from Control Command to end of A/D Conversion:	[130 + 5/analog range (volts)] microseconds for as well unipolar as bipolar signals.
A/D Converter Type:	Successive approximation
Format of Converted Analog Value:	12-bit binary, negative values given as 2-complements
Scale Factor:	±2048 corresponds to ± full scale signals of selected analog input range.
Overall Accuracy at a 99.9 per cent Confidence Level, and at 25 deg. C:	±0.15 per cent of full scale or ±20 microvolts ref. to input, whichever is greater ±1 least significant bit
Max. Temperature Coefficient:	(±1.5 microvolt ref. to input ±30 ppm) per deg. C.
Supply Voltages:	+5 V DC ±5 per cent +12 V DC ±5 per cent -6 V DC ±5 per cent +24 V DC ±2 per cent -24 V DC ±2 per cent
Ambient Air:	Temperature: 0 to 45 deg. C Relative Humidity: 30 to 70 per cent



130669AAJ 2010701A 031170 HC 19.1170 Rev. J.

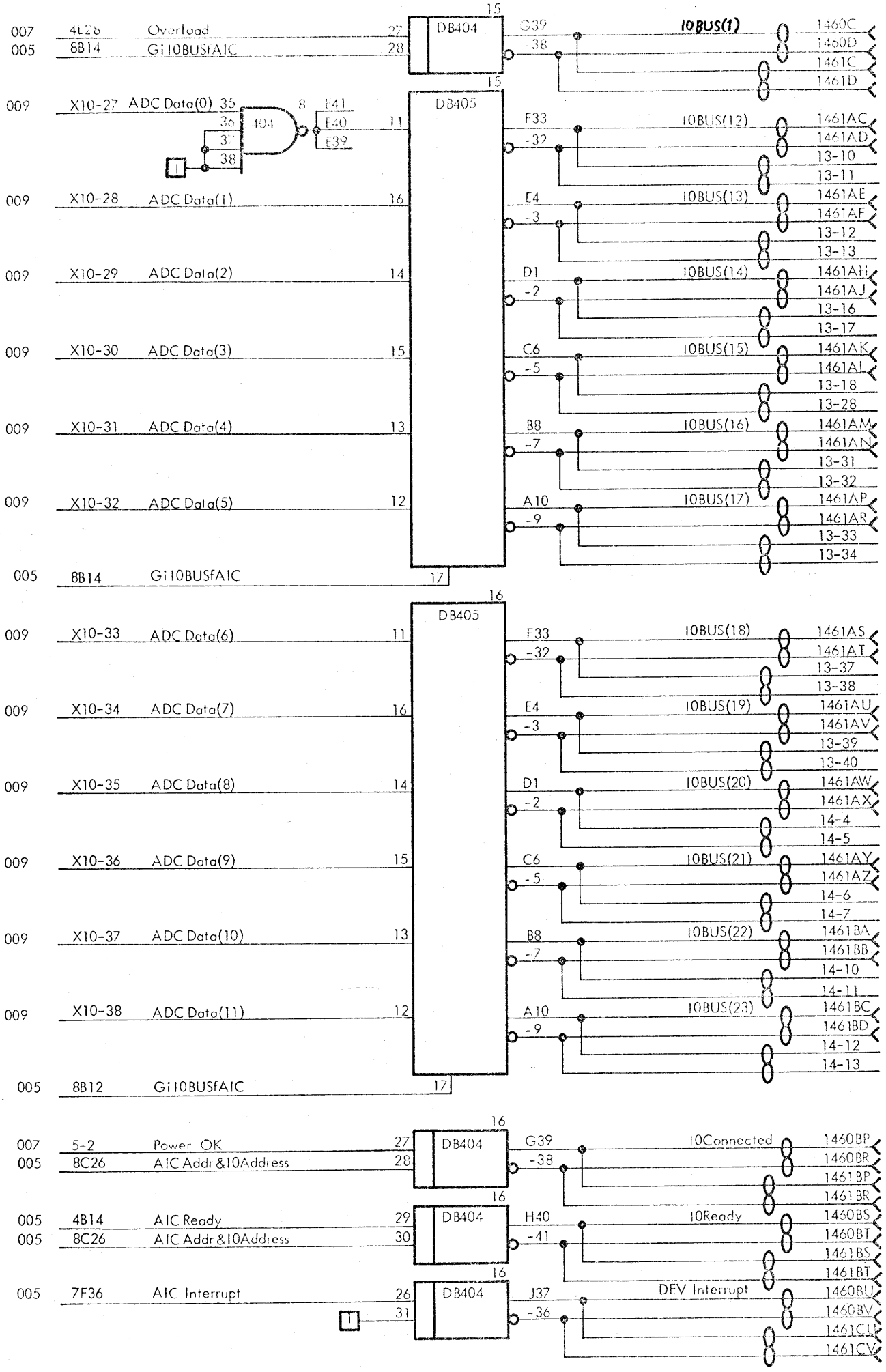
RC4000

V12093

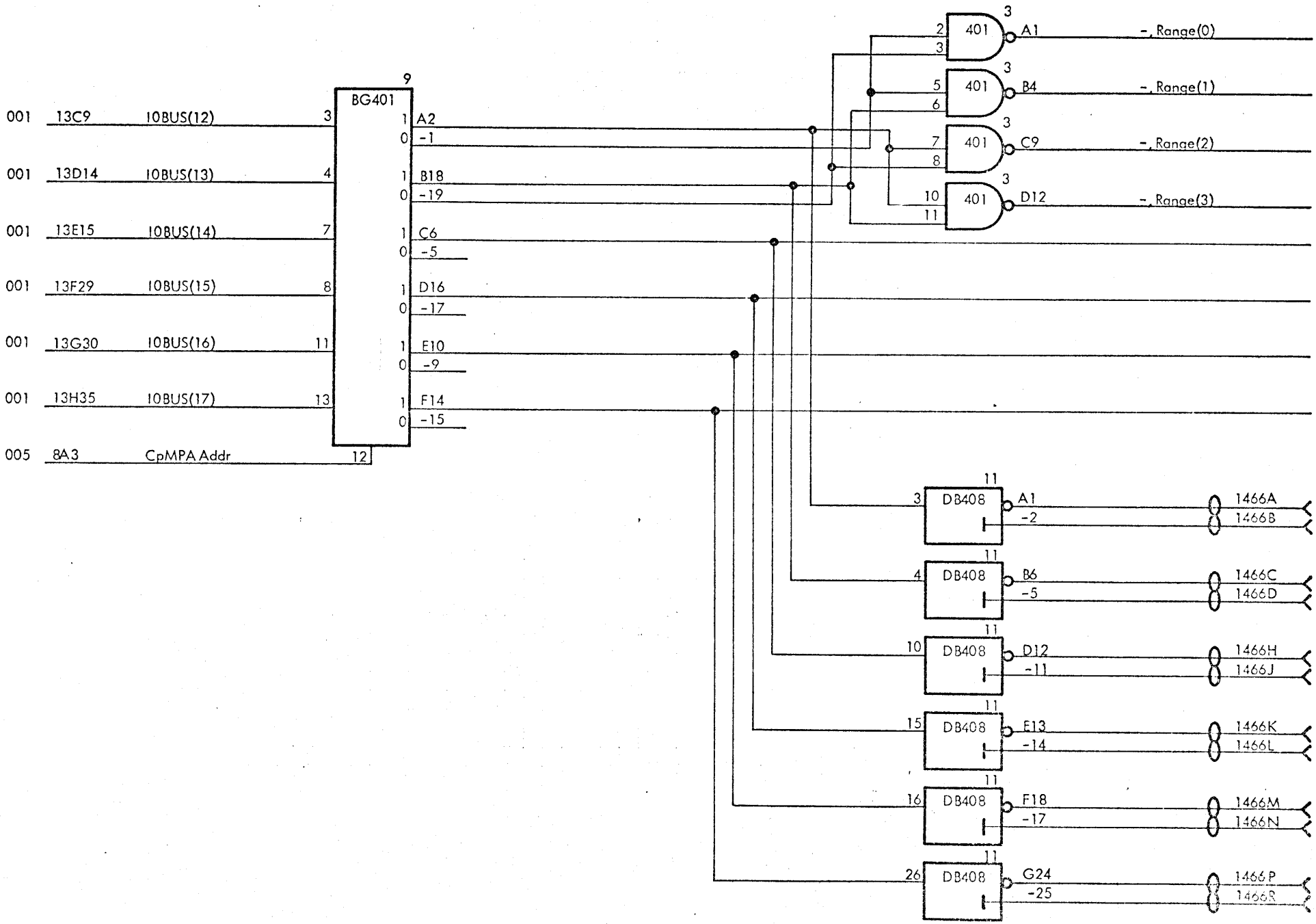
Input from Low Speed Bus, AIC401

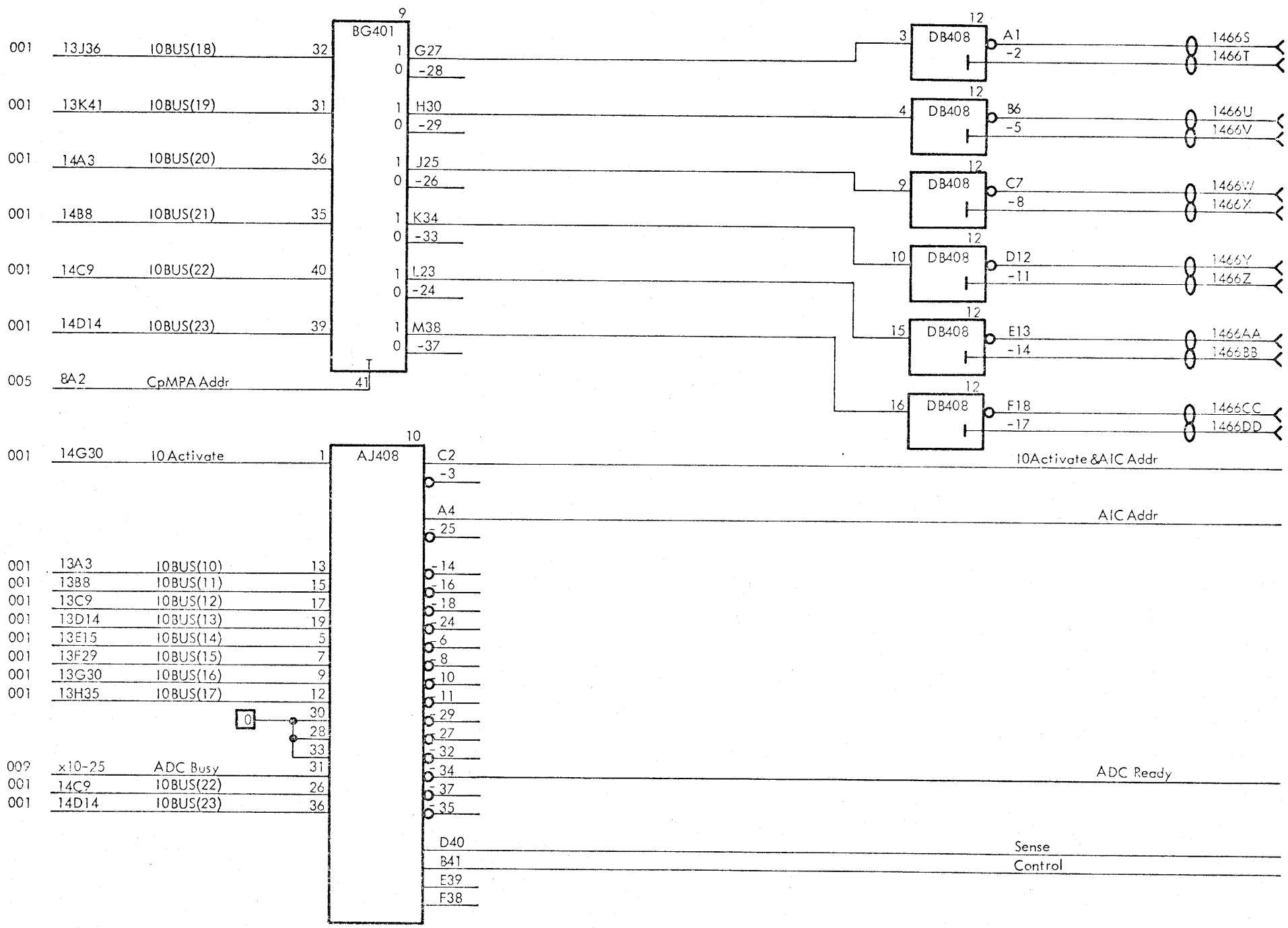
Logic Diagram

AIC001



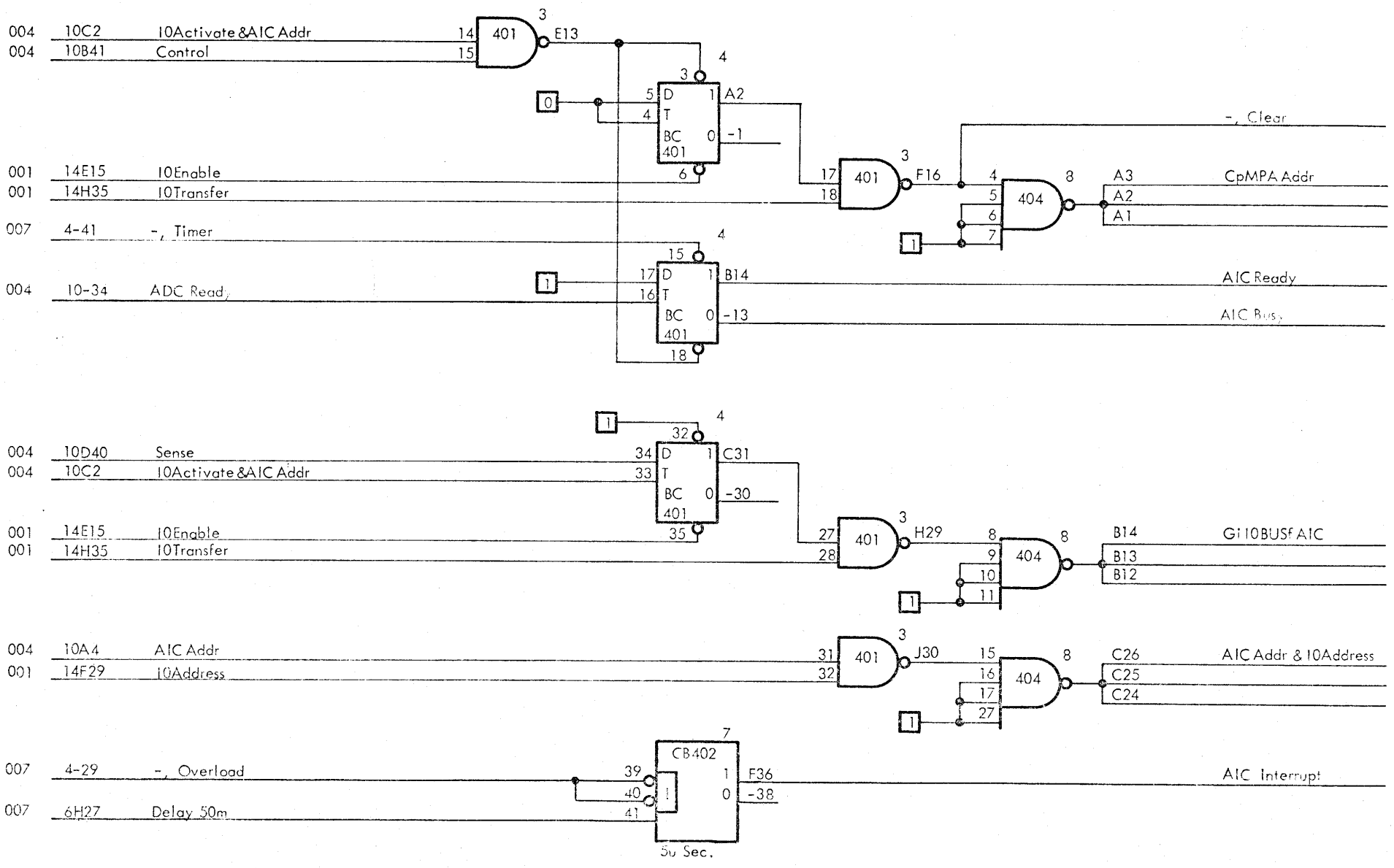
130669AAJ 2010701A 031170 HC 19112 Raf. V12094

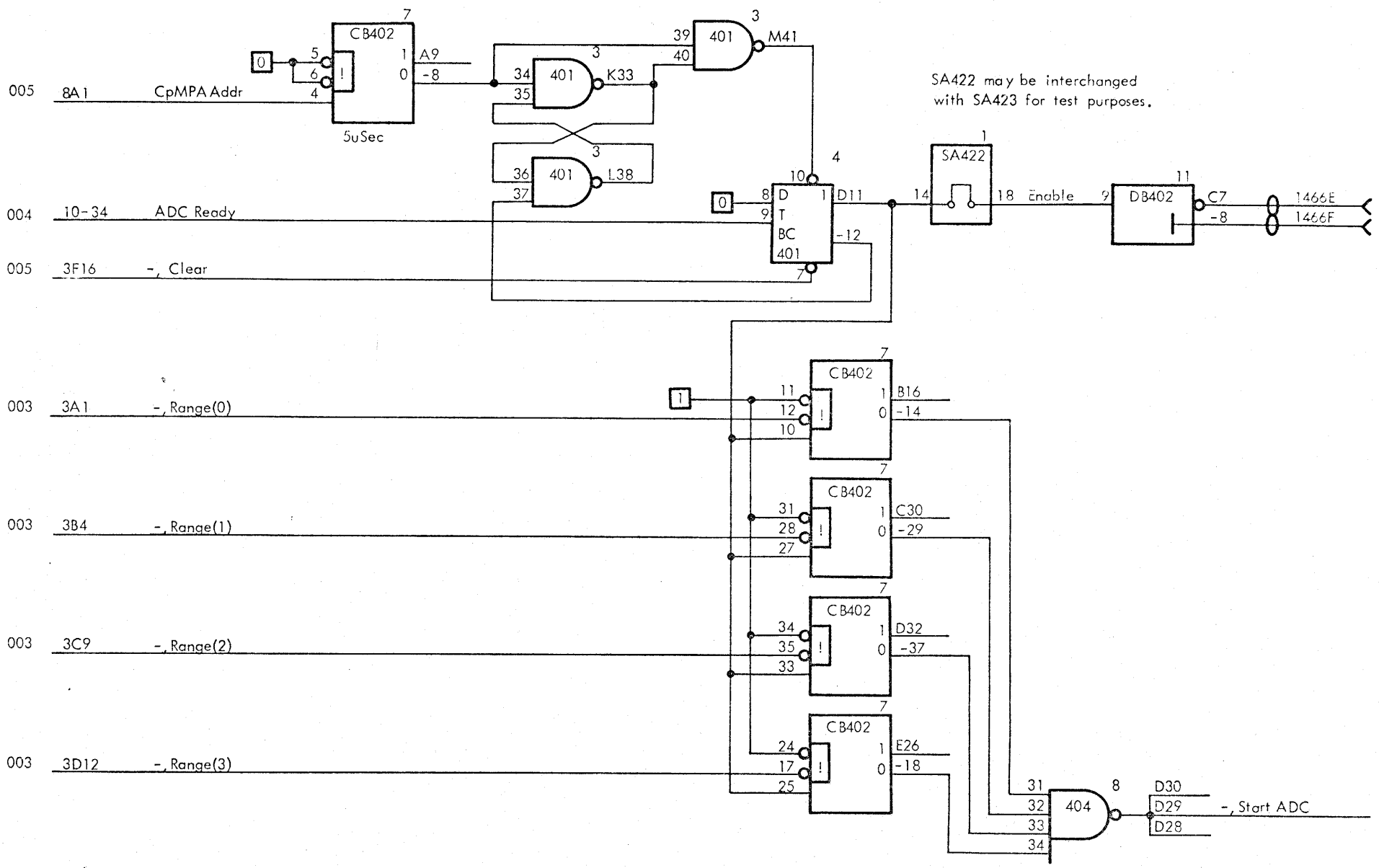

9
BG401
001 13C9 10BUS(12) 3
001 13D14 10BUS(13) 4
001 13E15 10BUS(14) 7
001 13F29 10BUS(15) 8
001 13G30 10BUS(16) 11
001 13H35 10BUS(17) 13
005 8A3 CpMPA Addr 12
1 A2
0 -1
1 B18
0 -19
1 C6
0 -5
1 D16
0 -17
1 E10
0 -9
1 F14
0 -15
3 401 A1 -, Range(0)
3 401 B4 -, Range(1)
3 401 C9 -, Range(2)
3 401 D12 -, Range(3)
11 DB408 3 A1 -2 1466A 1466B
11 DB408 4 B6 -5 1466C 1466D
11 DB408 10 D12 -11 1466H 1466J
11 DB408 15 E13 -14 1466K 1466L
11 DB408 16 F18 -17 1466M 1466N
11 DB408 26 G24 -25 1466P 1466R



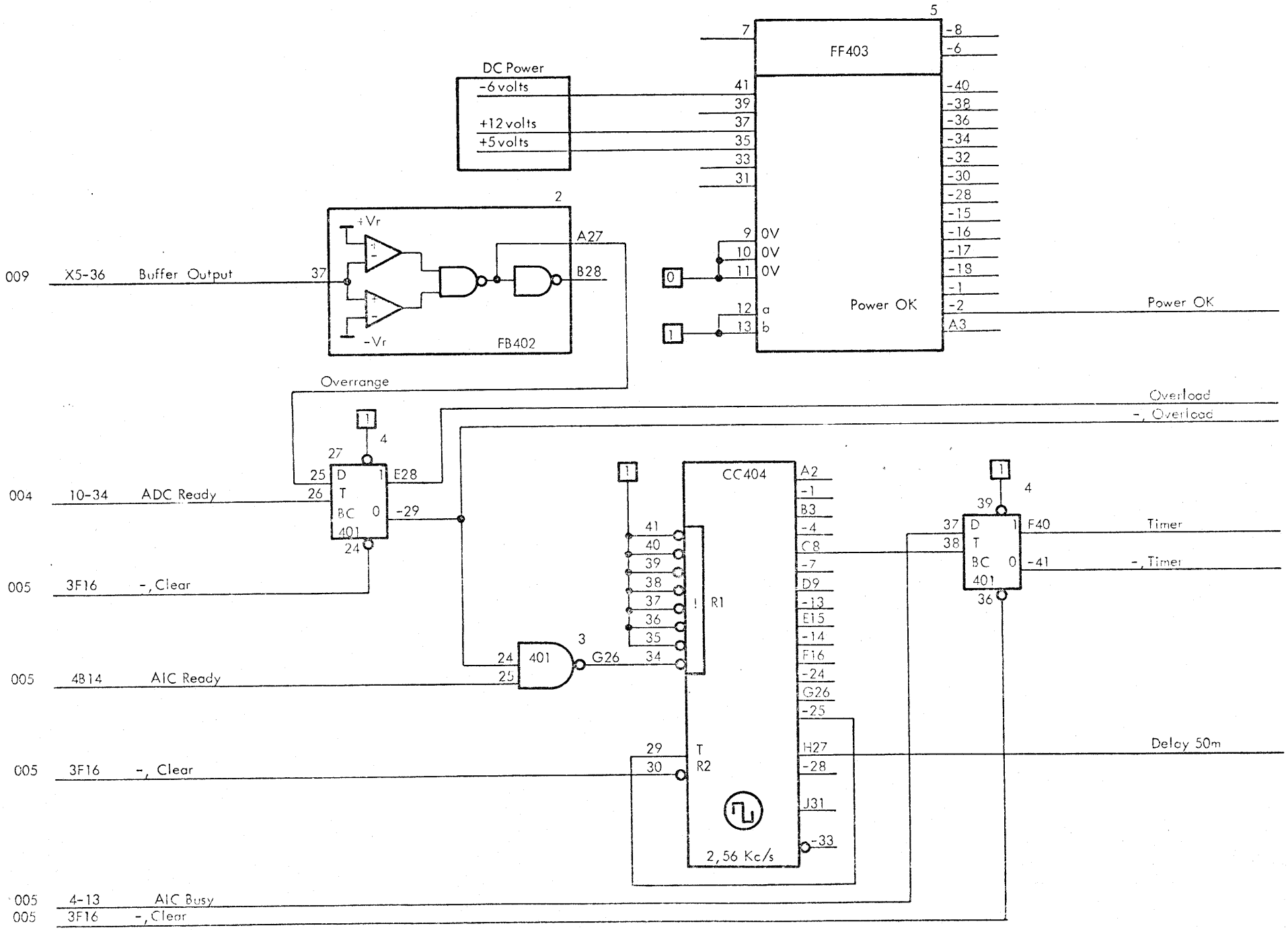
Buffer for MPA Address, Decoding of Device No., AIC401

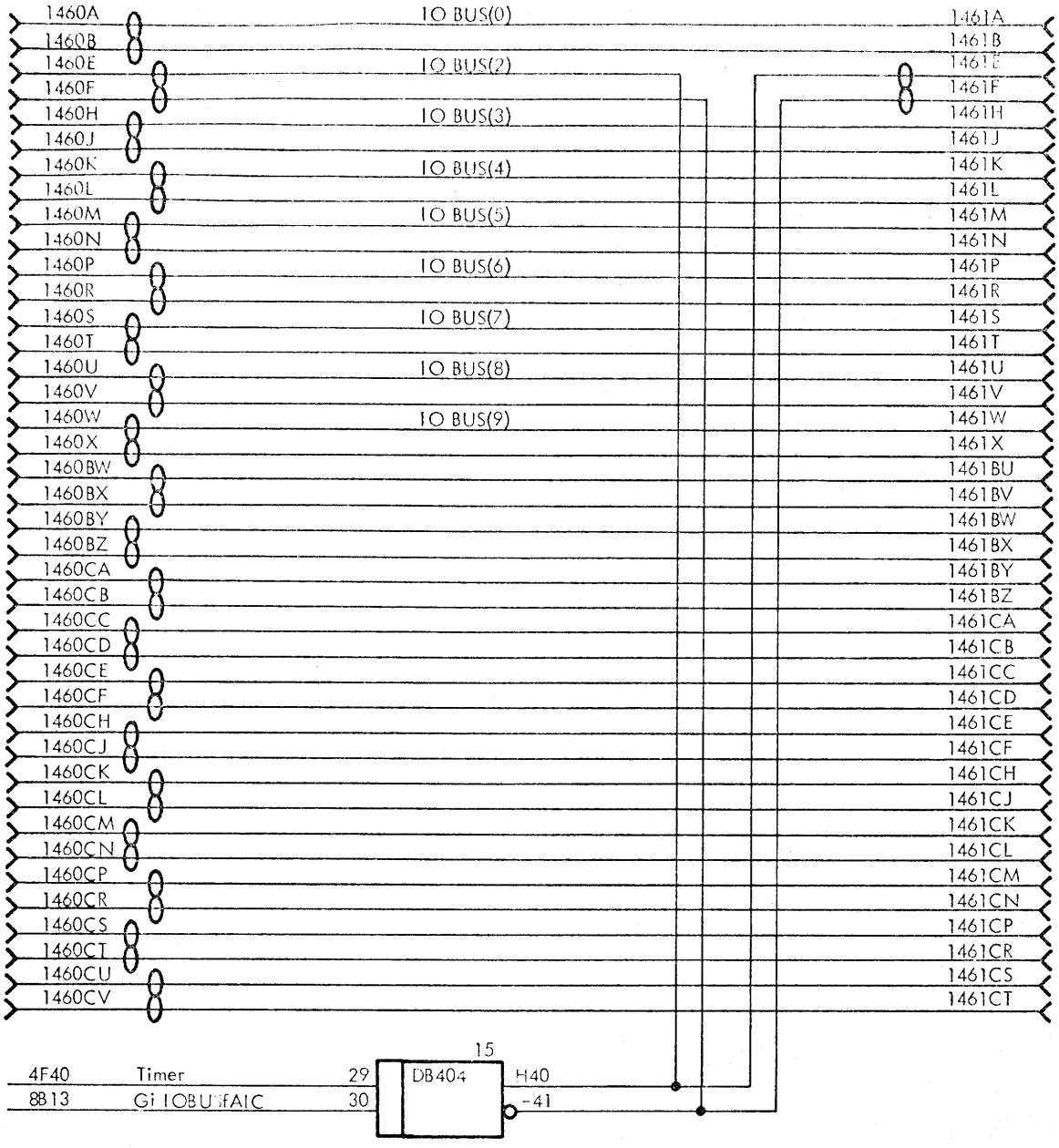
Logic Diagram


004 10C2 10Activate&AIC Addr
004 10B41 Control
001 14E15 10Enable
001 14H35 10Transfer
007 4-41 -, Timer
004 10-34 ADC Read,
004 10D40 Sense
004 10C2 10Activate&AIC Addr
001 14E15 10Enable
001 14H35 10Transfer
004 10A4 AIC Addr
001 14F29 10Address
007 4-29 -, Overload
007 6H27 Delay 50m
401
E13
A2
-1
F16
404
A3
A2
A1
-, Clear
CpMPA Addr
B14
-13
AIC Ready
AIC Busy
C31
-30
H29
B14
B13
B12
Gi10BUSf AIC
J30
C26
C25
C24
AIC Addr & 10Address
CB402
F36
-38
AIC Interrupt
5u Sec.



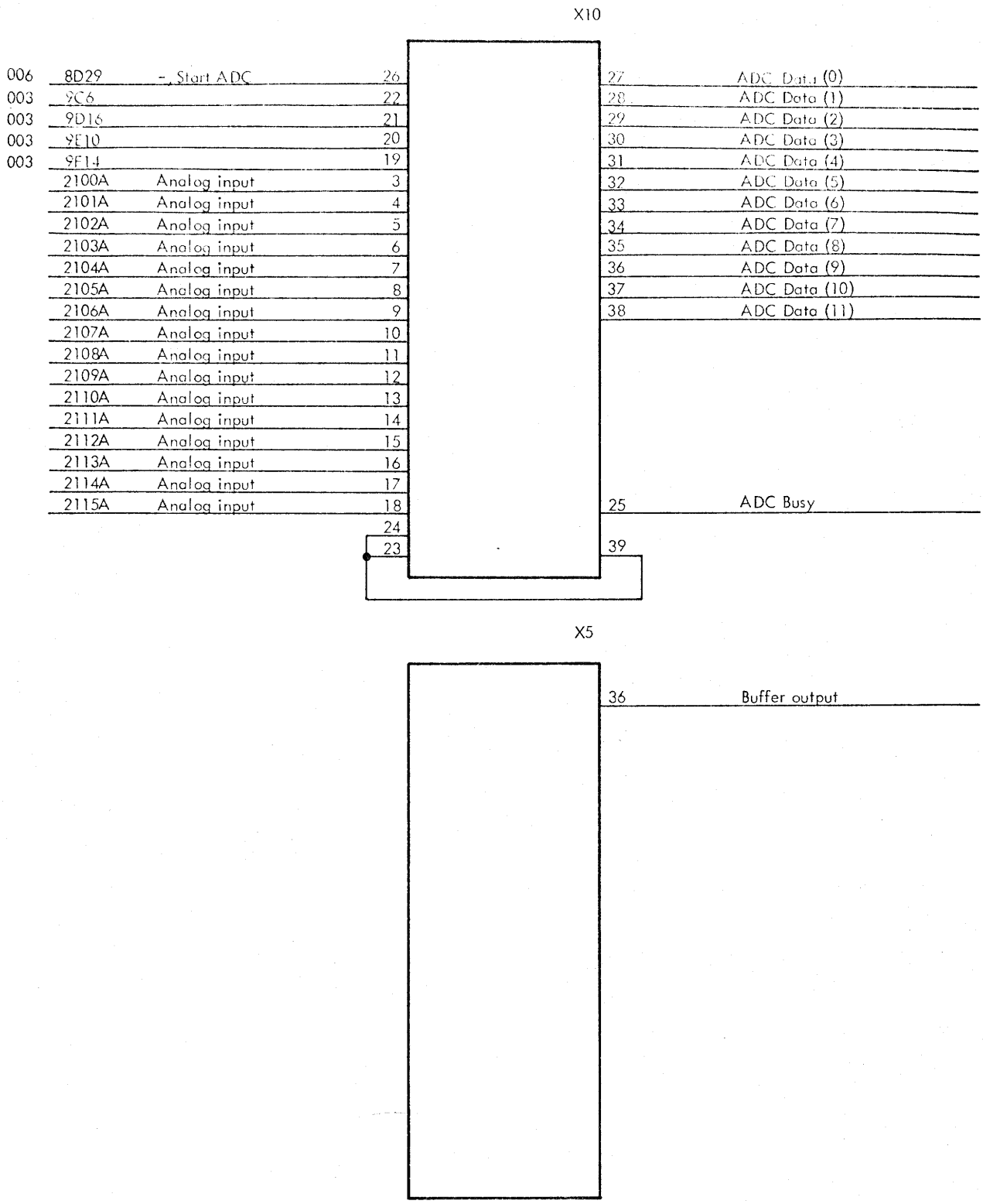
The pulse-time (T) for 7B, 7C, 7D and 7E are dependent on the installation.
T= (100 + 5/range) uSec
where range= 10/gain Volt


DC Power
-6 volts
+12 volts
+5 volts
FF403
Power OK
009 X5-36 Buffer Output
+Vr
-Vr
FB402
A27
B28
Overrange
Overload
-, Overload
004 10-34 ADC Ready
005 3F16 -, Clear
005 4B14 AIC Ready
005 3F16 -, Clear
005 4-13 AIC Busy
005 3F16 -, Clear
CC404
R1
R2
2,56 Kc/s
G26
H27
J31
E28
F40
Timer
-, Timer
Delay 50m
Power OK



AG=Analog ground pos. X5-17

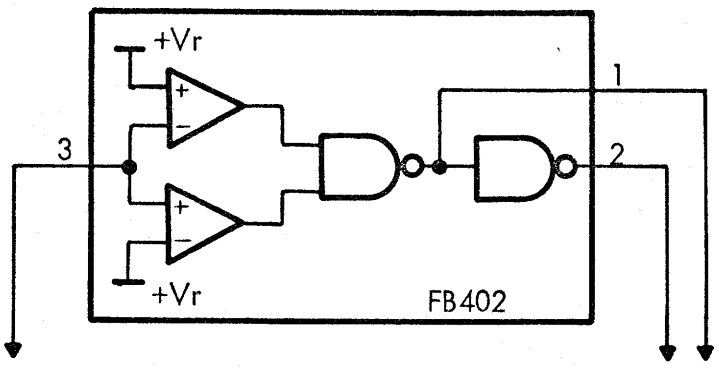
300470AAJ 2110701A 031170 HC 1411 Rev. P. V11866



X1, X2, X3, X4, X5, X6, X7, X8, X9 and X10 are the card positiones for the Raytheon analog to digital converter MADC12

201170UFL 201170HC 201170 HC 2011 Rv 4 FU. V12092

FB402



CIRCUIT DESCRIPTION

This comparator is designed to give a "zero" or a "one" if a voltage is greater or smaller than a predetermined value. The circuit can discriminate voltage from ±0,15 volt to ±20 volt. The discrimination worst case error of the comparator is 1,5 volt. This error can be reduced to 0,15V if potentiometers are placed in serie with the ref. voltages.

SPECIFICATIONS

R6//R7 = R2//R3 = Rt
R8//R9 = R4//R5 = Rv

Rt + Rv = (20-50) kΩ

$$\frac{Rt}{Rv} = \frac{Vin}{Vref}$$

$$R1 = 0.5 \times \frac{Rt}{Rv}$$

The discrimination error is:

$$Verror = Vref \frac{Rt}{Rv} = \underline{\underline{0,4}} \frac{Rt}{Rv}$$

temp range (20-50) ^{o}C.

Hysteresis much lower than the error.

$\pm$ Vref can be adjusted by potentiometers.

The error is now reduced to:

$$Verror = 0,1 \frac{Rt}{Rv}$$

it is a temperature error caused by change in temperature from 20 - 50 ^{o}C.

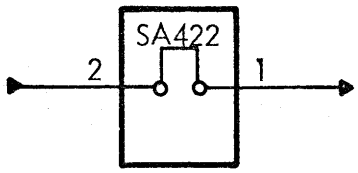
$\pm$ Vref is controlled by a double voltage regulator with low drift.

Rl , Rt and Rv should be low drift metalfilm resistors.

temp range (20-50)^{o}C.

RCSL: 31-D68
pp.: 1:1
November 1971

SA422



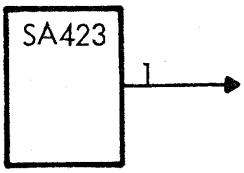
CIRCUIT DESCRIPTION

The only purpose for this card is to connect pin 14 to pin 18.

It is only used in connection with AIC401 and AIC402.

In AIC401/402 "normal" operation this card is used.
It can be replaced by a "testboard" in the test mode.

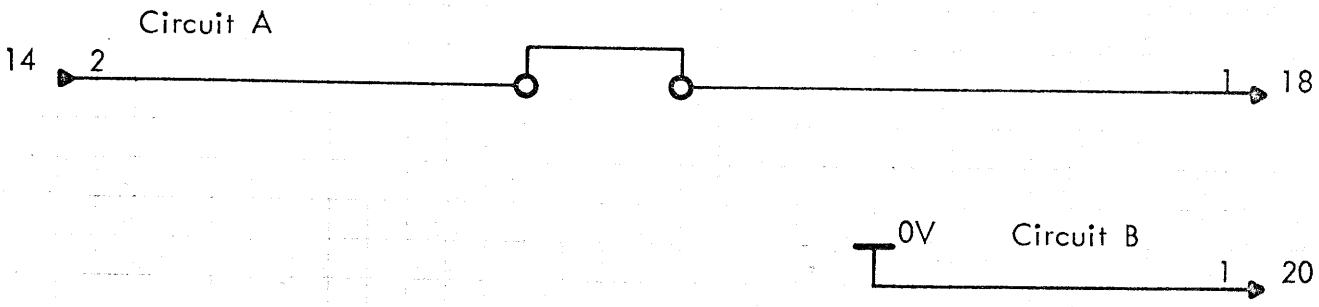
SA423



CIRCUIT DESCRIPTION

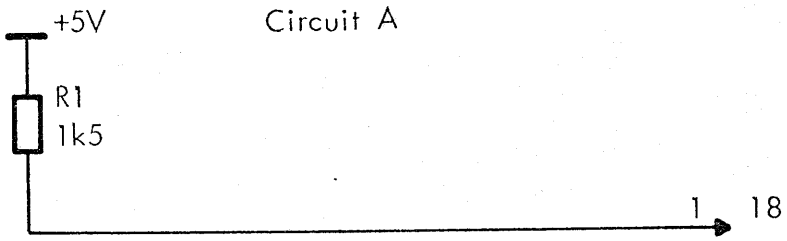
This card is a "testboard" and can only be used in connection with AIC401 and AIC402.

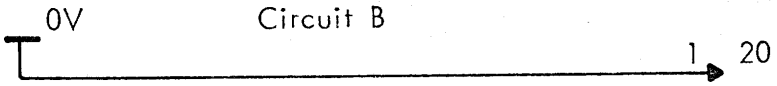
When the AIC "normal" card is replaced with the "testboard" a one generator is coupled to pin 18.



POWER REQUIREMENT		
+5V	PIN22	0 mA
0V	PIN21	
POWER DISSIPATION		0

191170UFL 15117 MOGK 18117(HOUM 18117(HOUM

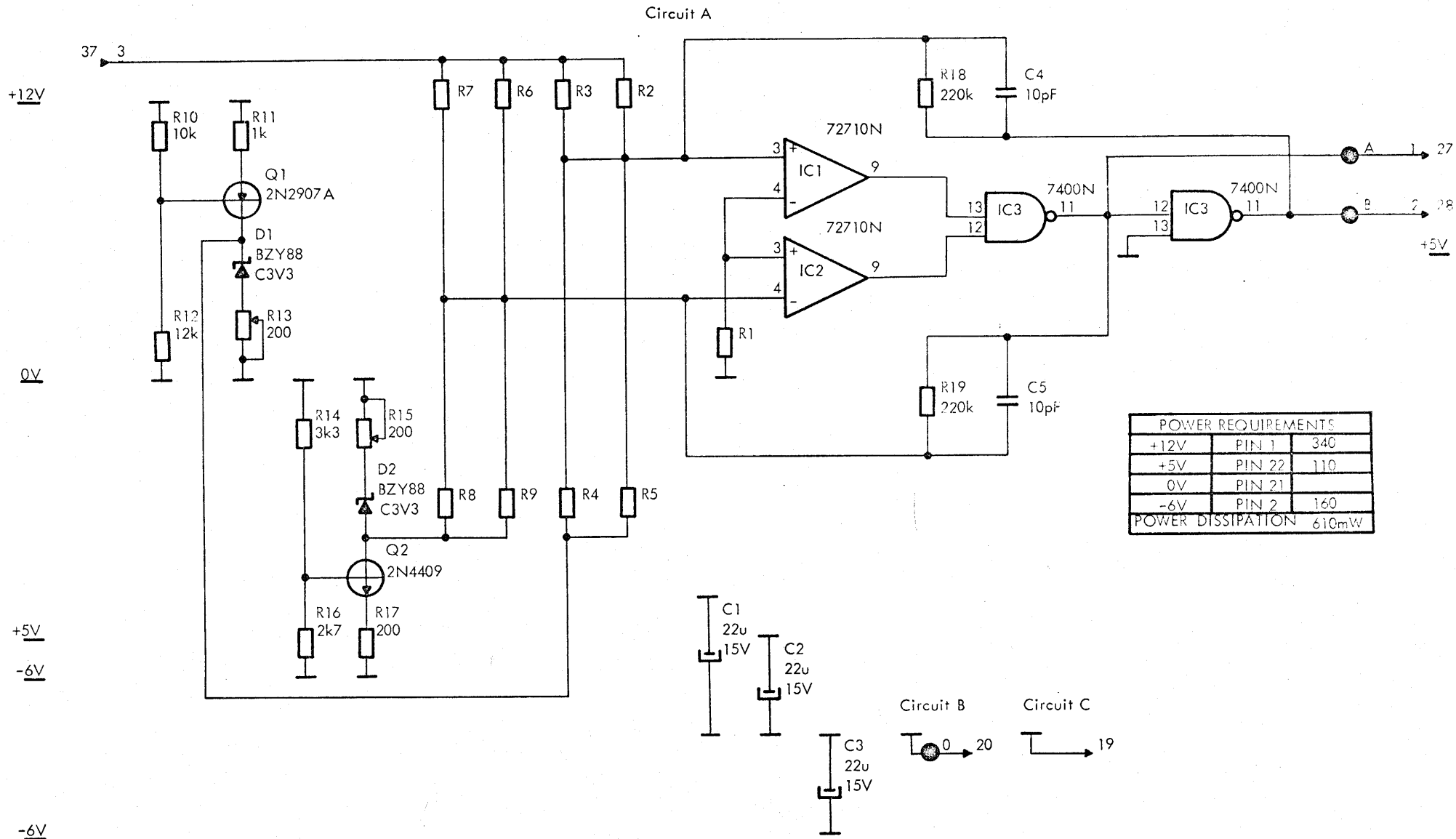




POWER REQUIREMENT		
+5V	PIN 22	4 mA
0V	PIN 21	
POWER DISSIPATION 20 mW		

V22342

PCBA Circuit Diagram



POWER REQUIREMENTS		
+12V	PIN 1	340
+5V	PIN 22	110
0V	PIN 21	
-6V	PIN 2	160
POWER DISSIPATION		610mW

MULTIPLEXER-ADDRESS DECODER, MAD401, AND CHASSIS, CHS401

Multiplexer-Address Decoder, MAD401, is a decoder module covering up to 64 analog input addresses.
It contains a fixed decoding of the 4 most significant bits and a x-y decoding of the 6 least significant bits of the 10-bit multiplexer address.
The fixed decoding defines the selection number (0 through 15) for the Multiplexer-Address Decoder and so for the relevant 64-channel group of inputs.
The x-y decoding defines the input channel to be selected within the 64-channel group.
Further MAD401 contains a 1 out of 4 decoding of 2 additional bits for control of gain-selection in Multigain Amplifier, AMP401.
MAD401 is placed in chassis CHS401 together with Multigain Amplifier, AMP401, and Analog Multiplexer, MPA401.
MAD401 modules are connected together and to the AIC401 unit as well by means of a one-way sub-busline system for which the signals are generated in the AIC-unit.

Specifications:

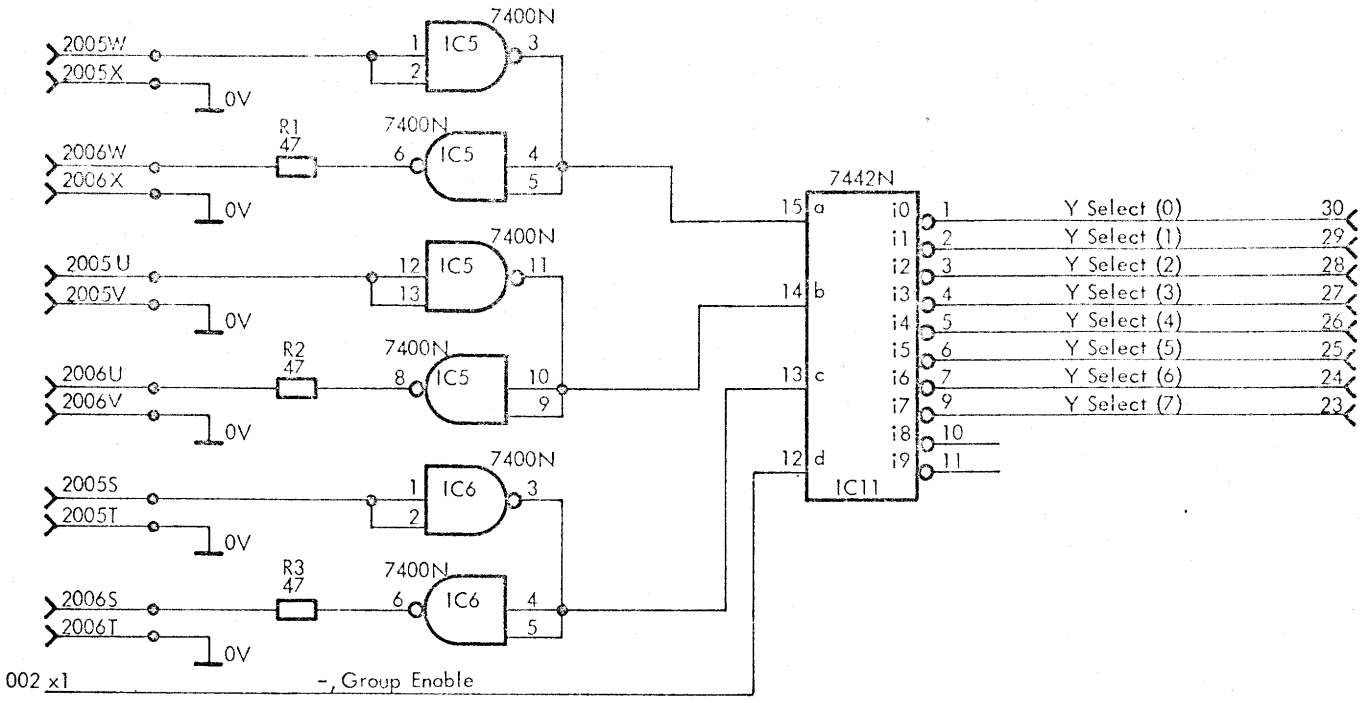
MAD401:

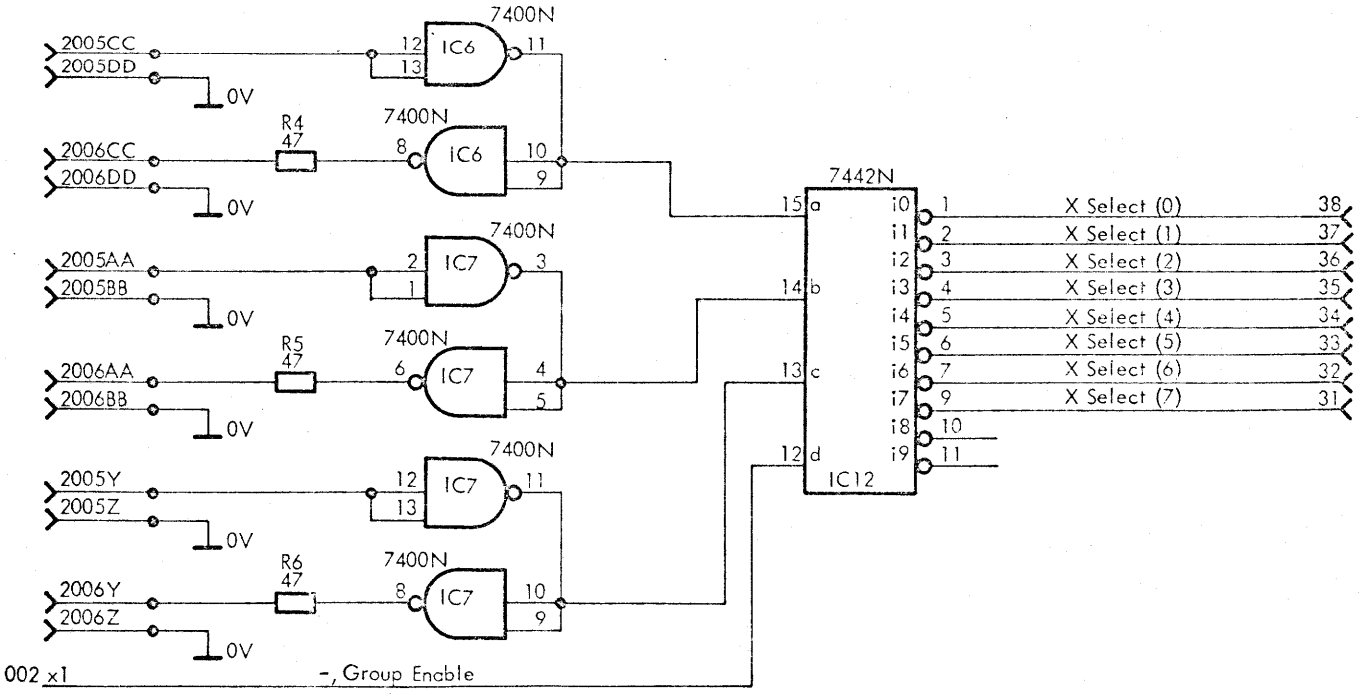
Control Buslines (from AIC):	10-bit binary multiplexer address
	2-bit binary gain address
	1-bit multiplexer 'enable'
Multiplexer Control Output:	8 y-wires (octal selection)
	8 x-wires (unit selection)
Multigain Amplifier Control Output:	4 gain selection outputs
	1 amplifier reset output

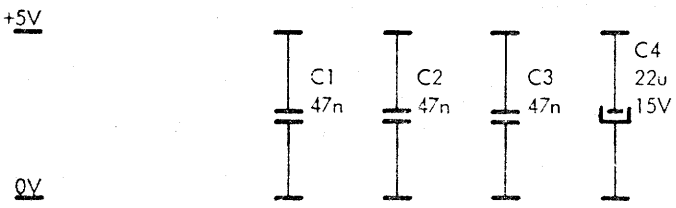
Logic Levels for Input/Output Signals:	TTL levels
Dimensions:	Height: 177 mm Width: 48 mm Depth: 450 mm
Supply Power:	+5 V ±5 per cent, 215 mA
Ambient Air:	Temperature: 0 to 45 degrees C Relative Humidity: 30 to 70 per cent
Weight:	0.5 kg

CHS401:

Max. Number of Analog Process Input Modules:	2 MAD401 + 2 AMP401 + 8 MPA401
Dimensions:	Height: 177 mm Width: 483 mm Depth: 592 mm
Weight:	12.5 kg







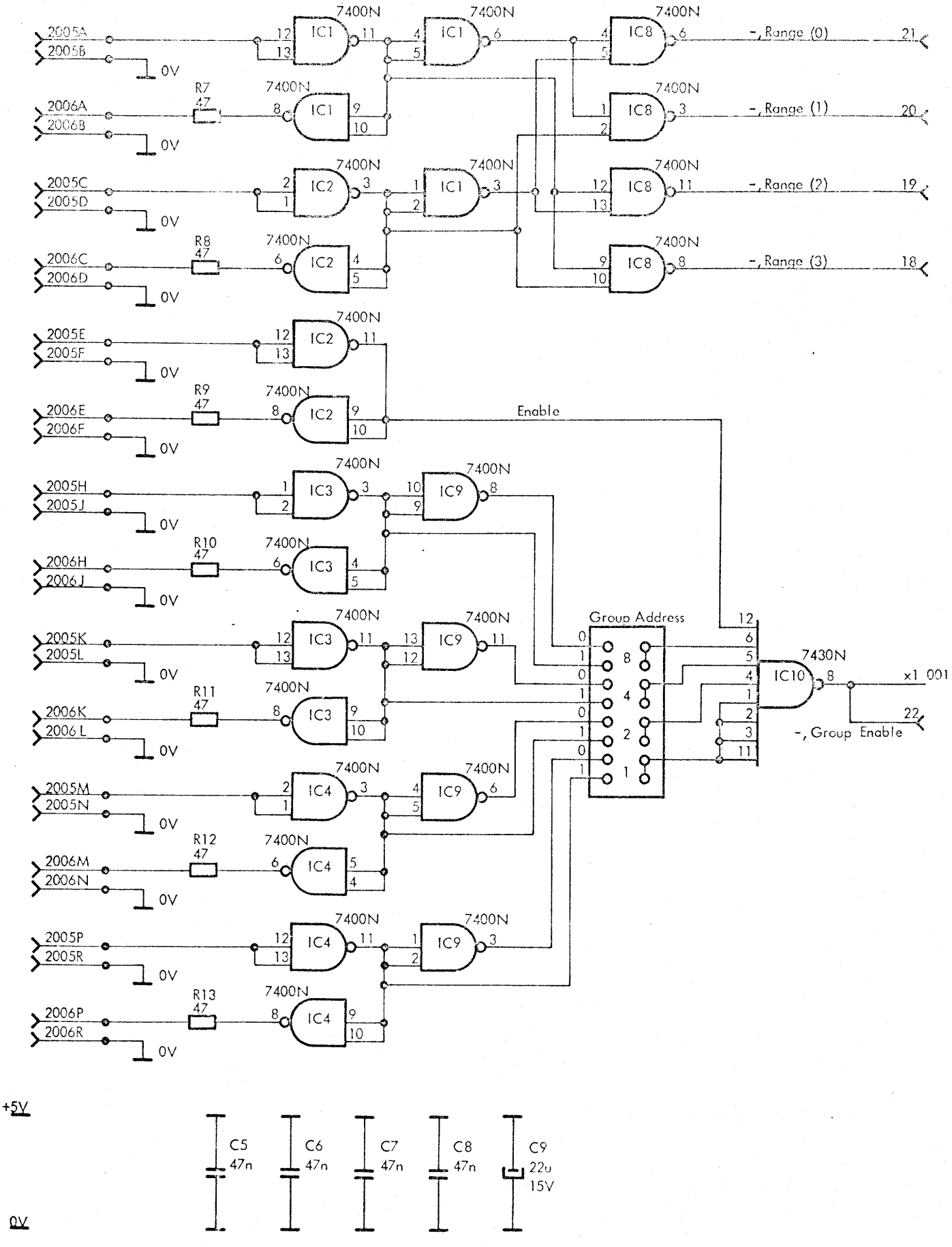
MAD401

V12106

ANALOG MULTIPLEXER ADDRESS DECODER

PCBA Circuit Diagram

MAD001



MAD401

V12107

ANALOG MULTIPLEXER ADDRESS DECODER

PCBA Circuit Diagram

MAD002

ANALOG MULTIPLEXER, MPA401

Analog Multiplexer, MPA401, is a 16-channel, differential, solid-state multiplexer module for low- and high-level analog signals. It can be placed in chassis CHS401 together with multigain-amplifier, AMP401, and Multiplexer-Address Decoder, MAD401. Up to 4 MPA401 can be used for each AMP401 and MAD401.

Application:

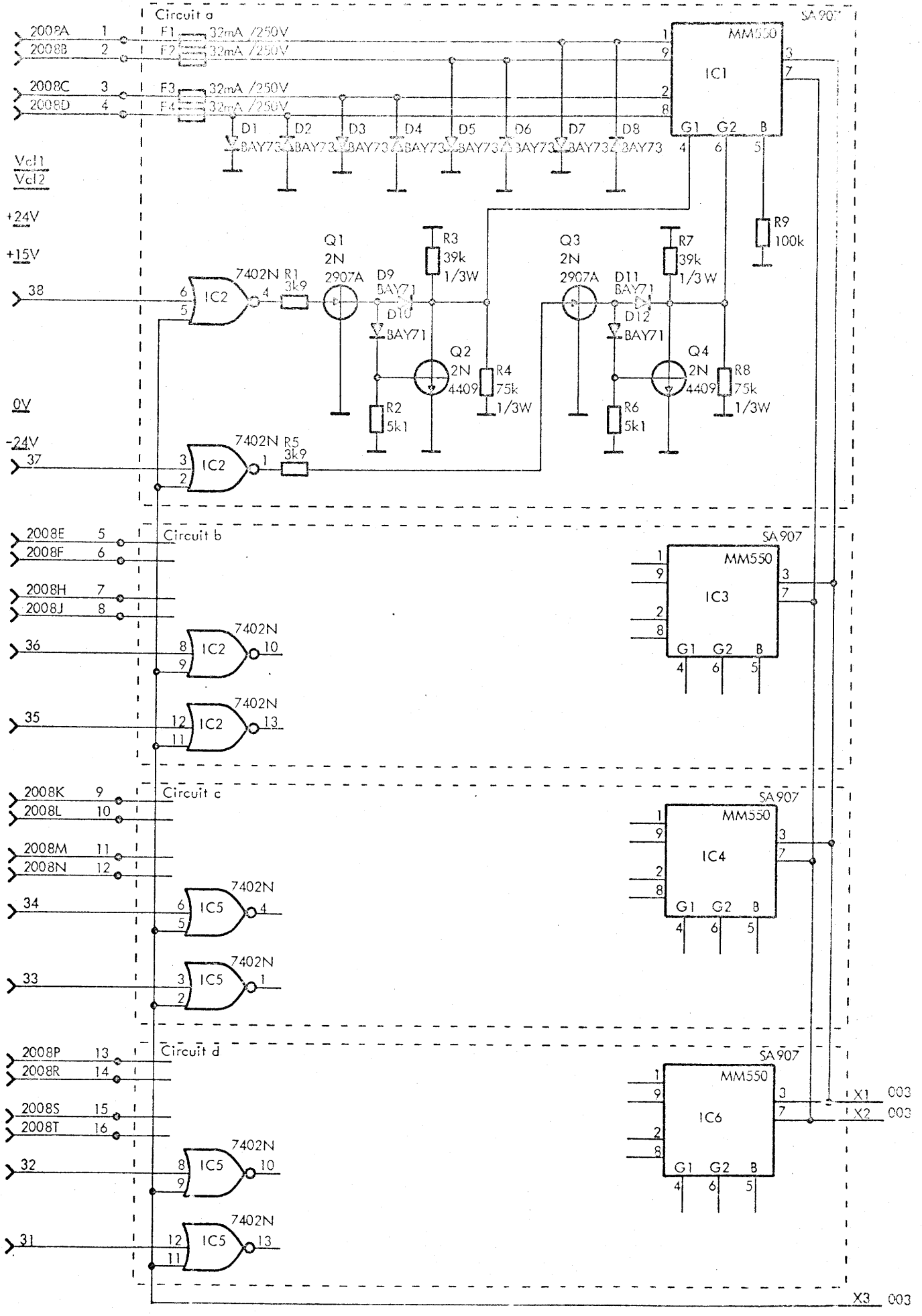
Multiplexing of high/low-level DC-signals in industrial process control.

Specifications:

MPA401:

Number of Channels:	16, differential
Max. ''On''-Resistance:	1200 ohms (each side)
Max. Input Voltage Range:	± 15 V (either side)
Max. Differential Offset Voltage:	10 micro V
Max. Leakage Current:	5 nA
Fault (Overvoltage) Protection:	2 fuses per channel
Control Inputs (Channel Selection):	8 X-inputs for unit selection (TTL) 2 Y-inputs for octal selection (TTL)

Dimensions:	Height: 177 mm Width: 24 mm Depth: 450 mm
Supply Power:	+ 24 V ± 2 per cent, 35 mA + 5 V ± 5 per cent, 65 mA - 24 V ± 2 per cent, 25 mA
Ambient Air:	Temperature: 0 to 45 degrees C Relative Humidity: 30 to 70 per cent
Weight:	0.5 kg



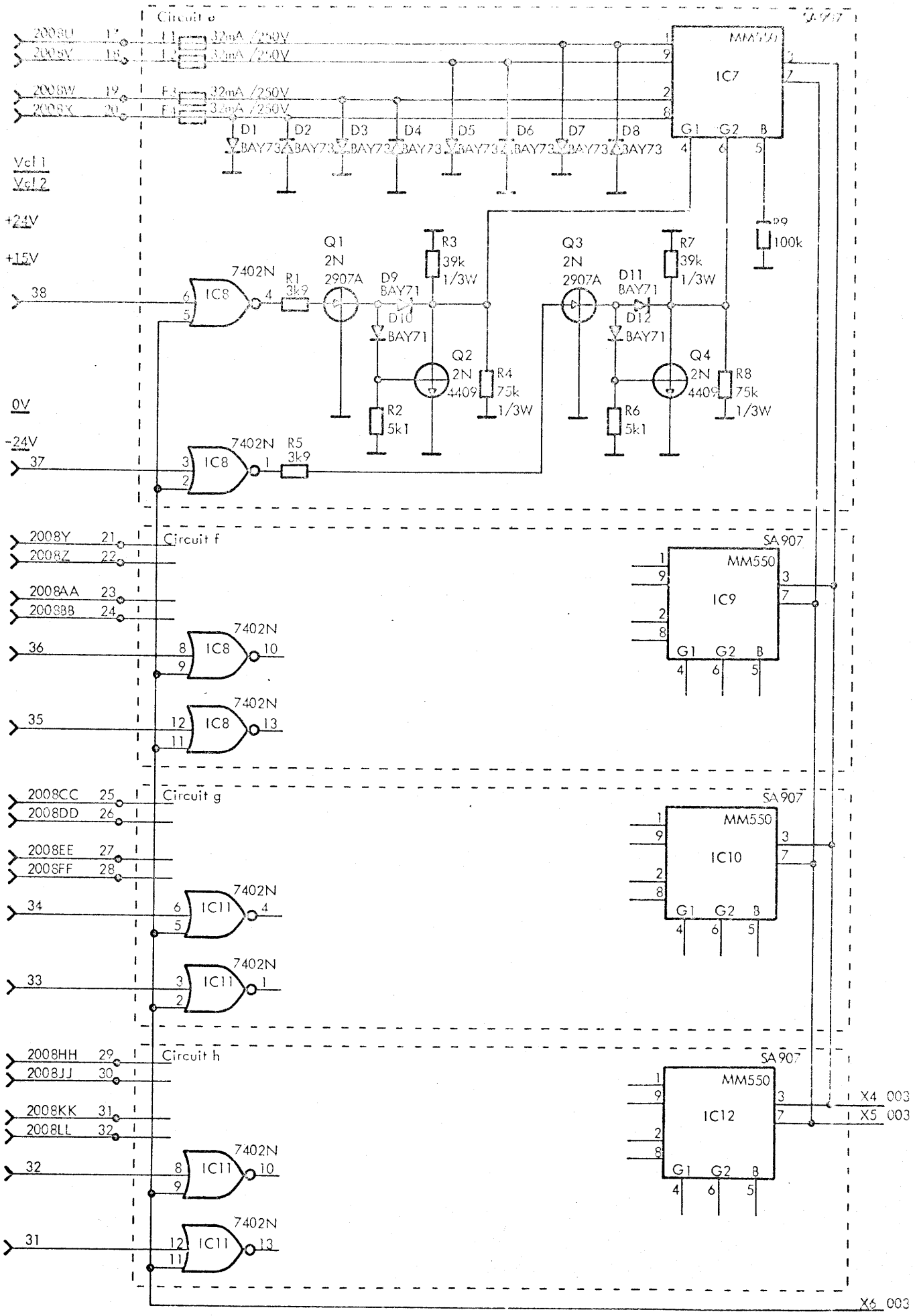
MPA401

V12073

ANALOG MULTIPLEXER

PCBA Circuit Diagram

MPA001



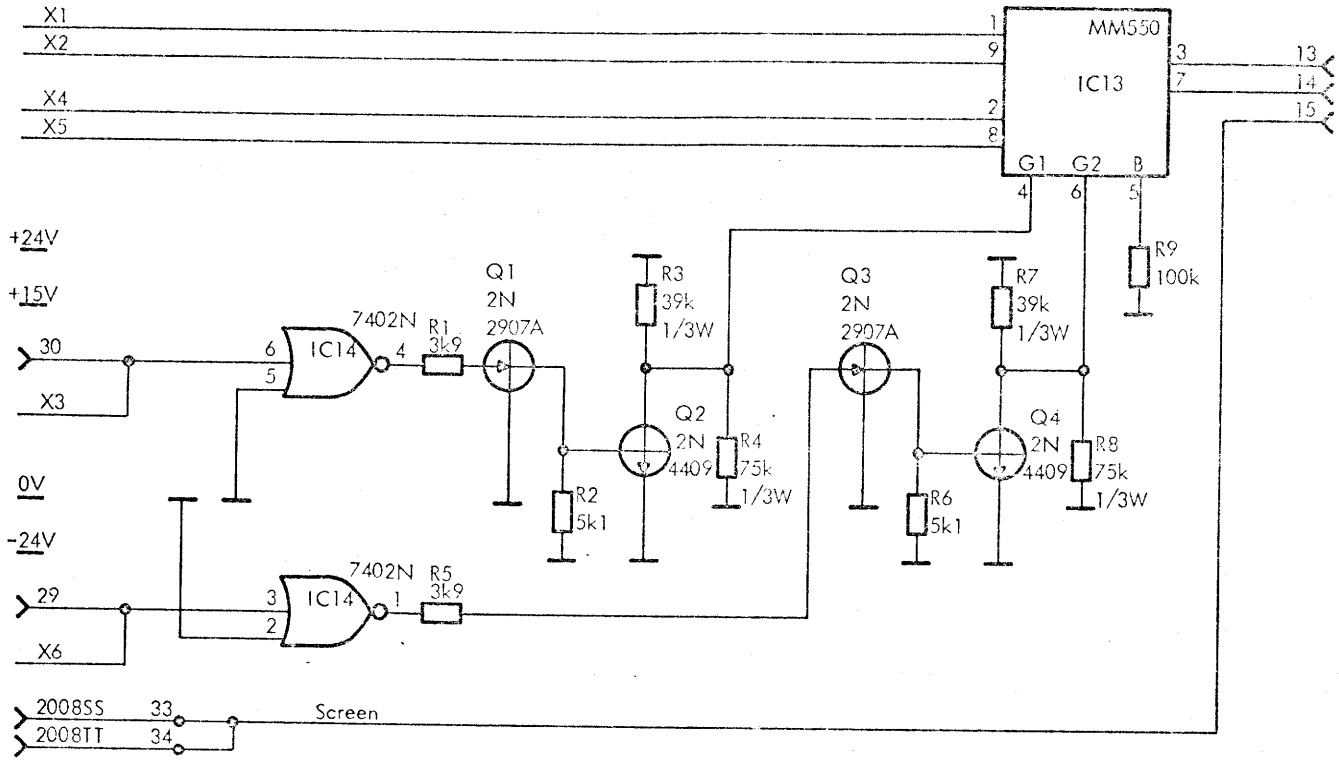
MPA401

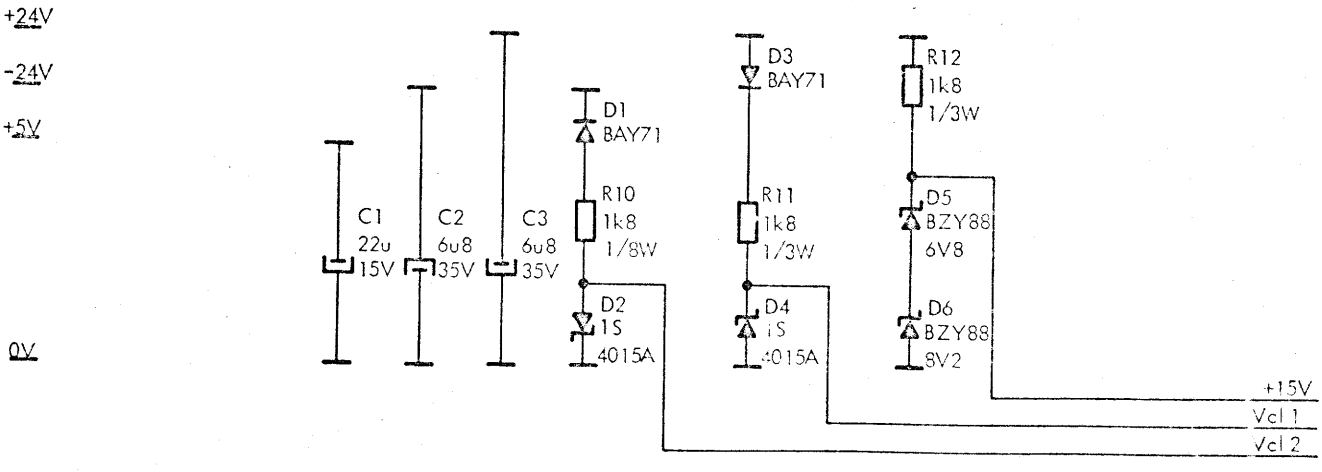
ANALOG MULTIPLEXER

MPA002

V12074

PCBA Circuit Diagram


X1
X2
X4
X5
MM550
IC13
G1
G2
B
+24V
+15V
30
X3
0V
-24V
29
X6
IC14
7402N
R1
3k9
Q1
2N
2907A
R3
39k
1/3W
Q2
2N
4409
R4
75k
1/3W
R2
5k1
Q3
2N
2907A
R7
39k
1/3W
Q4
2N
4409
R8
75k
1/3W
R6
5k1
R9
100k
R5
3k9
2008SS
2008TT
33
34
Screen


+24V
-24V
+5V
0V
C1
22u
15V
C2
6u8
35V
C3
6u8
35V
D1
BAY71
R10
1k8
1/8W
D2
1S
4015A
D3
BAY71
R11
1k8
1/3W
D4
1S
4015A
R12
1k8
1/3W
D5
BZY88
6V8
D6
BZY88
8V2
+15V
Vcl 1
Vcl 2

MULTIGAIN AMPLIFIER AMP 402

1. MAIN CHARACTERISTICS

Multigain Amplifier, AMP 402, is a differential DC amplifier equipped with logical inputs for external gain selection.
It can be placed in chassis CHS 401 together with Multiplexer Address Decoder, MAD 401, and Analog Multiplexer, MPA 401.

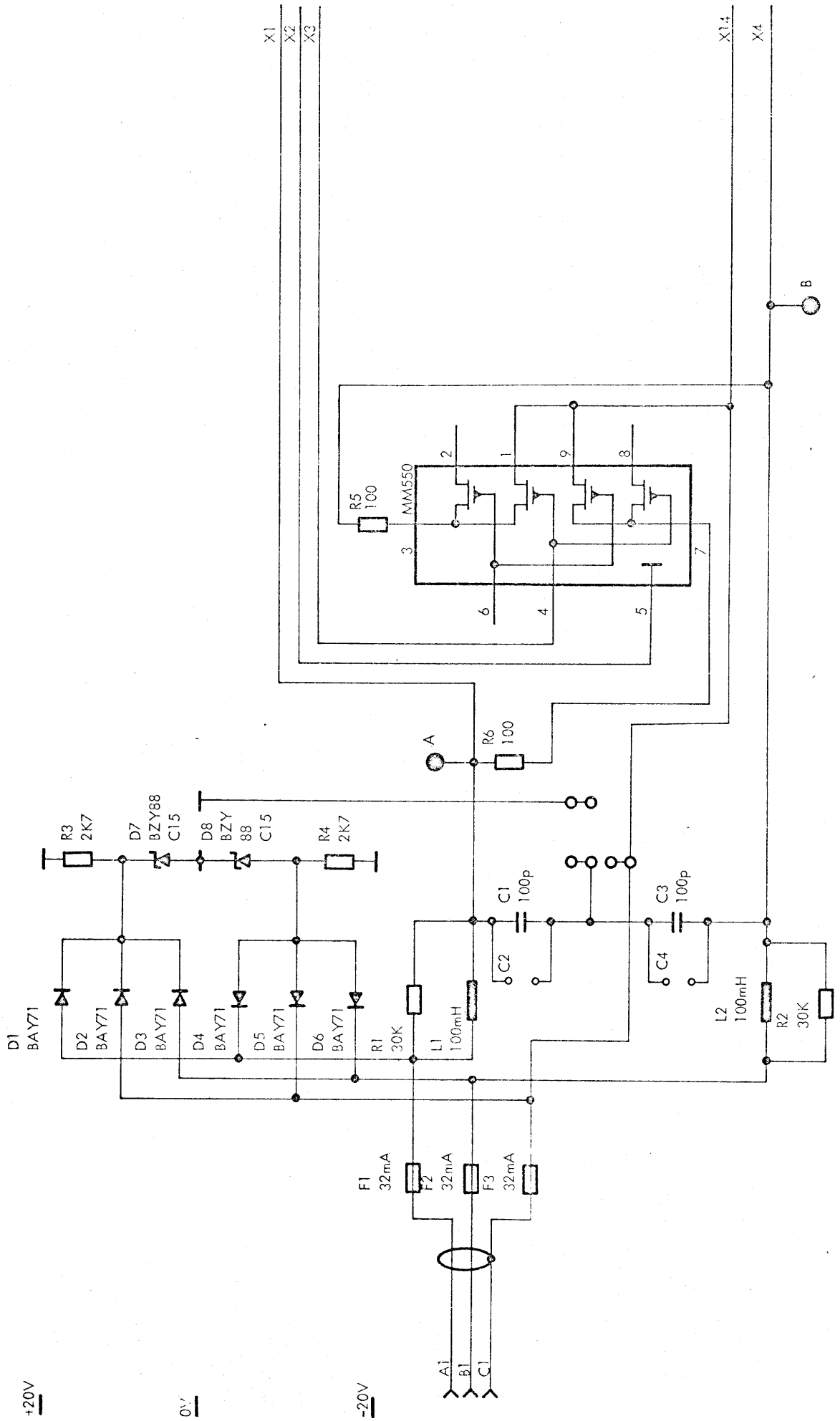
2. APPLICATIONS

Selective amplification of DC signals in industrial process control.

3. SPECIFICATIONS

Input Impedance:	Differential mode:	min. 10,000 Mohms
	Common mode:	min. 10,000 Mohms
Max. Input Voltage Range:	±13.5 V (either side)	
Differential Input Current:	Max. 0.5 nA	
CM - Input Current:	Max. 1 nA	
Output Impedance:	Max. 0.1 ohm	

Output Voltage Range:	±10 V (single-ended)
Output Current:	Max. 5 mA
Capacitive Load:	Max. 50 nF
Gains:	Totally 4 within 1 through 1000 (e.g.: 1, 10, 50, 500)
Accuracy at 25 degrees C:	±0.025 per cent of full scale or ±10 micro V whichever is greater (ref. to input)
Temperature Drift:	Max. (±1.5 micro V ref. to input ±30 ppm) per degree C
Common Mode Rejection Ratio at 50 cps:	[60 dB + 20 log (gain)] or 110 dB, whichever is less.
Settling Time (to within 0.01 per cent of final value):	(100 + 0.5×gain) microseconds (bipolar signals)
Control Input:	4 gain selection inputs (TTL levels) 1 amplifier reset input (TTL level)
Dimensions:	Height: 177 mm Width: 48 mm Depth: 450 mm
Supply Voltages:	+5 V ±5 per cent, 15 mA +24 V ±2 per cent, 400 mA (first 30 seconds), 80 mA continuous -24 V ±2 per cent, 400 mA (first 30 seconds), 80 mA continuous
Power Supply Rejection:	Min. 90 dB (V/V), ref. to output
Ambient Air:	Temperature: 0 to 45 degrees C Relative Humidity: 30 to 70 per cent
Weight:	0.7 kg

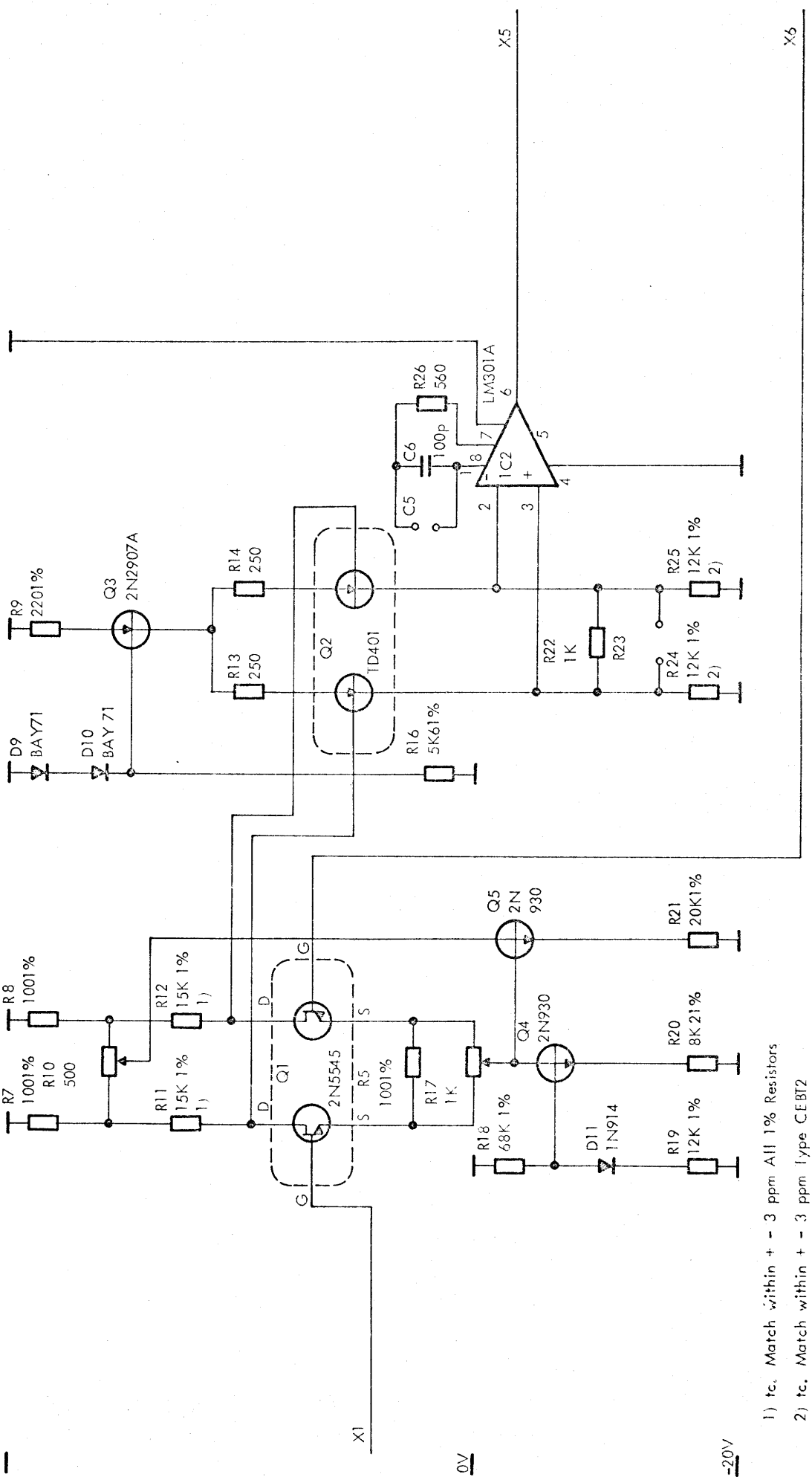


AMP402

AMP001

V12626

PCBA CIRCUIT DIAGRAM



1) tc. Match within + - 3 ppm All 1% Resistors

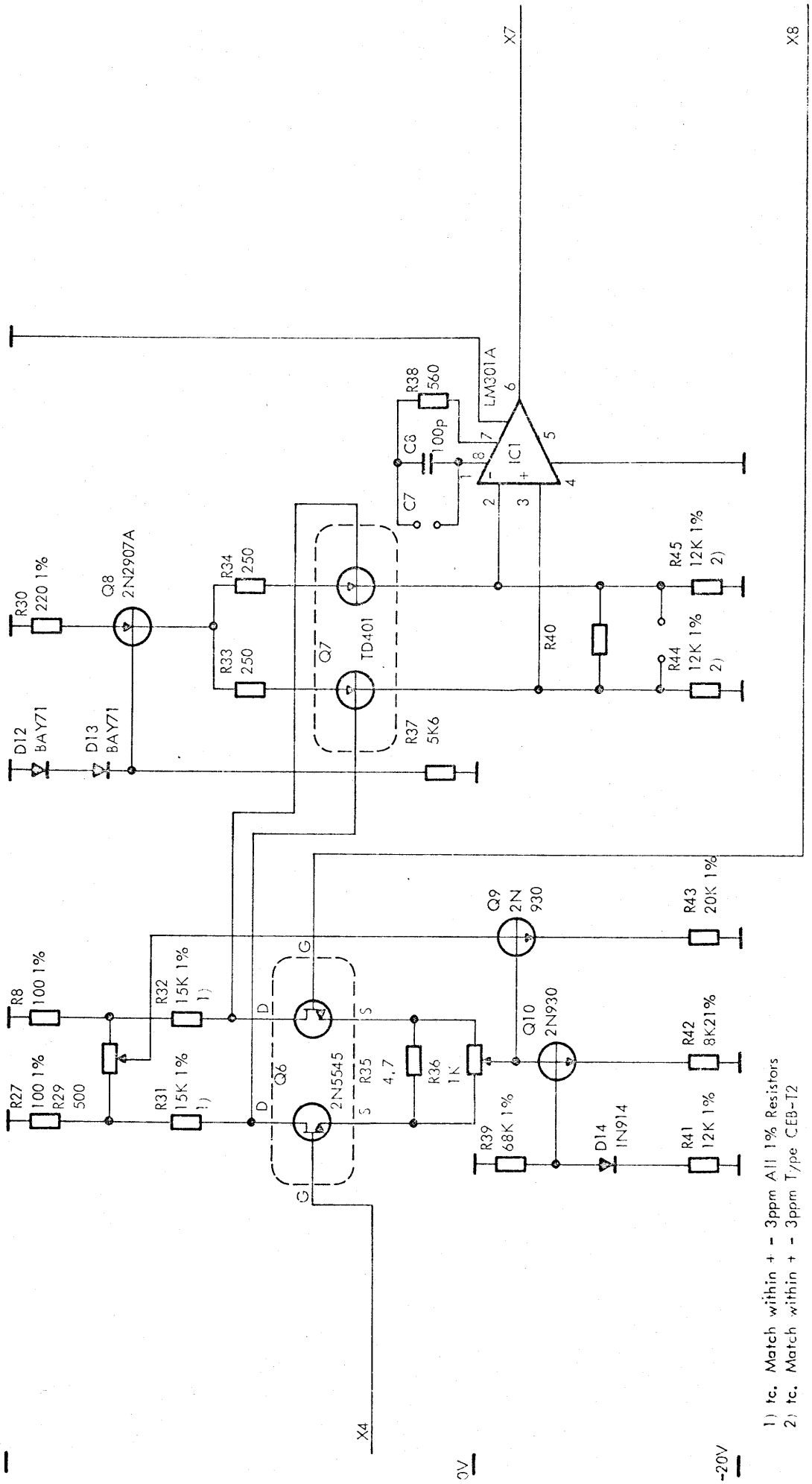
2) tc. Match within + - 3 ppm type CEBT2

AMP402

V12627

PCBA CIRCUIT DIAGRAM

AMP 002



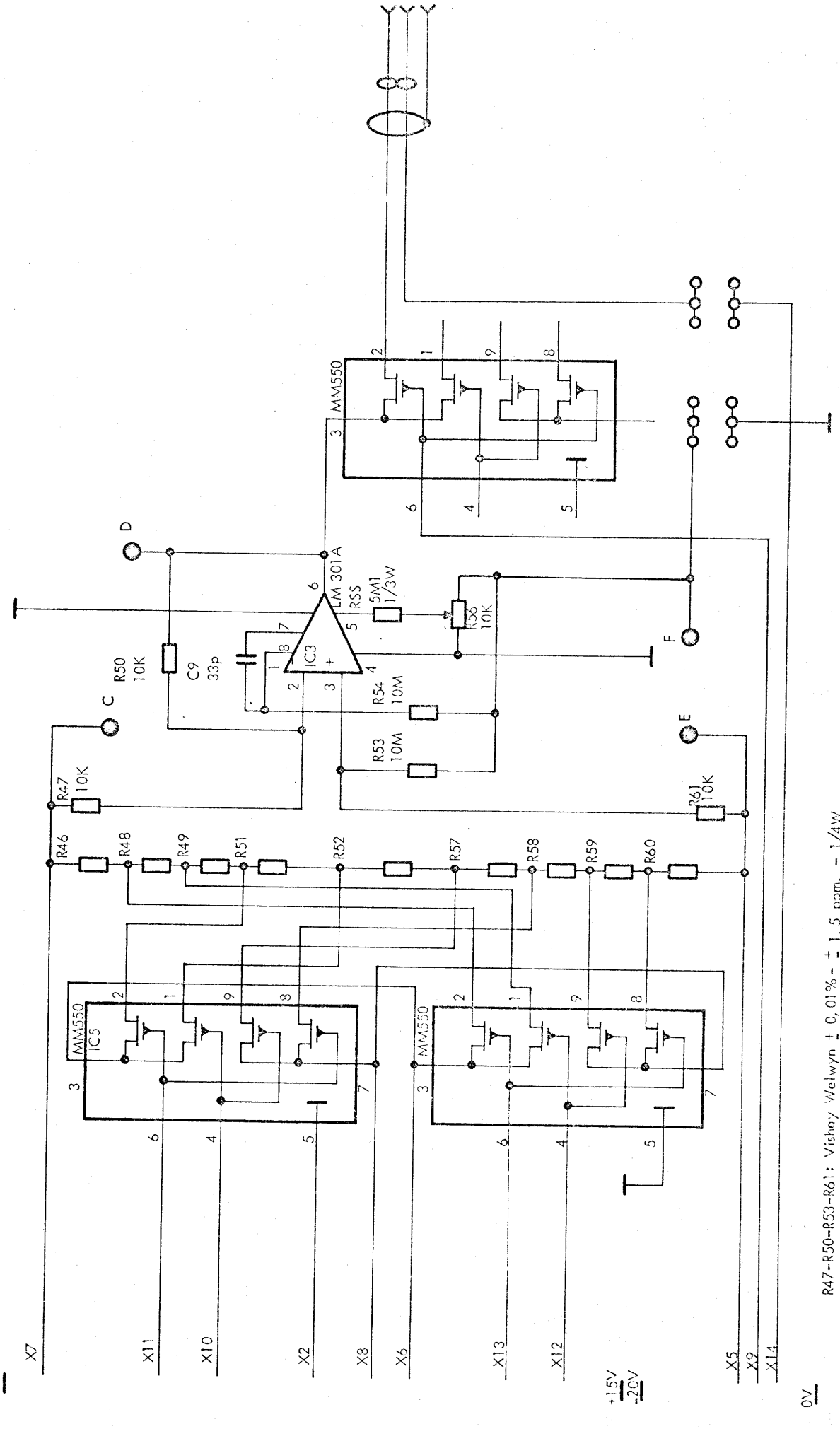
1) tc. Match within + - 3ppm All 1% Resistors
2) tc. Match within + - 3ppm Type CEB-T2

AMP402

V12628

PCBA CIRCUIT DIAGRAM

AMP003



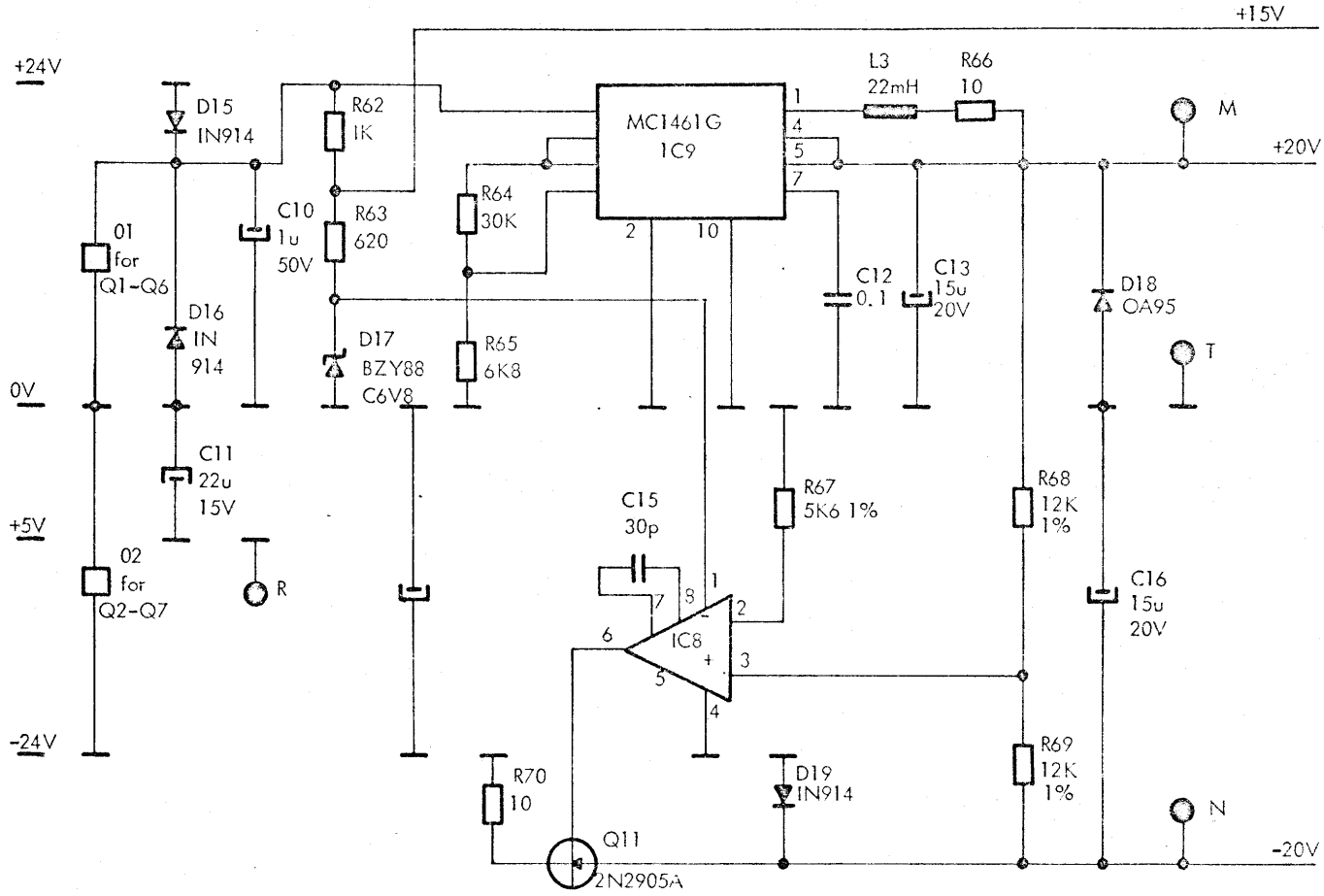
R47-R50-R53-R61: Vishay Welwyn ± 0,01% - ± 1,5 ppm. - 1/4W
R46-R48-R49-R51-R52-R57-R58-R59-R60. Customer Selected.

AMP 402

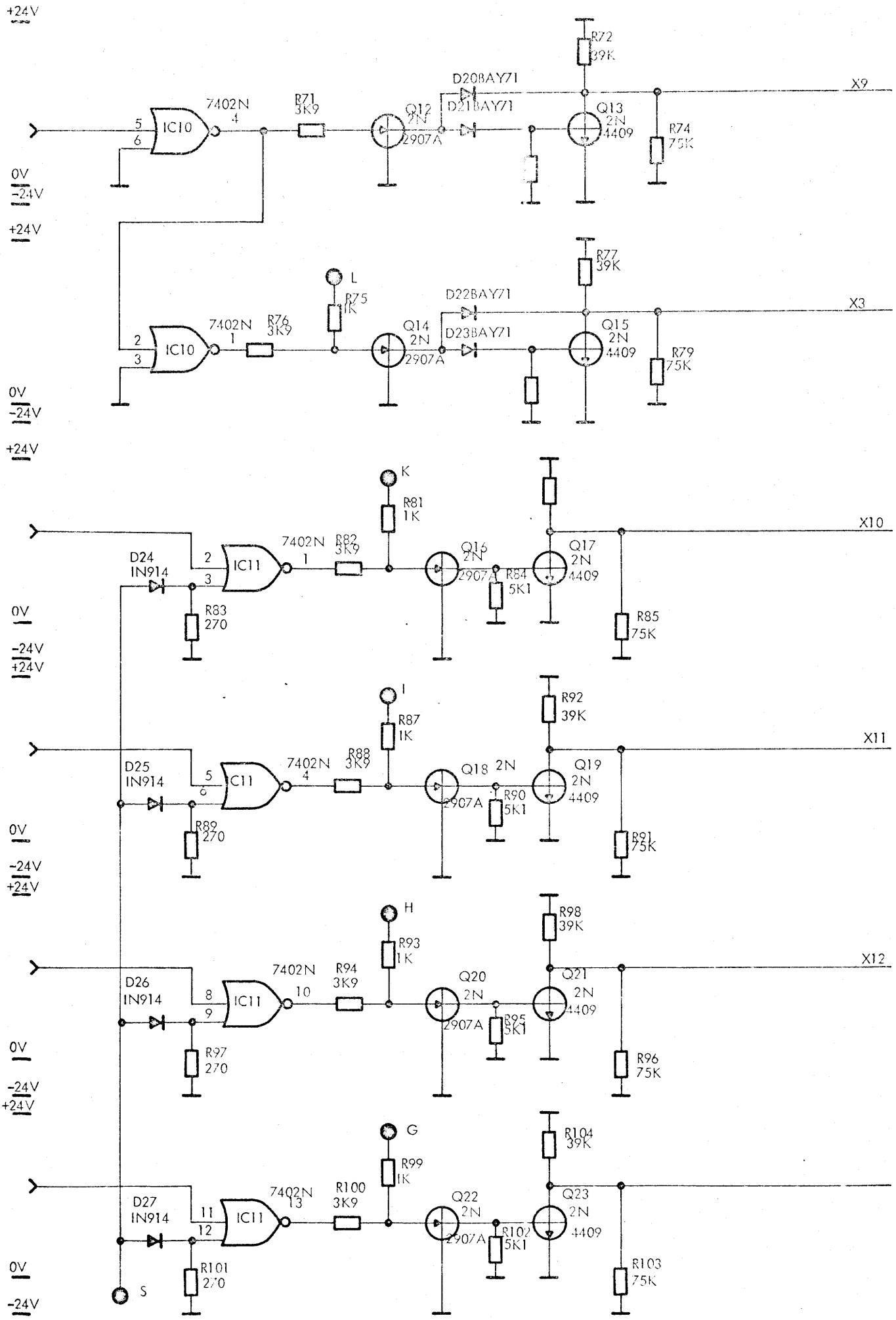
A MP004

J12629

PCBA CIRCUIT DIAGRAM



01 - 02: Owen Texas 4ST1-2
L3: Prahn type 1582
All 1% Resistors CEB-T2



AMP402

AMP006

V12631

PCBA CIRCUIT DIAGRAM

LOW-PASS FILTERS, FLT402 AND CHASSIS CHS405

FLT402 is a module equipped with 16 symmetrical, low-pass filters. Up to 8 FLT402 modules can be placed in chassis, CHS405.
FLT402 is used where suppression of differential-mode noise at line frequency or higher frequencies is necessary. One filter is used per analog input channel to ensure a high scanning rate.

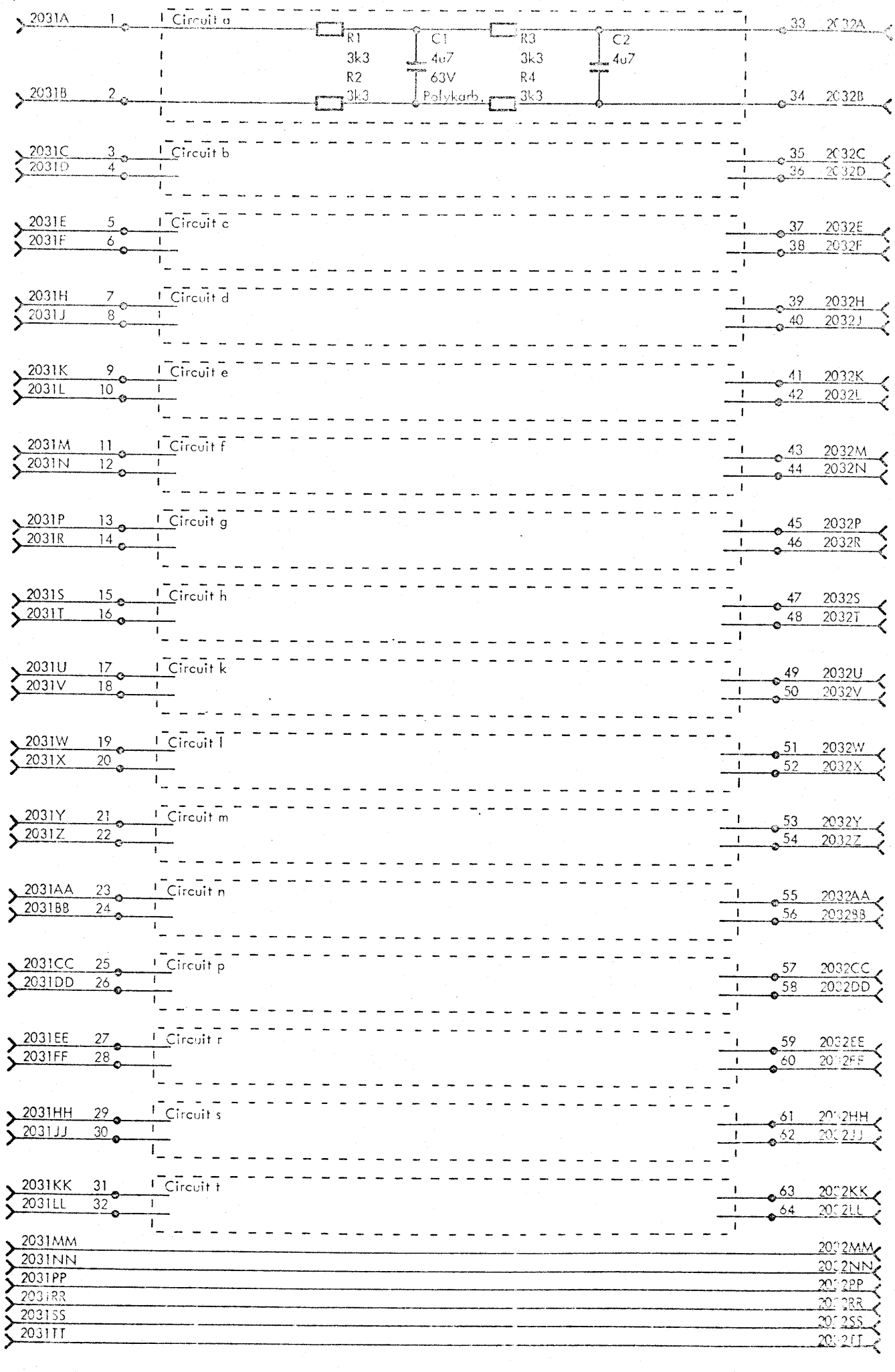
Specifications:

FLT402:

Number of Filters:	16
Filter Type:	Symmetrical 2nd order R-C filter with resistive input and capacitive output.
Resistance Value (each side):	3.3 Kohm ±5 per cent
Condenser Value:	4,7 uF ± 10 per cent, max. 63 V (metalized polycarbonate)
Attenuation at 50 Hz:	40 dB, increasing 40 dB per decade for increasing frequency.
Dimensions:	Height: 178 mm Width: 24 mm Depth: 450 mm
Ambient Air:	Temperature: 0 to 45 degrees C Relative humidity: 30 to 70 per cent
Weight:	0.5 kg

CHS405:

Max. Number of Filter Modules:	8 FLT402
Dimensions:	Height: 178 mm
	Width: 483 mm
	Depth: 592 mm
Weight:	12.0 kg



FLT 402

FLT001

V12109

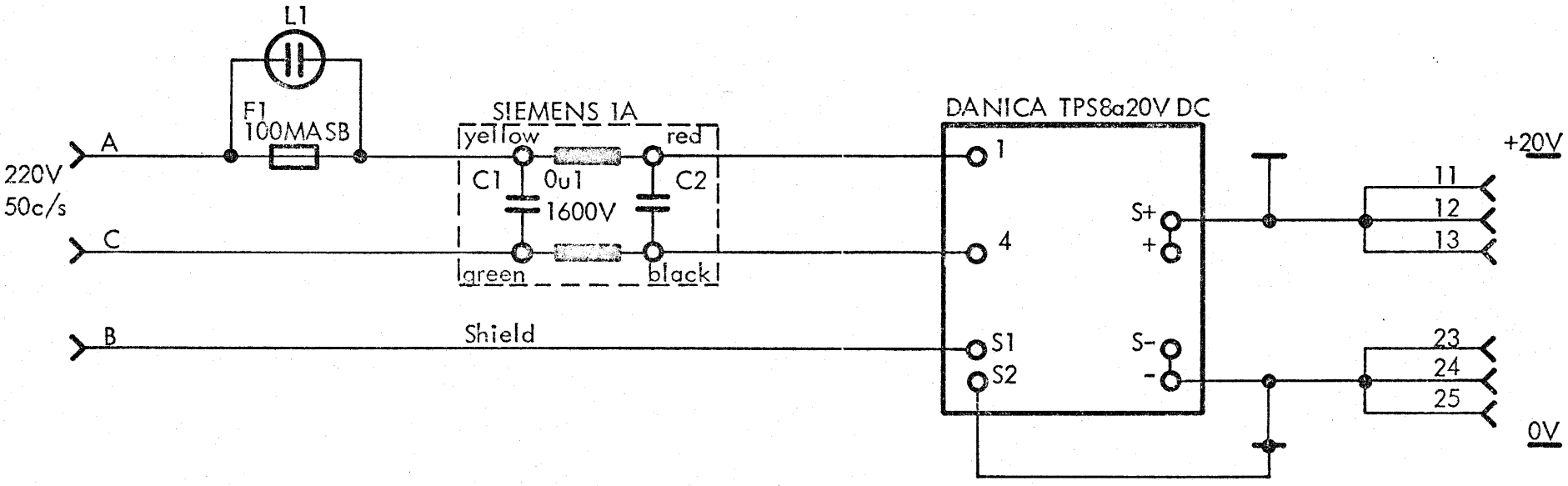
PCBA Circuit Diagram

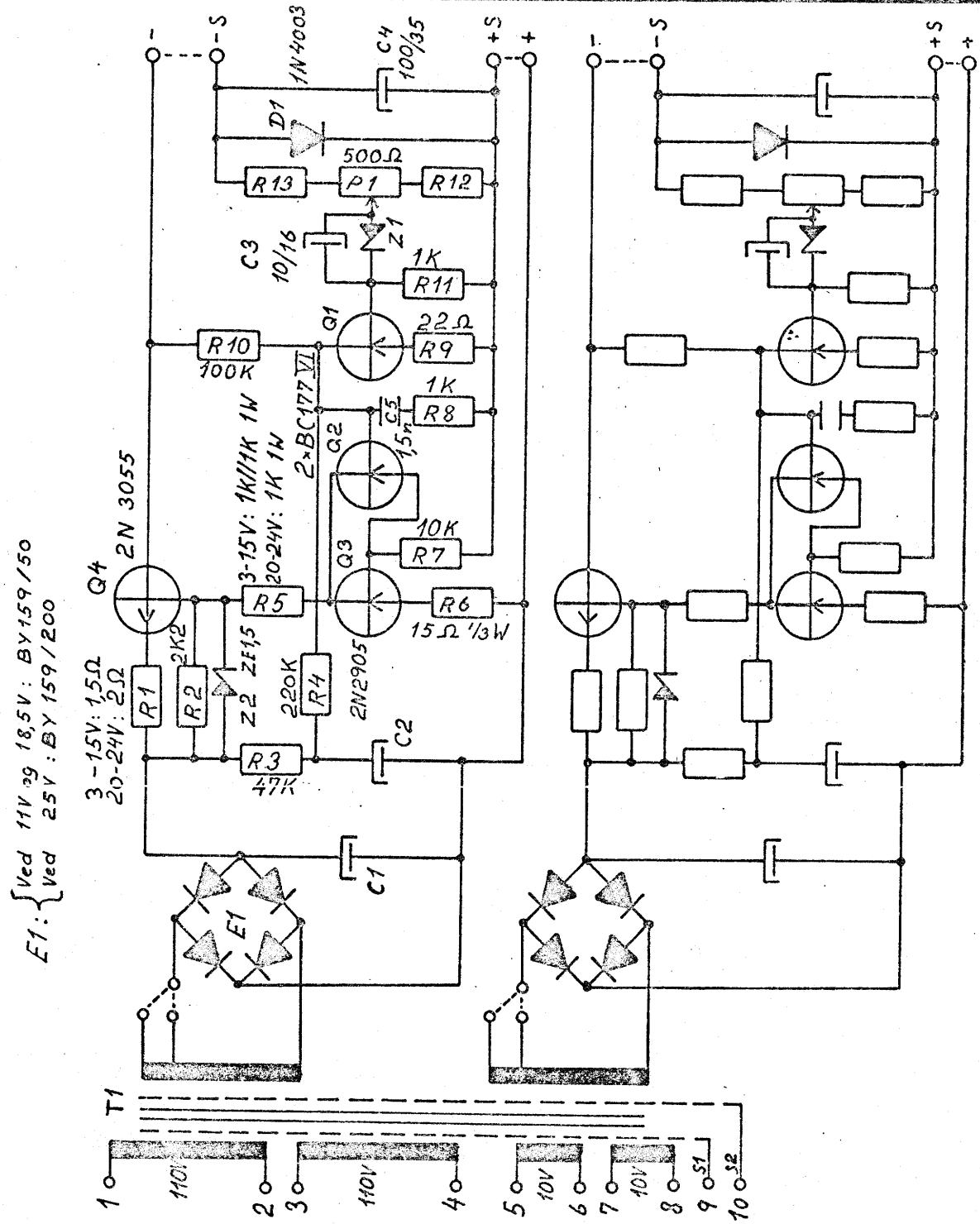
150469HAO 191170SSL 191170SSL 191170HAO

POW 410

POW 410 Wiring Diagram for 20V DC Power Supply

V21678





TPS 8a is a singel power supply consisting of one regulator unit.
$I_{load\ max}$ = 5oo mA. or 35o mA. (2o-24V)

TPS 8b is a double power supply consisting of two regulator units as shown in the diagram. $I_{load\ max}$ = 5oo mA from each unit, or 35o mA (2o-24V).

I_{max}	E_{out}	Z 1	R 12	R 13	C 1	C 2	E_{trf}
o,5 A	3 - 5 V	ZF 2,7	39o ohm	47 ohm	looouF/35V	25uF/25V	11 V
o,5 A	5 - 7 V	ZF 4,7	39o ohm	47 ohm	looouF/35V	25uF/25V	11 V
o,5 A	7 - V	1 N 7o8	82o ohm	22o ohm	looouF/35V	25uF/25V	11 V
o,5 A	12 -15 V	1 N 711	82o ohm	39o ohm	looouF/35V	25uF/25V	18,5V
o,35A	2o -24 V	1 N 711	68o ohm	1,5Kohm	looouF/5oV	louF/5oV	25 V

MODULAR POWER SUPPLY TPS 8a and 8b

Diagram

KONSTR.

TEGN. 9/3-7o AH

GODK.

MÅLESTOK

MATERIALE

DANICA ELEKTRONIK

TEGNING NR.

68o72/2

A 4

AGF 884

RESISTANCE-BRIDGES, RBG401

RBG401 is a module equipped with 16 identical precision resistance-bridges and an integrated dc-reference-voltage regulator. Up to 8 RGB401 modules can be placed in chassis CHS403 together with one powersupply POW 410.

Applications:

RBG401:

Resistance-to-Voltage conversion where the transducer is a resistance (e.g. a Platinthermometer with 100 ohm/at 0 degree centigrade). Connection is performed with 3 wires for cable resistance compensation.

Specifications:

RBG401:

Number of Inputs:	16
Resistance Value:	2 x 16Kohm, 0,02 per cent 1 x 100 ohm, ± 0,1 per cent
Input Terminal Connection:	3-wire for cable resistance compensation
Output Voltage:	$E_{out} = \frac{10\ R_{in}}{16000 + R_{in}} - \frac{1}{16,1}$ where Rin is the absolute value of the transmitter-resistance.
Output Voltage Range:	Eout = 0 - 150 mV, corresponding to transmitter-resistance values from about 100 ohms to 350 ohms.

$$R_{in} = \frac{16000 \times (16.1 \times E_{out} + 1)}{160 - 16.1 \times E_{out}}$$

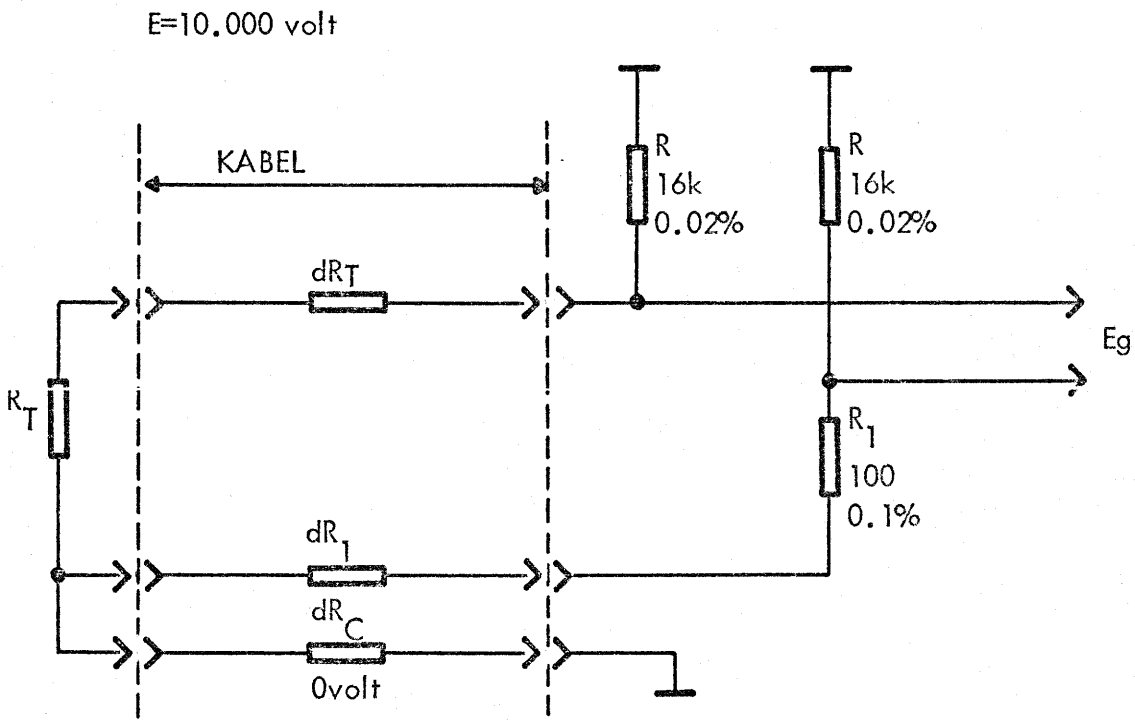
$$R_{-100} = \frac{16.1 \times 1610 \times E_{out}}{160 - 16.1 \times E_{out}}$$

$$R_T = R_0 (1 + AT + BT^2)$$

$A = 0,3907840760 \cdot 10^{-2}$ grad^{-1}

$B = -0,5784084 \cdot 10^{-6}$ grad^{-1}

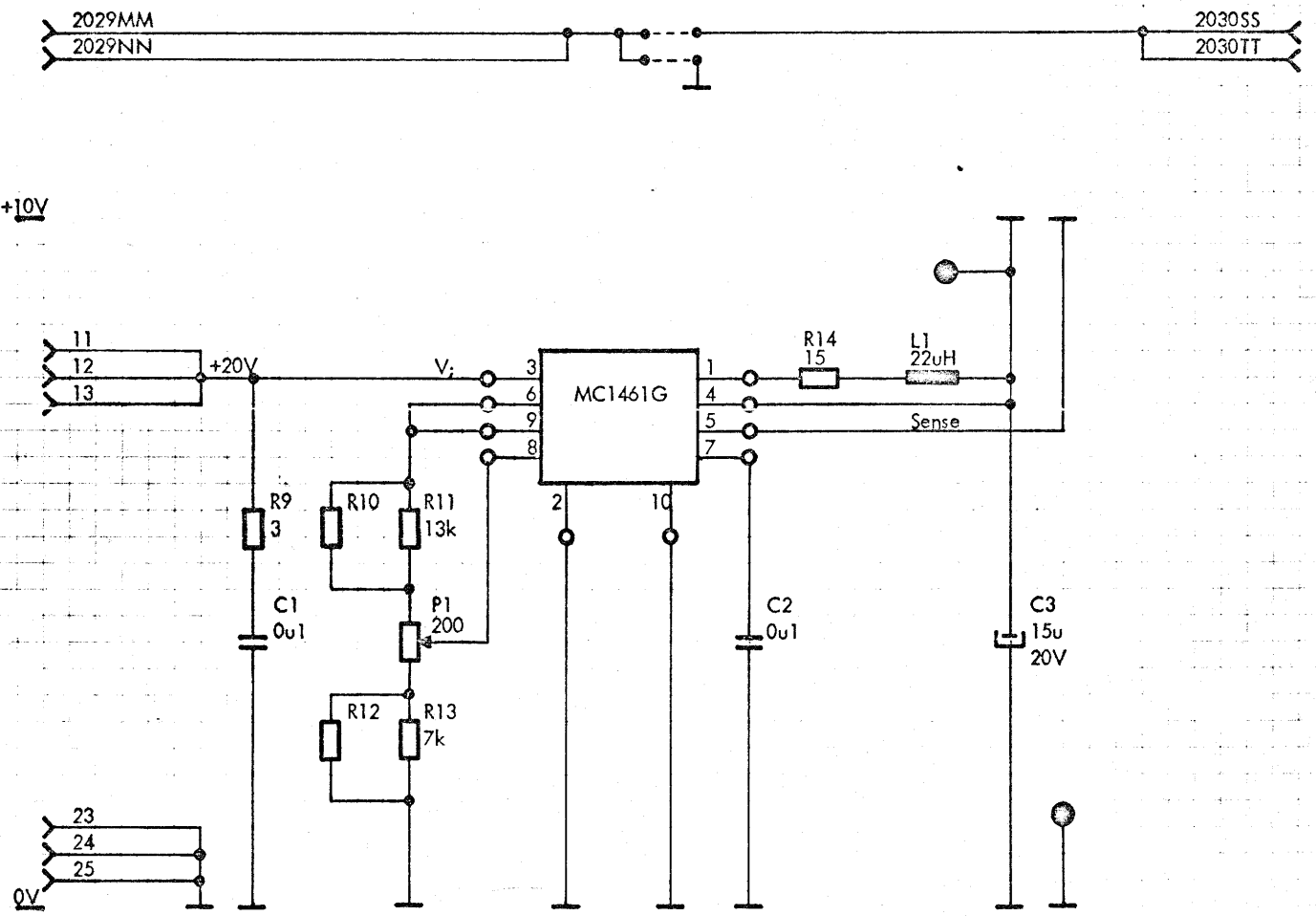
Accuracy, using 3-wire Connection and with a Cable Resistance of less than 10 ohms per wire:	Better than 0.25 per cent of reading.
Supply Power:	+ 20 V dc, 30 mA
Ambient Air:	Temperature: 0 - 45 degrees C Relative Humidity: 30 to 70 per cent
Dimensions:	Height: 177 mm Width: 24 mm Depth: 450 mm
Weight:	0.5 kg



Brokredsløbet er designet for tilslutning med tre-ledning-princippet, hvilket medfører minimum målefejl hidrørende fra kabelmodstand.

Unit:	Designed 231170HAO	PRINCIPDIAGRAM for MODSTANDSBROER RBG401	Drawing No V21682
CENTRALEN	Approved		Drawn by
	Checked		Checked
	Last Revision		Sheets / Sheet

69.55.AA-302.mod3



Replaced by Dwg. No.

due to ECN

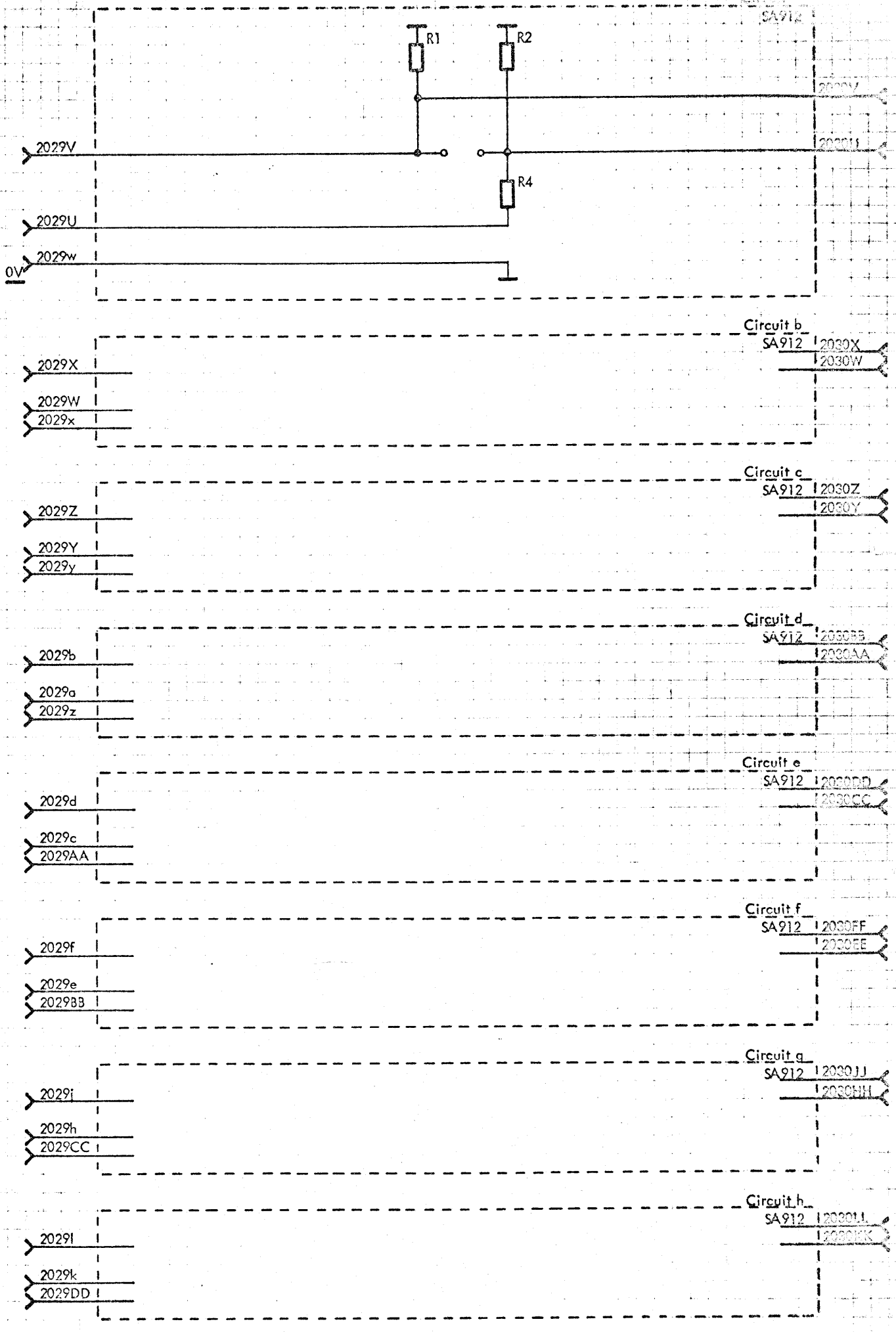
Replaces Dwg. No.

Drawn 171170PAJ 19/11/70

Designed by 150969HAO

A/S REGNECENTRALEN

Unit RSG 401		RSG001
Dwg. No. V12106	PCBA Circuit Diagram	



Designed by 150969HAO

Drawn by 171170PAJ

Design Check 19/11/70 0552

Replaces Dwg. No.

Due to ECN

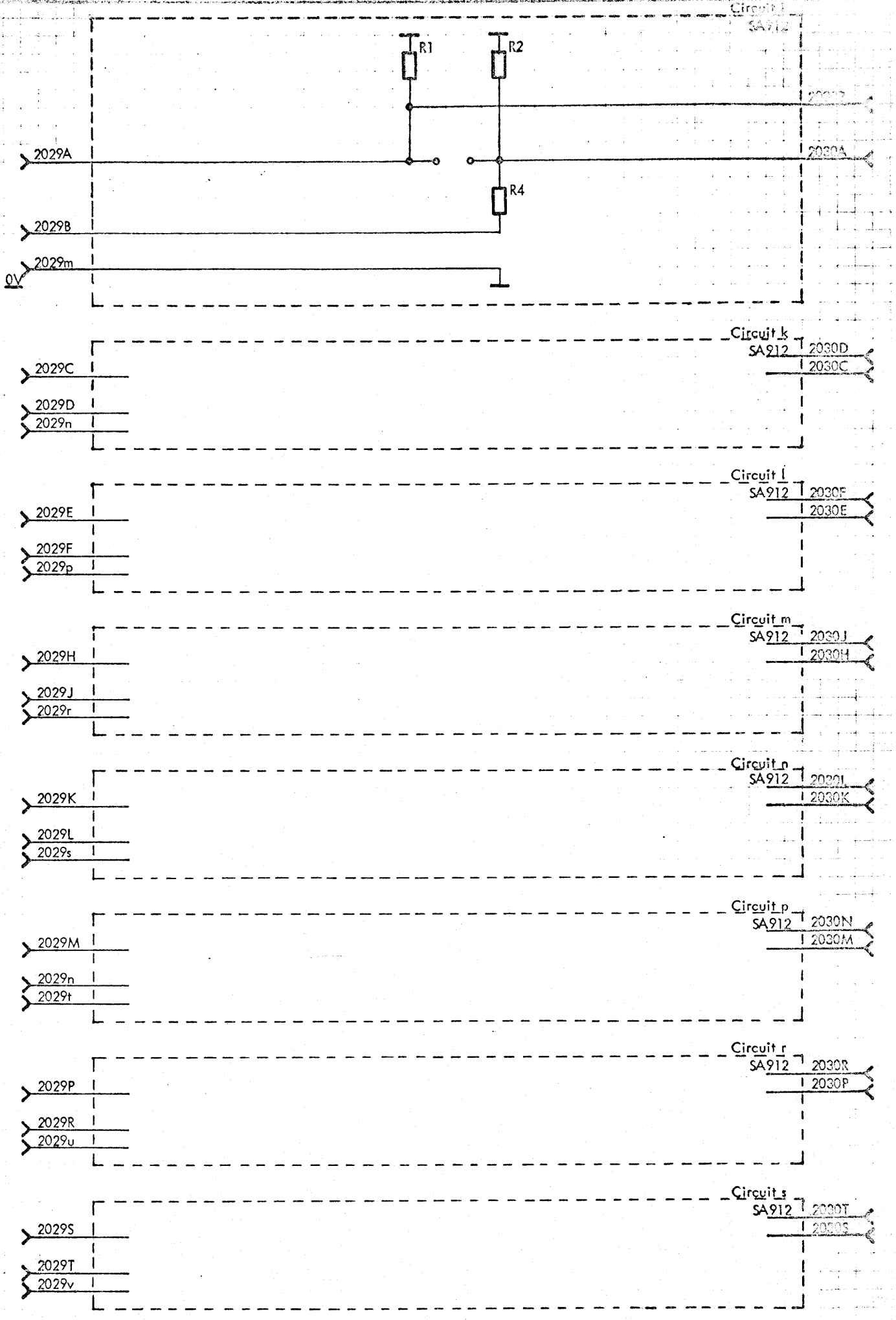
Replaced by Dwg. No.

A/S REGNECENTRALEN

Unit RBG 401

Dwg. No. V12137

PCBA Circuit Diagram



RBG 401	
V12138	PCBA Circuit Diagram

BUSLINE CONVERTER, BCV401 AND CHASSIS, CHS401

The Busline Converter, BCV401 is an adapter between the RC 4000 Low-Speed Data Channel and the sub-buslines of the CHS404 chassis in which up to 16 plug-in terminal units for process input/outputs can be placed. Thus the BCV401 can be shared among 16 digital process I/O-terminal units.

Specifications:

BCV401:

Connection to RC 4000:	Low-Speed Data Channel (LDC)
Conversion of Busline Signals:	All control and data buslines are converted from LDC levels to sub-busline levels and vice versa.
Number of Converted Interrupt Signals (Levels):	Max. 2
Dimensions:	Height: 355 mm Width: 48 mm Depth: 450 mm
Supply Power:	+ 5 V ± 5 per cent, 1500 mA + 12 V ± 5 per cent, 200 mA - 6 V ± 5 per cent, 500 mA
Ambient Air:	Temperature: 0 to 45 degrees C Relative Humidity: 30 to 70 per cent
Weight:	1.4 kg

Specifications (cont'd):

CHS404:

Max. Number of Digital Process I/O Modules (besides 1 BCV401):	16
Service Connector:	1 (at the rear of the chassis)
Dimensions:	Height: 355 mm Width: 483 mm Depth: 592 mm
Weight:	21.0 kg

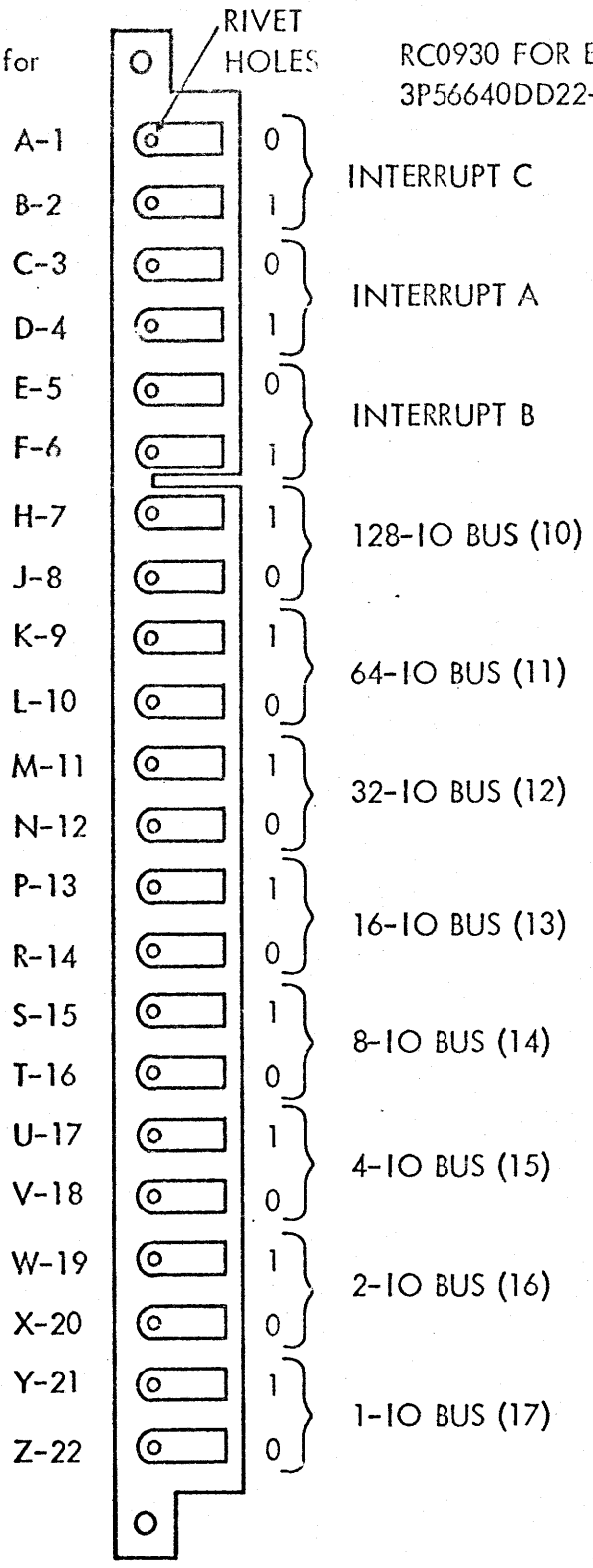
SUBBUSLINE IN CHS 404, CONNECTED TO RC 4000 LOW SPEED BUS VIA BCV 401.

SIGNAL - AND SUPPLY POWER - ALLOCATION:

UPPER CONNECTOR, ULTRA CONTINENTAL, 6P55600 DD40 - 40				LOWER CONNECTOR, ULTRA CONTINENTAL, 6P55600 DD40 - 40			
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	SHIELD	A	SHIELD	1	0V	A	0V
2	SHIELD	B	SHIELD	2	IO CONN	B	IO CONN.
3	+5V SUPPLY	C	+5V SUPPLY	3	0V	C	0V
4	-6V SUPPLY	D	-6V SUPPLY	4	IO READY	D	IO READY
5	+12V SUPPLY	E	+12V SUPPLY	5	0V	E	0V
6	INTERCONN.	F	INTERCONN.	6	INTERRUPT A	F	INTERRUPT A
7	INTERCONN.	H	INTERCONN.	7	0V	H	0V
8	NOT USED	J	NOT USED	8	INTERRUPT B	J	INTERRUPT B
9	0V	K	0V	9	0V	K	0V
10	IO BUS (0)	L	IO BUS (0)	10	IO BUS (12)	L	IO BUS (12)
11	0V	M	0V	11	0V	M	0V
12	IO BUS (1)	N	IO BUS (1)	12	IO BUS (13)	N	IO BUS (13)
13	0V	P	0V	13	0V	P	0V
14	IO BUS (2)	R	IO BUS (2)	14	IO BUS (14)	R	IO BUS (14)
15	0V	S	0V	15	0V	S	0V
16	IO BUS (3)	T	IO BUS (3)	16	IO BUS (15)	T	IO BUS (15)
17	0V	U	0V	17	0V	U	0V
18	IO BUS (4)	V	IO BUS (4)	18	IO BUS (16)	V	IO BUS (16)
19	0V	W	0V	19	0V	W	0V
20	IO BUS (5)	X	IO BUS (5)	20	IO BUS (17)	X	IO BUS (17)
21	0V	Y	0V	21	0V	Y	0V
22	IO BUS (6)	Z	IO BUS (6)	22	IO BUS (18)	Z	IO BUS (18)
23	0V	AA	0V	23	0V	AA	0V
24	IO BUS (7)	AB	IO BUS (7)	24	IO BUS (19)	AB	IO BUS (19)
25	0V	AC	0V	25	0V	AC	0V
26	IO BUS (8)	AD	IO BUS (8)	26	IO BUS (20)	AD	IO BUS (20)
27	0V	AE	0V	27	0V	AE	0V
28	IO BUS (9)	AF	IO BUS (9)	28	IO BUS (21)	AF	IO BUS (21)
29	0V	AH	0V	29	0V	AH	0V
30	IO BUS (10)	AJ	IO BUS (10)	30	IO BUS (22)	AJ	IO BUS (22)
31	0V	AK	0V	31	0V	AK	0V
32	IO BUS (11)	AL	IO BUS (11)	32	IO BUS (23)	AL	IO BUS (23)
33	0V	AM	0V	33	NOT USED	AM	NOT USED
34	IO ENABLE	AN	IO ENABLE	34	INTERCONN.	AN	INTERCONN.
35	0V	AP	0V	35	INTERCONN.	AP	INTERCONN.
36	IO ADDRESS	AR	IO ADDRESS	36	+12V SUPPLY	AR	+12V SUPPLY
37	0V	AS	0V	37	-6V SUPPLY	AS	-6V SUPPLY
38	IO ACTIVATE	AT	IO ACTIVATE	38	+5V SUPPLY	AT	+5V SUPPLY
39	0V	AU	0V	39	SHIELD	AU	SHIELD
40	IO TRANSFER	AV	IO TRANSFER	40	SHIELD	AV	SHIELD

NOTE: ALL LOGIC SIGNALS ARE IN LOW REPRESENTATION.

Device no and interrupt plug for process input/output units in CHS404, connected to RC4000 low speed bus via BCV401.



RIVET ALLOCATION: FOR INTERRUPTS: "1"-Position for Selected Interrupt
"0"-Position for not Selected Interrupts

FOR DEVICE ADDR: "1"-Position for effective Binary Figure
"0"-Position for non effective Binary Figure

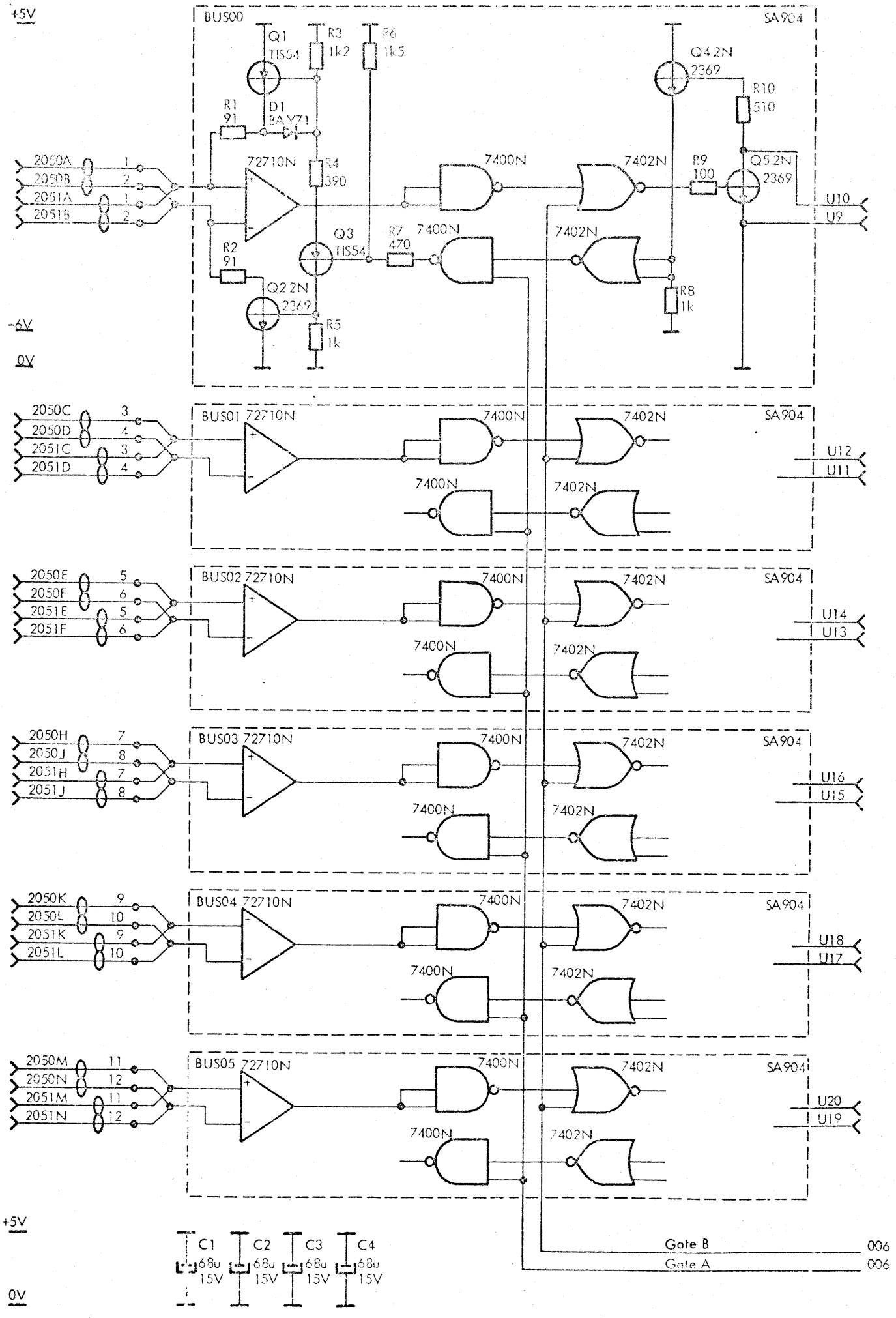
(EXAMPLE: Device Address 87 gives rivets in J-8, K-9, N-12, P-13, T-16, U-17, W-19, Y-21, as 87=0x128+1x64+0x32+1x16+0x8+1x4+1x2+1x1
Interrupt B selected gives Rivets in A-1, C-3, F-6)

I/O DEVICE ADDRESS PLUG FOR: _____

RC4000 INSTALATION: _____

RCSL: 51 - VB880 Maj 1970/VTP

DWG NO.



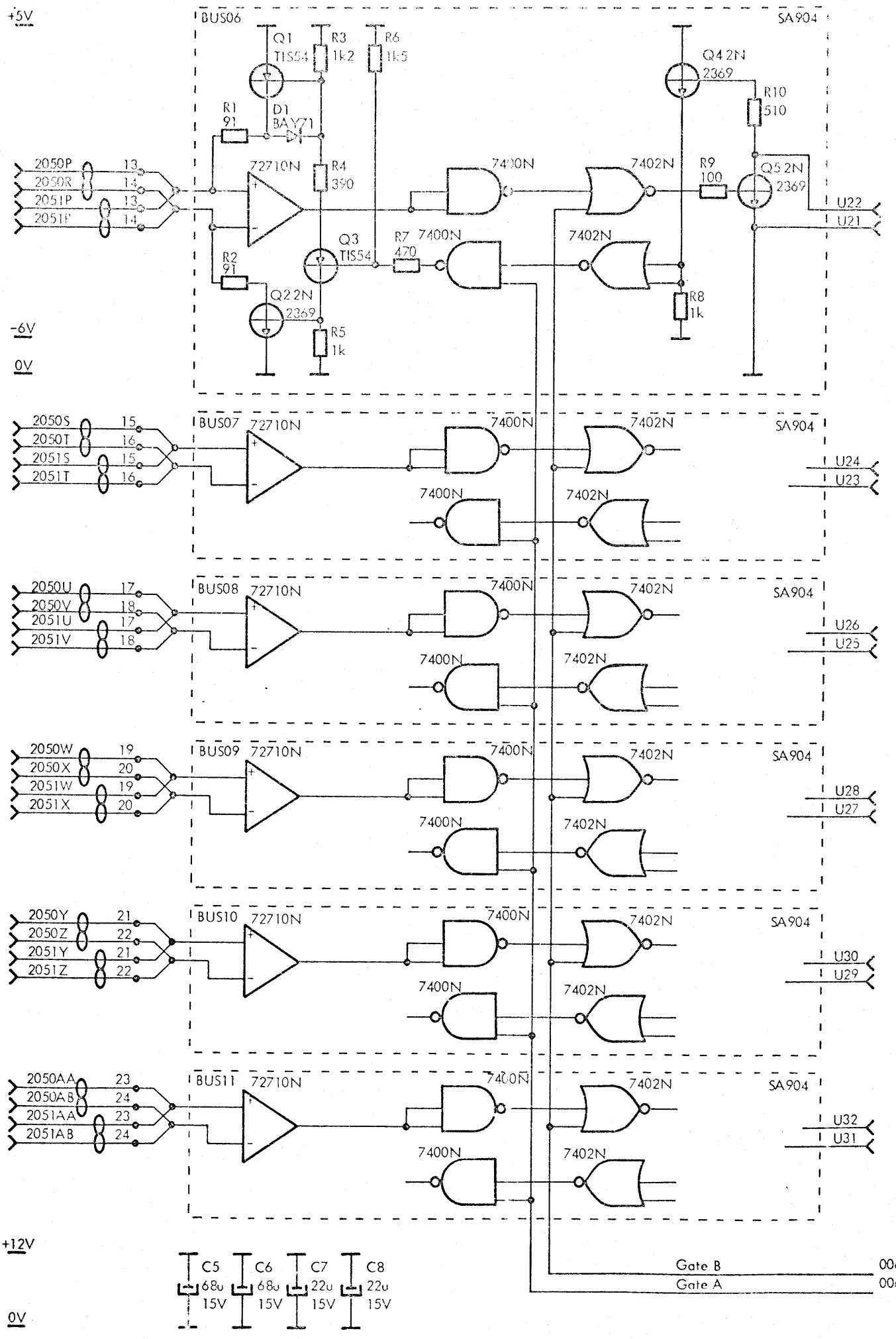
BCV401

BUS(0:5)

BCV001

V12064

PCBA Circuit Diagram



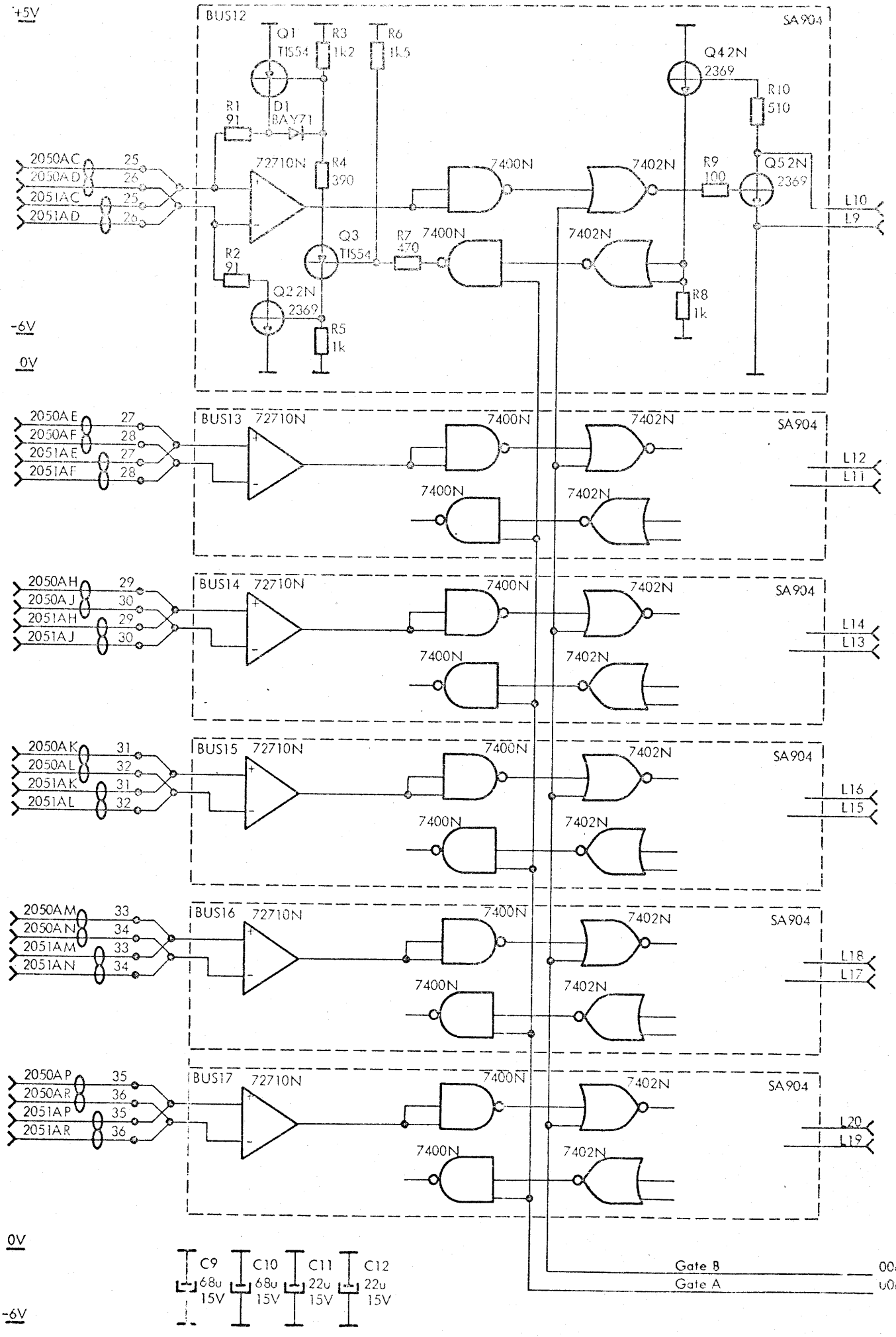
BCV401

BUS(6:11)

BCV002

V12065

PCBA Circuit Diagram



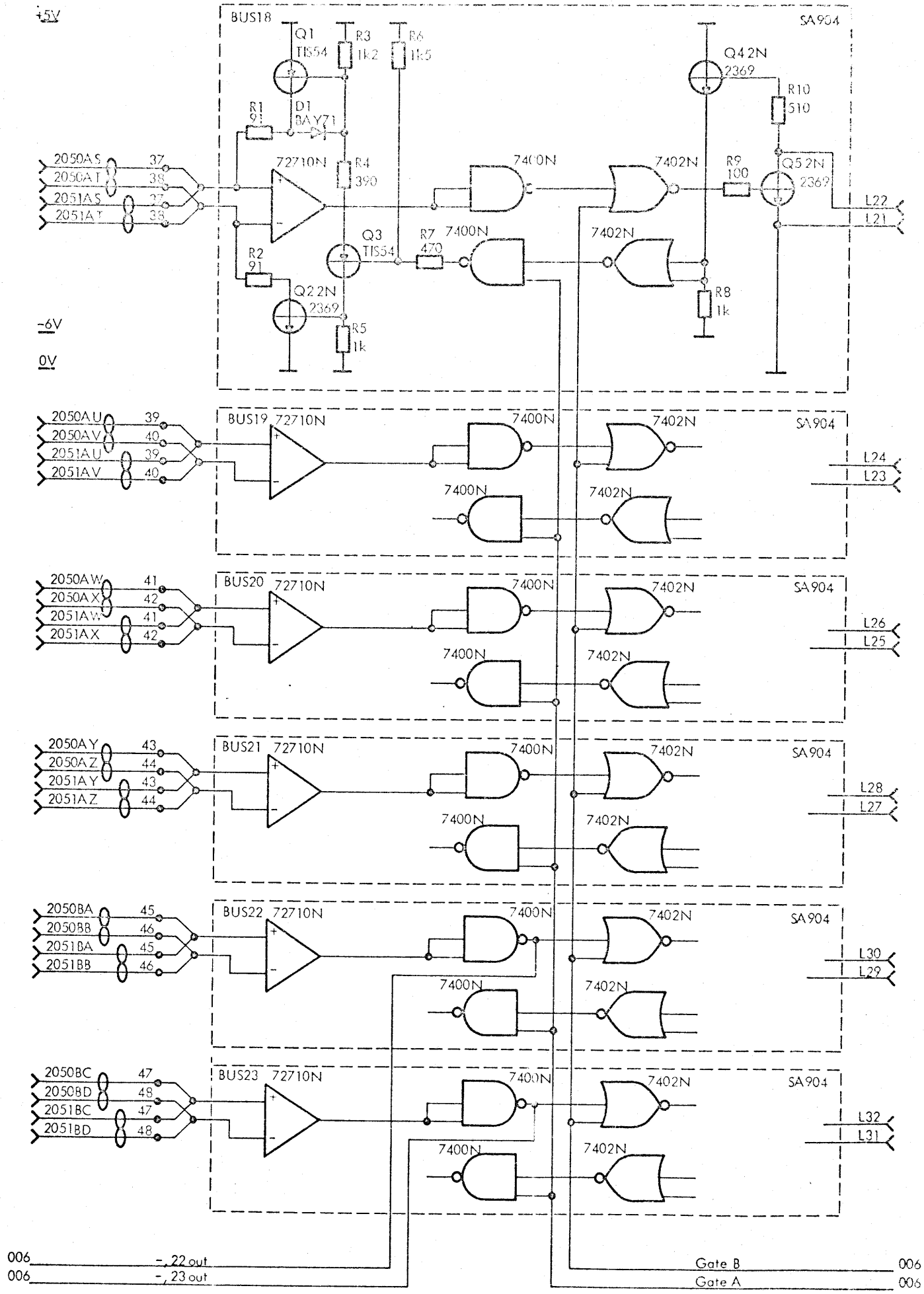
BCV401

BUS(12:17)

BCV003

V12066

PCBA Circuit Diagram



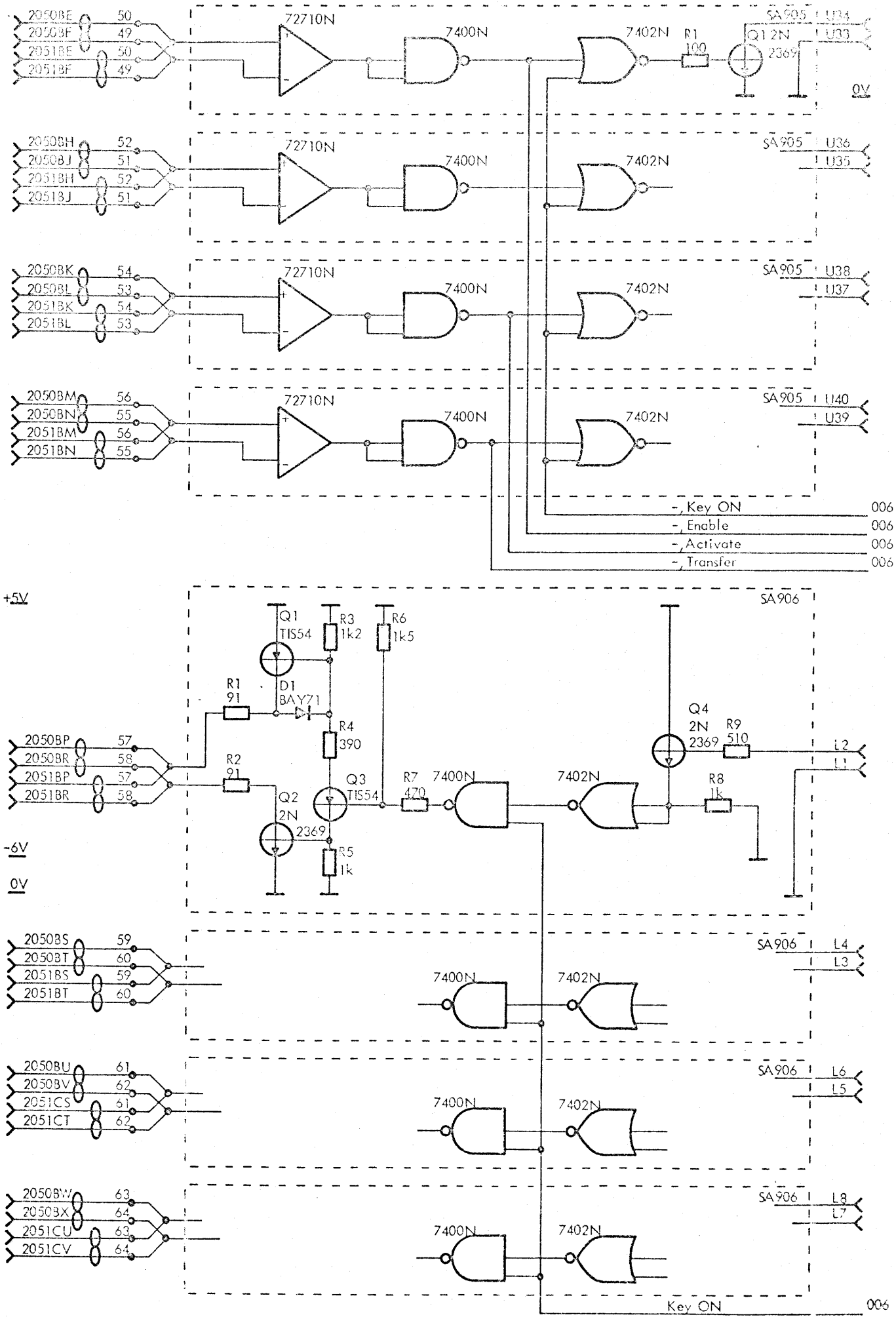
BCV401

V12067

BUS(18:23)

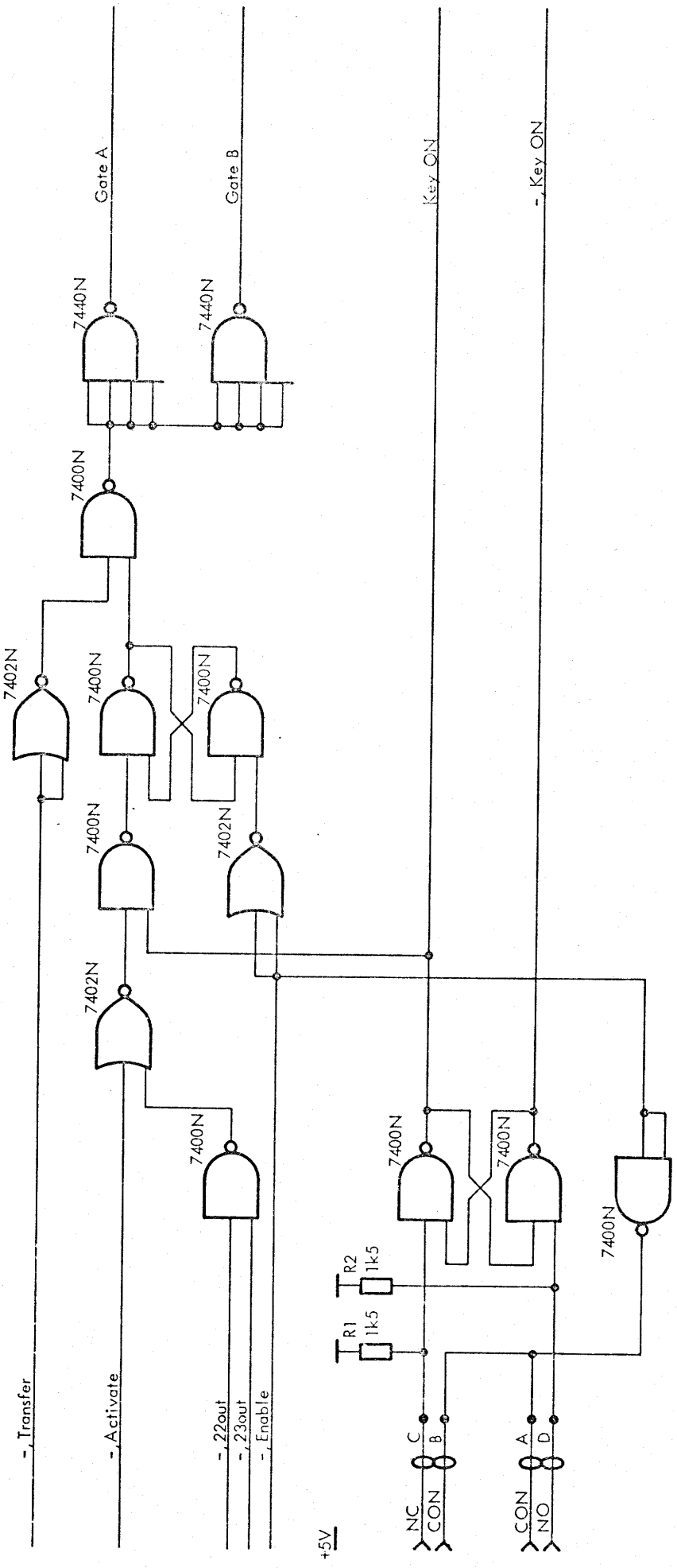
PCBA Circuit Diagram

BCV004



BCV401 Control Signals BCV005

V12068 PCBA Circuit Diagram



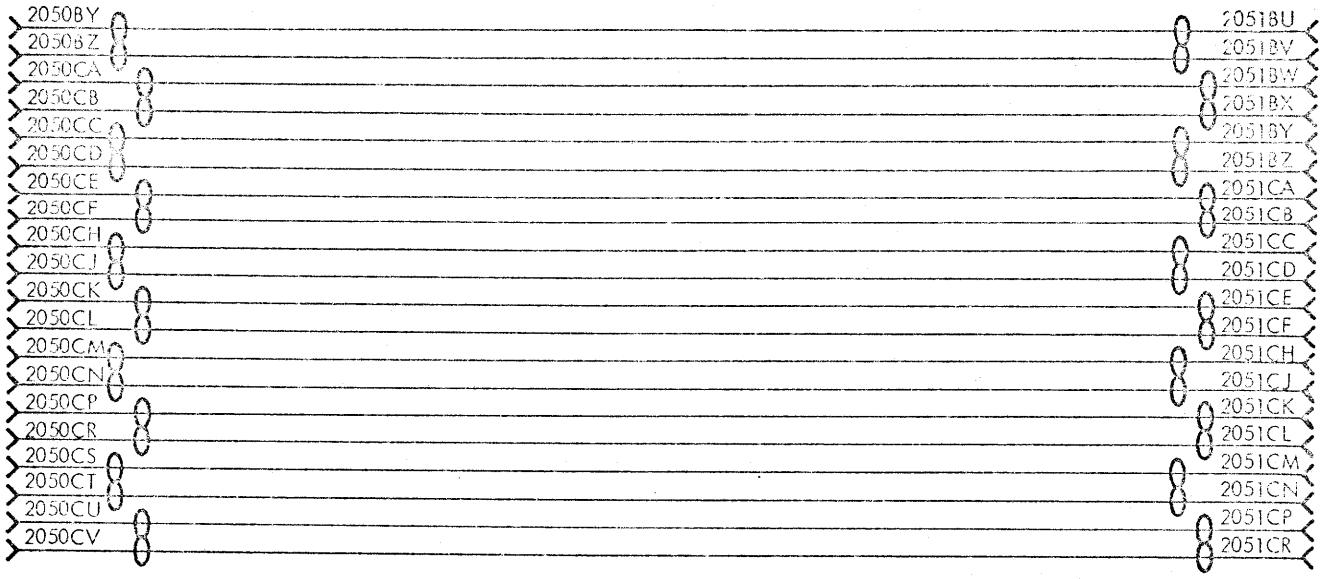
BCV401

V12069

Control Circuit

PCBA Circuit Diagram

BCV006


2050BY
2050BZ
2050CA
2050CB
2050CC
2050CD
2050CE
2050CF
2050CH
2050CJ
2050CK
2050CL
2050CM
2050CN
2050CP
2050CR
2050CS
2050CT
2050CU
2050CV
2051BU
2051BV
2051BW
2051BX
2051BY
2051BZ
2051CA
2051CB
2051CC
2051CD
2051CE
2051CF
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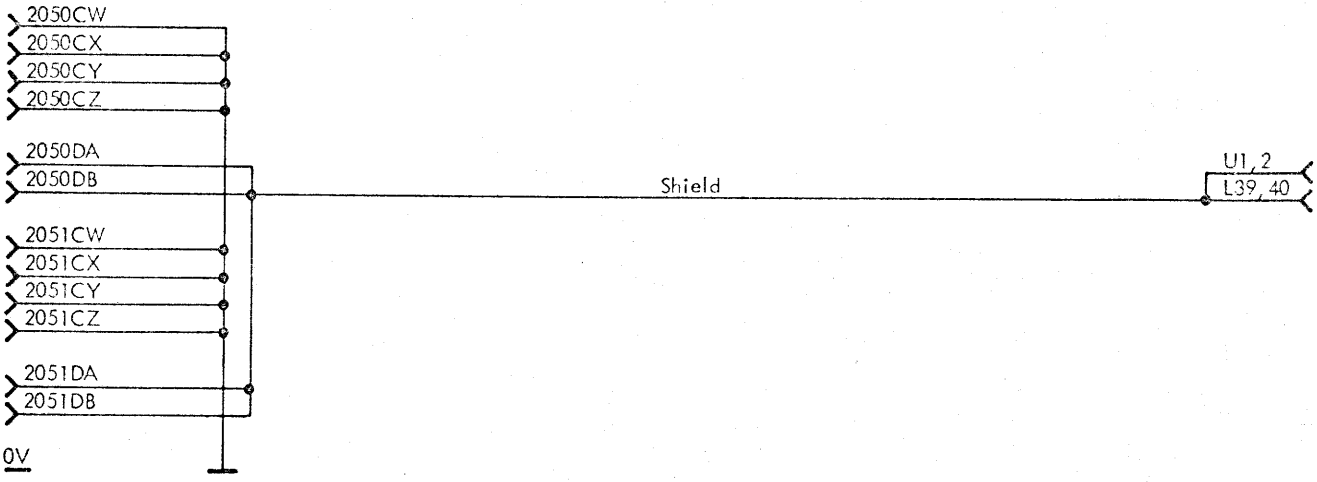
2051CJ
2051CK
2051CL
2051CM
2051CN
2051CP
2051CR


2050CW
2050CX
2050CY
2050CZ
2050DA
2050DB
2051CW
2051CX
2051CY
2051CZ
2051DA
2051DB
0V
Shield
U1, 2
L39, 40

DIGITAL SENSE TERMINALS, DST401 THRU 404

Digital Sense Terminals, DST401 thru 404, are 24-bit, unbuffered digital input units for RC 4000.
These are placed in chassis CHS404 and are connected to the Low-Speed Data Channel via Busline Converter, BCV401.
Data transfer to the W-register takes place by means of a Sense-command as determined by the process program in progress.
If input changes during execution of the Sense-command the data bit in question may be invalid.

Application:	Alarm contact-sensing in industrial process control.

Specifications:

DST401/402:

Selection:	I/O instruction with predetermined device address
Number of Digital Inputs:	24
Type of Input:	2-wire, contact-closure per input. For DST401: closed contact = 1 For DST402: open contact = 1 (referred to W-register)
Max. Cable Resistance: (Closed Contact)	250 ohms per pair
Min. Cable Resistance: (Open Contact)	50 Kohm per pair
Max. Contact Load:	18 V, 6 mA
Type of Contact:	Floating

Dimensions:	Height: 355 mm Width: 24 mm Depth: 450 mm
Supply Power:	+ 5 V ± 5 per cent, 1300 mA + 12 V ± 5 per cent, 110 mA - 6 V ± 5 per cent, 270 mA
Ambient Air:	Temperature: 0 to 45 degrees C Relative Humidity: 30 to 70 per cent
Weight:	1.2 kg

DST403/404:

Selection:	I/O instruction with predetermined device address
Number of Digital Inputs:	24
Type of Input:	2-wire current input from external source. For DST403: 40 mA = 1 For DST404: no current = 1 (referred to W-register)
Input Signal, nominal:	40 mA ± 10 per cent / 0 mA at max. 1.4 V
Input Signal, max.:	50 mA at max. 1.4 V
Input Circuits:	Ga-As light-emitting diodes + phototransistors ensuring galvanic isolation
Dimensions:	Height: 355 mm Width: 24 mm Depth: 450 mm
Supply Power:	+ 5 V ± 5 per cent, 1300 mA + 12 V ± 5 per cent, 110 mA - 6 V ± 5 per cent, 270 mA

DM402

Ambient Air:	Temperature: 0 to 45 degrees C Relative Humidity: 30 to 70 per cent
Weight:	1.2 kg

RCSL: 51-VB488
Author: V. Toft Pedersen
Edited: July 1969

RC 4000 PERIPHERAL DEVICES

DST401, 402, 403 AND 404 DIGITAL SENSE TERMINAL

PRELIMINARY SPECIFICATIONS

ABSTRACT:

This report describes the logic structure of the Digital Sense Terminal, DST401, 402, 403 and 404, when used in connection with the RC 4000 Computer.

A/S REGNECENTRALEN
Falkoneralle 1
Copenhagen F.

Main Characteristics:

The Digital Sense Terminal is designed for collection of 24 static digital inputs from e.g. an industrial process.

The Digital Sense Terminal does not include a buffer register, which means that only a momentary value of the input setting can be transferred.

The Digital Sense Terminal is connected to the RC 4000 via the Low-Speed Data Channel and is addressed as a normal device.

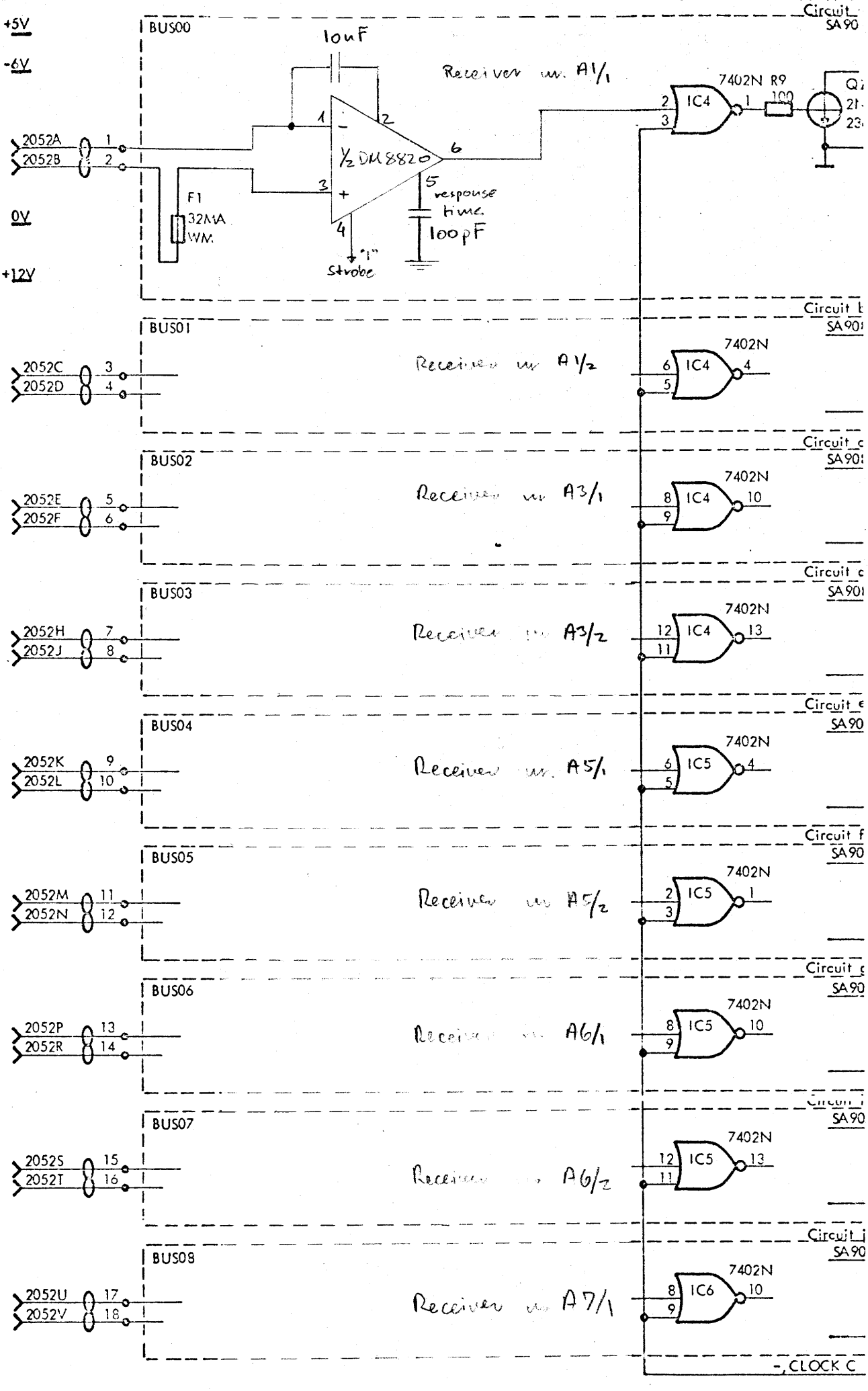
Commands:

The momentary value of the 24 inputs can be transferred to the selected working register by a Sense command.

Modifications of the Sense command will be ignored as well as the commands Read, Write and Control.

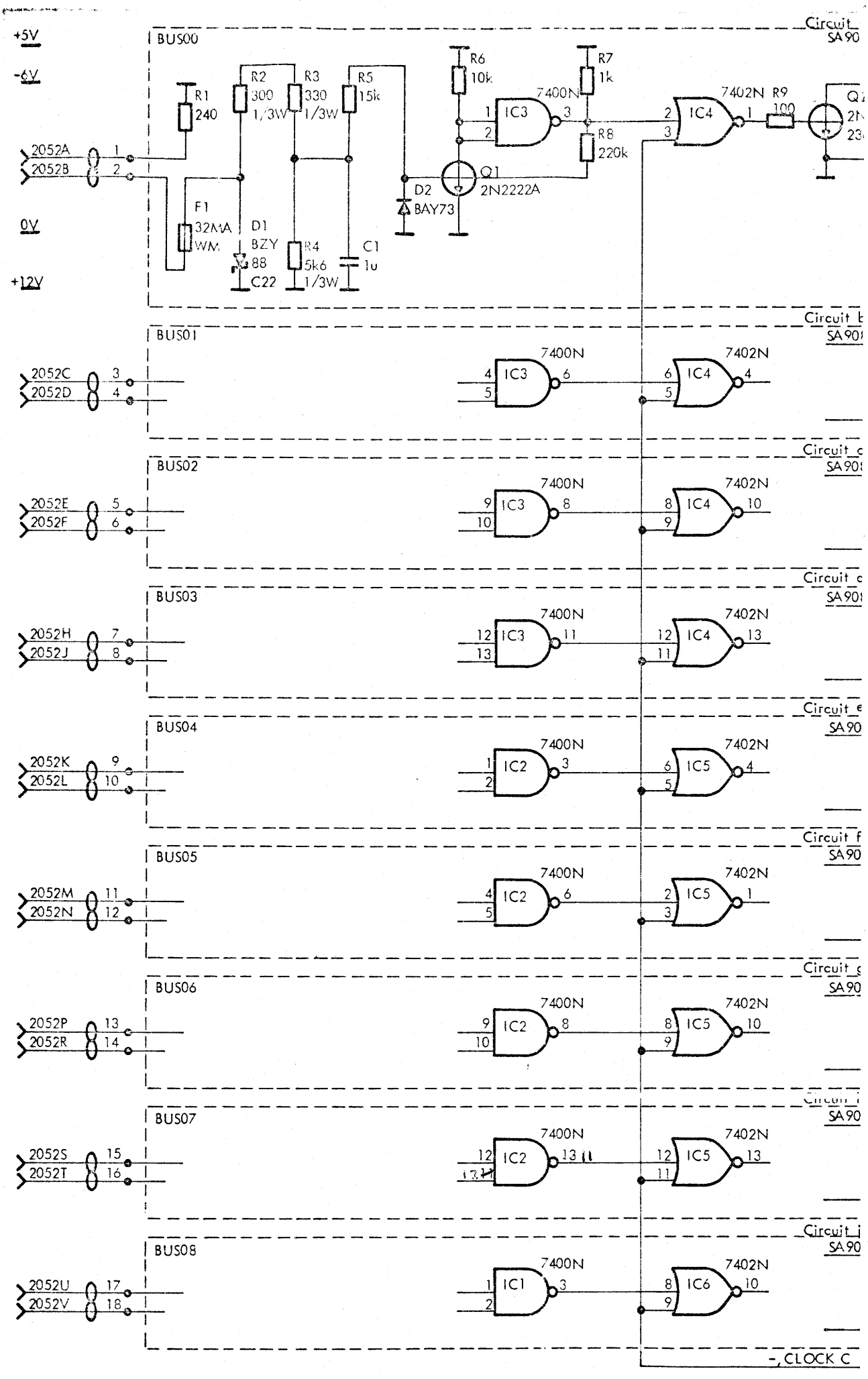
Interrupt:

The Digital Sense Terminal will not generate any interrupt signals.



DST401 (BUS00-08)

V12100 PCBA Circuit Diagram

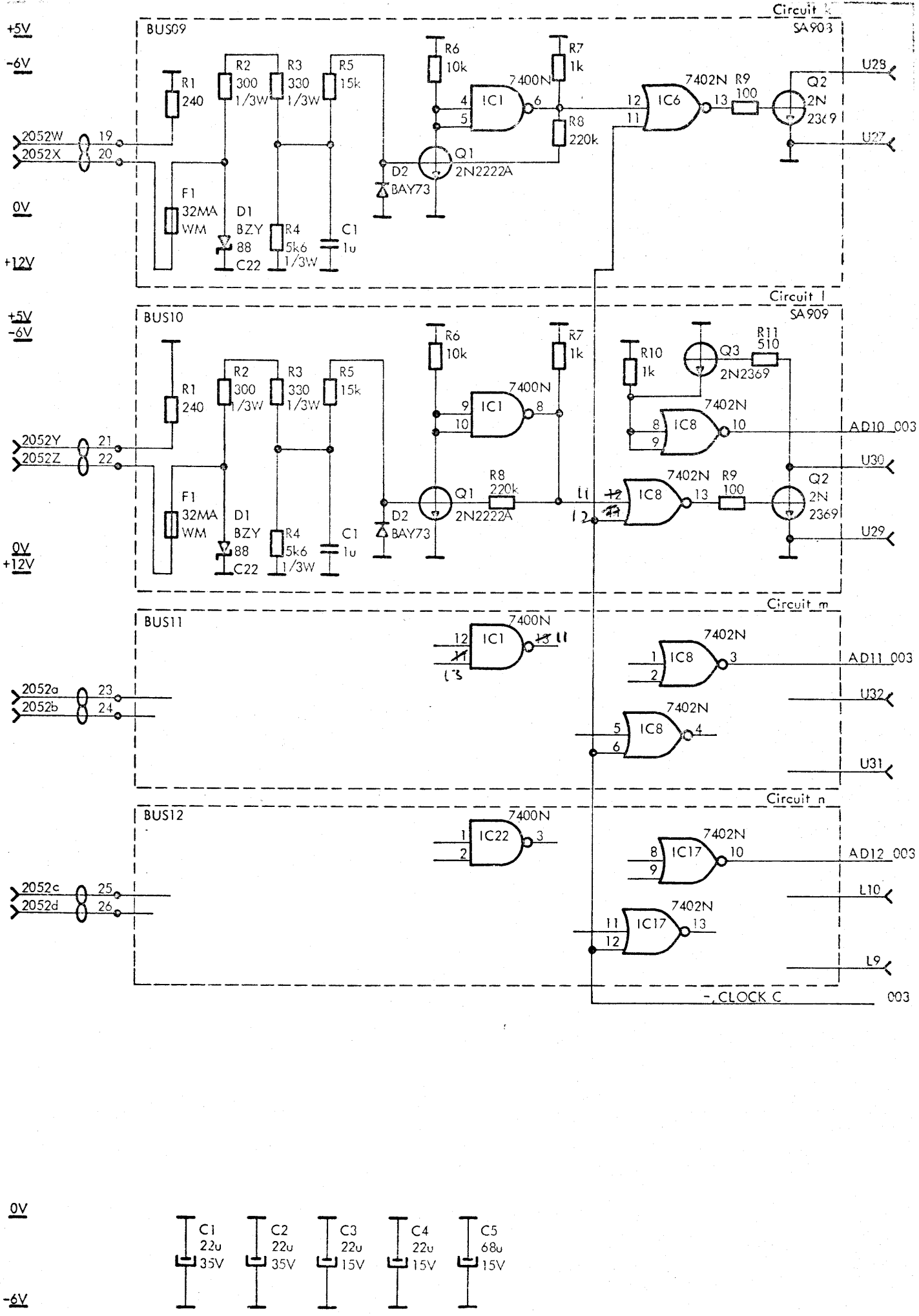


DST401

V12100

(BUS00-08)

PCBA Circuit Diagram



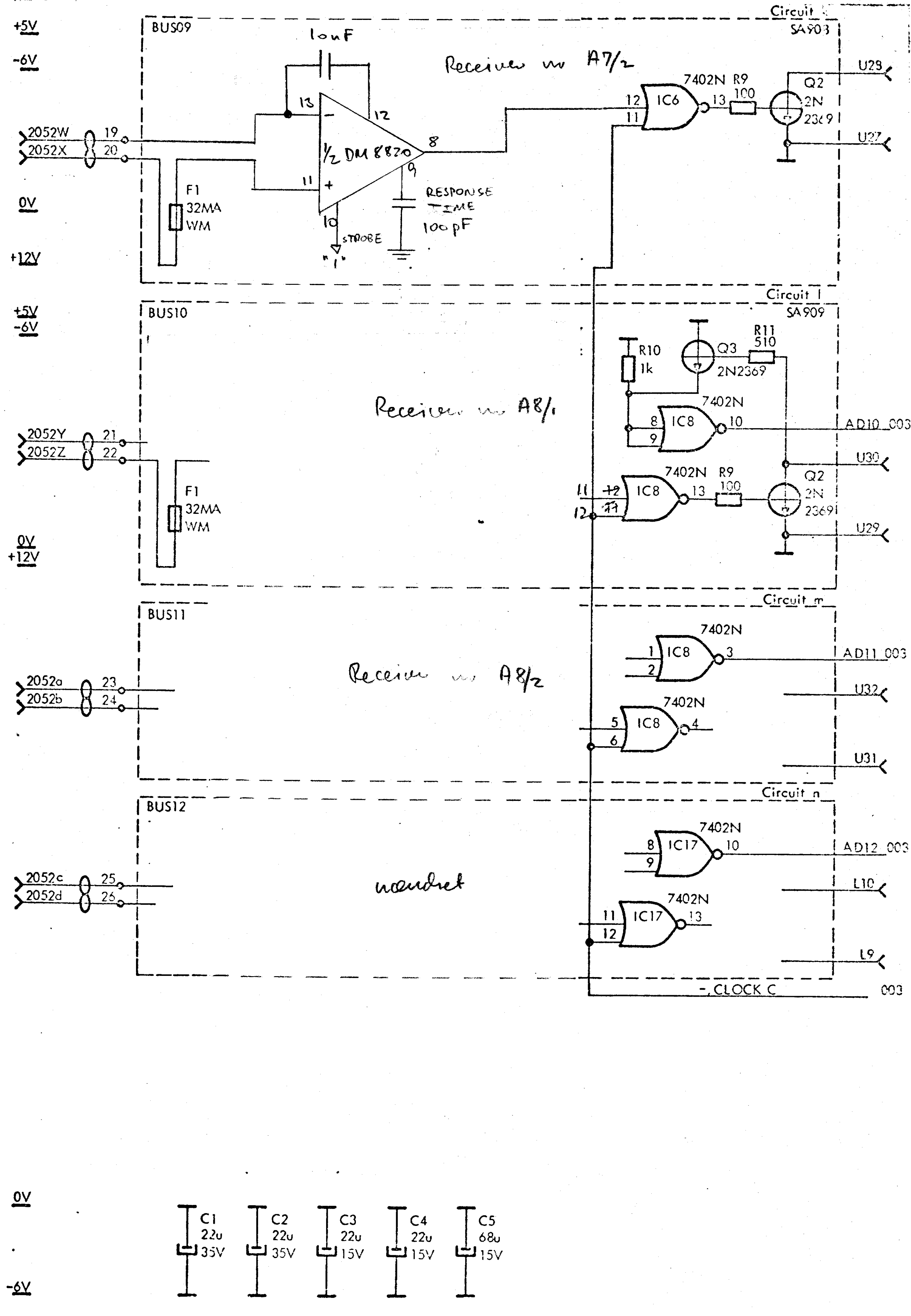
DST401

(BUS09-12)

DST002

V12101

PCBA Circuit Diagram



DST401

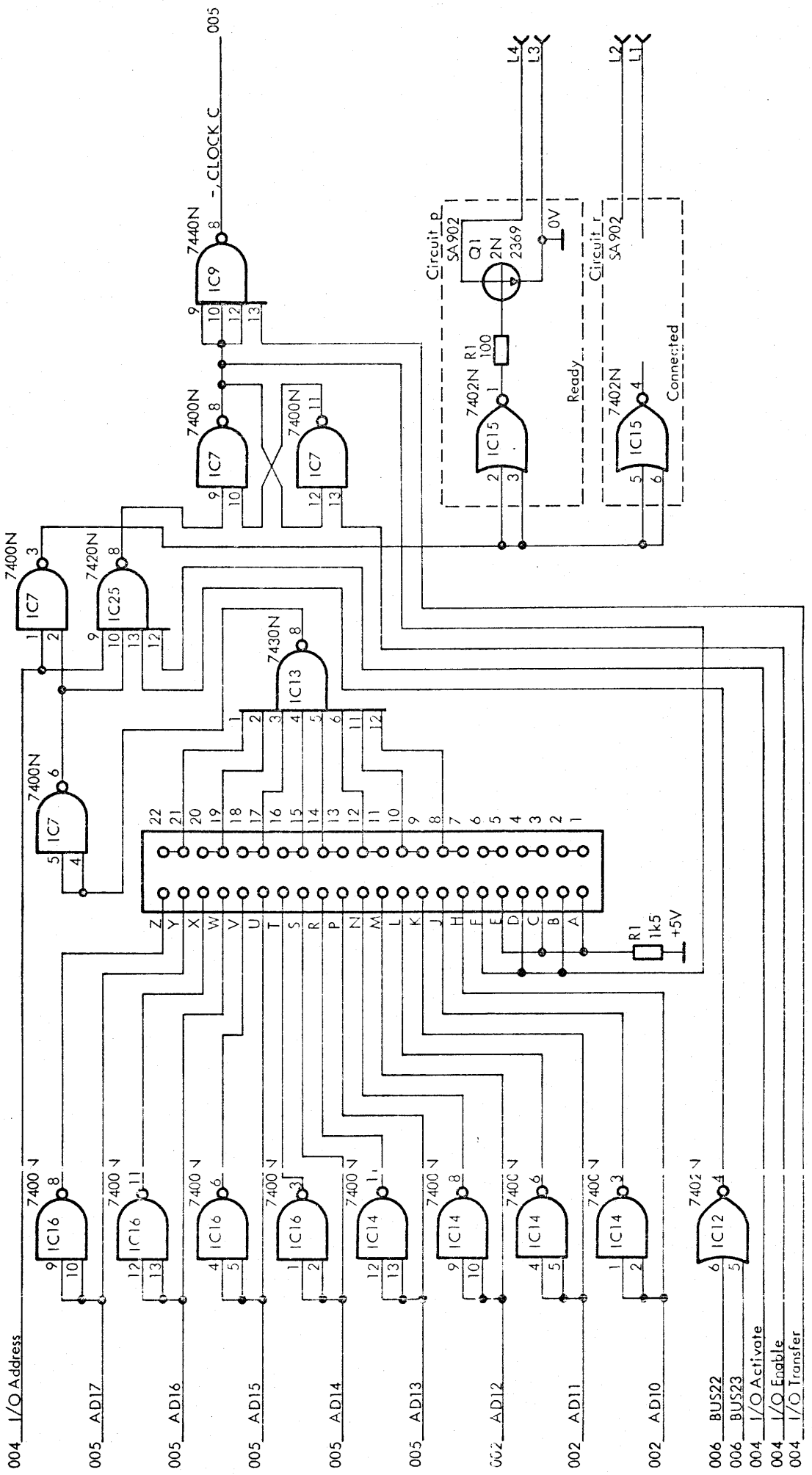
V12101

(BUS09-12)

PCBA Circuit Diagram

DST002

ELCO con.			kreds/ben	Lus nr = PCB no.	Receiver	output ben
A	rød	inut	3/3	1	A1/1	6
B	bla°	u.md.				
C	rød					
D	bla°		3/6	2	A1/2	8
E	rød					
F	bla°		3/8	3	A3/1	6
H	rød					
J	bla°		3/11	4	A3/2	8
k	rød					
L	bla°		2/3	5	A5/1	6
M	rød					
N	bla°		2/6	6	A5/2	8
P	rød					
R	bla°		2/8	7	A6/1	6
S	rød					
T	bla°		2/11	8	A6/2	8
U	rød					
V	bla°		1/3	9	A7/1	6
W	rød					
X	bla°		1/6	10	A7/2	8
Y	rød					
Z	bla°		1/8	11	A8/1	6
a	rød					
b	bla°		1/11	12	A8/2	8



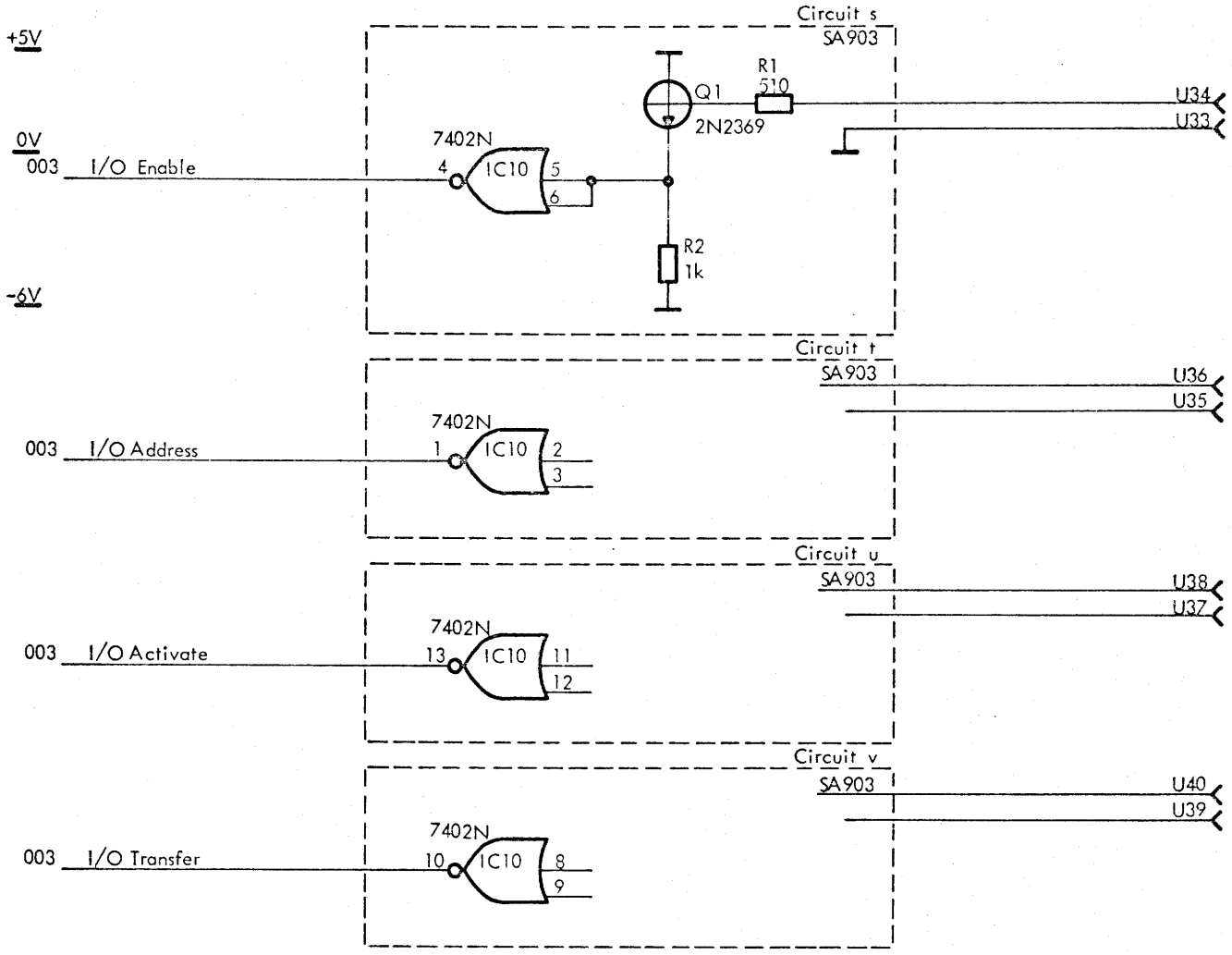
DST401

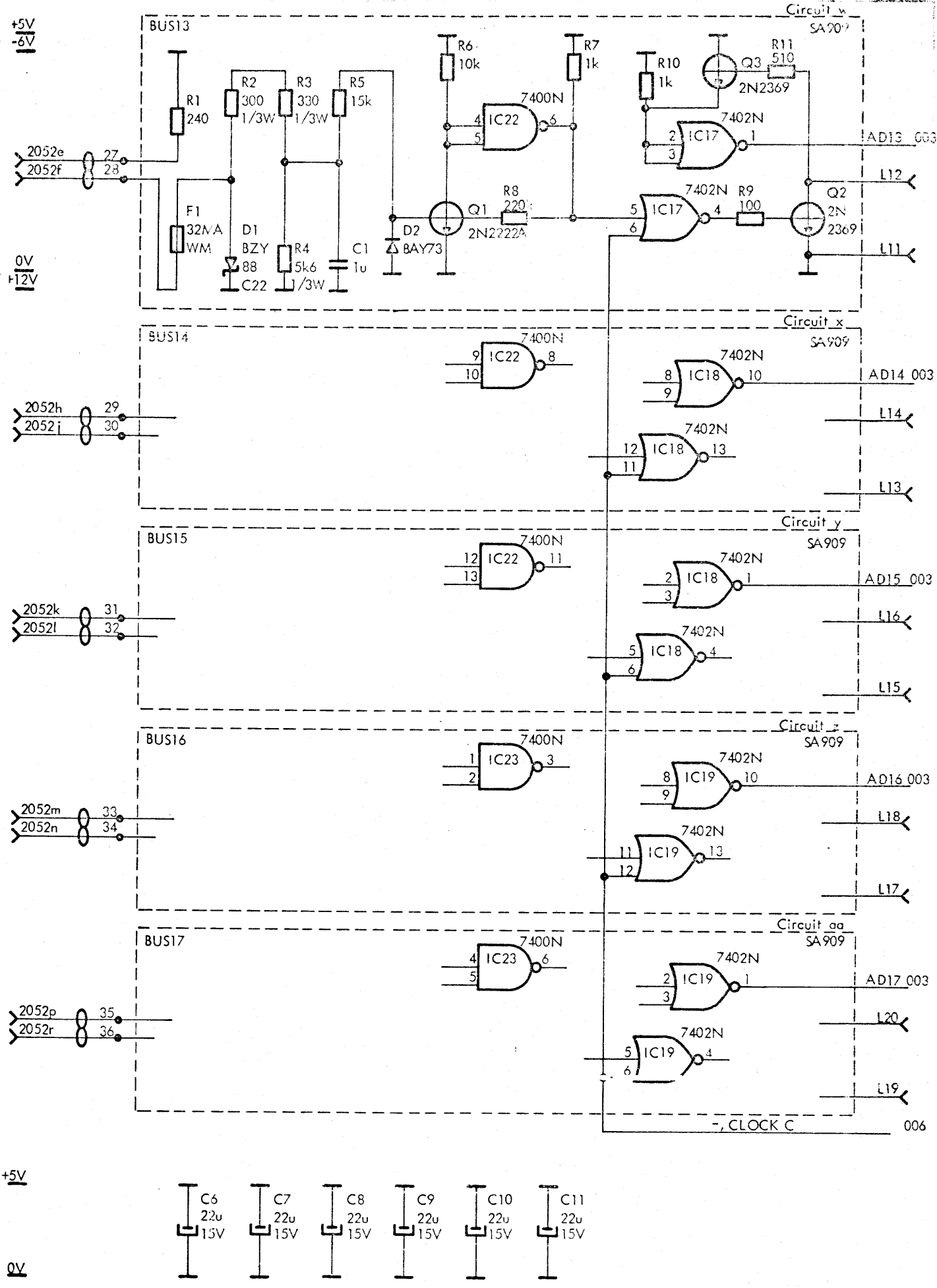
Address Decoding

DST003

V12102

PCBA Circuit Diagram


Circuit s
SA903
+5V
0V
003 I/O Enable
-6V
7402N
4
IC10
5
6
Q1
2N2369
R1
510
R2
1k
U34
U33
Circuit t
SA903
003 I/O Address
7402N
1
IC10
2
3
U36
U35
Circuit u
SA903
003 I/O Activate
7402N
13
IC10
11
12
U38
U37
Circuit v
SA903
003 I/O Transfer
7402N
10
IC10
8
9
U40
U39



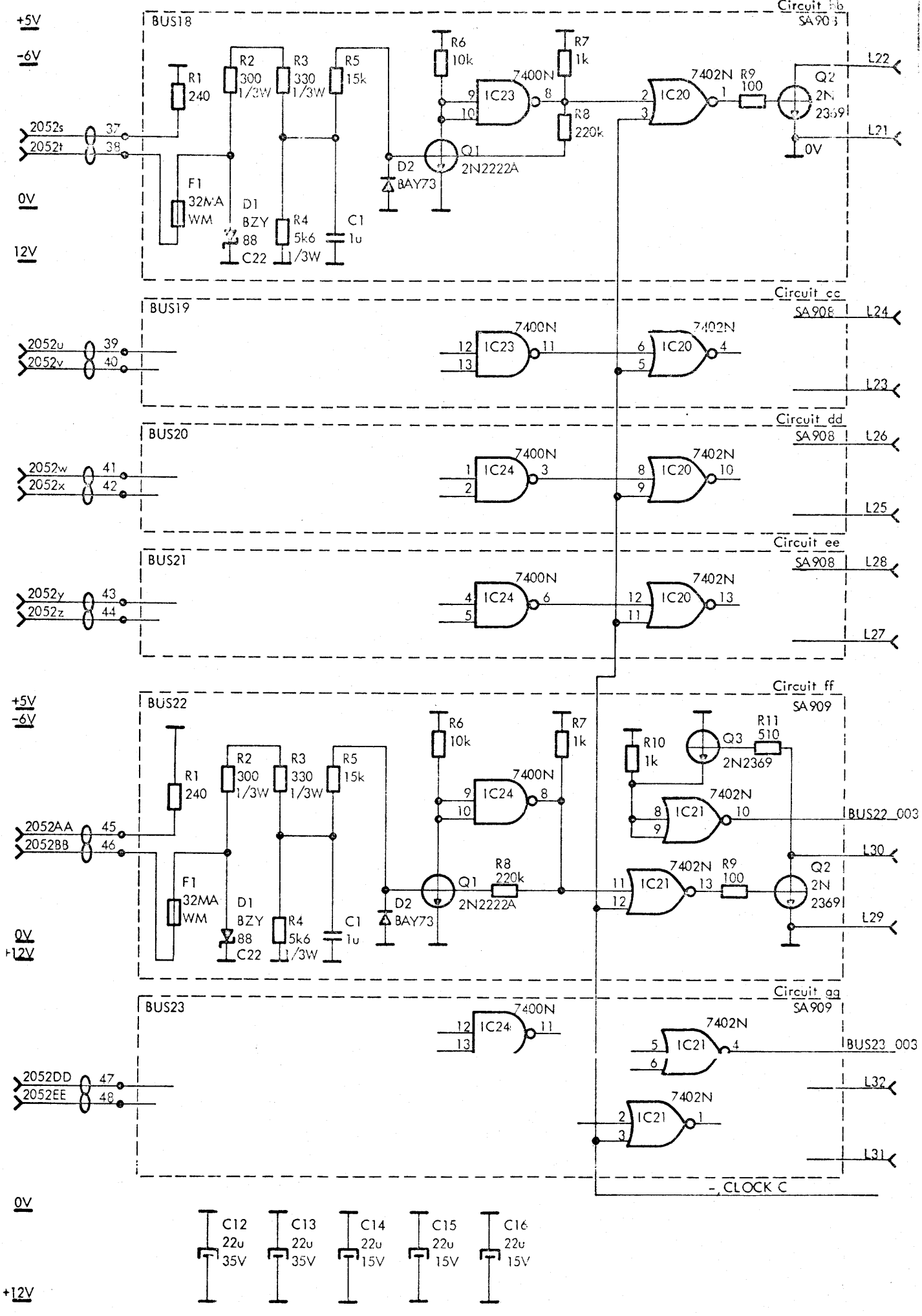
DST401

(BUS13-17)

DST005

V12104

PCBA Circuit Diagram



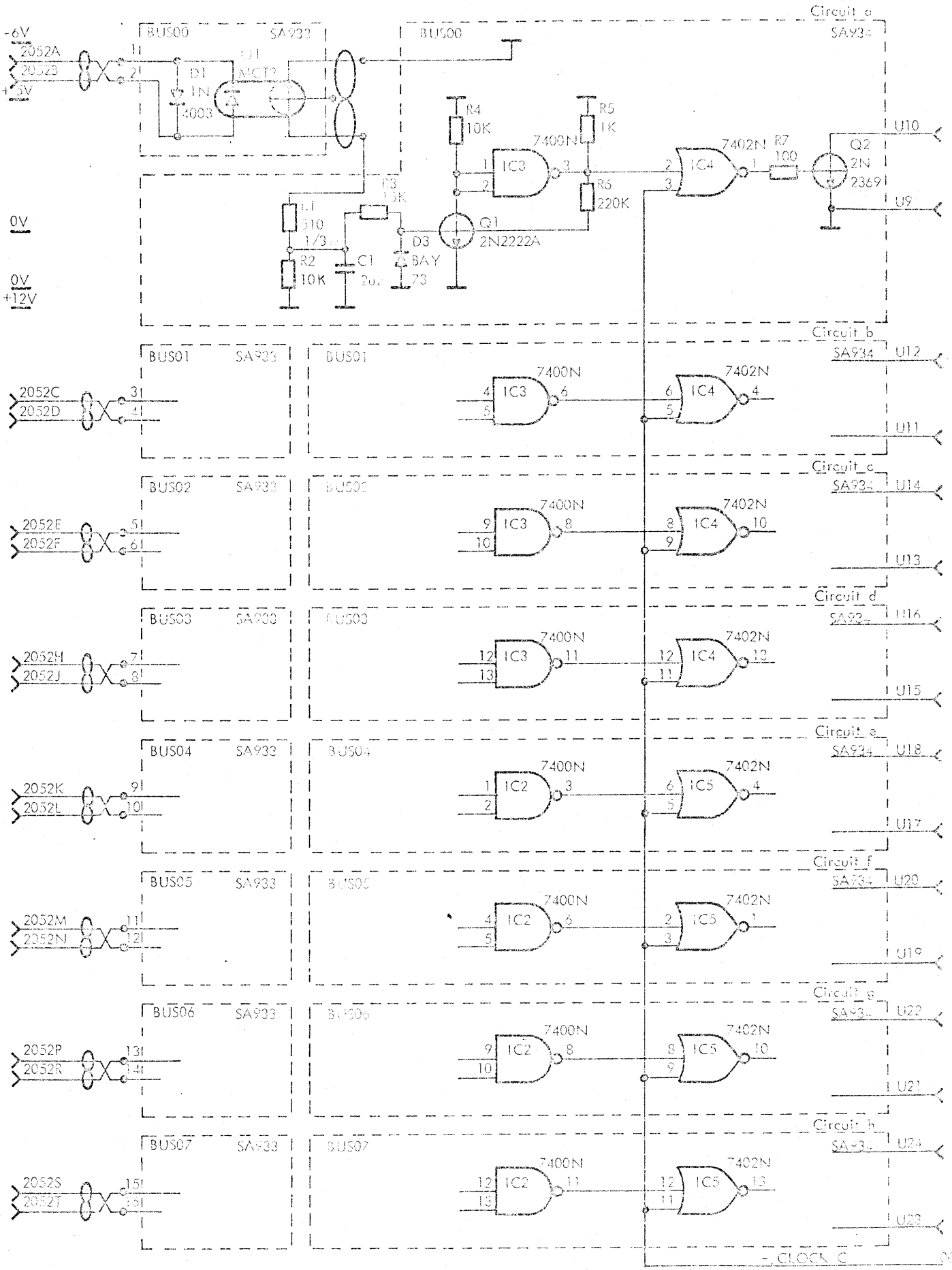
DST401

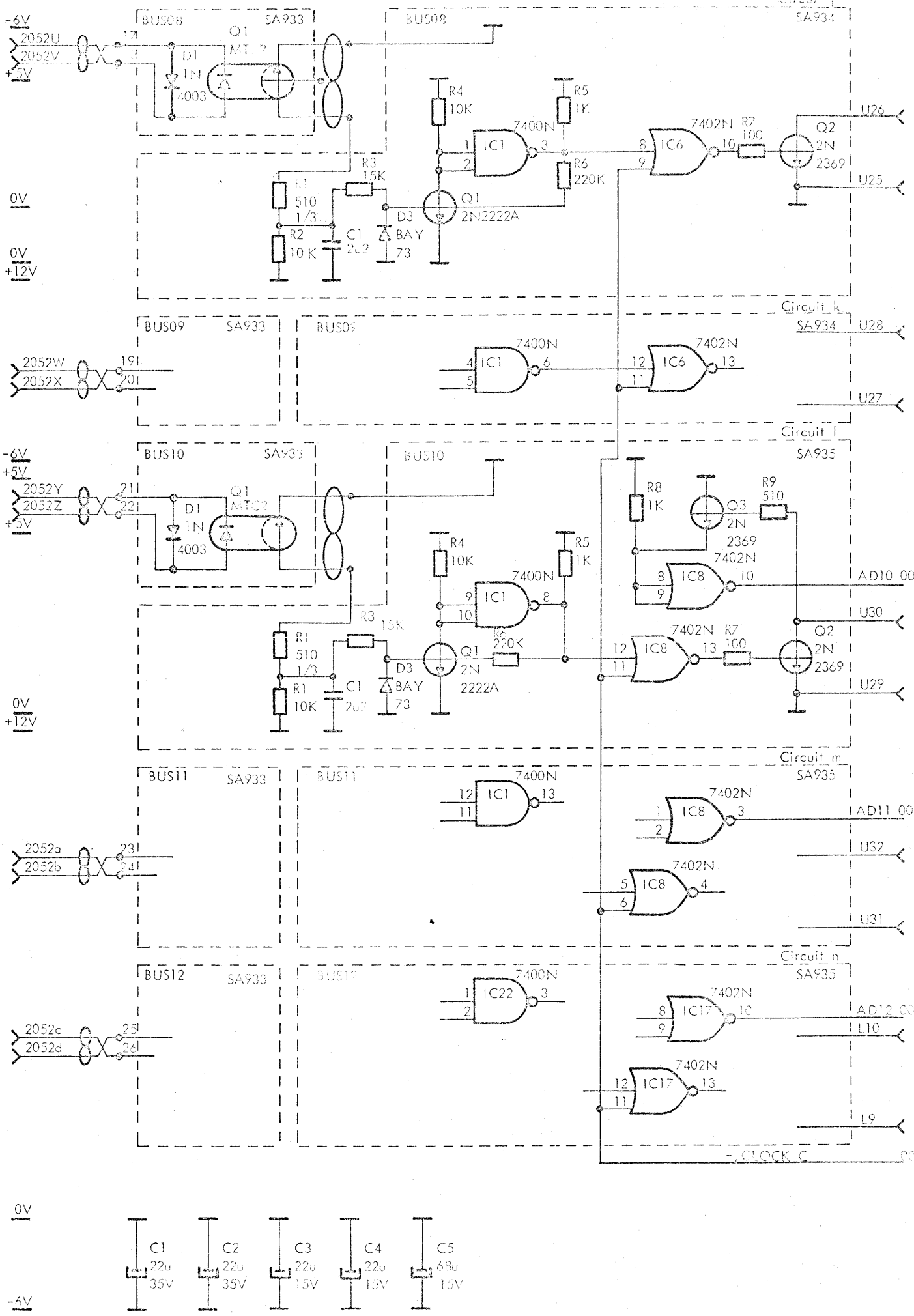
V12105

(BUS18-23)

PCBA Circuit Diagram

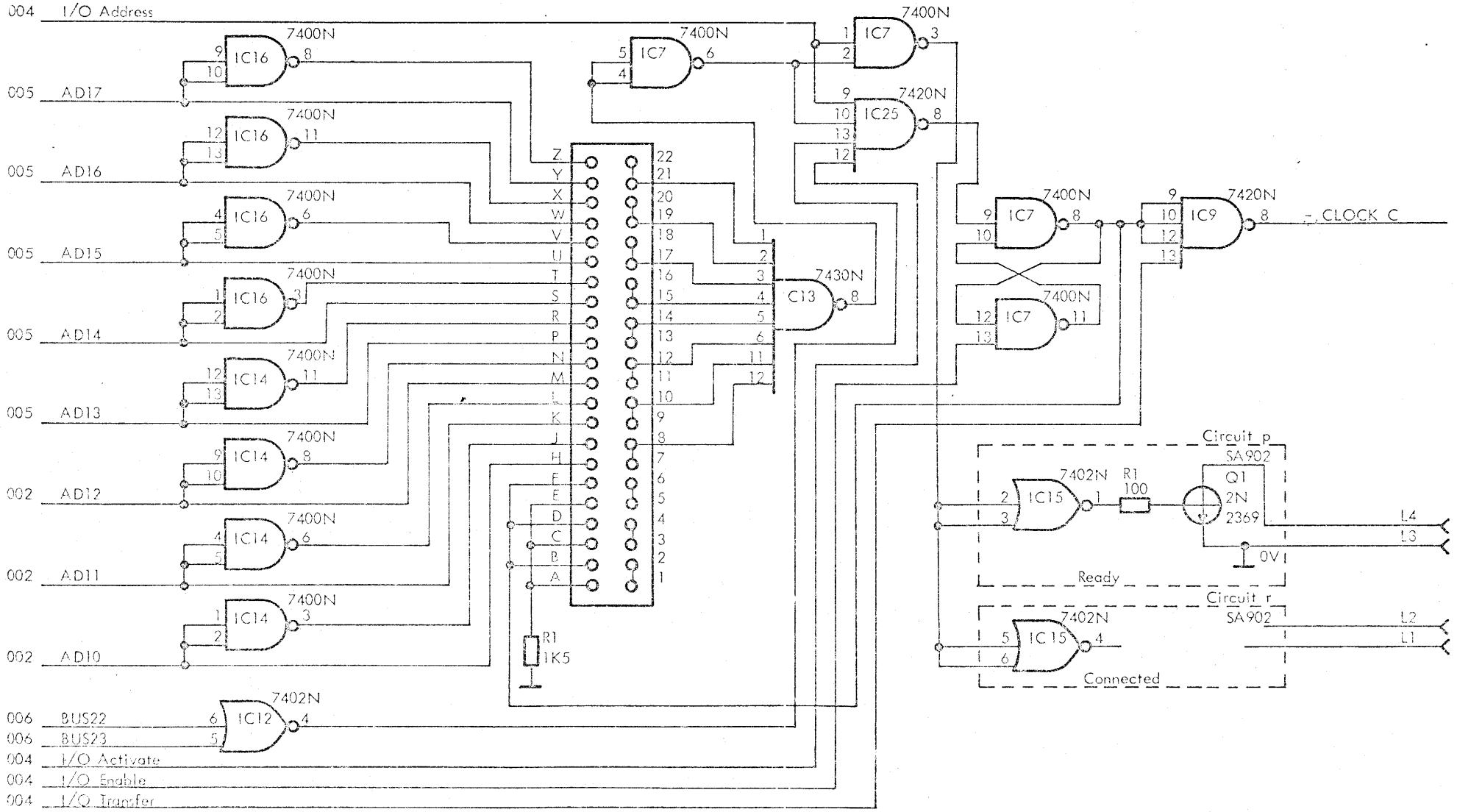
DST006

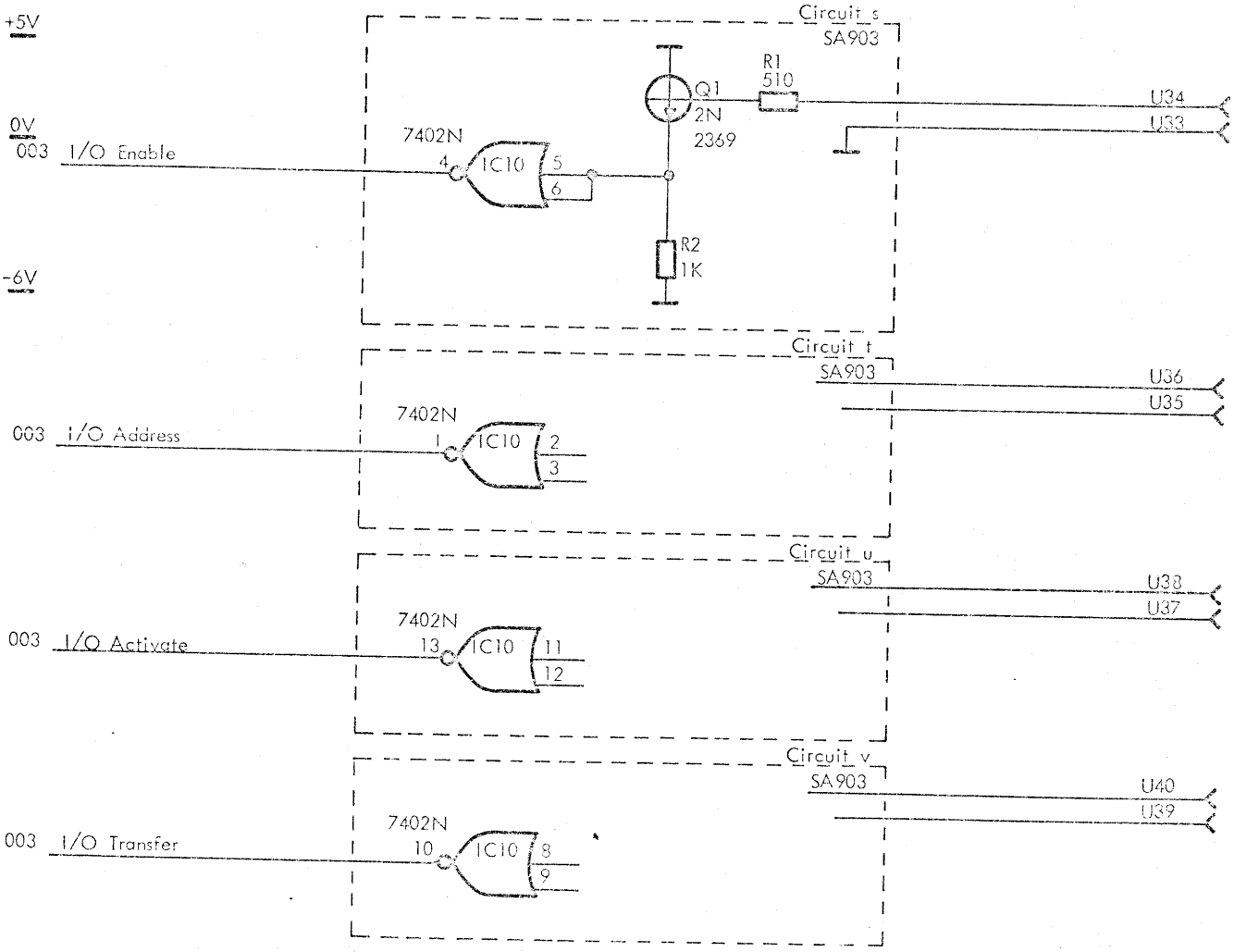

Circuit_a
SA934
BUS00
SA933
-6V
2052A
2052B
+5V
D1
IN
4003
D2
MCT2
R4
10K
R5
1K
7400N
IC3
7402N
IC4
R7
100
Q2
2N
2369
U10
U9
R6
220K
R3
15K
R1
510
1/3W
R2
10K
C1
20n
D3
BAY
73
Q1
2N2222A
0V
0V
+12V
Circuit_b
SA934
U12
U11
BUS01
SA933
2052C
2052D
Circuit_c
SA934
U14
U13
BUS02
SA933
2052E
2052F
Circuit_d
SA934
U16
U15
BUS03
SA933
2052H
2052J
Circuit_e
SA934
U18
U17
BUS04
SA933
2052K
2052L
IC2
IC5
Circuit_f
SA934
U20
U19
BUS05
SA933
2052M
2052N
Circuit_g
SA934
U22
U21
BUS06
SA933
2052P
2052R
Circuit_h
SA934
U24
U23
BUS07
SA933
2052S
2052T
CLOCK_C
1003744552 160374 ~ Rel. V12708
020271PAJ
200569LPH



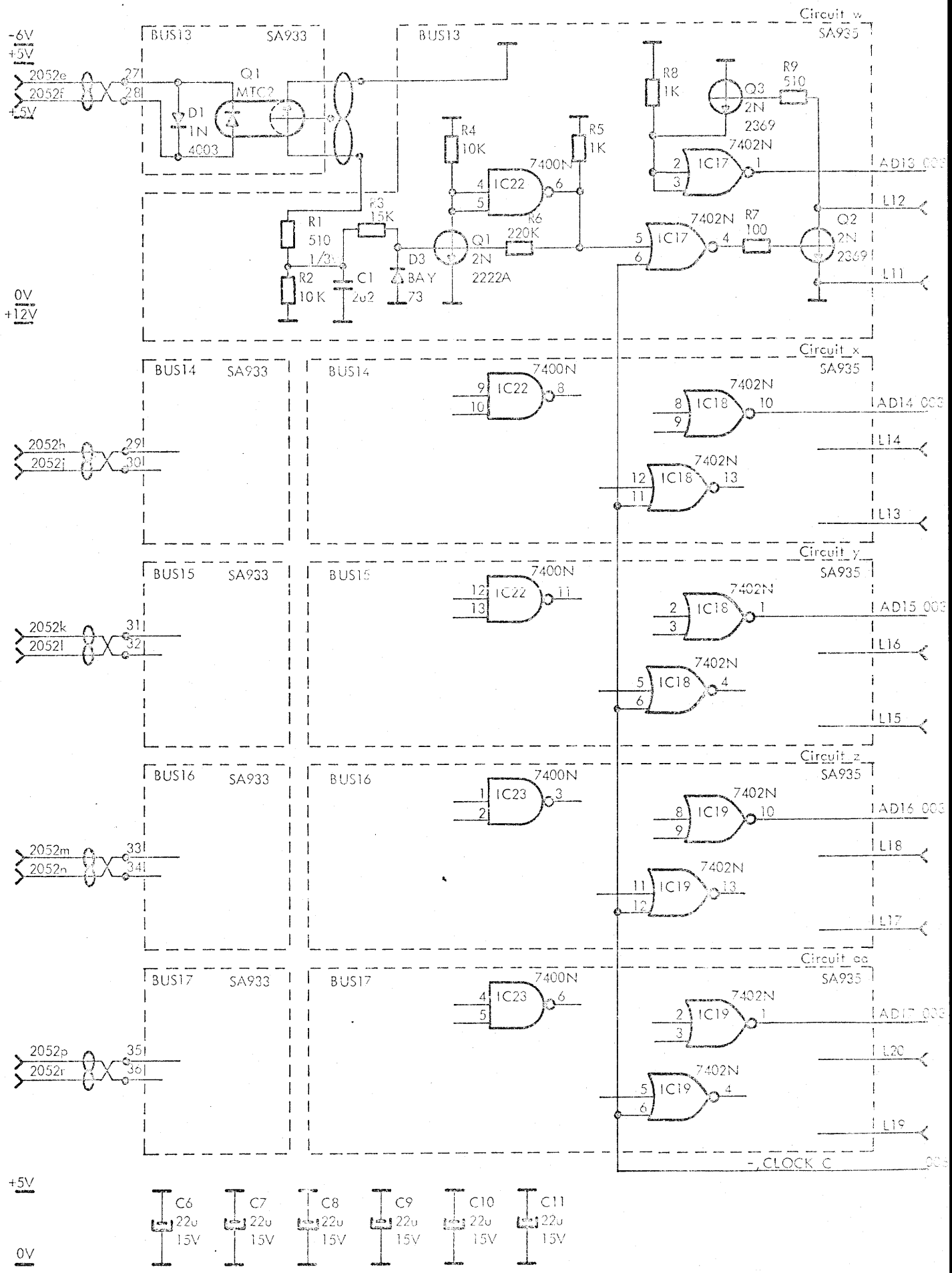
DST 403 (BUS08-12) DST002

V12871 PCBA Circuit Diagram


004 I/O Address
005 AD17
005 AD16
005 AD15
005 AD14
005 AD13
002 AD12
002 AD11
002 AD10
006 BUS22
006 BUS23
004 I/O Activate
004 I/O Enable
004 I/O Transfer
7400N
7420N
7430N
7402N
IC16
IC14
IC12
IC7
IC25
C13
IC9
IC15
R1
1K5
100
Q1
2N
2369
SA902
Circuit p
Circuit r
Ready
Connected
0V
CLOCK C
L4
L3
L2
L1

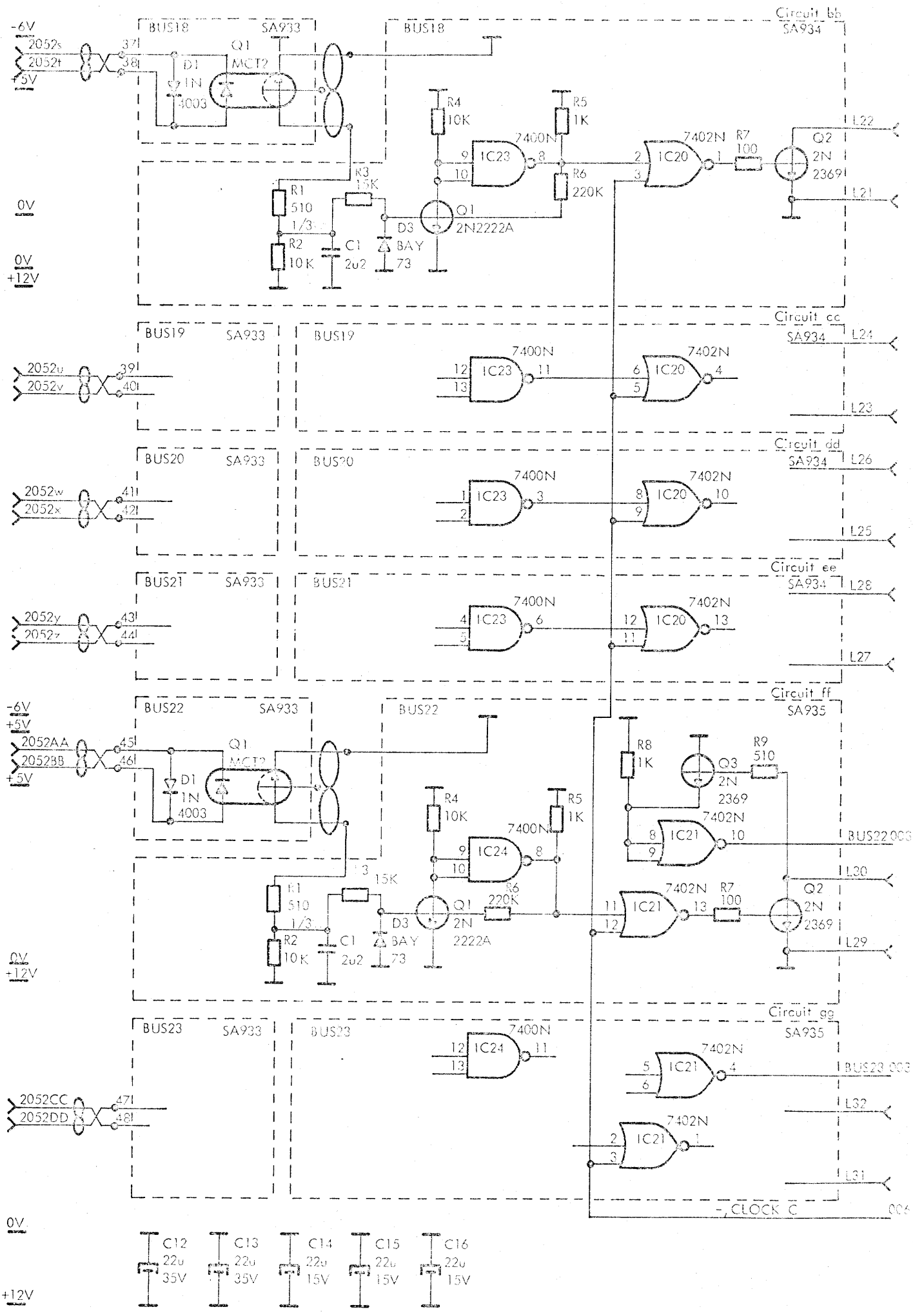


200569LPH 020271PAJ 100277-452 260371-02 Pol



DST 403 (BUS13-17) DST005

V12868 PCBA Circuit Diagram



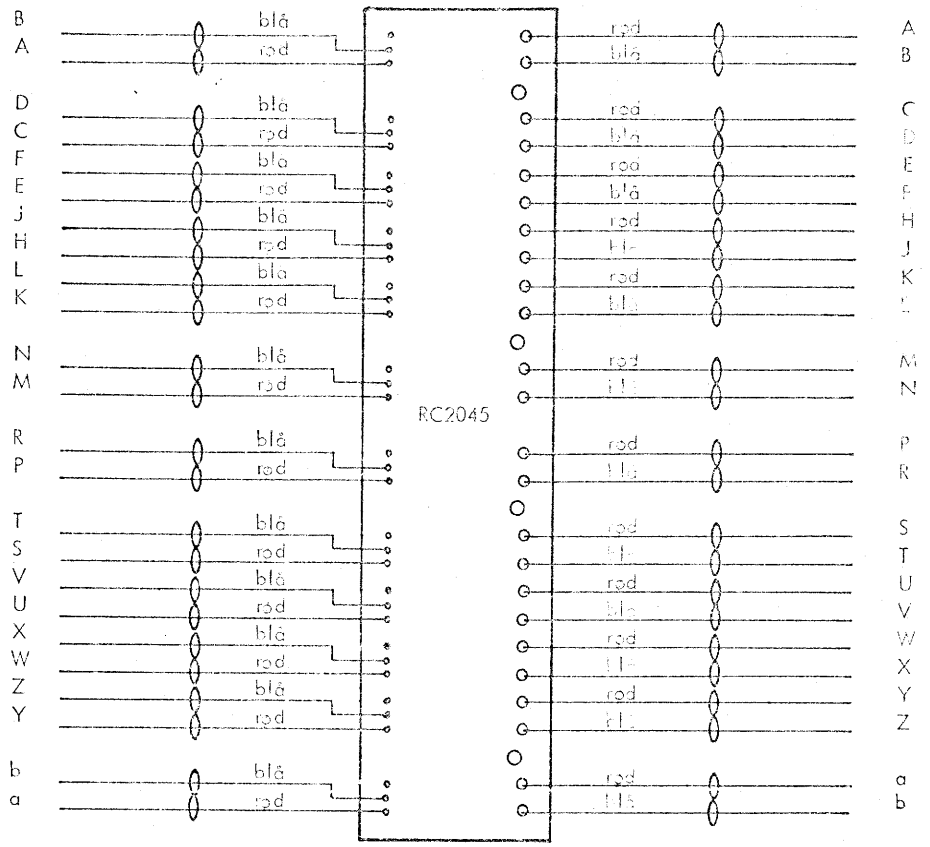
DST 403

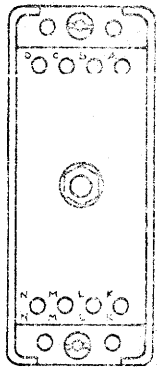
(BUS18-23)

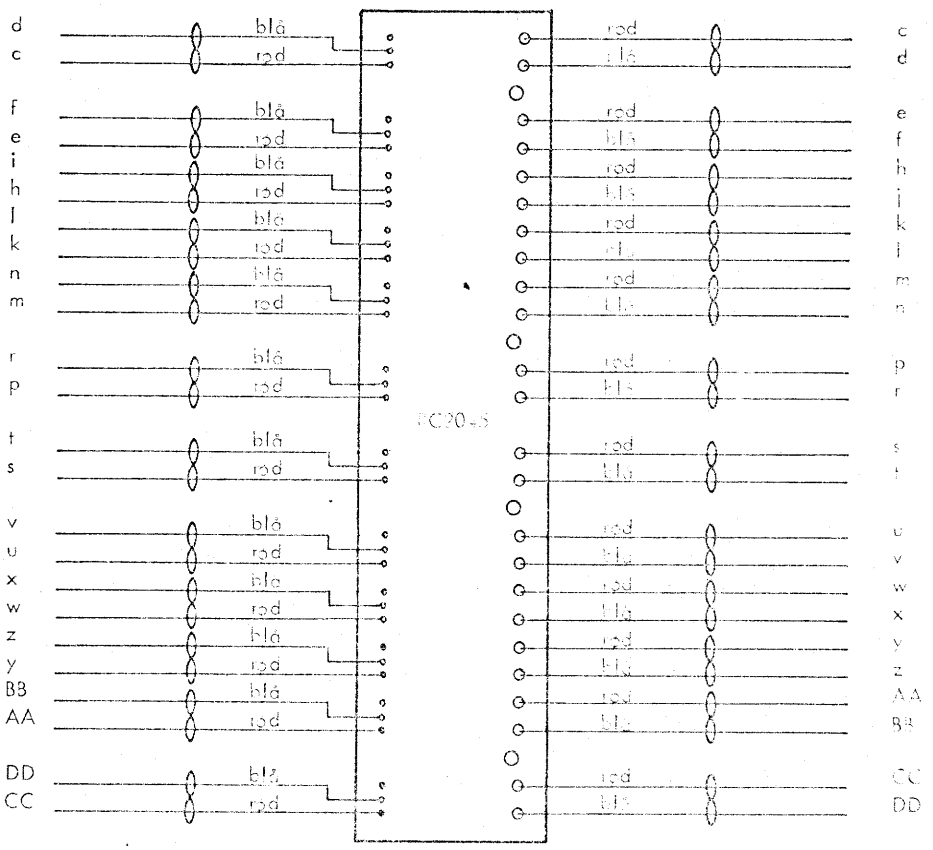
DST006

V12869

PCBA Circuit Diagram







Printpladens loddeside er vist på tegning.

090172 HOKM

031271 FLC

INTERRUPT EXPANDER IXP401 THRU 404

Interrupt expander IXP401 thru 404 are 24-channel buffered digital input units which are equipped with a logical output to be connected either to one of the interrupt-level inputs of RC 4000 or to one of the inputs of Interrupt Expander IXP406.
The interrupt-output change states if an input pulse is applied to one or more of the 24 inputs.
All interrupt expander types can be placed in chassis CHS404 and are connected to the Low-Speed Data Channel via Busline Converter BCV401.
Similar to the PIT401 thru 404 data transfer of the contents of the 24-bit buffer register to the W-register takes place by means of a Sense command as determined by the program in progress (e.g. an interrupt response program).
When a transfer has been executed the buffer register and the interrupt-output as well is cleared.

Application: High priority alarm contact input, keyboard input, or low-speed counting in industrial process control.

Specifications:

IXP401/402:

Selection:	I/O instruction with predetermined device address
Number of Inputs:	24
Type of Input:	2-wire contactclosure per input For IXP401: closed contact = 1 For IXP402: open contact = 1 (referred to W-register)

Max. Cable Resistance (closed contact):	250 ohm per pair
Min. Cable Resistance (open contact):	50 Kohm per pair
Max. Contact Load:	18 V, 5 mA
Type of Contact:	Floating
Minimum Pulse Duration:	20 ms (open contact) 10 ms (closed contact)
Number of Outputs:	1 interrupt output
Type of Output (Interrupt):	TTL logic levels
Dimensions:	Height: 355 mm Width: 24 mm Depth: 450 mm
Supply Power:	+ 5 V ± 5 per cent, 1300 mA +12 V ± 5 per cent, 110 mA - 6 V ± 5 per cent, 270 mA
Ambient Air:	Temperature: 0 to 45 degrees C Relative Humidity: 30 to 70 per cent
Weight:	1.2 kg

IXP403/404:

Selection:	I/O instruction with predetermined device address
Number of Inputs:	24

Type of Input:	2-wire current input from external source, For IXP403: 40 mA = 1 For IXP404: no current = 1 (referred to W-register)
Input Signal, nominal:	40 mA ± 10 per cent / 0 mA at max. 1.4 V
Input Signal, max.:	50 mA at max. 1.4 V
Input Circuits:	Ga-As light-emitting diodes + phototransistor ensuring galvanic isolation
Minimum Input Pulse Duration:	25 us (between 90 per cent points)
Minimum Input Pulse Spacing:	35 us (between 10 per cent points)
Number of Outputs:	1 interrupt output
Type of Output (Interrupt):	TTL logic levels
Dimensions:	Height: 355 mm Width: 24 mm Depth: 450 mm
Supply Power:	+ 5 V ± 5 per cent, 1300 mA +12 V ± 5 per cent, 110 mA - 6 V ± 5 per cent, 270 mA
Ambient Air:	Temperature: 0 to 45 degrees C Relative Humidity: 30 to 70 per cent
Weight:	1.2 kg

RCSL: 51-VB461
Author: M. Strange
Edited: July 1969

RC 4000 PERIPHERAL DEVICES

IXP401, 402, 403 AND 404 INTERRUPT EXPANDER

PRELIMINARY SPECIFICATIONS

ABSTRACT:

This report describes the logic structure of the Interrupt Expander IXP401, 402, 403 and 404, when used in connection with the RC 4000 Computer.

A/S REGNECENTRALEN
Falkoneralle 1
Copenhagen F.

Main Characteristics:

The Interrupt Expander is designed to attach 24 external interrupt signals to a single interrupt level, i. e. a single bit of the interrupt register (IR), of the RC 4000.

The Interrupt Expander includes a 24 bits buffer for collection of 24 interrupt signals. If one or more of these signals change to 1 a single common interrupt signal will be generated to activate one of the interrupt levels of the RC 4000.

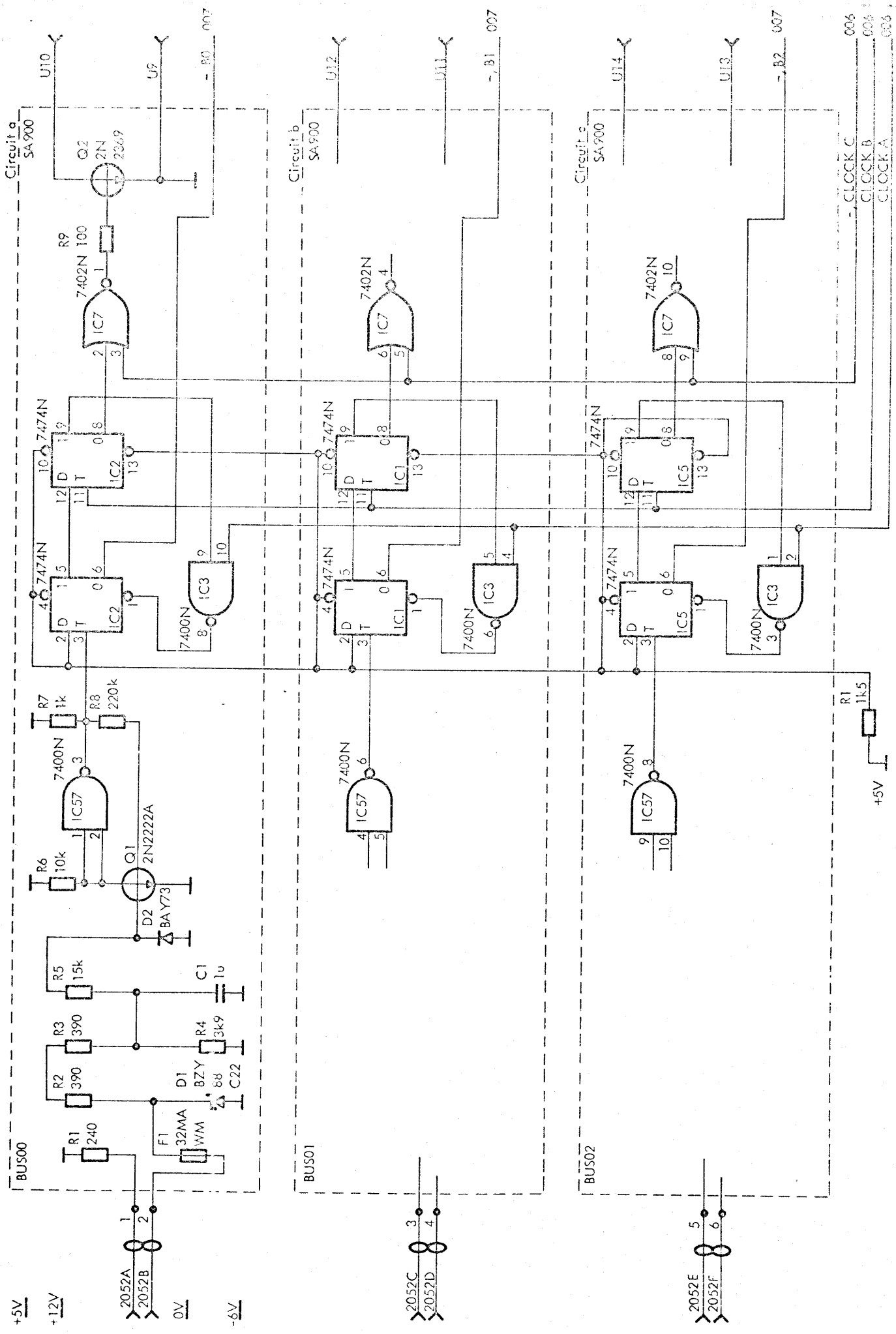
The Interrupt Expander is connected to the RC 4000 via the Low-Speed DATA Channel and is addressed as a normal device.

Commands:

The contents of the Interrupt Expander buffer register can be transferred to the selected working register by a Sense command. After this transfer the buffer register is cleared. Modifications of the Sense command will be ignored as well as the commands Read, Write and Control.

Interrupt:

The Interrupt Expander generates an interrupt signal when at least one bit of the buffer register contains of 1. Between 2 Sense commands only one interrupt signal is transferred to the interrupt register (IR) of the RC 4000, even if several external interrupt signals are collected in the buffer register.



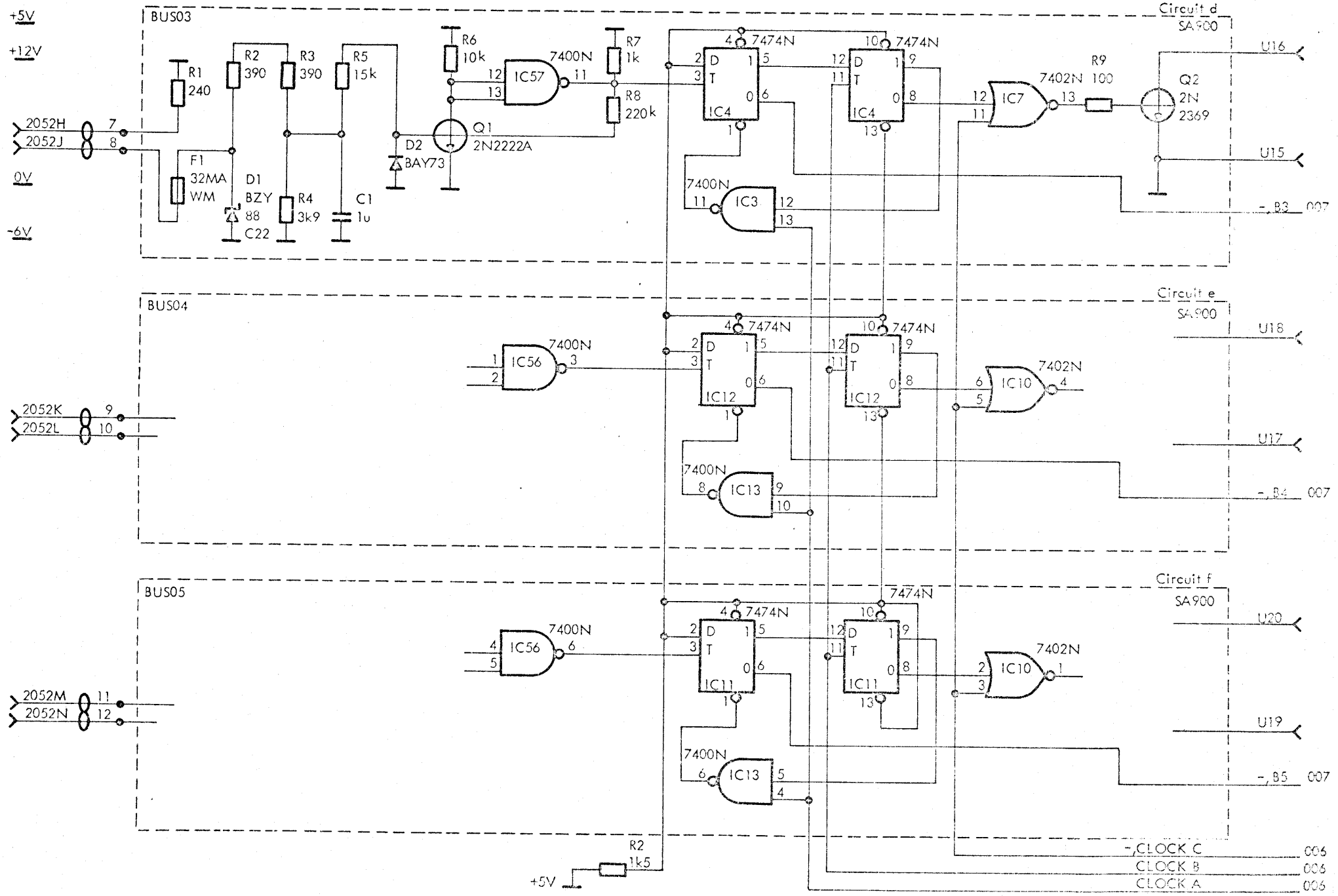
IXP401

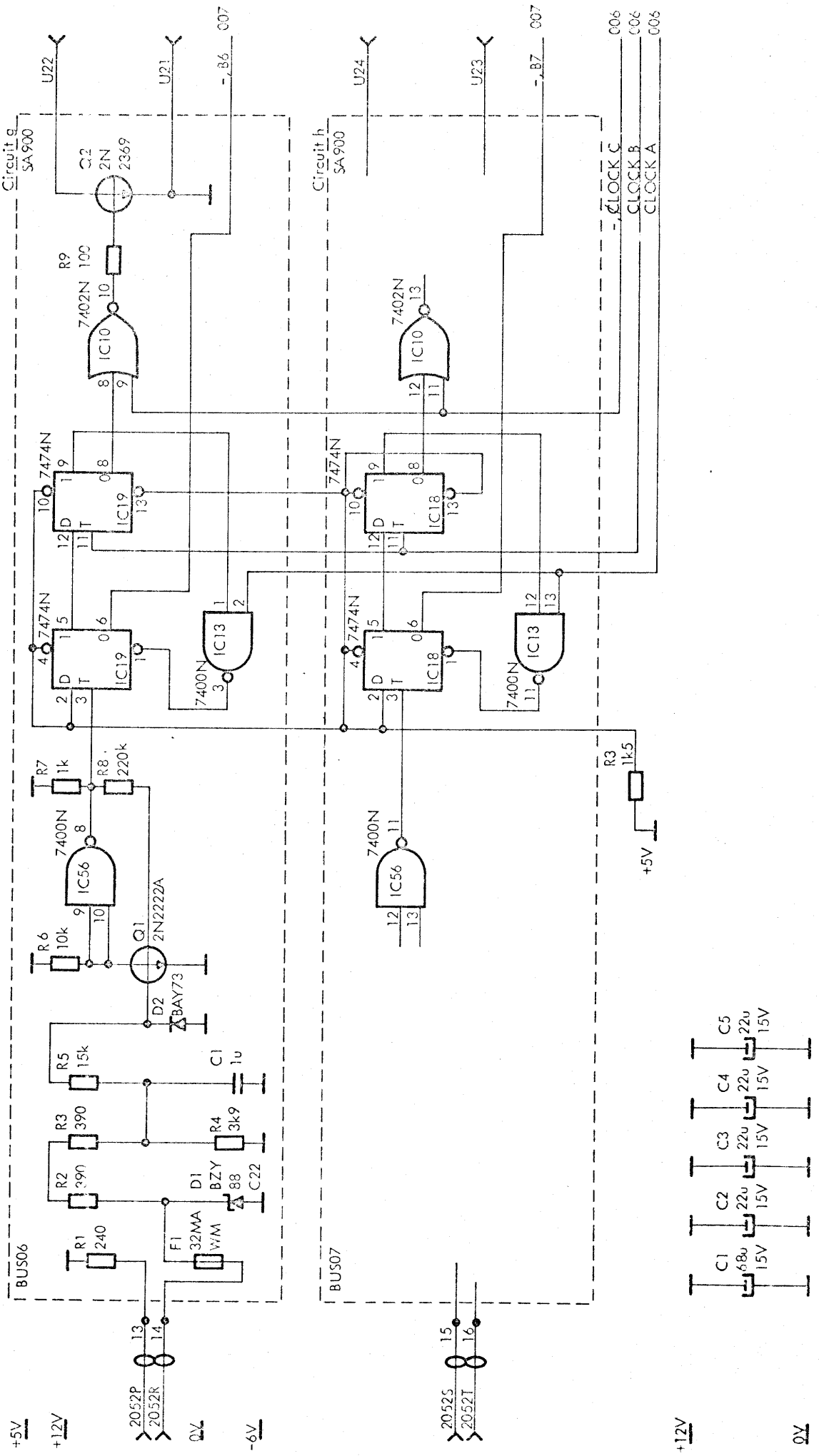
(BUS 00-02)

1) P001

V12081

PCBA Circuit Diagram


IXP401
V12082
PCBA Circuit Diagram
(BUS 3-5)
I <P002
+5V
+12V
0V
-6V
BUS03
BUS04
BUS05
2052H
2052J
2052K
2052L
2052M
2052N
R1 240
R2 390
R3 390
R4 3k9
R5 15k
R6 10k
R7 1k
R8 220k
R9 100
R2 1k5
F1 32MA WM
D1 BZY 88 C22
C1 1u
D2 BAY73
Q1 2N2222A
Q2 2N 2369
IC57
IC56
IC3
IC13
IC7
IC10
IC4
IC12
IC11
7400N
7402N
7474N
Circuit d SA900
Circuit e SA900
Circuit f SA900
U16
U15
U18
U17
U20
U19
-,B3 007
-,B4 007
-,B5 007
-,CLOCK C 006
CLOCK B 006
CLOCK A 006

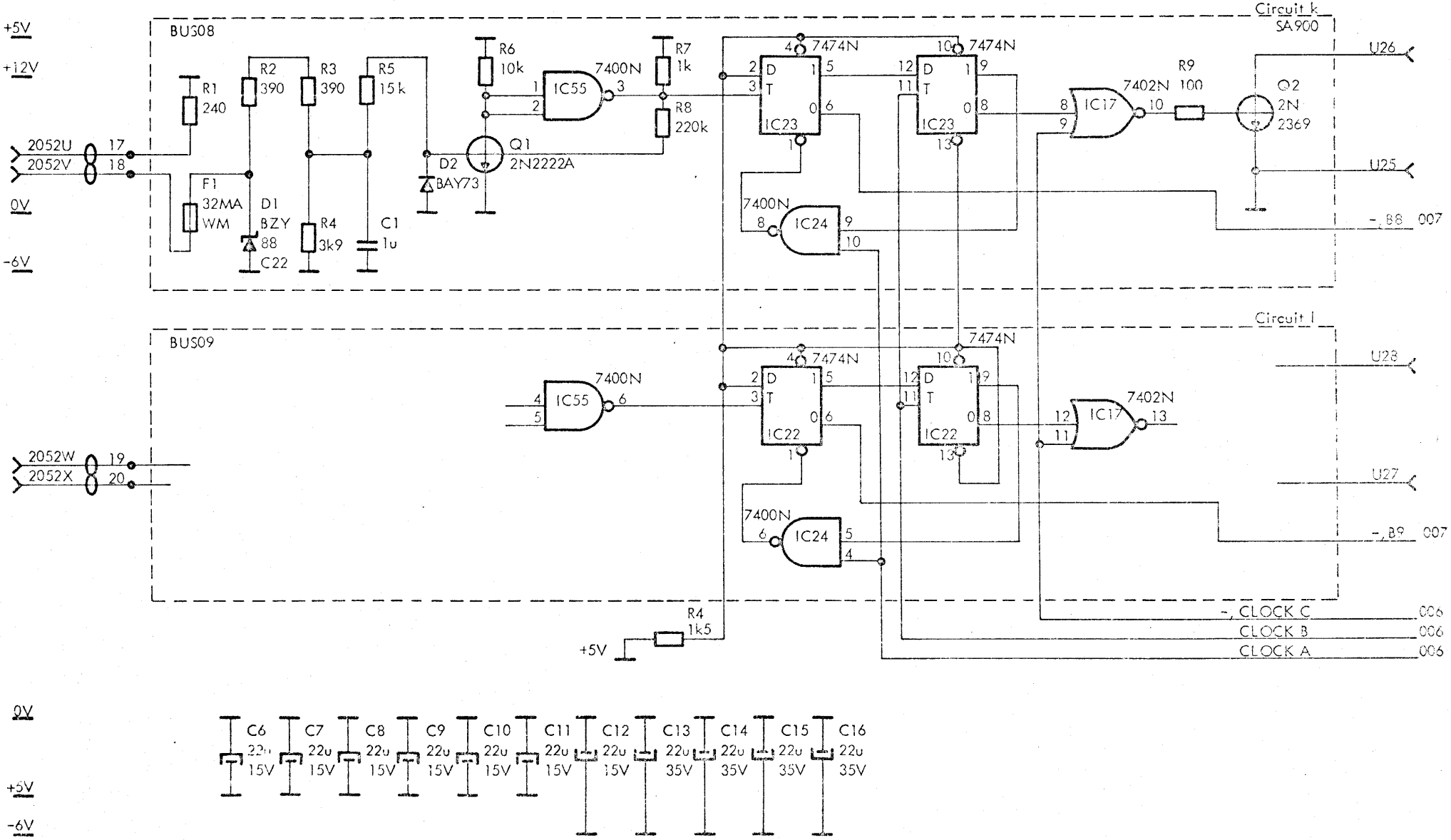


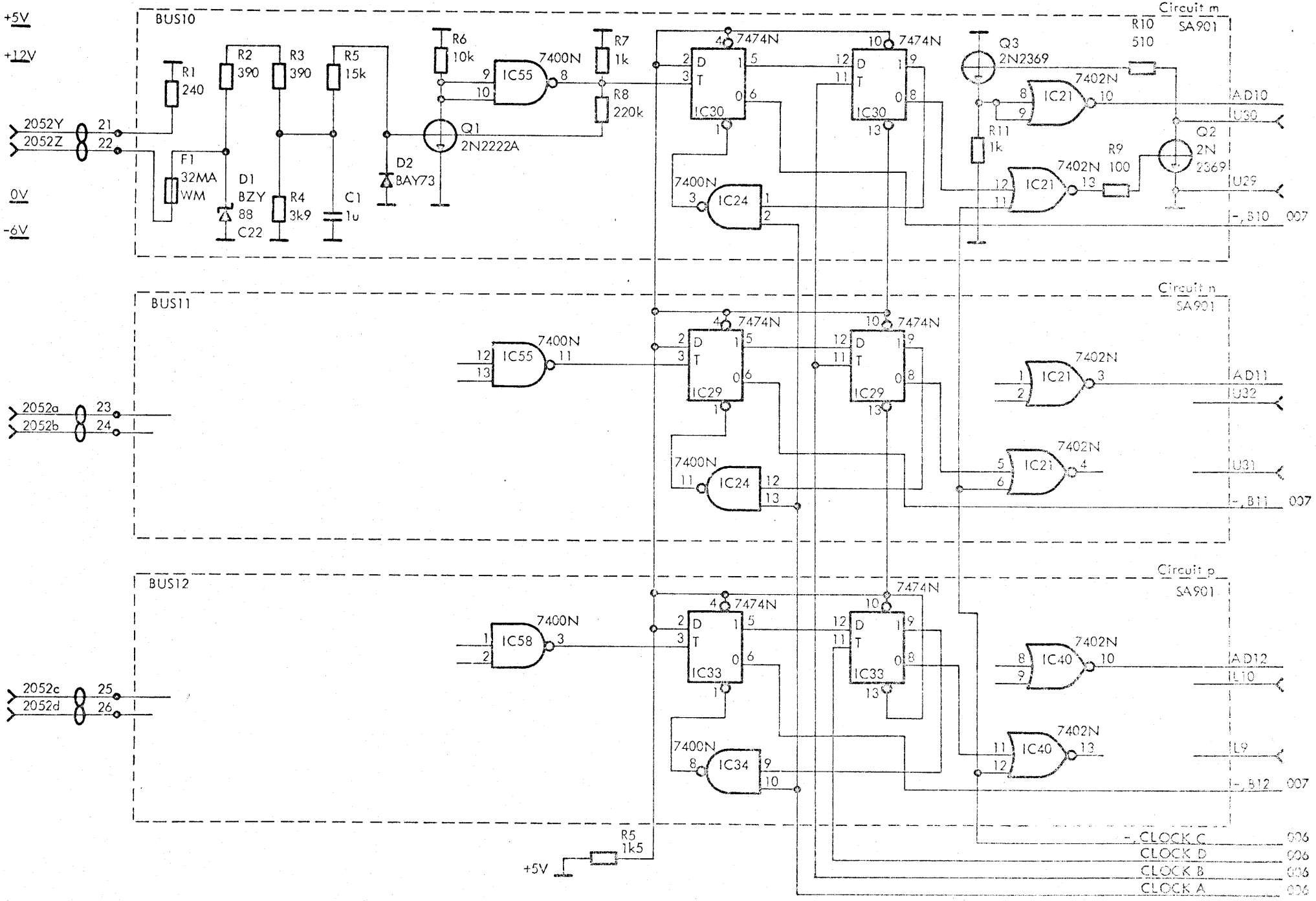
IXP401
V12083

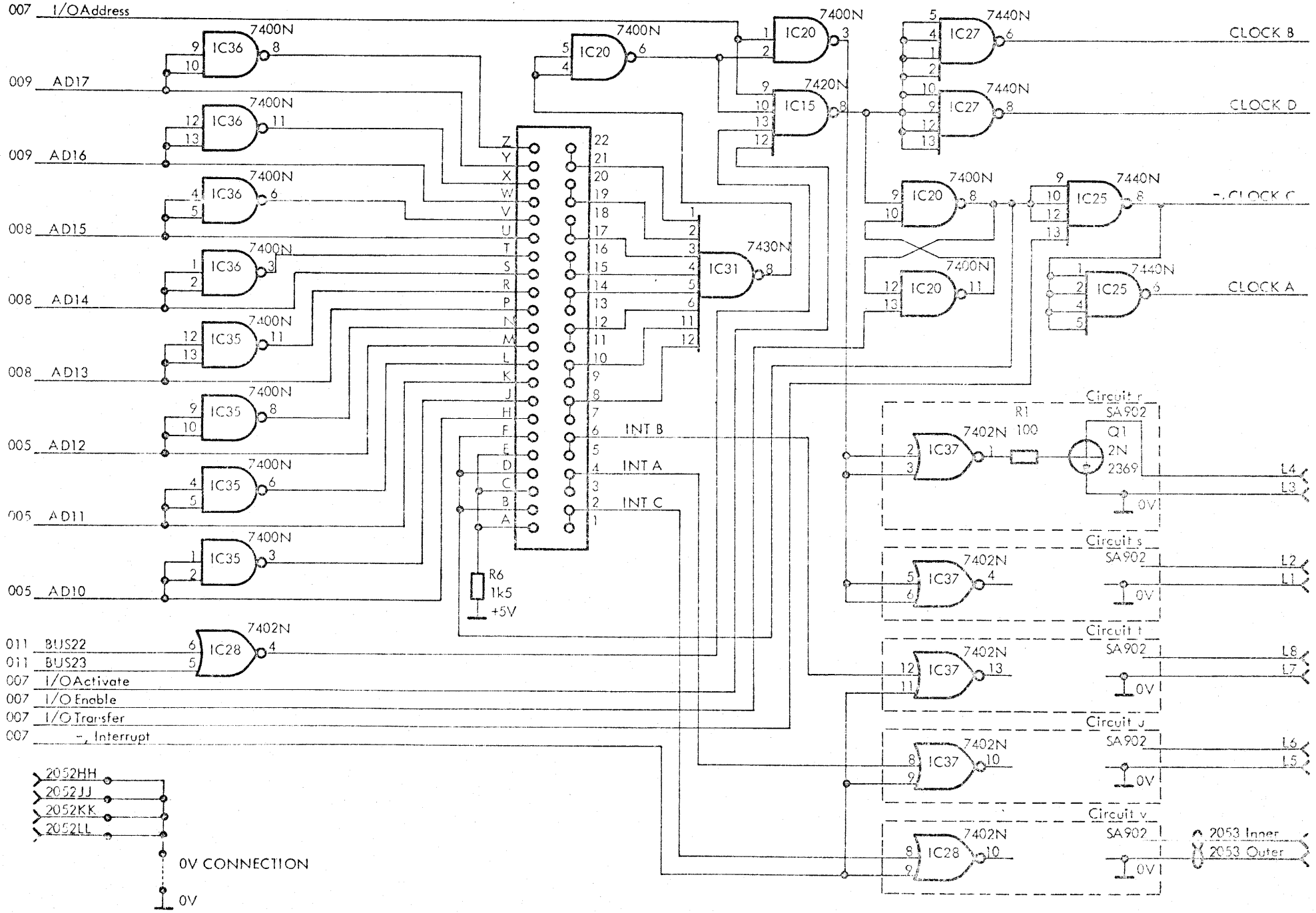
(BUS 6-7)

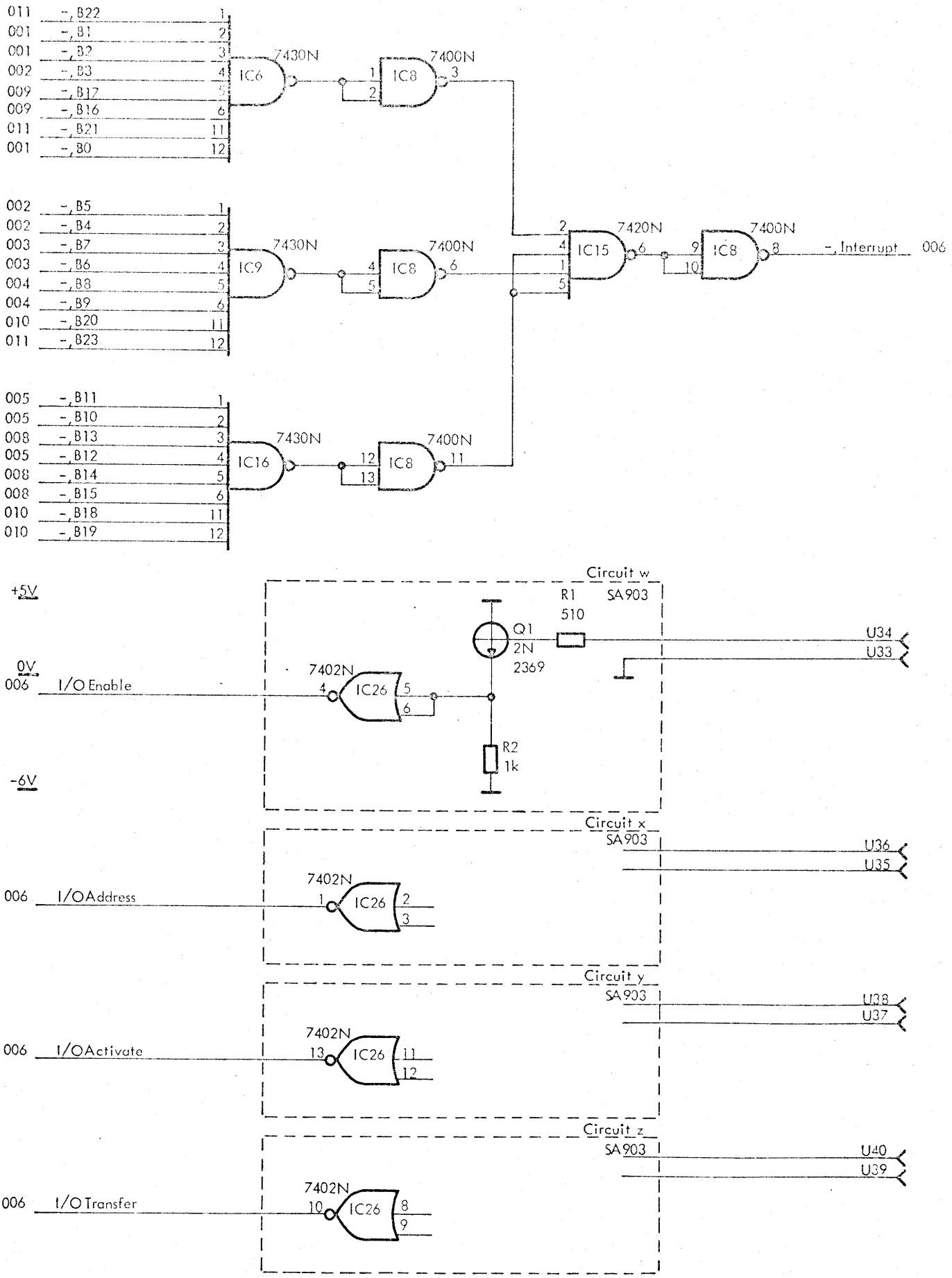
IXP003

PCBA Circuit Diagram


+5V
+12V
0V
-6V
BUS08
BUS09
Circuit k
SA900
Circuit l
2052U 17
2052V 18
2052W 19
2052X 20
R1 240
R2 390
R3 390
R4 3k9
R5 15k
R6 10k
R7 1k
R8 220k
R9 100
F1 32MA WM
D1 BZY 88 C22
D2 BAY73
Q1 2N2222A
Q2 2N 2369
C1 1u
IC55 7400N
IC23 7474N
IC24 7400N
IC17 7402N
IC22 7474N
U26
U25
U28
U27
-, BB 007
-, BB 007
R4 1k5
-, CLOCK C 006
CLOCK B 006
CLOCK A 006
0V
+5V
-6V
C6 22u 15V
C7 22u 15V
C8 22u 15V
C9 22u 15V
C10 22u 15V
C11 22u 15V
C12 22u 15V
C13 22u 35V
C14 22u 35V
C15 22u 35V
C16 22u 35V


V12085
IXP401
(BUS 10-12)
PCBA Circuit Diagram
XP005
+5V
+12V
0V
-6V
BUS10
BUS11
BUS12
Circuit m
SA901
Circuit n
SA901
Circuit p
SA901
2052Y
2052Z
2052a
2052b
2052c
2052d
R1 240
R2 390
R3 390
R4 3k9
R5 15k
R6 10k
R7 1k
R8 220k
R9 100
R10 510
R11 1k
F1 32MA WM
D1 BZY 88 C22
D2 BAY73
C1 1u
Q1 2N2222A
Q2 2N 2369
Q3 2N2369
7400N
7402N
7474N
IC55
IC24
IC21
IC30
IC29
IC33
IC58
IC34
IC40
AD10
AD11
AD12
U30
U29
U32
U31
L10
L9
-,B10
-,B11
-,B12
007
-,CLOCK C
CLOCK D
CLOCK B
CLOCK A
006
R5 1k5


007 I/OAddress
009 AD17
009 AD16
008 AD15
008 AD14
008 AD13
005 AD12
005 AD11
005 AD10
011 BUS22
011 BUS23
007 I/OActivate
007 I/O Enable
007 I/O Transfer
007 -, Interrupt
7400N
7402N
7420N
7430N
7440N
IC36
IC35
IC20
IC15
IC31
IC28
IC27
IC25
IC37
INT B
INT A
INT C
R6
1k5
+5V
R1
100
Q1
2N
2369
SA902
Circuit r
Circuit s
Circuit t
Circuit u
Circuit v
0V
L4
L3
L2
L1
L8
L7
L6
L5
CLOCK B
CLOCK D
-, CLOCK C
CLOCK A
2053 Inner
2053 Outer
2052HH
2052JJ
2052KK
2052LL
0V CONNECTION
0V

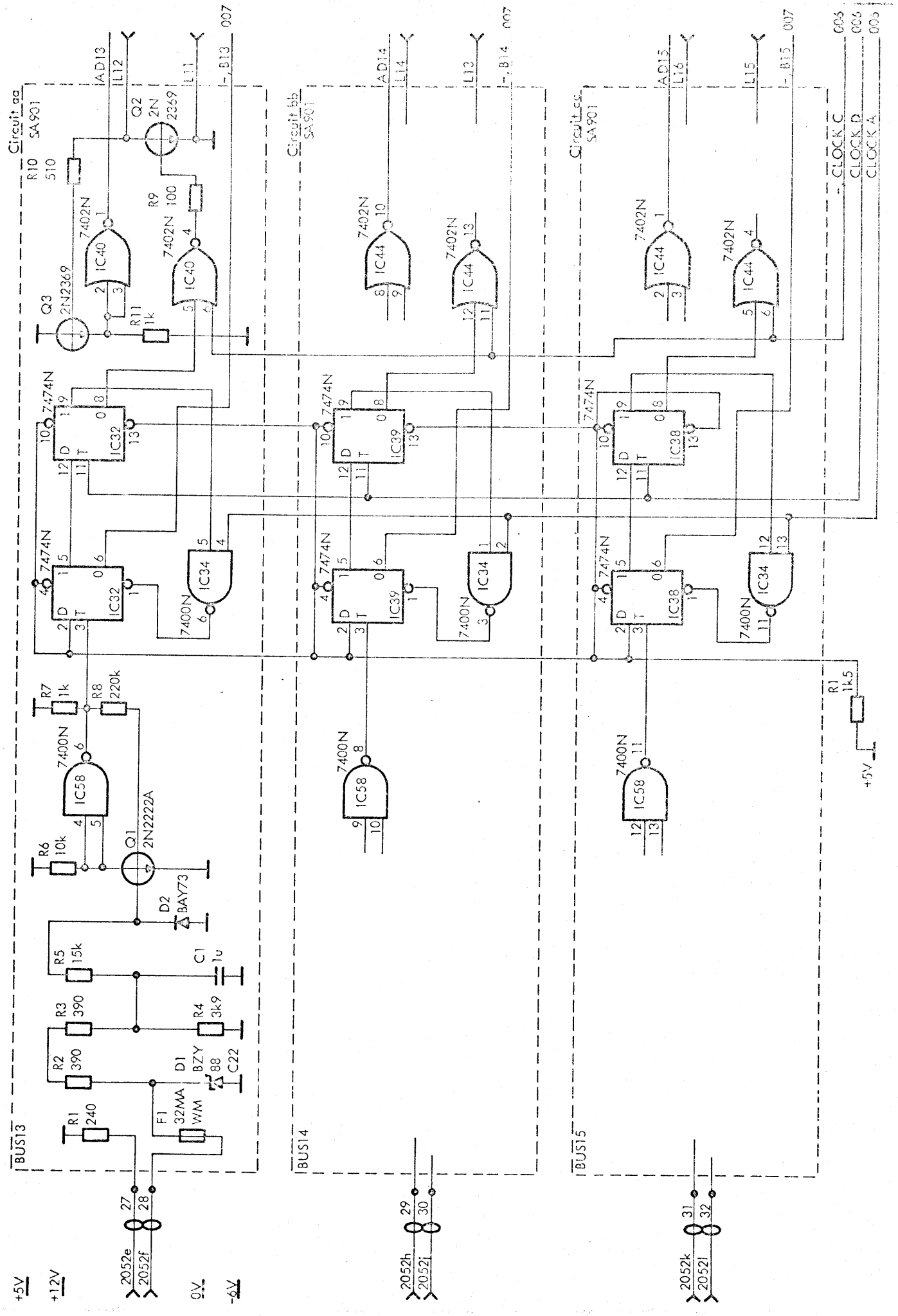


IXP401

IXP007

V12087

PCBA Circuit Diagram



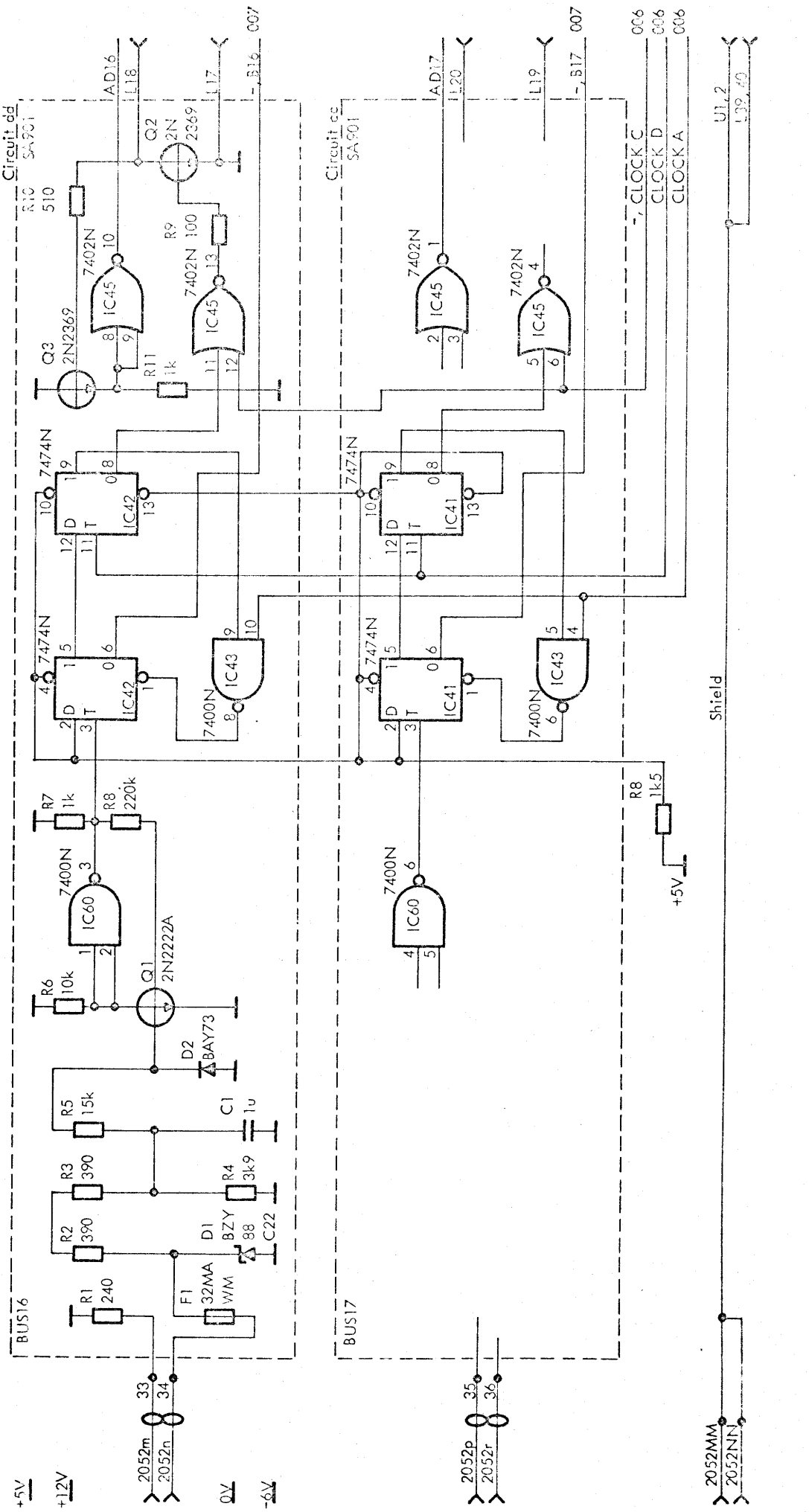
IXP401

(BUS 13-15)

IXP008

V12088

PCBA Circuit Diagram



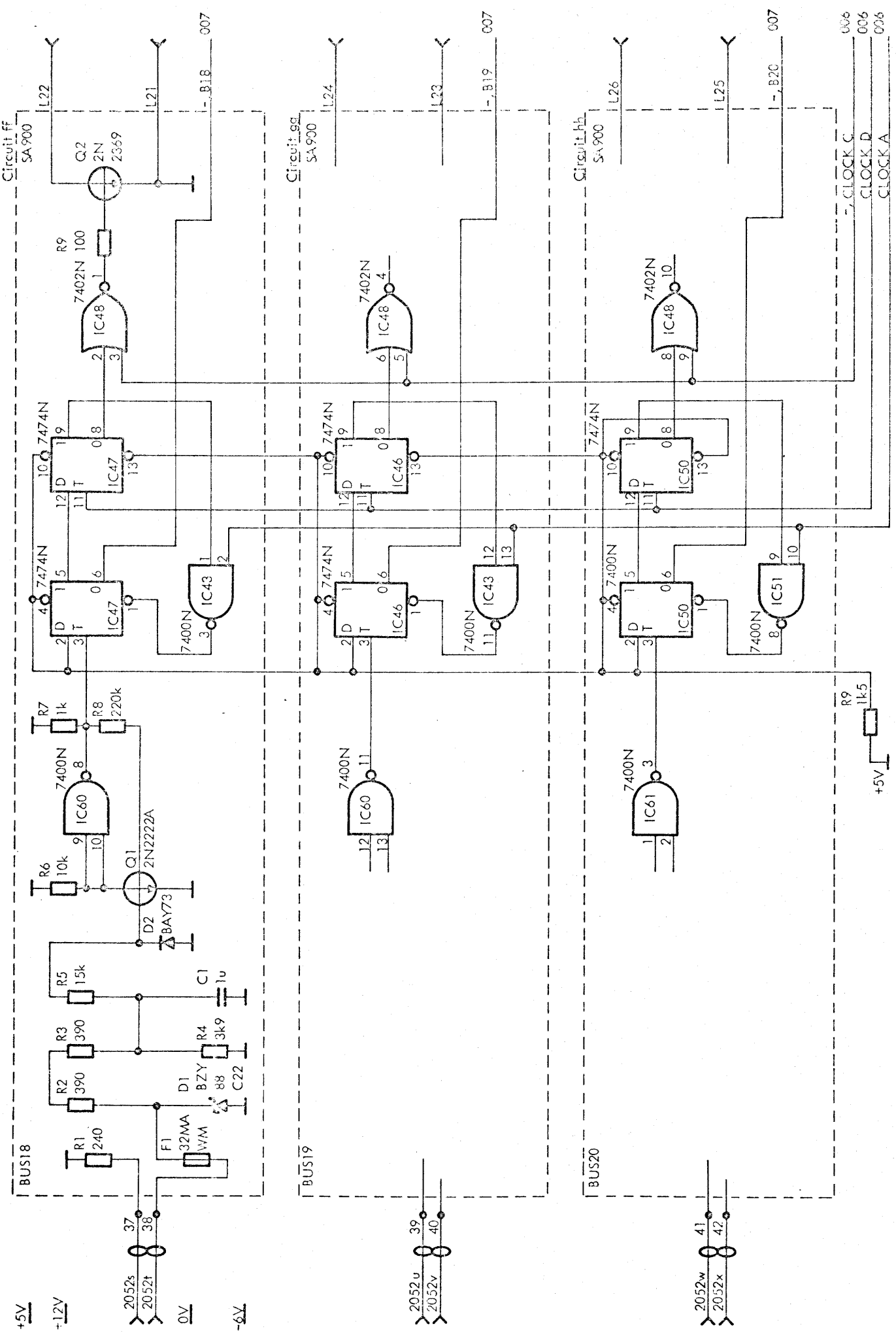
IXP401

V12089

(BUS 16-17)

PCBA Circuit Diagram

IXP009



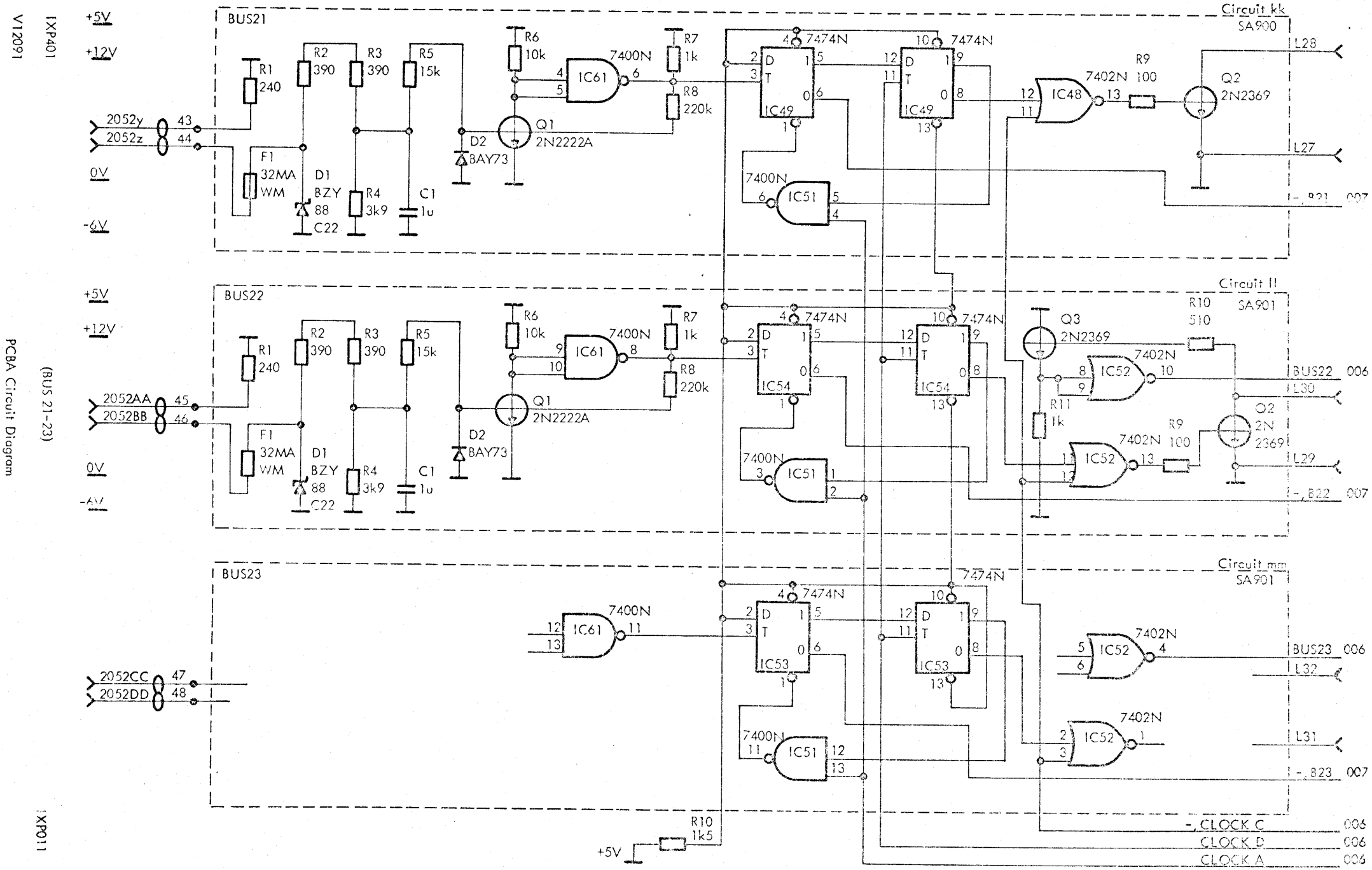
IXP401

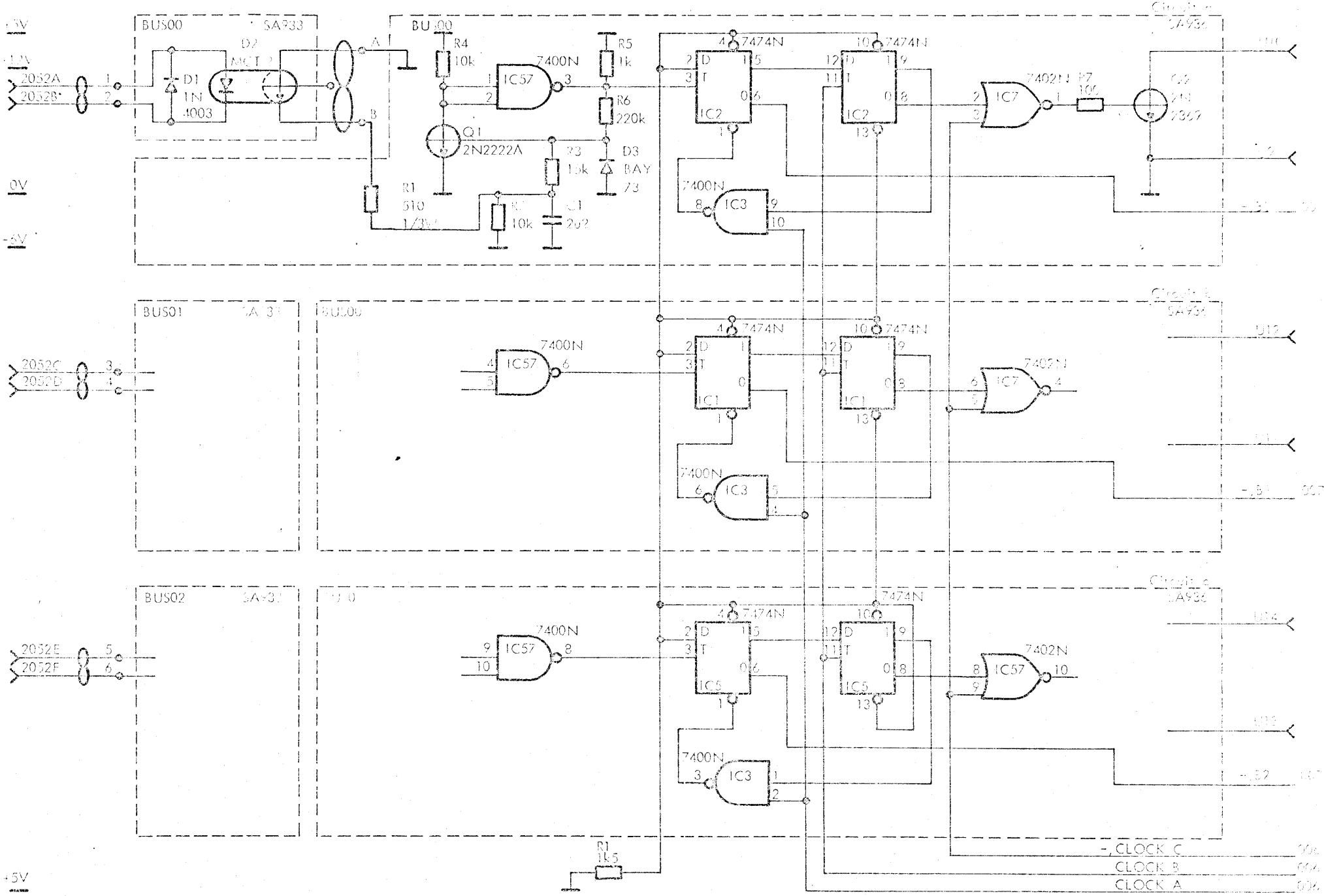
(BUS 18-20)

IXP010

V12090

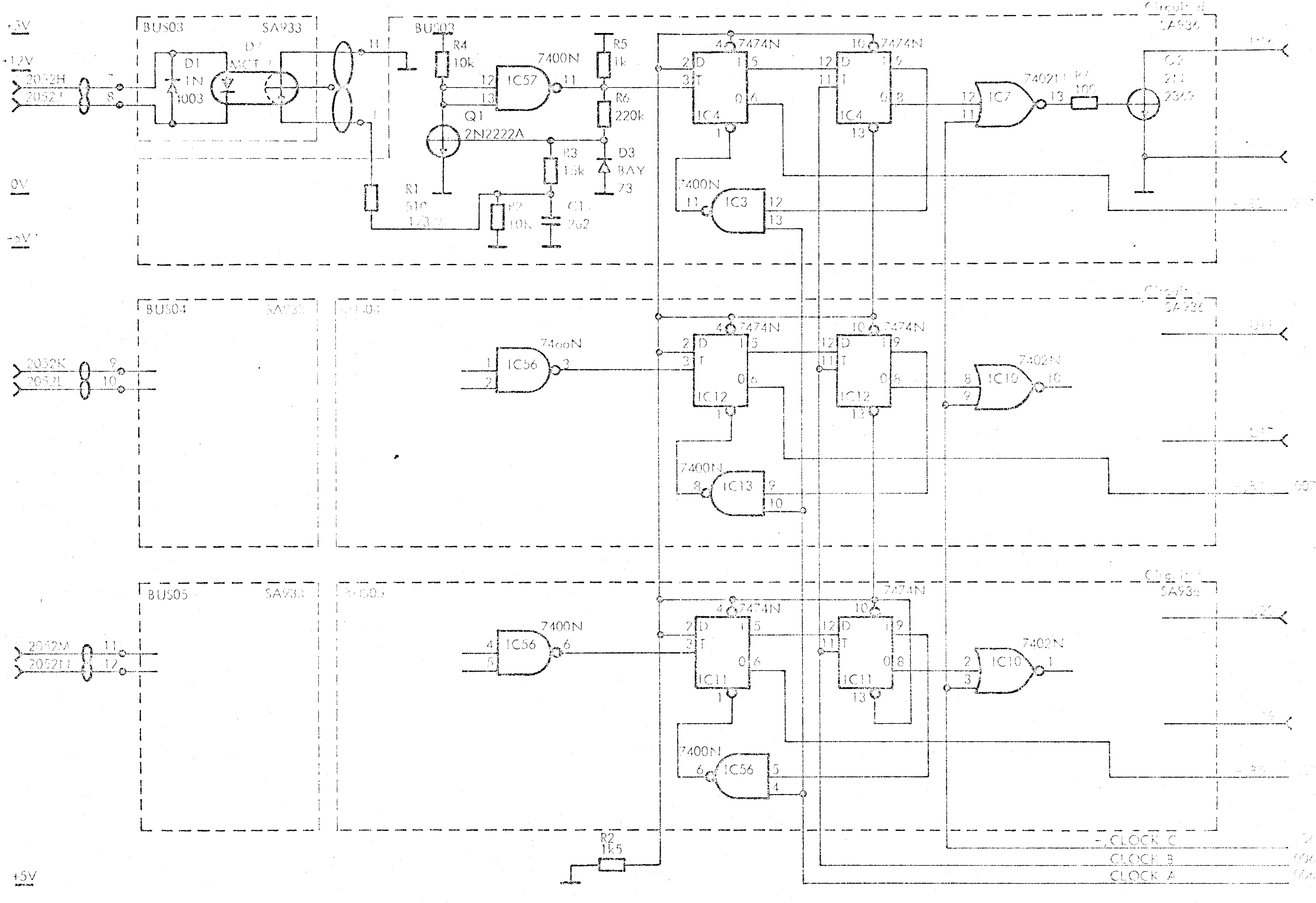
PCBA Circuit Diagram


PCBA Circuit Diagram
V12091
IXP401
(BUS 21-23)
IXP011
BUS21
BUS22
BUS23
+5V
+12V
0V
-6V
2052y
2052z
2052AA
2052BB
2052CC
2052DD
R1 240
R2 390
R3 390
R4 3k9
R5 15k
R6 10k
R7 1k
R8 220k
R9 100
R10 510
R10 1k5
R11 1k
C1 1u
F1 32MA WM
D1 BZY 88 C22
D2 BAY73
Q1 2N2222A
Q2 2N2369
Q3 2N2369
IC61
IC48
IC49
IC51
IC52
IC53
IC54
7400N
7402N
7474N
Circuit kk SA900
Circuit ll SA901
Circuit mm SA901
L28
L27
L30
L29
L32
L31
BUS22 006
BUS23 006
-,B21 007
-,B22 007
-,B23 007
-,CLOCK C 006
CLOCK D 006
CLOCK A 006

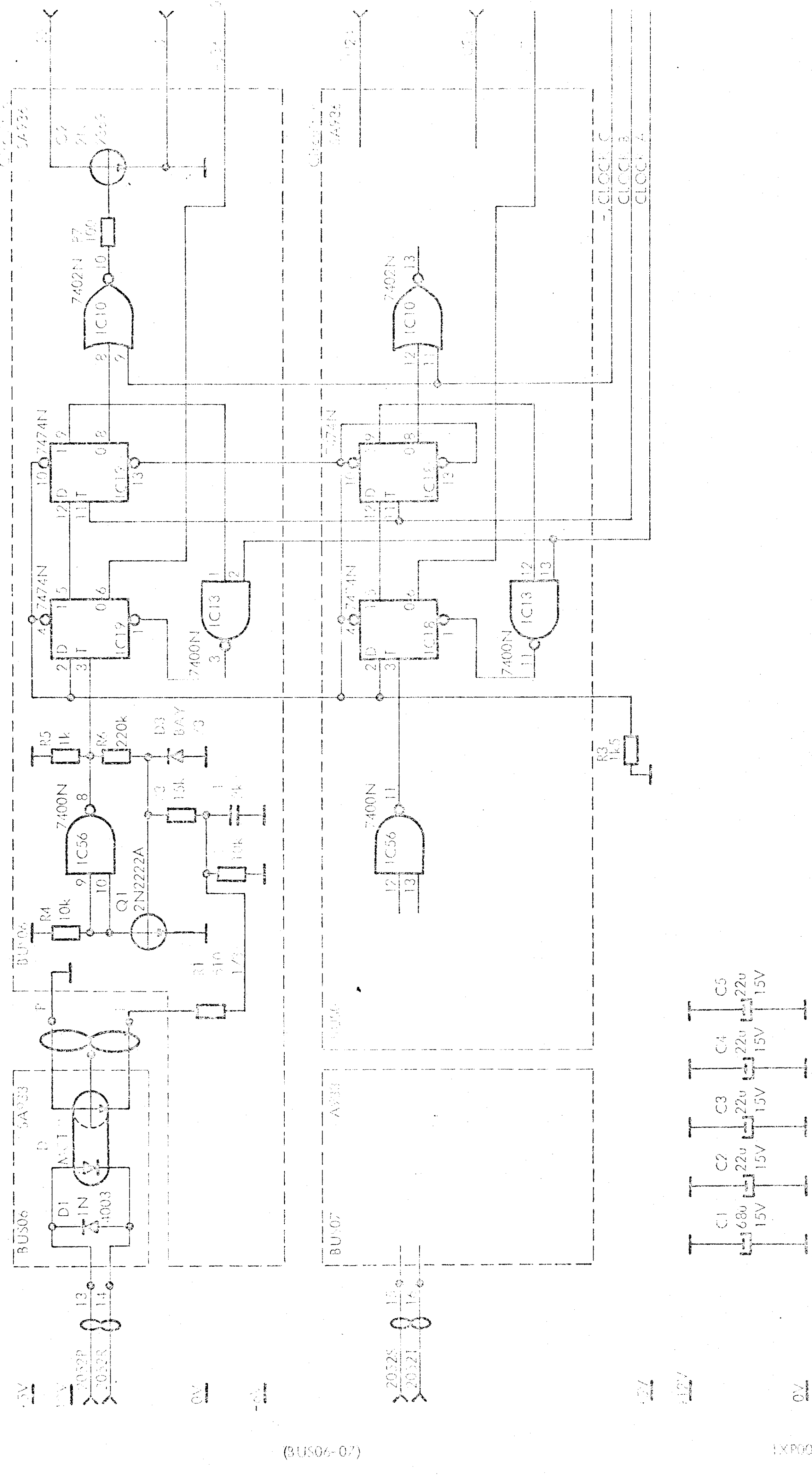


PCBA Circuit Diagram (BUS00-03)

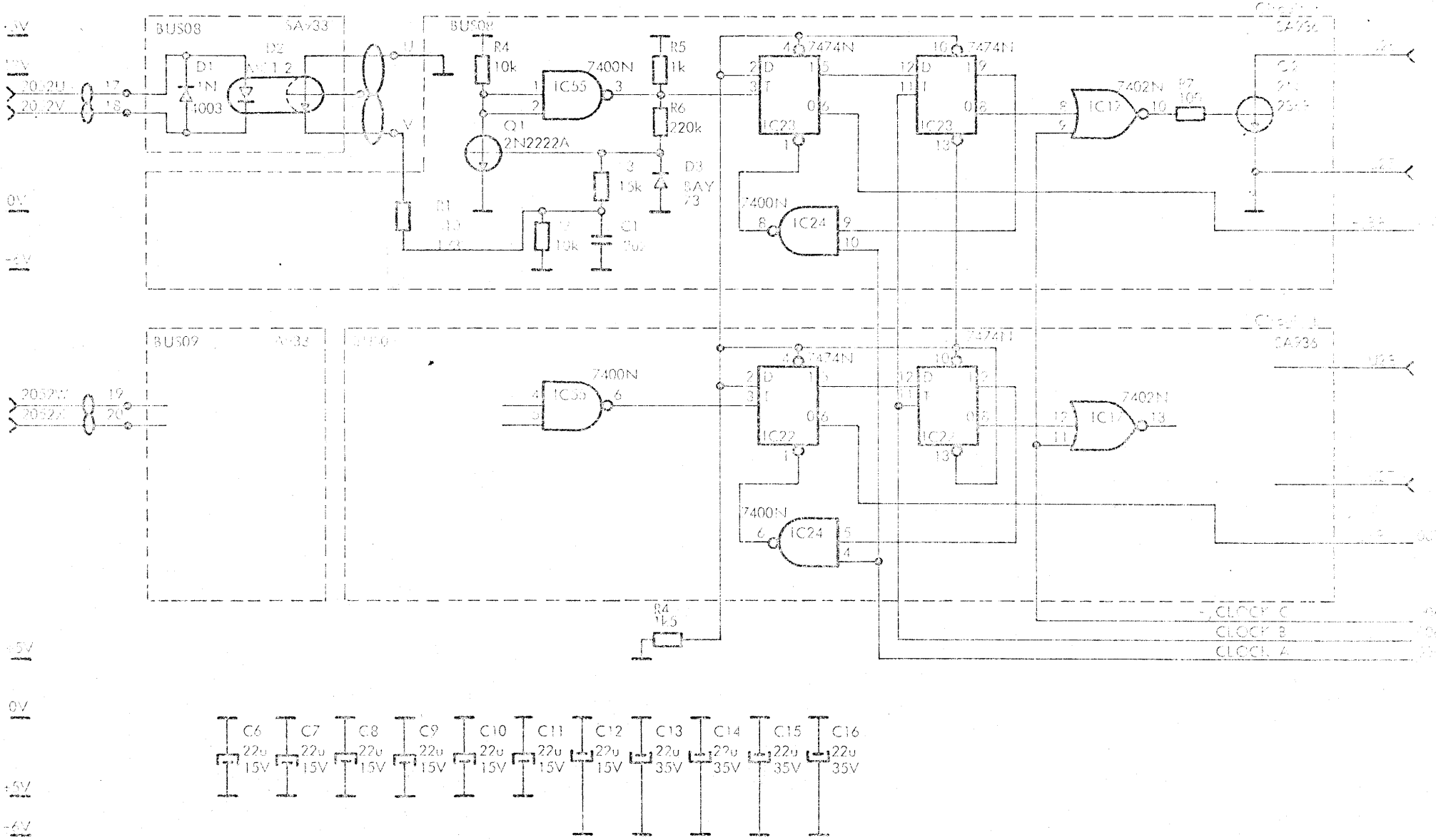
200569LPH 250371SSL 130471 ANOC 130491 LPdL V12649



200569LPH 250371SSL 130471 ANOC 130471 LPH V17650



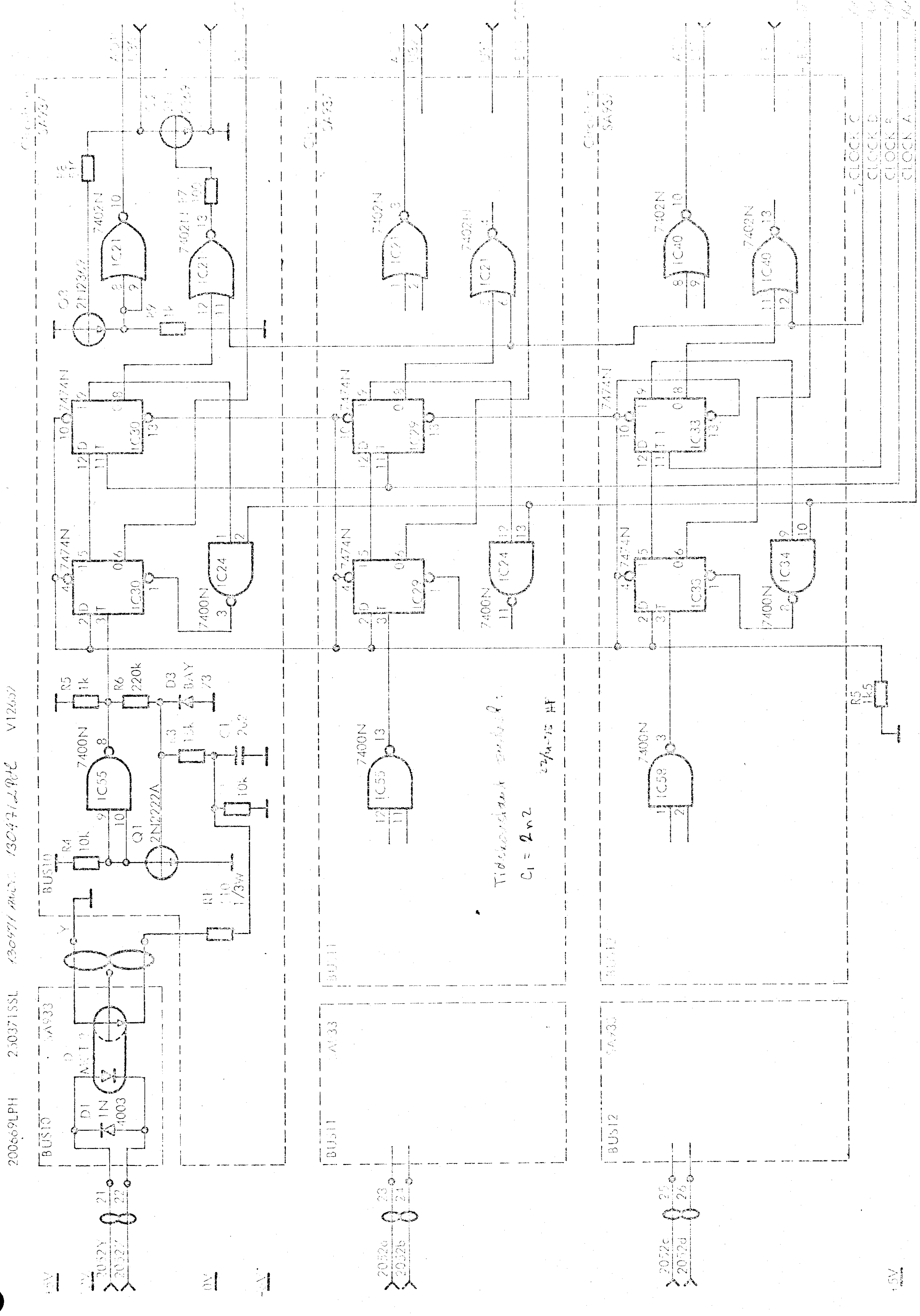
200569LPH 250371SSL 130471 AVEC 130471_LPH, V12651



(BUS02-09)

PCBA Circuit Diagram

1XP004



IXP 403 (BUS10-12) IXP005

V12914 PCBA Circuit Diagram

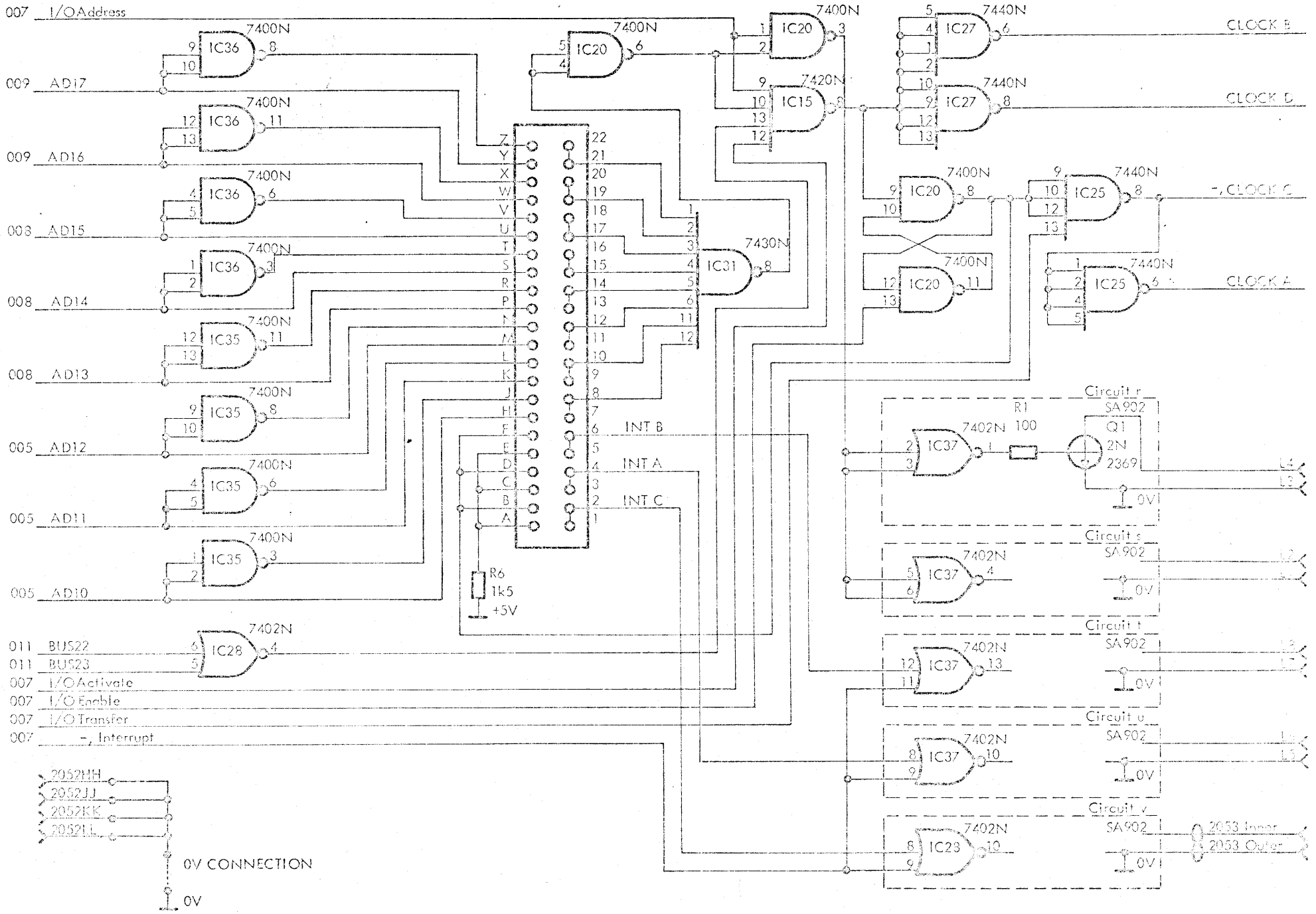
200569LPH 201070SSL 021170IA 111170 LRH.

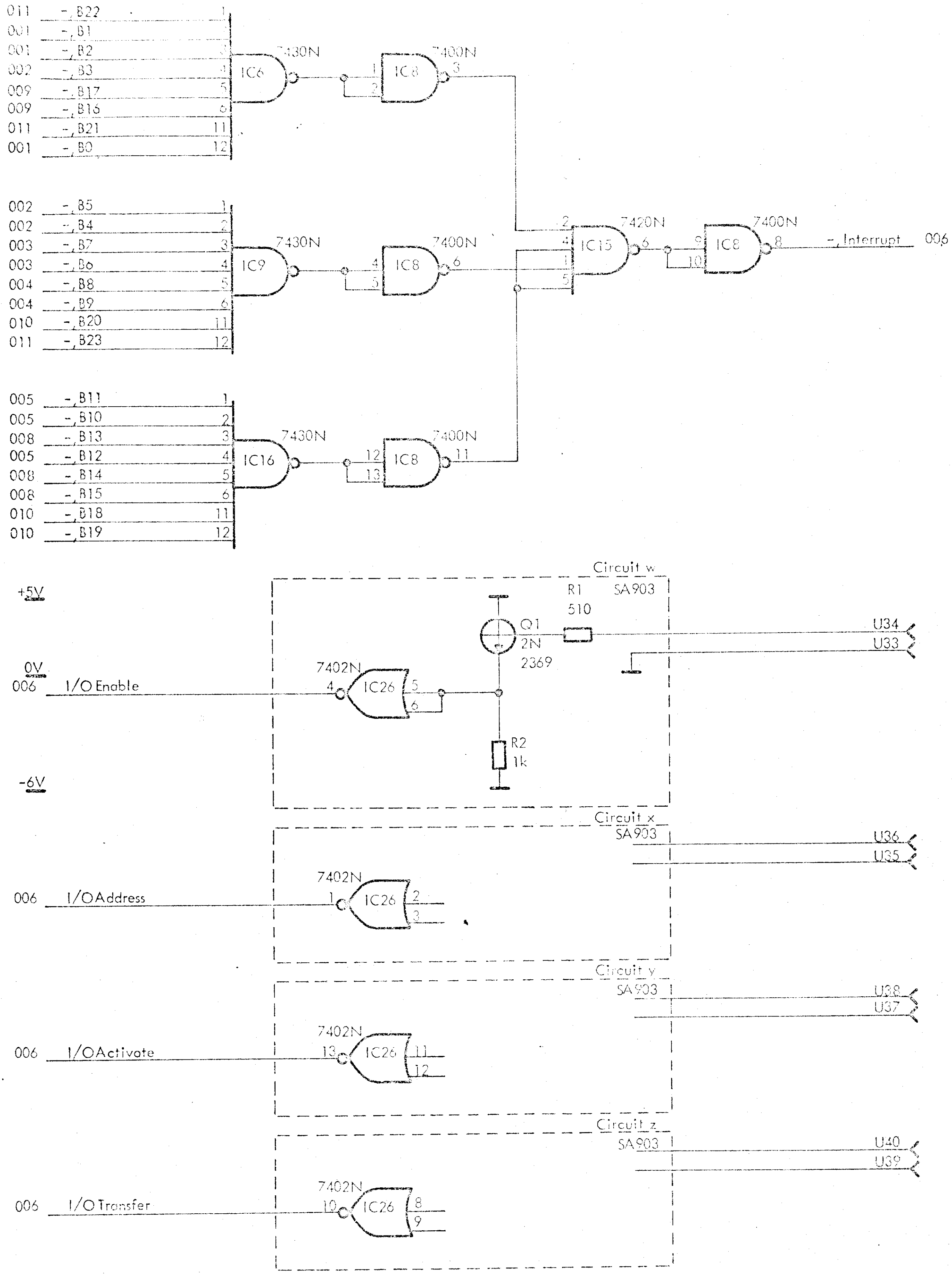
V12653

IXP 403

PCBA Circuit Diagram

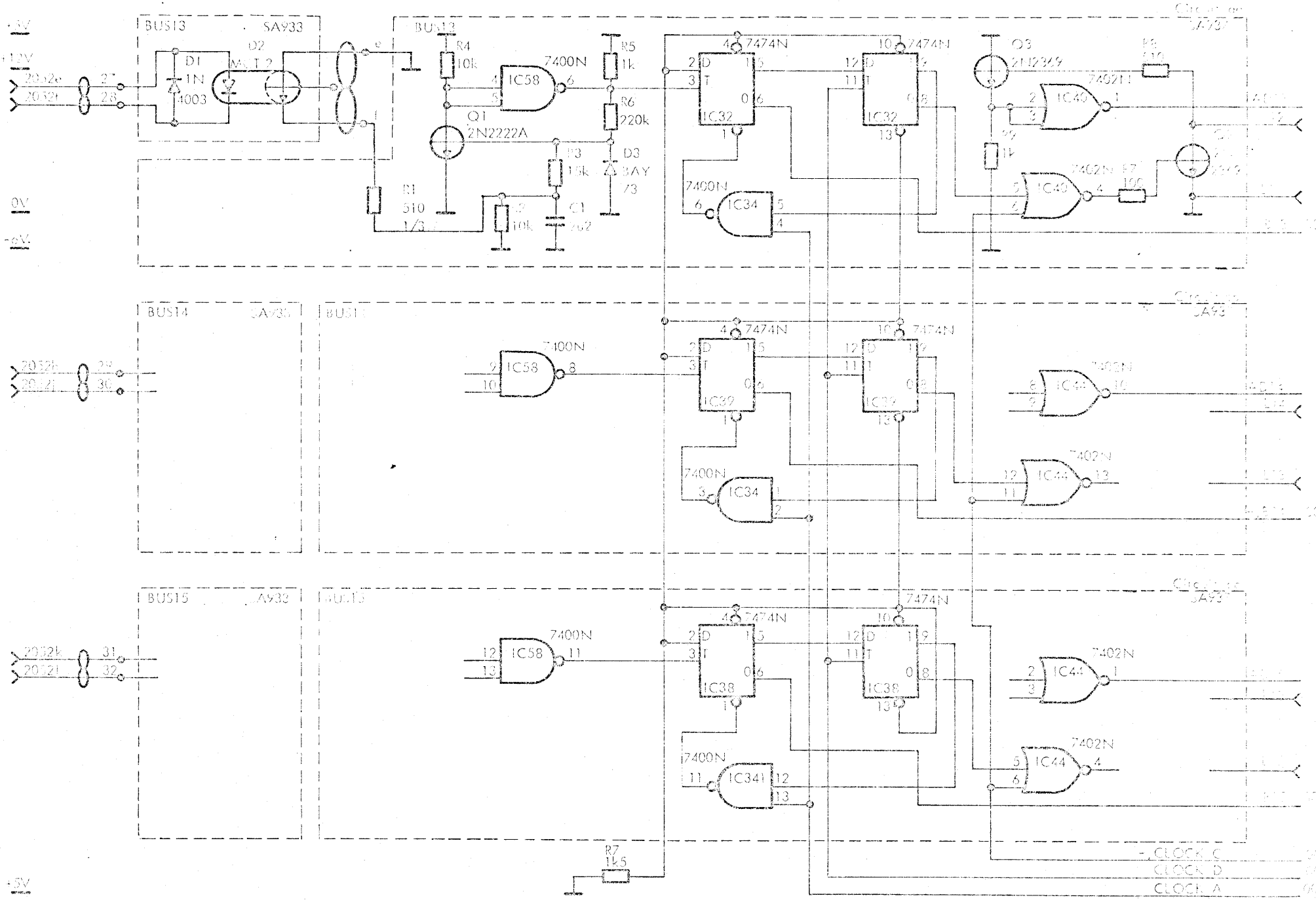
IXP006



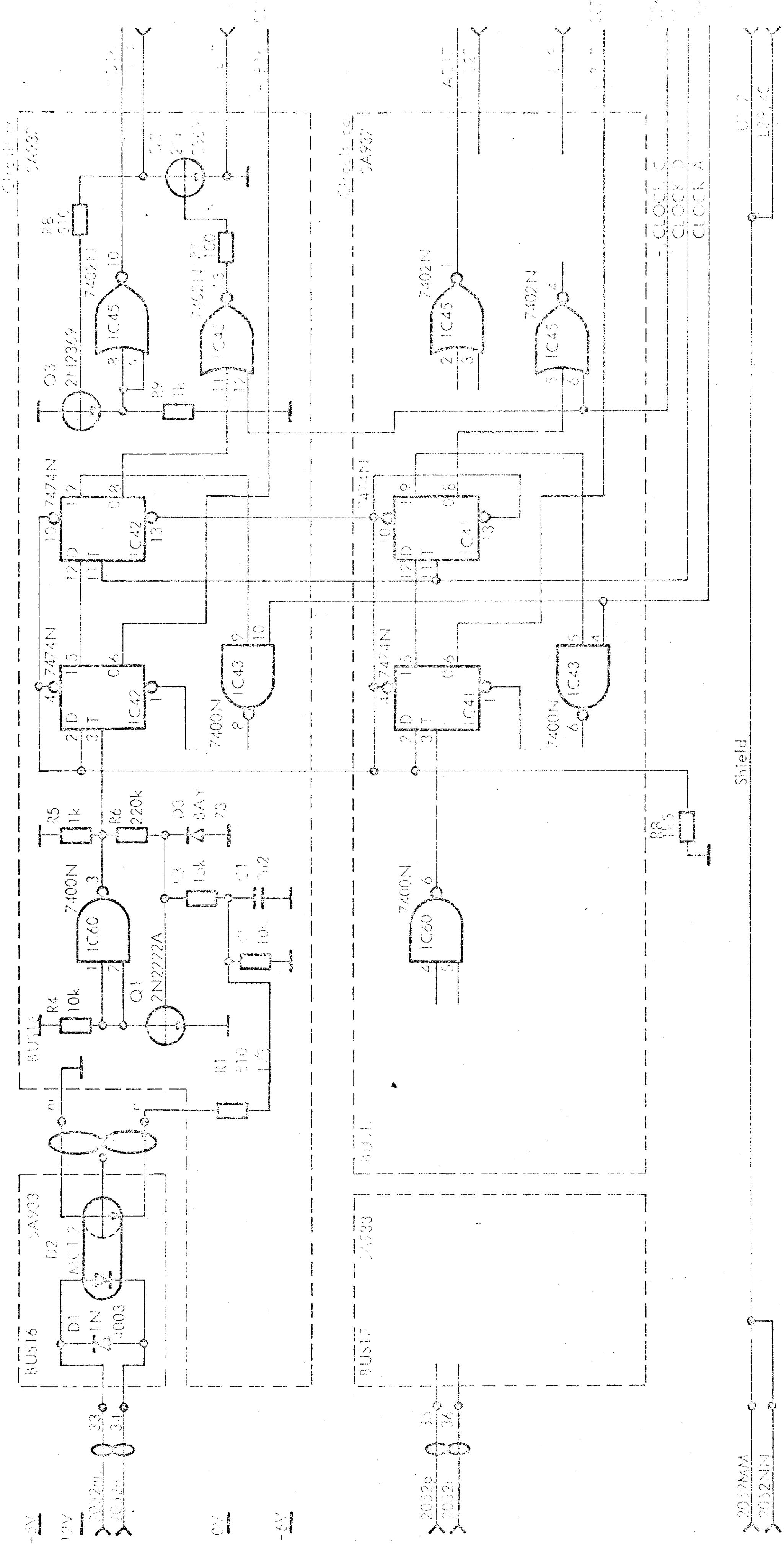


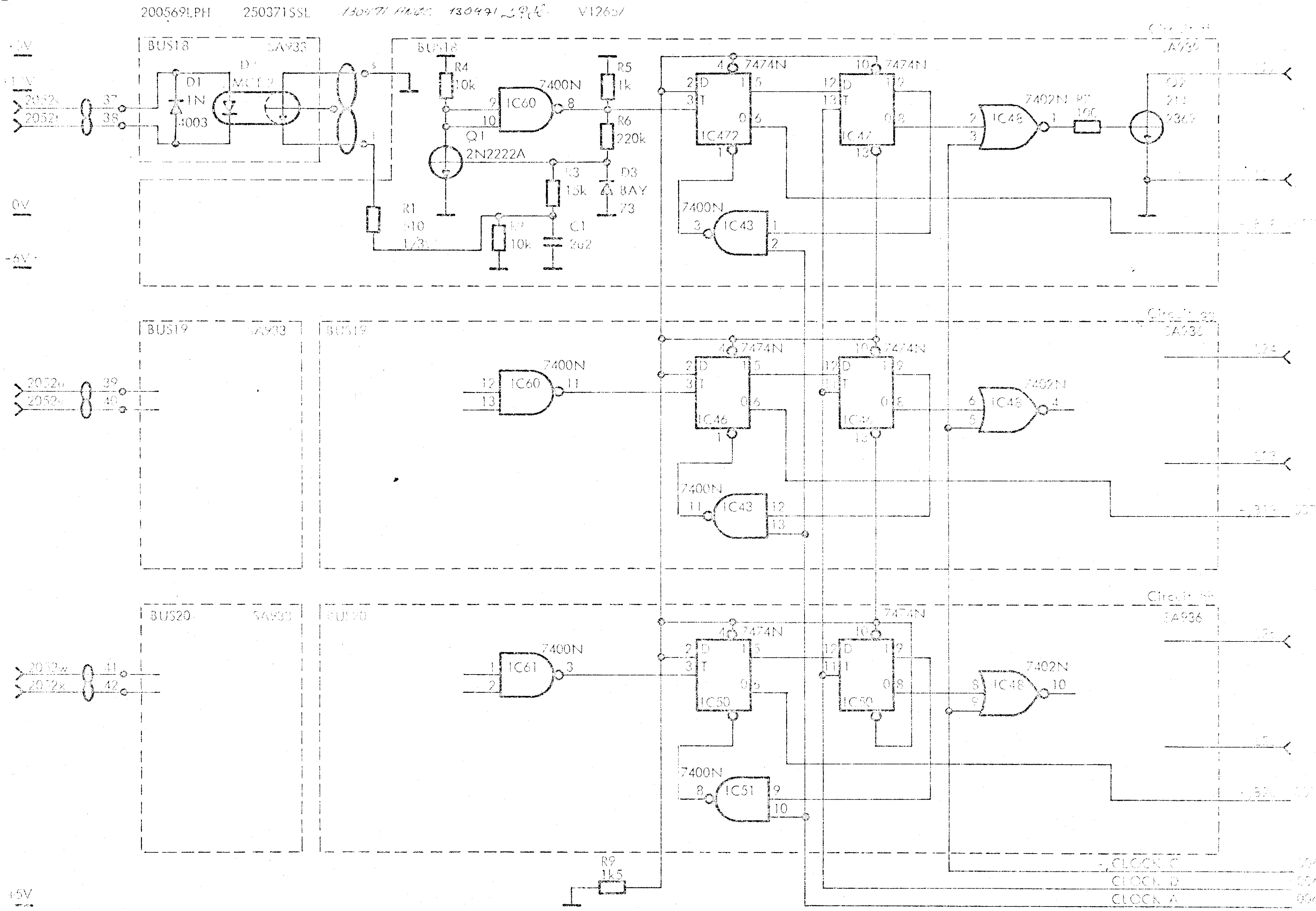
201070SSL

200569LPH


BUS13 SA933
BUS12
BUS14 SA933
BUS13
BUS15 SA933
BUS15
+5V
+12V
0V
-6V
D1 1N 4003
D2
R1 510 1/3
R2 10k
R3 15k
R4 10k
R5 1k
R6 220k
R7 1k5
D3 BAY 73
Q1 2N2222A
Q3 2N2369
7400N IC58
7400N IC34
7400N IC34
7400N IC34
7474N IC32
7474N IC32
7474N IC32
7474N IC38
7474N IC38
7474N IC38
7402N IC40
7402N IC40
7402N IC44
7402N IC44
7402N IC44
7402N IC44
CLOCK C
CLOCK D
CLOCK A

200569LPH 250371SSL 130471 AMOC 1304 71 ... V12656





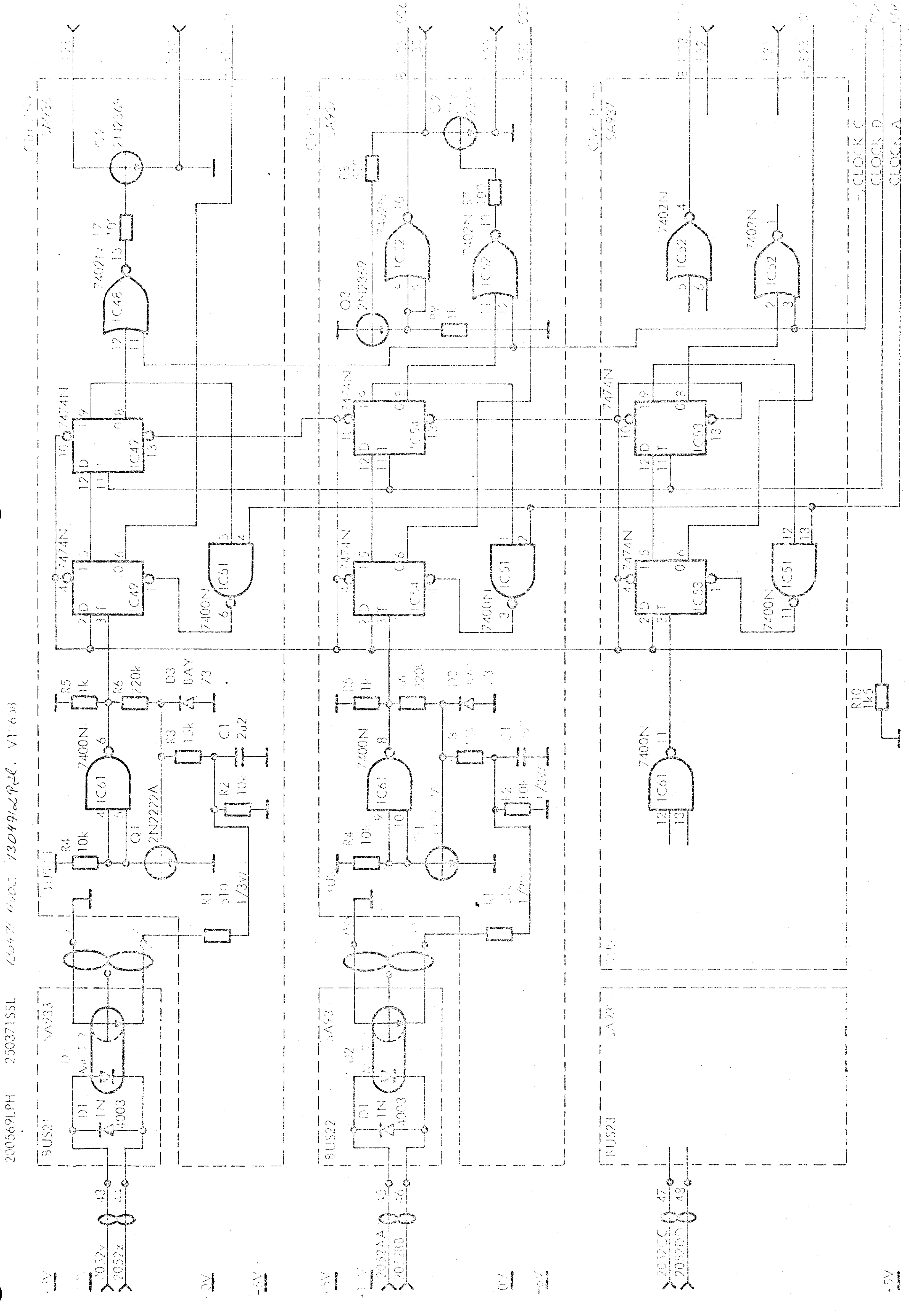
1XP403

V12817

(BUS18-20)

PCBA Circuit Diagram

1XP010



J13218 PCBA Circuit Diagram

INTERRUPT EXPANDER IXP406

Interrupt expander IXP406 is a 24-channel buffered digital input unit with 24 separate input connectors. It is equipped with a logical output to be connected either to one of the interrupt-level inputs of RC 4000 or via a separate output connector to an input of another Interrupt Expander, IXP406. IXP406 can be placed in chassis CHS404 and is connected to the Low-Speed Data Channel via Busline Converter , BCV401. The interrupt-output changes state first time a logical one is applied to one of the inputs of a cleared IXP406.

This input pulse and possible following input pulses will be stored in the buffer register.

Data transfer of the contents of the 24-bit buffer register to the W-register takes place by means of a Sense command as determined by the program in progress (e.g. an interrupt response program).

When a transfer has been executed the buffer register and the interrupt-output as well is cleared.

Application:	Selective interconnection of interrupt signals from an unlimited number of RC 4000 Input/Output modules (e.g. IXP401 -404, SPT401 etc.)

Specifications:

Selection:	I/O instruction with predetermined device address
Number of Inputs:	24, one connector per input.
Type of Input:	TTL logic levels, with individual return wire.

Input Cable Resistance:	max. 2 ohms.
Input Cable Distance:	max. 5 meters.
Type of Cable:	Twisted pair with shield, characteristic impedance: 100 ohms.
Number of Outputs:	1 interrupt output
Type of Output (Interrupt):	TTL logic levels
Dimensions:	Height: 355 mm Width: 24 mm Depth: 450 mm
Supply Power:	+ 5 V ± 5 per cent, 2000 mA - 6 V ± 5 per cent, 150 mA
Ambient Air:	Temperature: 0 to 45 degrees C Relative Humidity: 30 to 70 per cent
Weight:	1.2 kg.

20-10-1972

Interrupt liste IXP406

device no.: 41

interrupt level: 16

Bit	signalgiver	device no.
00	IXP403	42
01	BCTIXP	73
02	(faic0)	(142)
03	(aoc1)	(140)
04	(aoc2)	(141)
05	(aocb)	(11)
06	SPTIXP	37
07	(sct20)	(143)
08	(ikt)	(144)
09	(aict)	(145)
10	(ppuls1)	(24)
11	(ppuls2)	(25)
12	(ppuls3)	(26)
13	(ppuls4)	(27)
14		
15		
16		
17		
18		
19		
20		
21		
22		

RCSL: 51-VB883
Author: P. E. Pedersen
Edited: May 1970

RC 4000 PERIPHERAL DEVICES

IXP 406 INTERRUPT EXPANDER

Preliminary Specifications

ABSTRACT: This report describes the logic structure of the Interrupt Expander IXP 406 when used in connection with the RC 4000 Computer.

A/S REGNECENTRALEN
Falkoneralle 1
DK 2000 Copenhagen F

1. MAIN CHARACTERISTICS

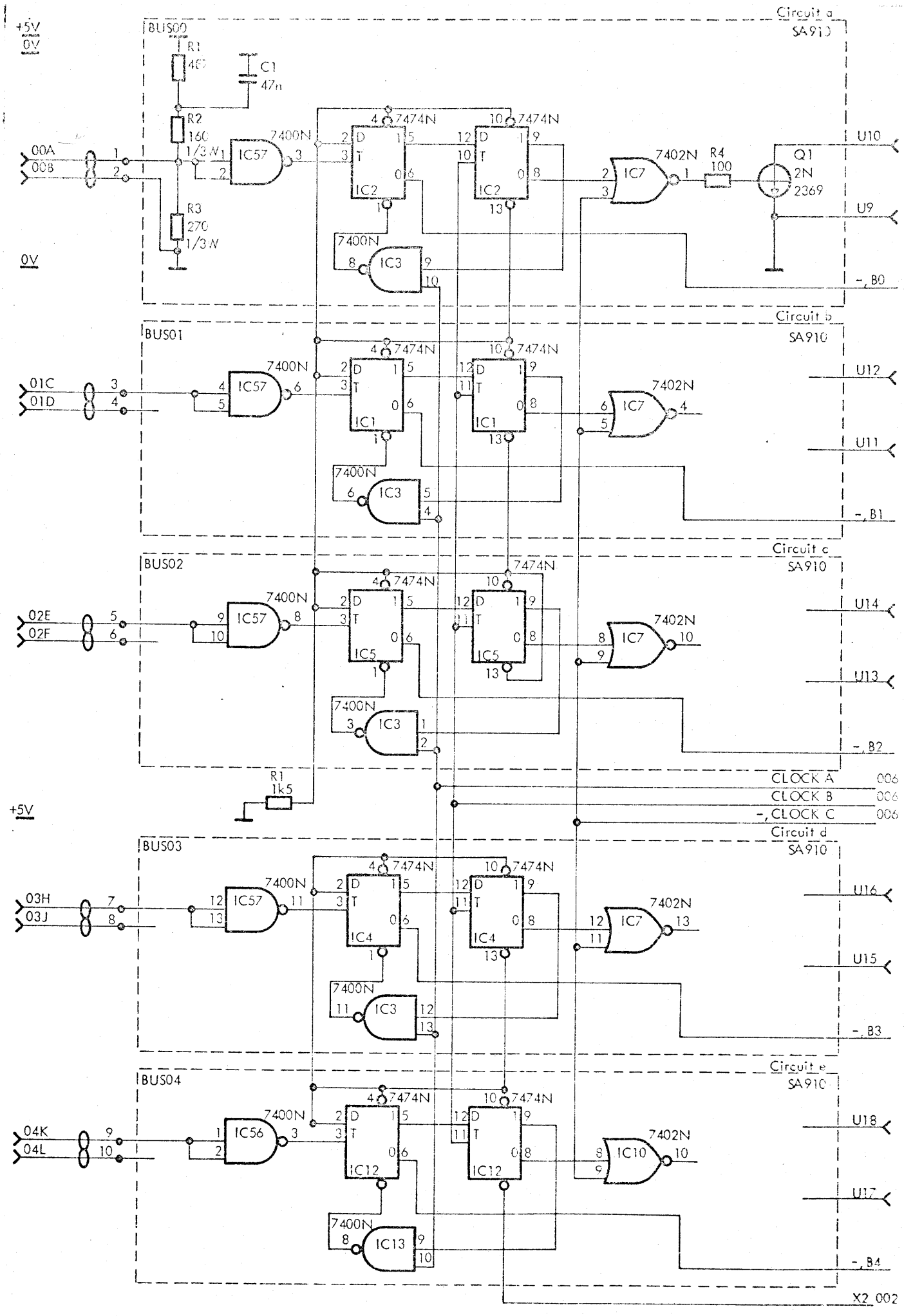
The Interrupt Expander is designed to attach 24 external interrupt signals to a single interrupt level, i.e. a single bit of the interrupt register (IR), of the RC 4000.
The Interrupt Expander includes a 24-bit buffer for collection of 24 interrupt signals. The first of these signals that changes to 1 will cause the IXP 406 to generate a single common interrupt signal.
Changing to 1 for any other of these signals will not generate new interrupt signals to the RC 4000, but will be registered as logical ones in the buffer register. The contents of the buffer register can be transferred to the RC 4000 by means of a sense command.
The Interrupt Expander is connected to the RC 4000 via the Low-Speed Data Channel and is addressed as a normal device.

2. COMMANDS

The contents of the Interrupt Expander buffer register can be transferred to the selected working register by a Sense command. After this transfer the buffer register is cleared. Modifications of the Sense command will be ignored as well as the commands Read, Write and Control.

3. INTERRUPT

Between two sense commands, the first of the external interrupt signals that goes to logical one will let the IXP 405 generate an interrupt signal to the RC 4000.
The following external interrupt signals will not cause new interrupt signals to the RC 4000, but will be registered in the buffer register as logical ones.



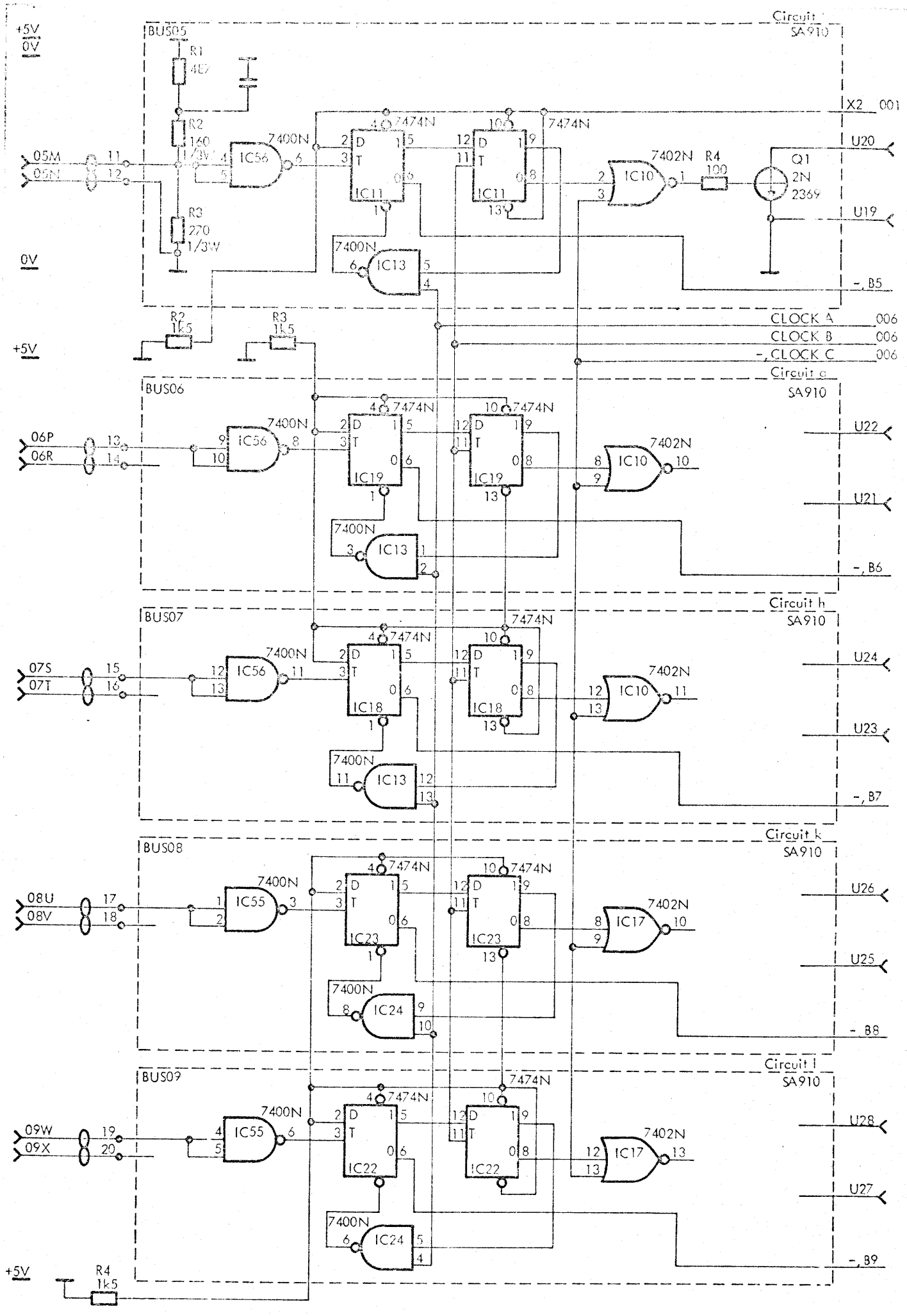
IXP406

(BUS00-04)

iXP001

V12114

PCBA Circuit Diagram



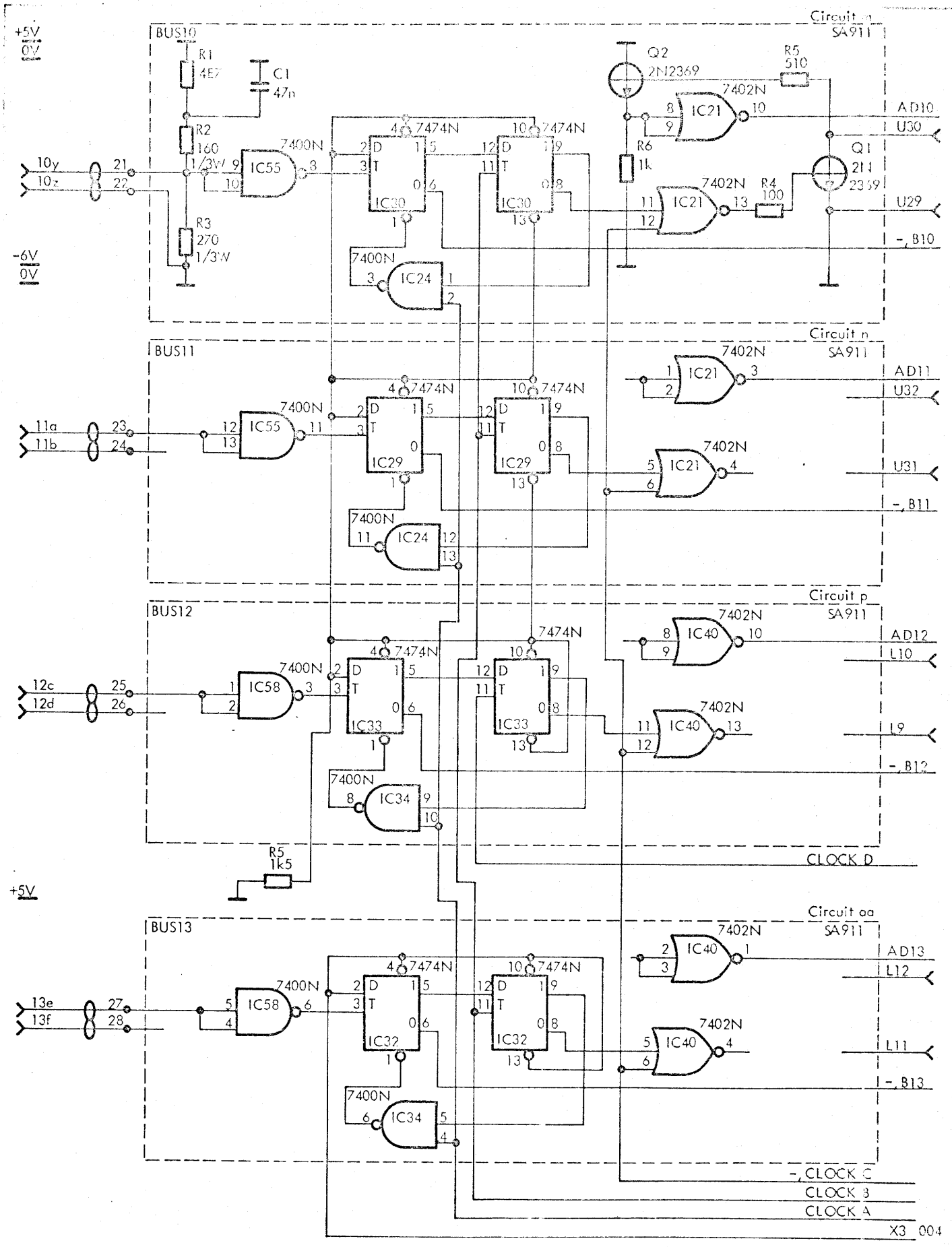
IXP406

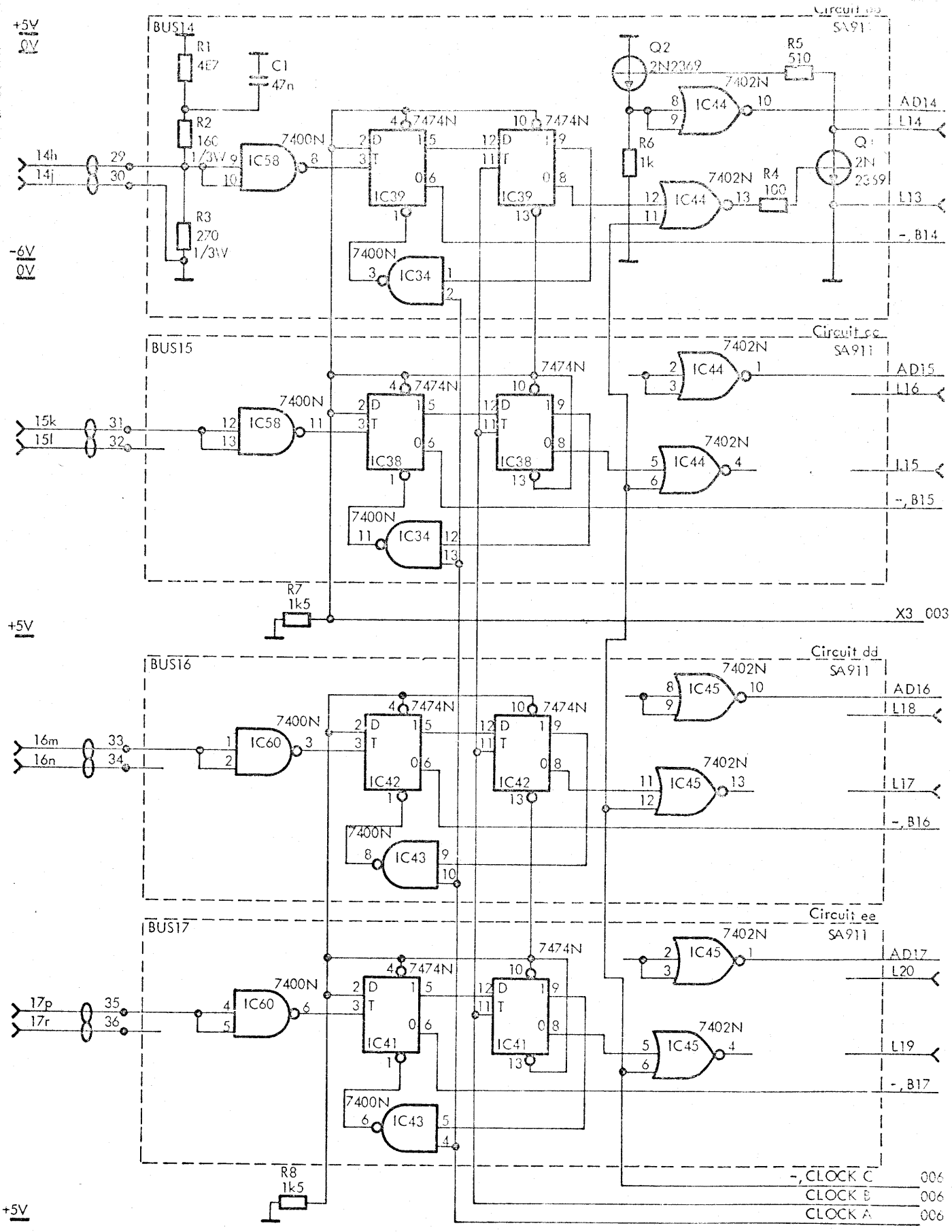
(BUS05-09)

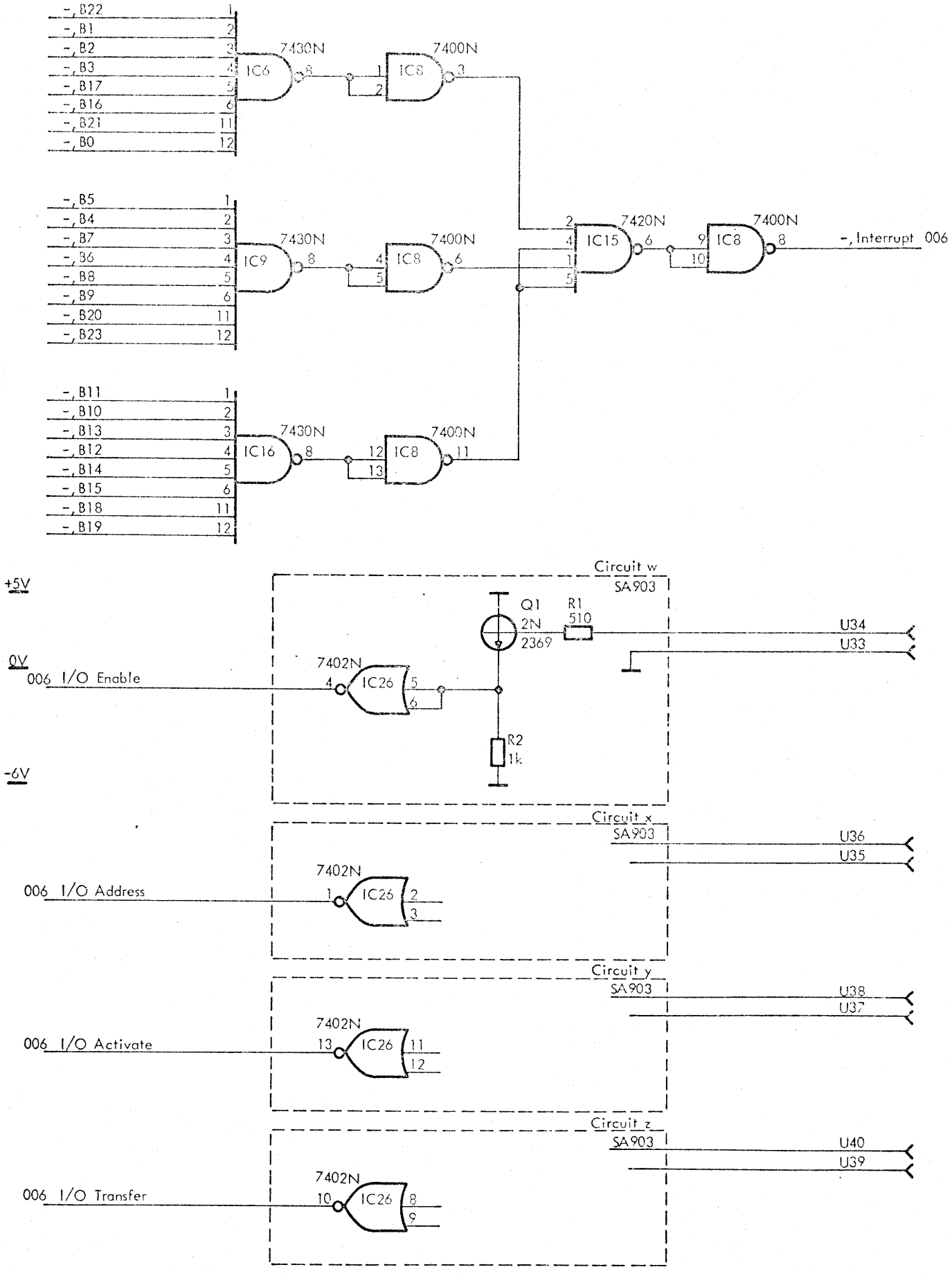
IXP002

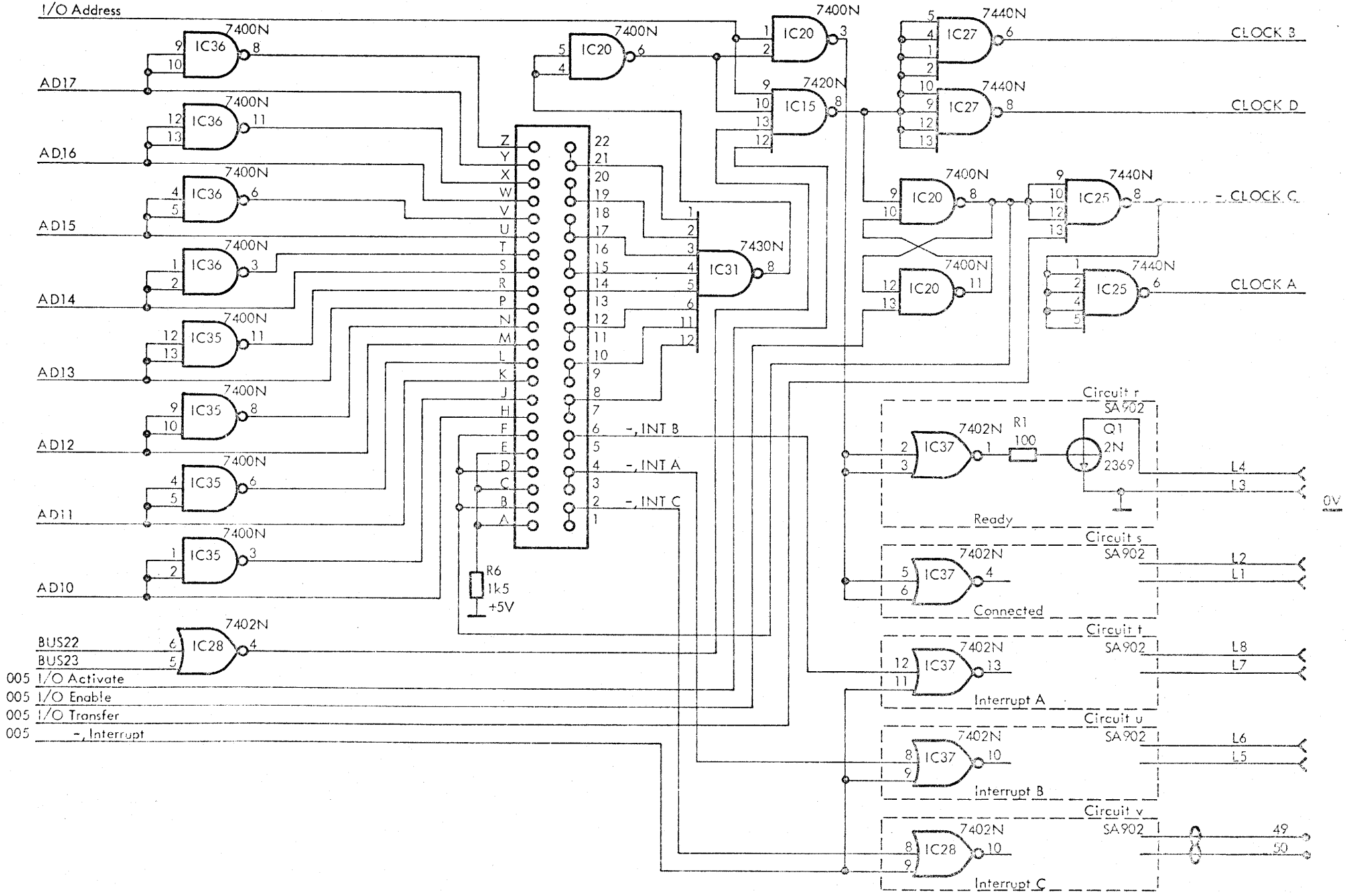
V12115

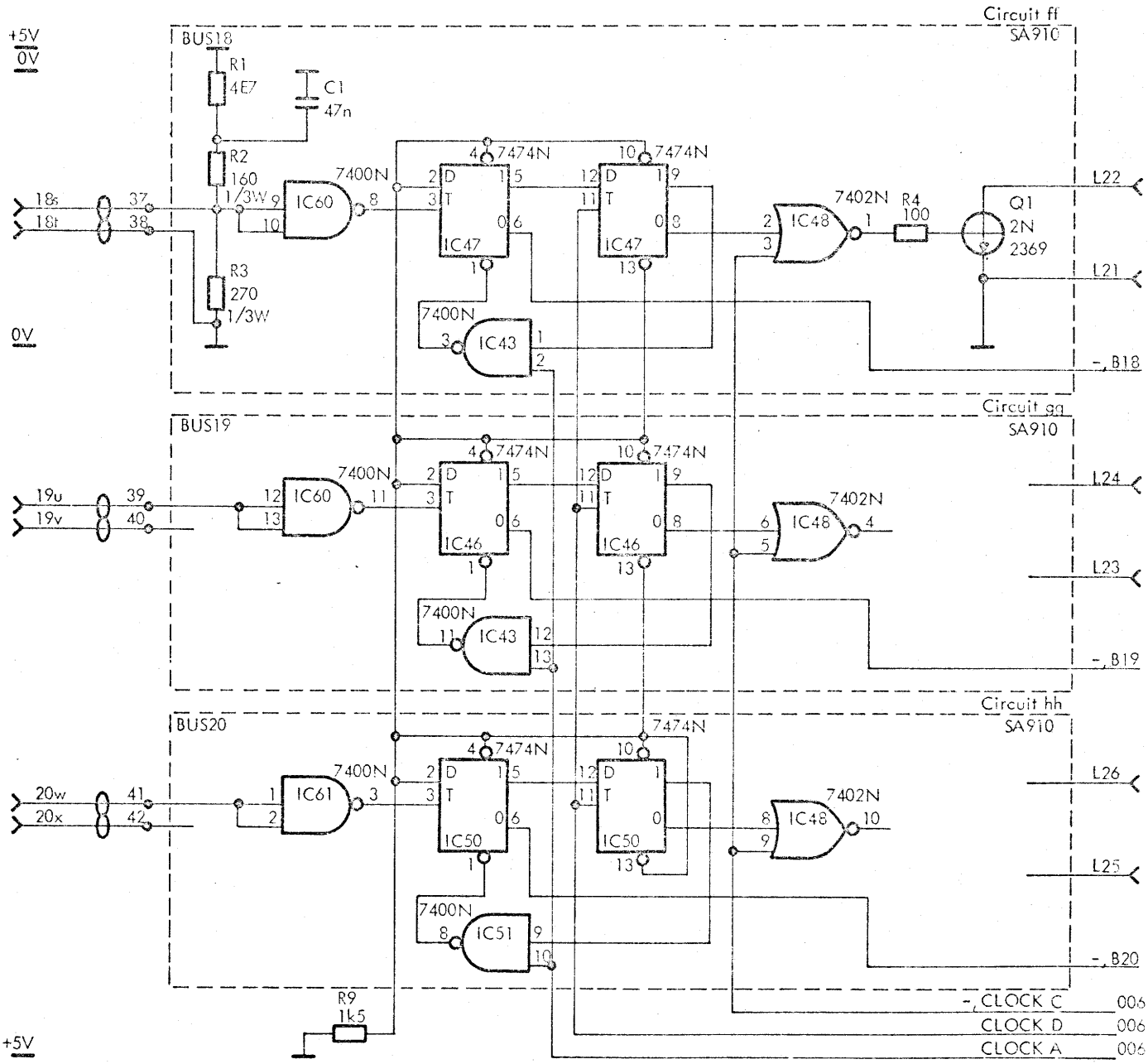
PCBA Circuit Diagram

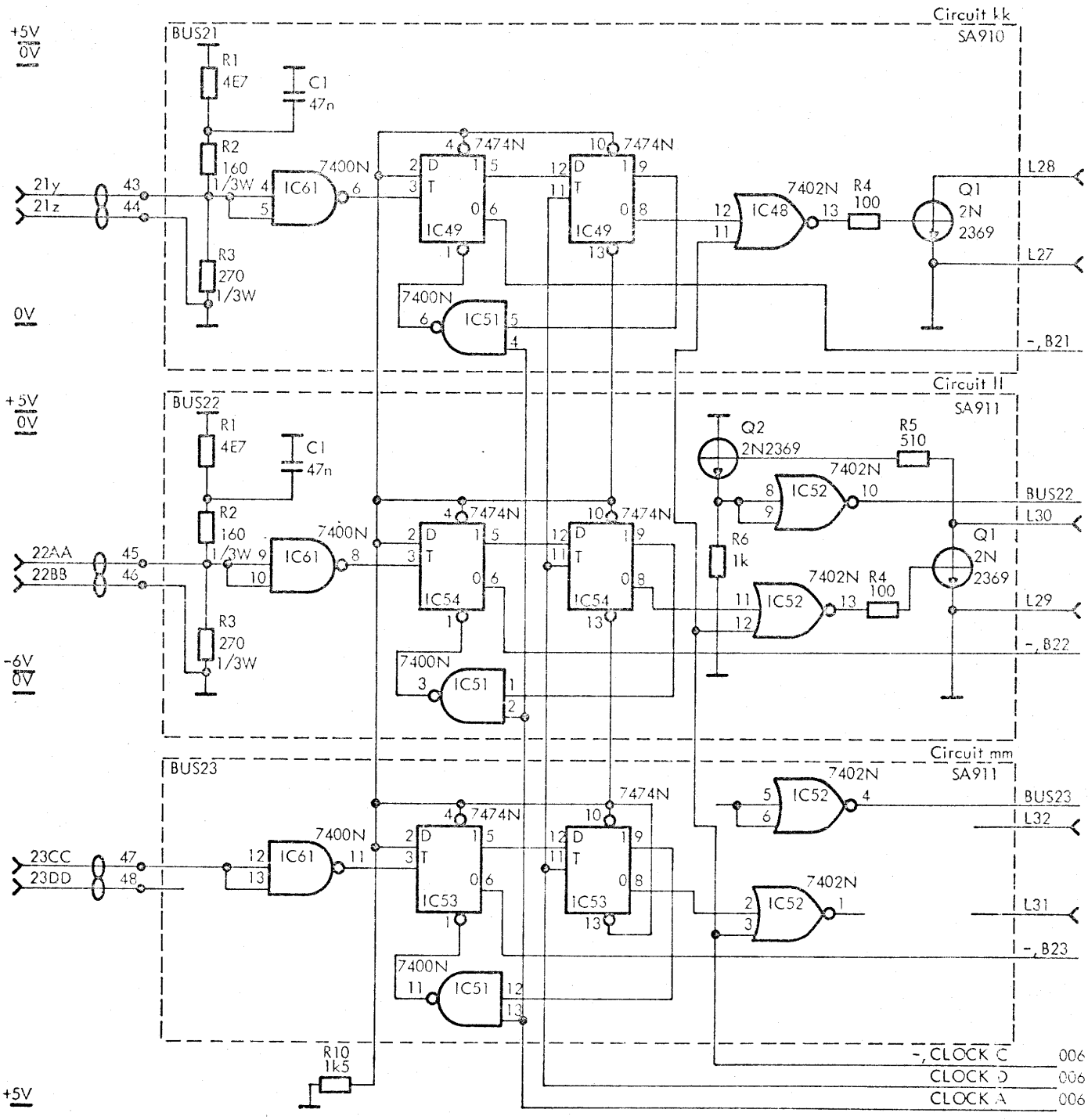

+5V
0V
-6V
0V
+5V
BUS10
BUS11
BUS12
BUS13
R1
4E7
C1
47n
R2
160
1/3W
R3
270
1/3W
R5
1k5
Q2
2N2369
Q1
2N2369
R5
510
R6
1k
R4
100
7400N
7474N
7402N
IC55
IC24
IC30
IC29
IC33
IC34
IC32
IC21
IC40
IC58
10y
10z
11a
11b
12c
12d
13e
13f
AD10
U30
U29
-,B10
AD11
U32
U31
-,B11
AD12
L10
L9
-,B12
AD13
L12
L11
-,B13
CLOCK D
-,CLOCK C
CLOCK B
CLOCK A
X3 004
Circuit n
SA911
Circuit p
SA911
Circuit aa
SA911

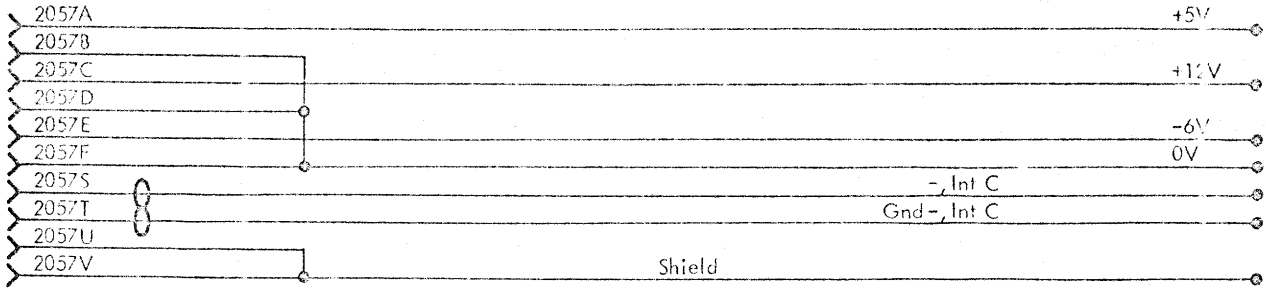

+5V
0V
BUS14
R1
4E7
C1
47n
R2
160
1/3W
R3
270
1/3W
-6V
0V
14h
14j
29
30
IC58
7400N
7474N
IC39
IC34
Q2
2N2369
R5
510
7402N
IC44
AD14
L14
R6
1k
R4
100
Q1
2N2369
L13
-, B14
Circuit cc
SA911
BUS15
15k
15l
31
32
IC38
AD15
L16
L15
-, B15
R7
1k5
X3 003
+5V
Circuit dd
SA911
BUS16
16m
16n
33
34
IC60
IC42
IC45
AD16
L18
L17
-, B16
Circuit ee
SA911
BUS17
17p
17r
35
36
IC41
IC43
AD17
L20
L19
-, B17
R8
1k5
+5V
-, CLOCK C
CLOCK B
CLOCK A
006
006
006

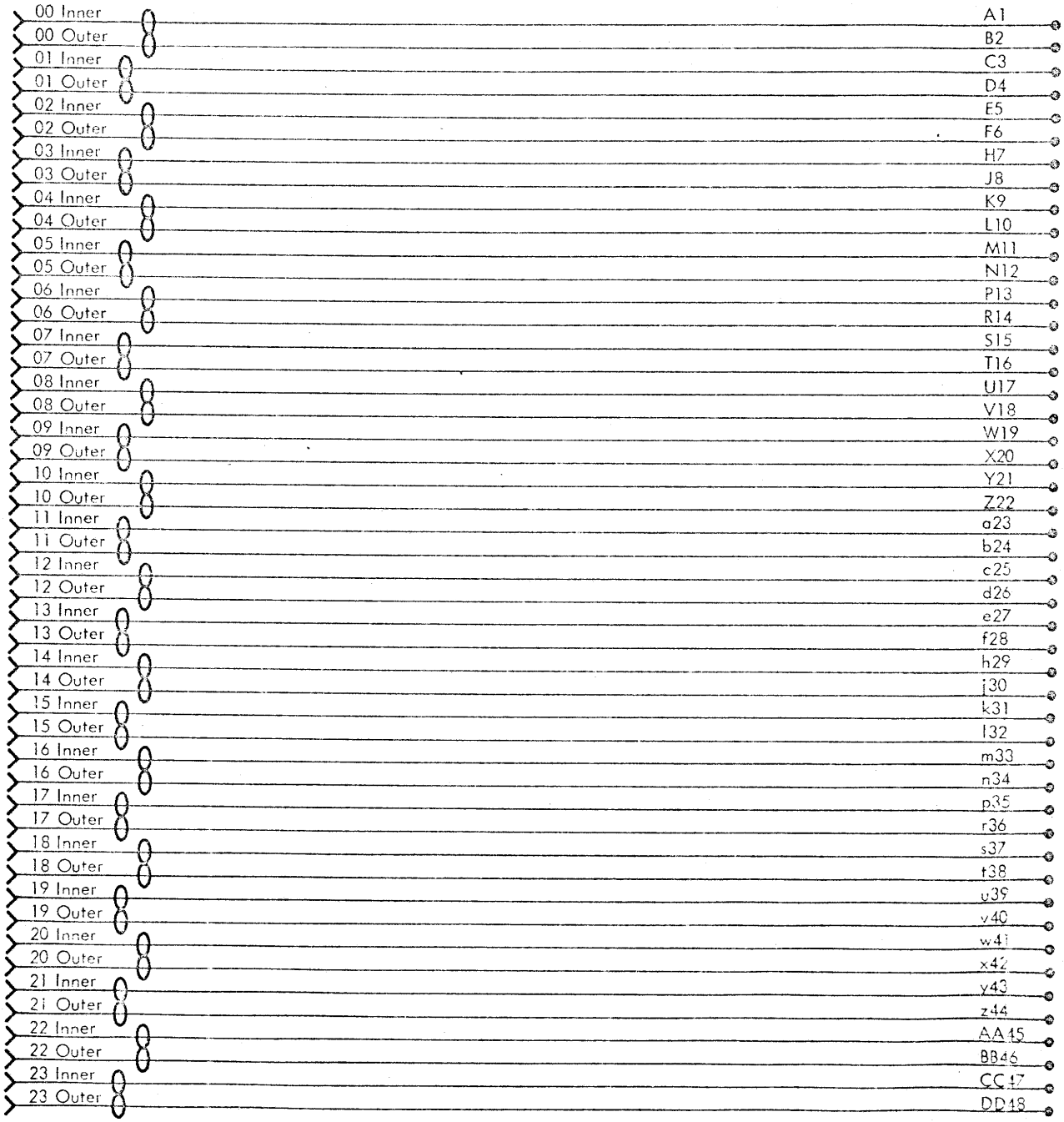

-, B22
-, B1
-, B2
-, B3
-, B17
-, B16
-, B21
-, B0
7430N
IC6
7400N
IC8
-, B5
-, B4
-, B7
-, B6
-, B8
-, B9
-, B20
-, B23
7430N
IC9
7400N
IC8
7420N
IC15
7400N
IC8
-, Interrupt 006
-, B11
-, B10
-, B13
-, B12
-, B14
-, B15
-, B18
-, B19
7430N
IC16
7400N
IC8
+5V
0V
-6V
006 I/O Enable
006 I/O Address
006 I/O Activate
006 I/O Transfer
7402N
IC26
Circuit w
SA903
Q1
2N
2369
R1
510
R2
1k
U34
U33
Circuit x
SA903
U36
U35
Circuit y
SA903
U38
U37
Circuit z
SA903
U40
U39


I/O Address
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
BUS22
BUS23
005 I/O Activate
005 I/O Enable
005 I/O Transfer
005 -, Interrupt
7400N
IC36
IC35
IC20
7402N
IC28
IC37
7420N
IC15
7430N
IC31
7440N
IC27
IC25
SA902
Z
Y
X
W
V
U
T
S
R
P
N
M
L
K
J
H
F
E
D
C
B
A
-, INT B
-, INT A
-, INT C
R6
1k5
+5V
R1
100
Q1
2N
2369
0V
CLOCK B
CLOCK D
- CLOCK C
CLOCK A
Circuit r
Circuit s
Circuit t
Circuit u
Circuit v
Ready
Connected
Interrupt A
Interrupt B
Interrupt C
L4
L3
L2
L1
L8
L7
L6
L5
49
50


Circuit ff
SA910
BUS18
+5V
0V
R1
4E7
C1
47n
R2
160
1/3W
R3
270
1/3W
IC60
7400N
IC47
7474N
IC43
IC48
7402N
R4
100
Q1
2N
2369
L22
L21
-, B18
Circuit gg
SA910
BUS19
IC46
L24
L23
-, B19
Circuit hh
SA910
BUS20
IC61
IC50
IC51
L26
L25
-, B20
R9
1k5
-, CLOCK C
CLOCK D
CLOCK A


Circuit kk
SA910
BUS21
+5V
0V
R1
4E7
C1
47n
R2
160
1/3W
R3
270
1/3W
21y
21z
43
44
IC61
7400N
IC49
7474N
IC48
7402N
R4
100
Q1
2N
2369
L28
L27
-, B21
Circuit ll
SA911
BUS22
Q2
2N2369
R5
510
R6
1k
IC52
IC54
22AA
22BB
45
46
L30
L29
-, B22
-6V
Circuit mm
SA911
BUS23
IC53
23CC
23DD
47
48
L32
L31
-, B23
R10
1k5
-, CLOCK C
CLOCK D
CLOCK A
006


2057A
2057B
2057C
2057D
2057E
2057F
2057S
2057T
2057U
2057V
+5V
+12V
-6V
0V
-, Int C
Gnd -, Int C
Shield


00 Inner
00 Outer
01 Inner
01 Outer
02 Inner
02 Outer
03 Inner
03 Outer
04 Inner
04 Outer
05 Inner
05 Outer
06 Inner
06 Outer
07 Inner
07 Outer
08 Inner
08 Outer
09 Inner
09 Outer
10 Inner
10 Outer
11 Inner
11 Outer
12 Inner
12 Outer
13 Inner
13 Outer
14 Inner
14 Outer
15 Inner
15 Outer
16 Inner
16 Outer
17 Inner
17 Outer
18 Inner
18 Outer
19 Inner
19 Outer
20 Inner
20 Outer
21 Inner
21 Outer
22 Inner
22 Outer
23 Inner
23 Outer
A1
B2
C3
D4
E5
F6
H7
J8
K9
L10
M11
N12
P13
R14
S15
T16
U17
V18
W19
X20
Y21
Z22
a23
b24
c25
d26
e27
f28
h29
j30
k31
l32
m33
n34
p35
r36
s37
t38
u39
v40
w41
x42
y43
z44
AA45
BB46
CC47
DD48

DIGITAL OUTPUT TERMINALS, DOT401 THRU 404

Digital Output Terminals, DOT401 thru 404, are 24-bit, buffered digital output units for RC 4000.
These are placed in chassis CHS404 and are connected to the Low-Speed Data Channel via Busline Converter, BCV401.
Data are transferred from the W-register to the buffer register of an Digital Output Terminal by means of a Write command as determined by the process programm in progress.
The Digital Output Terminals are equipped with various types of output circuitries controlled by the buffer register outputs as given by the specifications.

DOT402 and 404 are not ready during the output pulse and a predetermined time after the end of the pulse. For these two versions an interrupt-signal will be generated when the device becomes ready. The timing circuitries are common for all 24 bits.

Application:	Relay or alarm-lamp driving in industrial process control.

Specifications:

DOT401 thru 404:

Selection:	I/O instruction with predetermined device address.
Number of Outputs:	24
Type of Outputs for a 1 transferred from W-register:	DOT401: 2-wire, static voltage output for floating loads, 12 V (other voltages optional), max. 4.8A totally per 24 bits.

Type of Outputs for a 1 transferred from W-register (cont'd):

DOT402: 2-wire, single pulse voltage output for floating loads, 12 V (other voltages optional) max. 4.8A totally per 24 bits.

DOT403: 2-wire, static contact closure output for non-floating loads.

DOT404: 2-wire, single pulse contact closure output for non-floating loads.

Contact Specifications:

Type:	Isolated transistor switch
Ratings:	
Max. Current, dc:	0.5 A
Max. Current, peak:	1.0 A
Max. nom. lamp current (no preheating):	0.15 A
Abs. max. supply voltage:	60 V DC
Max. common mode voltage (403 and 404 only):	250 V RMS
Max. load inductance switched at max. current:	4 Hy
Max. repetition frequency at max. inductance and max. current:	1 Hz
Max. repetition frequency at max. current and non-inductive load:	100 Hz

Characteristics:

On voltage drop at 0.5 A:	0.4 V max.
Turn-on time:	0.02 ms typ.
Turn-off time:	1.0 ms typ.
Pulse duration (402 and 404 only):	1 - 1000 ms
Wait time (402 and 404 only):	1 - 1000 ms
Dimensions:	Height: 355 mm Width: 24 mm Depth: 450 mm
Supply Power:	+ 5 V ± 5 per cent, 1.3 A + 12 V ± 5 per cent, 1.0 A - 6 V ± 5 per cent, 250 mA + 12 V ± 5 per cent, (DCF401 and 402 only), 4.8 A (other voltages optional)
Ambient Air:	Temperature 0 to 45 degrees C Relative Humidity: 30 to 70 per cent
Weight:	1.2 kg

RCSL: 51-VB489
Author: V. Toft Pedersen
Edited: July 1969

RC 4000 PERIPHERAL DEVICES

DOT401, 402, 403 AND 404 DIGITAL OUTPUT TERMINAL

PRELIMINARY SPECIFICATIONS

ABSTRACT:

This report describes the logic structure of the Digital Output Terminal DOT401, 402, 403 and 404, when used in connection with the RC 4000 Computer.

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Copenhagen F.

Main Characteristics:

The Digital Output Terminal is designed to apply 24 digital signals to external equipment e.g. actuators, lamps etc. in industrial process control.

The Digital Output Terminal includes a 24 bits buffer register which controls 24 output amplifiers.

For DOT401 and DOT403 the state of the output amplifiers is steady and equal to the actual states of buffer register elements. Updating of the buffer register can take place at any time as determined by the process program in progress as the device always will be in the ready state.

For DOT402 and DOT404 the state of the output amplifiers is equal to the actual states of the buffer register element in a limited time interval after an updating of the buffer register has taken place. During this time interval the device is not ready. When this interval is terminated the device will go to the ready state and all the output amplifiers will go to the 0-state.

The time interval can be selected within the range of 1 ms thru 1000 ms.

Commands:

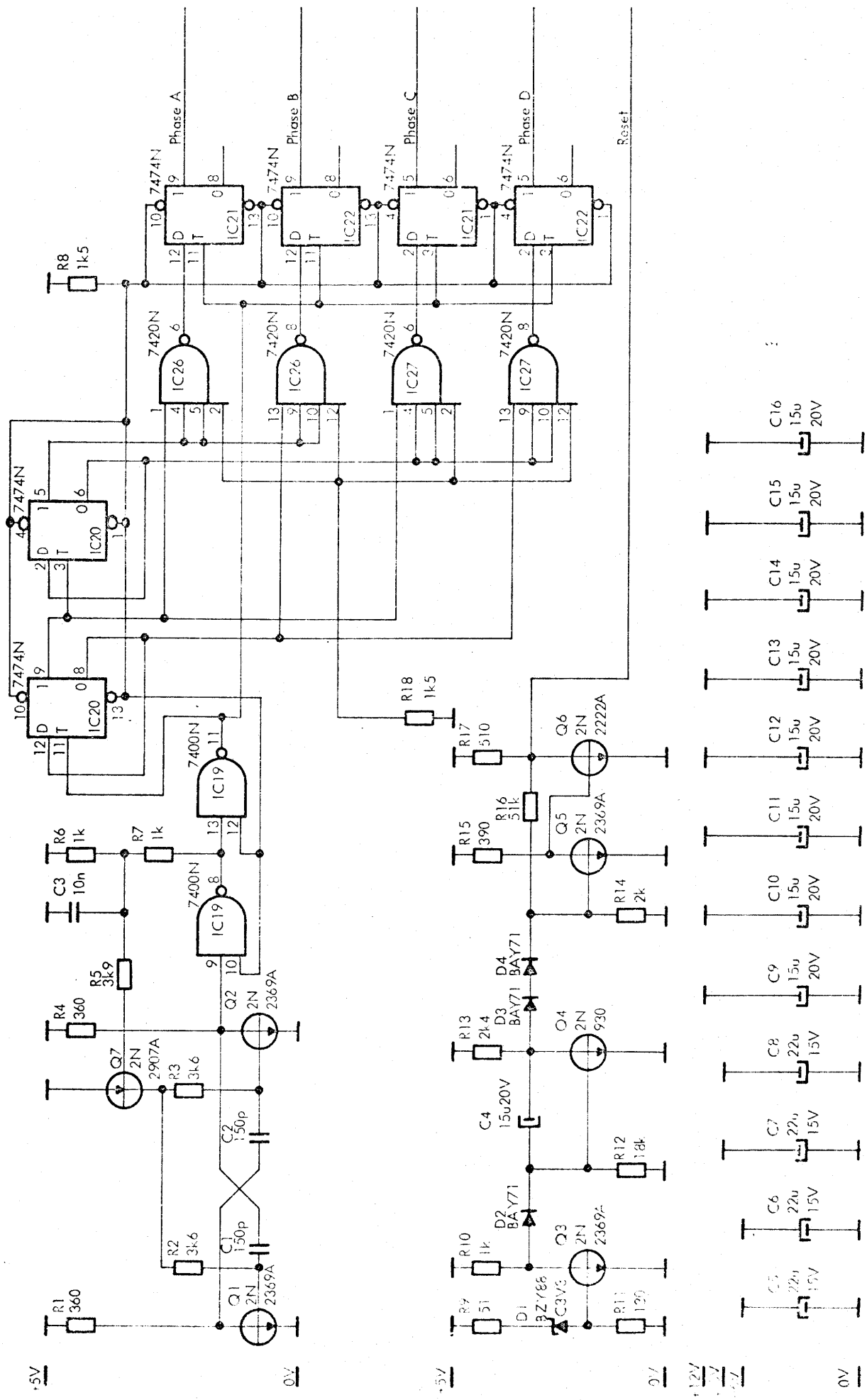
The contents of the selected working register can be transferred to the Digital Output Terminal by a Write command.

Modifications of the Write command will be ignored as well as the commands Sense, Read and Control.

Interrupt:

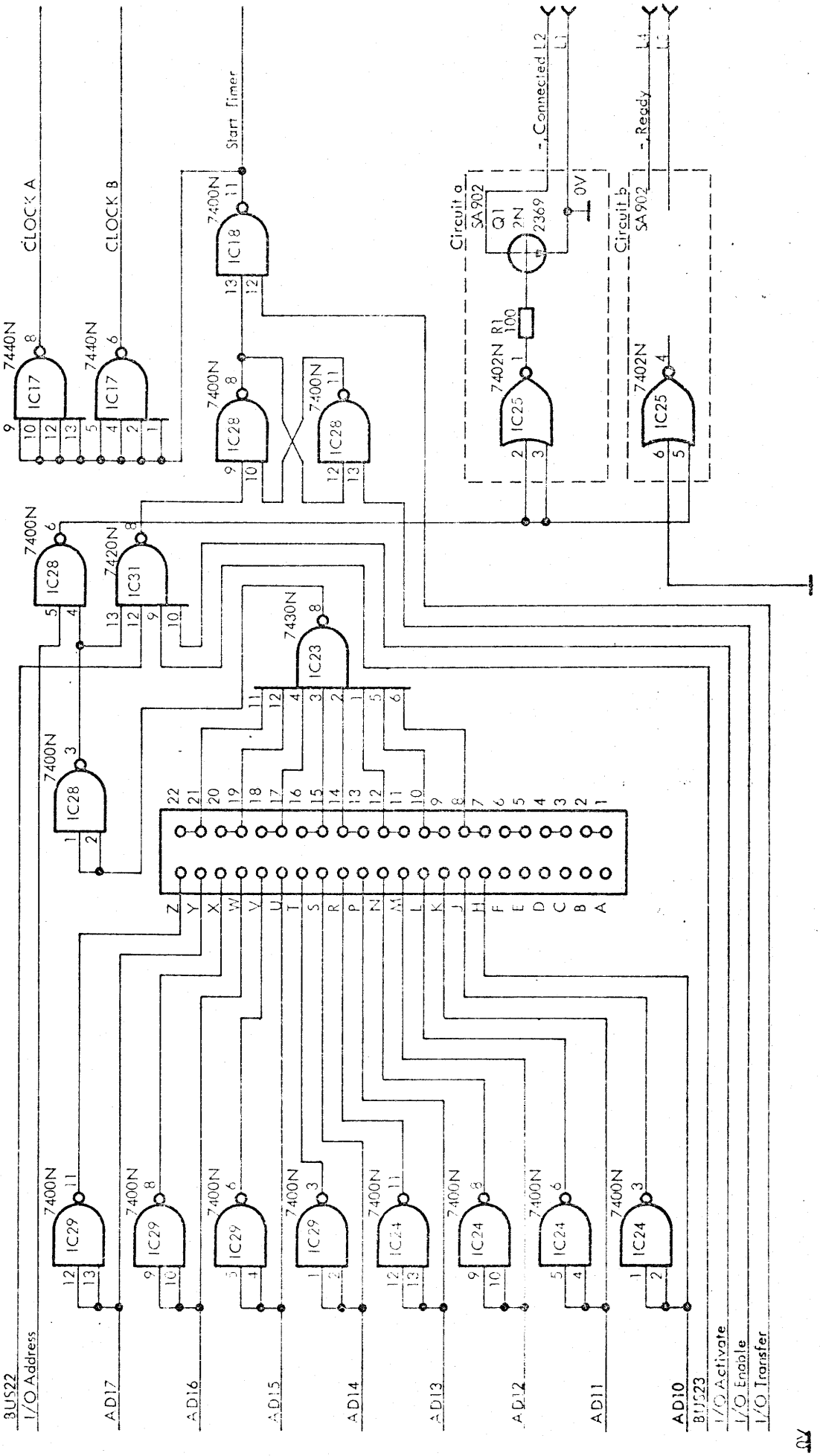
The Digital Output Terminal versions DOT402 and DOT404 will generate an interrupt signal when the device becomes ready.

The versions DOT401 and DOT403 will not generate any interrupt signals.



DOT 403 TIMING PULSE GENERATOR AND POWER START-UP CIRCUIT DOT00

V12566 PCBA Circuit Diagram



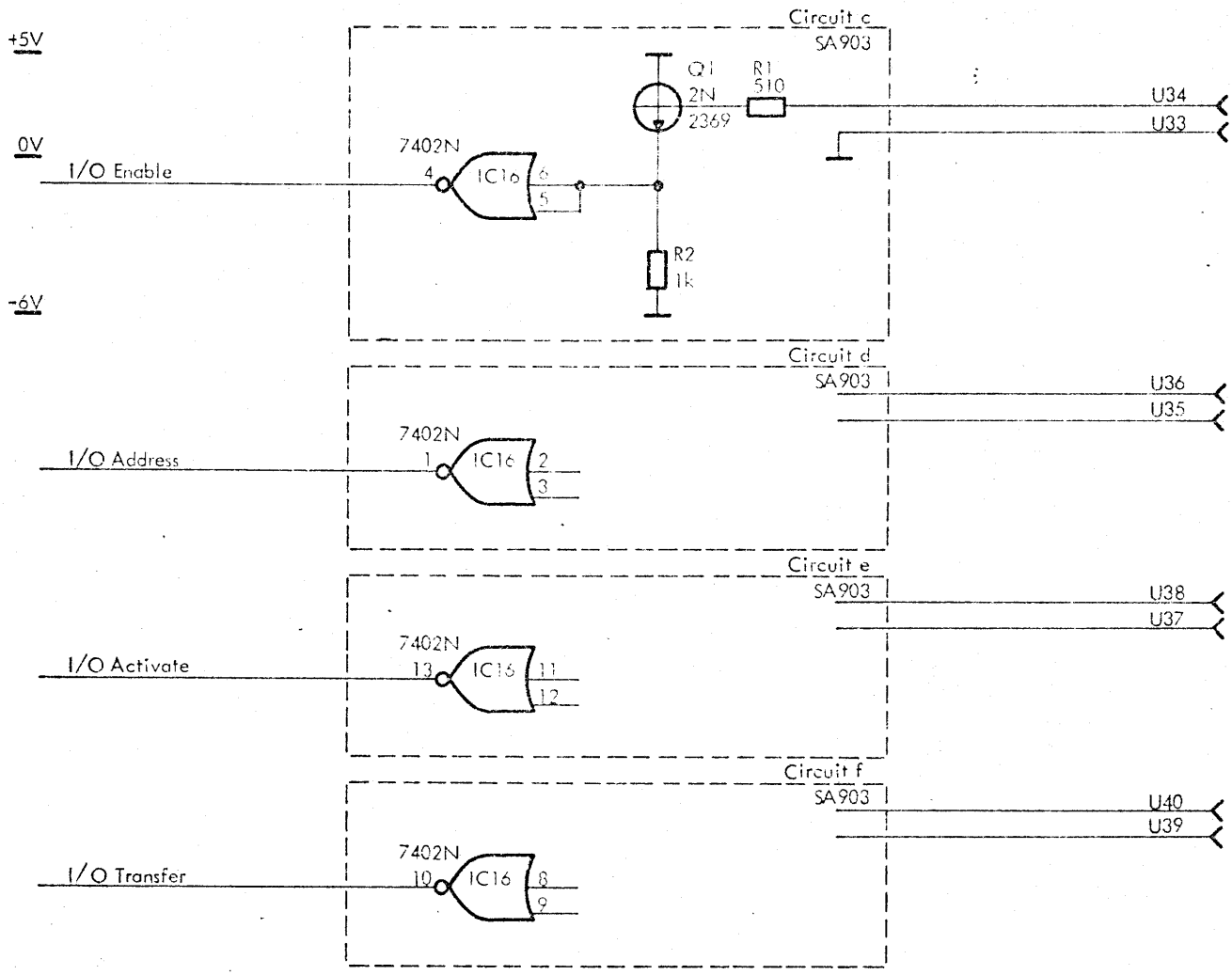
DOT 403

ADDRESS DECODING, READY, CONNECTED AND INTERRUPT GENERATOR

DOT00

V12528

PCBA Circuit Diagram



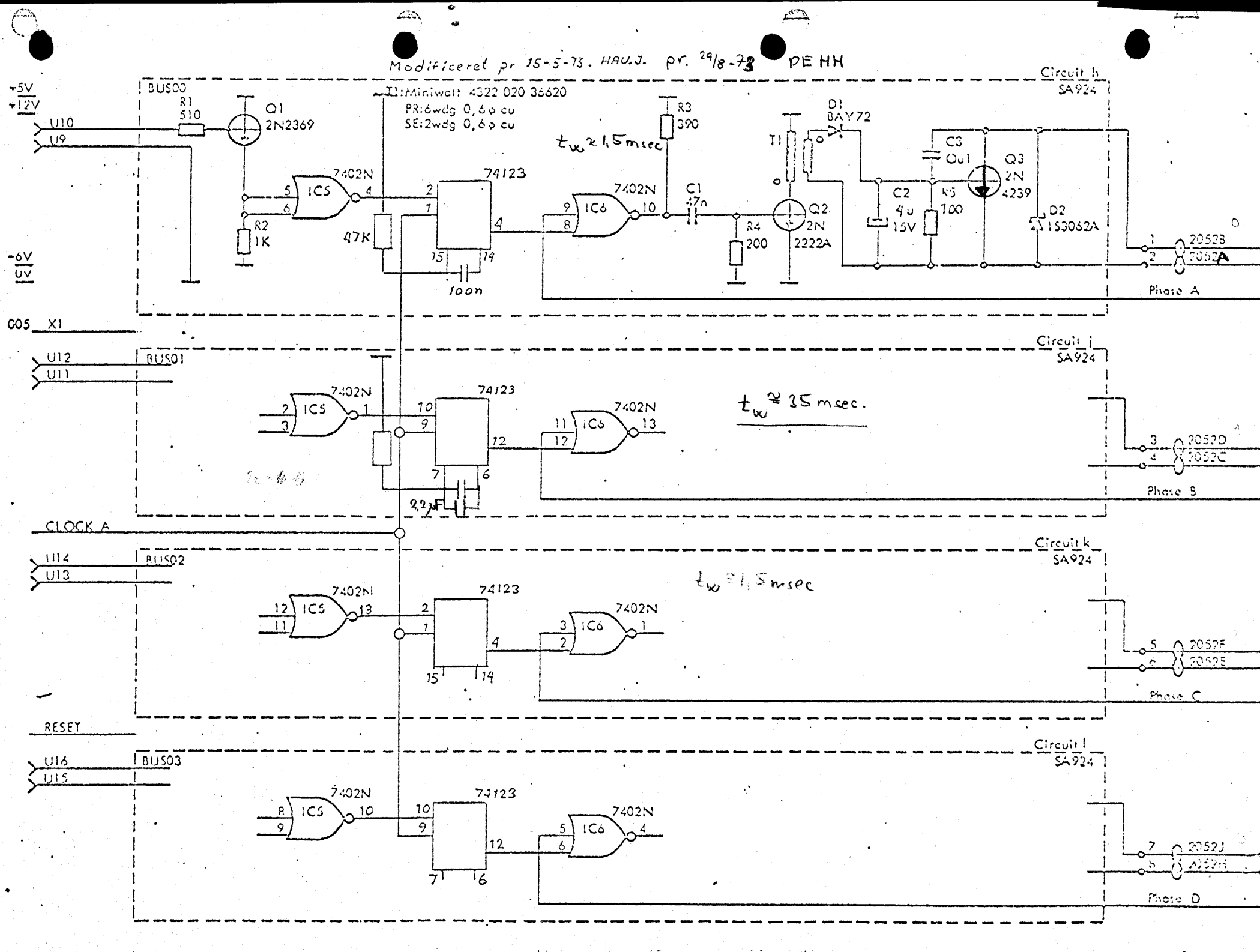
DOT 403

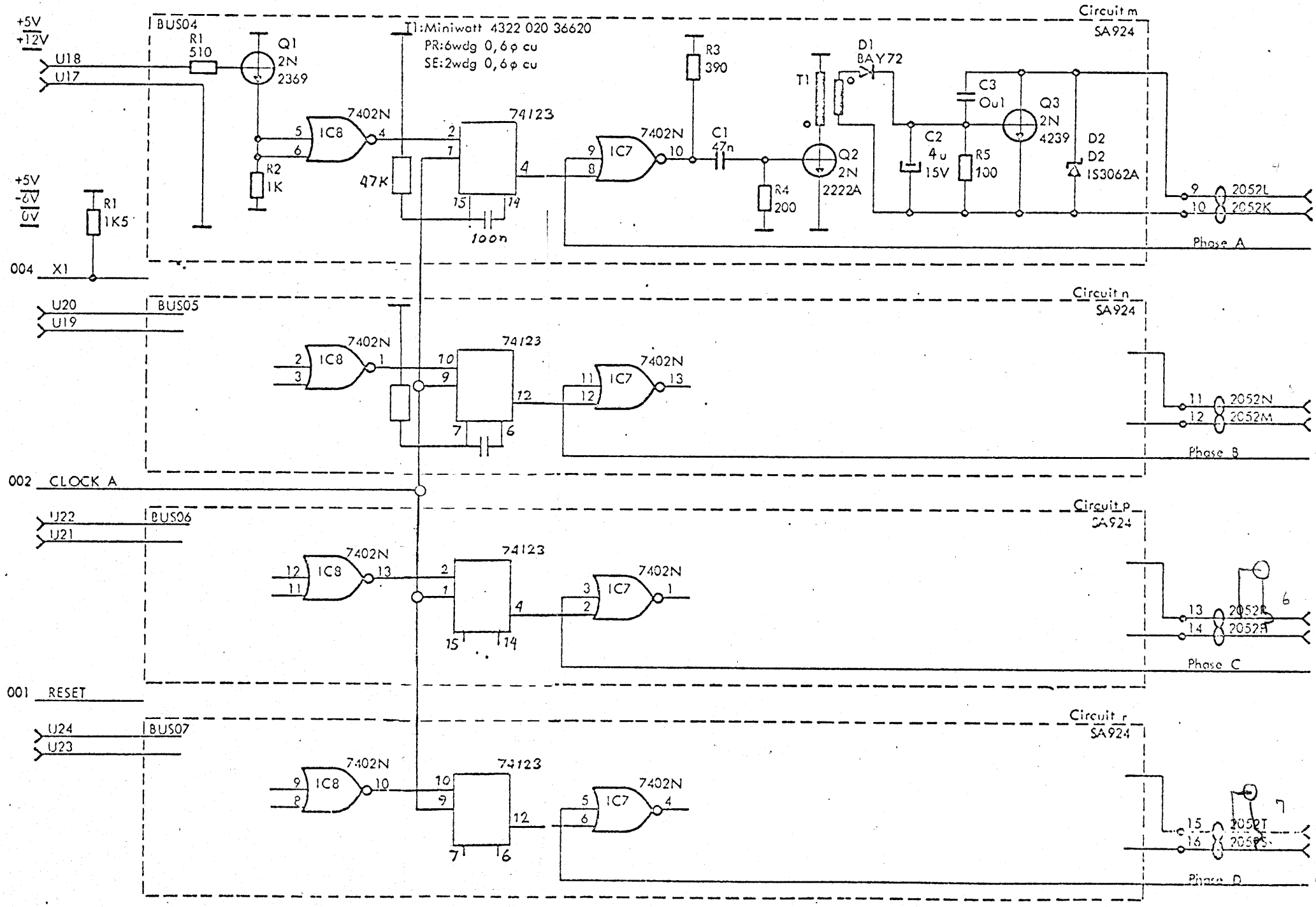
RECEIVERS FOR I/O BUS CONTROL SIGNALS

DOT003

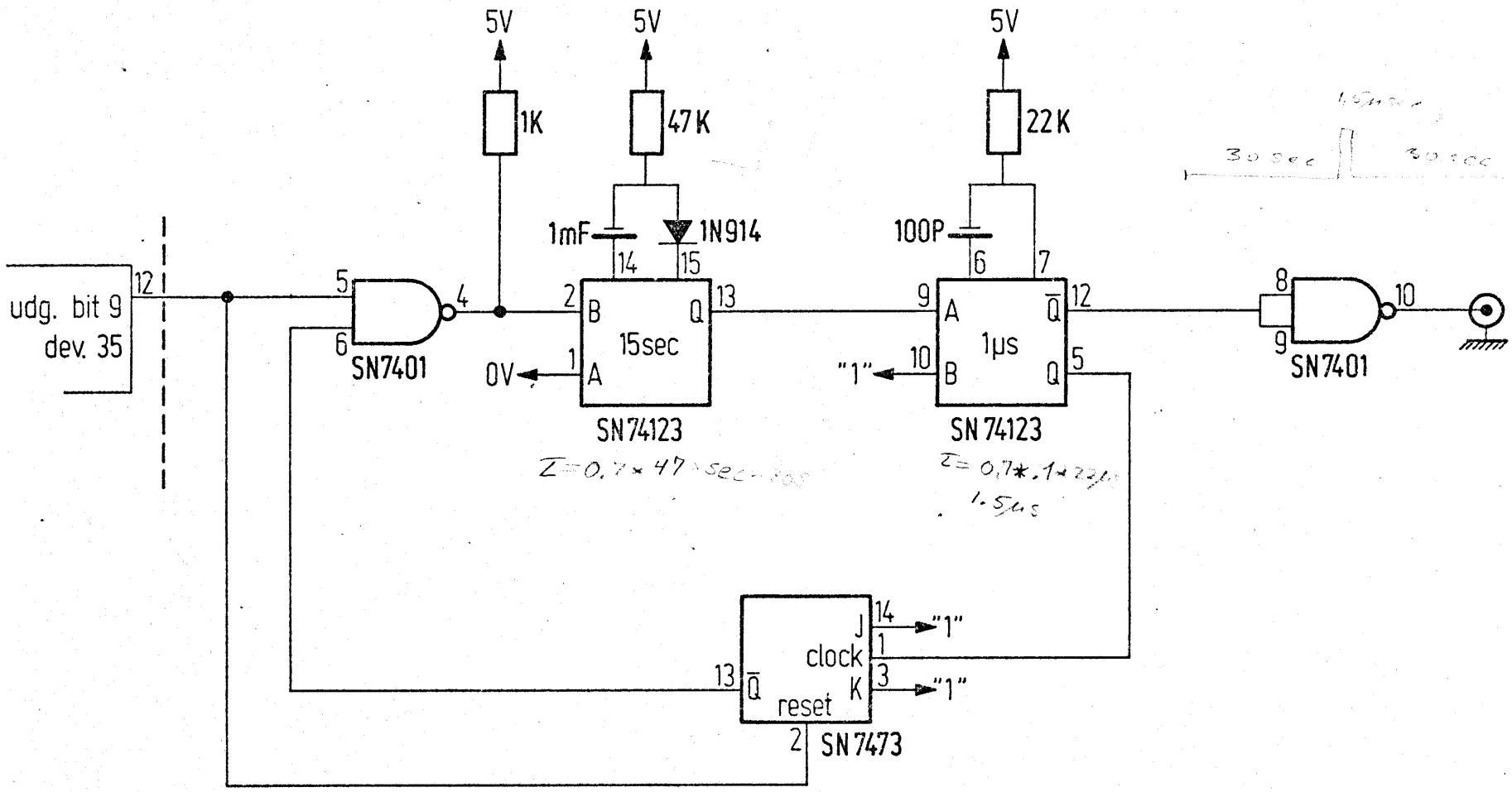
V12529

PCBA Circuit Diagram

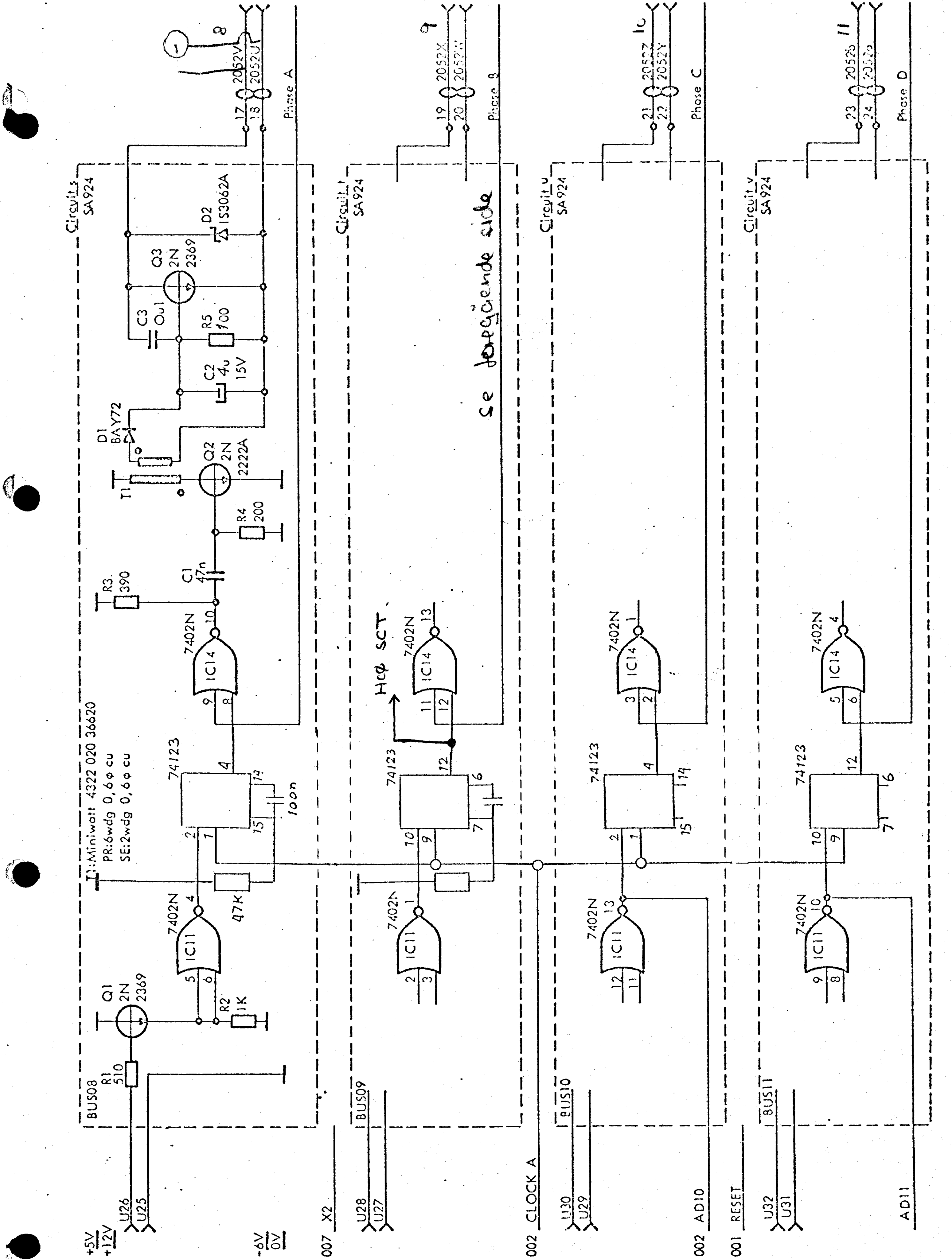

Modificeret pr 15-5-73. HAU.J. pr. 29/8-73 PE HH
V12530
DOT 403 M
PCBA Circuit Diagram
(BUS00-03)
DOT004
+5V
+12V
-6V
UV
BUS00
U10
U9
R1 510
Q1 2N2369
R2 1K
IC5 7402N
47K
74123
100n
T1: Miniwatt 4322 020 36620
PR: 6wdg 0,6 ø cu
SE: 2wdg 0,6 ø cu
R3 390
tw ≈ 1,5 msec
IC6 7402N
C1 47n
R4 200
Q2 2N 2222A
T1
D1 BAY72
C2 4u 15V
R5 100
C3 Out
Q3 2N 4239
D2 1S3062A
Circuit h SA924
2052B
2052A
Phase A
005 X1
U12
U11
BUS01
tw ≈ 35 msec.
Circuit i SA924
2052D
2052C
Phase B
CLOCK A
U14
U13
BUS02
tw ≈ 1,5 msec
Circuit k SA924
2052F
2052E
Phase C
RESET
U16
U15
BUS03
Circuit l SA924
2052J
2052H
Phase D



Modifié le 15-5-73 : HHU


5V
5V
5V
1K
47K
22K
1mF
1N914
100P
udg. bit 9
dev. 35
12
5
6
4
SN7401
2
B
Q
13
15sec
1
A
0V
SN74123
9
A
Q
12
10
B
Q
5
1µs
"1"
SN74123
8
10
9
SN7401
14
15
6
7
J
clock
K
reset
14
1
3
2
13
Q
"1"
"1"
SN7473

20/9-73 PEH



DOT 403 M

(BUS08-11)

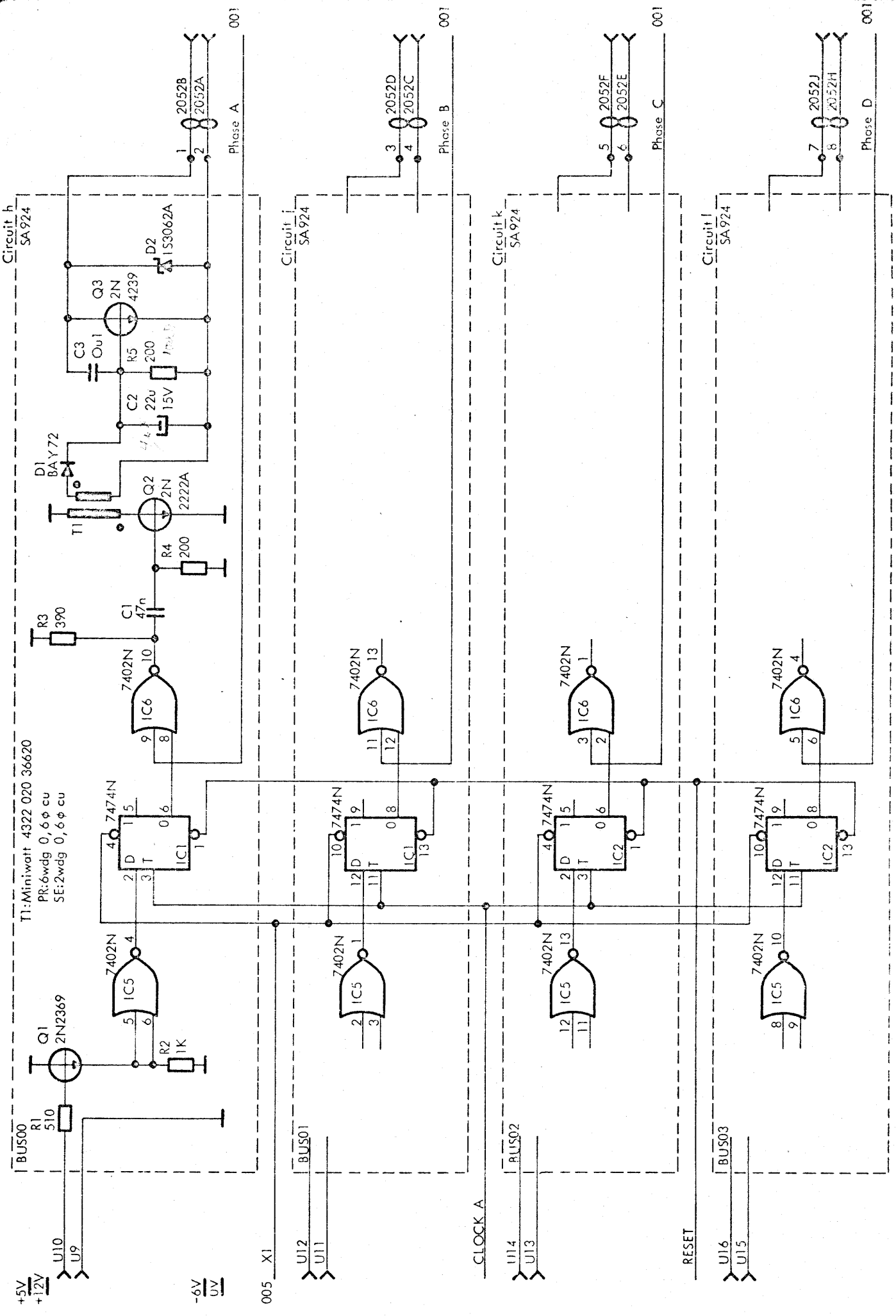
DOT006

V12532

PCBA Circuit Diagram

Modificeret 30/8-73 PBN

Modificeret 15-5-73 HAL



DOT 403

(BUS00-03)

DOT004

V12530

PCBA Circuit Diagram

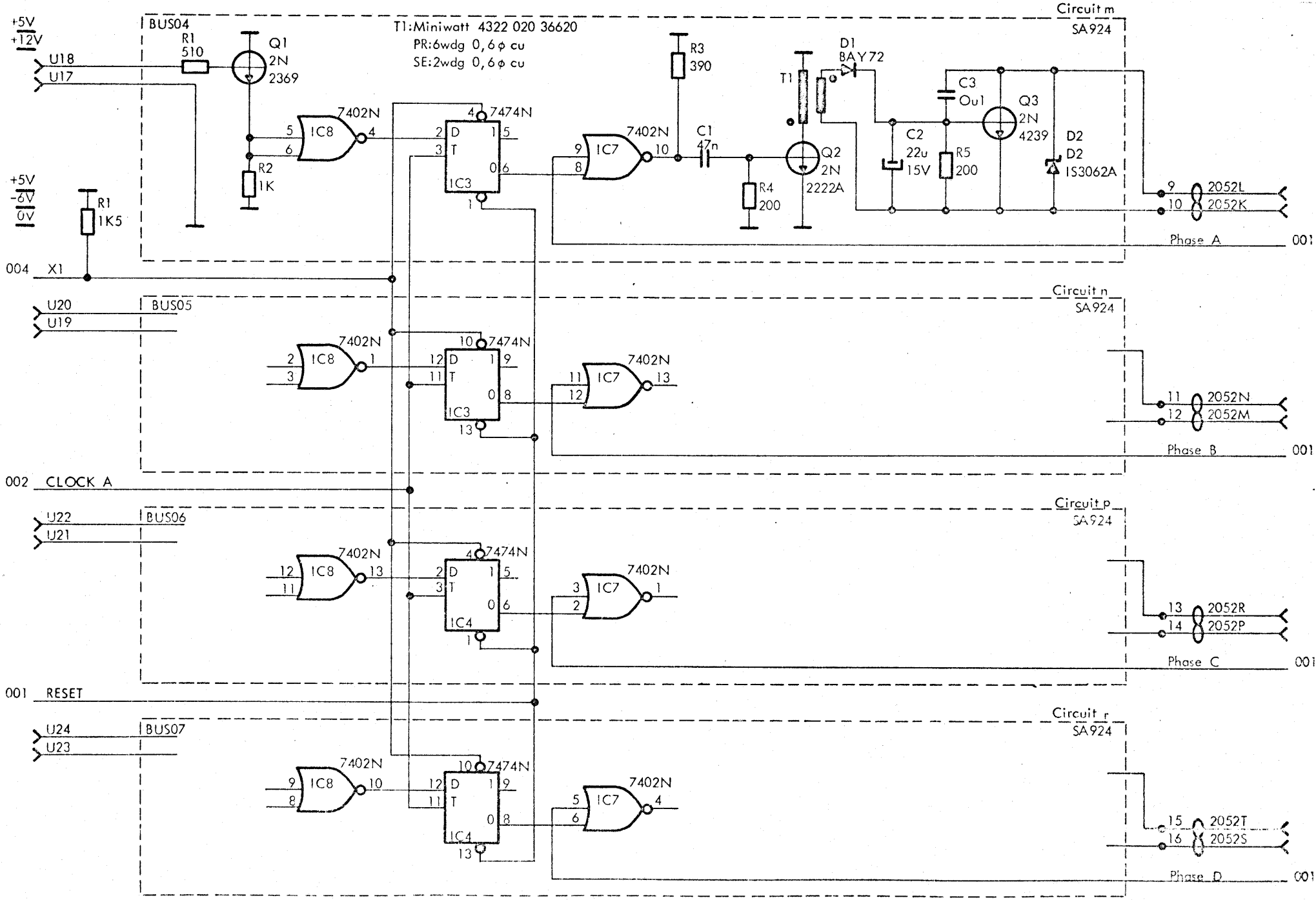
V12531

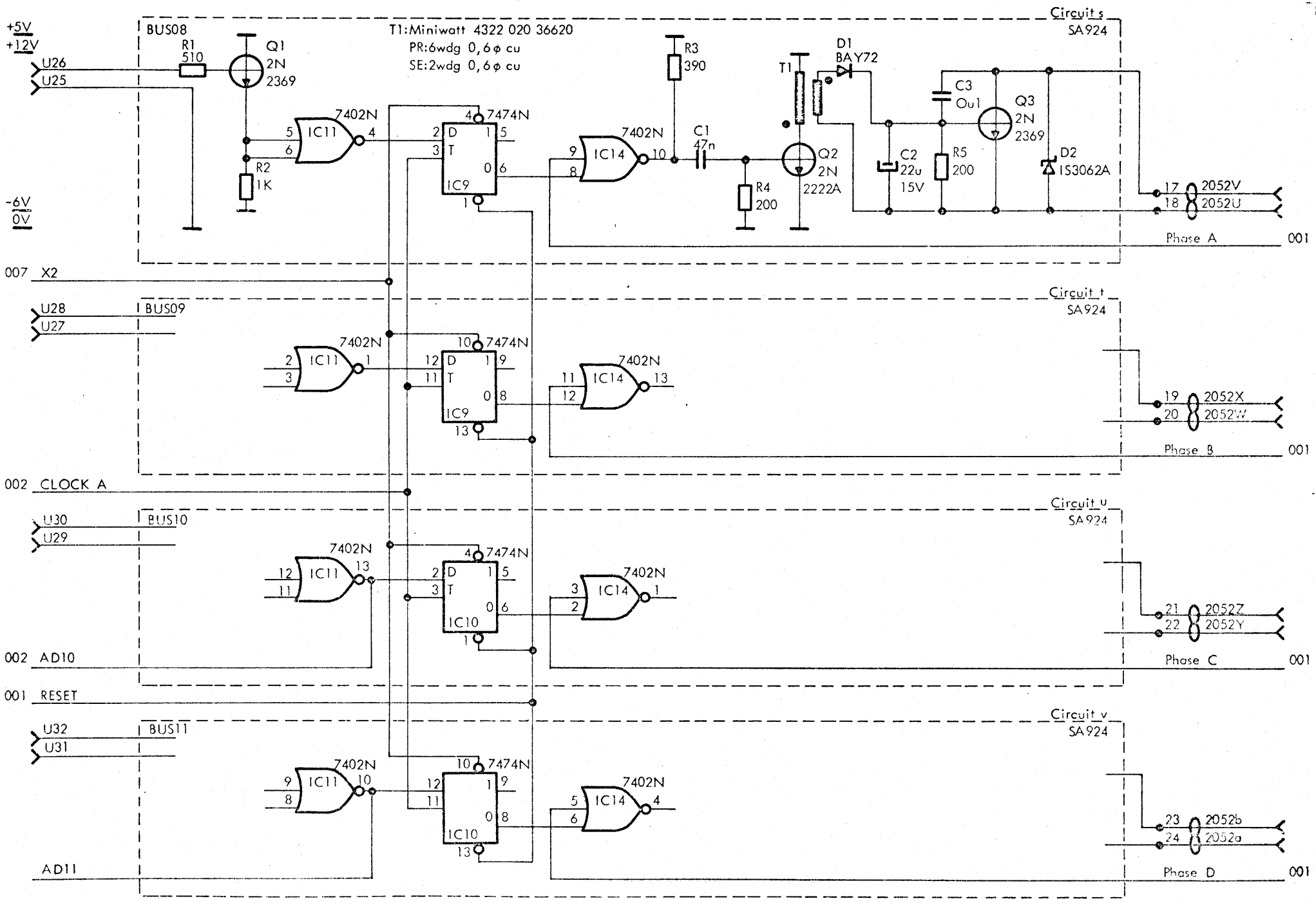
DOT 403

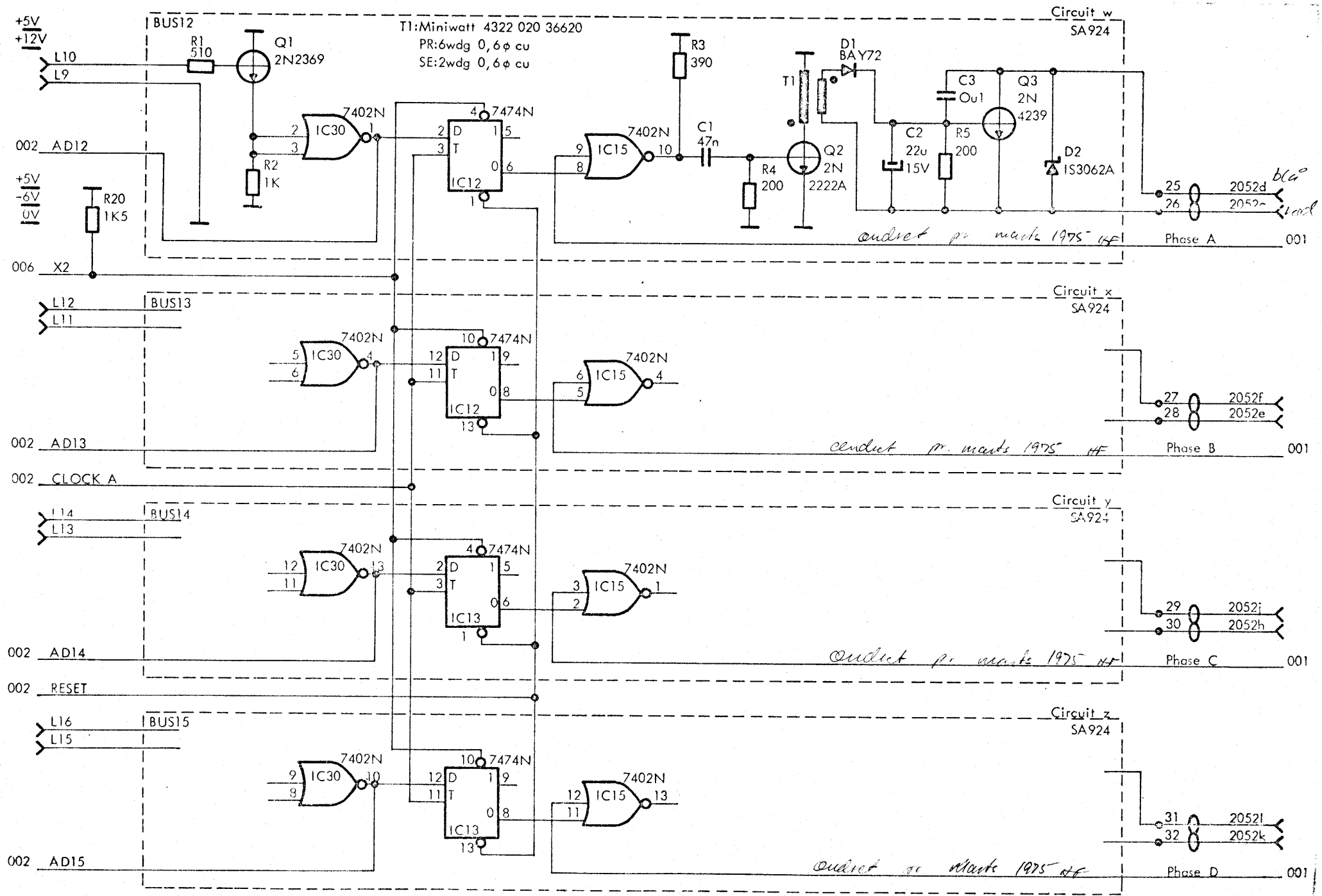
PCBA Circuit Diagram

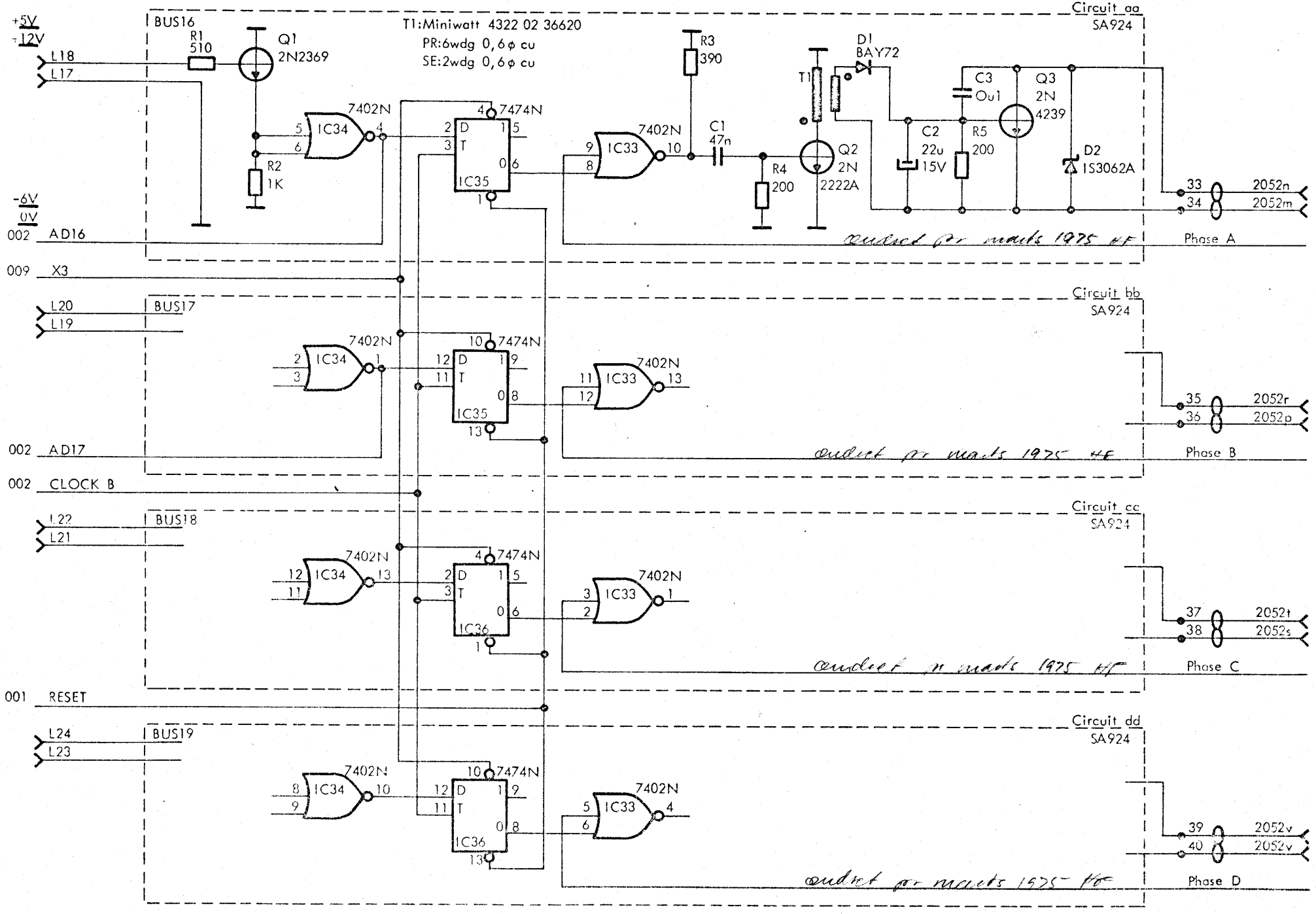
(BUS04-07)

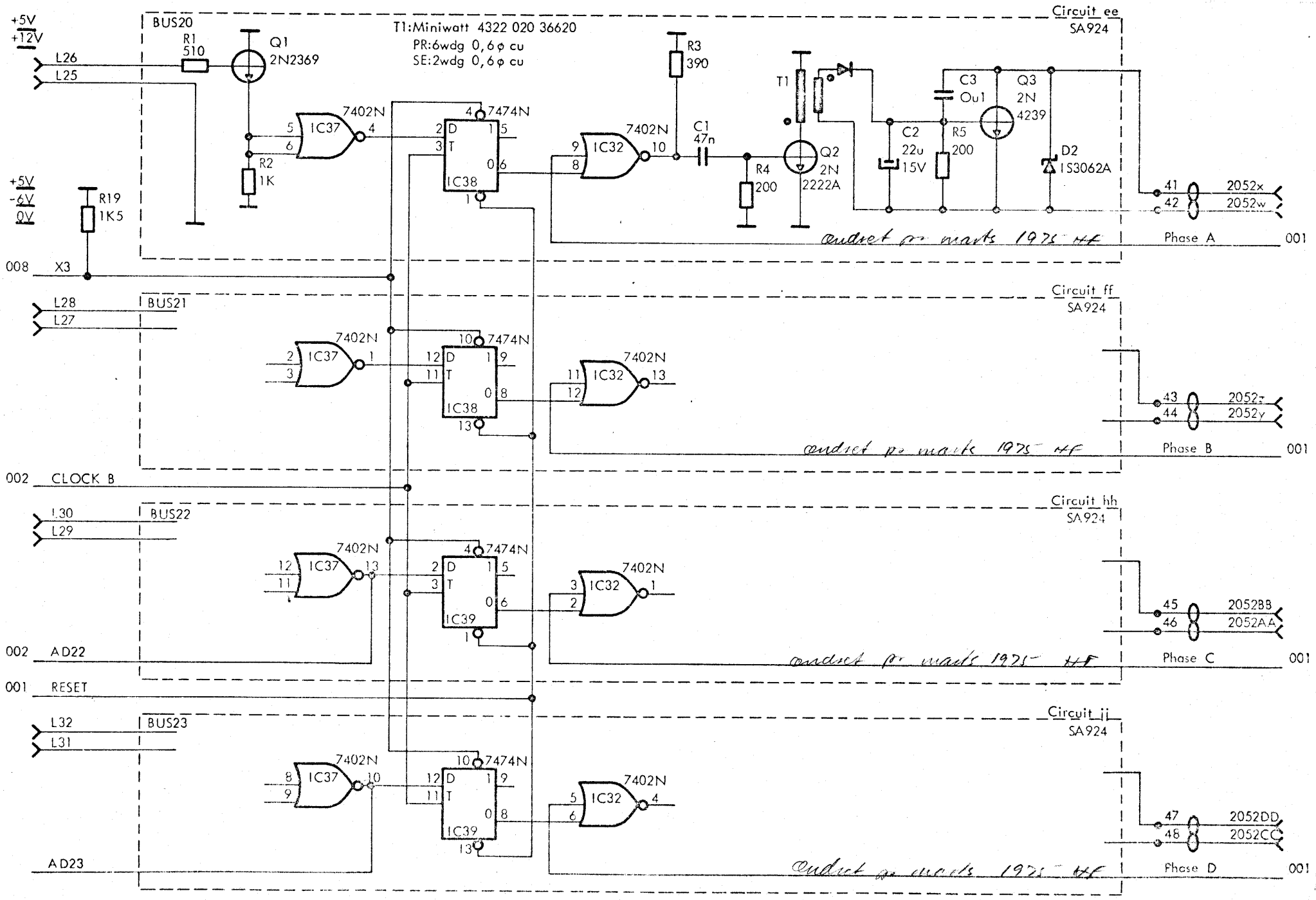
DOT005

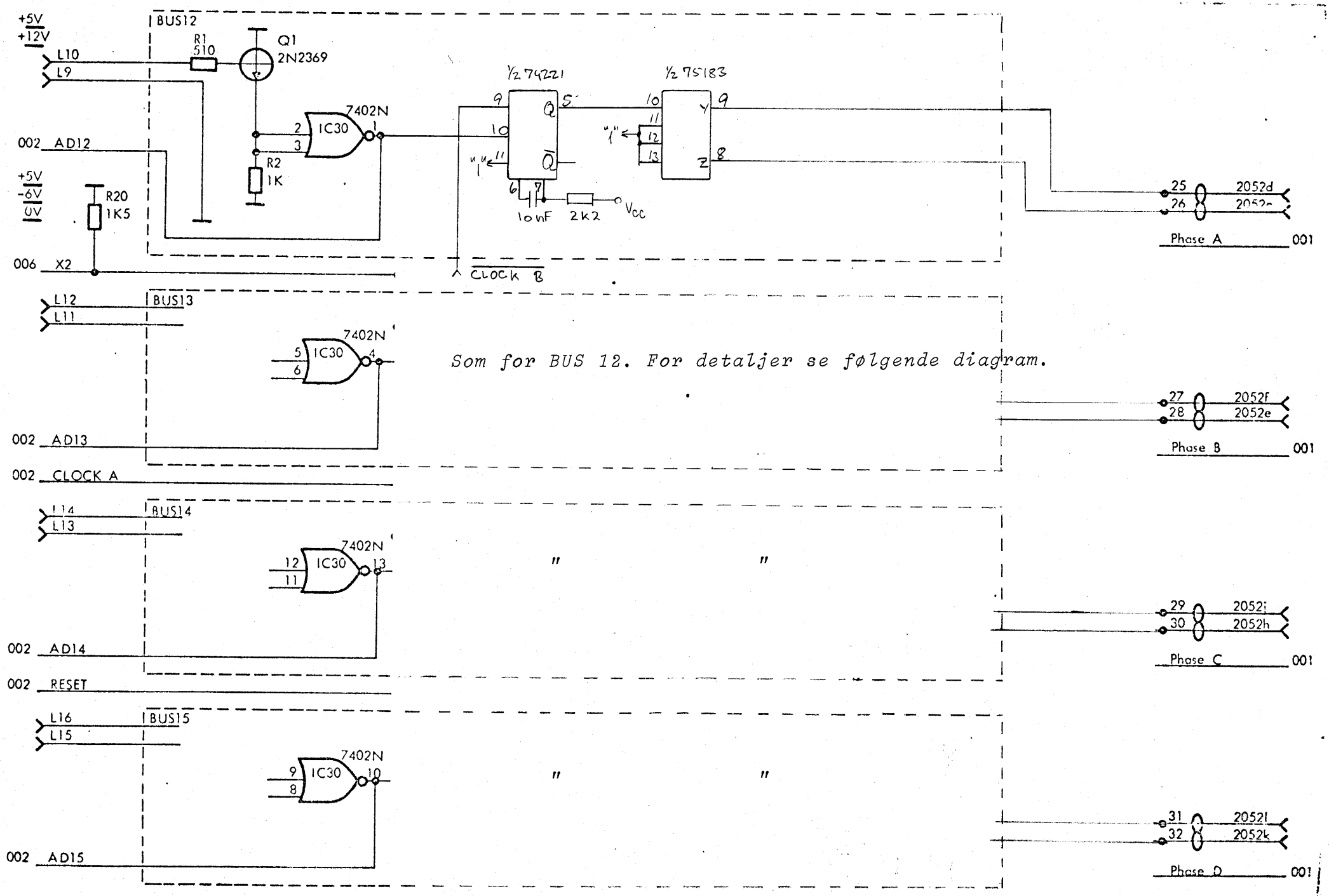


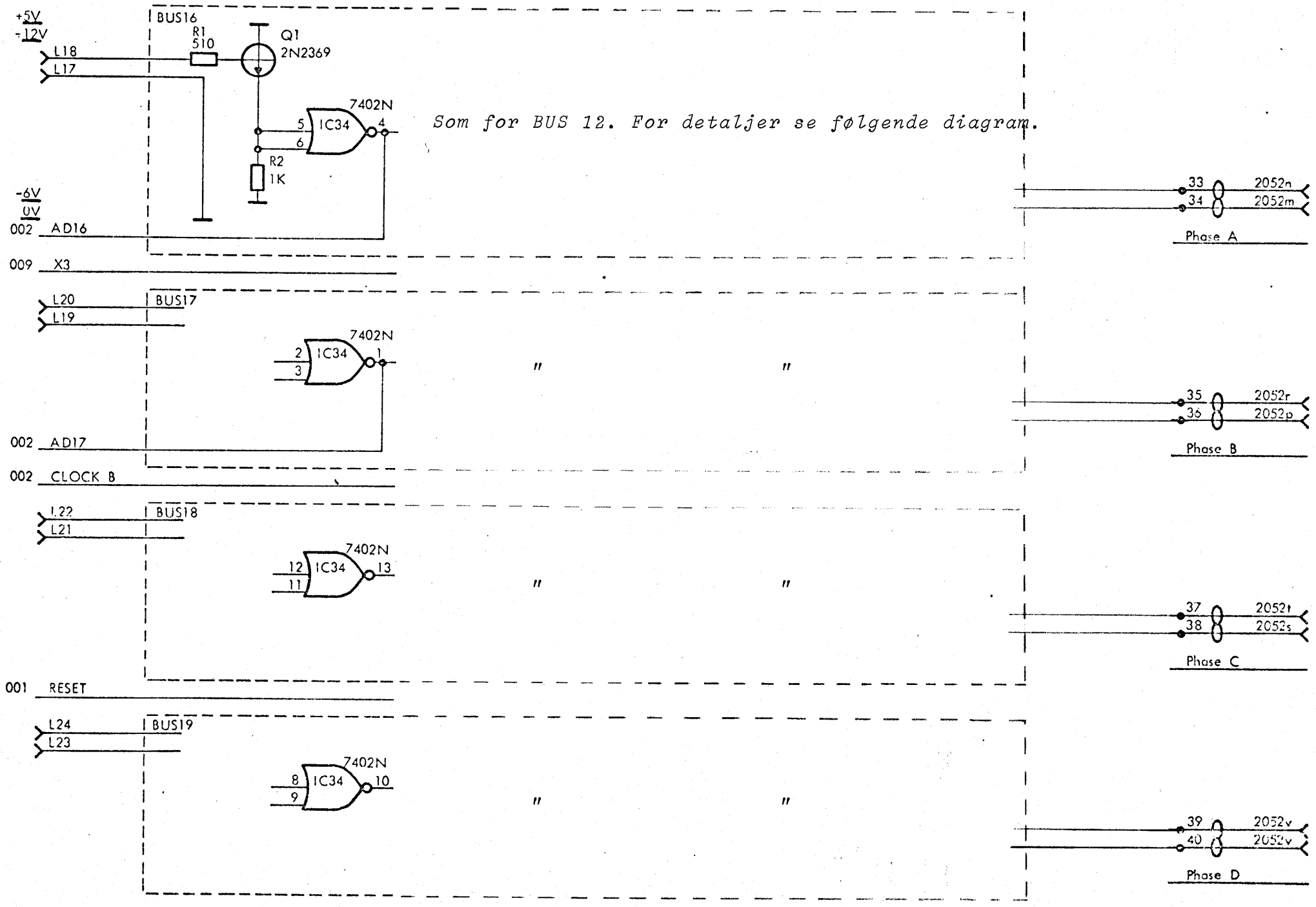

+5V
+12V
-6V
0V
BUS08
R1 510
Q1 2N 2369
R2 1K
T1:Miniwatt 4322 020 36620
PR:6wdg 0,6φ cu
SE:2wdg 0,6φ cu
R3 390
C1 47n
R4 200
T1
D1 BAY72
Q2 2N 2222A
C2 22u 15V
C3 Ou1
R5 200
Q3 2N 2369
D2 IS3062A
Circuit s SA924
17 2052V
18 2052U
Phase A 001
IC11 7402N
IC9 7474N
IC14 7402N
007 X2
BUS09
Circuit t SA924
19 2052X
20 2052W
Phase B 001
002 CLOCK A
BUS10
Circuit u SA924
21 2052Z
22 2052Y
Phase C 001
002 AD10
001 RESET
BUS11
Circuit v SA924
23 2052b
24 2052a
Phase D 001
AD11


Circuit w
SA924
BUS12
T1:Miniwatt 4322 020 36620
PR:6wdg 0,6φ cu
SE:2wdg 0,6φ cu
+5V
+12V
L10
L9
R1
510
Q1
2N2369
7402N
IC30
7474N
IC12
IC15
R3
390
C1
47n
T1
D1
BAY72
C2
22u
15V
C3
Ou1
R5
200
Q3
2N
4239
D2
IS3062A
R4
200
Q2
2N
2222A
R2
1K
R20
1K5
002 AD12
+5V
-6V
0V
006 X2
25
26
2052d
Phase A
001
Circuit x
SA924
L12
L11
BUS13
IC13
27
28
2052f
2052e
Phase B
002 AD13
002 CLOCK A
Circuit y
SA924
L14
L13
BUS14
29
30
2052j
2052h
Phase C
002 AD14
002 RESET
Circuit z
SA924
L16
L15
BUS15
31
32
2052l
2052k
Phase D
002 AD15

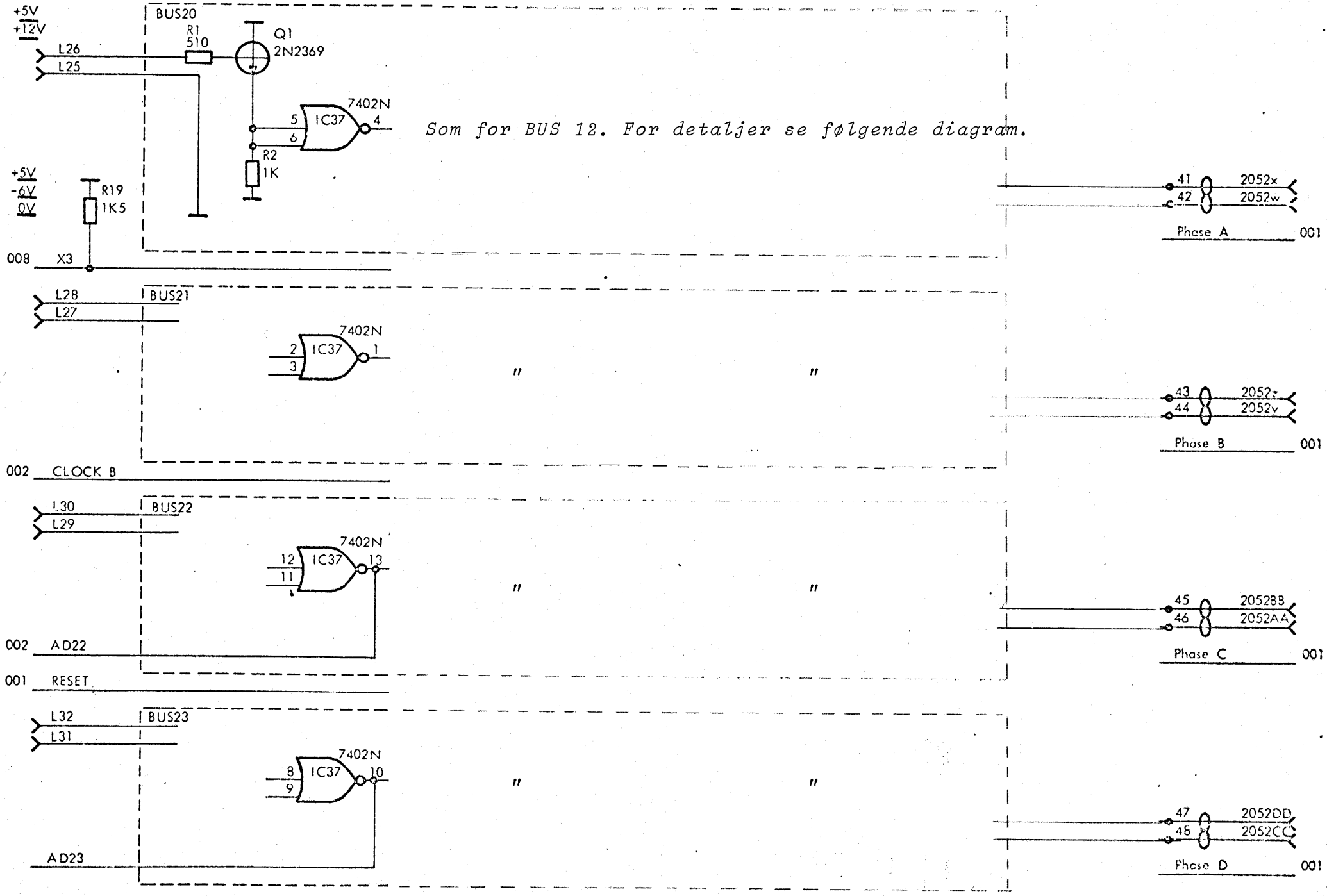

+5V
+12V
-6V
0V
BUS16
L18
L17
R1
510
Q1
2N2369
T1:Miniwatt 4322 02 36620
PR:6wdg 0,6φ cu
SE:2wdg 0,6φ cu
R3
390
D1
BAY72
T1
C3
Ou1
Q3
2N
4239
C2
22u
15V
R5
200
D2
1S3062A
C1
47n
R4
200
Q2
2N
2222A
7402N
IC34
7474N
IC35
IC33
R2
1K
002 AD16
009 X3
Circuit aa
SA924
33
34
2052n
2052m
Phase A
BUS17
L20
L19
002 AD17
Circuit bb
SA924
35
36
2052r
2052p
Phase B
002 CLOCK B
BUS18
L22
L21
Circuit cc
SA924
IC36
37
38
2052t
2052s
Phase C
001 RESET
BUS19
L24
L23
Circuit dd
SA924
39
40
2052v
2052v
Phase D

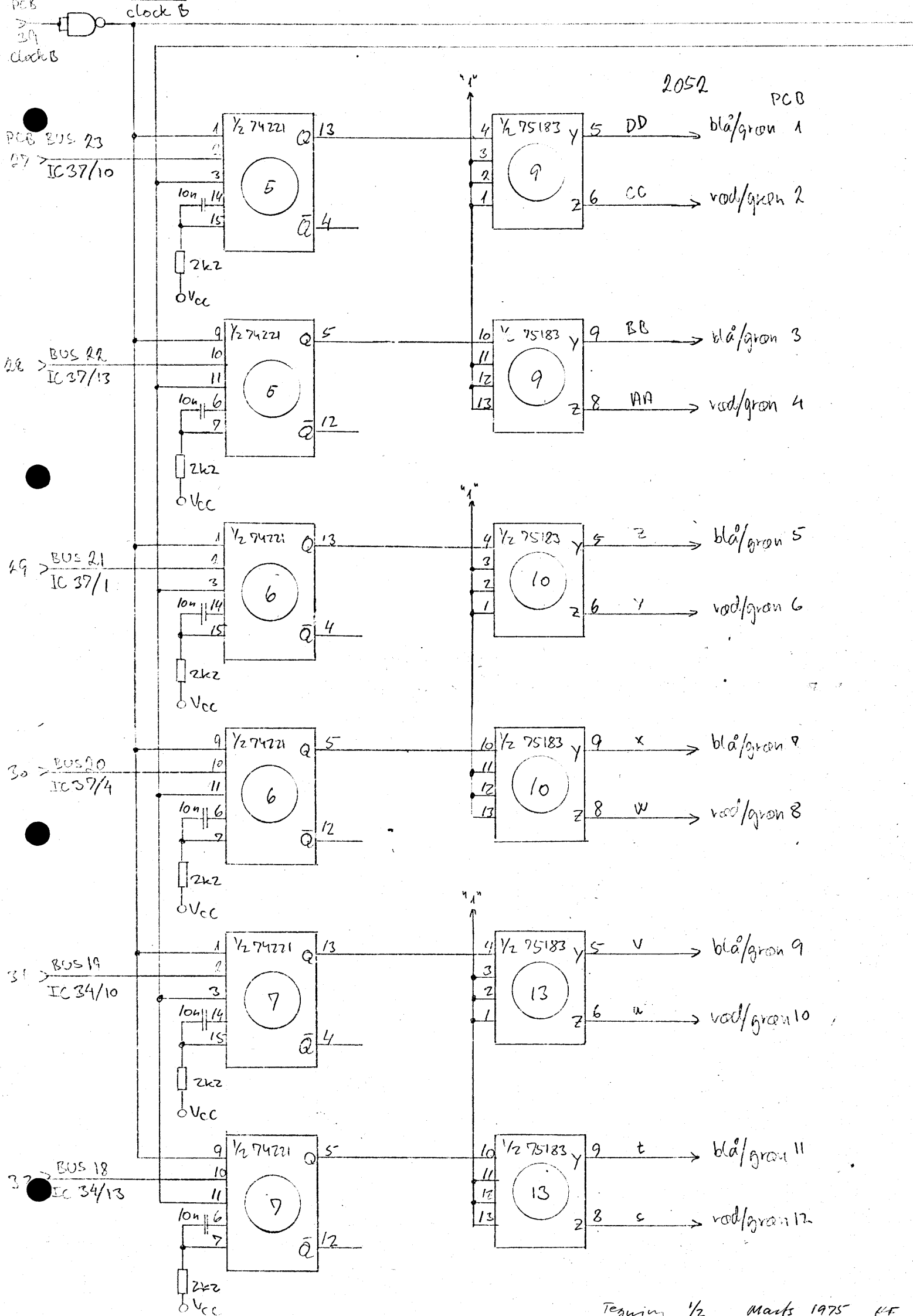

Circuit ee
SA924
BUS20
T1:Miniwatt 4322 020 36620
PR:6wdg 0,6φ cu
SE:2wdg 0,6φ cu
+5V
+12V
L26
L25
R1
510
Q1
2N2369
7402N
IC37
7474N
IC38
R2
1K
R3
390
C1
47n
IC32
T1
C2
22u
15V
C3
Ou1
Q3
2N
4239
R5
200
R4
200
Q2
2N
2222A
D2
1S3062A
+5V
-6V
0V
R19
1K5
008 X3
41
42
2052x
2052w
Phase A
001
Circuit ff
SA924
L28
L27
BUS21
43
44
2052z
2052y
Phase B
002 CLOCK B
Circuit hh
SA924
L30
L29
BUS22
45
46
2052BB
2052AA
Phase C
002 AD22
001 RESET
Circuit jj
SA924
L32
L31
BUS23
47
48
2052DD
2052CC
Phase D
AD23
conduct en marks 1975 HF


+5V
+12V
L10
L9
BUS12
R1
510
Q1
2N2369
7402N
IC30
002 AD12
+5V
-6V
0V
R20
1K5
R2
1K
½ 74221
½ 75183
10nF
2k2
Vcc
006 X2
CLOCK B
25
26
2052d
Phase A
001
L12
L11
BUS13
7402N
IC30
Som for BUS 12. For detaljer se følgende diagram.
27
28
2052f
2052e
Phase B
001
002 AD13
002 CLOCK A
L14
L13
BUS14
7402N
IC30
"
"
29
30
2052i
2052h
Phase C
001
002 AD14
002 RESET
L16
L15
BUS15
7402N
IC30
"
"
31
32
2052l
2052k
Phase D
001
002 AD15

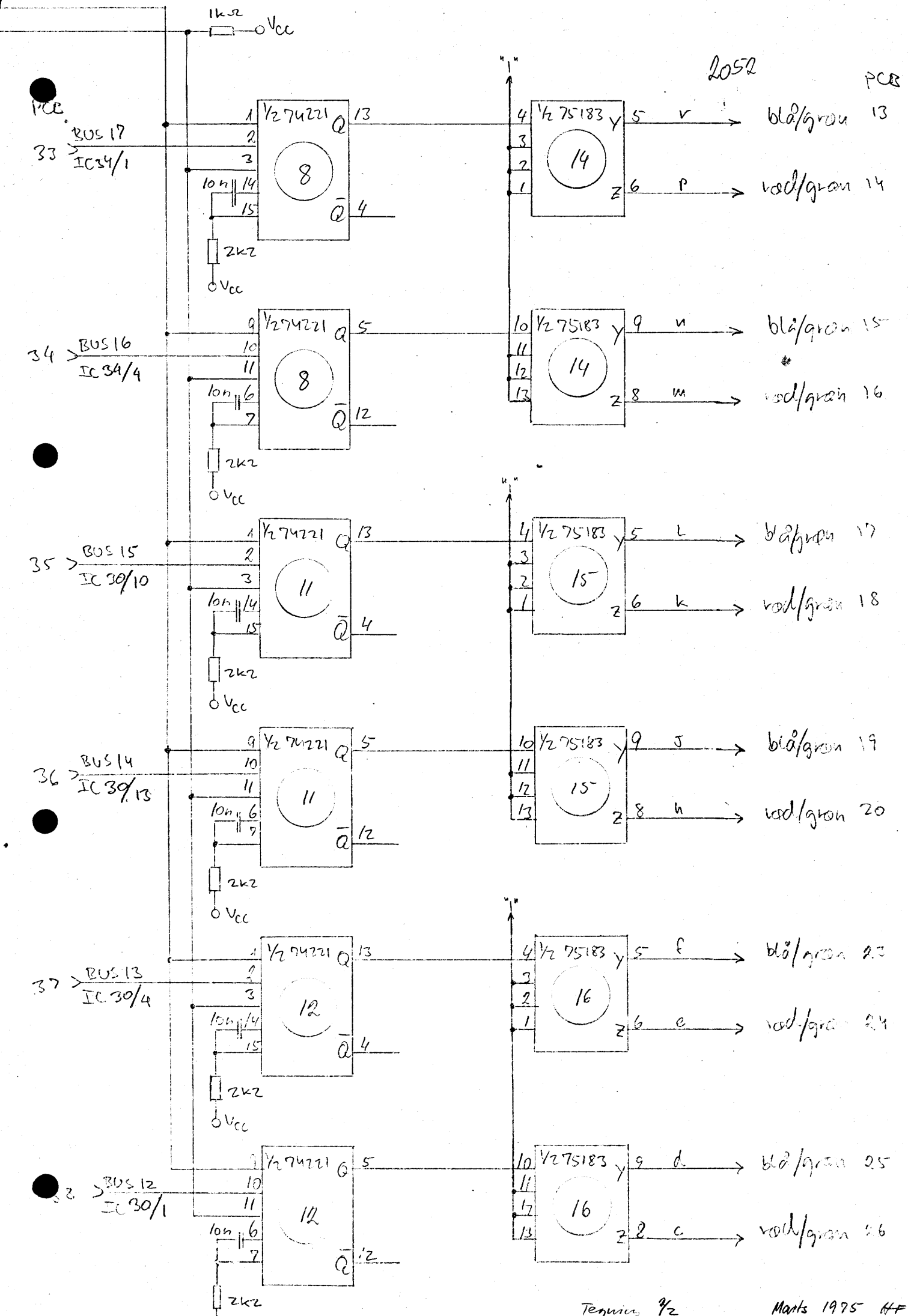


Som for BUS 12. For detaljer se følgende diagram.


+5V
+12V
BUS20
R1
510
Q1
2N2369
L26
L25
7402N
5
IC37
4
6
R2
1K
+5V
-6V
0V
R19
1K5
008 X3
Som for BUS 12. For detaljer se følgende diagram.
41 2052x
42 2052w
Phase A 001
L28
L27
BUS21
7402N
2
IC37
1
3
"
"
43 2052z
44 2052v
Phase B 001
002 CLOCK B
L30
L29
BUS22
7402N
12
IC37
13
11
"
"
45 2052BB
46 2052AA
Phase C 001
002 AD22
001 RESET
L32
L31
BUS23
7402N
8
IC37
10
9
"
"
47 2052DD
48 2052CC
Phase D 001
AD23



Tegnim ½ Mars 1975 KF


1kΩ
Vcc
2052
PCB
PCB
33
BUS 17
IC34/1
1/2 74221
8
10n
2kΩ
1/2 75183
14
V
blå/grön 13
P
röd/grön 14
34
BUS 16
IC 34/4
blå/grön 15
röd/grön 16
35
BUS 15
IC 30/10
11
15
L
blågrön 17
K
röd/grön 18
36
BUS 14
IC 30/13
J
blå/grön 19
röd/grön 20
37
BUS 13
IC 30/4
12
16
F
blå/grön 23
röd/grön 24
BUS 12
IC 30/1
D
blå/grön 25
C
röd/grön 26
Tegnin
Mars 1975 HF

SET-POINT TERMINAL SPT 401

1. MAIN CHARACTERISTICS

Terminal Unit SPT 401 is a digital input/output terminal with 24-bit digital inputs and 16-bit buffered digital outputs. Inputs and outputs are of the floating type to ensure insulation from the power supply system in the computer. SPT 401 is to be placed in chassis CHS 404 and connected to the low-speed data channel via busline converter BCV 401. Data from the terminal can be transferred to the selected W-register by means of a sense command.

Data can be transferred from the W-register to the buffer register in SPT 401 by means of a write command. The width of all 16 output pulses is equal, and determined by a capacitor (C5 and C6 in parallel). The device is busy for a period determined by the choice of a capacitor (C1,C2,C3, and C4 in parallel).

2. APPLICATIONS

1. 24-bit digital input terminal for floating 12-volt inputs. Typical 11 mA per input, and/or
2. digital output terminal with 8 groups of 2 floating contacts for 12 volts, maximum 100 mA. (Maximum one contact per group can be on at the same time)
3. set-point controller for 8 set-point stations, each one supplied with up- and down pulses, and sensed for upper- or lower limit exceeded and local/remote status.

3. SPECIFICATIONS

Selection:	Input/output instruction with predetermined device address.
Interrupt Output:	Interrupt output to front panel and/or mother board, predetermined by wiring of the address selection plug-in board.
Busy:	After accepting a write command, the device becomes not ready for a time determined by choice of capacitors. For C in microfarad, typical busy time is given as To = 20(C1+C2+C3+C4)mSec. (C1+C2) shall be equal to (C3+C4) ±40 per cent.
Inputs:	
Number of Inputs:	24 bits (bit 0:23)
Type of Inputs:	2-wire, contact sensing for floating 12-volt supply. (Other voltages optional) Closed contact:= 1 transferred to the W-register. Open contact:= 0 transferred to the W-register.
Voltage Supply:	12-volt nominal ±20 per cent
Load Current:	11 mA nominal
Cable Resistance:	Maximum 500 ohms (including contact resistance)
Common Mode:	500 volts common mode voltage between input circuits and logic ground acceptable. Capacity between input circuit and logic system is 3 pF/input.

Outputs:

Number of Outputs:	16 bits (bit 1:2,4:5,7:8,10:11,13:14,16:17, 19:20,22:23)
Type of Outputs:	2-wire, single pulse contact-closure for floating loads, max. 12 volts (Other voltages optional)
Load Current:	100 mA maximum.
Bit Representation:	For n:= 1,4,7,10,13,16,19,22 W(n,n+1) = 1.0: One single pulse at output terminal n. W(n,n+1) = 0.1: One single pulse at output terminal n+1. W(n,n+1) = 0.0 or 1.1: No pulses.
Pulse Length:	Determined by capacitor. For C in microfarad, typical pulse length is given as Tp = 20(C5+C6)mSec. (C5+C6) shall be less than (C1+C2+C3+C4)/2. Capacity between output circuit and logic system is 3 pF/output.
Common Mode:	500 volts common mode voltage between output circuits and electronic ground acceptable.

Stray Capacity: Total capacity between all input- and output circuits and the electronic system is about 130 pF.
Stray capacity between input- or output circuits and environment is about 25 pF/circuit.

Power Supply:

5 volts	720 mA
12 volts	0-75 mA
-6 volts	200 mA
12 volts spec.	300 mA (e.g. external power supply)

Power Dissipation: 8.0 Watt

Dimensions:

Height:	355 mm
Width:	24 mm
Depth:	450 mm

Weight: 1.2 kg

RCSL: 51-VB909
Author: P.E. Pedersen
Edited: June 1970
Revision 16 May 1972
Anders Lindgård

RC 4000 PERIPHERAL DEVICES

SPT 401 SET-POINT TERMINAL

~~Preliminary~~ Specifications

ABSTRACT: This report describes the logic structure of the Set-Point Terminal SPT 401 when used in connection with the RC 4000 Computer.

A/S REGNECENTRALEN
Falkoneralle 1
DK 2000 Copenhagen F

CONTENTS

pp.: 1:5

1. MAIN CHARACTERISTICS

The set-point terminal, SPT 401, is connected to the low-speed data channel, and is designed to control up to 8 stepping-motor driven set-point stations. By means of a write command all 8 set-point stations can be activated simultaneously; but with individual step commands: All the set-point stations may individually be ordered either to step one step up, one step down, or to stay unchanged. When the activation interval is finished, an interrupt signal is generated.

Each set-point station is supplied with two limits, upper and lower limit inside which the set-point station may be controlled. ~~These limits are set by the control room operator.~~

Each set-point station is also supplied with ~~two push-buttons, COMPUTER CONTROLLED, and NOT COMPUTER CONTROLLED~~, by means of which the control room-operator can determine whether the set-point station should be controlled by the computer or manually.

The status of all set-point stations can be transferred to the computer. Status will indicate whether upper limit is exceeded, lower limit is exceeded, or the computer control is switched off.

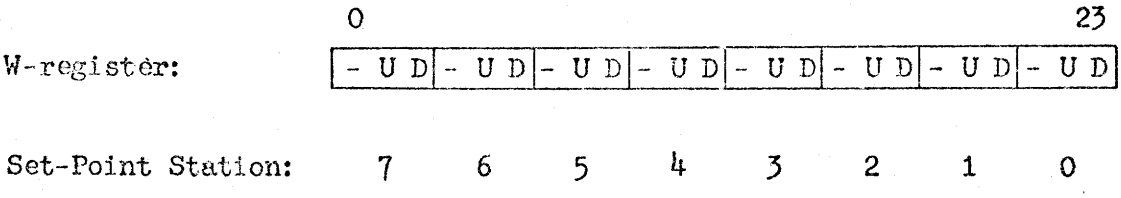
2. COMMANDS

SPT 401 accepts sense and write commands. In the input/output instructions specifying these commands, the value of the modifier field, i.e. bits 18:21 in the effective address, is irrelevant.

Use of read- or control commands will not affect SPT 401.

2.1. Write Command.

When SPT 401 is ready, it will accept a write command. The set-point stations connected can in this way be stepped individually one step up, one step down, or neither up nor down. The contents of the working register selected by the input/output instruction is interpreted as follows:



U: UP command. Set-point station moves one step up.

D: DOWN command. Set-point station moves one step down.

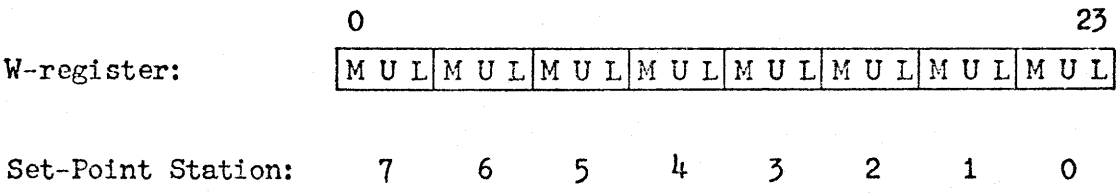
-: not used.

Simultaneous UP- and DOWN commands for a certain set-point station will not move the set-point station.

After the initiation of a write command the set-point terminal is busy for approximately 100 msec. The set-point terminal gives an interrupt signal when it becomes ready.

2.2. Sense Command.

~~When SPT 401 is ready~~, a status word can be transferred to a working register by means of a sense command:



M: Manual Control.

The status bit indicates that the operator has switched off the computer control of the set-point station concerned. ~~UP- or DOWN commands have no influence on the set-point station.~~

U: Upper limit exceeded.

This status bit indicates that the set-point station concerned has passed the upper limit. ~~UP- or DOWN commands have no influence on the set-point station.~~

L: Lower limit exceeded.

This status bit indicates that the set-point station concerned has passed the lower limit. ~~UP- or DOWN commands have no influence on the set-point station.~~

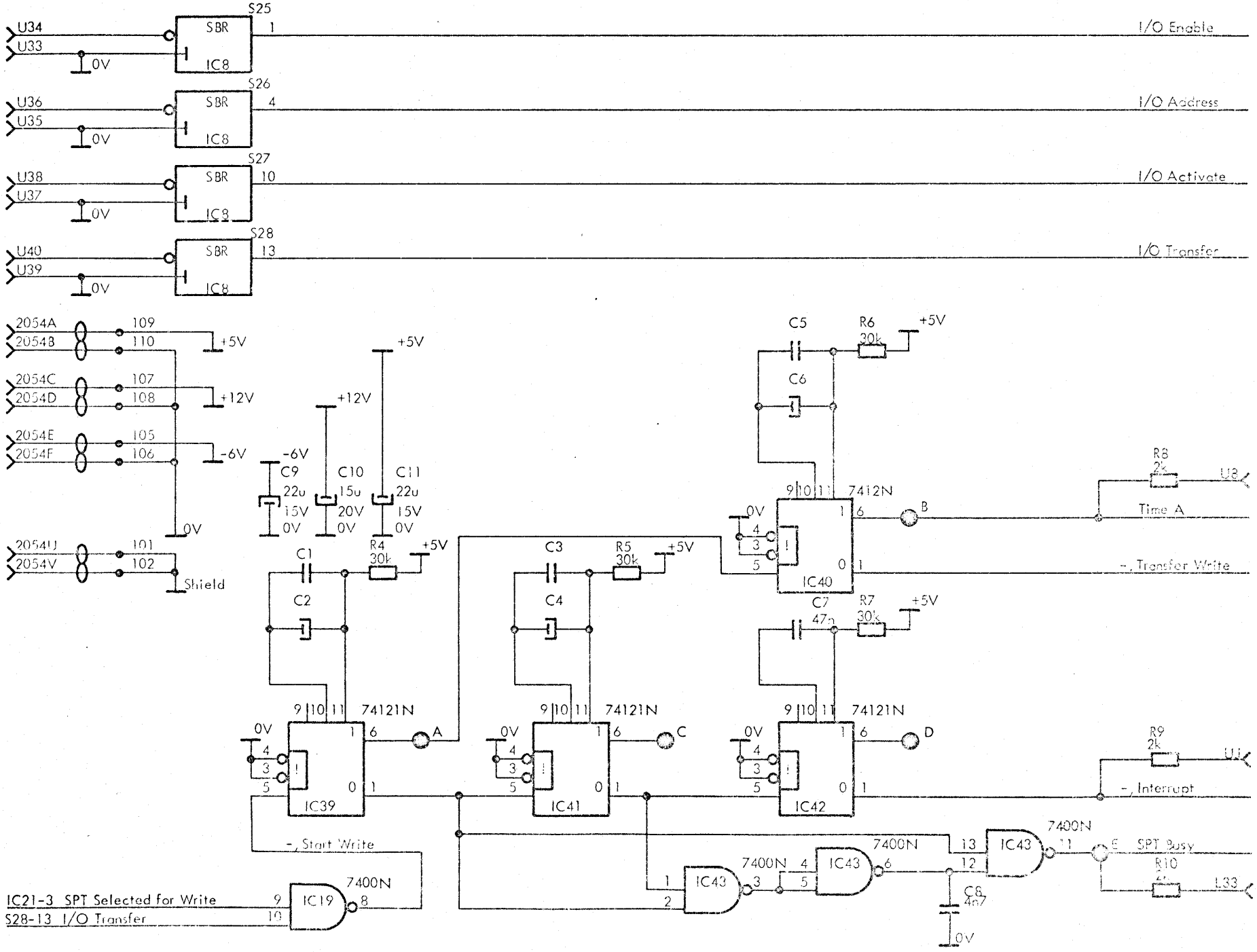
When upper or lower limit has been exceeded, the control room-operator must manually move the set-point to be within limits in order to bring the station back under computer control again.

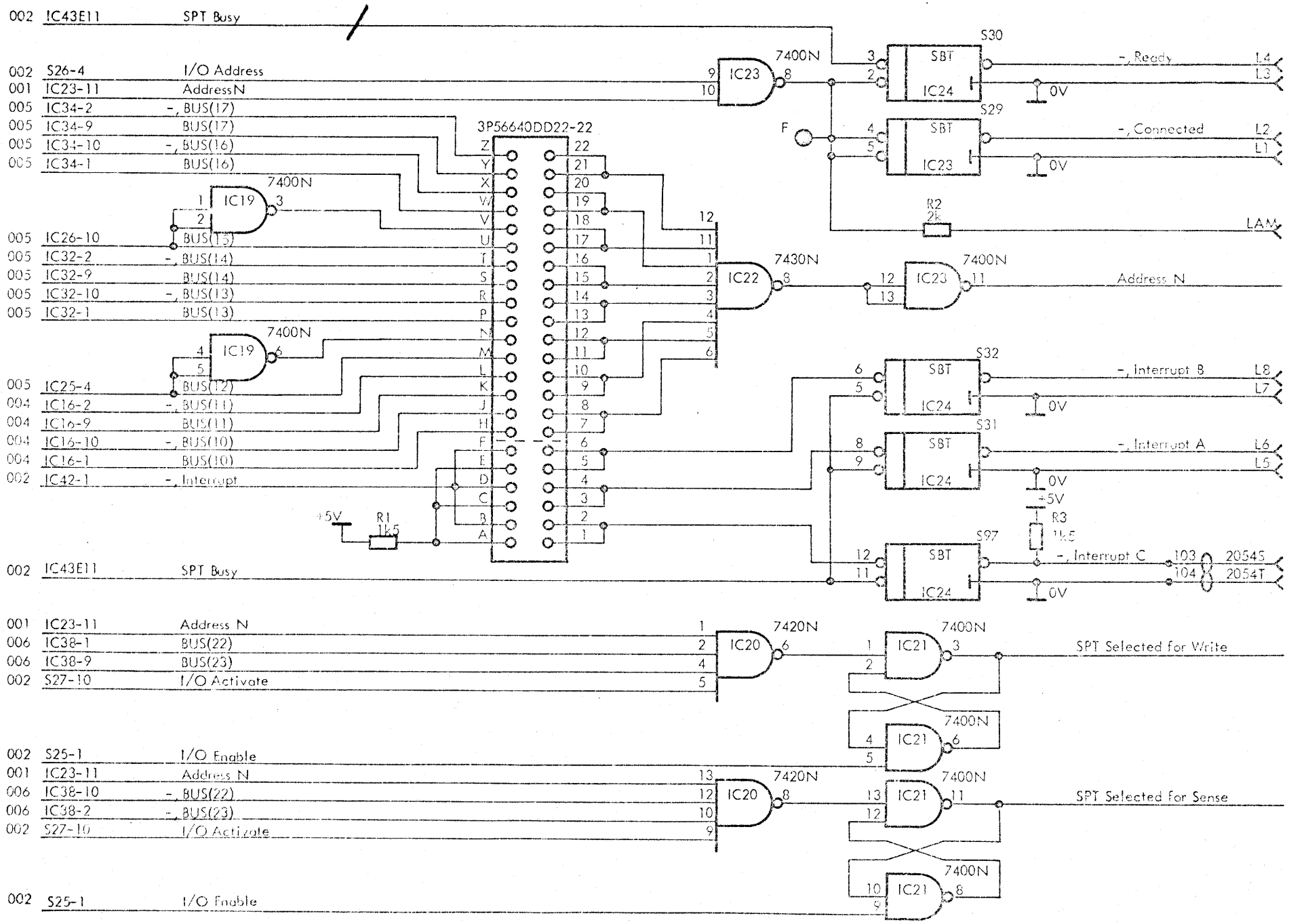
Der er fjernet en hardware-ændring, således at terminalen ikke er busy under en sense-command. Se ændringen på side SPT-012.

J. Oxenbøll 16-5-72

Receivers for Control Signals and Pulse Timing

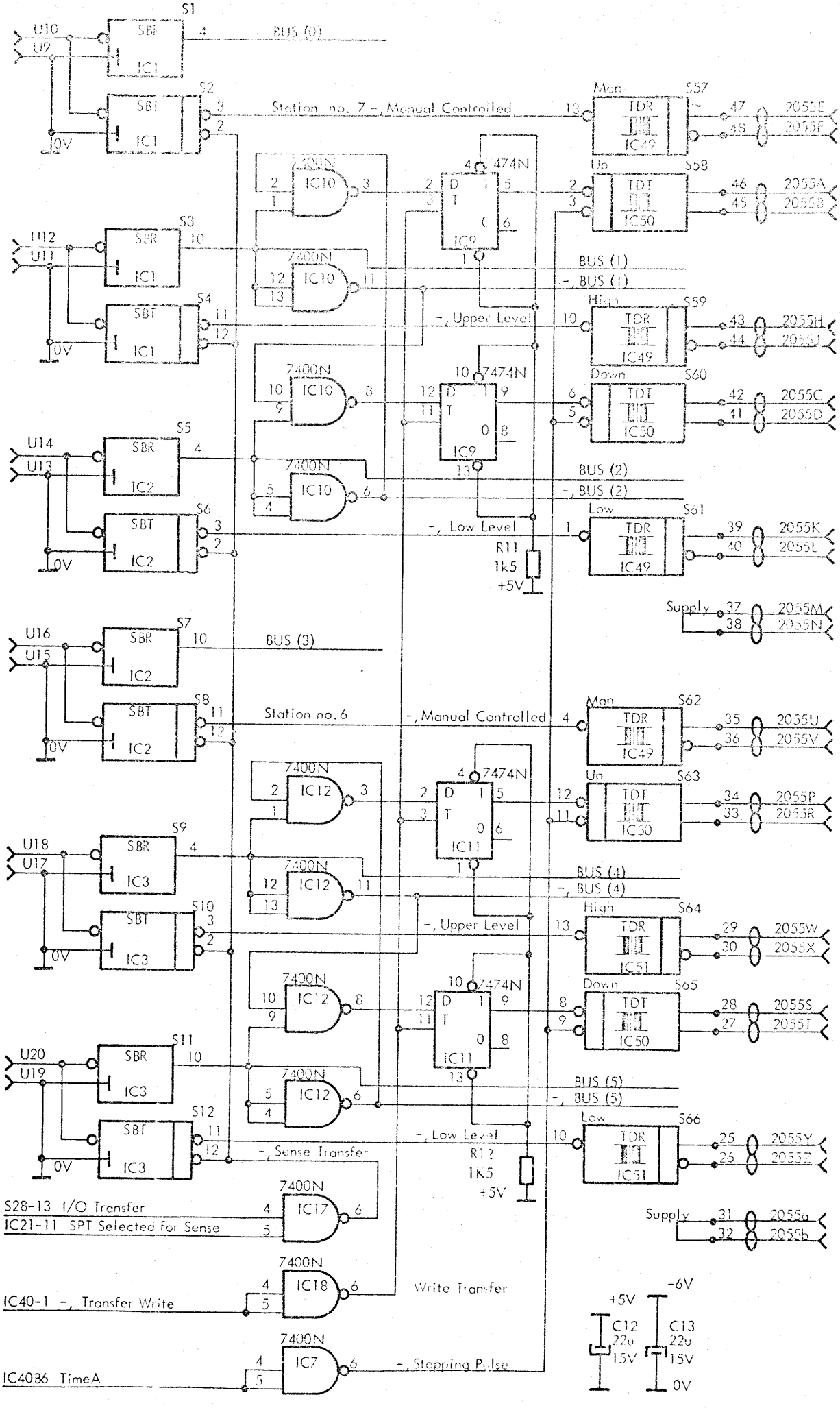
PCBA Circuit Diagram





Address Decoding, Ready, Connected, Interrupt and Selection

PCBA Circuit Diagram



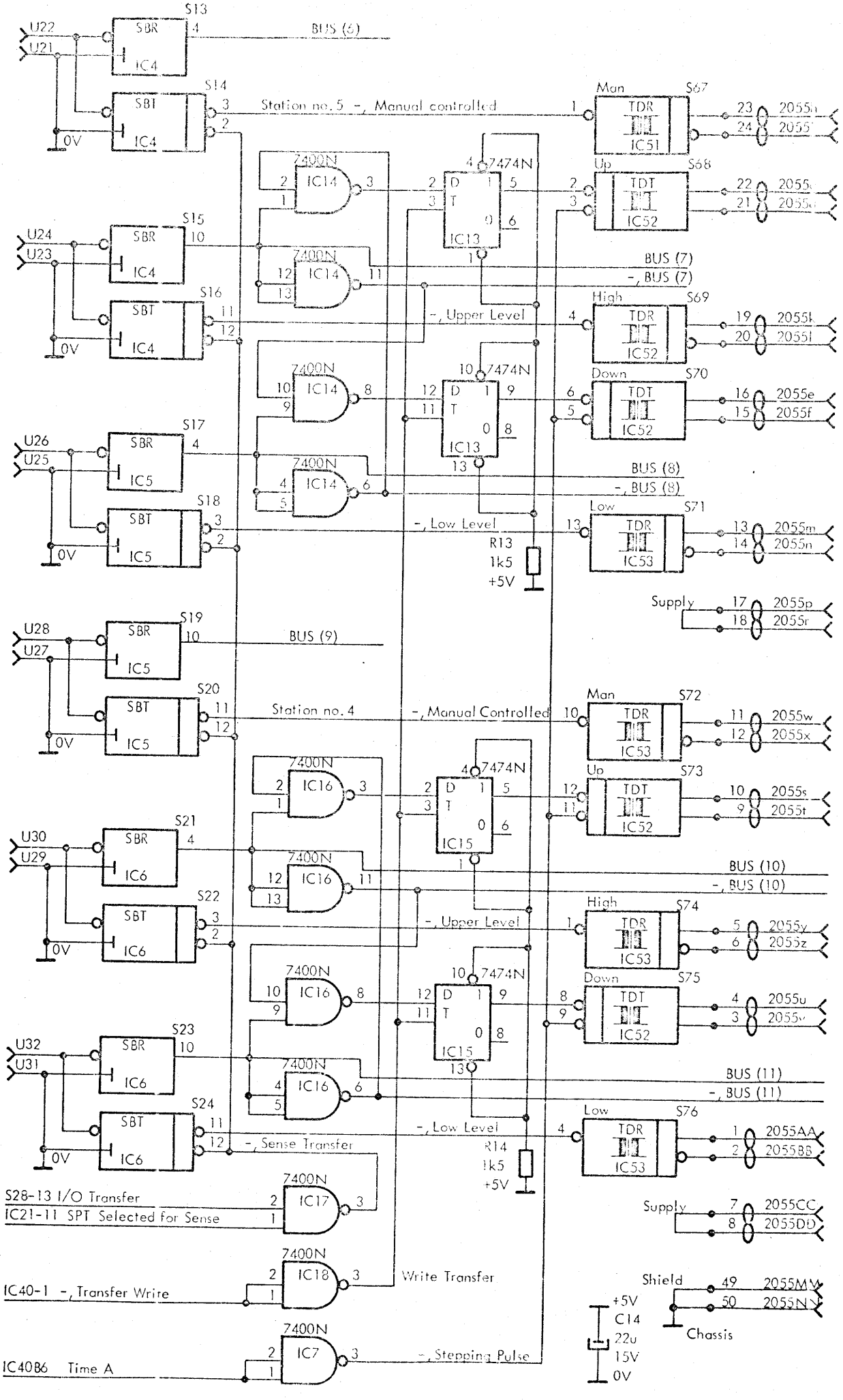
SPT401

V11989

BIT (0:5)

PCBA Circuit Diagram

SPT003



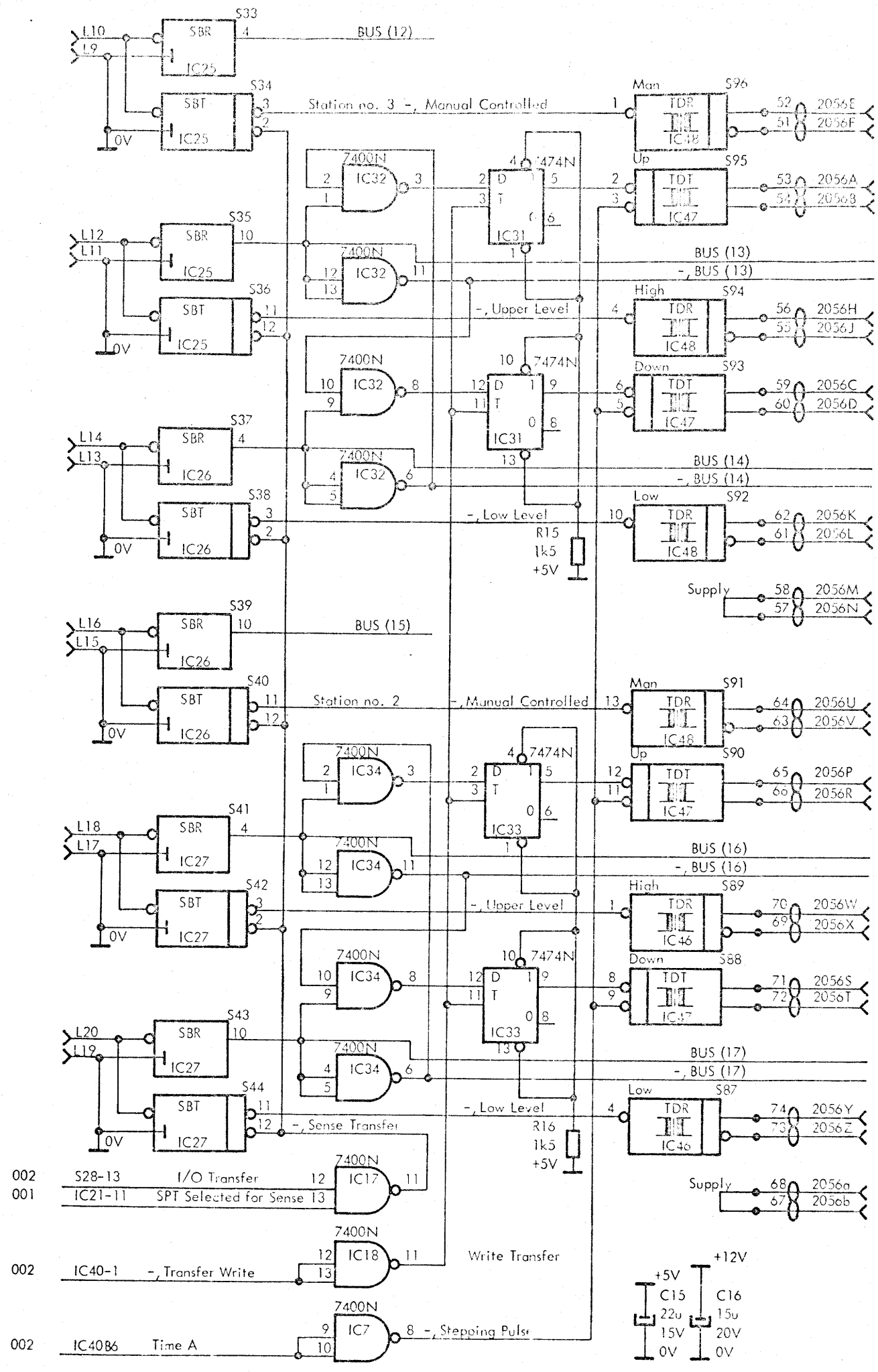
SPT401

BIT (6:11)

SPT004

V11990

PCBA Circuit Diagram



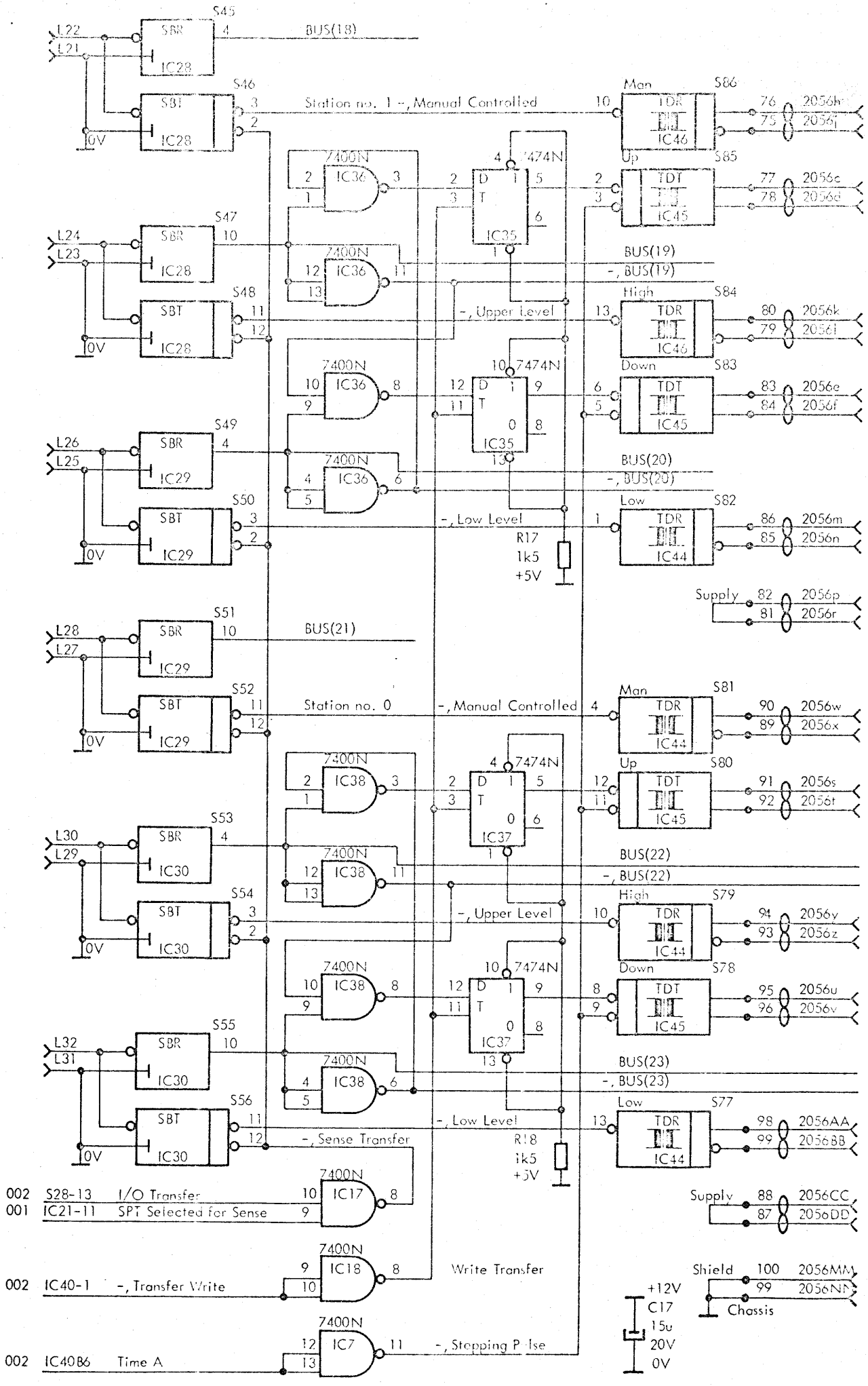
SPT401

BIT (12:17)

SPT005

V11991

PCBA Circuit Diagram



SPT401 BIT(18:23) SPT006

V11992 PCBA Circuit Diagram

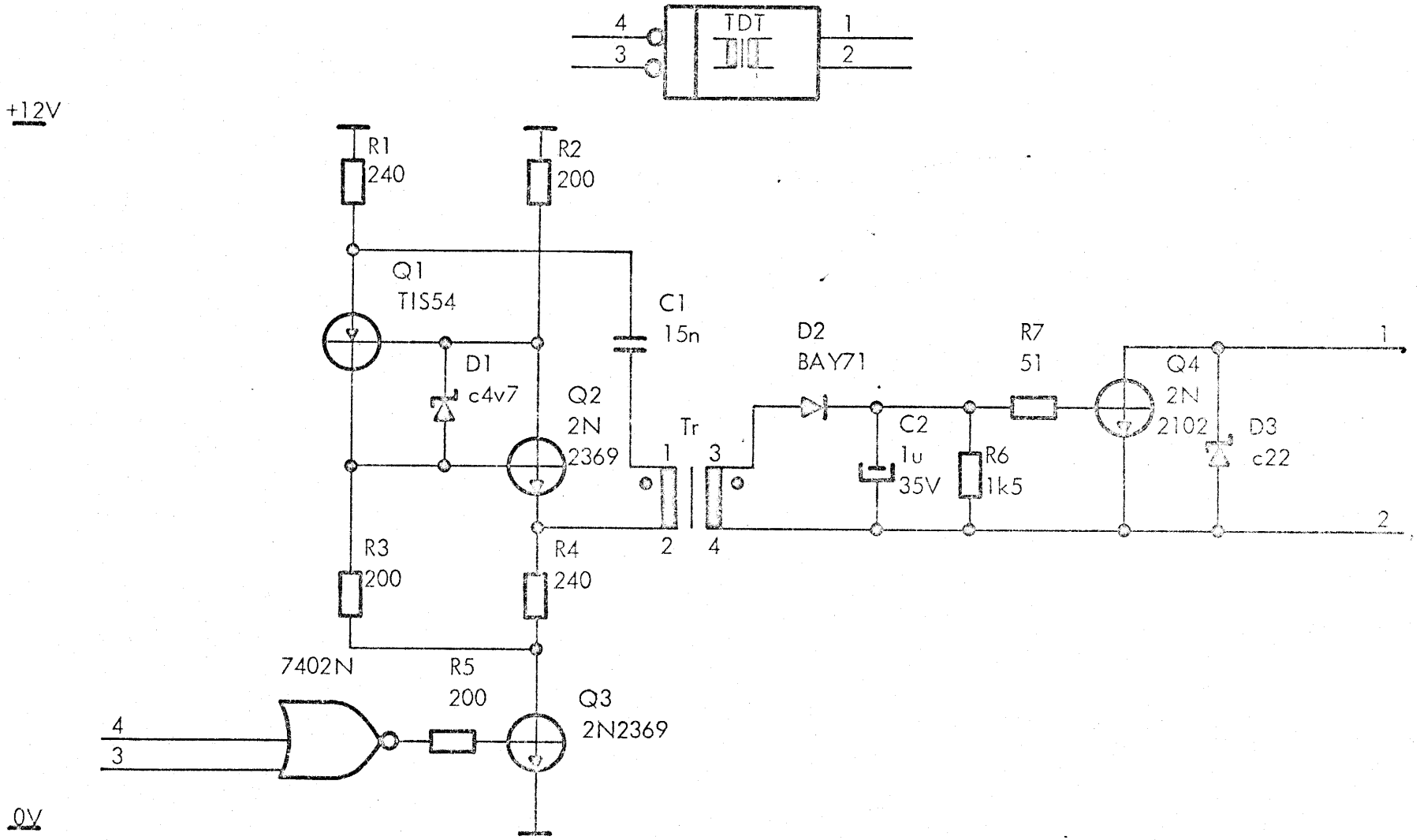
SPT401

V21540

Transformer Driven Transmitter

Logic Symbol and Circuit Diagram

SPT007



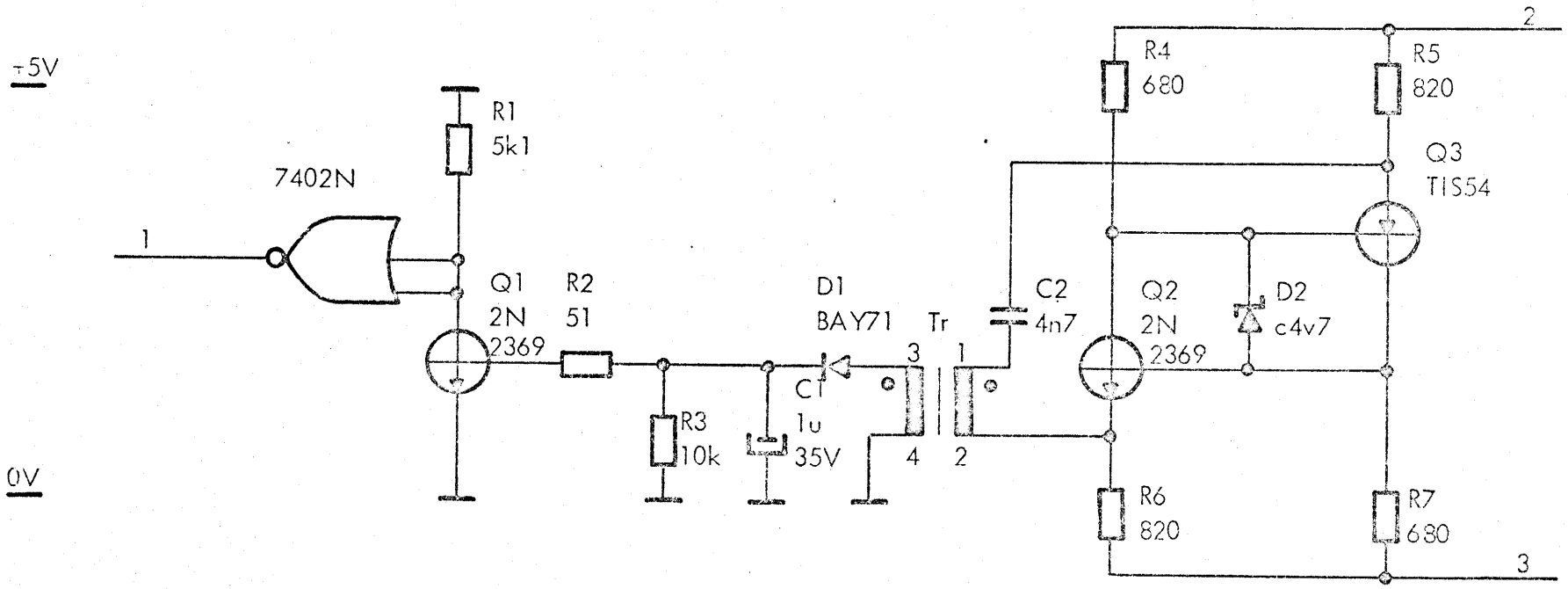
Tr: Toroid Transformer.
Core: Miniwatt, 9 x 6 x 3, blue, 4322 020 36670.
Windings: Prim. 1-2: 5 Wdg. 26 AWG 600V Irravin Type A2030.
Windings: Sec 3-4: 10Wdg. 0,3 mm solderable Dätwyler Type Fewil L 3,2.

SPT401

V21541

Transformer Driven Receiver

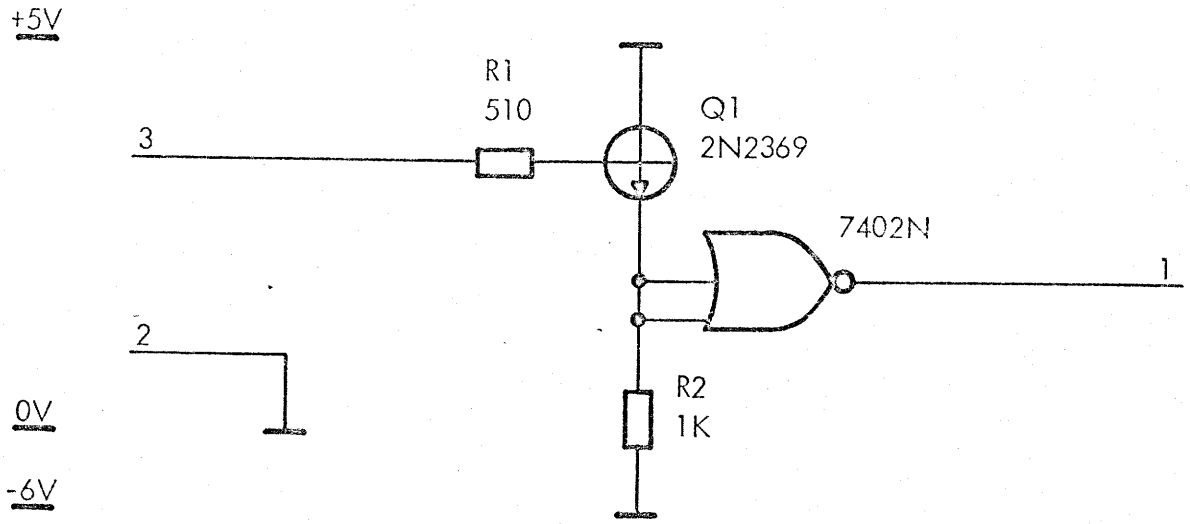
Logic Symbol and Circuit Diagram

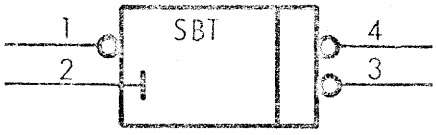


Tr; Toroid Transformer.
Core: Miniwatt, 9 x 6 x 3, blue, 4322 020 36670.
Windings: Prim. 1 -2: 5 wdg. 26 AWG 600V Irravin Type A2030.
Windings: Sec. 3 - 4: 10 wdg. 0,3mm solderable Dätwyler Type Fewil L3,2.

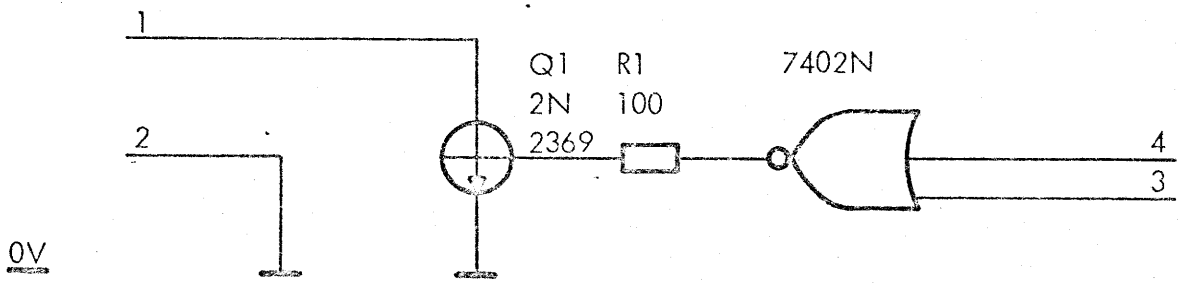
SPT008

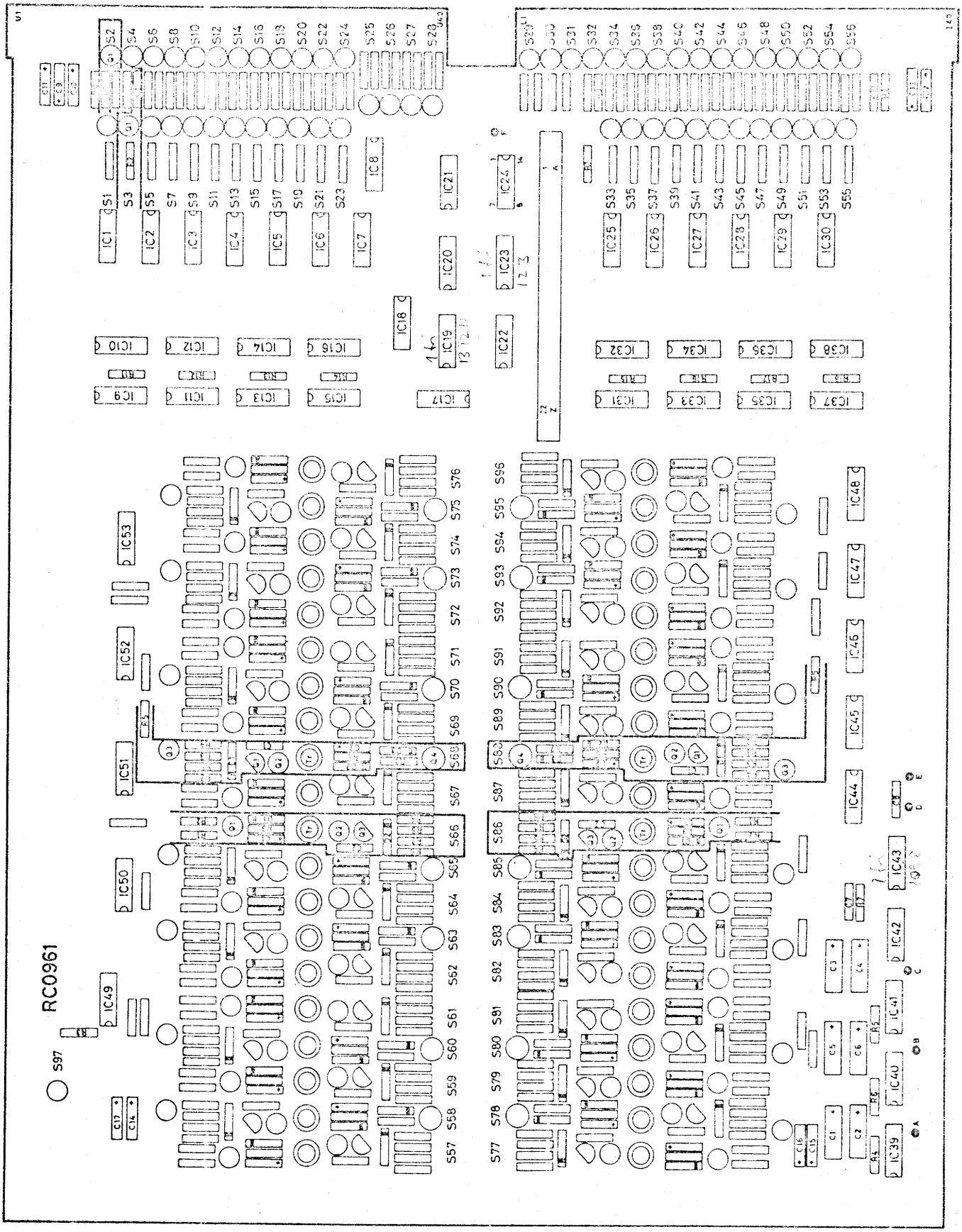

3
2
SBR
1


+5V
R1
510
Q1
2N2369
3
7402N
1
2
R2
1K
0V
-6V


1
2
SBT
4
3


4
3
SBT
1
2


1
2
0V
Q1
2N
2369
R1
100
7402N
4
3



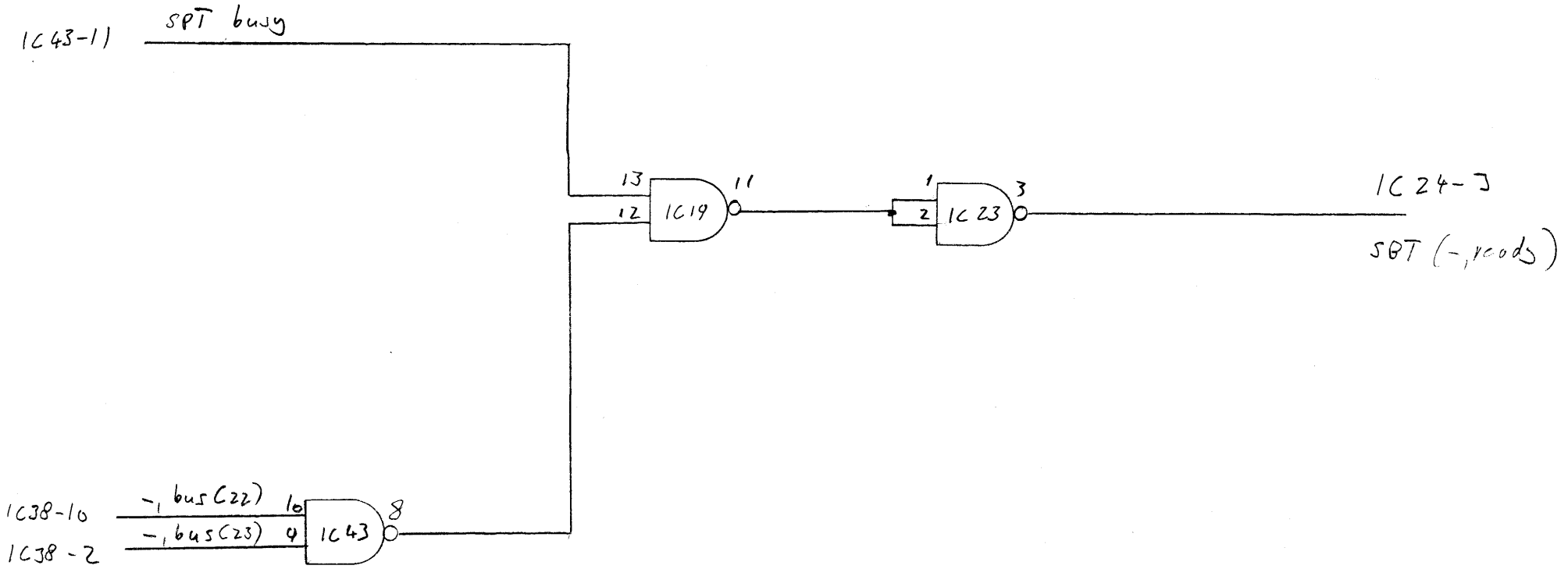
SPT401

Circuit Board Assembly

SPT011

V12024

Forbindelsen mellem IC 43-11 (SPT-busy) og IC 24-3 (SBT-ready) skares op, og følgende sættes imellem:



210-105

Torenball
16-5-72

SPECIFICATION AOC401

ANALOG OUTPUT CONVERTER AND CONTROLLER, AOC401

The Analog Output Converter and Controller, AOC401, forms the connection between the low-speed data channel of the RC 4000 and the analog process to be controlled. In order to do this the following functions are performed:

- ~~Transmitting~~ Receiving and buffering of data ~~to~~ from the low-speed data channel via the bus converter.
- Digital to analog conversion
- Galvanic separation to RC 4000.

1. SPECIFICATIONS

AOC401:

Number of D/A Converters per Module:	2

Voltage Output:

Voltage range	±10 V
Output impedance	< 1 ohm
Max. output current	±5 mA
Accuracy at 25 degrees C	±0.05 per cent
Drift	±50 ppm/degrees C f.s.

Max. Conversion Time:	15 µsec.

Power Supply Requirements:

The AOC can be supplied either from RC 4000 or from the process under control.

+24 V ±5 per cent	0.2 amp.
+5 V ±5 per cent	2 amp.
-24 V ±5 per cent	0.2 amp.
Power	app. 20 watt

Ambient Air:

Temperature:	0 to 45 degrees C
Relative Humidity:	30 to 70 per cent

Dimensions:

Height:	355 mm
Width:	24 mm
Depth:	450 mm

Weight: 1.5 kg

Connection to RC 4000: Low-speed data channel via bus converter (I/O instruction with predetermined device address).

I/O Commands: Write: Two bytes data.

Format of Write Information (One Write Command):

1. One byte data transferred from selected w register bits 0-11. Zero is the most significant bit.
2. One byte data transferred from selected w register bits 12-23. Twelve is the most significant bit.

Rettelser / D-to-A-omsætter [illegible]

i layout

2 stk 1 μF/50 V indføres

2 stk 20 Ω parallel over 10 Ω i 17 V supply

2 potmeter flyttes (kan out)

[illegible] til ±24 V [illegible]

AOC 401

Endl/Lab

Forplade bestilt d 19/7 71
til levering d 9/8 71

stikrække 2059 20 pol Elco bit 0-11
2060 — " — " — " 12-23

Sagsnr. 31025

A: output	
B: 0 V	
S: +24 V	
T: -24 V	
U: } 0 V	
V:	
W	
X	

Intr connection AOC 401

PCBA → Front panel.

upper circuit:

20 pole Elco.

A: output B: analog ground

S: +24V I: −24V.

U-V: 0V

lower circuit:

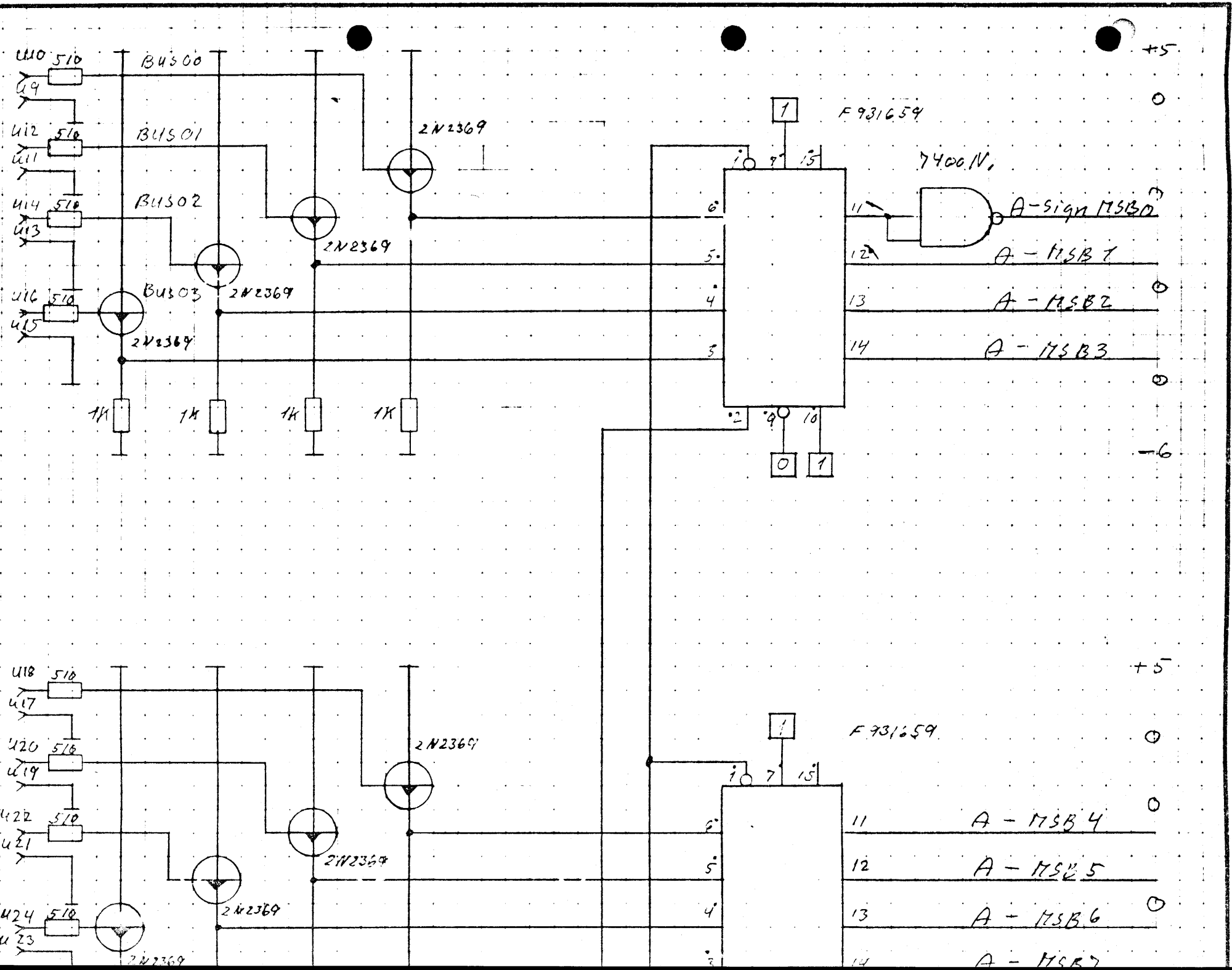
20 pole Elco.

A: output B: analog ground

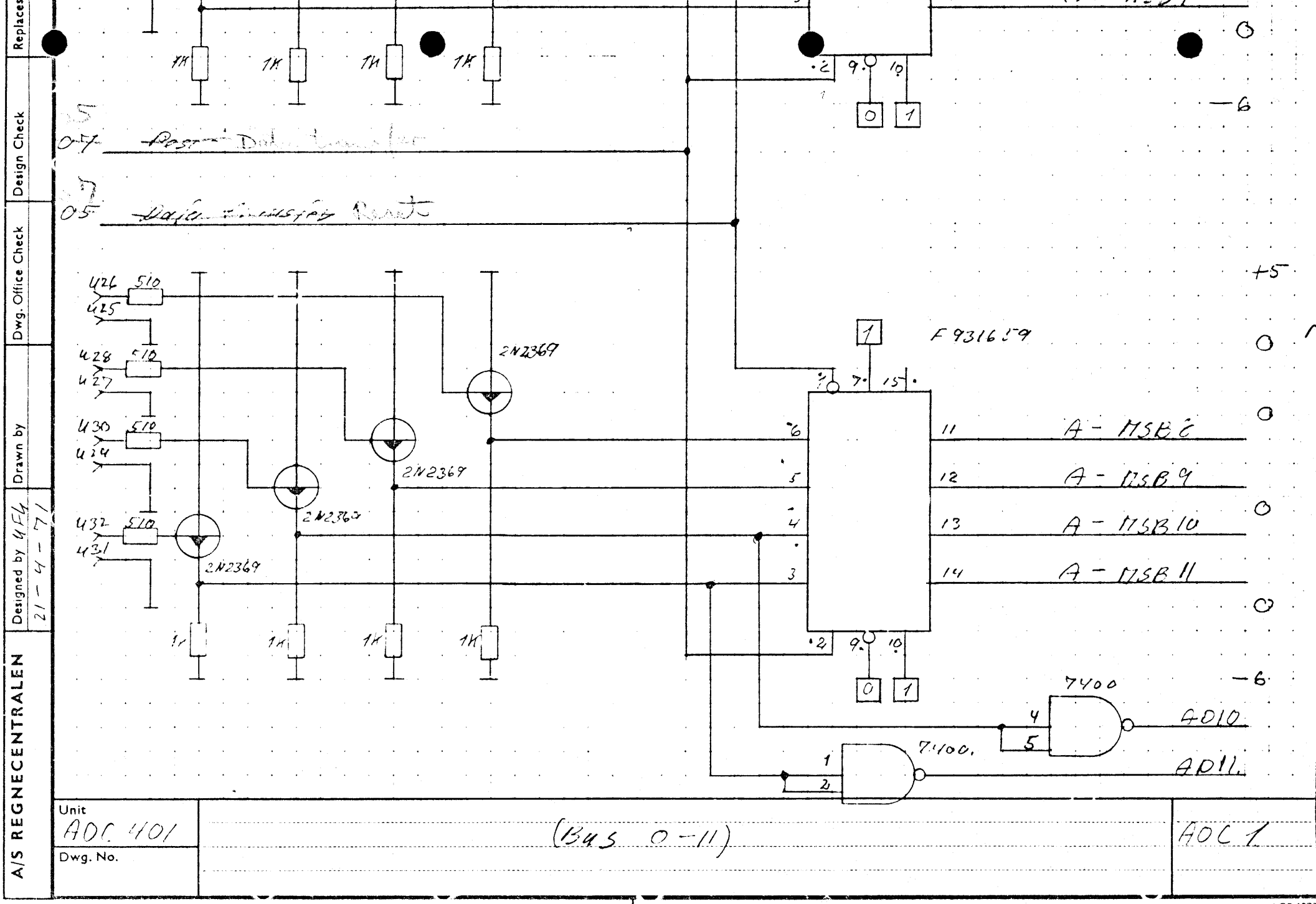
S: +24V I: −24V

U-V: 0V

MPL.
24-6-71



Dwg. No.	due to ECN	Replaced by Dwg. No.



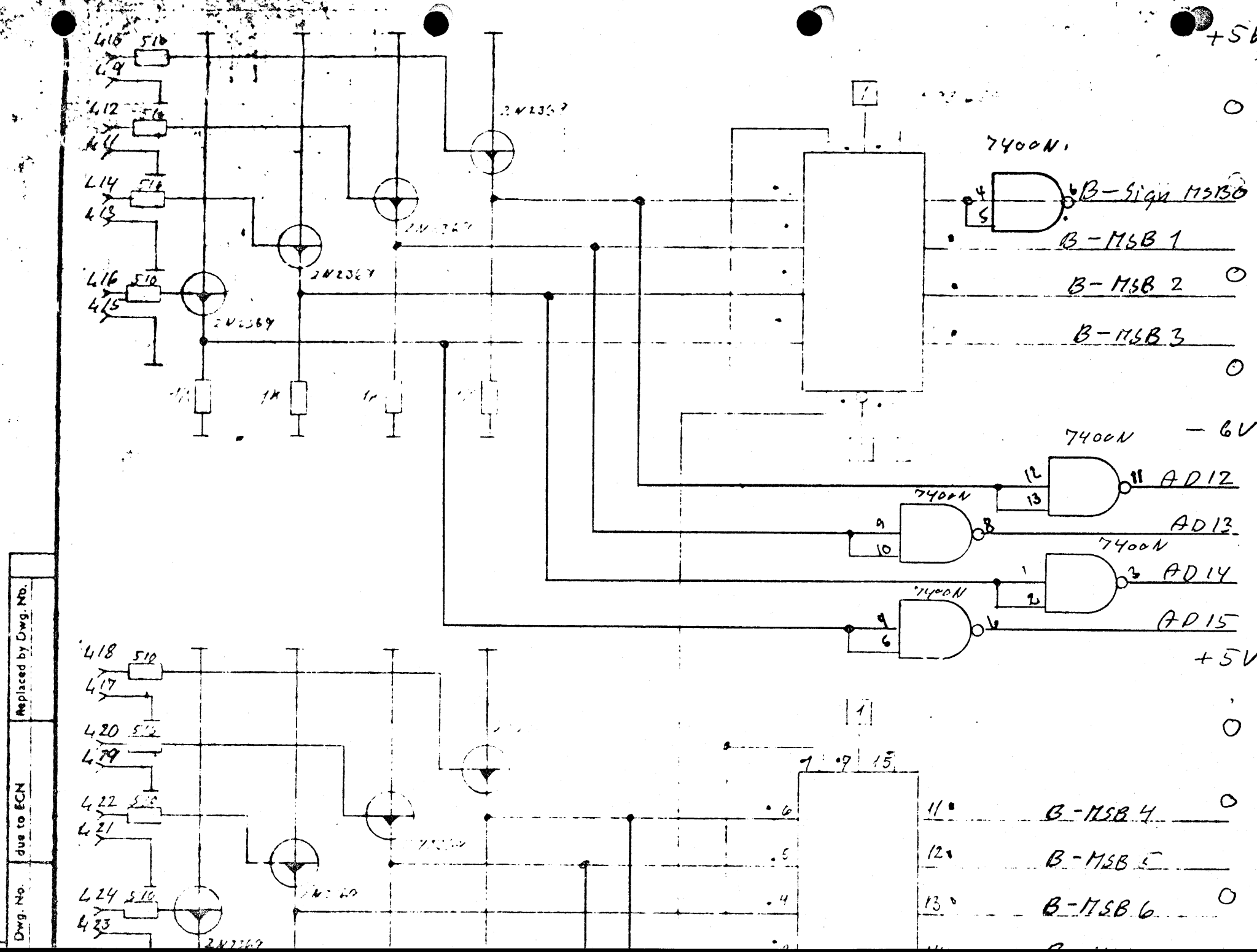
Unit
AOC 401

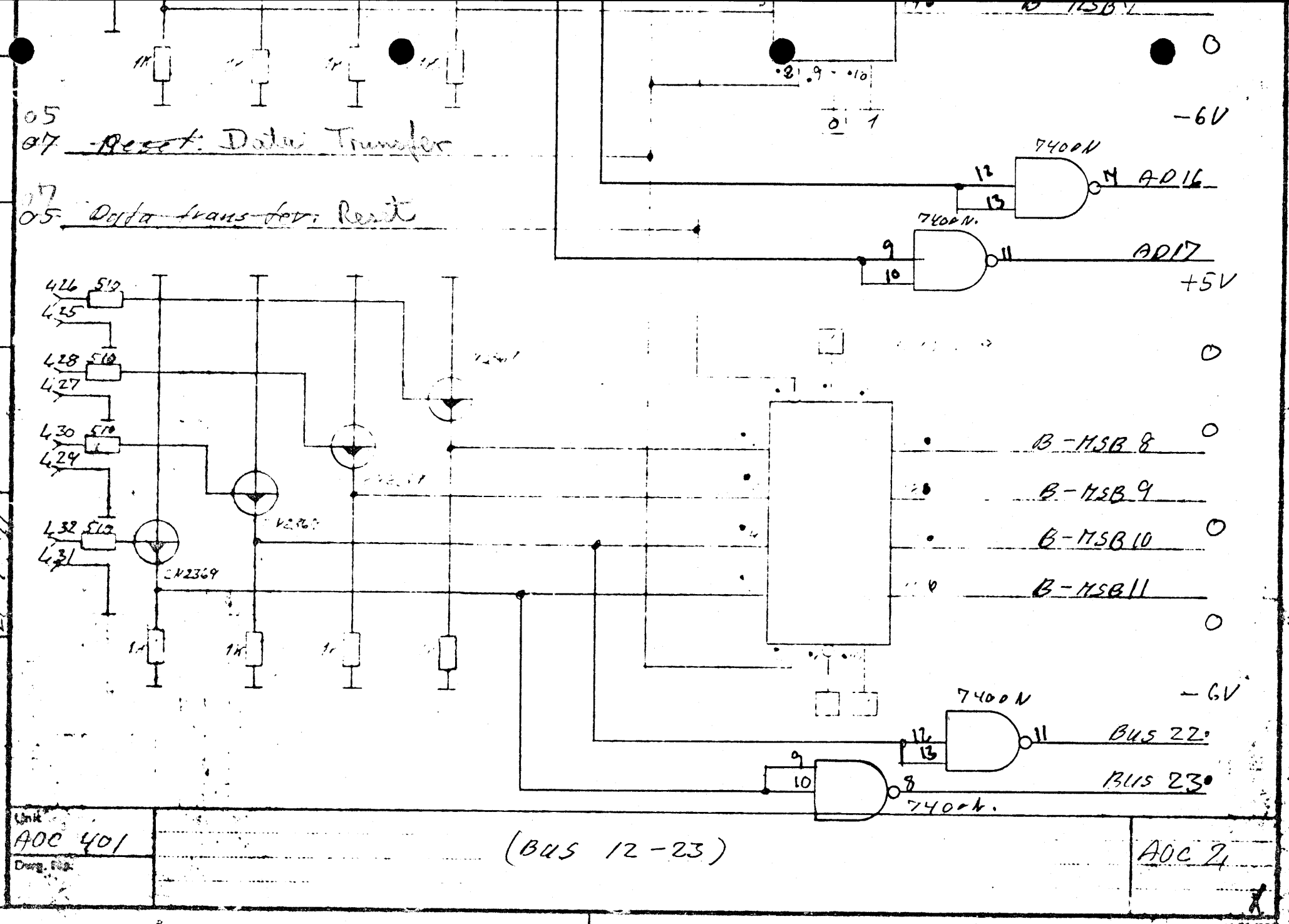
Dwg. No.

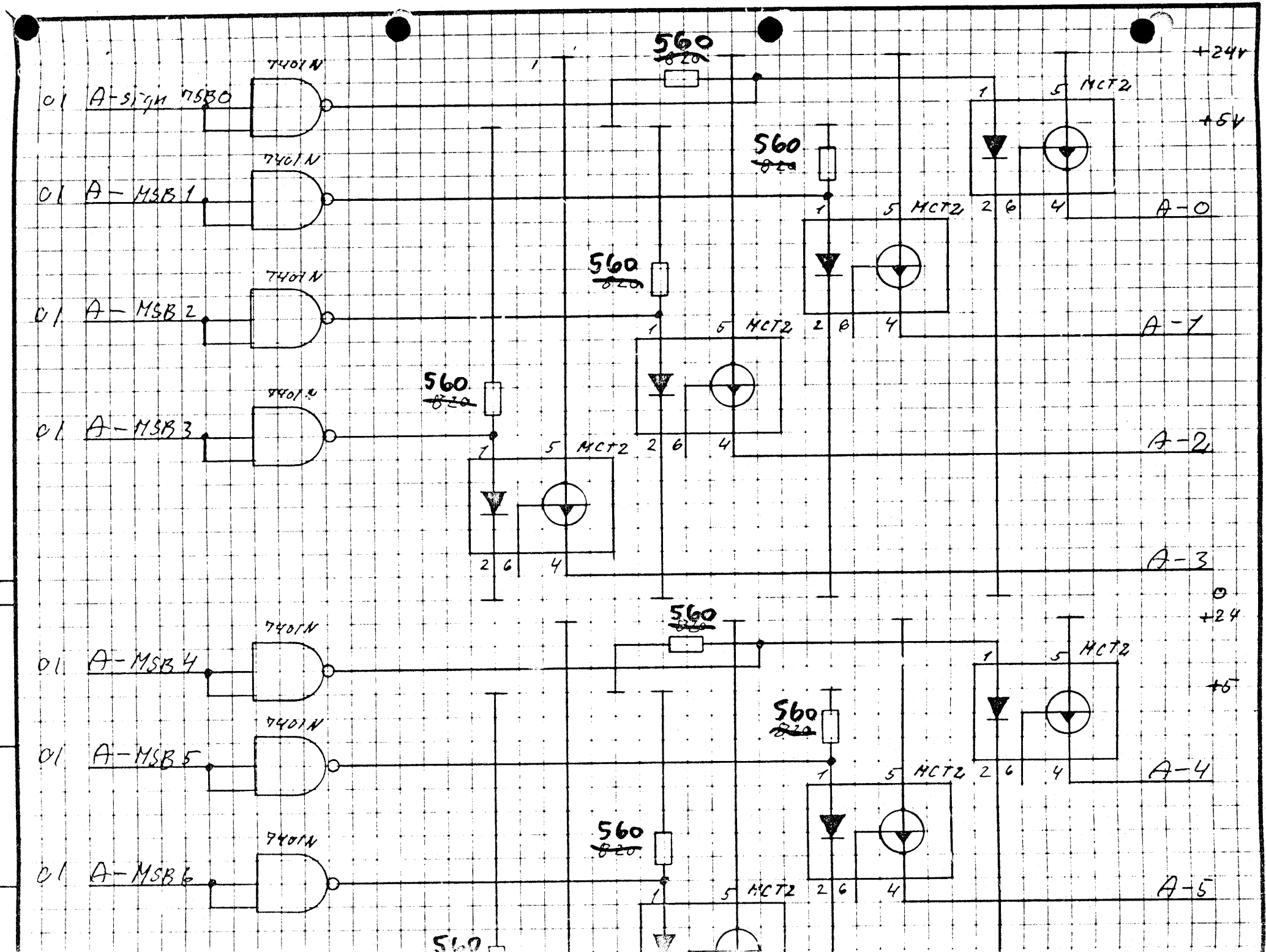
(BUS 0-11)

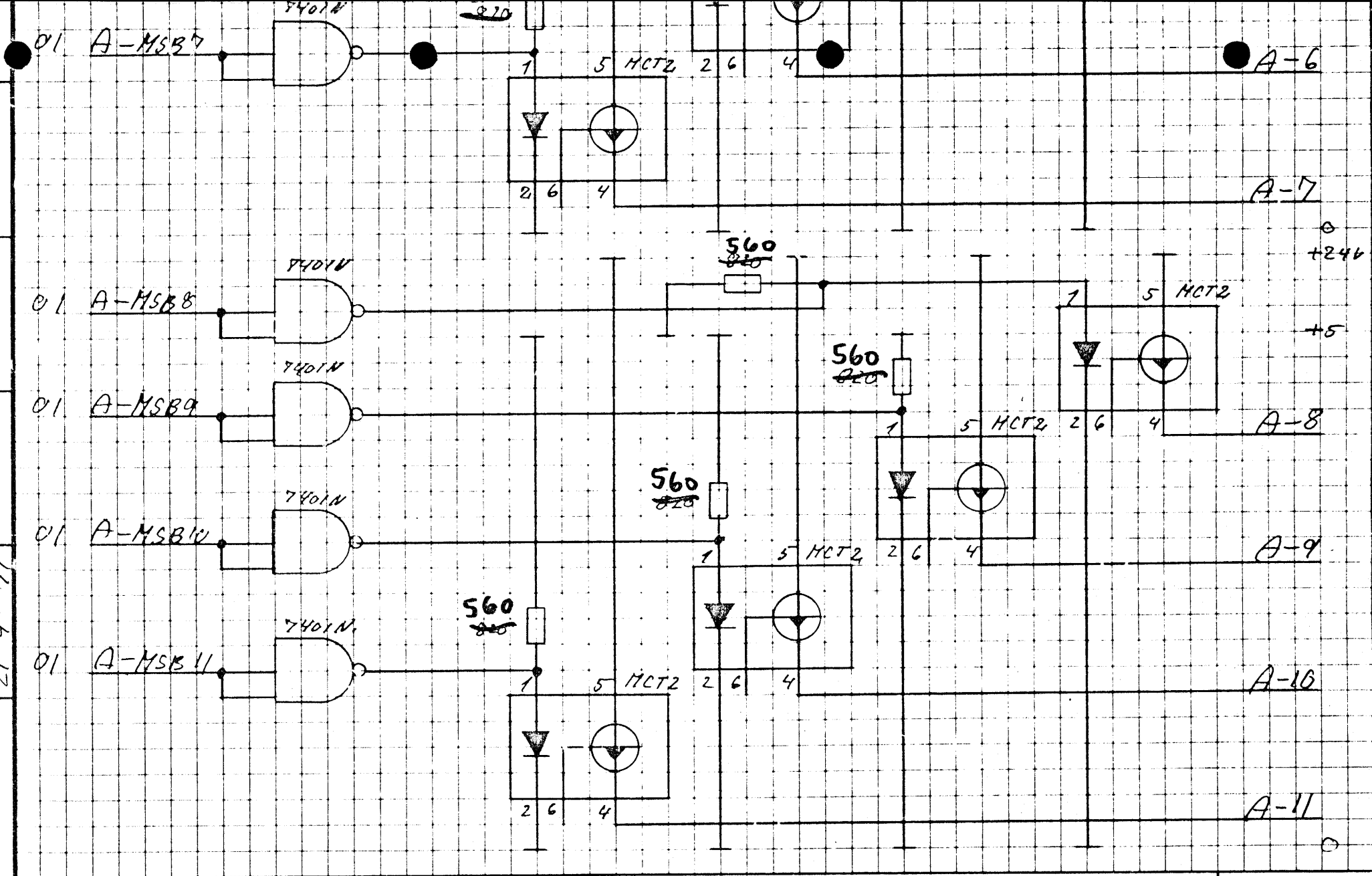
AOC 1

AGF 1973


+5V
7400N
B-Sign MSB
B-MSB 1
B-MSB 2
B-MSB 3
-6V
AD12
AD13
AD14
AD15
+5V
B-MSB 4
B-MSB 5
B-MSB 6
2N2369
Replaced by Dwg. No.
due to ECN
Dwg. No.


05
07 Reset: Data Transfer
17
05 Data transfer: Reset
7400N
7400N.
AD16
AD17
+5V
-6V
B-MSB 8
B-MSB 9
B-MSB 10
B-MSB 11
-6V
7400N
BUS 22
BUS 23
7400N.
CM2369
Designed by: WFL
21-4-71
Drawn by:
Dwg. Office Check
Design Check
Replaced
A/S REGNECENTRALEN
Unit
AOC 401
Dwg. No.
(BUS 12-23)
AOC 24


7401N
01 A-SIGN MSB0
01 A-MSB1
01 A-MSB2
01 A-MSB3
01 A-MSB4
01 A-MSB5
01 A-MSB6
560
560
560
560
560
560
560
MCT2
MCT2
MCT2
MCT2
MCT2
MCT2
MCT2
+24V
+5V
A-0
A-1
A-2
A-3
+24
+5
A-4
A-5
Replaced by Dwg. No.
due to ECN
Dwg. No.



Replaces D

Design Check

Dwg. Office Check

Drawn by

Designed by HFH 21-4-71

A/S REGNECENTRALEN

Unit
AOC 401

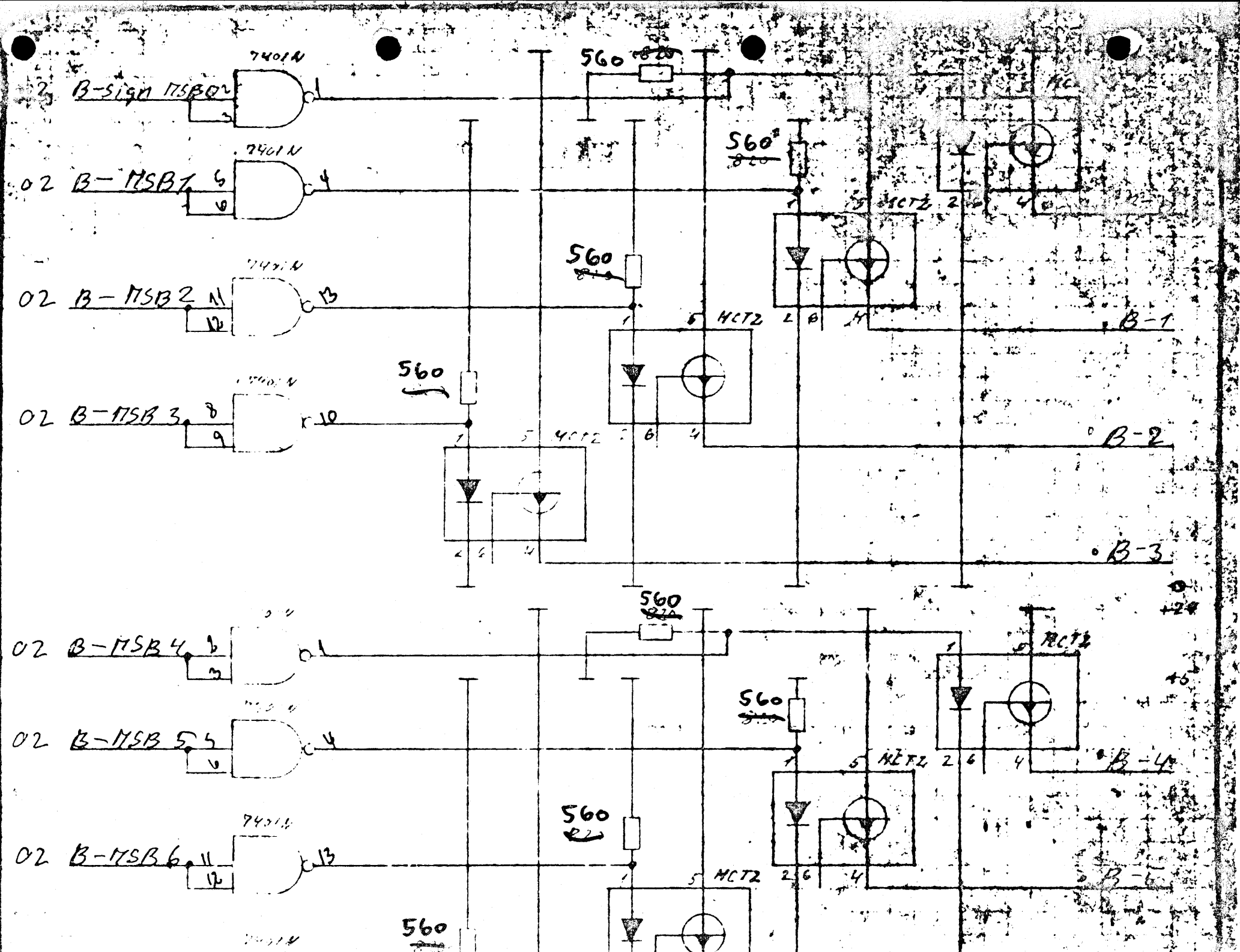
Dwg. No.

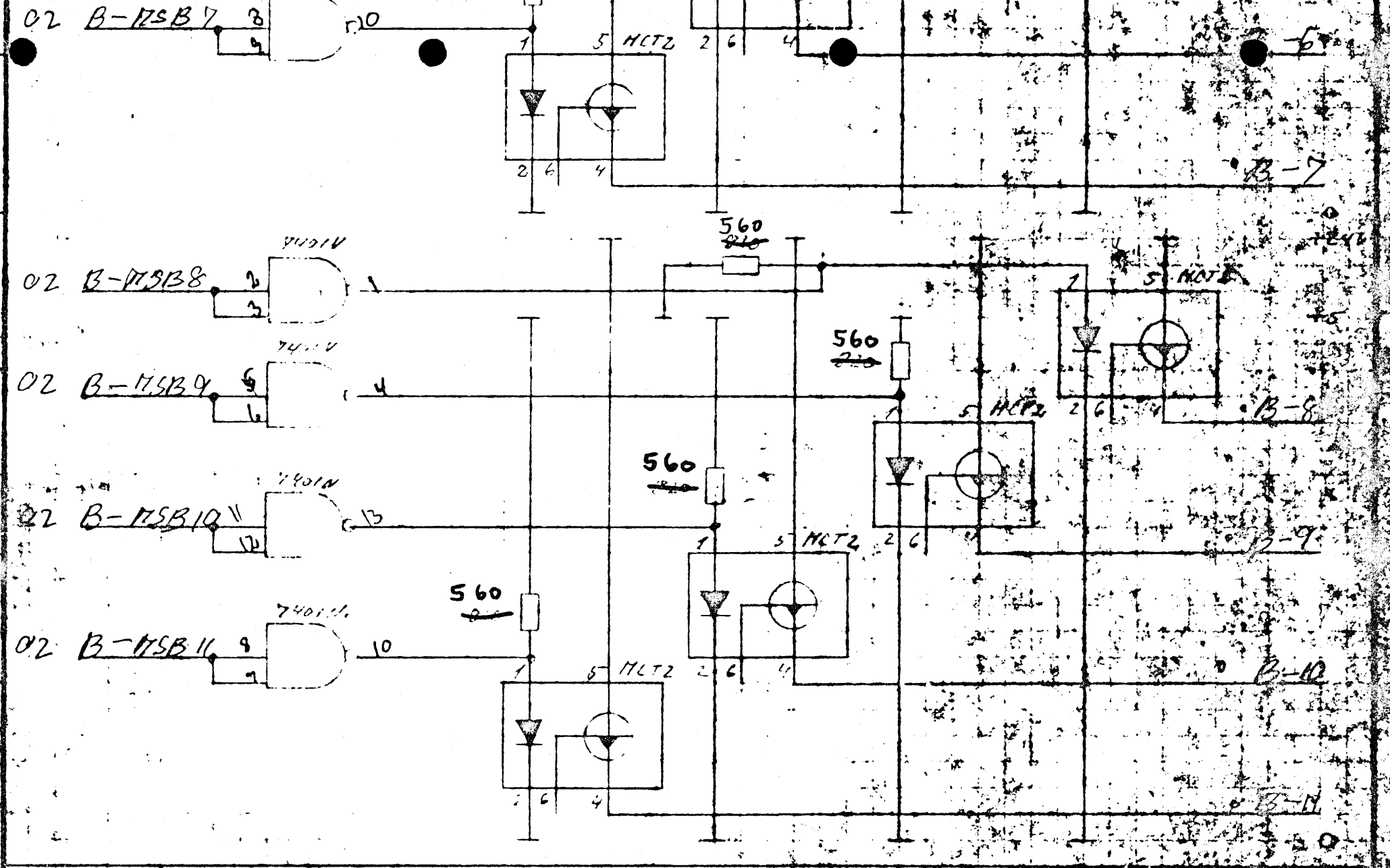
Galvanic separation.

AOC 3

RC doc: VB 140

AGF 1973


7401N
B-Sign MSBQ
02 B-MSB 1
02 B-MSB 2
02 B-MSB 3
02 B-MSB 4
02 B-MSB 5
02 B-MSB 6
560
HCT2
B-1
B-2
B-3
B-4
Replaced by Dwg. No.
Add to ECN
Dwg. No.



Unit	AOC 401
Dwg. No.	

Galvanic separation

AOC 4

~~190669FBP~~ 171170SSL 191670SSL 231170 FBP

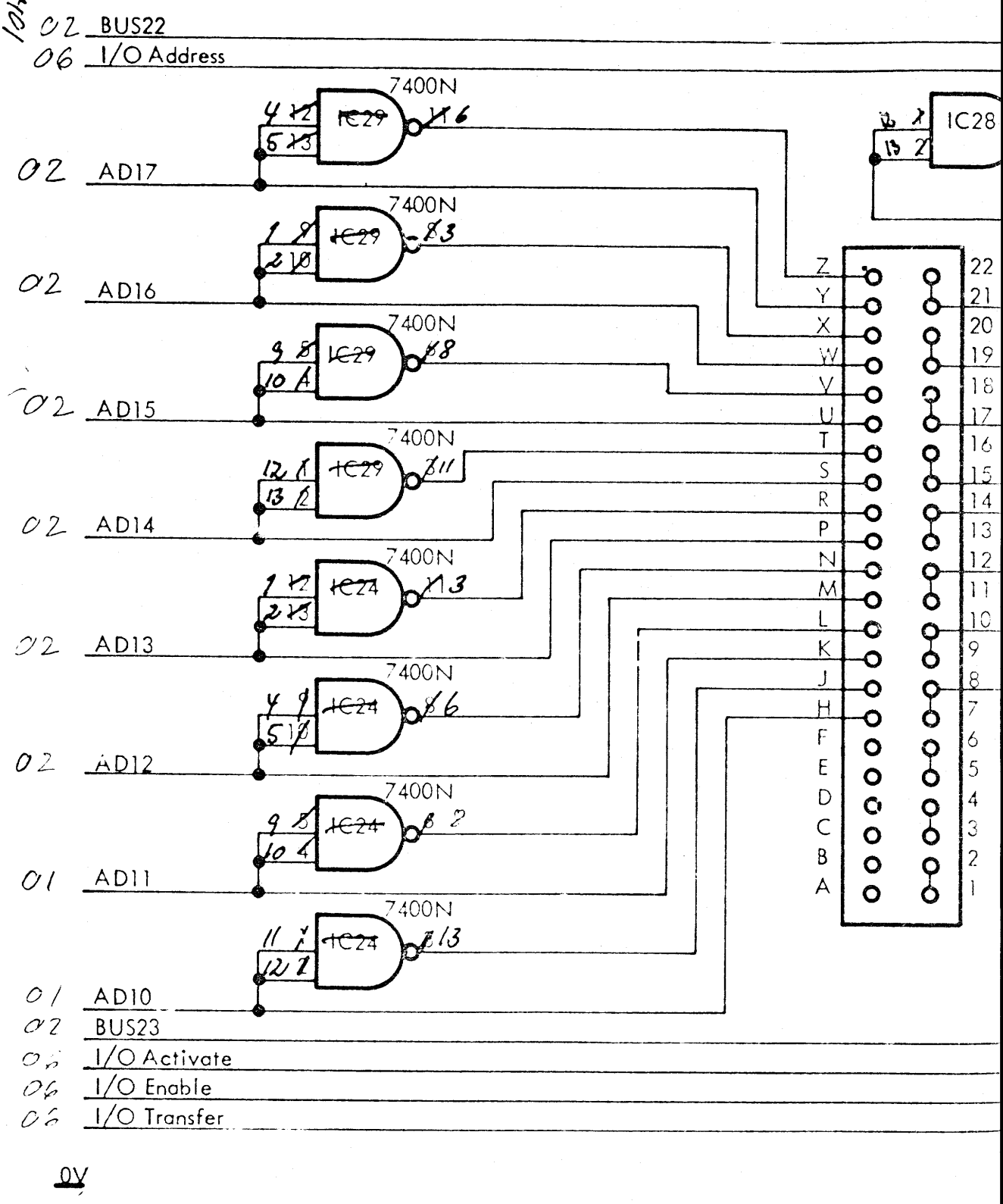
4F4

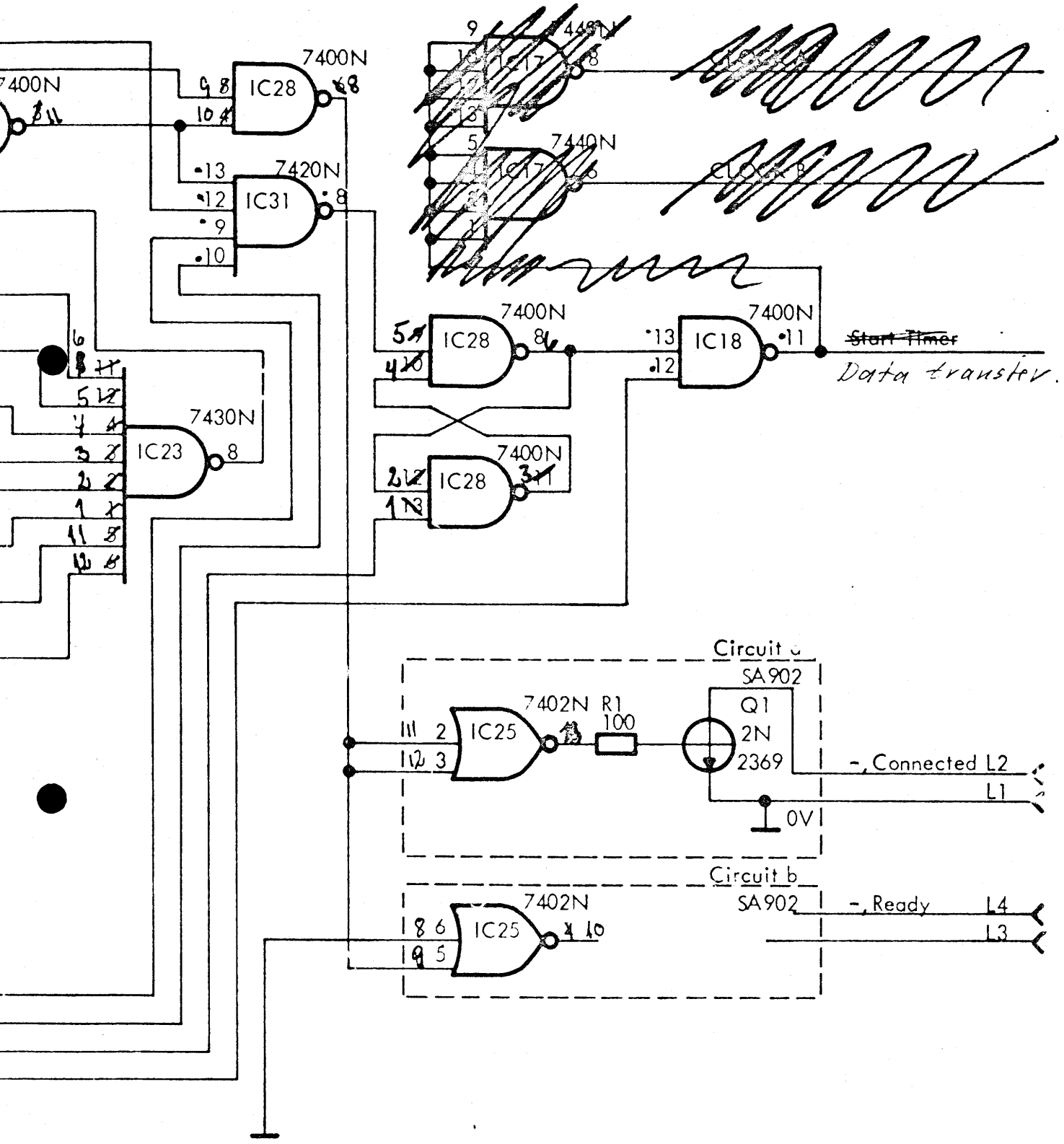
21-4-71

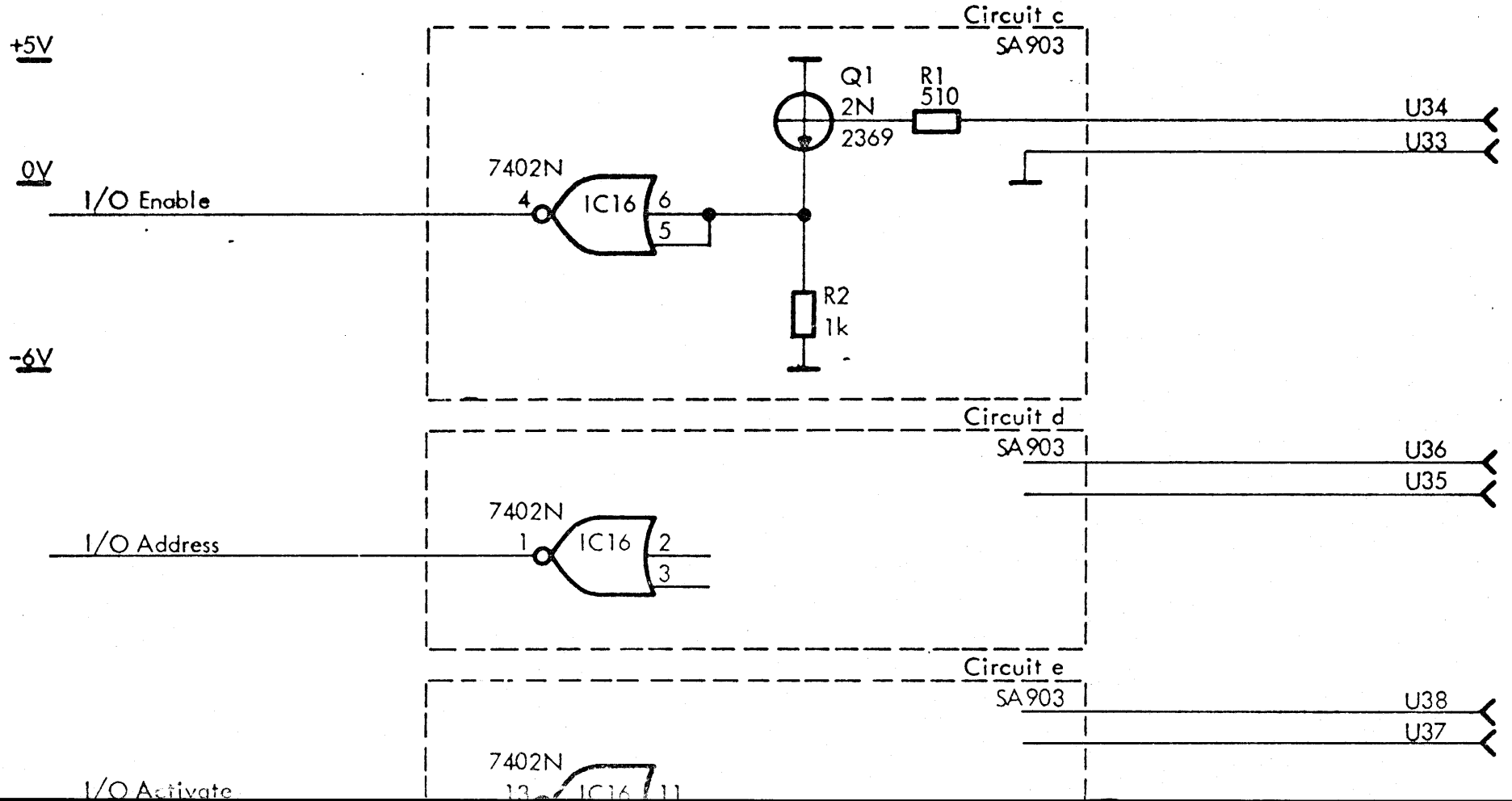
V12135

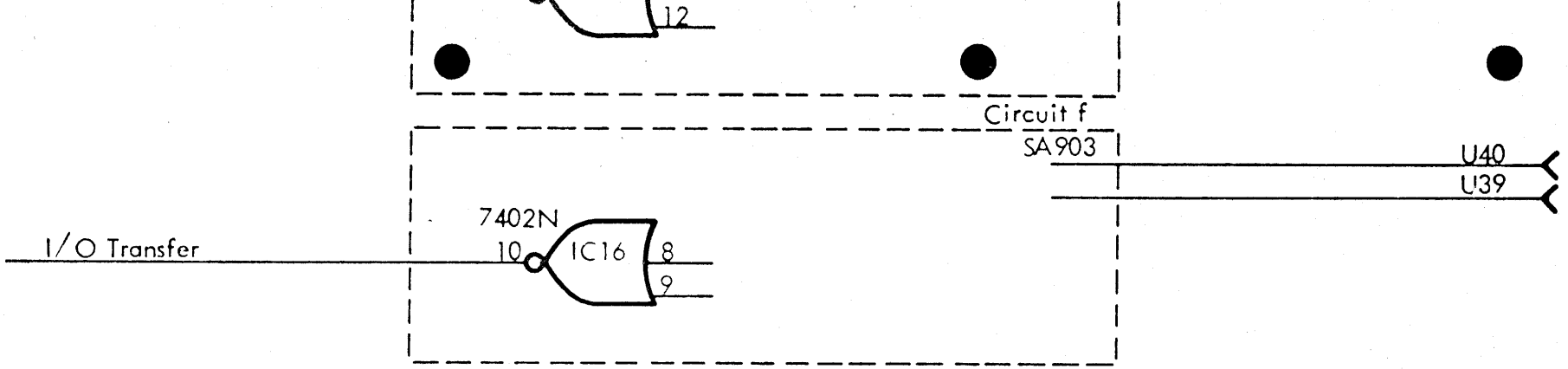
PCBA Circuit Diagram

ADDRESS DECODING, READY, CONNECTED AND INTERRUPT GENERATOR




7400N
IC28
7420N
IC31
7430N
IC23
7440N
IC17
IC18
Start Timer
Data transfer.
Circuit a
SA902
7402N
IC25
R1
100
Q1
2N
2369
Connected L2
L1
0V
Circuit b
Ready
L4
L3


Circuit c
SA903
+5V
0V
-6V
I/O Enable
7402N
4
IC16
6
5
Q1
2N
2369
R1
510
R2
1k
U34
U33
Circuit d
SA903
I/O Address
7402N
1
IC16
2
3
U36
U35
Circuit e
SA903
I/O Activate
7402N
IC16
U38
U37



~~1Z1170SSL~~ ~~1Y1170SSL 1Y1170 FBP~~

~~180669FBP~~

4 FL
2-4-77

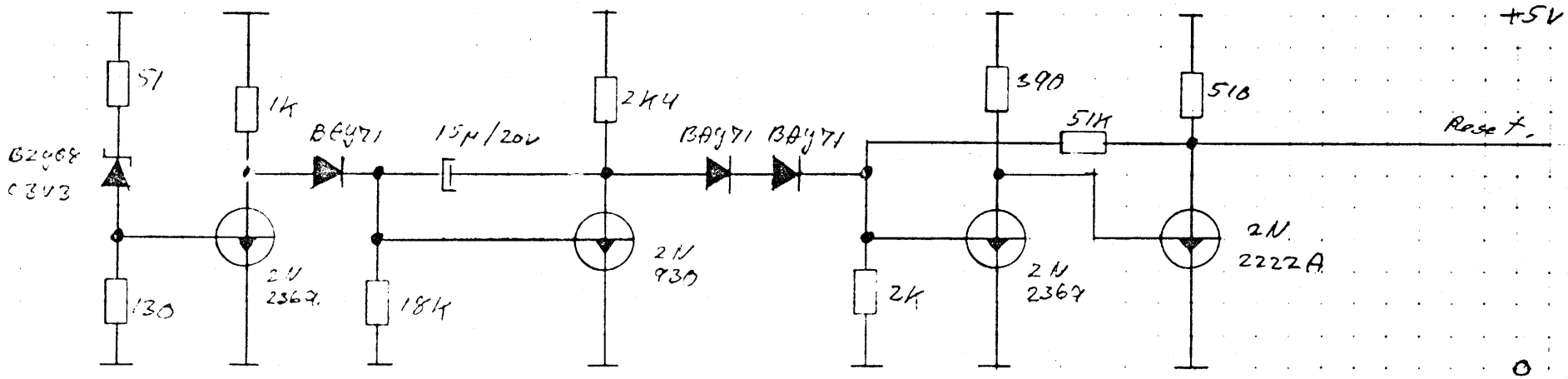
AOC401
~~DOT401~~

~~V12138~~

RECEIVERS FOR I/O BUS CONTROL SIGNALS

PCBA Circuit Diagram

AOC6
~~DOT003~~



Dwg. No.	due to ECN	Replaced by Dwg. No.

A/S REGNECENTRALEN

Designed by	Drawn by	Dwg. Office Check	Design Check	Replaces
MFL 21-11-71				

Unit: 40C401

Dwg. No.:

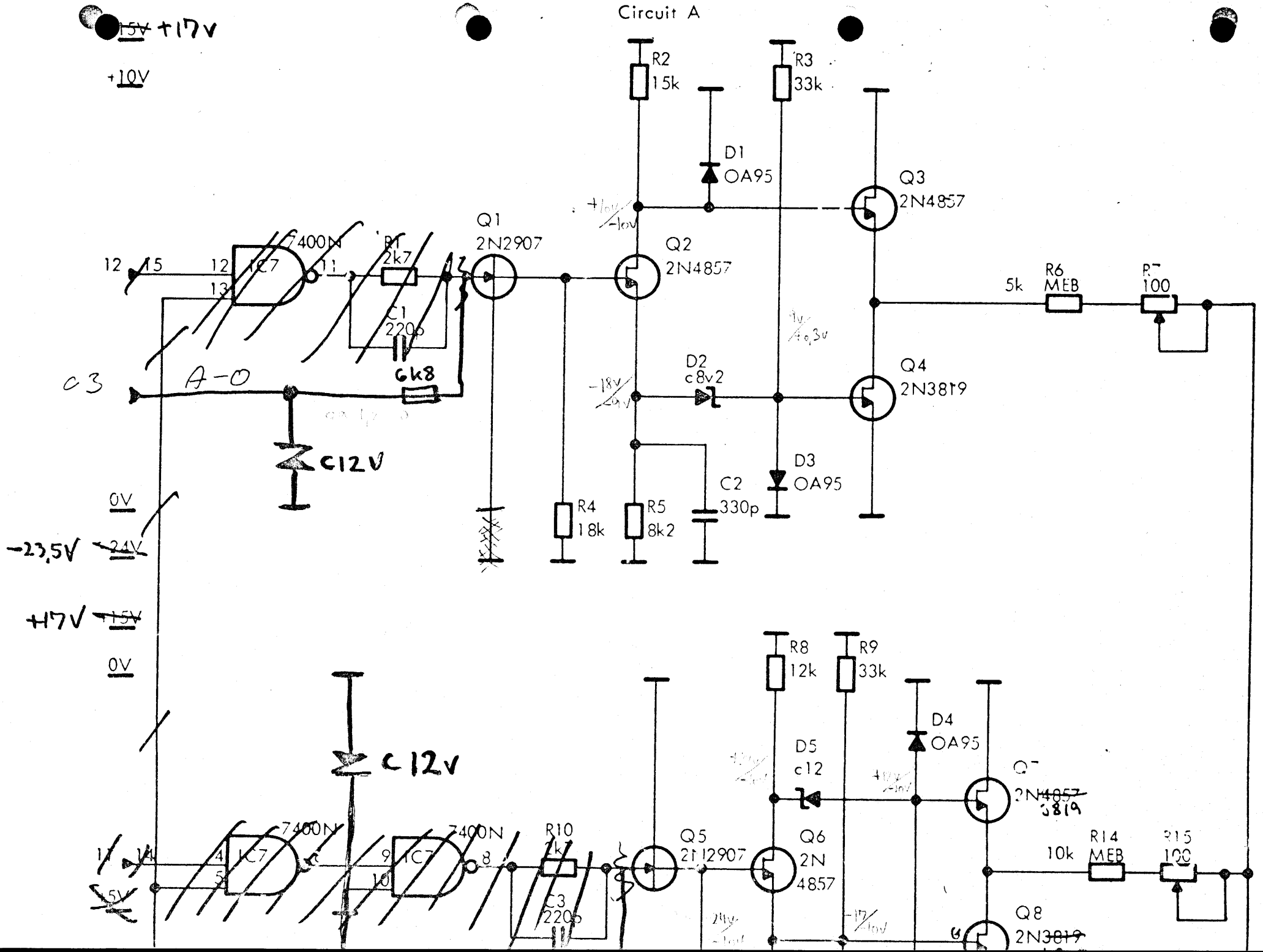
Power start up circuit.

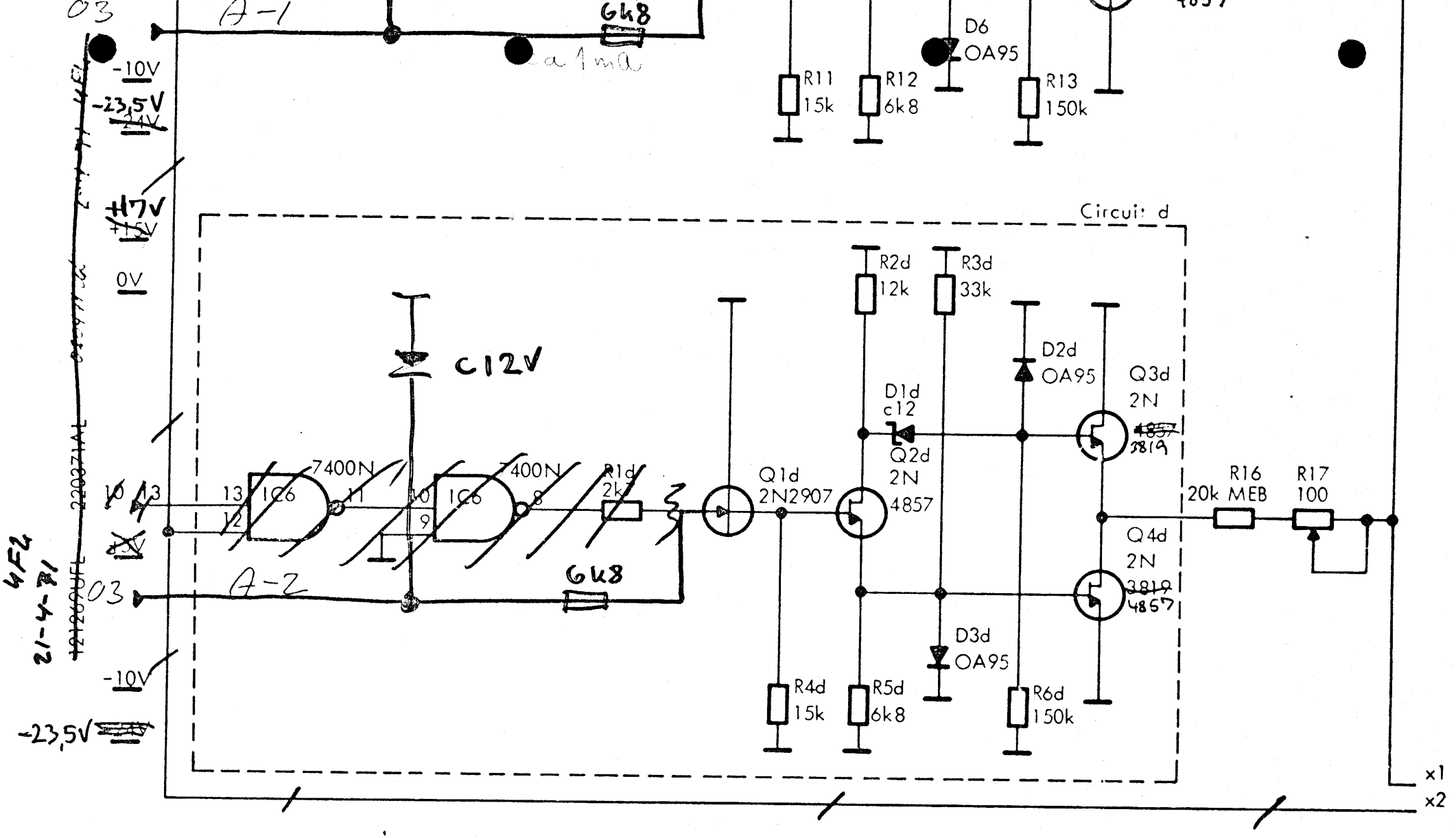
AOC 7

X

RC doc. VB 140

AGF 1973


Circuit A
+17v
+10V
R2
15k
R3
33k
D1
OA95
Q3
2N4857
Q1
2N2907
Q2
2N4857
7400N
IC7
R1
2k7
C1
220p
6k8
A-O
C12V
D2
c8v2
Q4
2N3819
5k
R6
MEB
R7
100
R4
18k
R5
8k2
C2
330p
D3
OA95
0V
-23,5V
-24V
+17V
+15V
0V
C12V
R8
12k
R9
33k
D4
OA95
D5
c12
Q5
2N2907
Q6
2N
4857
Q7
2N3819
R10
2k7
C3
220p
R14
10k
MEB
R15
100
Q8
2N3819



AOC401

~~RCLM400~~

~~V12632~~

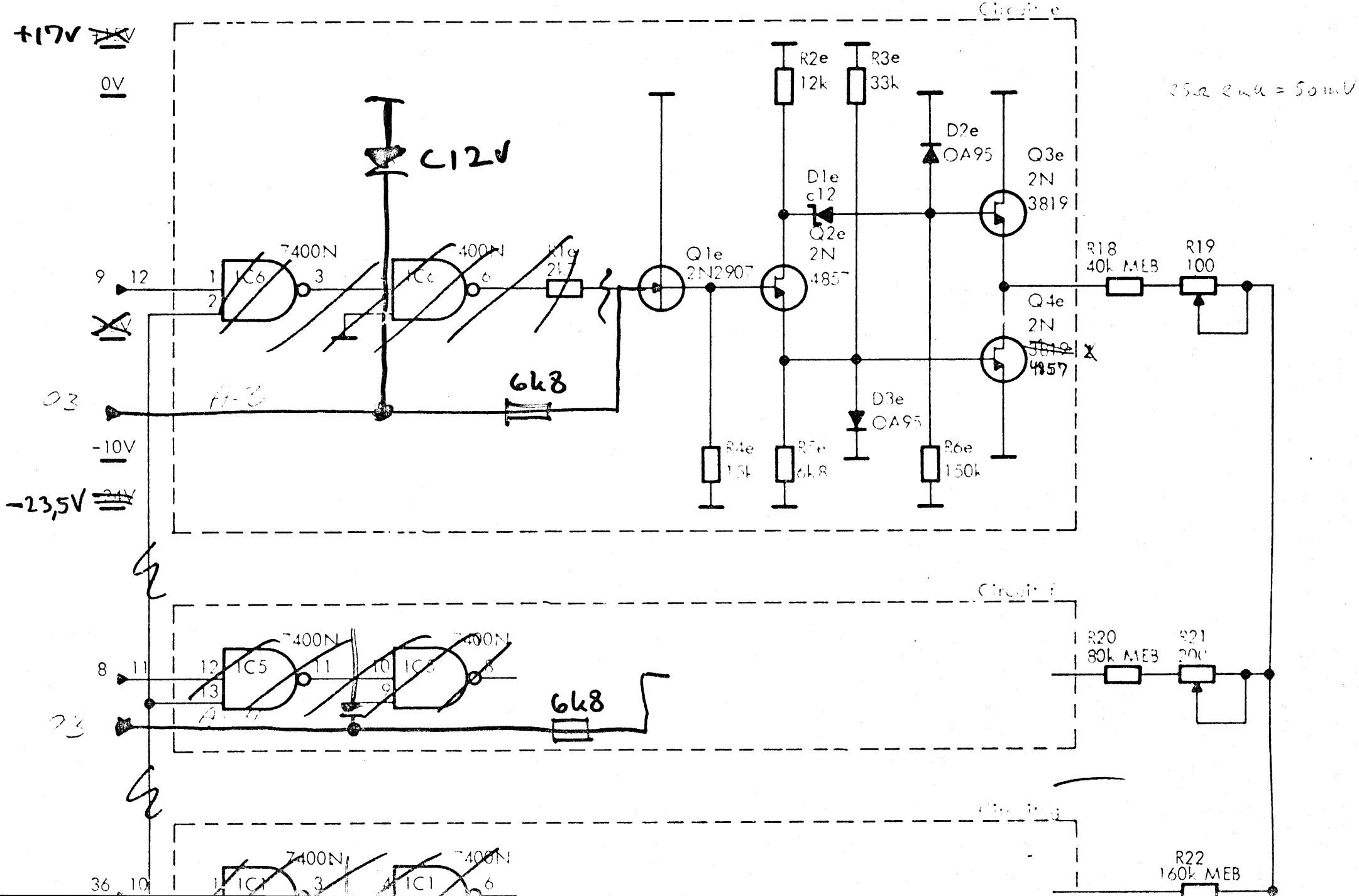
Analog switches. -A

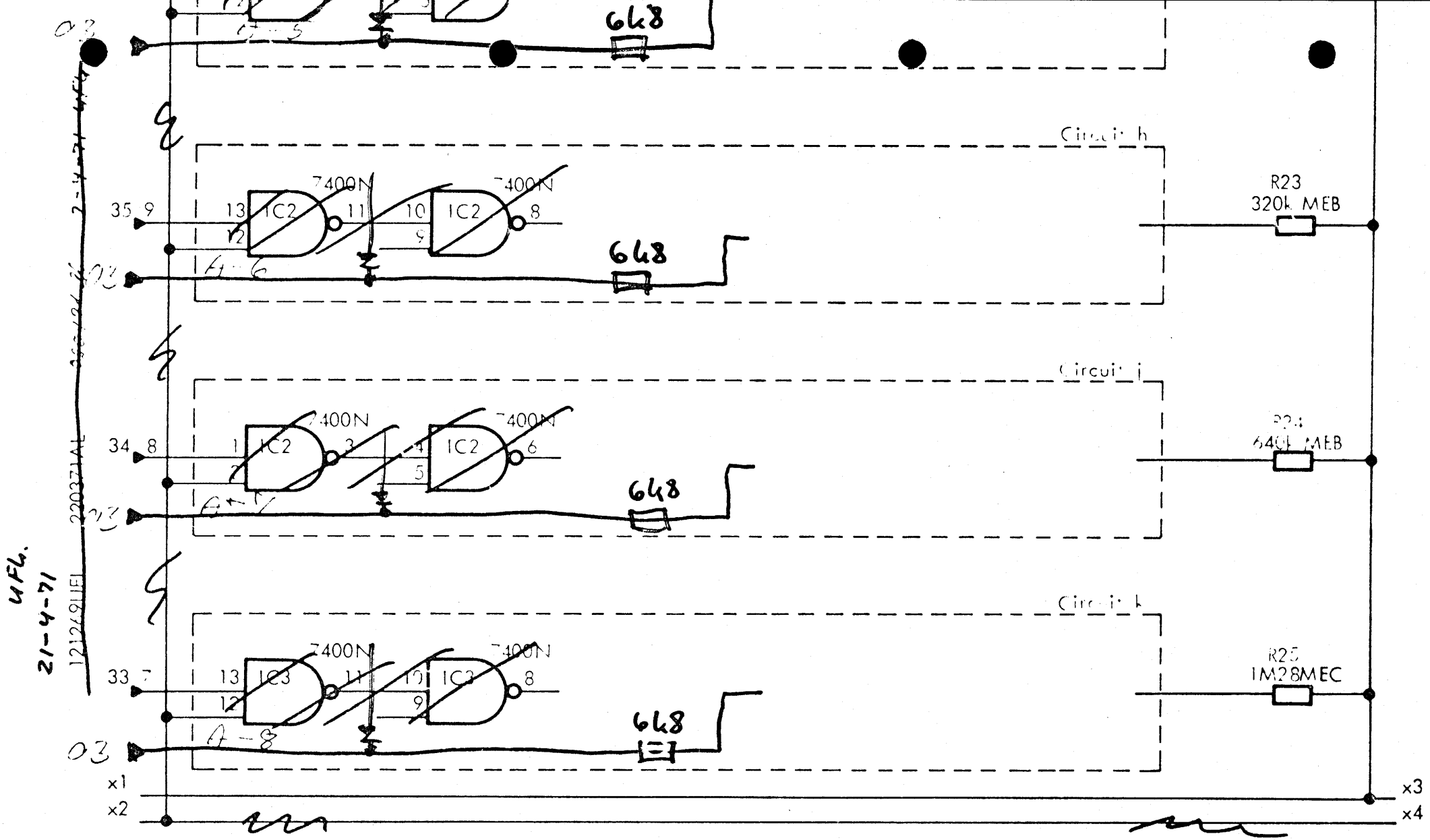
~~TFD401~~

PCBA Circuit Diagram

AOC8

~~RC0937-1~~
~~RC0938-1~~
~~RC0939-1~~
p.1 of 5


+17V
0V
C12V
-10V
-23,5V
R2e
12k
R3e
33k
D2e
OA95
Q3e
2N
3819
D1e
c12
Q2e
2N
4857
Q1e
2N2907
R18
40k MEB
R19
100
Q4e
2N
4857
6k8
D3e
OA95
R4e
15k
R5e
6k8
R6e
150k
7400N
IC6
IC5
IC1
R20
80k MEB
R22
160k MEB
6k8
6k8



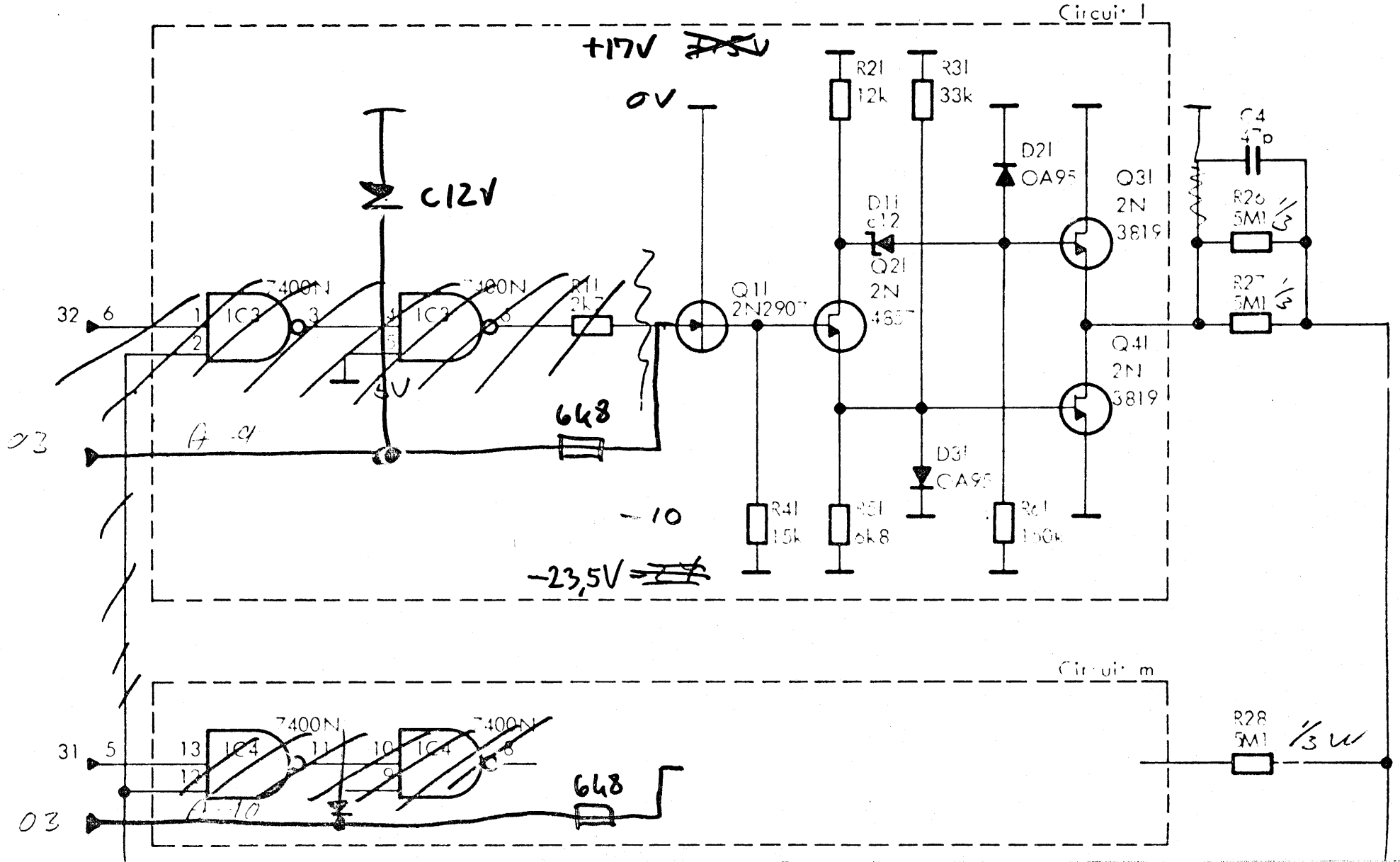
AOC 401
~~RCLM400~~

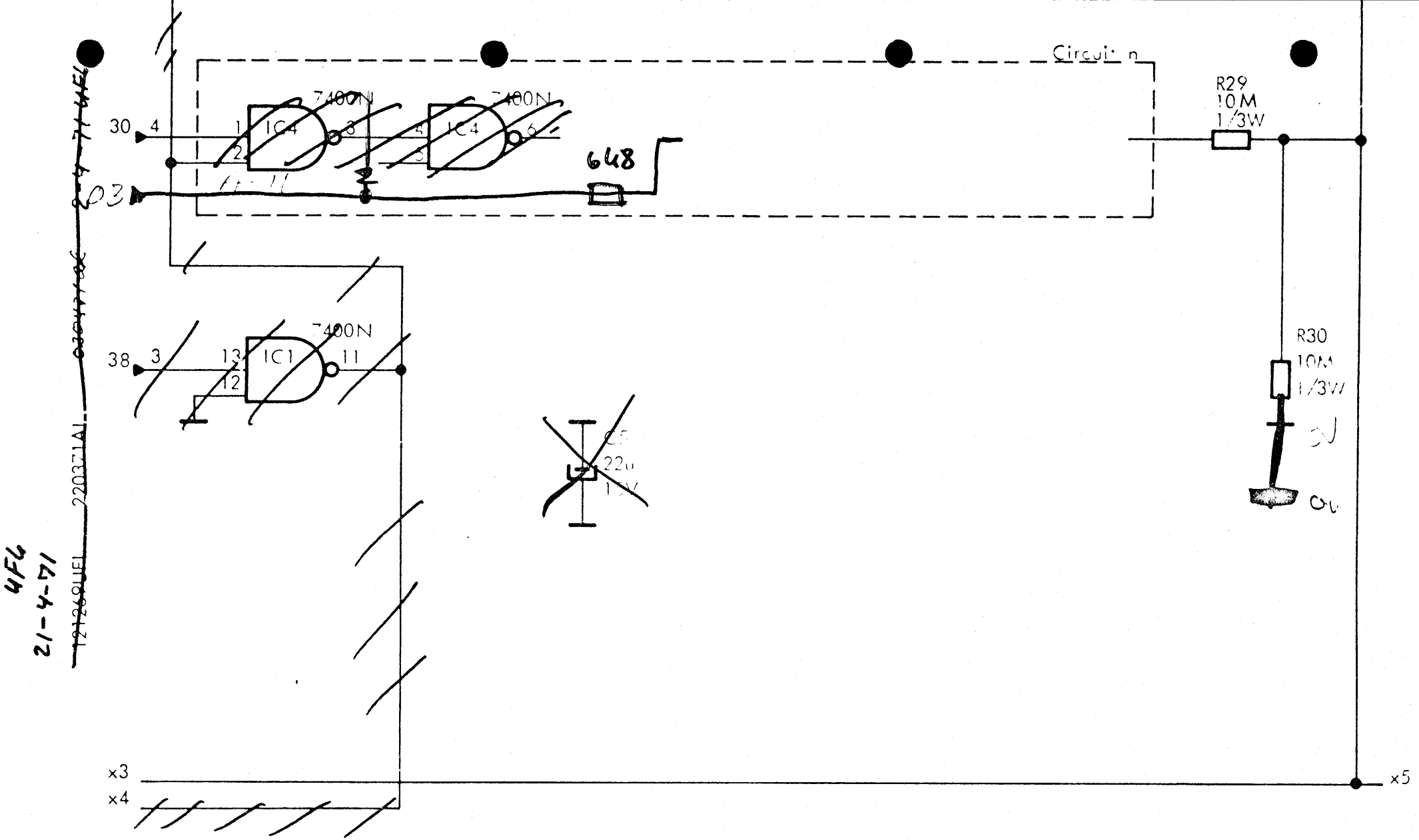
V12633

Analog switches - A
~~1FD 401~~

PCBA Circuit Diagram

AOC 9
~~RC0937-1~~
~~RC0938-1~~
~~RC0939-1~~
~~p. 2 of 5~~


Circuit I
+17V
0V
C12V
R2I
12k
R3I
33k
D2I
OA95
D1I
C12
Q2I
2N
4857
Q3I
2N
3819
Q4I
2N
3819
C4
47p
R26
5M1
1/3
R27
5M1
1/3
32
6
IC3
7400N
Q1I
2N2907
R1I
2k7
648
03
A-9
D3I
OA95
-10
R4I
15k
R5I
6k8
R6I
150k
-23,5V
Circuit m
31
5
IC4
7400N
648
03
A-10
R28
5M1
1/3 W



4/6
21-4-71

RGLM400
AOC 401
V12634

Analog switches. -A
ED 101

PCBA Circuit Diagram

AOC10
RC0937-1
RC0938-1
RC0939-1
p 3 of 3

~~121269UFL 220371AL 080471AL 2-4-71 4FL~~

21-4-71
4FL.

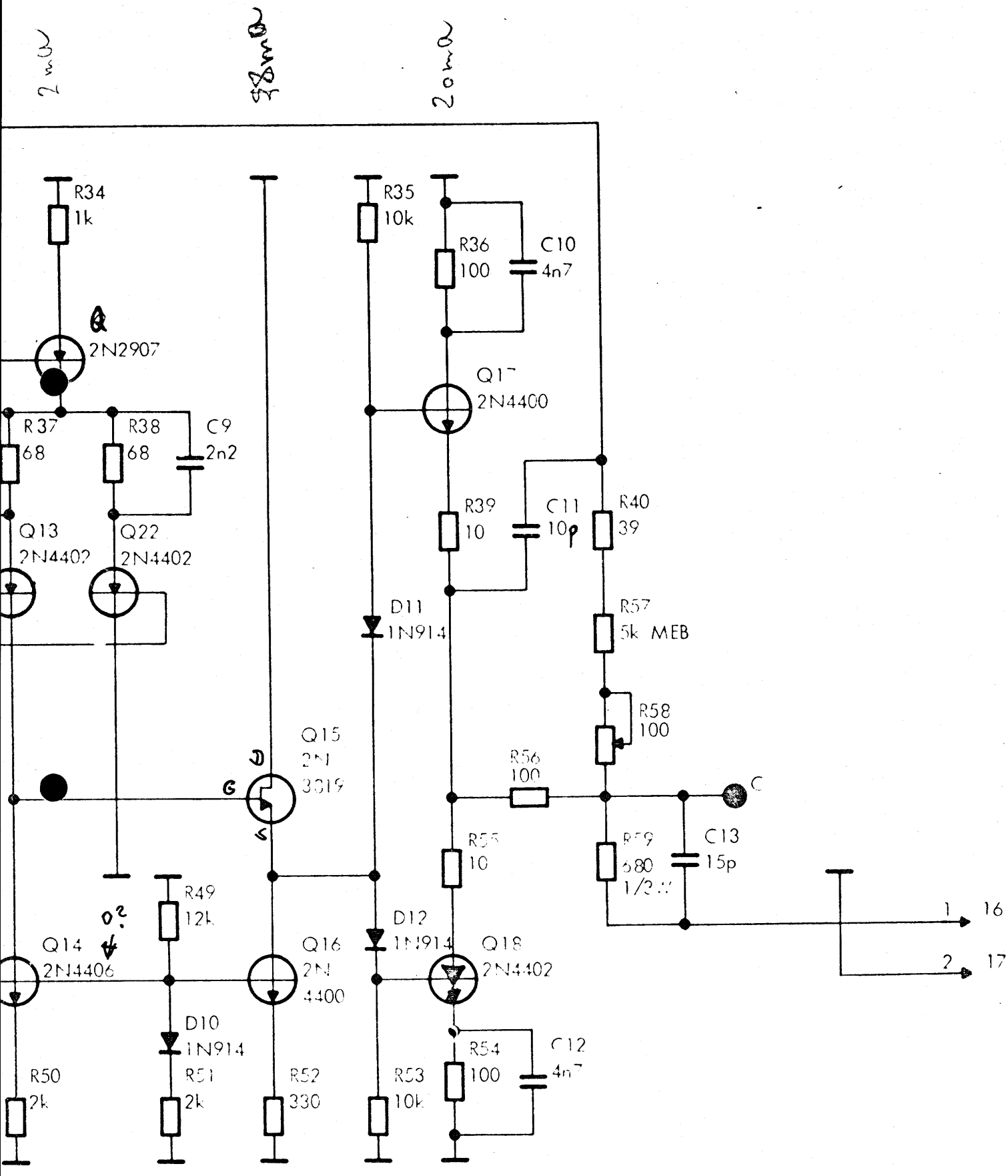
AOC401
~~RCE11800~~
~~X12635~~

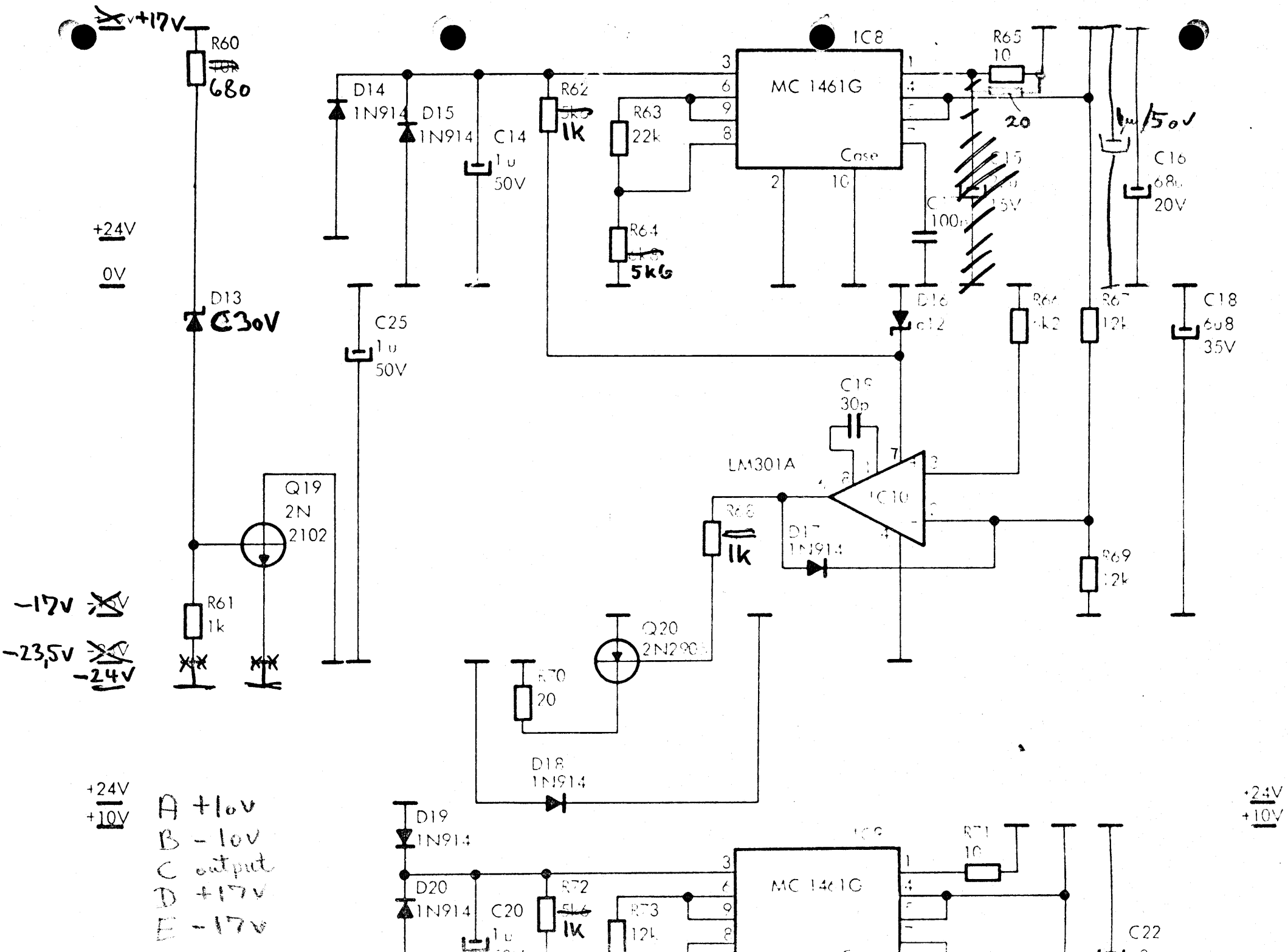
PCBA Circuit Diagram

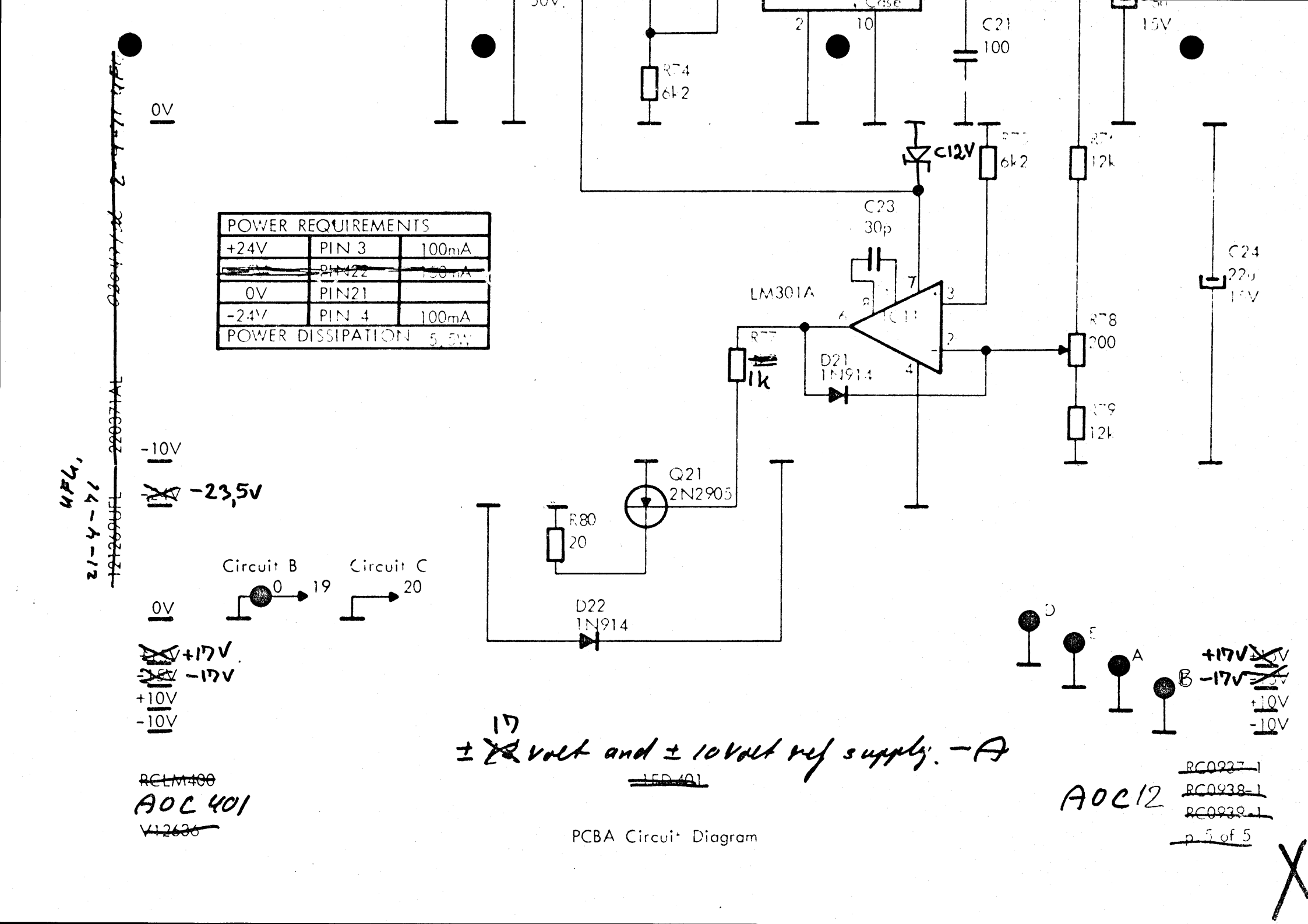
output amplifier -A

~~EB401~~

AOC11
~~RCE0837-1~~
~~RCE0838-1~~
~~RCE0839-1~~


R34
1k
R35
10k
R36
100
C10
4n7
Q
2N2907
Q17
2N4400
R37
68
R38
68
C9
2n2
Q13
2N4402
Q22
2N4402
R39
10
C11
10p
R40
39
D11
1N914
R57
5k MEB
R58
100
Q15
2N
3819
R56
100
C
R55
10
R59
680
1/2W
C13
15p
R49
12k
D12
1N914
Q18
2N4402
Q14
2N4406
Q16
2N
4400
D10
1N914
R54
100
C12
4n7
R50
2k
R51
2k
R52
330
R53
10k
1
16
2
17


+17V
R60
680
D14
1N914
D15
1N914
C14
1u
50V
R62
1k
IC8
MC 1461G
R63
22k
R64
5kG
Case
R65
10
20
C15
15V
C16
68u
20V
1u/50V
+24V
0V
D13
C30V
C25
1u
50V
D16
C12
R66
1k2
R67
12k
C18
6u8
35V
C19
30p
LM301A
IC10
R68
1k
D17
1N914
R69
12k
Q19
2N
2102
-17V
R61
1k
-23,5V
-24V
Q20
2N2905
R70
20
D18
1N914
+24V
+10V
A +10V
B -10V
C output
D +17V
E -17V
D19
1N914
D20
1N914
C20
1u
R72
1k
MC 1461G
R73
12k
R71
10
C22
+24V
+10V



POWER REQUIREMENTS		
+24V	PIN 3	100mA
~~-24V~~	~~PIN 22~~	~~150mA~~
0V	PIN21	
-24V	PIN 4	100mA
POWER DISSIPATION 5.5W		

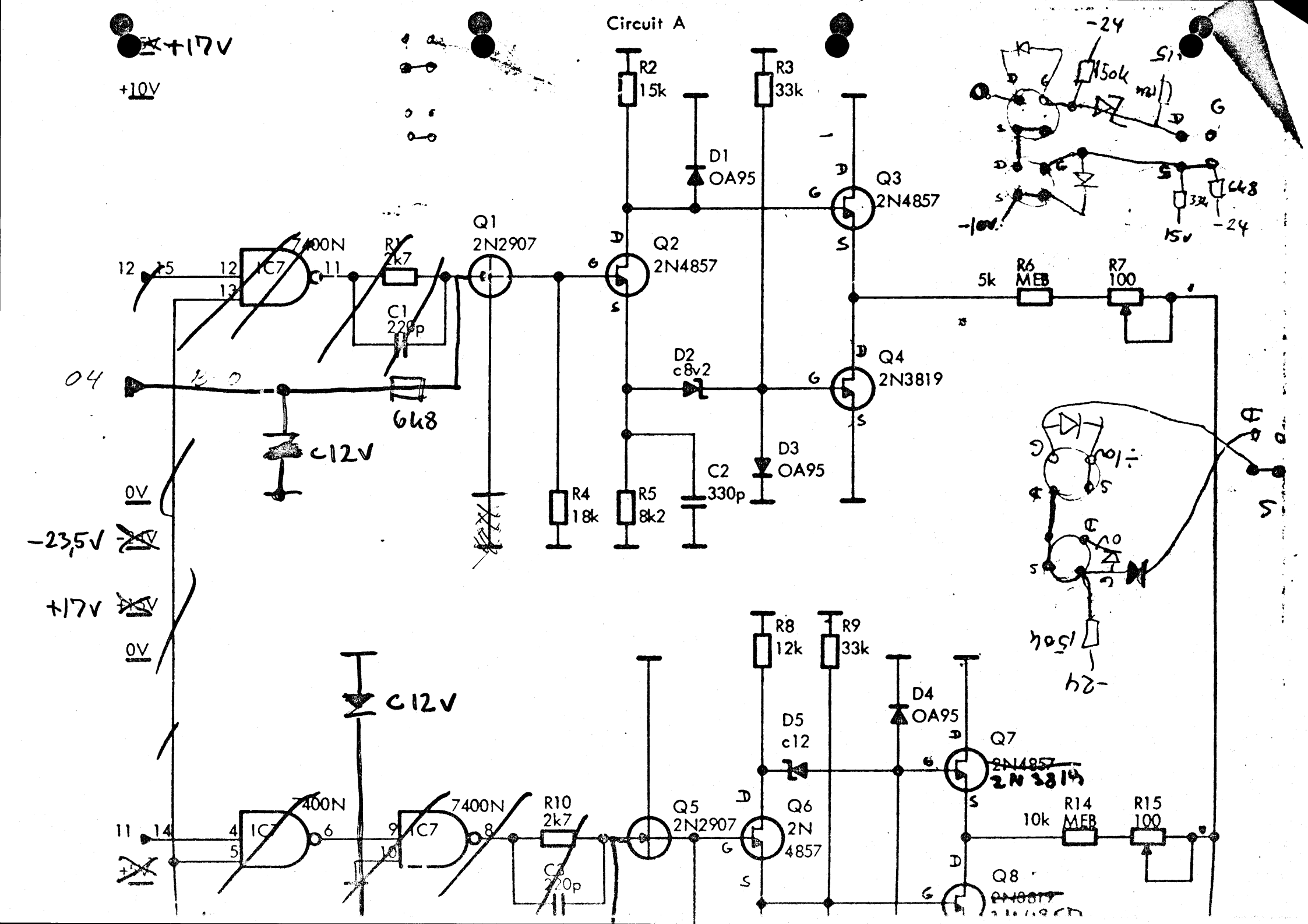
~~RCLM400~~
AOC 401
~~V12636~~

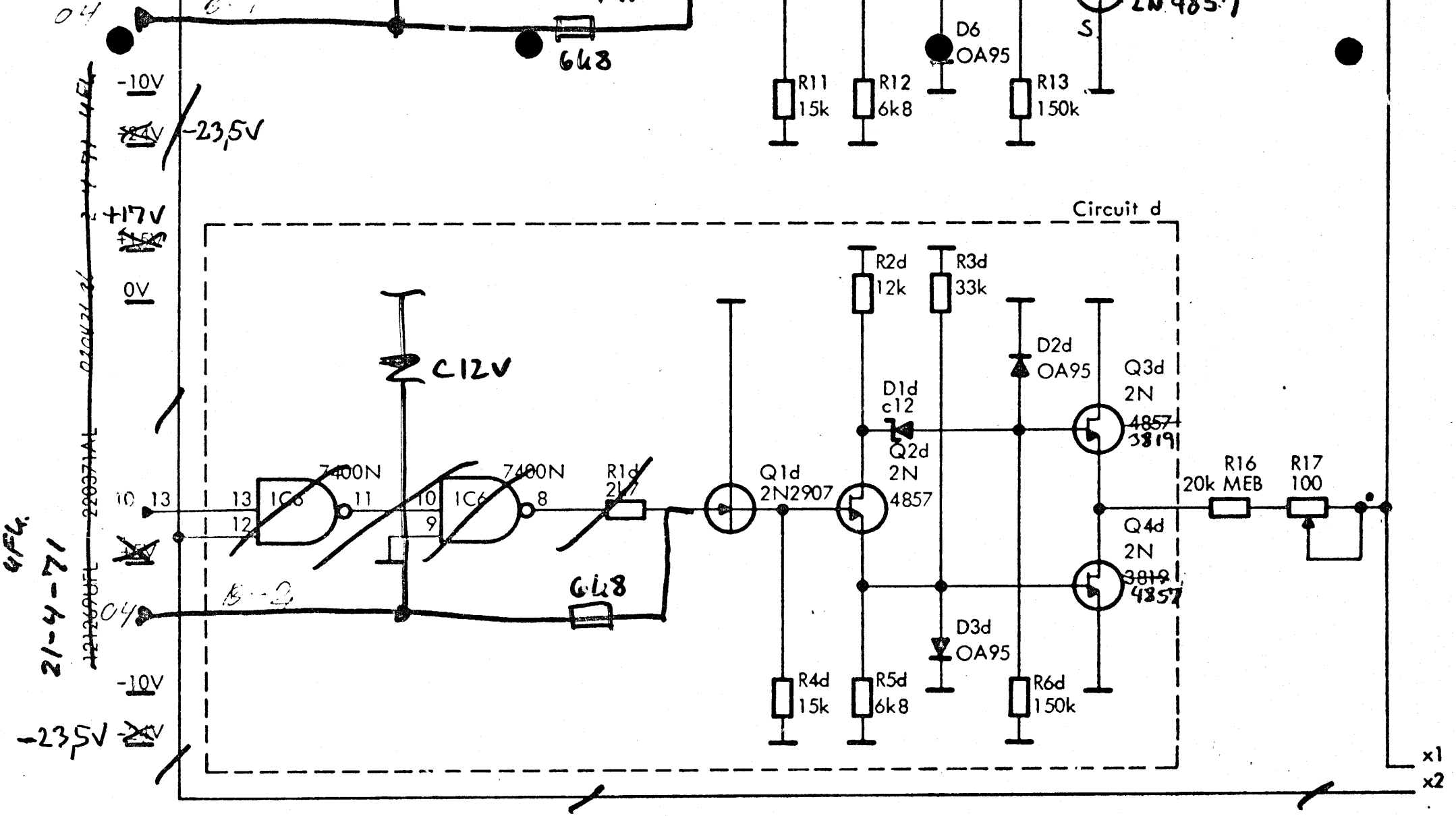
± 17 volt and ± 10 volt ref supply. -A

~~15D401~~

PCBA Circuit Diagram

AOC12
~~RC0937-1~~
~~RC0938-1~~
~~RC0939-1~~
p 5 of 5


Circuit A
+17V
+10V
R2
15k
R3
33k
D1
OA95
Q3
2N4857
Q1
2N2907
Q2
2N4857
7400N
IC7
R1
2k7
C1
220p
648
c12V
0V
-23,5V
+17V
D2
c8v2
Q4
2N3819
D3
OA95
C2
330p
R4
18k
R5
8k2
5k
R6
MEB
R7
100
-24
1504
-10V
15V
-24
R8
12k
R9
33k
D4
OA95
D5
c12
Q7
2N3819
R10
2k7
C3
220p
Q5
2N2907
Q6
2N
4857
R14
10k
MEB
R15
100
Q8
150k
-24



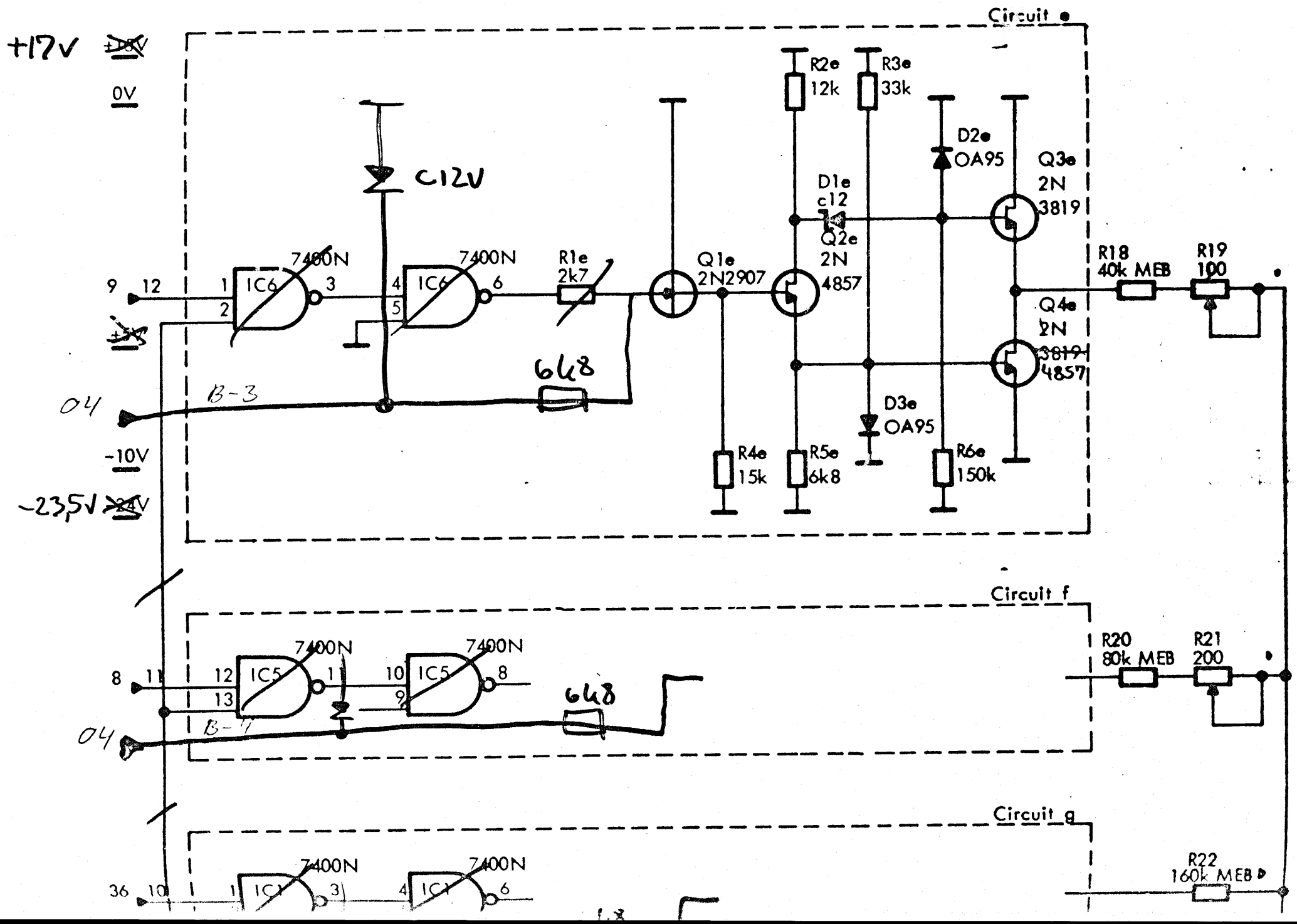
AOC 401

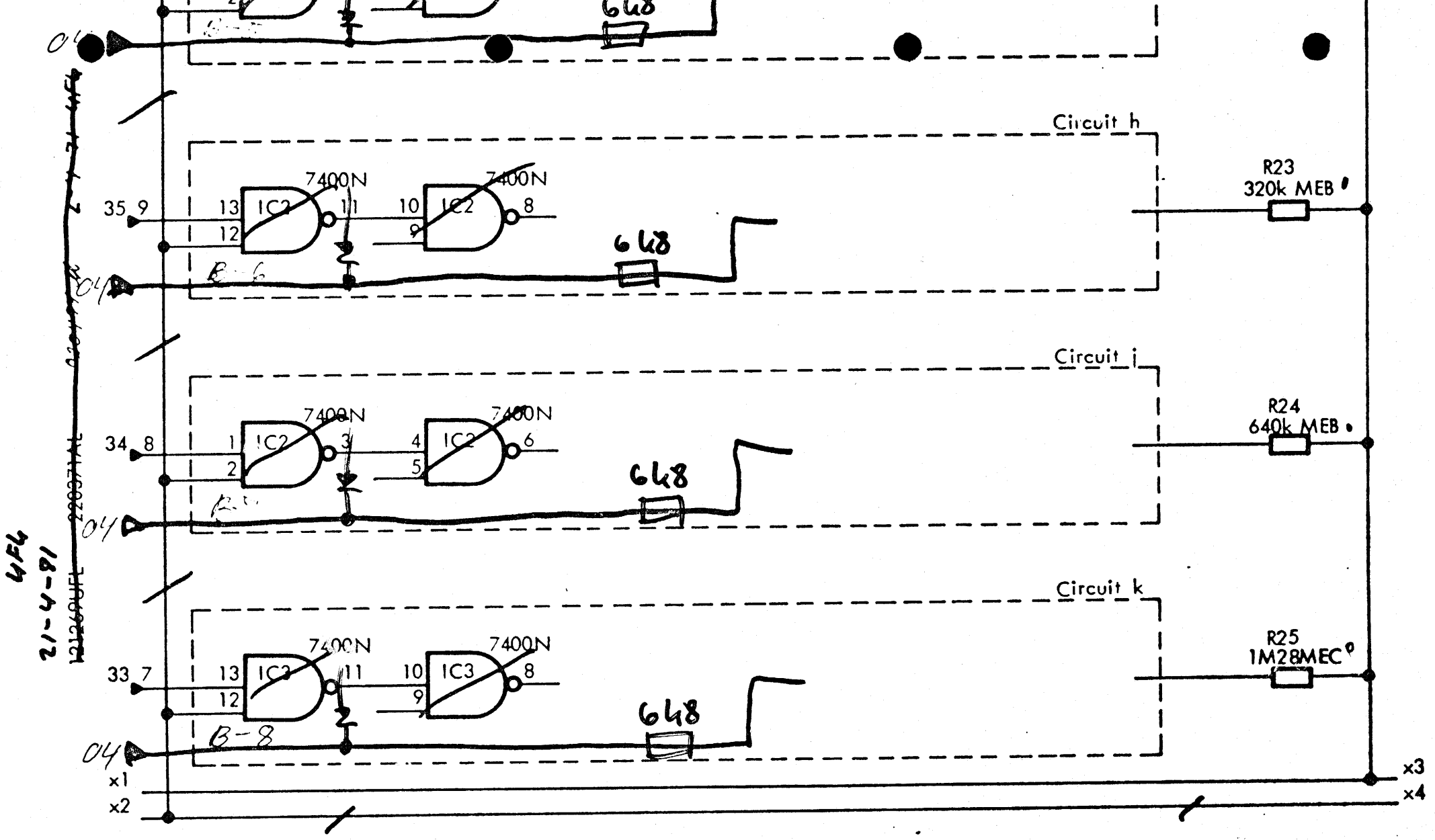
Analog switches – B

AOC 13

V12632

PCBA Circuit Diagram


+17V
0V
-10V
-23,5V
Circuit e
C12V
7400N
IC6
R1e
2k7
648
B-3
Q1e
2N2907
R2e
12k
R3e
33k
D1e
c12
Q2e
2N
4857
D2e
OA95
Q3e
2N
3819
Q4e
2N
3819
4857
D3e
OA95
R4e
15k
R5e
6k8
R6e
150k
R18
40k MEB
R19
100
Circuit f
7400N
IC5
B-7
R20
80k MEB
R21
200
Circuit g
7400N
IC1
R22
160k MEB



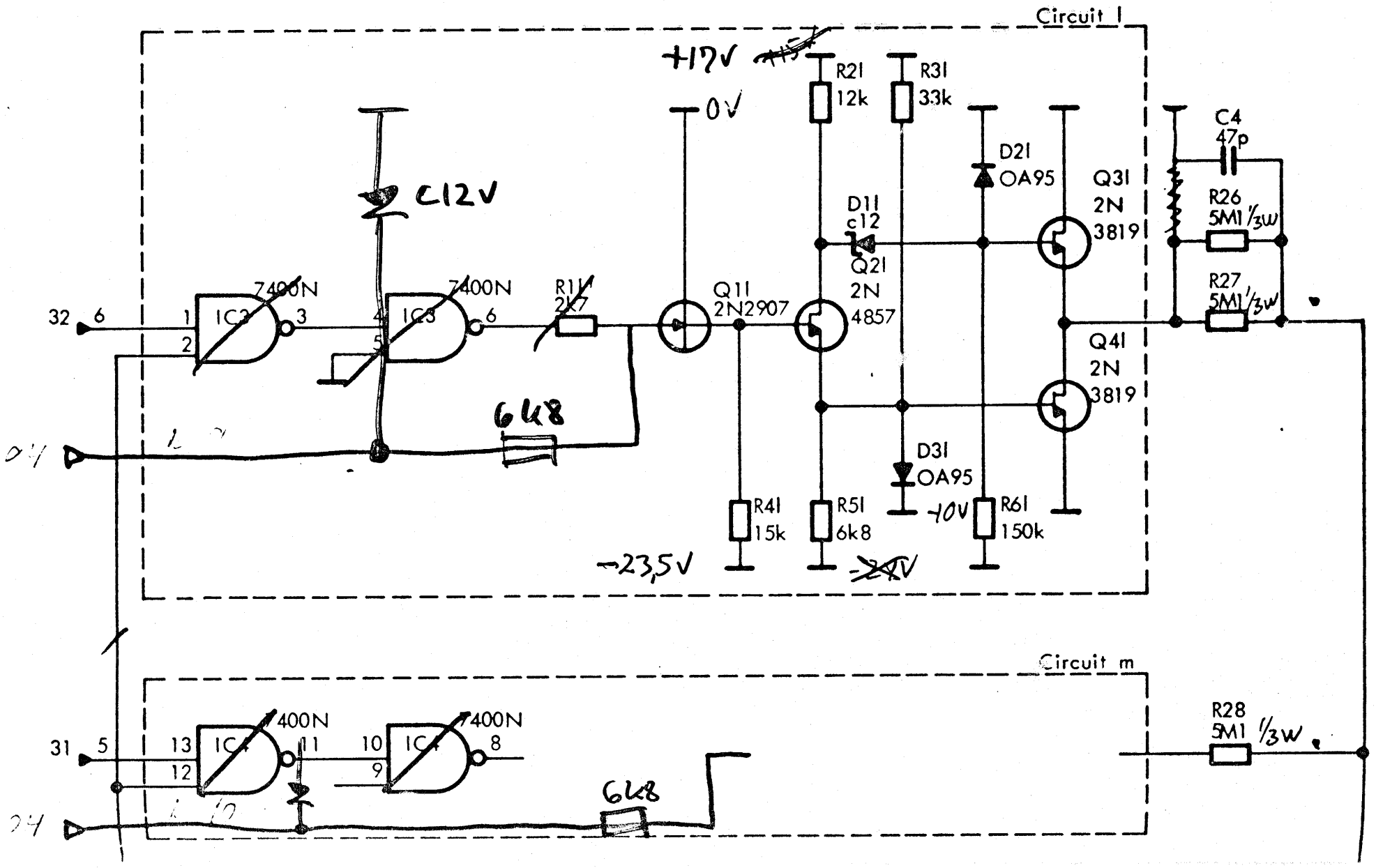
AOC401
~~RCLM400~~

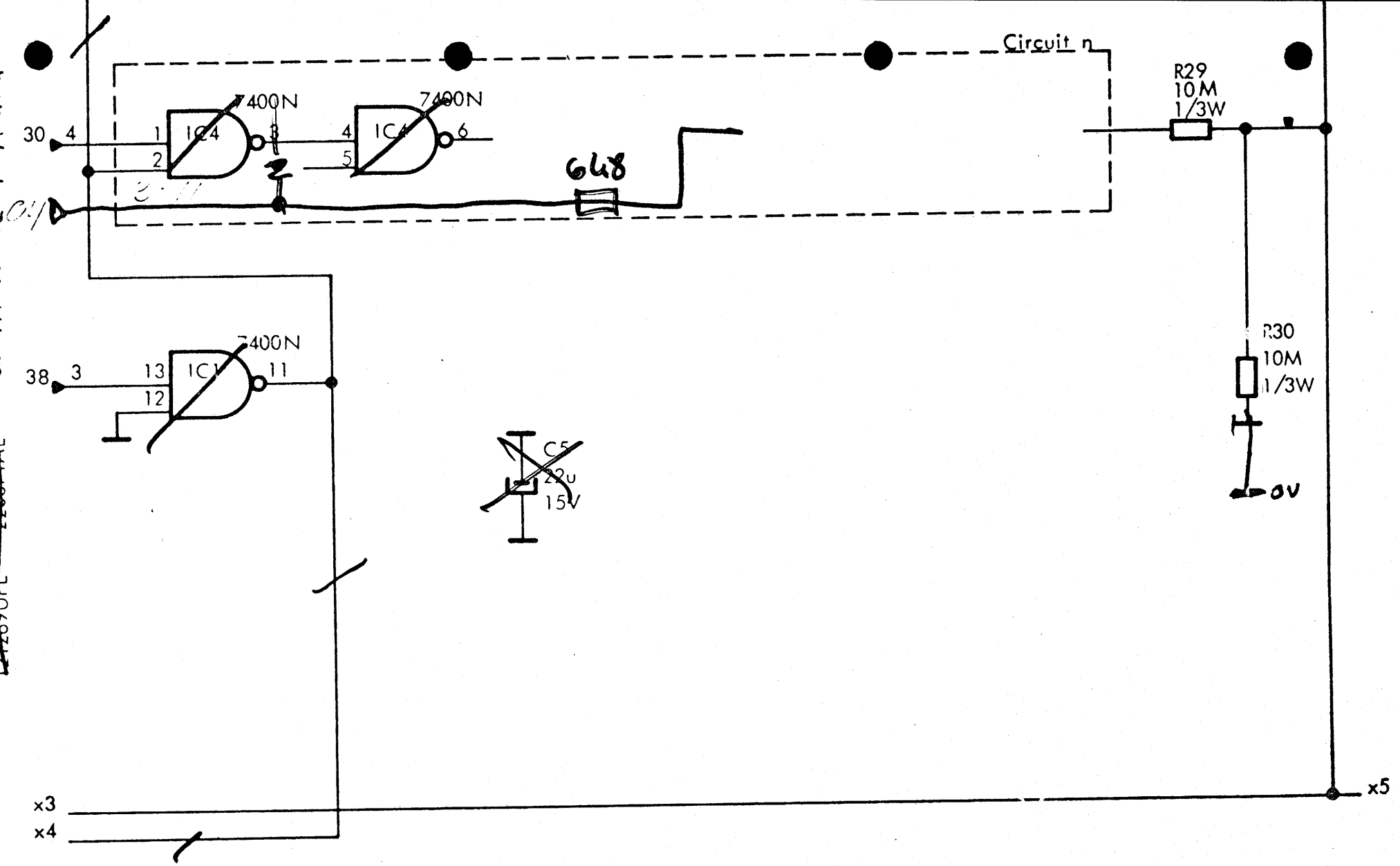
~~V12633~~

Analog switches. – 13
~~LED401~~

PCBA Circuit Diagram

AOC14 ~~RC0937-1~~ ~~RC0938-1~~ ~~RC0939-1~~ ~~p.2 of 5~~


Circuit l
+17V
0V
C12V
R21
12k
R31
33k
D21
OA95
Q31
2N
3819
C4
47p
R26
5M1 1/3W
D11
c12
Q21
2N
4857
R27
5M1 1/3W
32
6
1
2
IC3
7400N
3
4
5
IC3
7400N
6
R11
2K7
Q11
2N2907
Q41
2N
3819
6k8
D31
OA95
+10V
R41
15k
R51
6k8
R61
150k
-23,5V
Circuit m
31
5
13
12
IC4
400N
11
10
9
IC4
400N
8
R28
5M1 1/3W
6k8



AOC 401

~~RCLM400~~

~~V12634~~

Analog switches – B

~~AFD401~~

PCBA Circuit Diagram

AOC 15

~~RC0937-1~~

~~RC0938-1~~

~~RC0939-1~~

~~pp 3 of 5~~

UFL.
21-4-71

~~121269UFL 220371AL 020471AL 2-4-71 UFL~~

AOC 401

x5

+17V

R31 2k
R32 2k
R33 2k
D7 1N914
Q9 2N4402
Q23 2N4402
C8 2n2
D8 OA95
D9 OA95
Q10 2N2453
C6 100p
R43 390
R44 390
C7 100p
R41 1k5
R42 12k
R45 100
Q11 2N 4400
R46 220k
R47 1k
R48 27k
R5[illegible] 2k

Output amplifier. - B

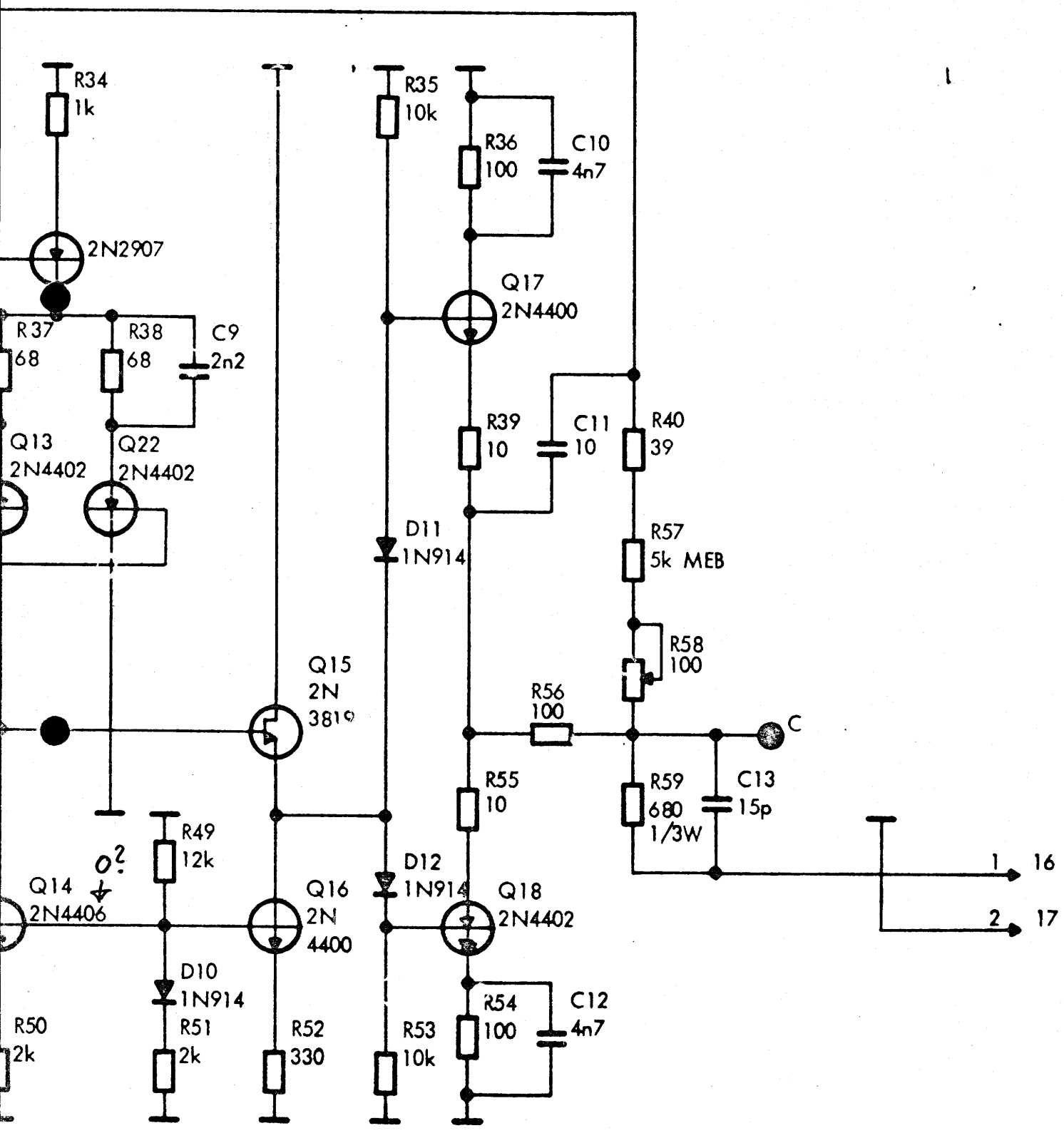
0V

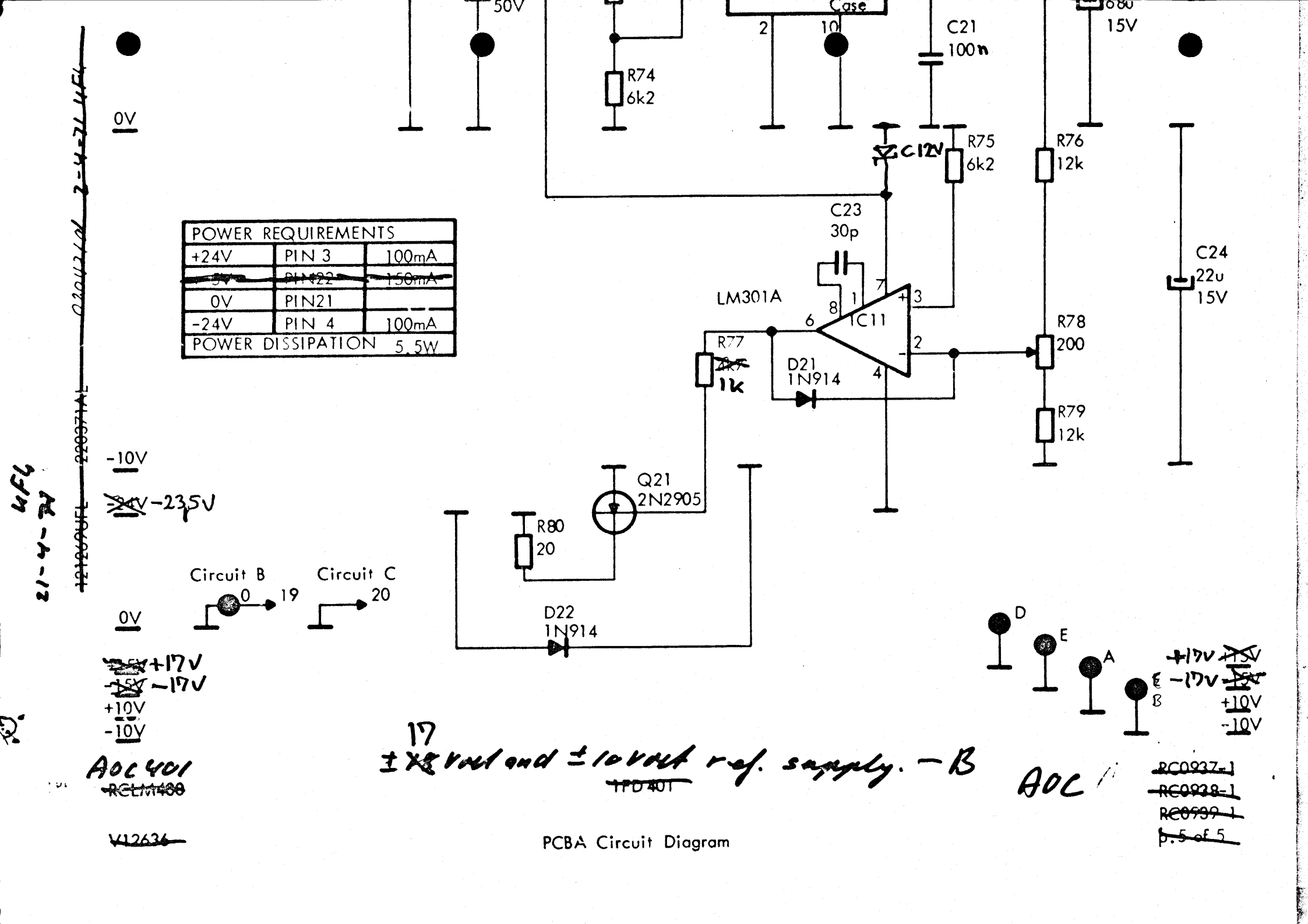
AOC

-17V

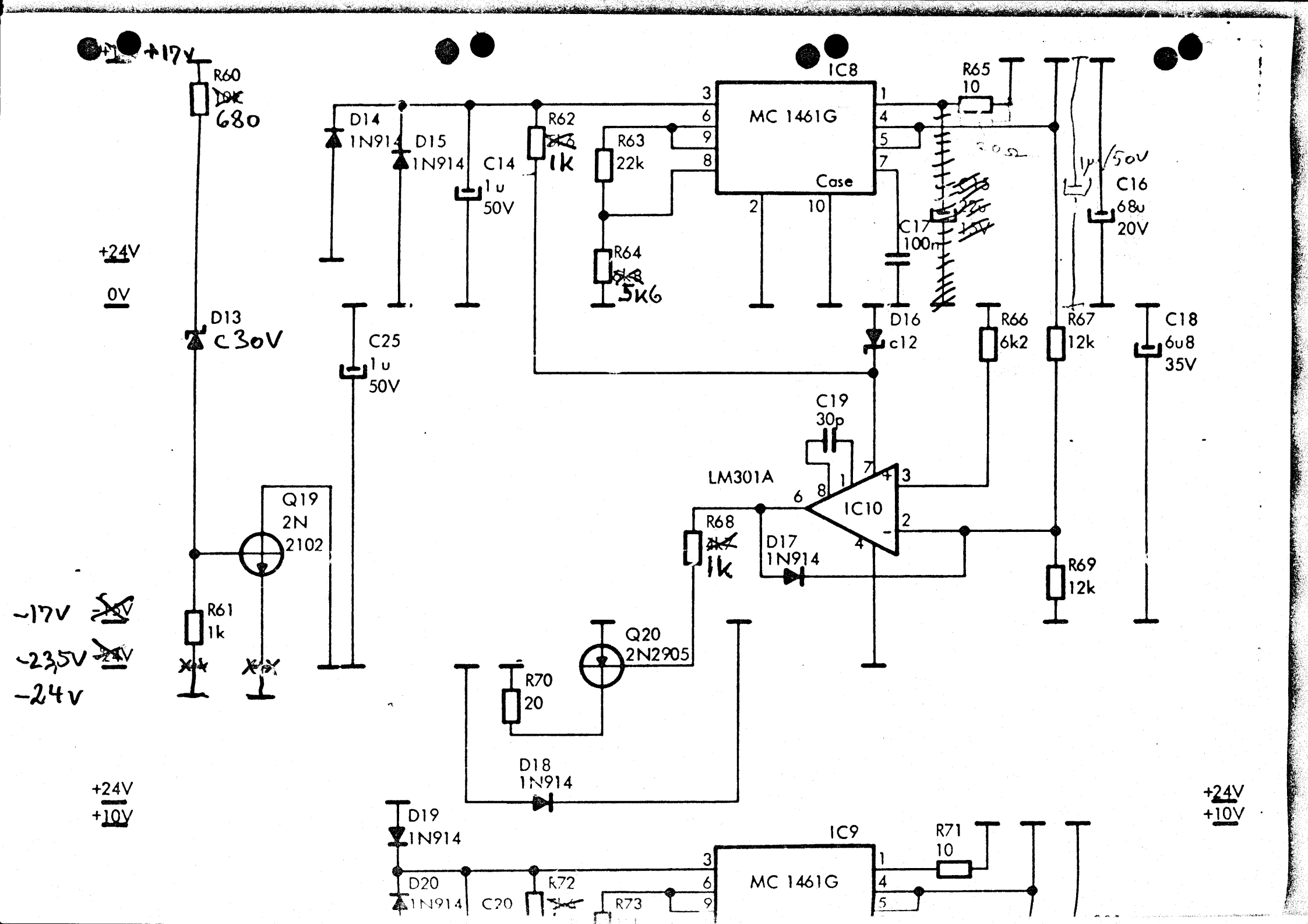
PCBA Circuit Diagram

~~RC0027-1~~
~~RC0028-1~~
~~RC0033-1~~
~~p.c.b.5~~


R34
1k
2N2907
R37
68
R38
68
C9
2n2
Q13
2N4402
Q22
2N4402
R35
10k
R36
100
C10
4n7
Q17
2N4400
R39
10
C11
10
R40
39
D11
1N914
R57
5k MEB
R58
100
Q15
2N
3819
R56
100
C
R55
10
R59
680
1/3W
C13
15p
1
16
2
17
R49
12k
Q14
2N4406
Q16
2N
4400
D12
1N914
Q18
2N4402
D10
1N914
R50
2k
R51
2k
R52
330
R53
10k
R54
100
C12
4n7



PCBA Circuit Diagram


+17V
R60
680
D14
1N914
D15
1N914
C14
1u
50V
R62
1k
R63
22k
R64
5k6
IC8
MC 1461G
Case
R65
10
C16
68u
20V
C17
100n
D16
c12
R66
6k2
R67
12k
C18
6u8
35V
+24V
0V
D13
c30V
C25
1u
50V
C19
30p
LM301A
IC10
R68
1k
D17
1N914
R69
12k
Q19
2N
2102
R61
1k
-17V
-23,5V
-24V
Q20
2N2905
R70
20
D18
1N914
+24V
+10V
D19
1N914
D20
1N914
C20
R72
R73
IC9
MC 1461G
R71
10
+24V
+10V

A/S REGNECENTRALEN

SCANDINAVIAN INFORMATION PROCESSING SYSTEMS

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TELEPHONE: (01) 105366 . TELEX: 6282 RCHQ DK . CABLES: REGNECENTRALEN