

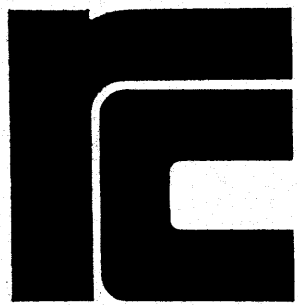
RC LOG LIST

UNIT *001* *425* MODEL NO

This LOG LIST contains information on modifications of the basic unit, due to Options, Engineering Change Notes, and Field Change Orders.

Do not forget to list all future modifications on this page.

OPTION ECN or FCO No.	DATE of Installation	SIGN	SHORT DESCRIPTION
	<i>20-23-10-11</i>	<i>SP</i>	<i>Modify + add. 05 RC 012-05</i>



TECHNICAL MANUAL

RC 4005 LOGIC DIAGRAMS

~~CPU 402, CPU 404, CPU 408~~ CPU 405

(MFC, STC, ITR, LCI, HCI)

Microprogram Controller (MFC)

Dwg. No.

MFC001	PRIMARY CLOCK PULSE GENERATOR	V10238
002	MAR(0) MICRO ADDRESS REGISTER	V10239
003	MAR(1) MICRO ADDRESS REGISTER	V10240
004	MAR(2) MICRO ADDRESS REGISTER	V10241
005	MAR(3) MICRO ADDRESS REGISTER	V10242
006	MAR(4) MICRO ADDRESS REGISTER	V10243
007	MAR(5) MICRO ADDRESS REGISTER	V10244
008	MAR(6) MICRO ADDRESS REGISTER	V10245
009	MAR(7) MICRO ADDRESS REGISTER	V10246
010	MAR(8) MICRO ADDRESS REGISTER	V10247
011	MAR(9) MICRO ADDRESS REGISTER	V10248
012	MC(1:10)	V10249
013	MC(11:20)	V10250
014	MC(21:30)	V10251
015	MC(31:40)	V10252
016	MC(41:50)	V10253
017	MC(51:60)	V10254
018	MC(61:70)	V10255
019	JS(71:80)	V10256
020	JS(81:90)	V10257
021	JS(91:100)	V10258
022	PARITY LOGIC	V10259
023	PARITY LOGIC	V10260
024	PARITY LOGIC	V10261
025	PARITY LOGIC	V10262
026	CLOCK PULSES	V10263
027	MAR Control	V10264
028	MANUAL MODE	V10265
029	NORMAL MODE AND RUNNING MODE	V10266
030	START STOP LOGIC	V10267

Microprogram Controller (MPC)

Dwg. No.

MPC031	MPS PARITY CONTROL	V10268
032	CORE STORE PARITY CONTROL	V10269
033	OPERATOR MODE AND CONDITION RESET	V10270
034	START AND AUTOLOAD CONDITIONS	V10271
035	ARU DISPLAY CONTROL	V10272
036	POWER SUPPLY SUPERVISION	V10481
037	LAMP CONTROL	V10273
038	DISPLAY	V10274
050	+5 VOLT, 0 VOLT, AND CHASSIS CONNECTIONS	V11391

Store Controller (STC)

STC001	PRIORITY SYSTEM	V10567
002	TIME BASE COUNTERS	V10568
003	BUFFER SECTION	V13516 V10569
004	ADDRESS CONTROL	V10570
005	CORE STORE 1 CONTROL SIGNALS	V13517 V11396 V13518
006	READ AND WRITE CONTROL	V10572
007	READ AND WRITE CONTROL	V10573
008	ADDRESS GENERATION	V10574
009	ADDRESS GENERATION	V10575
010	STBUS(0:5)	V13519 V10576 V13520
011	STBUS(6:11)	V10557 V13520
012	STBUS(12:17)	V13578 V13522
013	STBUS(18:23)	V10579 V13523
014	STBUS(24:27)	V10580
015	PARITY CHECK AND GENERATION	V10581
016	ADDRESS TRANSMISSION FROM CPU TO CORE STORE 1	V13511 V10582
017	DATA TRANSMISSION FROM CPU TO CORE STORE 1	V13512 V10583
018	DATA TRANSMISSION FROM CPU TO CORE STORE 1	V13513 V10584

Store Controller (STC)

Dwg. No.

STC019	DATA TRANSMISSION FROM CORE STORE 1 TO CPU	V13514 V10585
020	DATA TRANSMISSION FROM CORE STORE 1 TO CPU	V13515 V10586 V13524 V10894
021	POWER SUPERVISION	V10894
022	TERMINATION OF UNUSED WIRES IN CORE STORE CABLES	V13525 V11397
023	TERMINATION OF UNUSED WIRES IN CORE STORE CABLES	V13526

Interrupt Unit (ITR)

ITR001	IR(0:3), IM(0:3), RM(0:3)	V10642
002	IR(4:7), IM(4:7), FR(4:7)	V10643
003	IR(8:11), IM(8:11), FR(8:11)	V10644
004	IR(12:15), IM(12:15), FR(12:15)	V10645
005	IR(16:19), IM(16:19), FR(16:19)	V10646
006	IR(20:23), IM(20:23), FR(20:23)	V10647
007	ITR REQUEST, GrS1(0:5)	V10648
008	ITRno(18:21), NOInGr(0:3)	V10649
009	ITRno(22)	V10650
010	CONTROL AND TIMING SIGNALS	V10651
011	INTERRUPT(3:11)	V11084
012	INTERRUPT(12:23)	V11085
013	CONNECTIONS BETWEEN INPUT CONNECTOR AND PLUG BOARD	V10654
014	INTERRUPTS FROM BASIC I/O UNITS	V11086

Low-Speed Data Channel Interface (LCI)

Dwg. No.

LCI001	SB(0:11)	V10601
002	SB(12:23)	V10602
003	LDC CONTROL SIGNALS	V10603
004	I/O CONNECTED AND I/O READY	V10604
008	DATA(0:7)	V10608
009	I/O DATA(8:15)	V10609
010	I/O DATA(16:23)	V10610
011	RPT CONTROL SIGNALS	V10611
012	RPT CONTROL SIGNALS, SB(16:23)	V10612
020	LDC CONTROL SIGNALS - BUS CABLE 1061	V11072
021	I/O BUS(0:5) - BUS CABLE 1061	V11073
022	I/O BUS(6:9) - BUS CABLE 1061	V11074
023	I/O BUS(10:15) - BUS CABLE 1061	V11075
024	I/O BUS(16:17) - BUS CABLE 1061	V11076
025	I/O BUS(18:23) - BUS CABLE 1061	V11077
026	LDC CONTROL SIGNALS - BUS CABLE 1062	V11078
027	I/O BUS(0:5) - BUS CABLE 1062	V11079
028	I/O BUS(6:9) - BUS CABLE 1062	V11080
029	I/O BUS(10:15) - BUS CABLE 1062	V11081
030	I/O BUS(16:17) - BUS CABLE 1062	V11082
031	I/O BUS(18:23) - BUS CABLE 1062	V11083

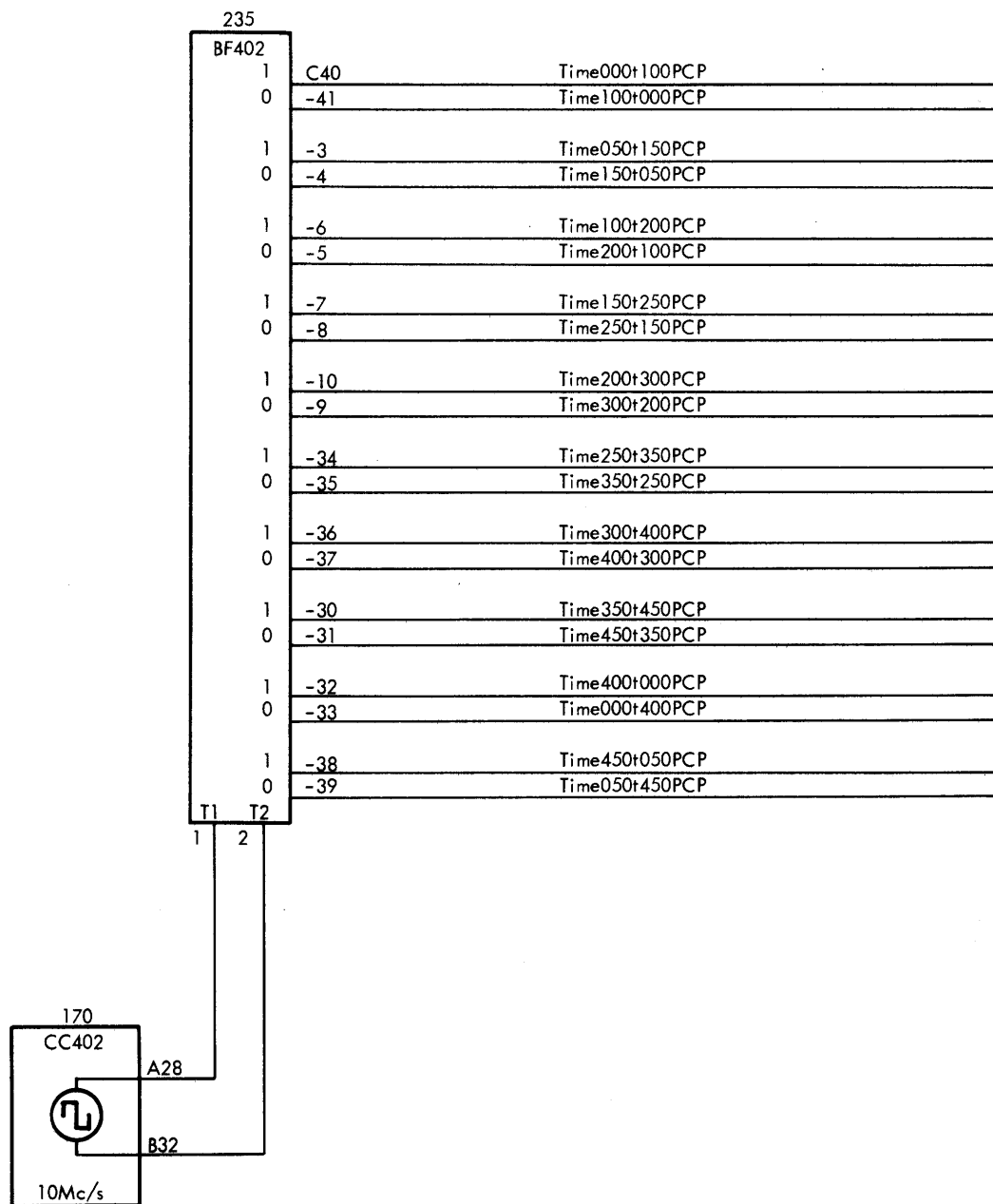
High-Speed Data Channel Interface (HCI)

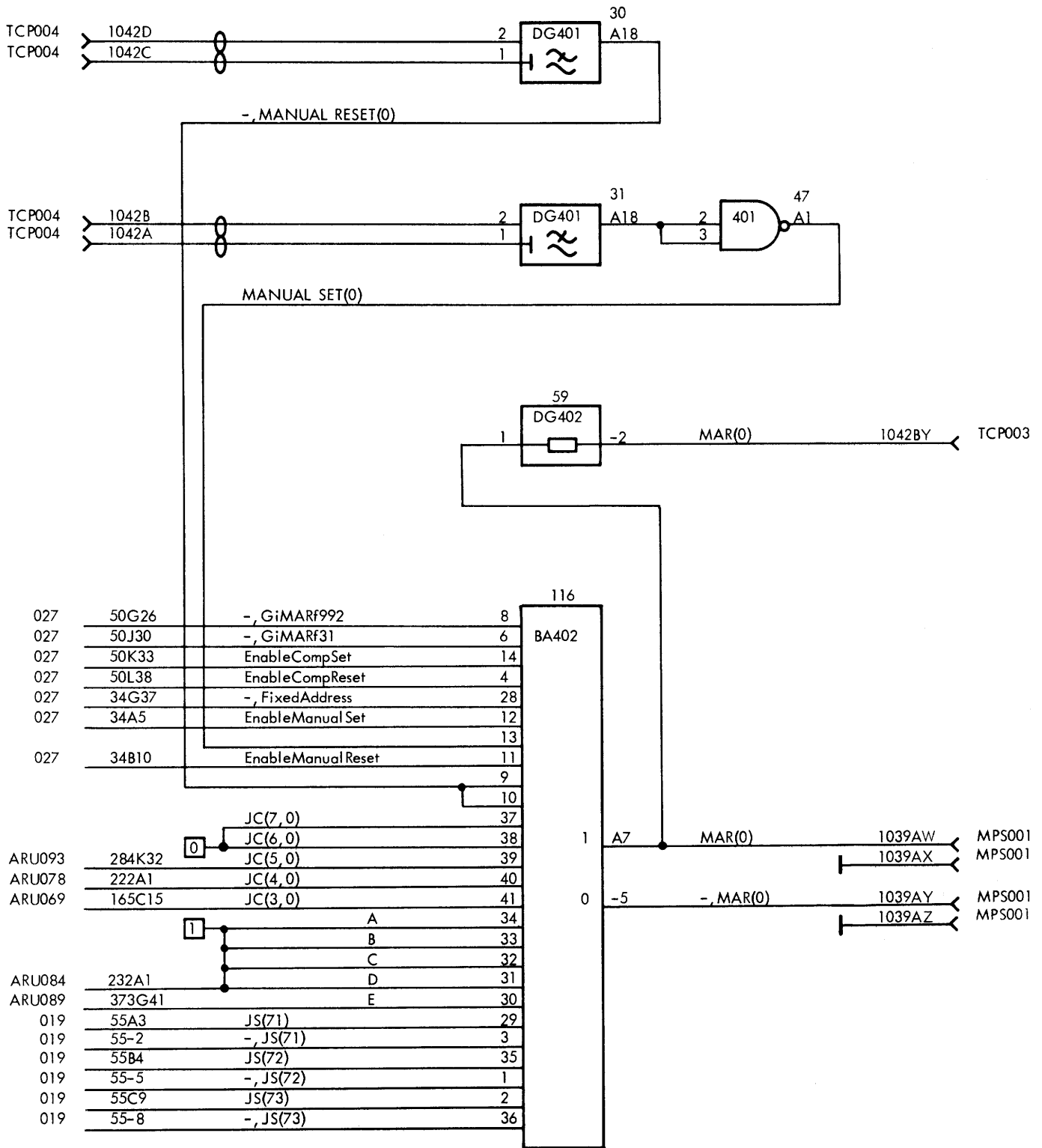
HCI001	CYS Request(0:7)	V10895
002	CYS Request(8:15)	V10896
003	RQ REGISTER	V10897
004	PRIORITY DECODING	V10898
005	PRIORITY DECODING	V10899
006	SelReqBf(0:15)	V10900
007	HDC GIAddr(0:11)	V10901
008	HDC GIData(0:11)	V10902
009	HDC GIAddr(12:15), HDC GIData(12:15)	V10903
010	HDC BUSout(0:9)	V10904

High-Speed Data Channel Interface (HCI)

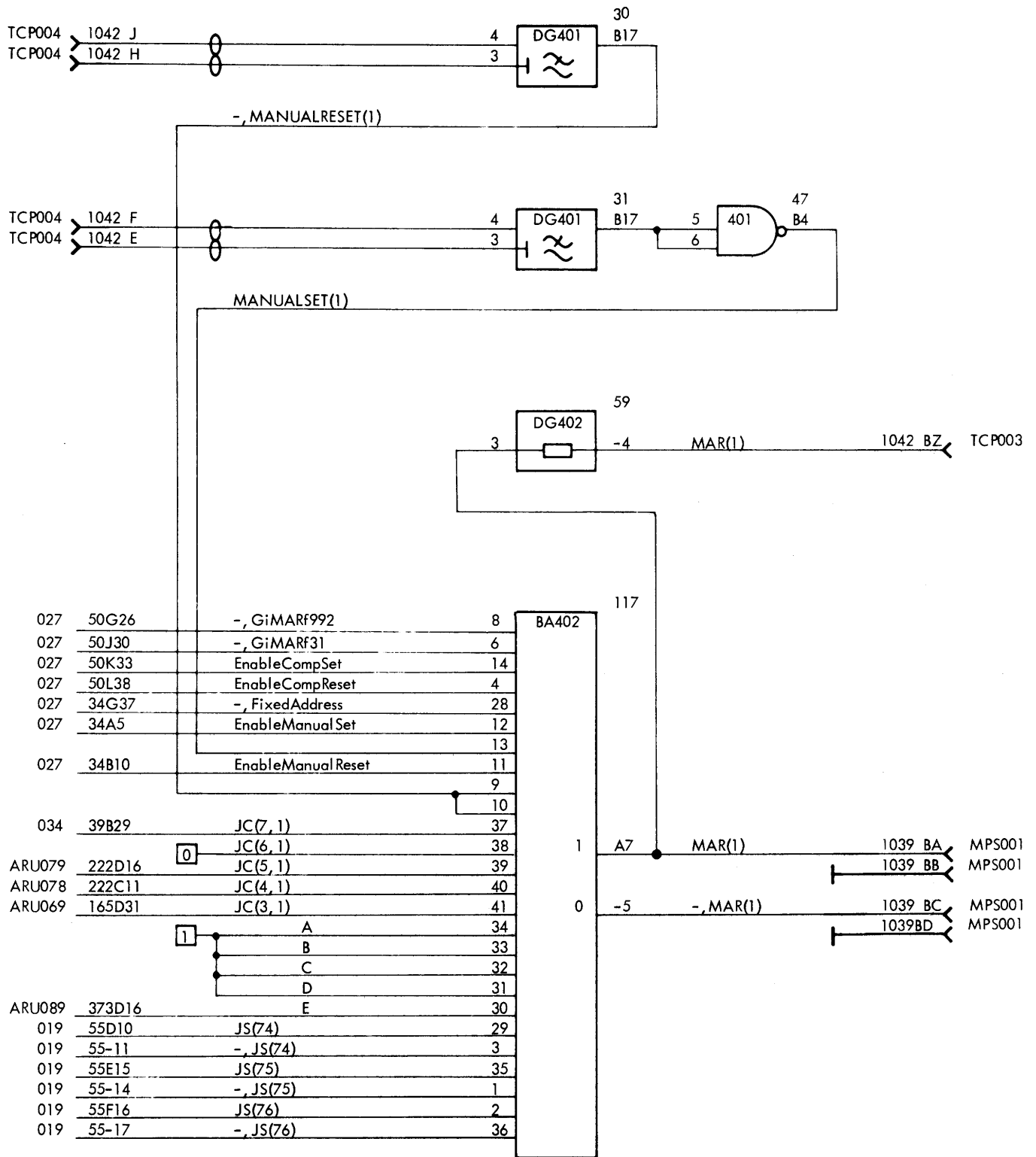
Dwg. No.

HCI011	HDC BUSout(10:23)	V10905
012	HDC BUSin(0:11)	V10906
013	HDC BUSin(12:23)	V10907
014	BUFFER REGISTER FOR HDC ADDRESS AND INPUT DATA	V10908
015	BUFFER REGISTER FOR HDC ADDRESS AND INPUT DATA	V10909
016	TERMINATIONS FOR INPUT-OUTPUT CABLES	V10910
017	TERMINATIONS FOR INPUT-OUTPUT CABLES	V10911
018	TERMINATIONS FOR INPUT-OUTPUT CABLES	V10912
019	TERMINATIONS FOR INPUT-OUTPUT CABLES	V10913
020	TERMINATIONS FOR INPUT-OUTPUT CABLES	V10914
021	TERMINATIONS FOR INPUT-OUTPUT CABLES	V10915
022	HCI CONTROL	V10916
023	HCI CONTROL	V10917
024	HCI CONTROL	V10918
025	HCI CONTROL	V10919
026	HCI CONTROL	V10920
027	3<HDCBF<WORD LIMIT	V13527
	32K-CORE-STORE-MODULE	V11153

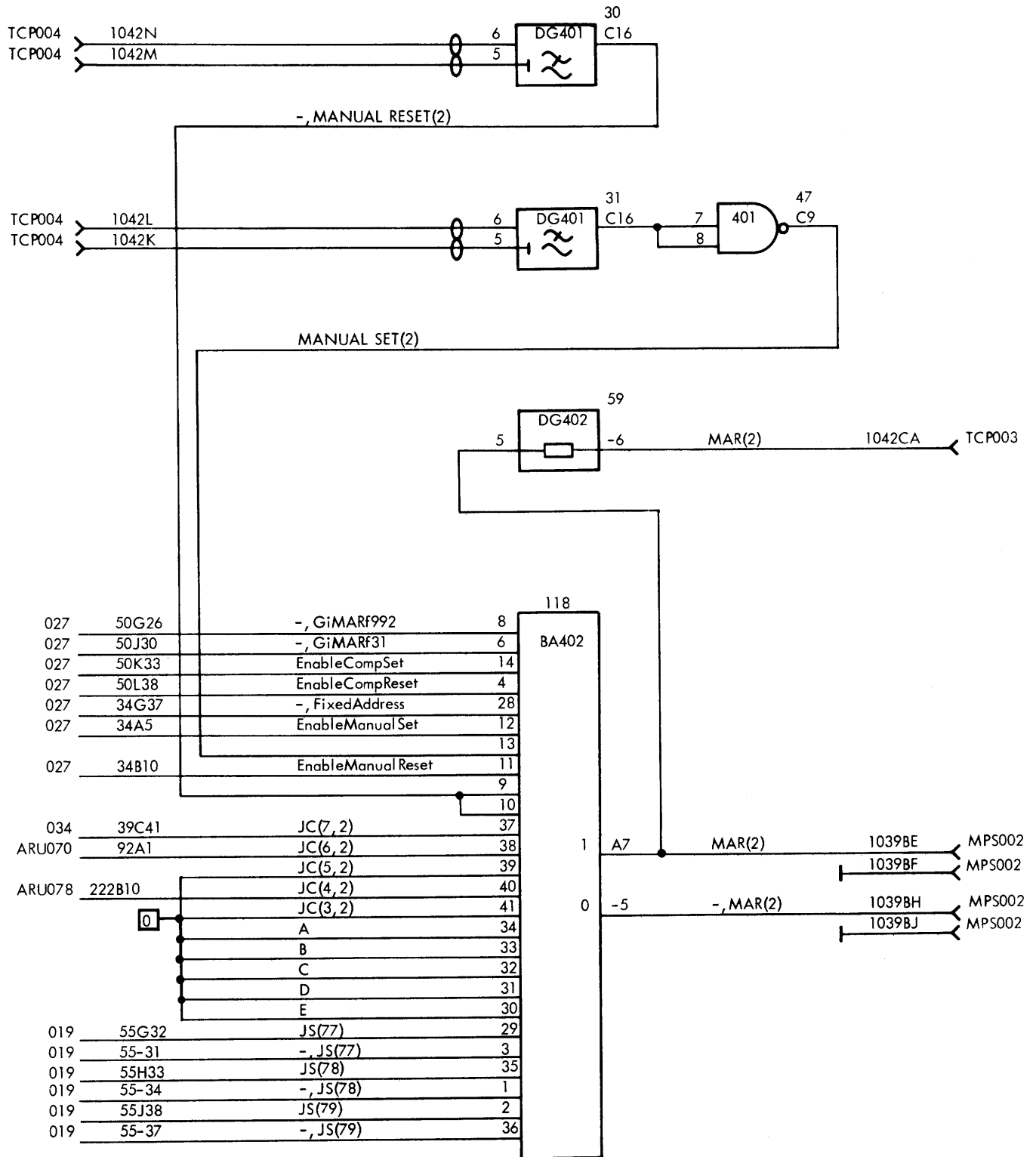




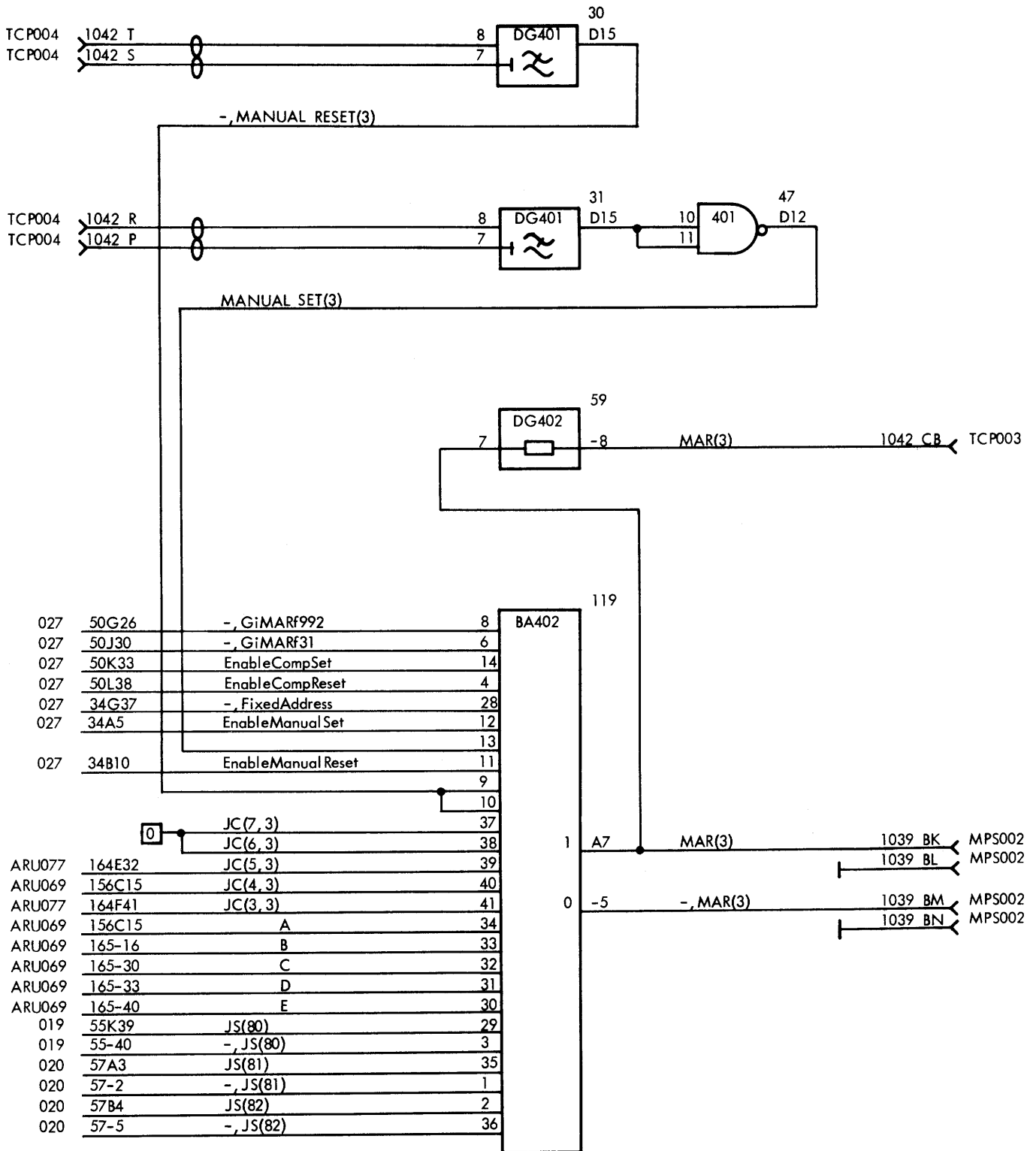
JC(2,0)=A&B&C&D&E



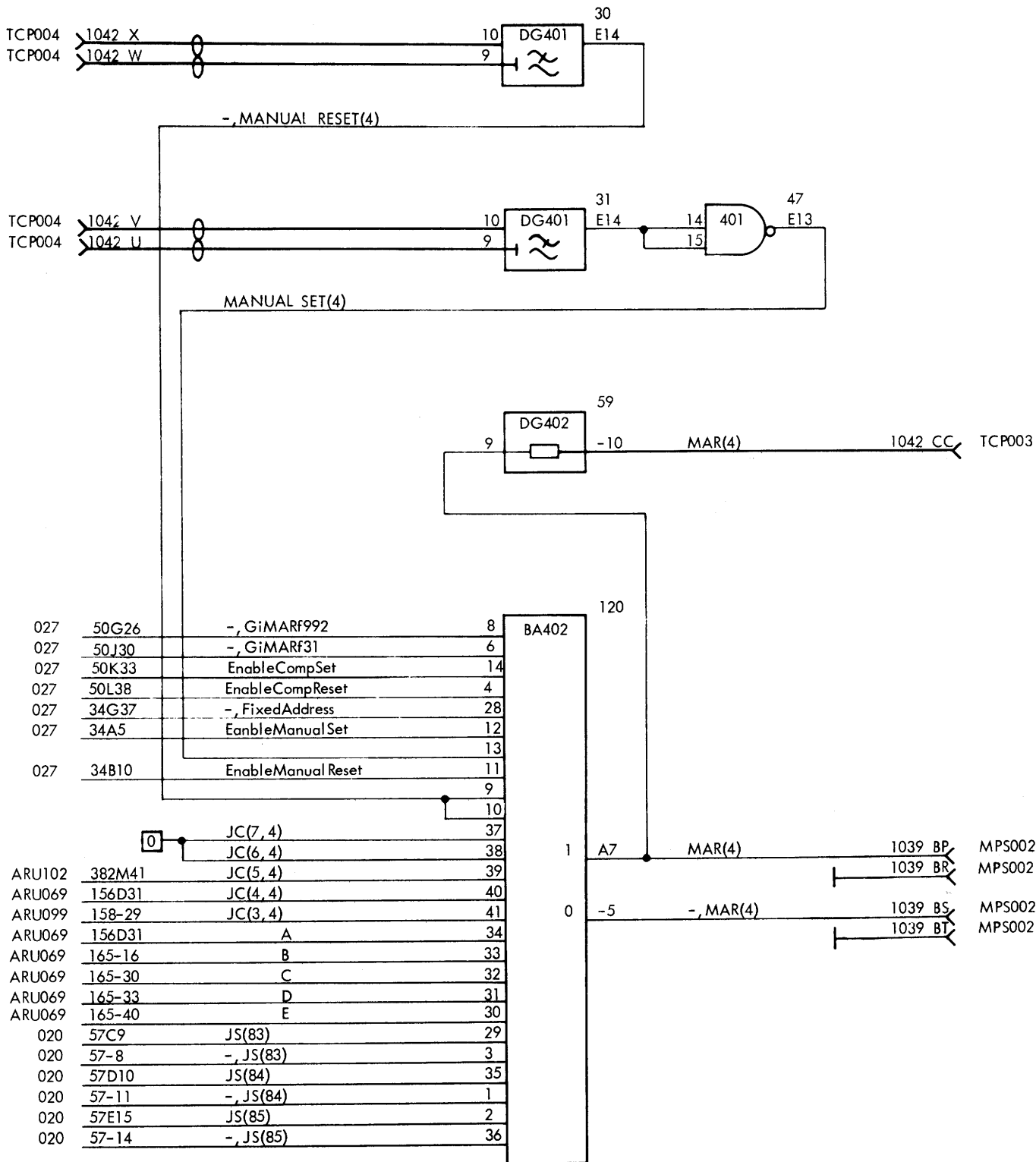
JC(2, 1) = A & B & C & D & E



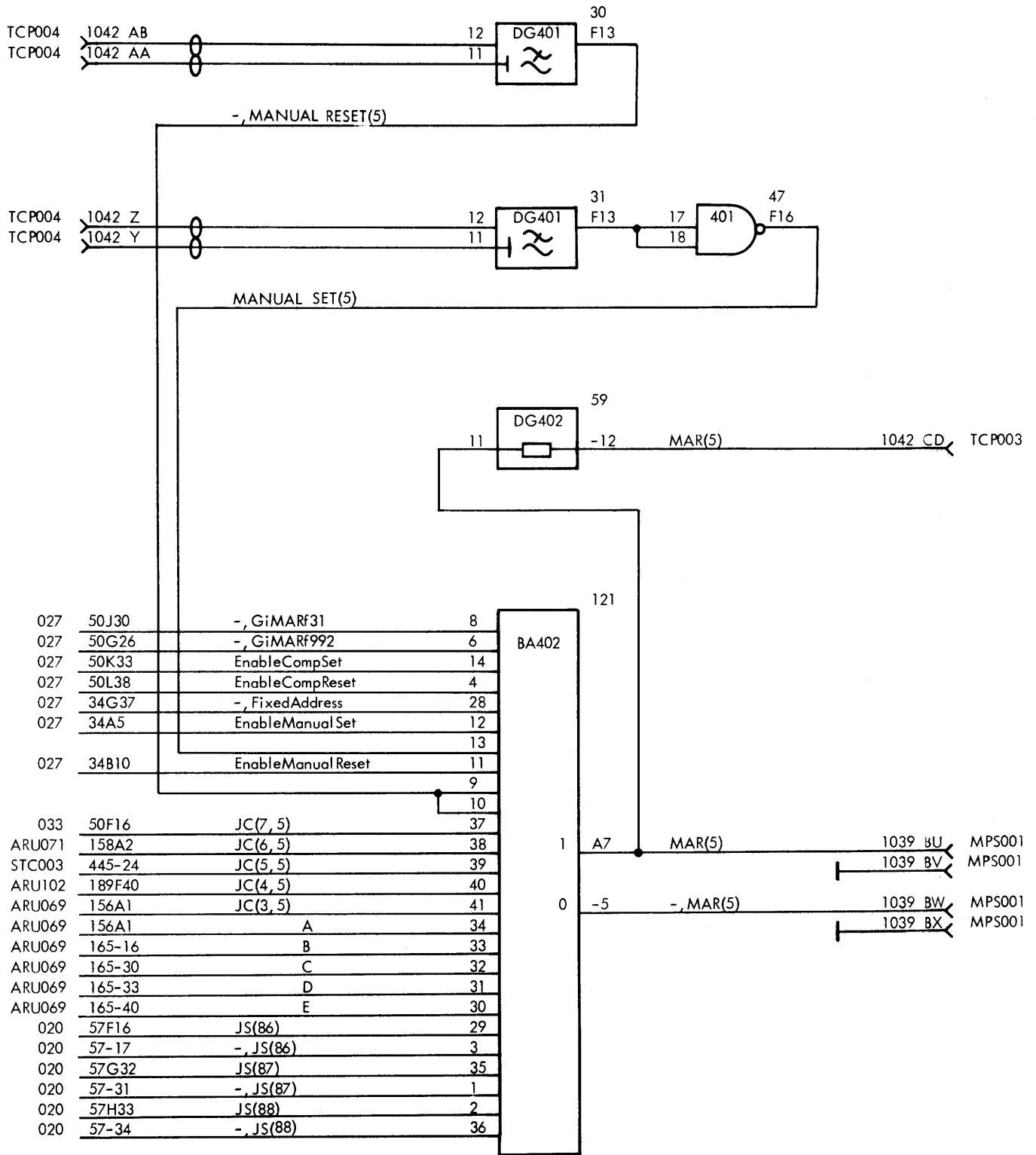
JC(2, 2)=A&B&C&D&E



JC(2, 3)=A&B&C&D&E



JC(2, 4)=A&B&C&D&E

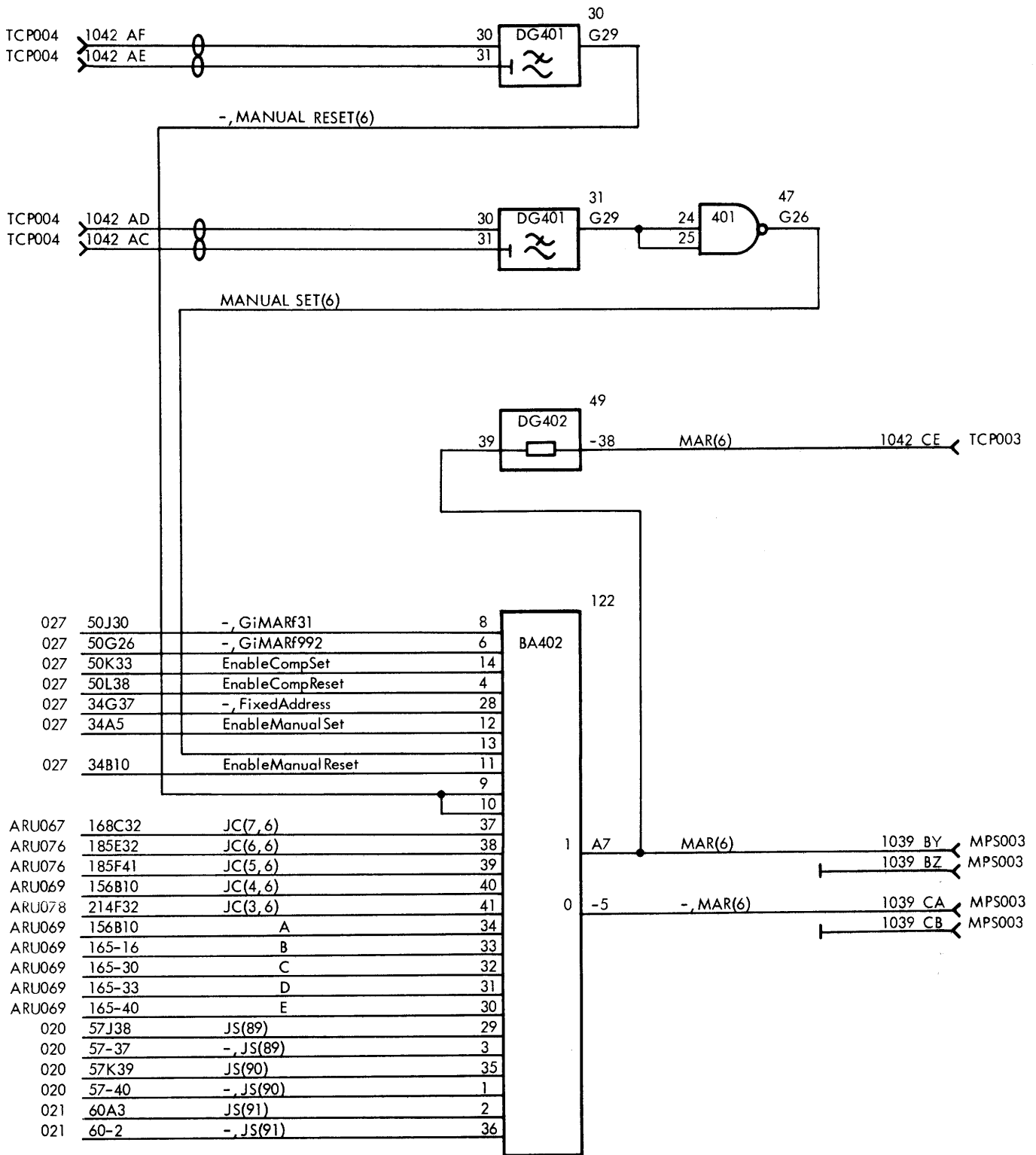


TCP004
TCP004

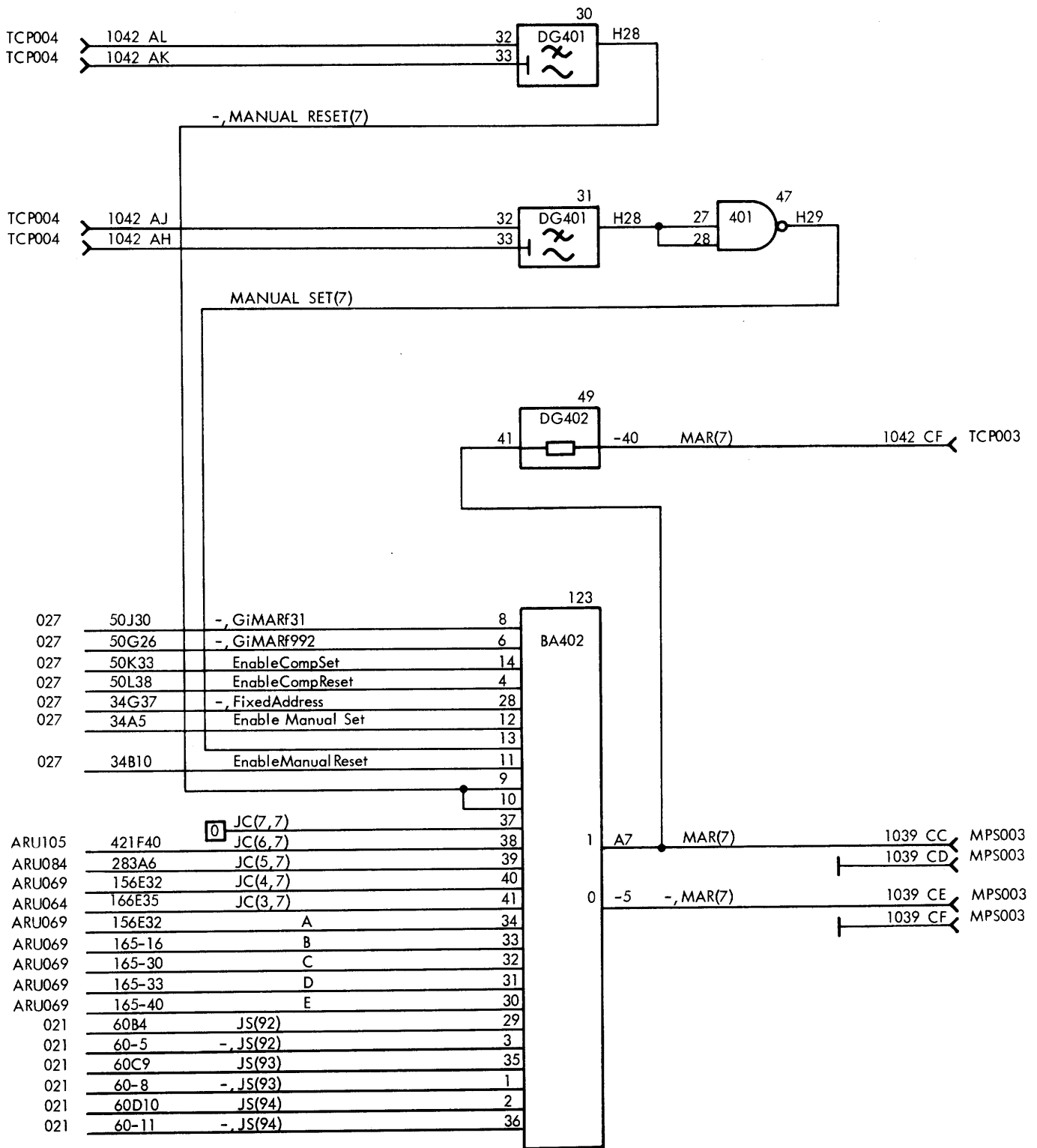
TCP004
TCP004

027	50J30	- , GiMARF31	8
027	50G26	- , GiMARF992	6
027	50K33	EnableCompSet	14
027	50L38	EnableCompReset	4
027	34G37	- , FixedAddress	28
027	34A5	EnableManualSet	12
027	34B10	EnableManualReset	11
033	50F16	JC(7, 5)	37
ARU071	158A2	JC(6, 5)	38
STC003	445-24	JC(5, 5)	39
ARU102	189F40	JC(4, 5)	40
ARU069	156A1	JC(3, 5)	41
ARU069	156A1	A	34
ARU069	165-16	B	33
ARU069	165-30	C	32
ARU069	165-33	D	31
ARU069	165-40	E	30
O20	57F16	JS(86)	29
O20	57-17	- , JS(86)	3
O20	57G32	JS(87)	35
O20	57-31	- , JS(87)	1
O20	57H33	JS(88)	2
O20	57-34	- , JS(88)	36

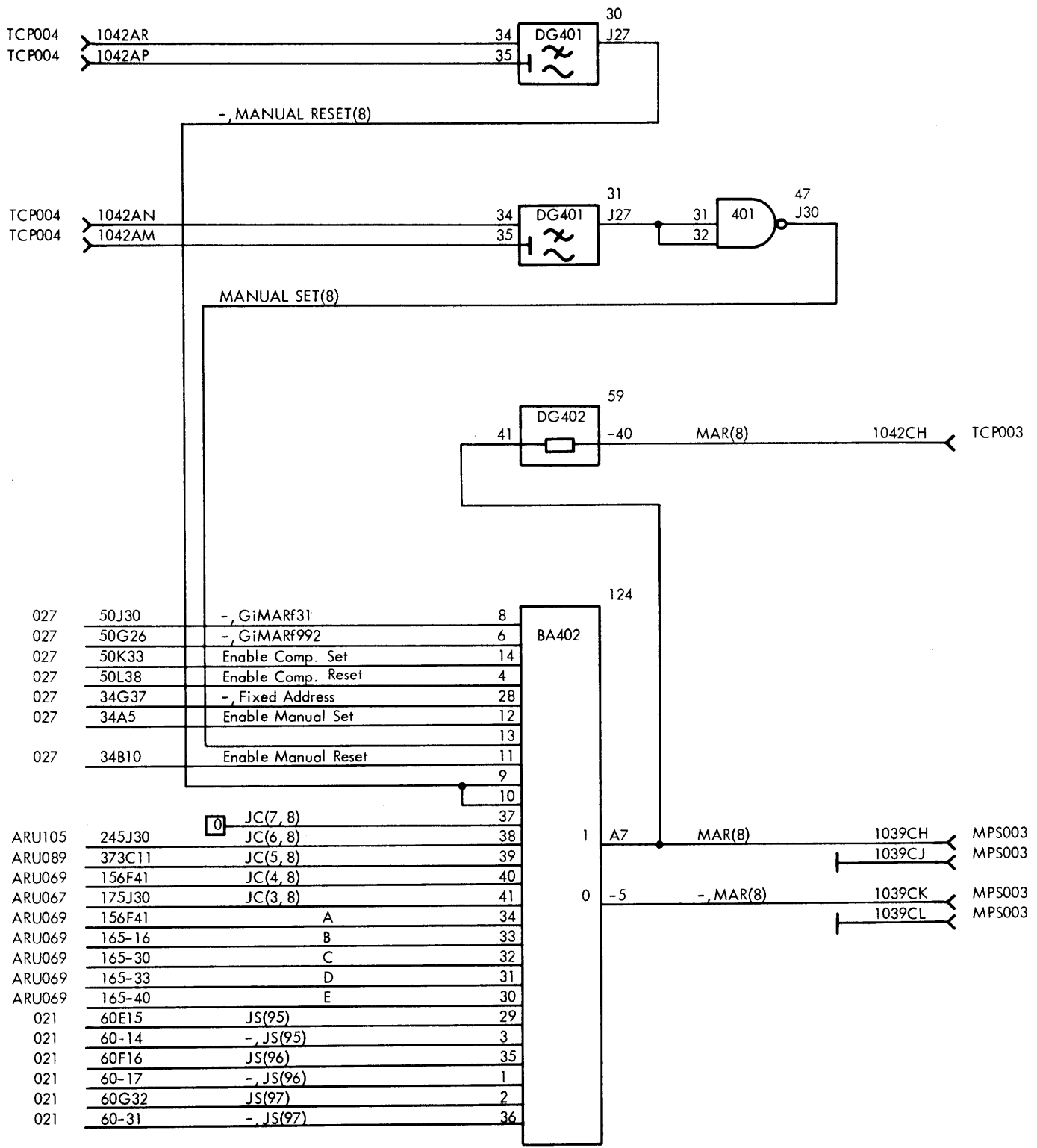
JC(2, 5)=A&B&C&D&E



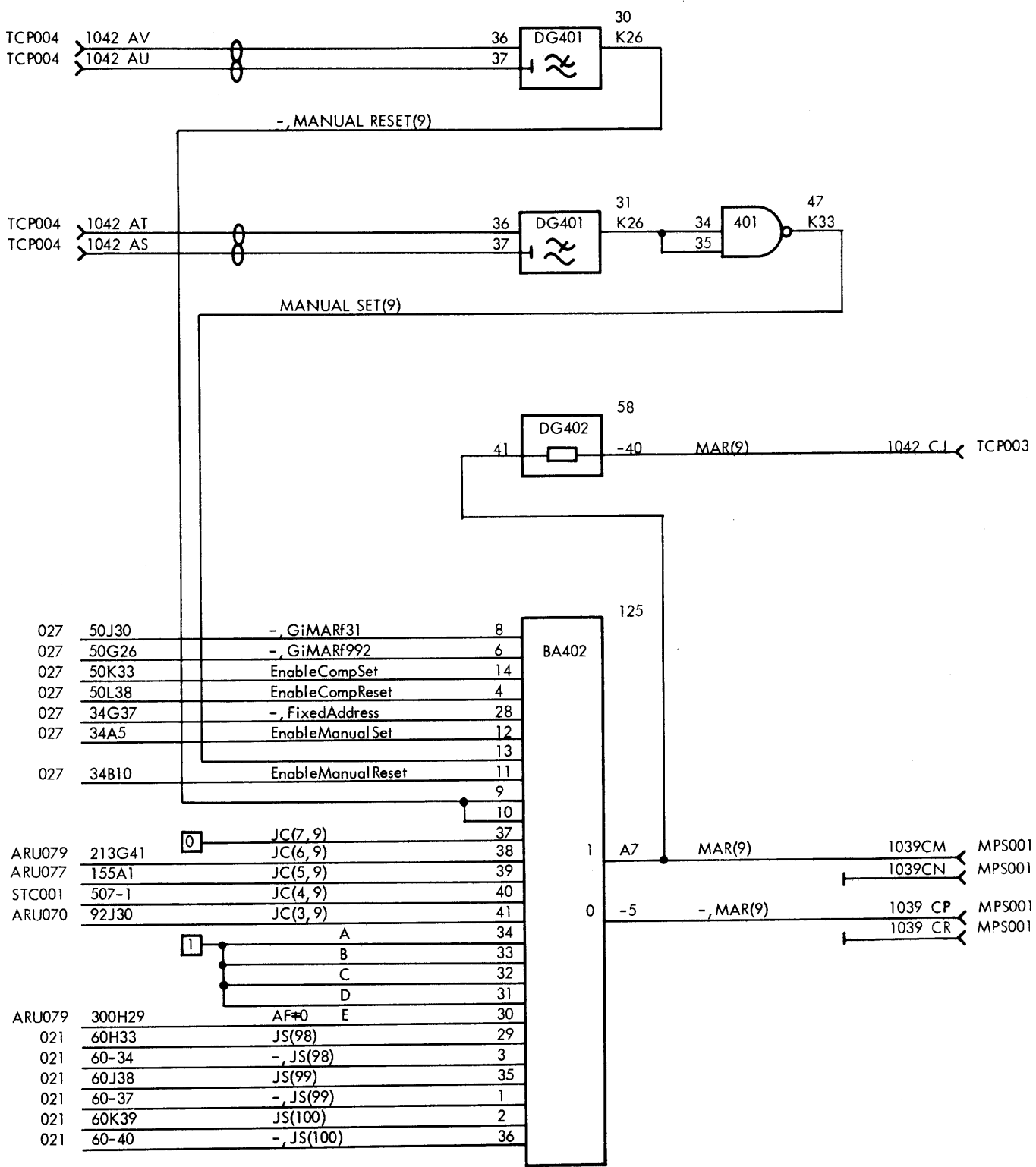
JC(2,6)=A&B&C&D&E



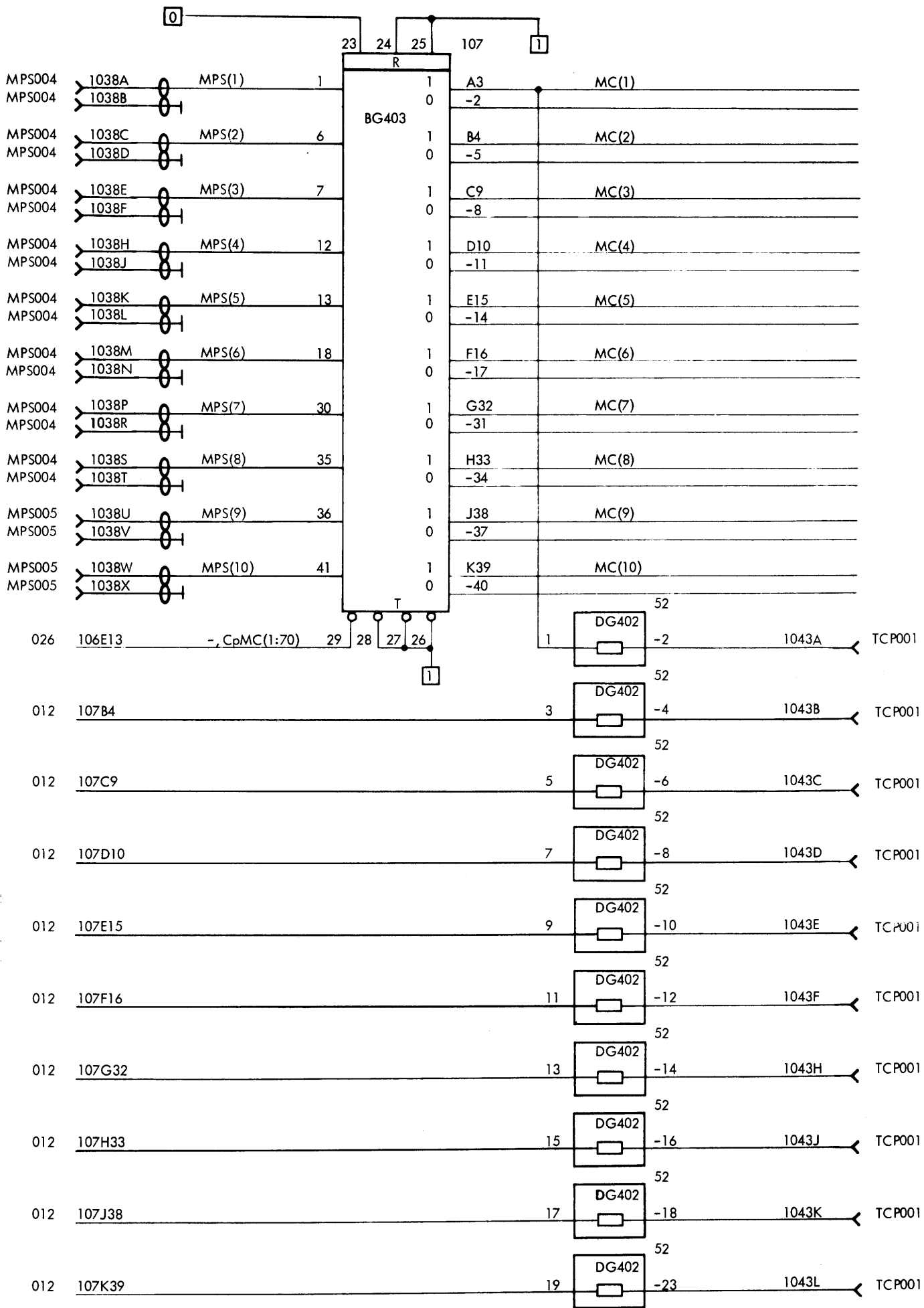
JC(2,7)=A&B&C&D&E

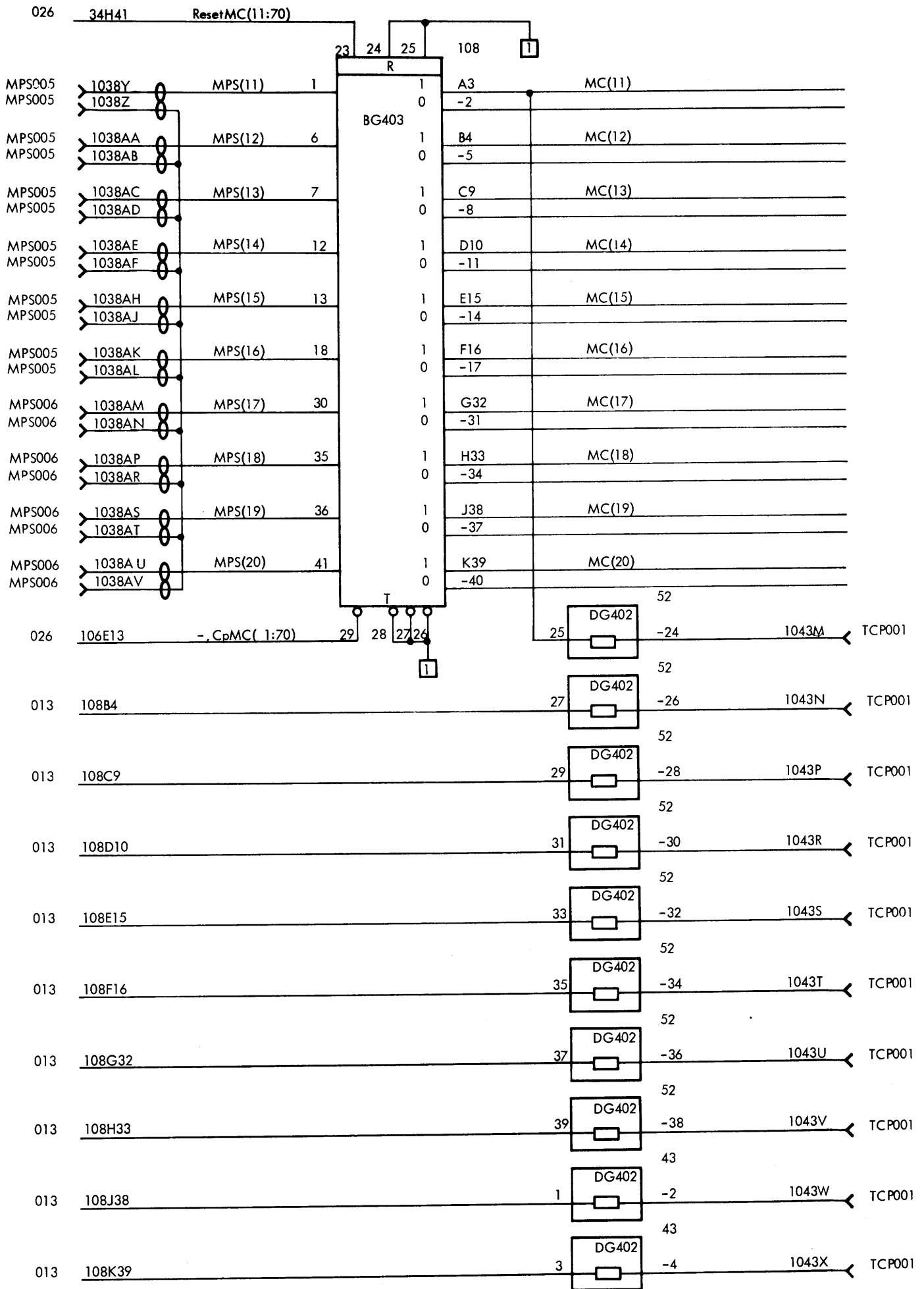


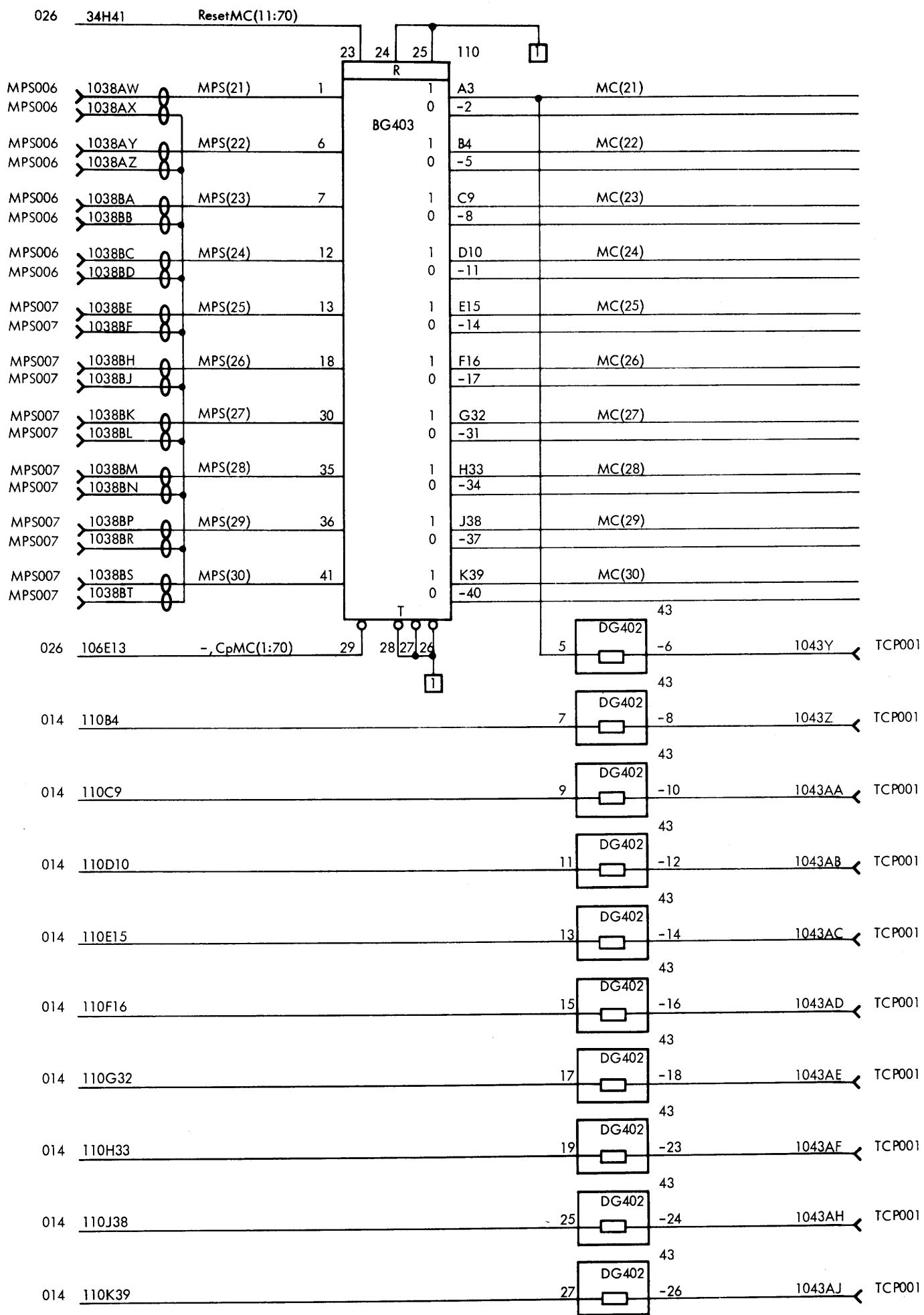
JC(2, 8)=A&B&C&D&E



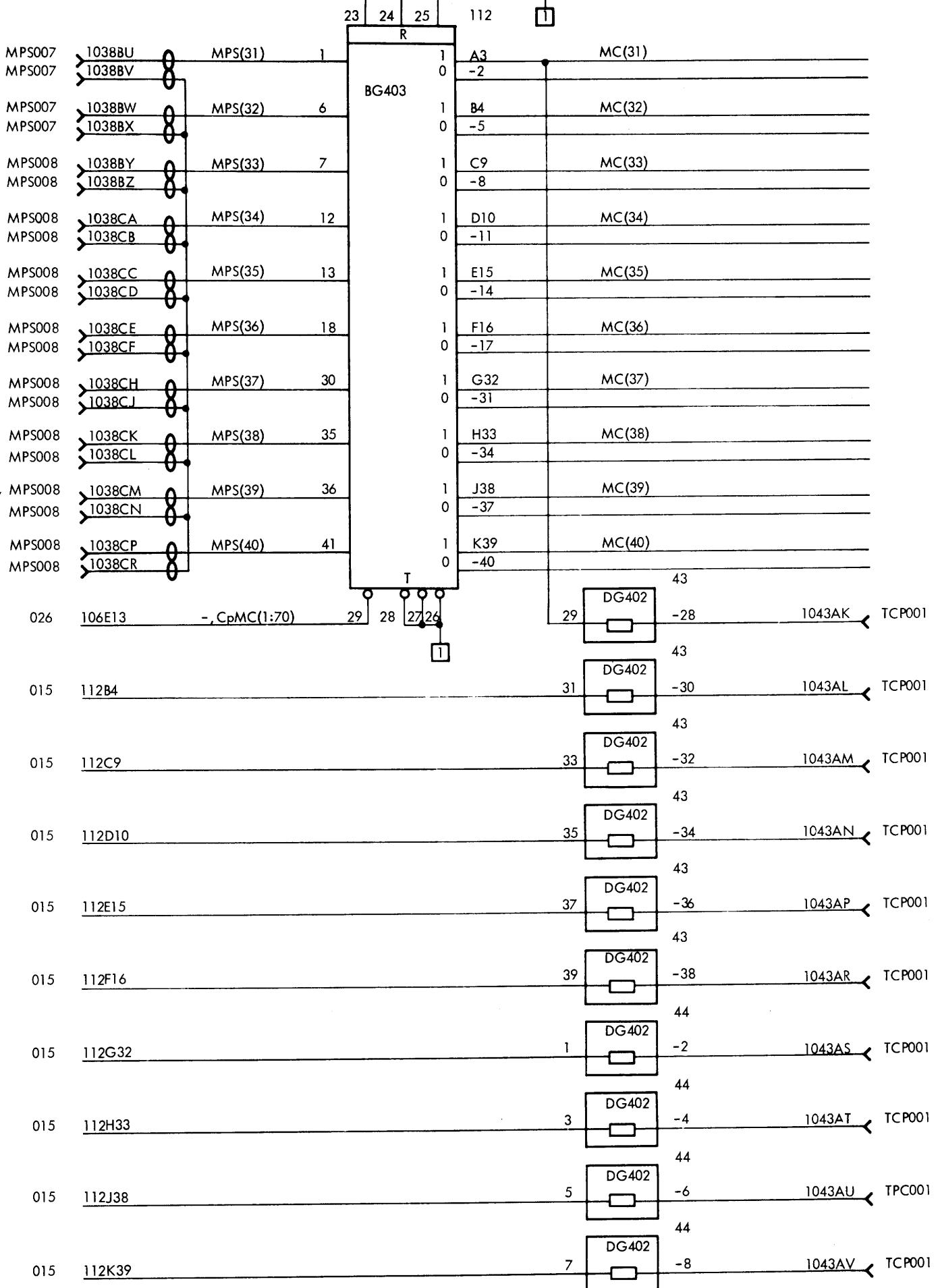
JC(2,9)=A&B&C&D&E







026 34H41 ResetMC(11:70)



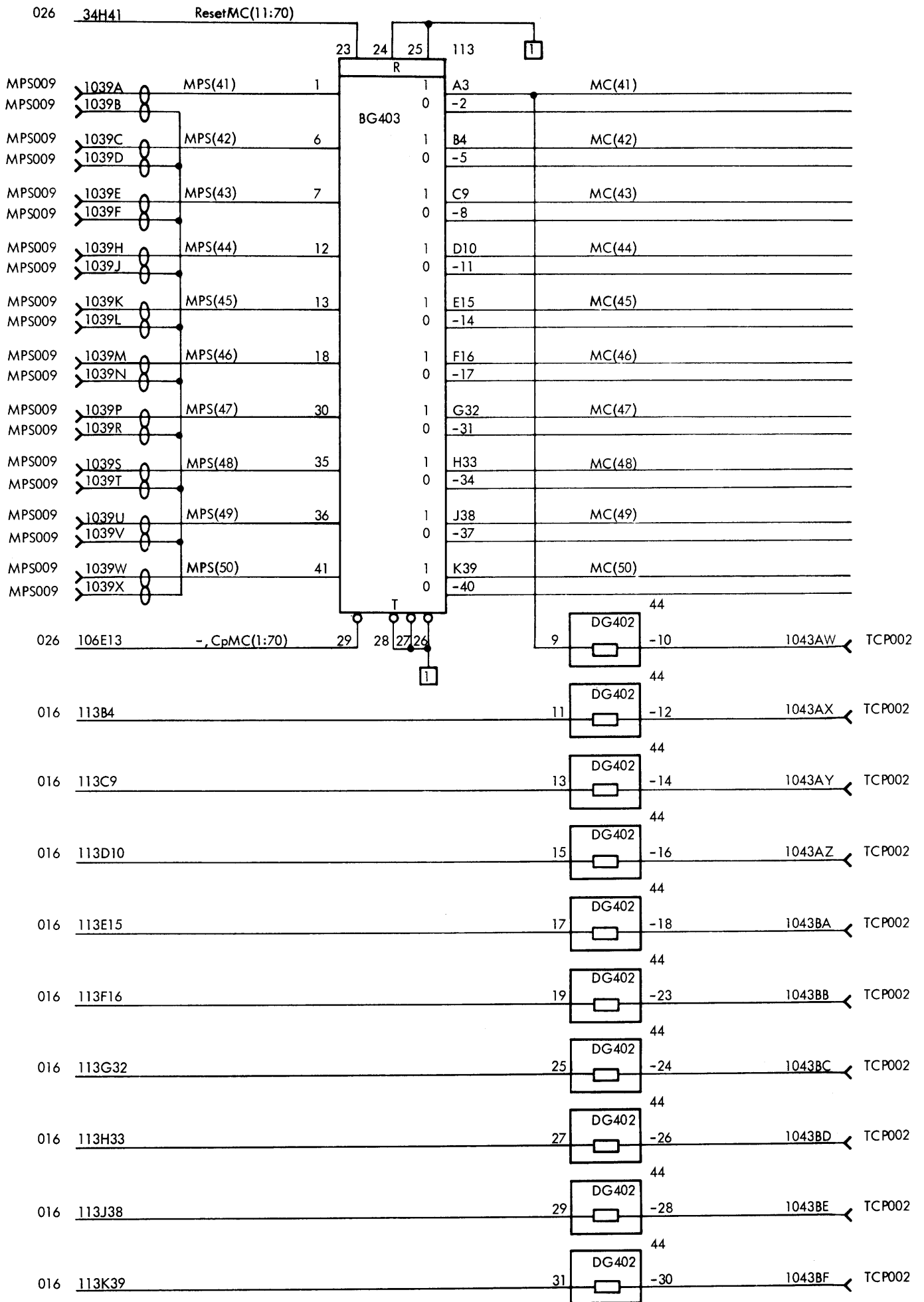
RC4000

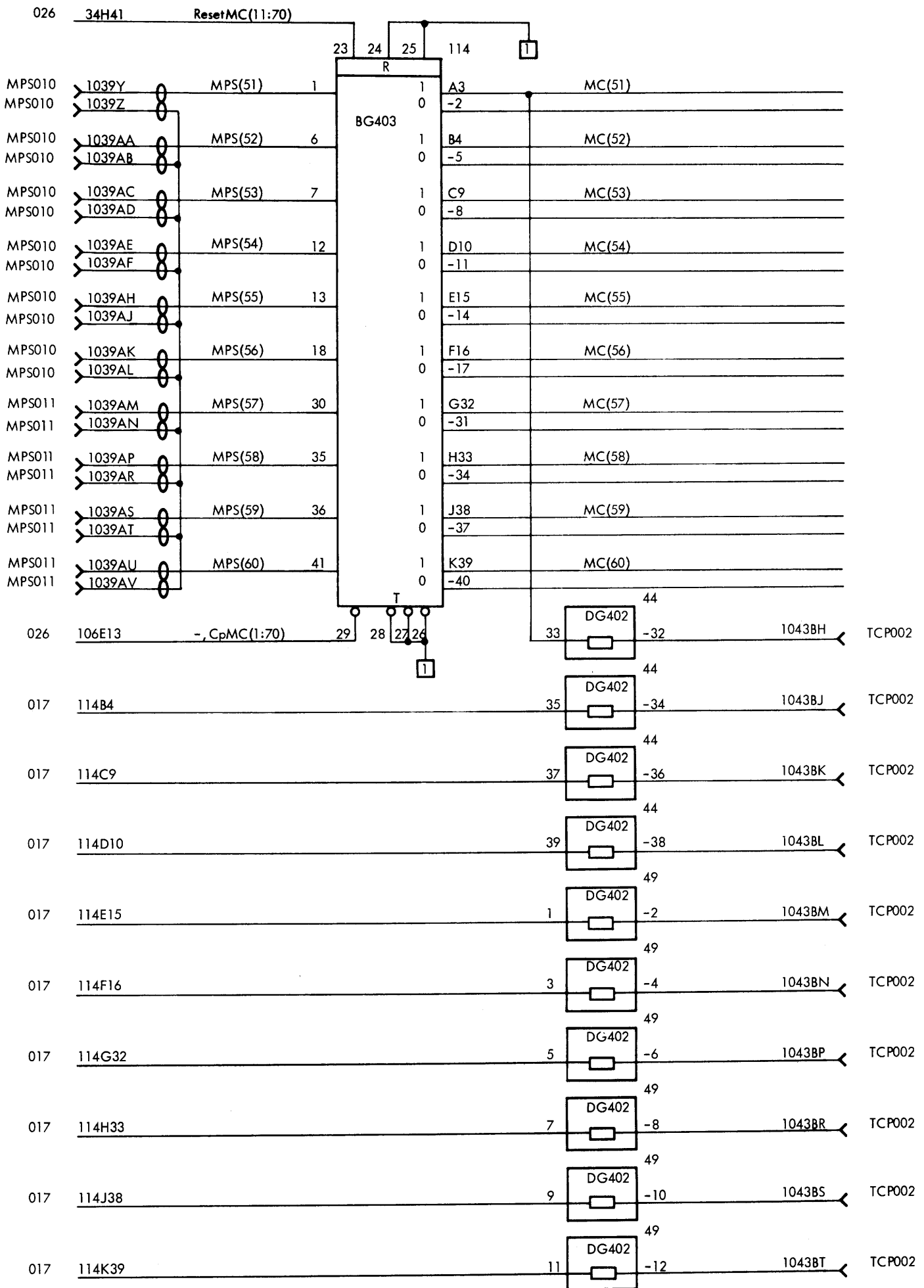
MC(31:40)

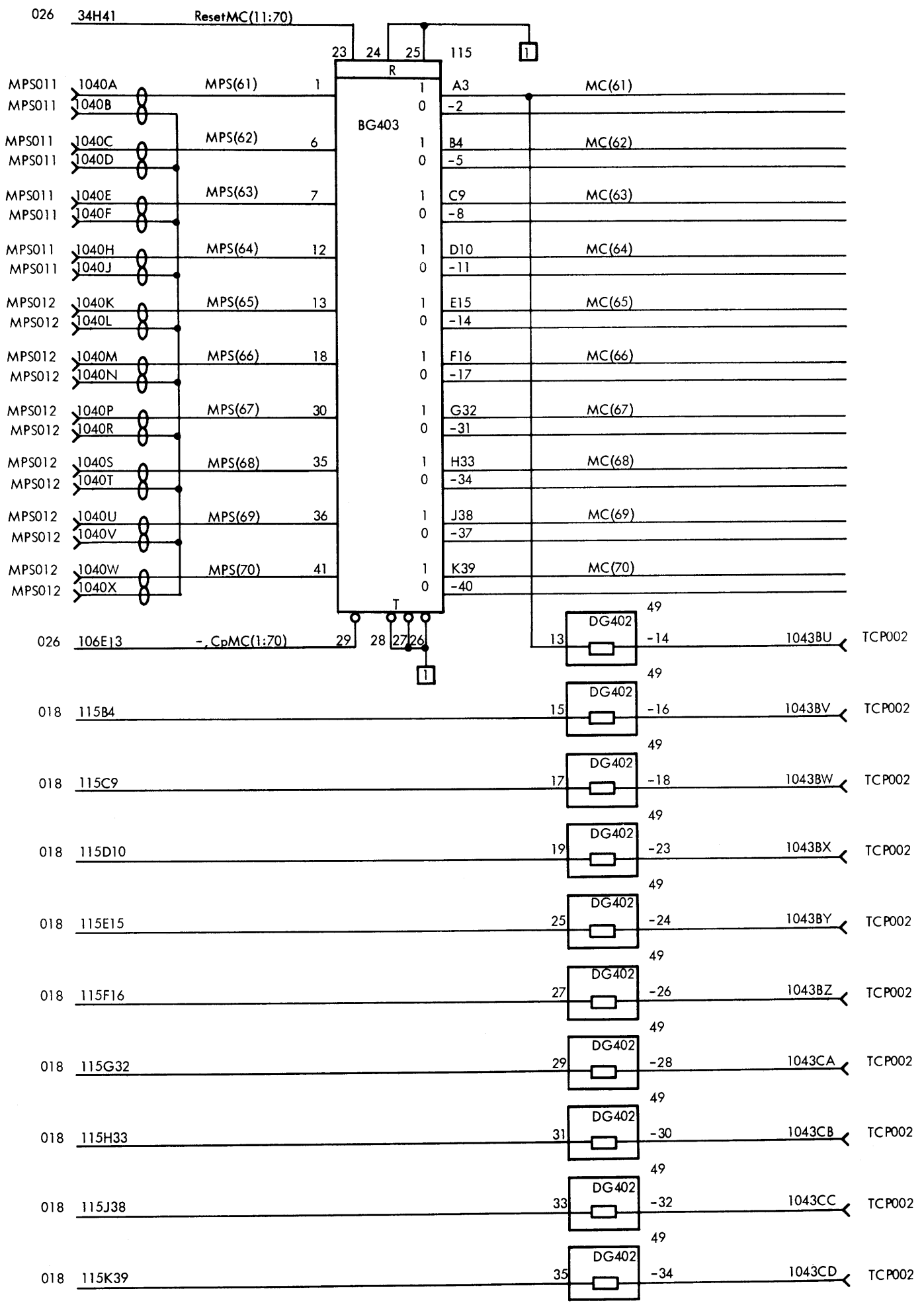
MPC015

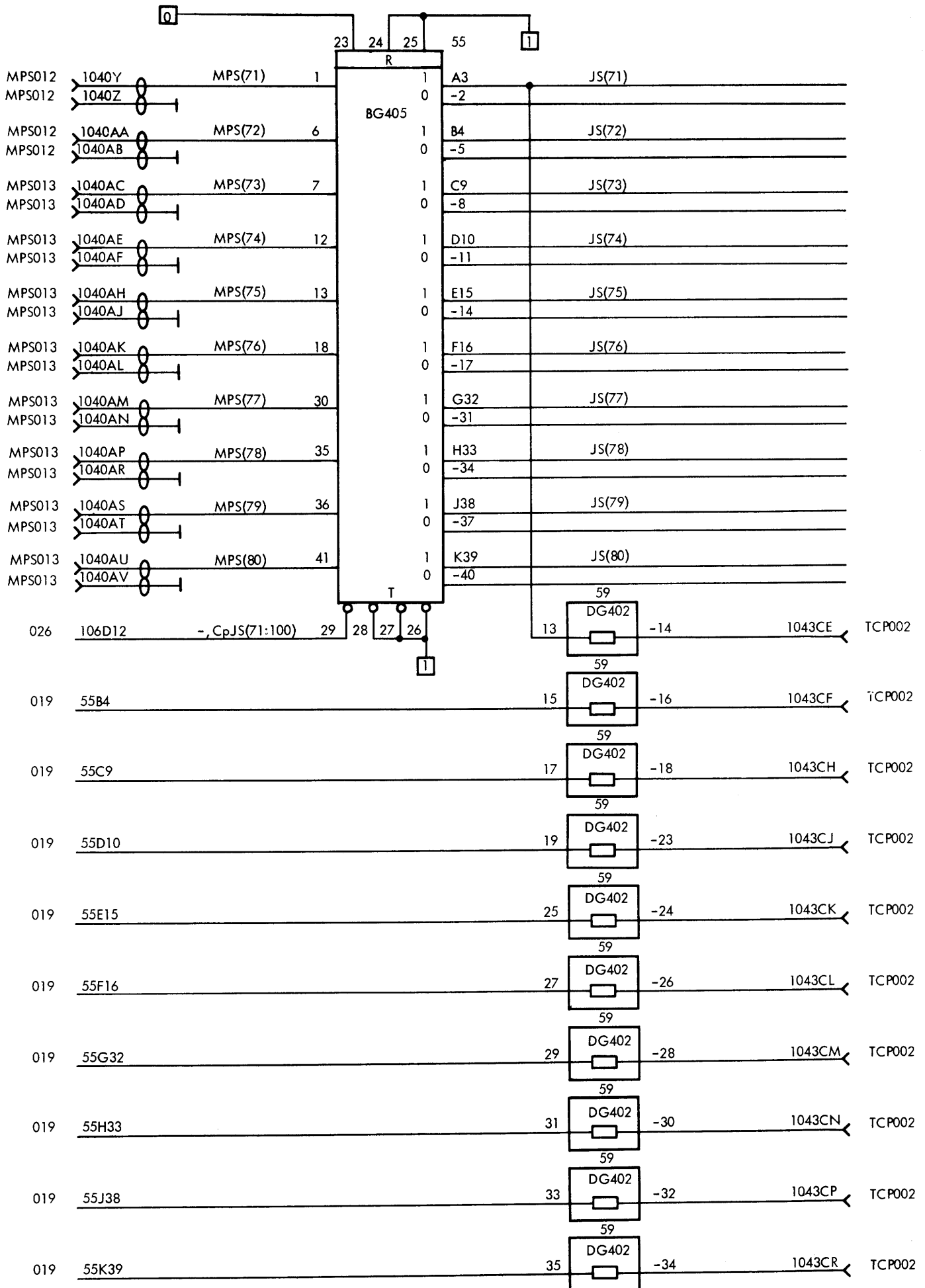
V10252

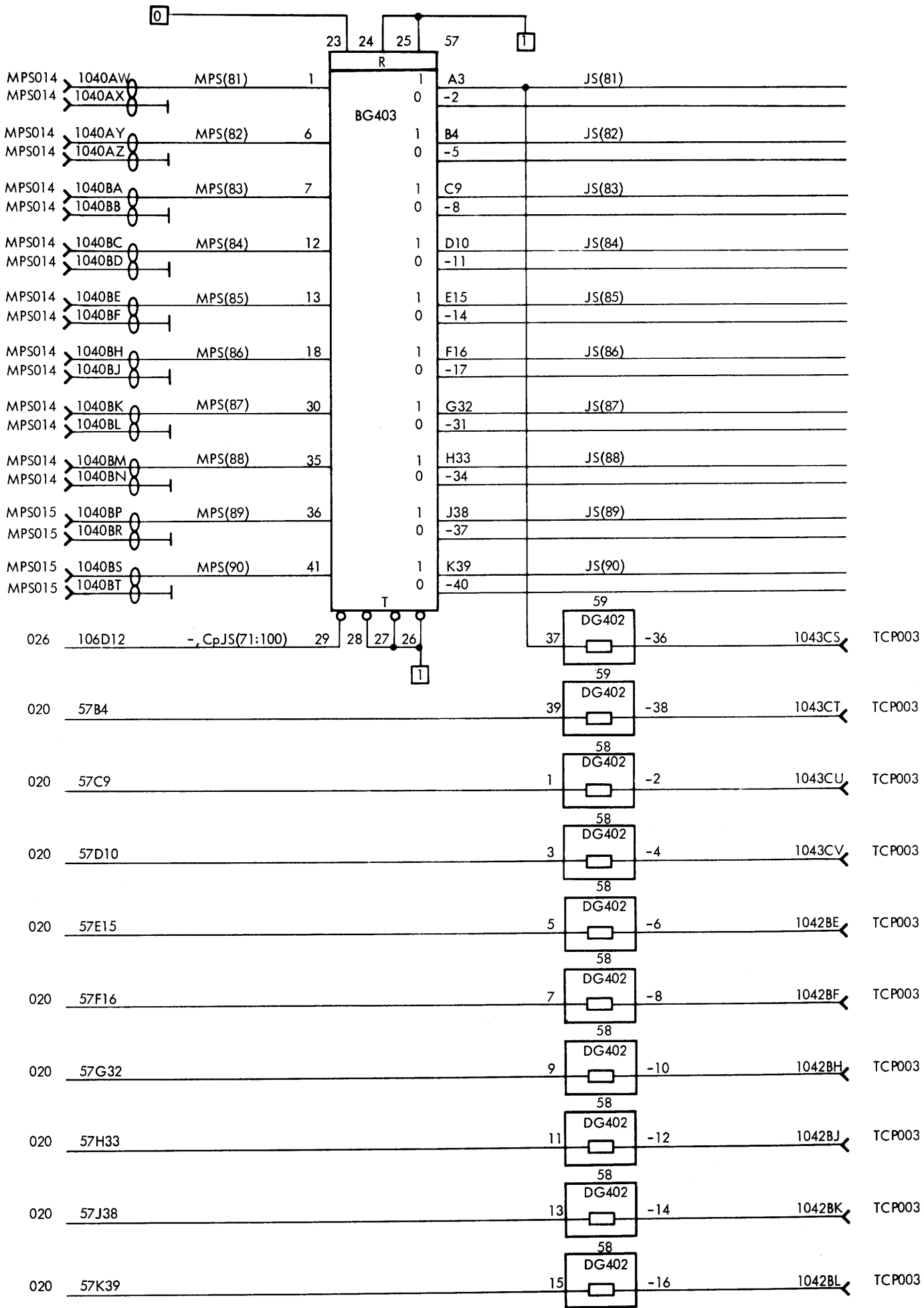
Logic Diagram

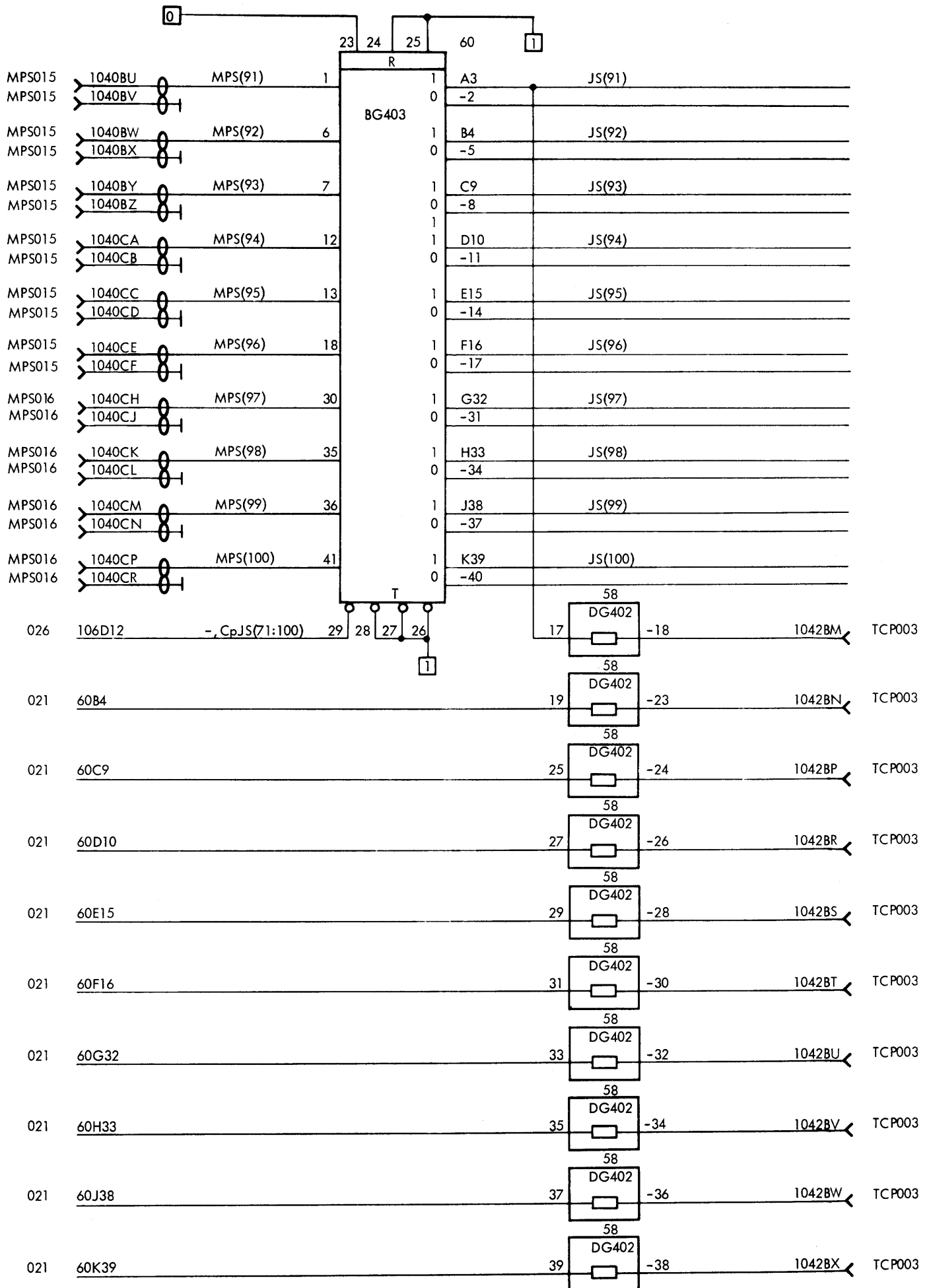


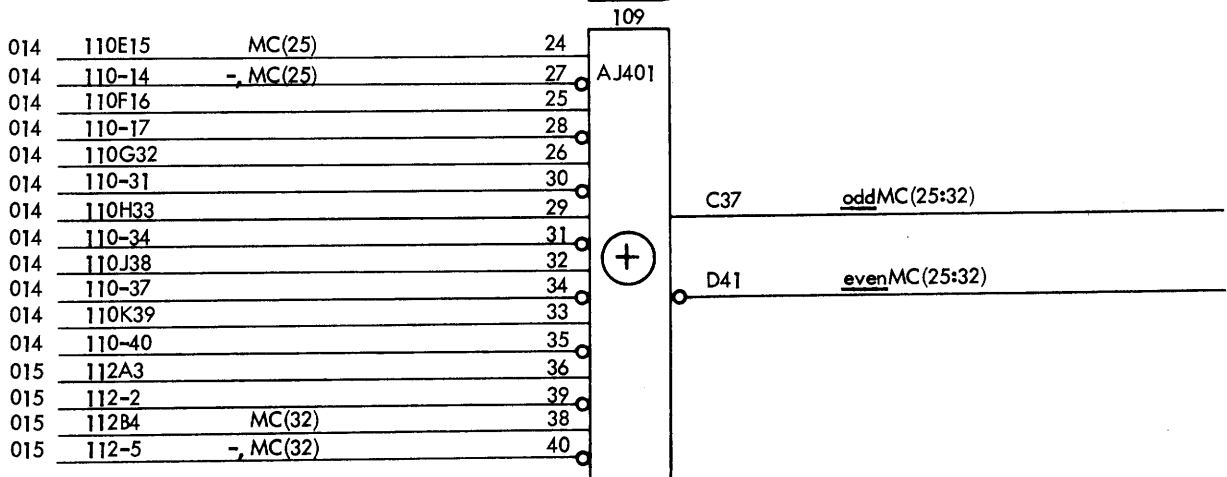
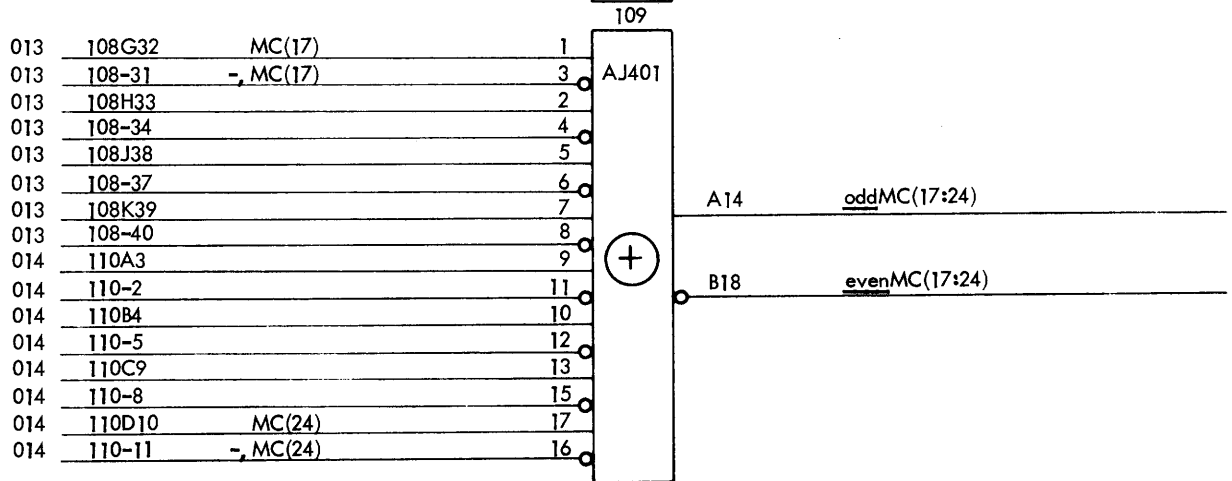
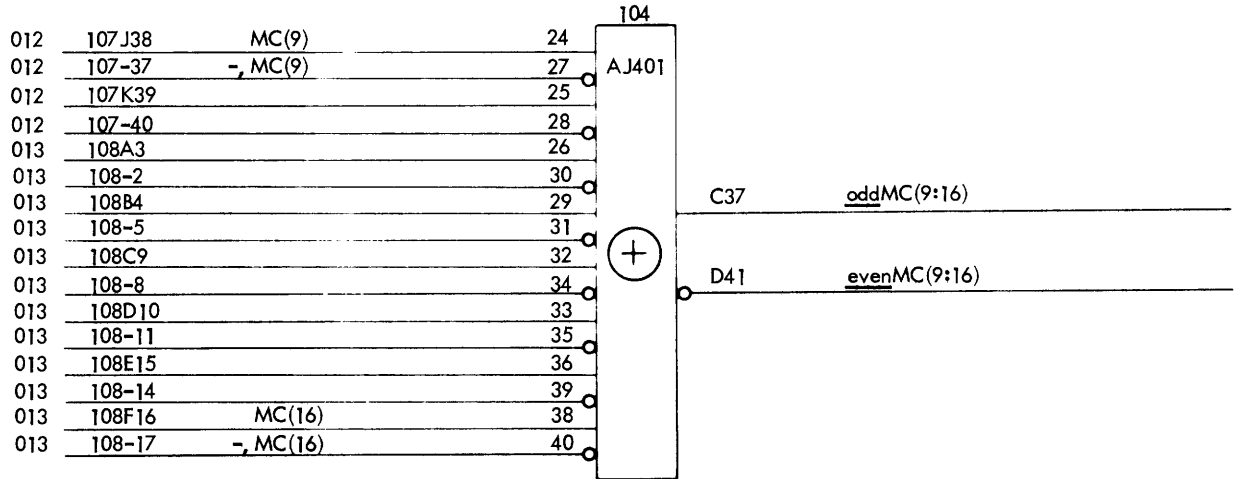
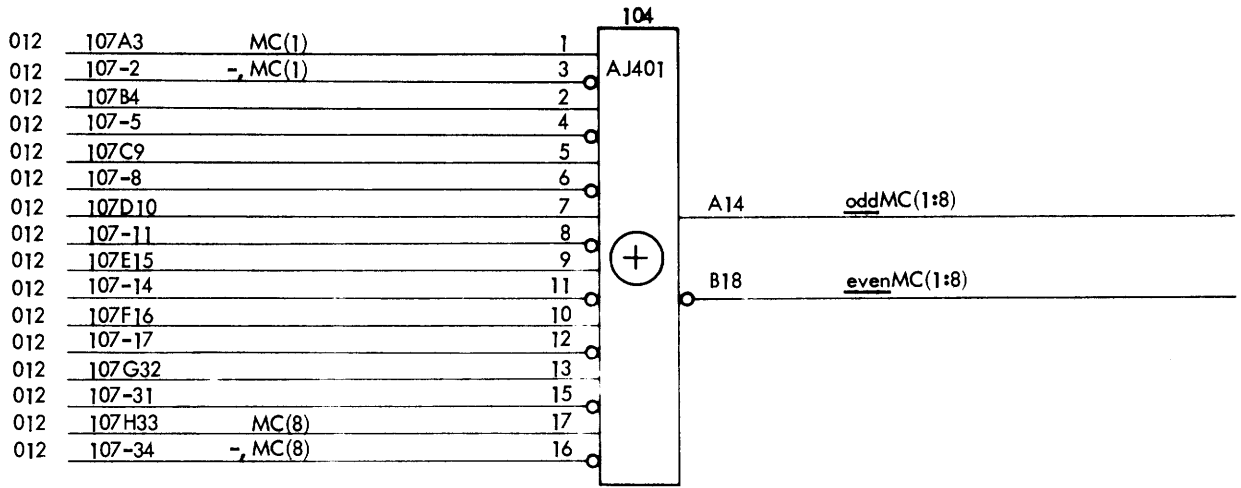


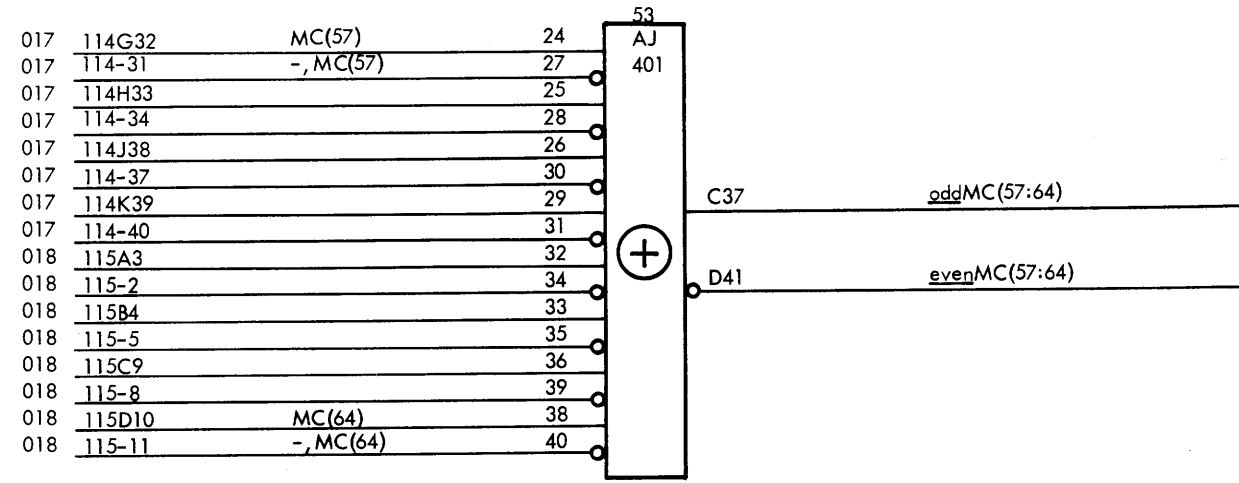
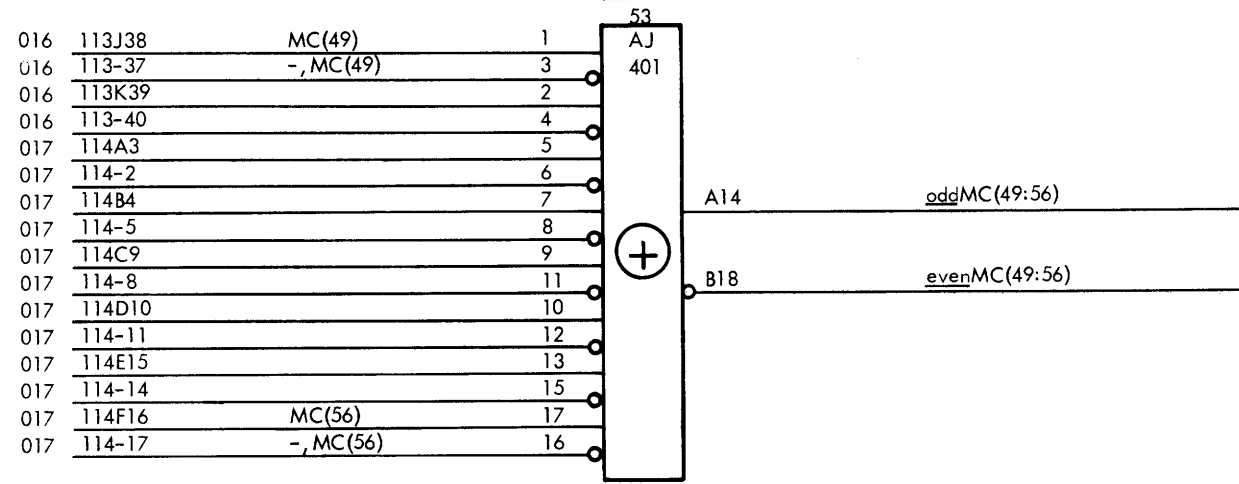
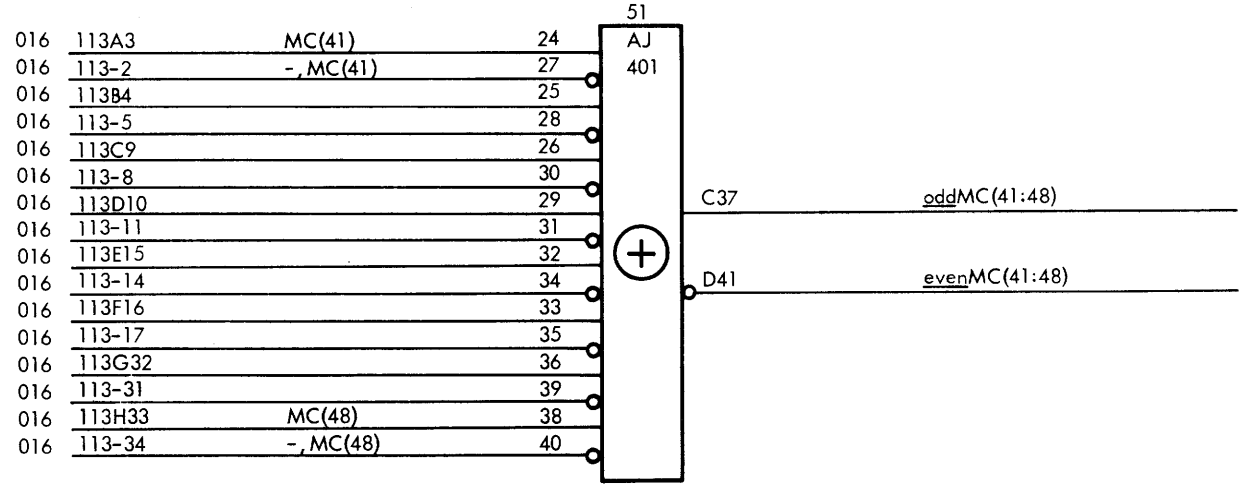
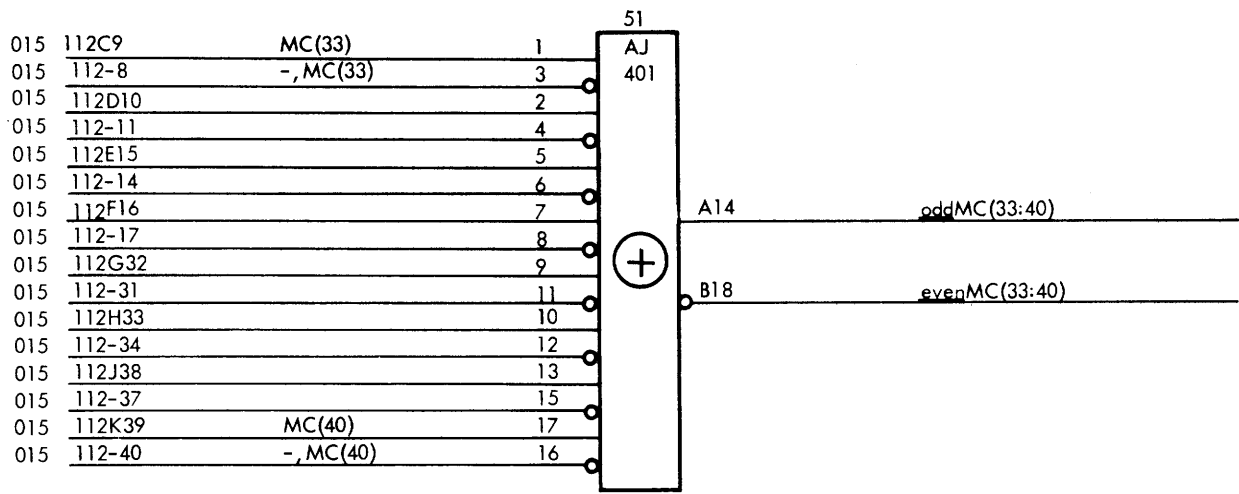


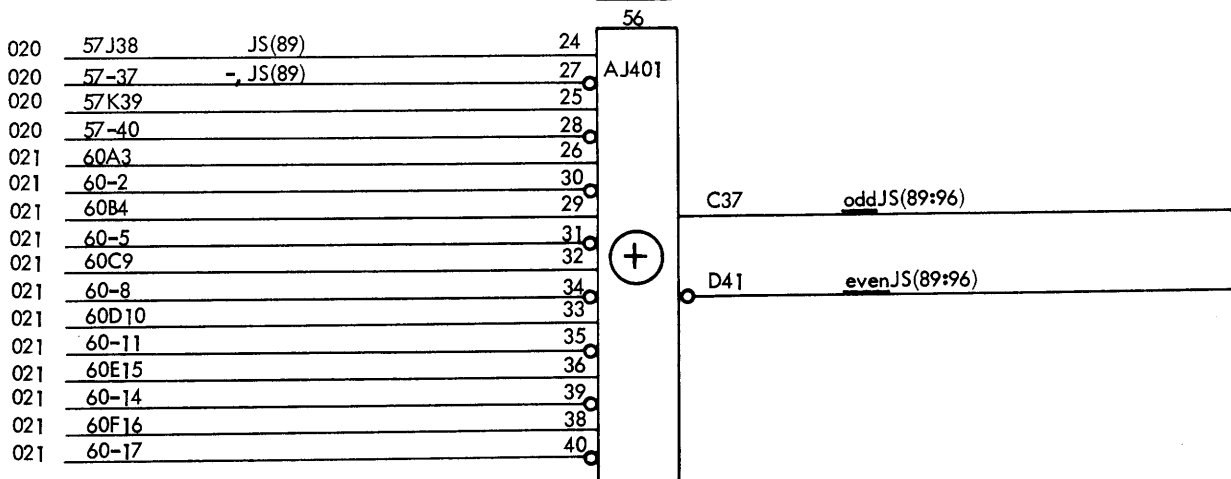
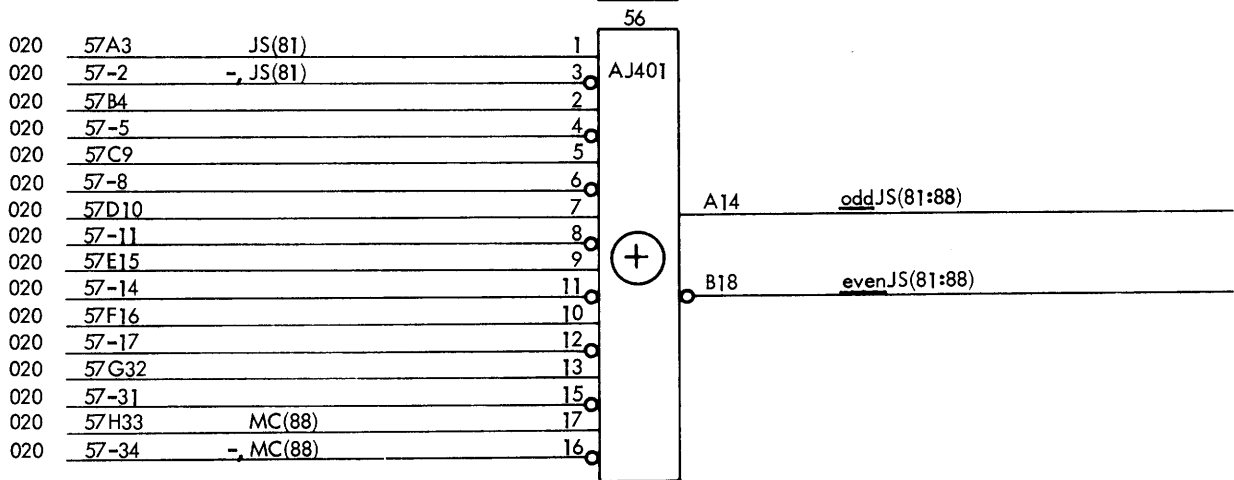
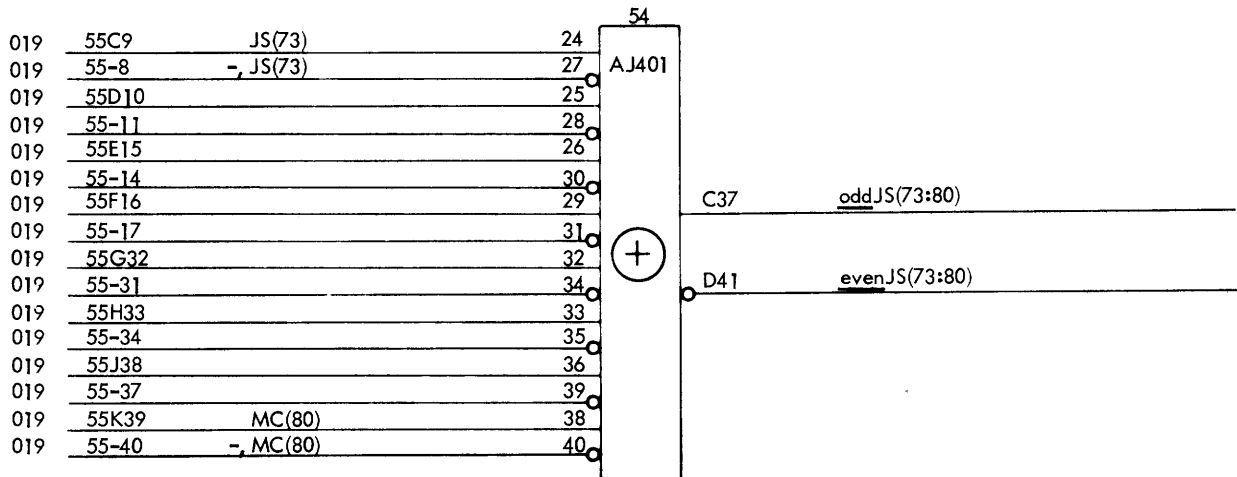
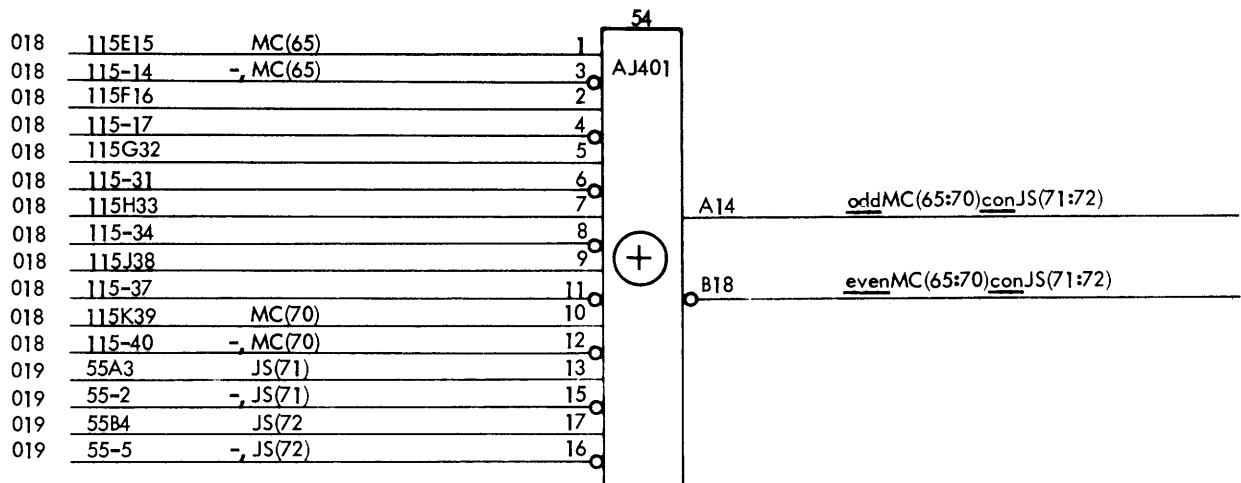


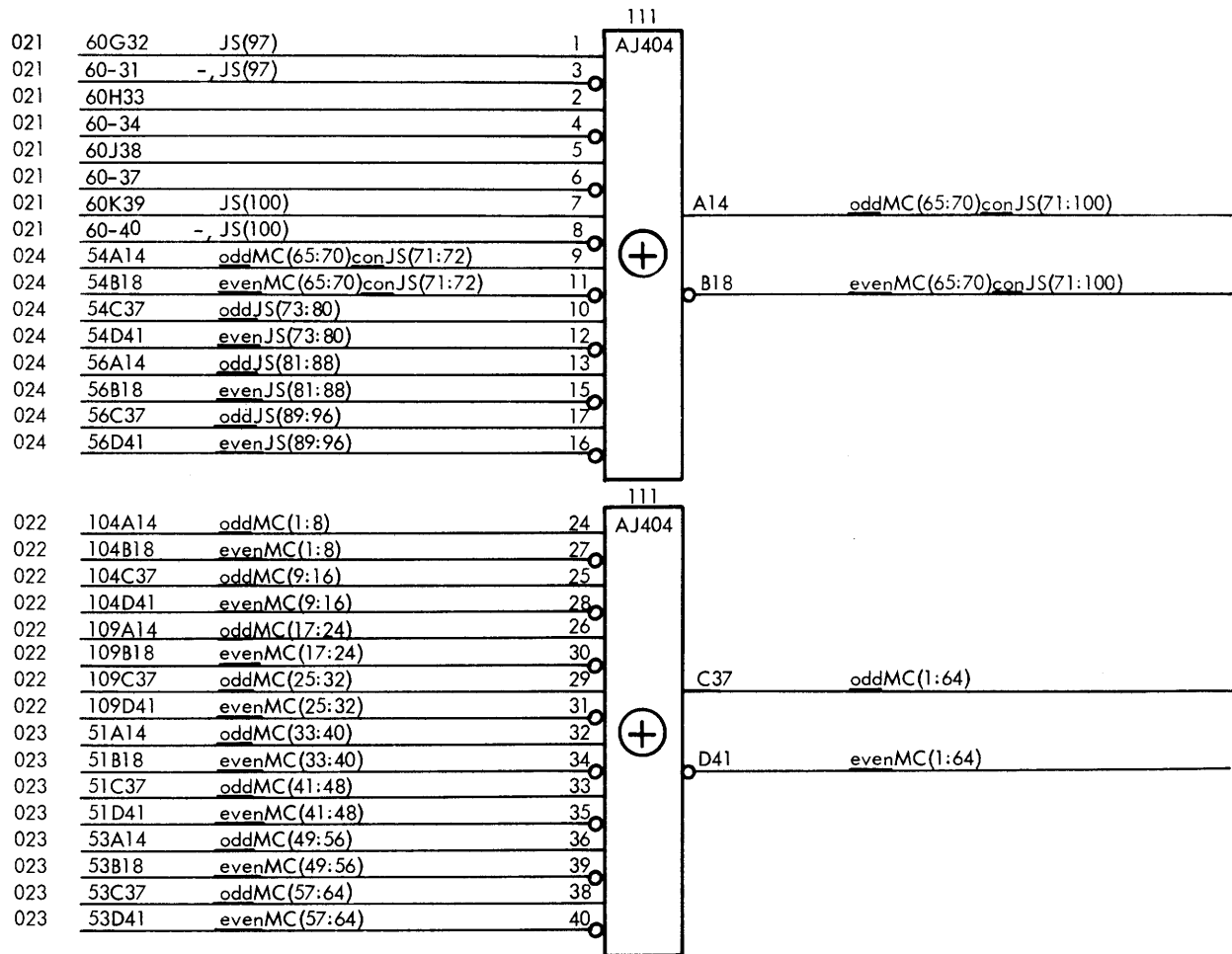


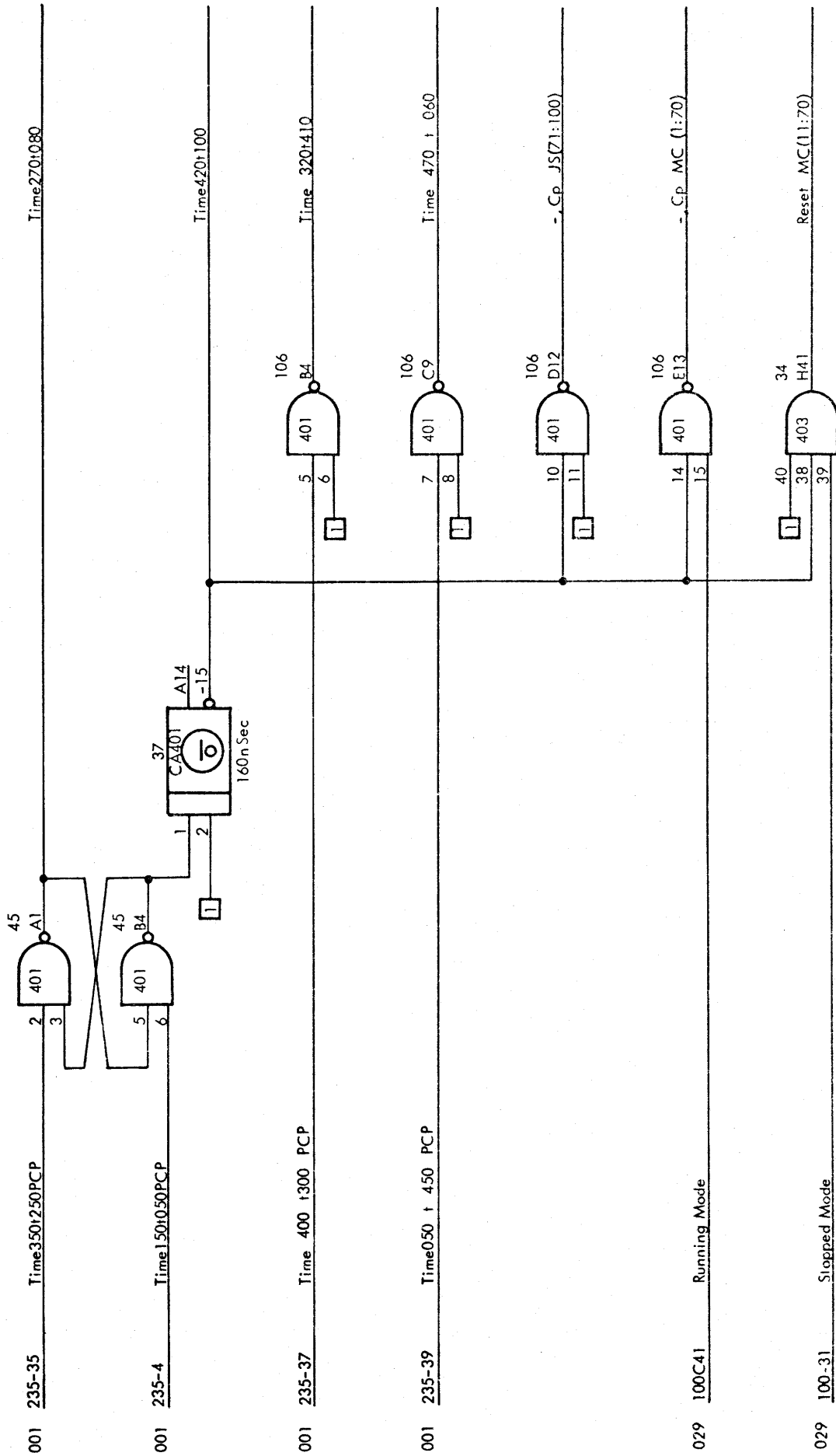


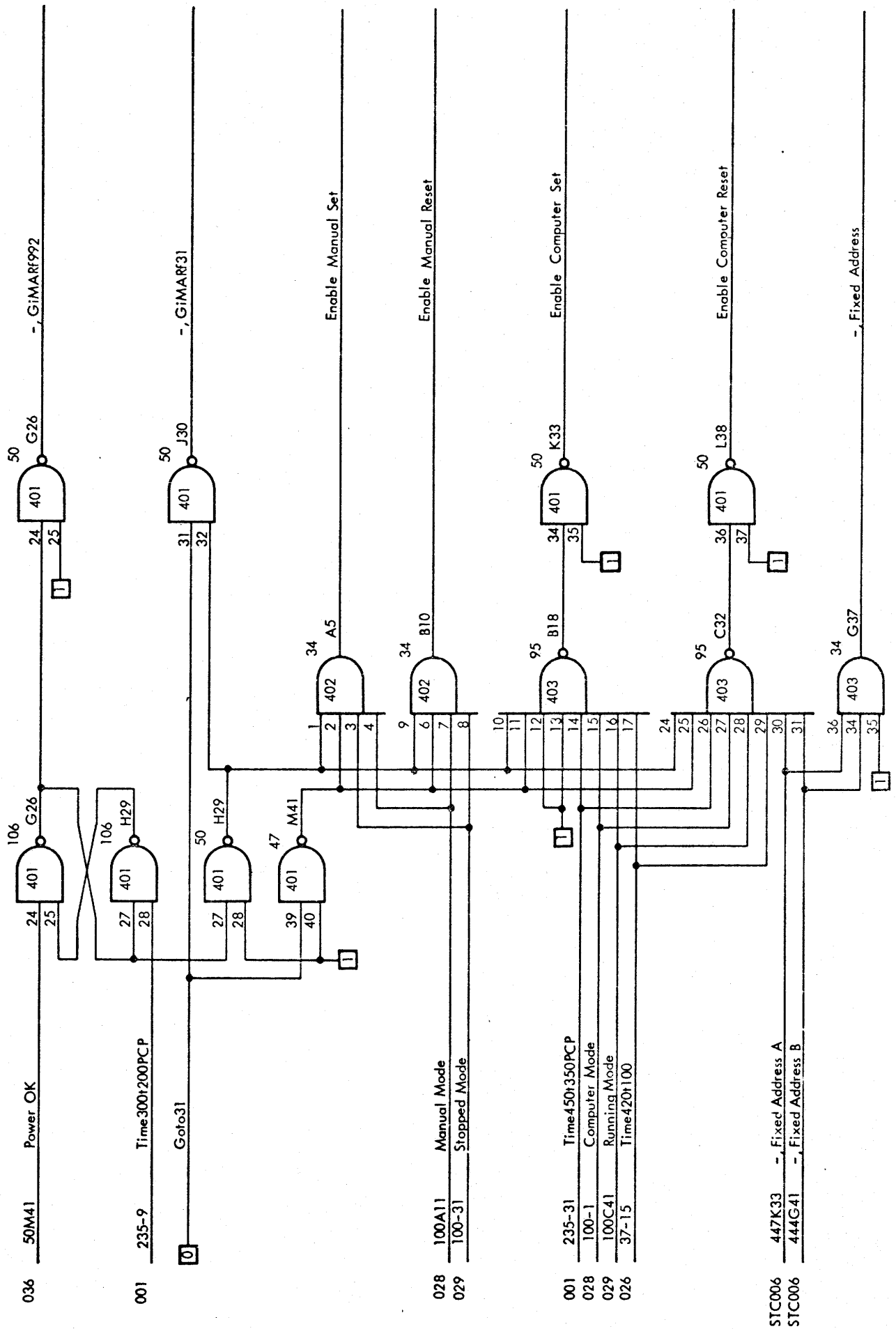


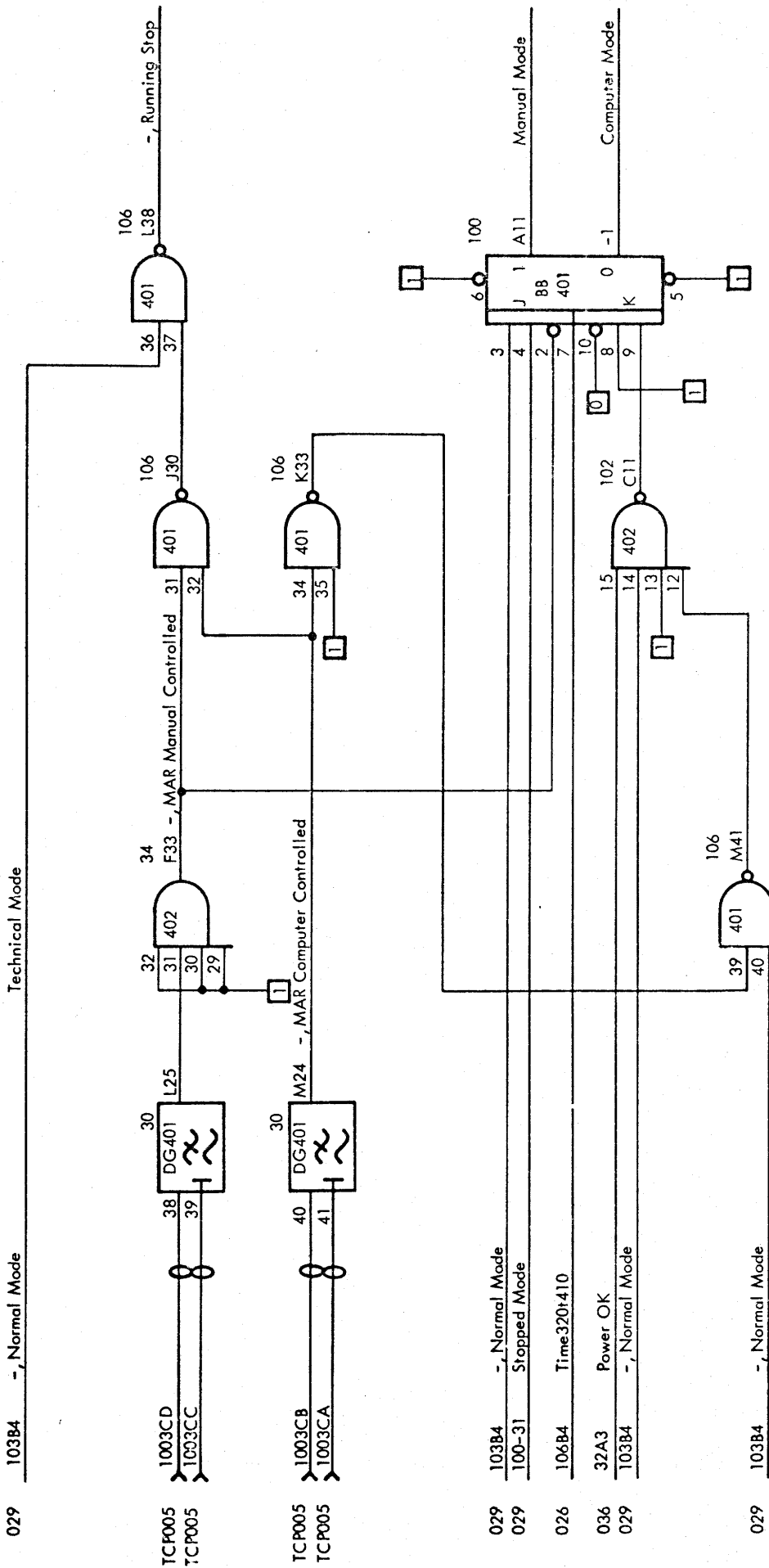






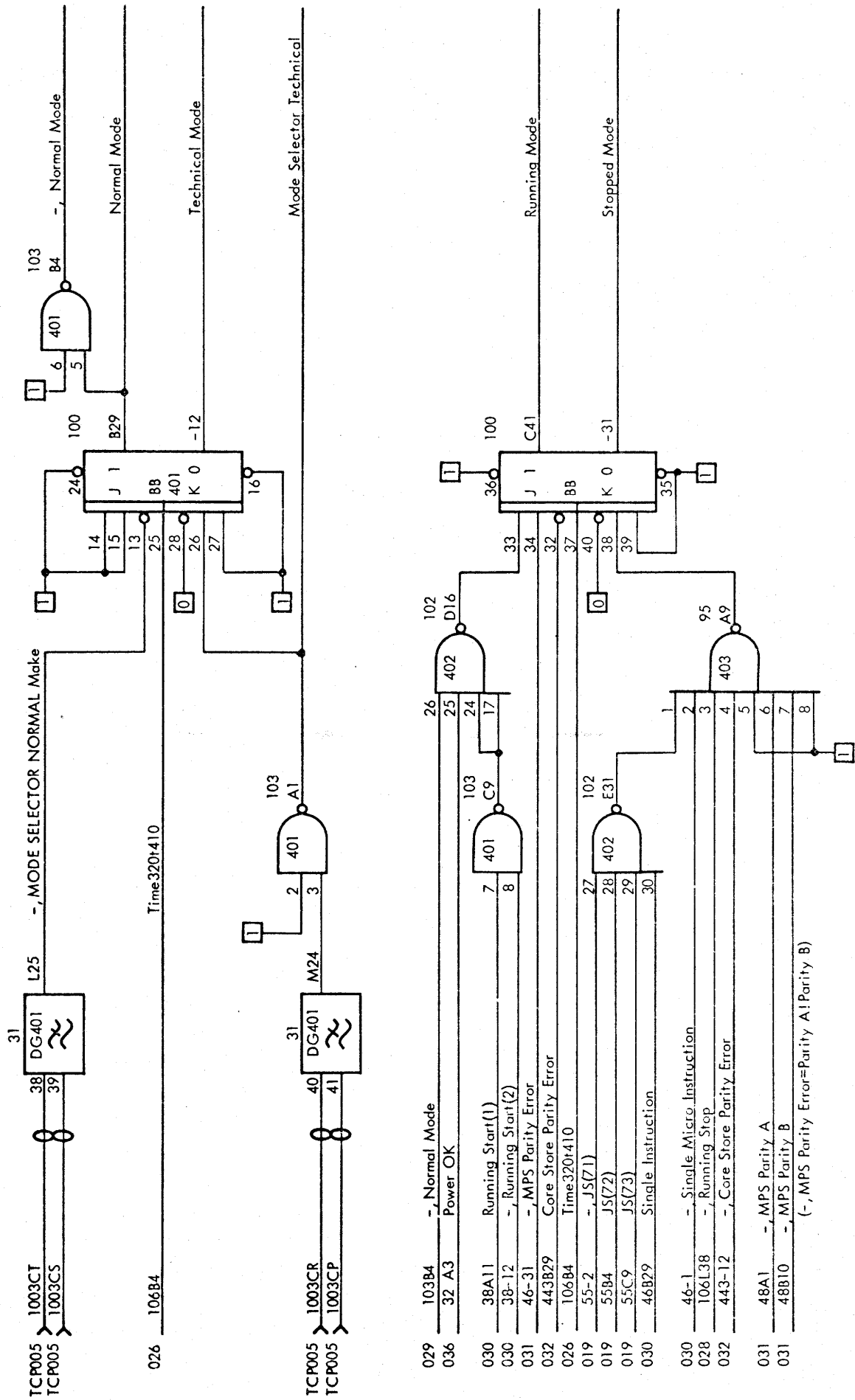


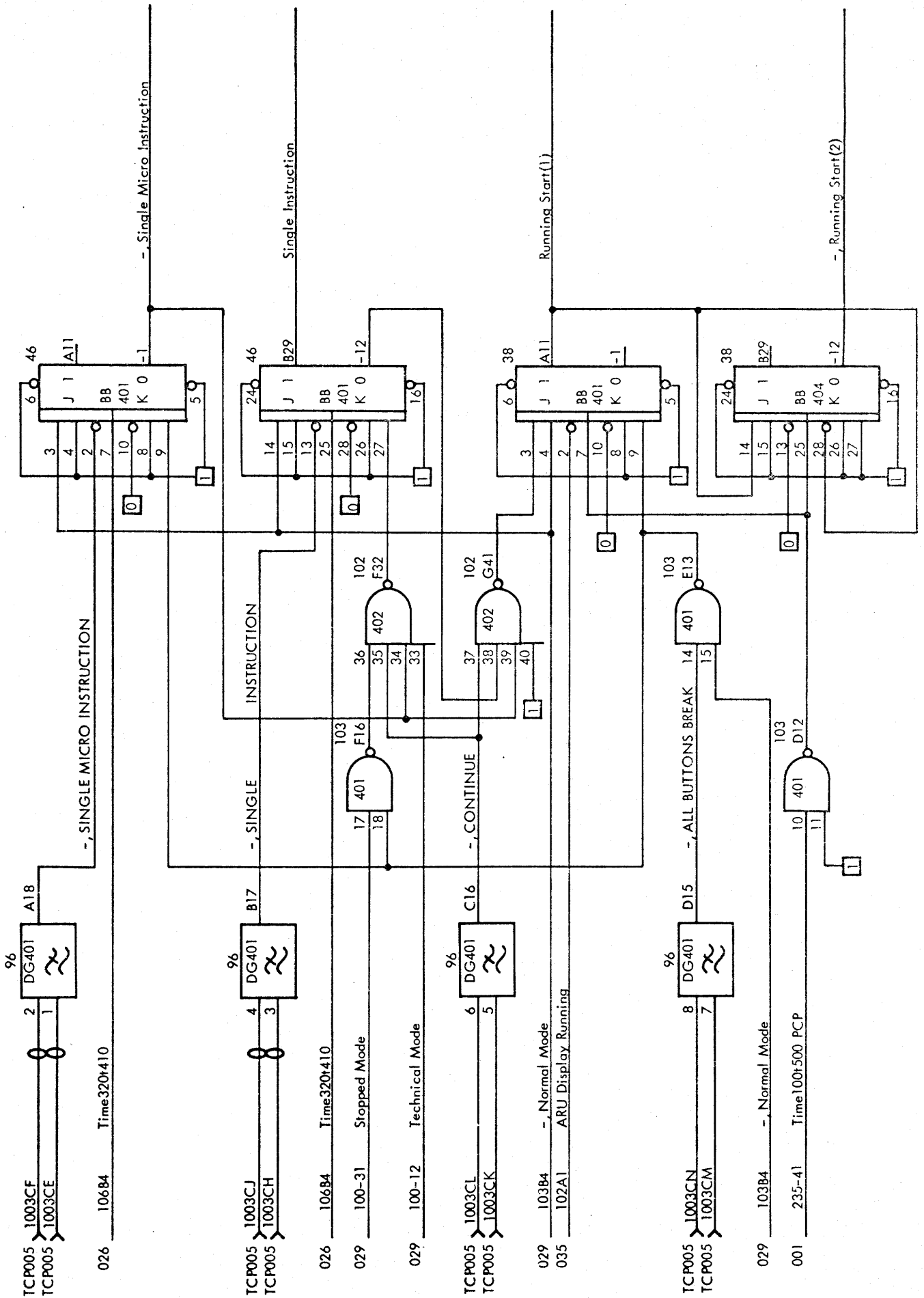




MANUAL MODE

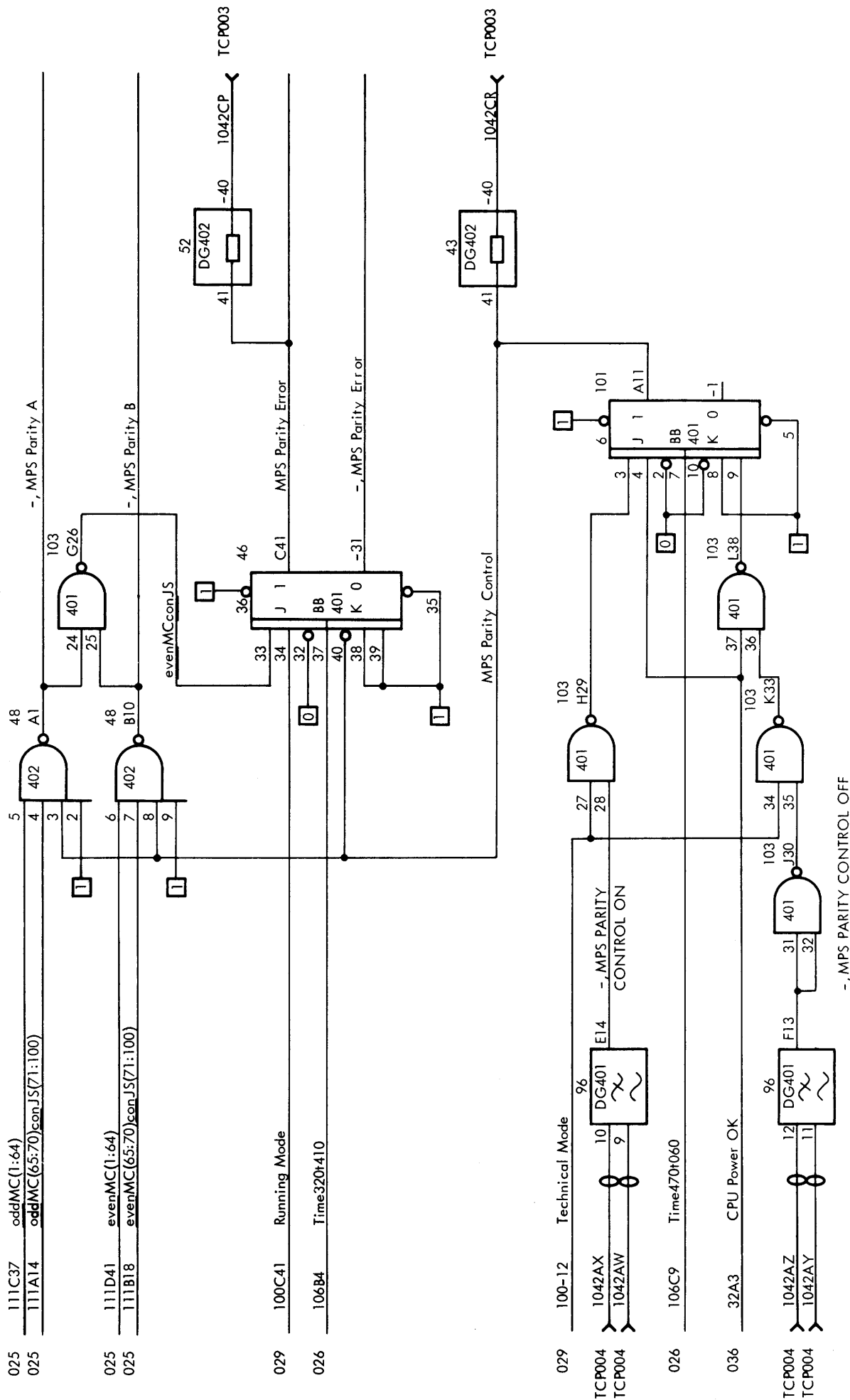
Logic Diagram





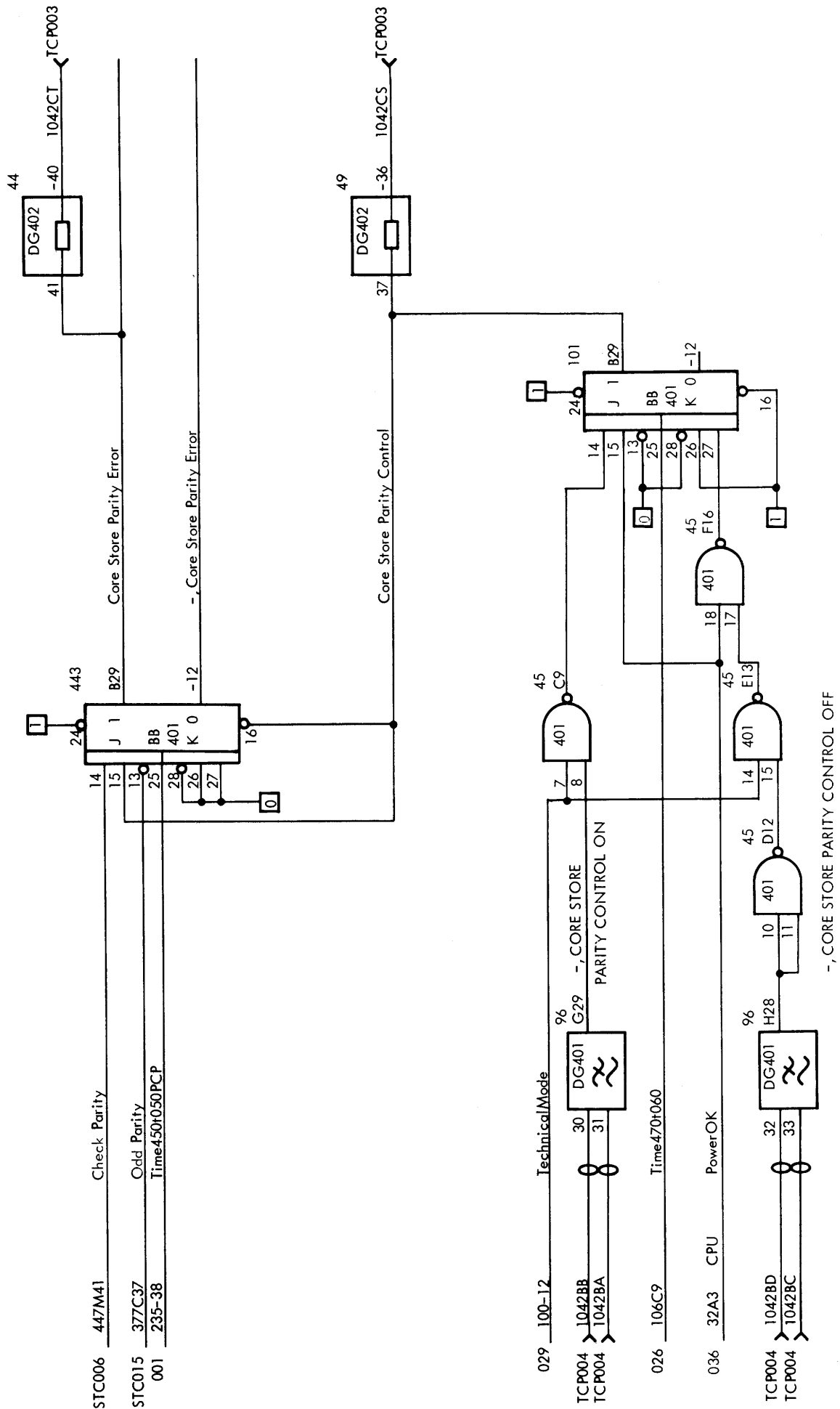
MPS PARITY CONTROL

Logic Diagram

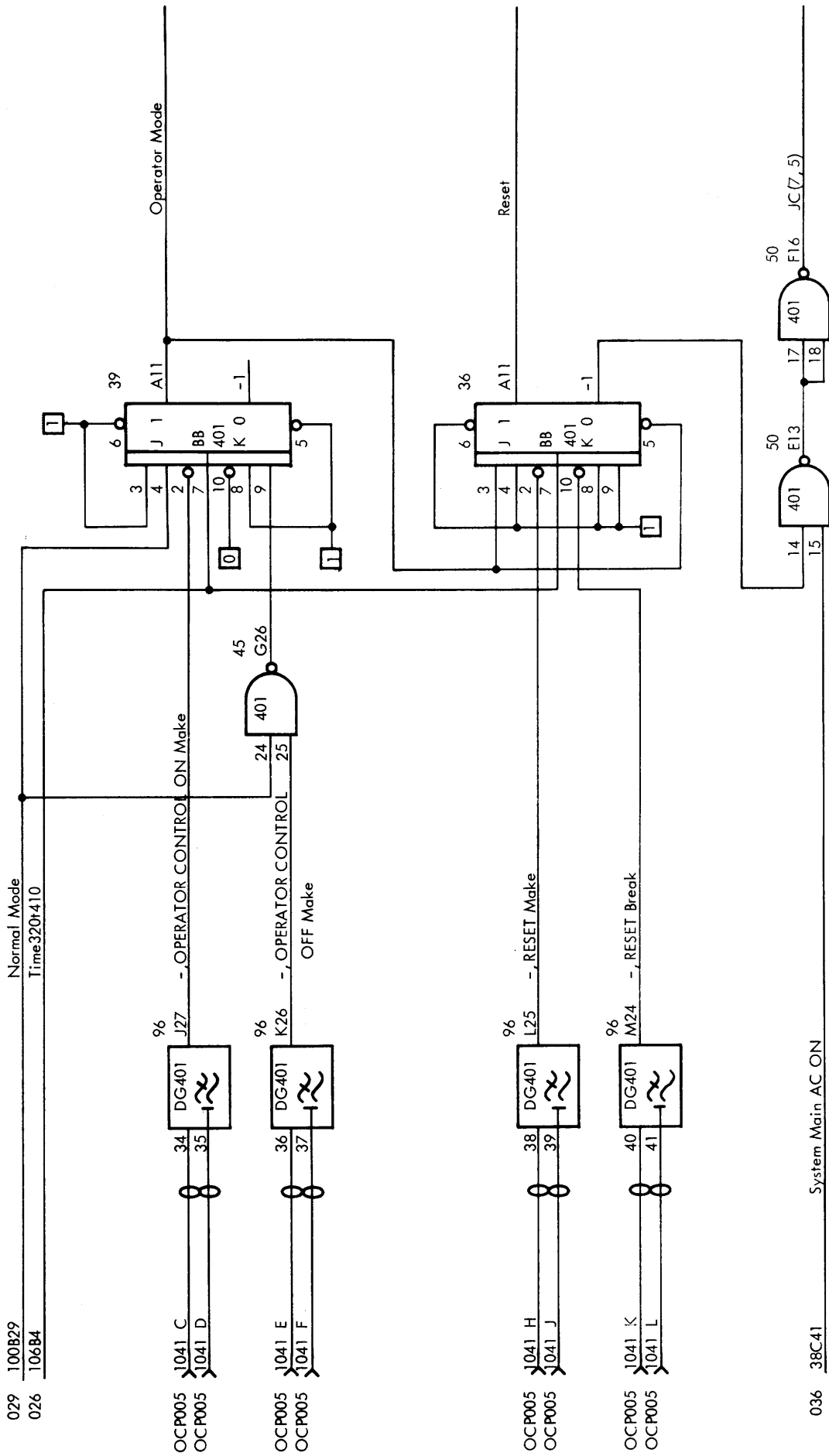


CORE STORE PARITY CONTROL

Logic Diagram



OPERATOR MODE AND CONDITION RESET



Main Power Key ON
~~Core Stop Power OK~~
 & - , RESET

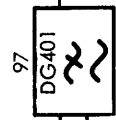
033 39A11
026 106B4

Operator Mode
Time320:410

OC P005

1041 M

2 1

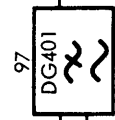


A18 - START Make

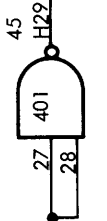
OC P005

1041 P

4 3



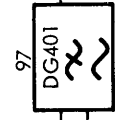
B17



OC P005

1041 S

6 5

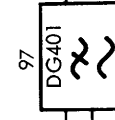


C16 - AUTOLOAD Make

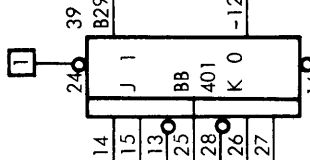
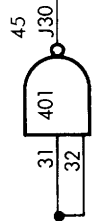
OC P005

1041 U

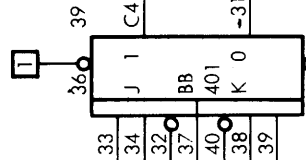
8 7



D15



Start, JC(7, 1)



Autoload, JC(7, 2)

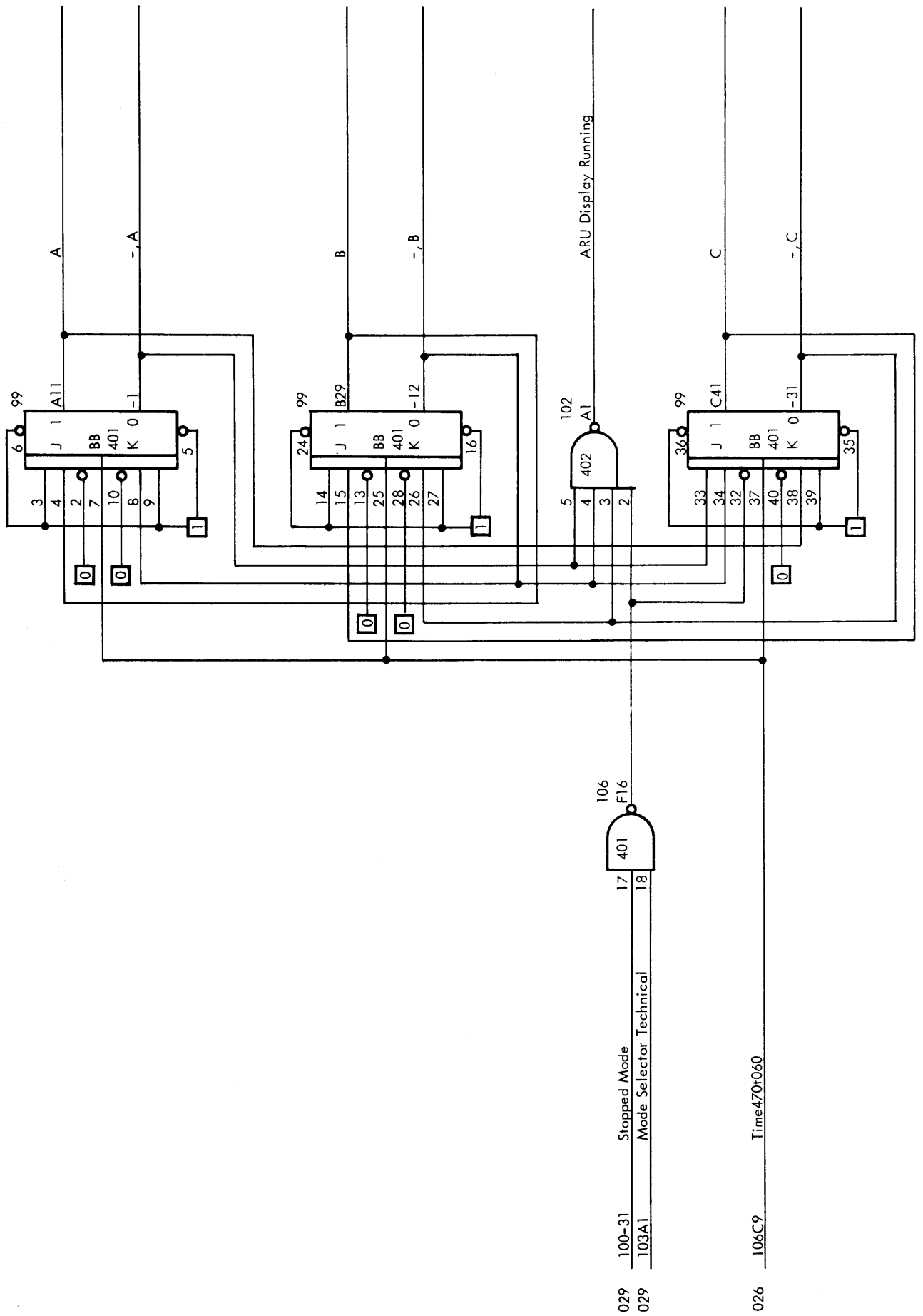


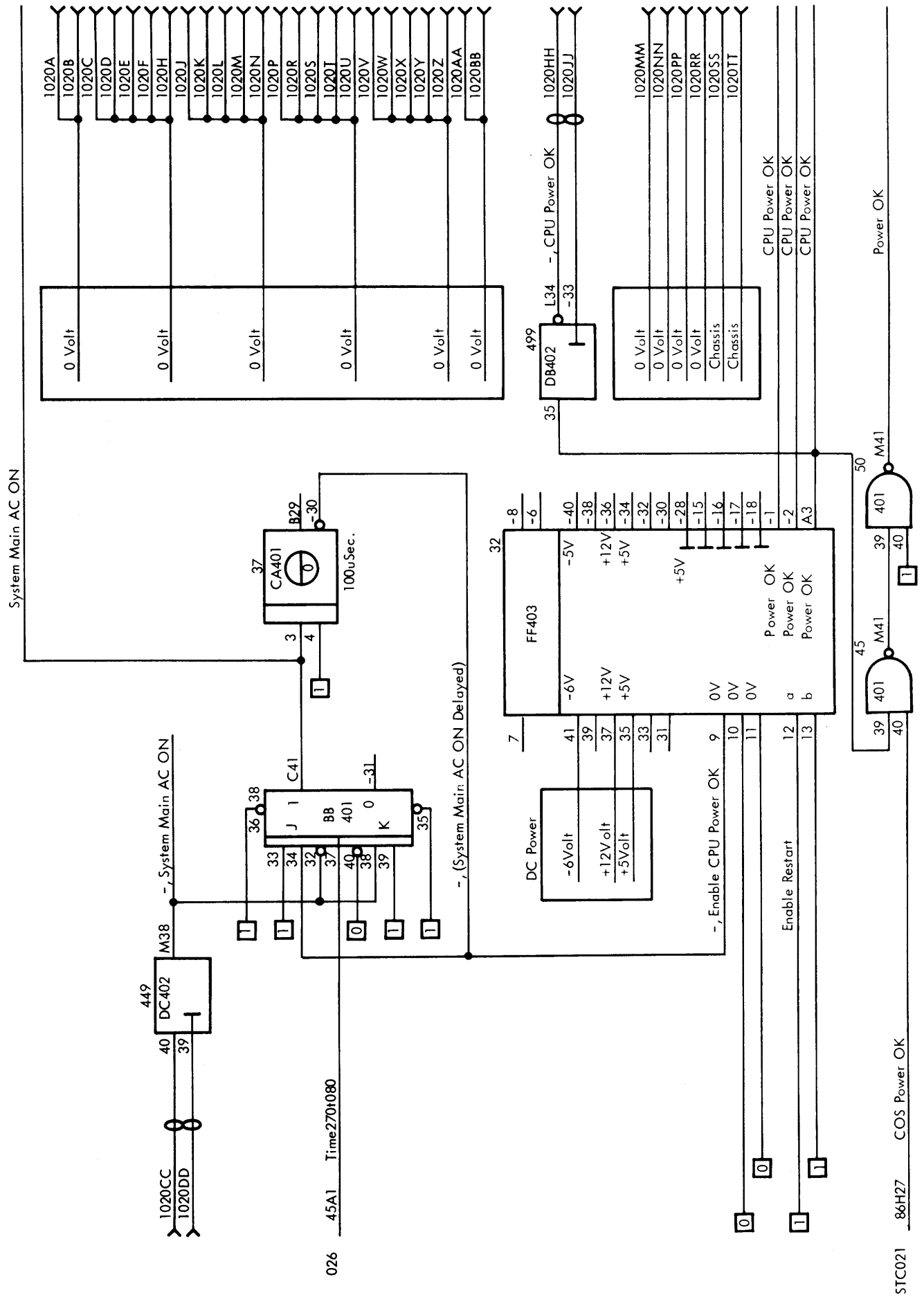
Enable Start Autoload



-(START Break AUTOLOAD Break

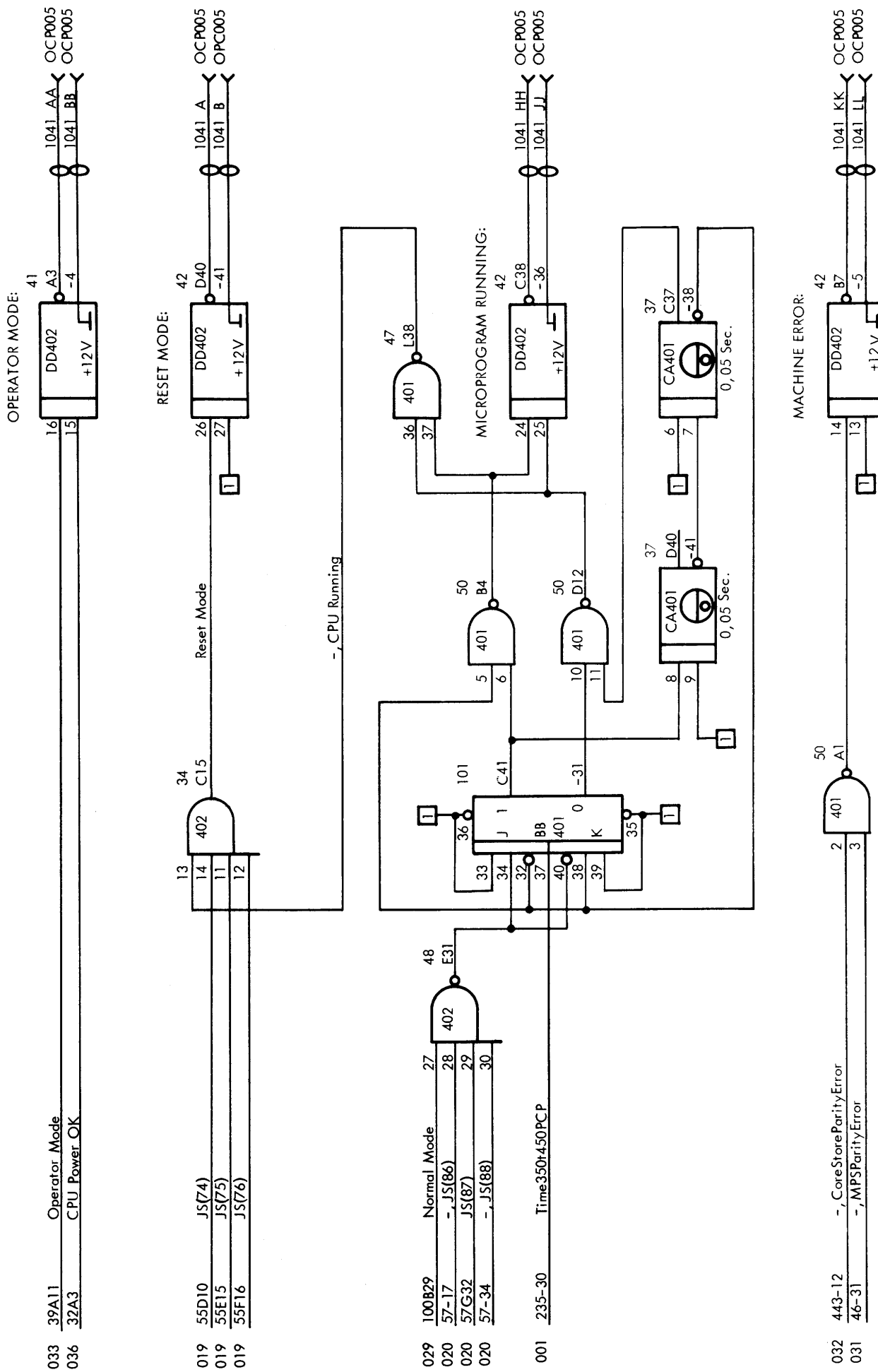
ARU DISPLAY CONTROL
Logic Diagram





LAMP CONTROL

Logic Diagram



033 39A11 Operator Mode
 036 32A3 CPU Power OK
 OC P005
 OC P005

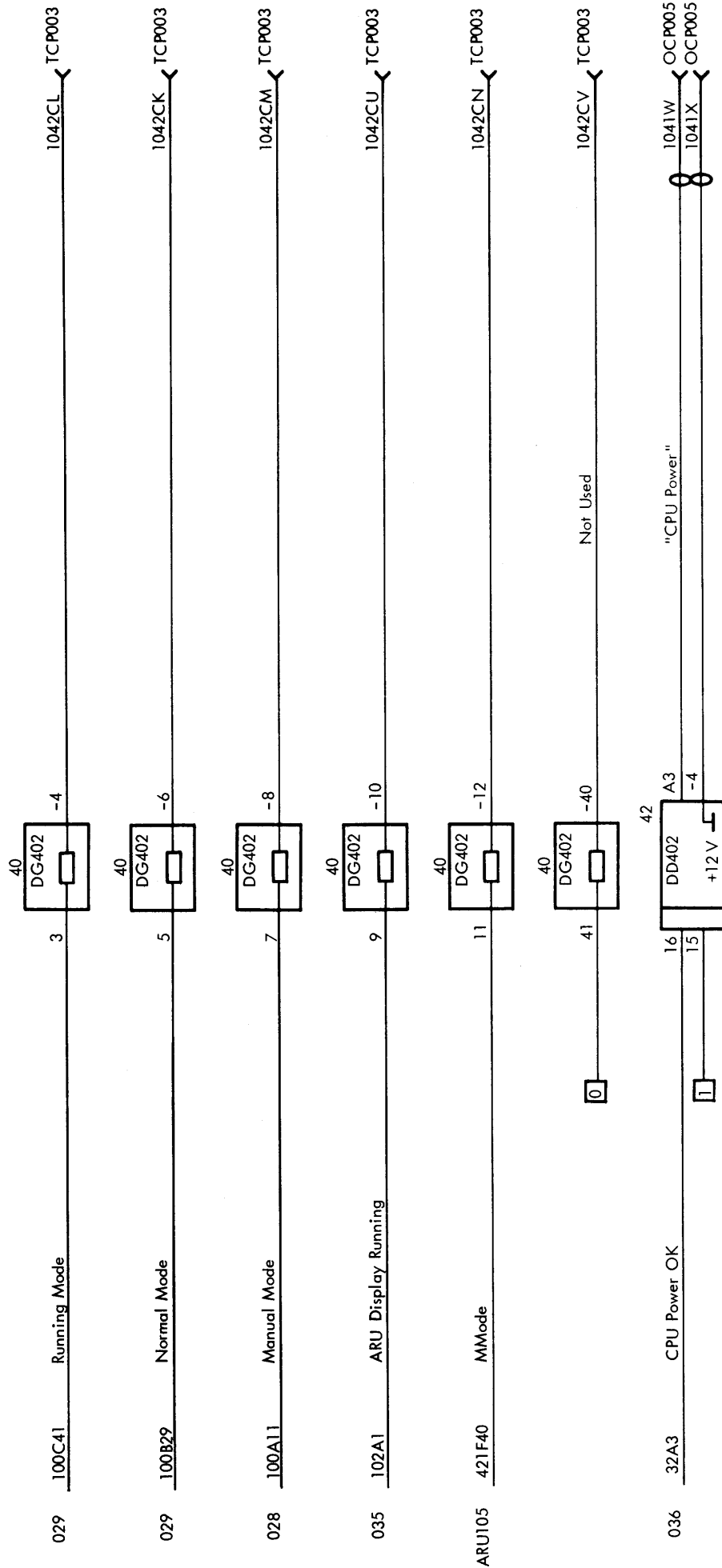
019 55D10 JS(74)
 019 55E15 JS(75)
 019 55F16 JS(76)
 C15
 42 D40
 -41
 +12V

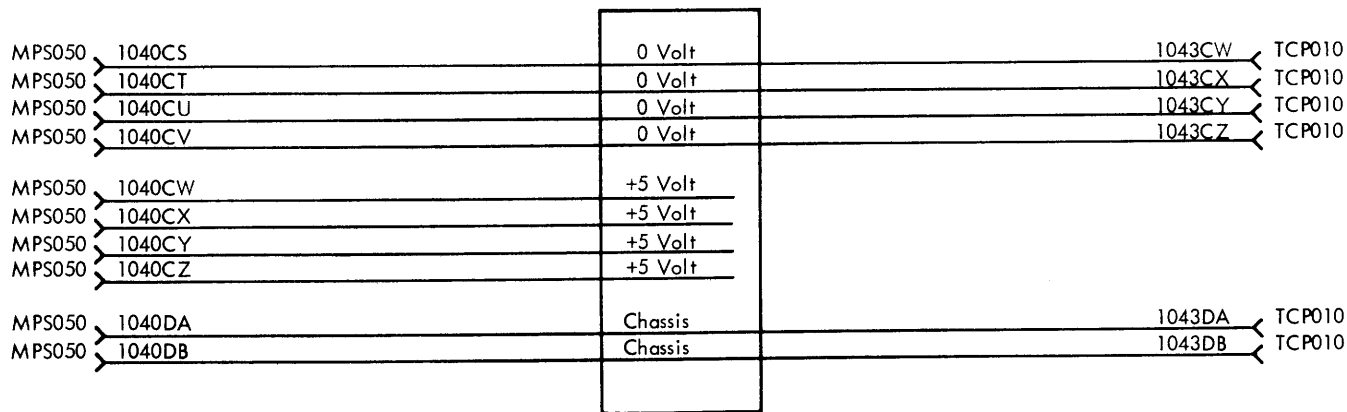
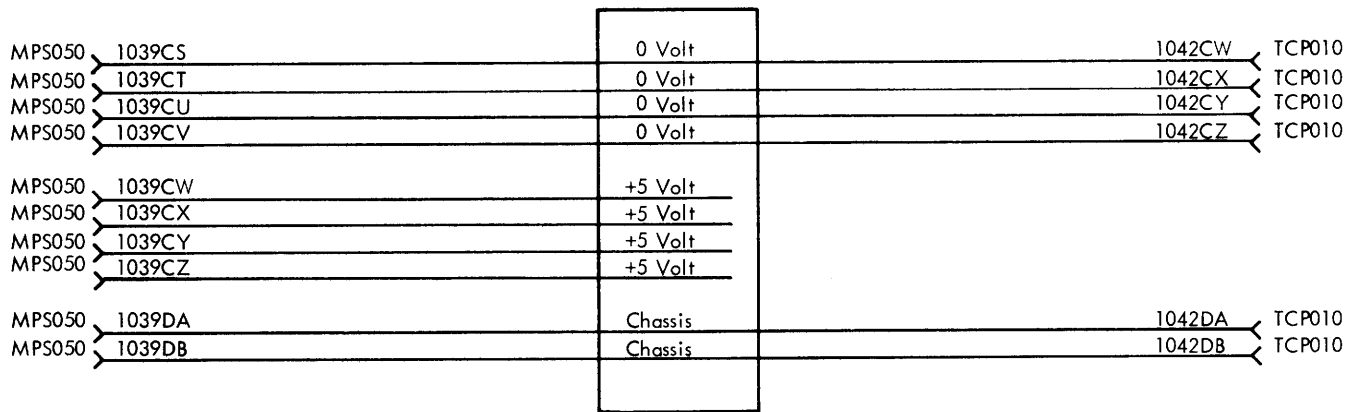
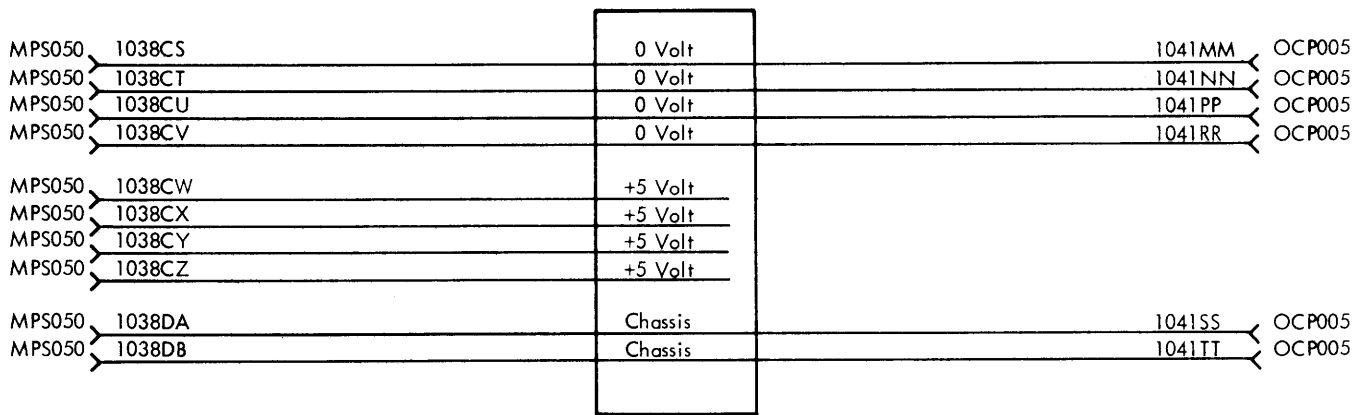
029 100B29 Normal Mode
 020 57-17 -, JS(86)
 020 57G32 JS(87)
 020 57-34 -, JS(88)
 Time 350+450 PCP
 001 235-30
 C38
 -36
 +12V
 OC P005
 OC P005

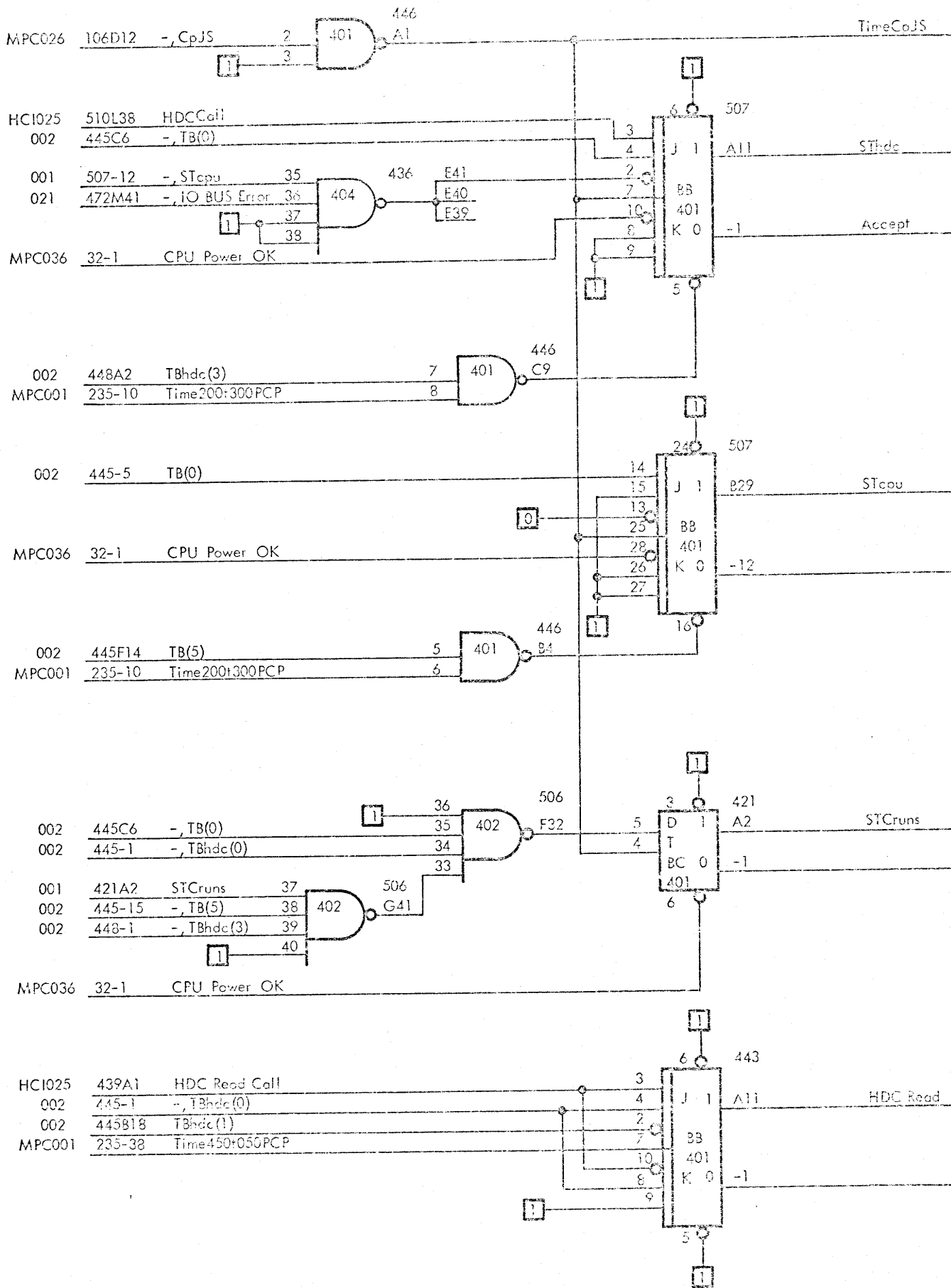
032 443-12 -, CoreStoreParityError
 031 46-31 -, MPSParityError
 42 B7
 -5
 +12V
 OC P005
 OC P005

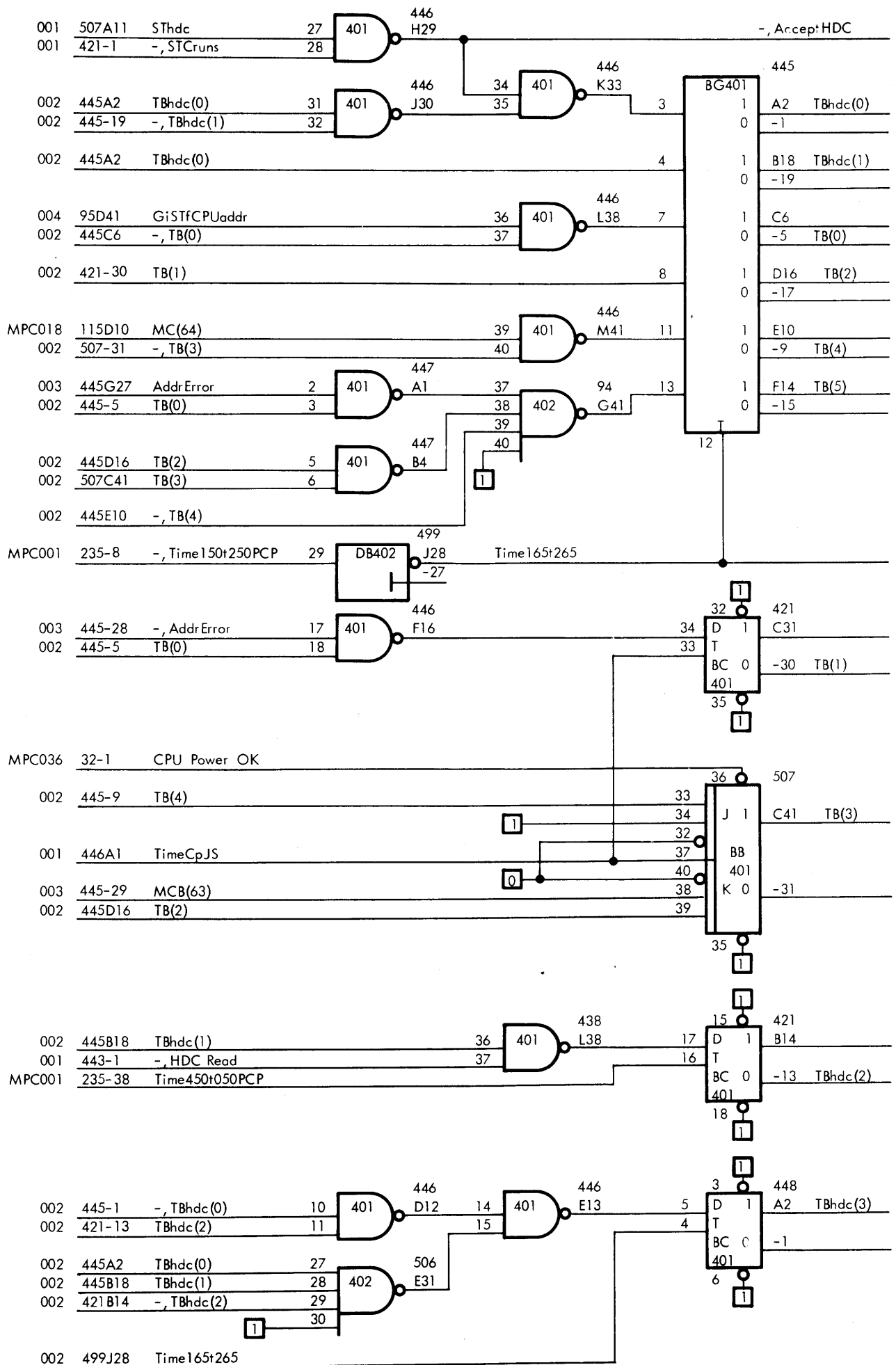
DISPLAY

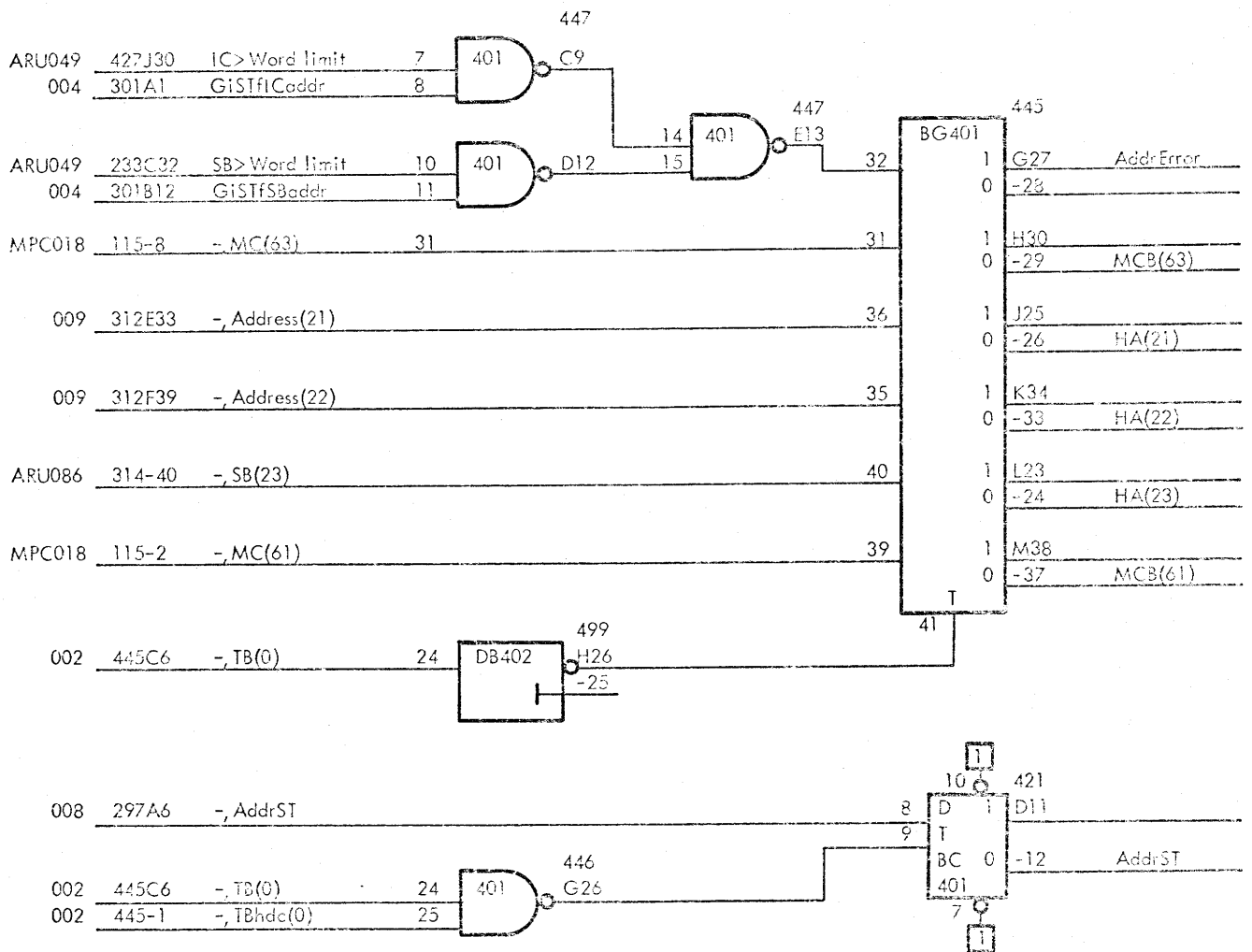
Logic Diagram

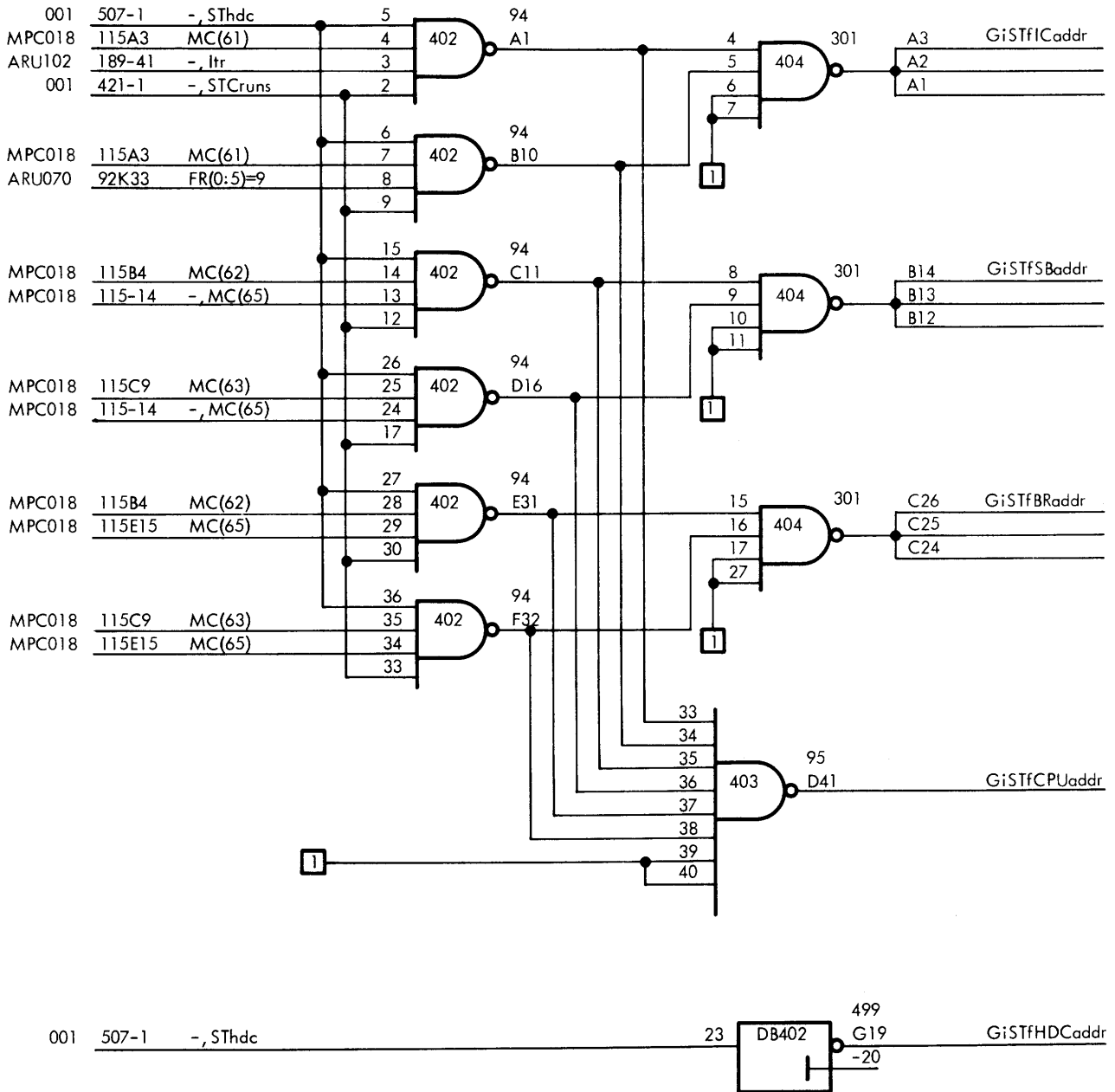


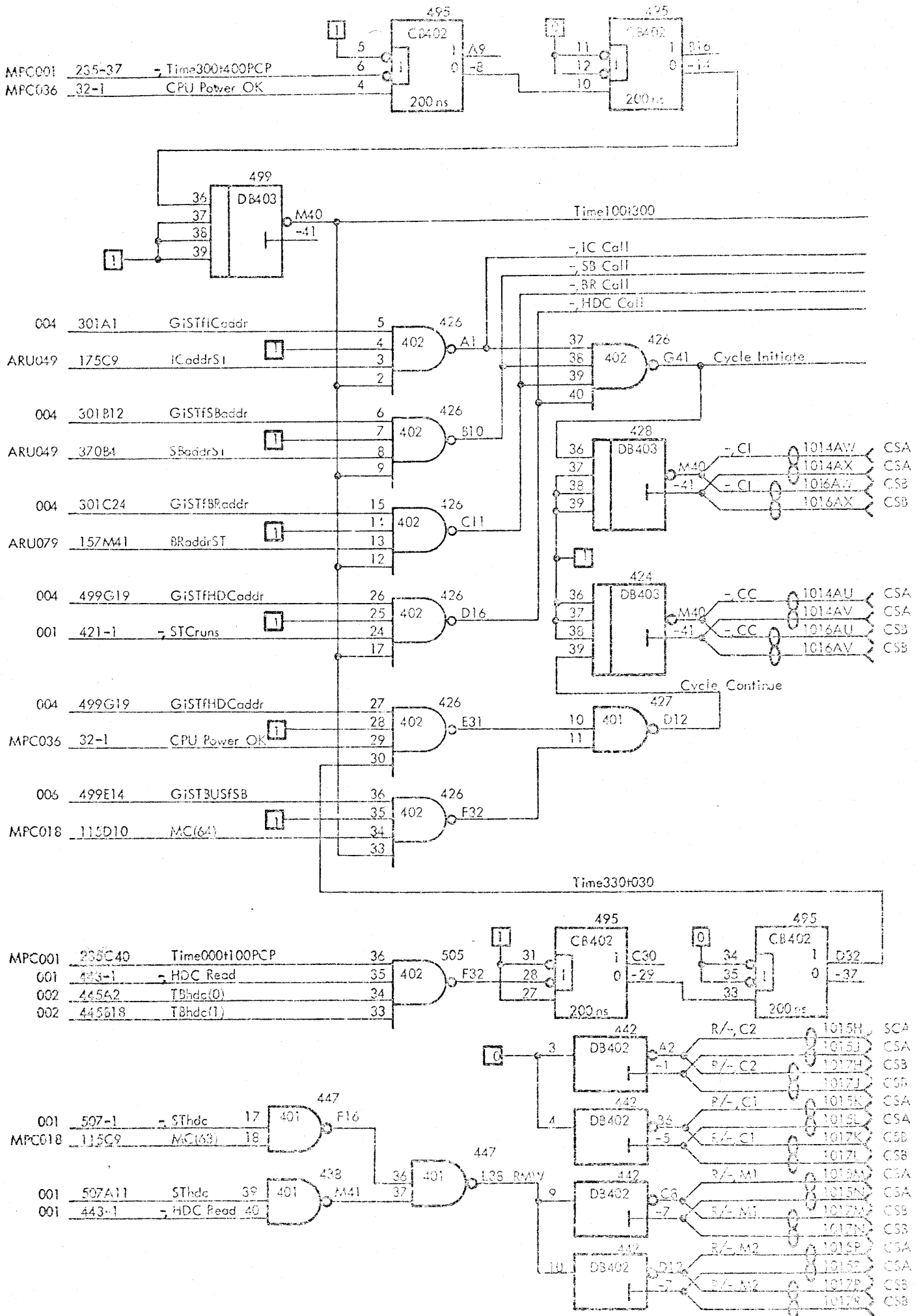


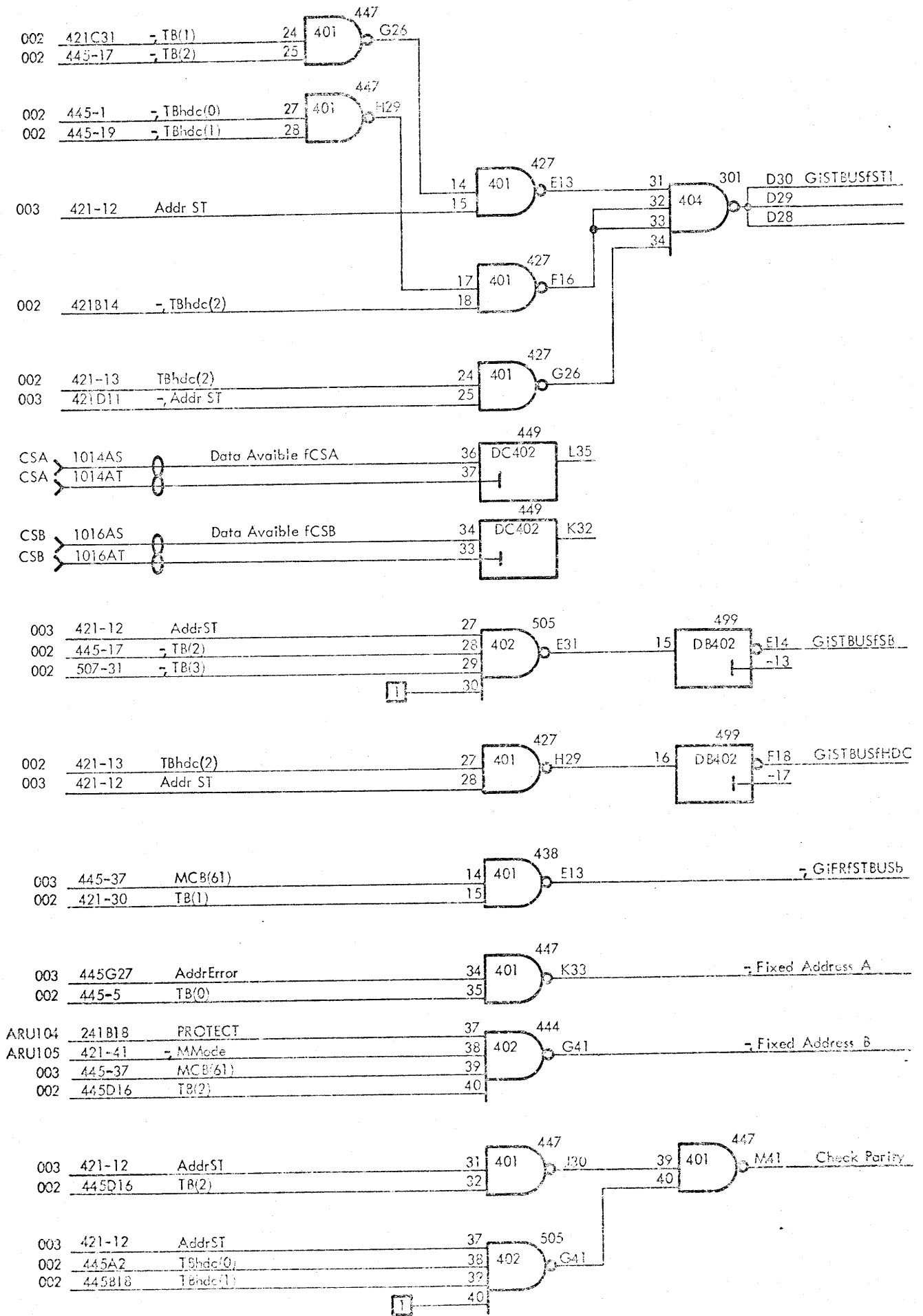


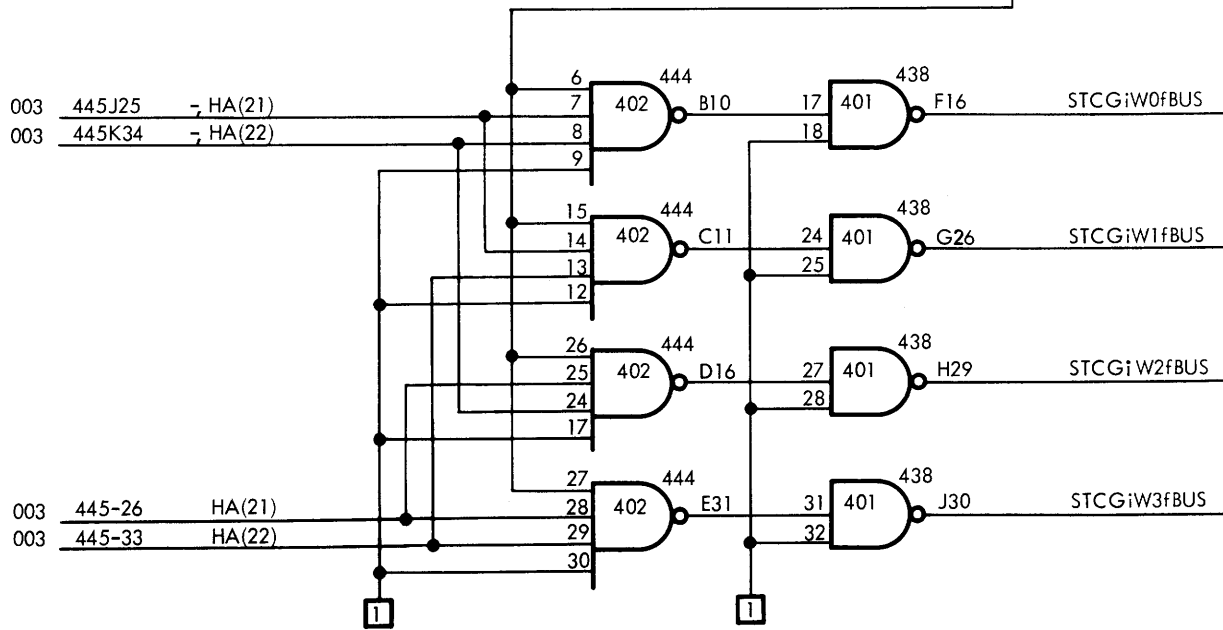
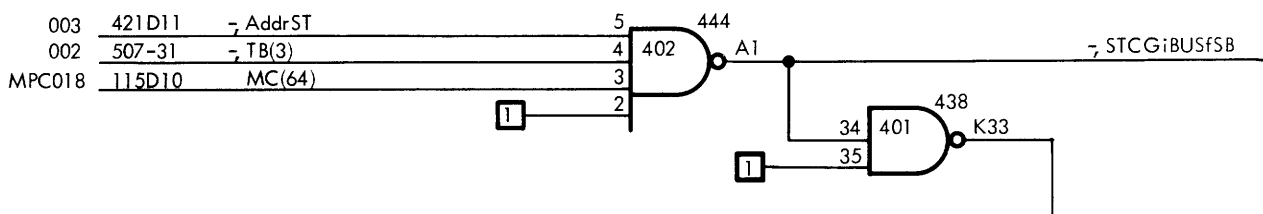
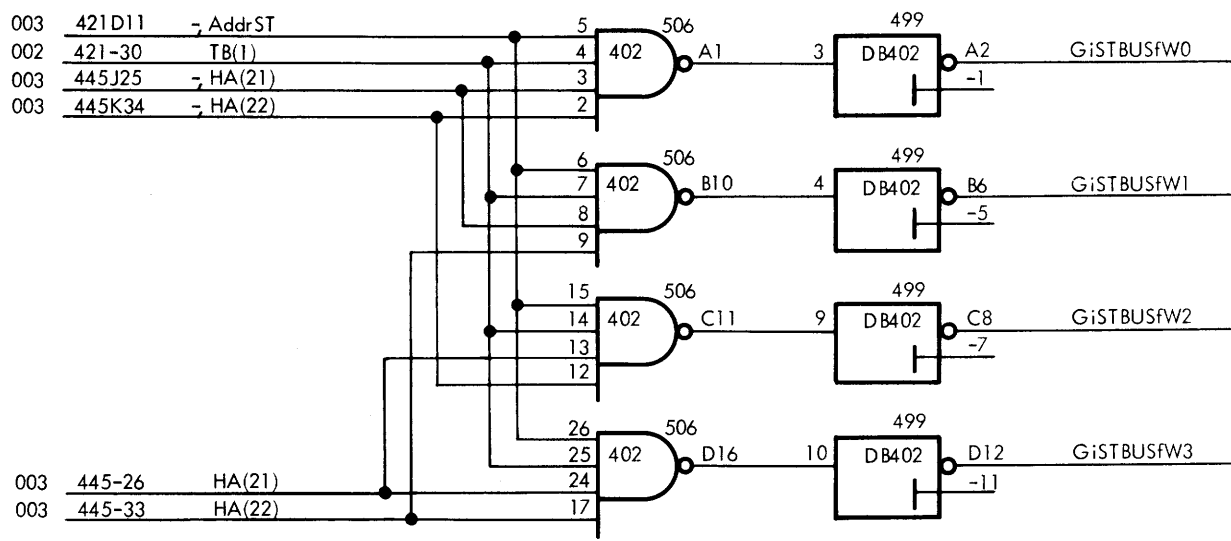
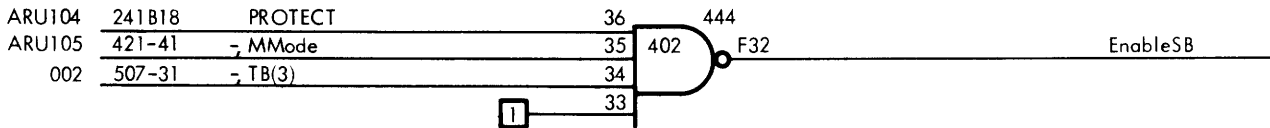


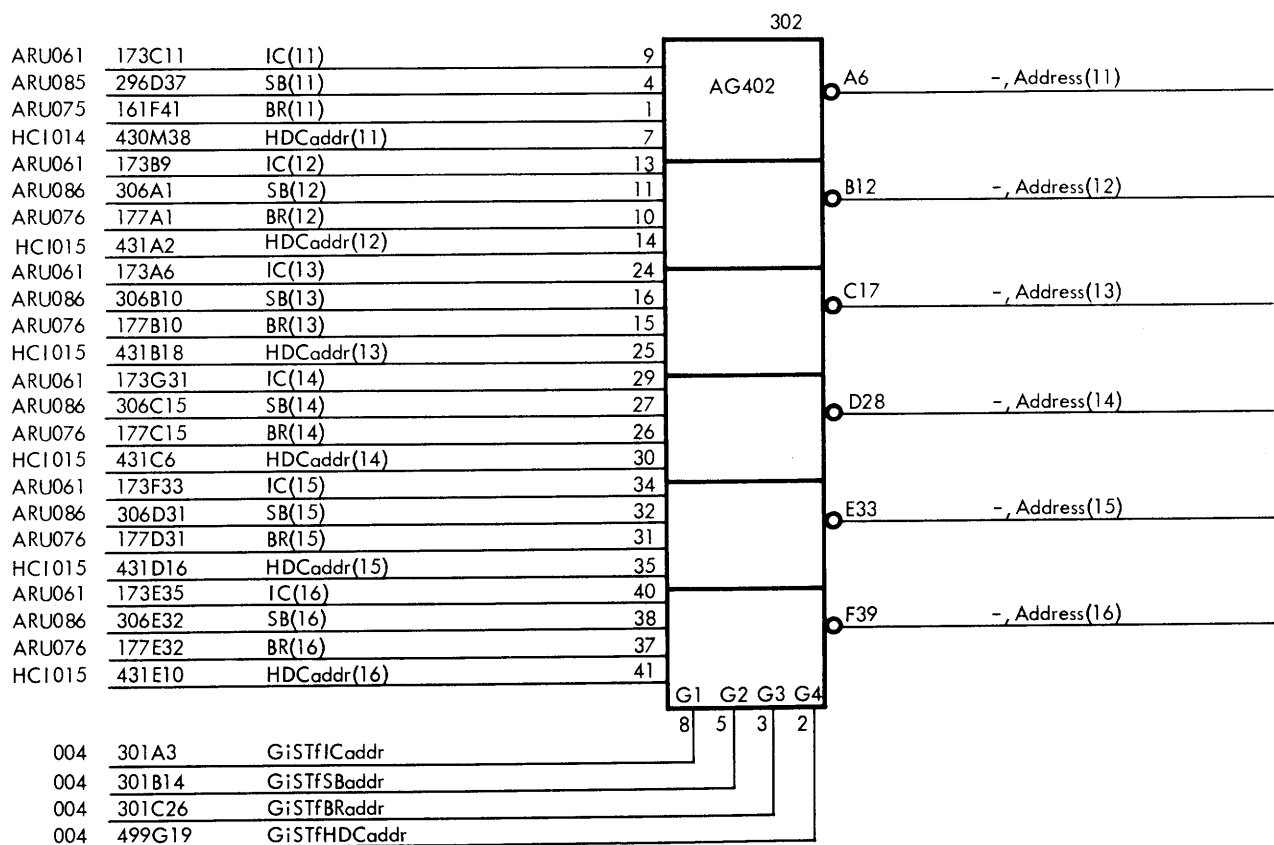
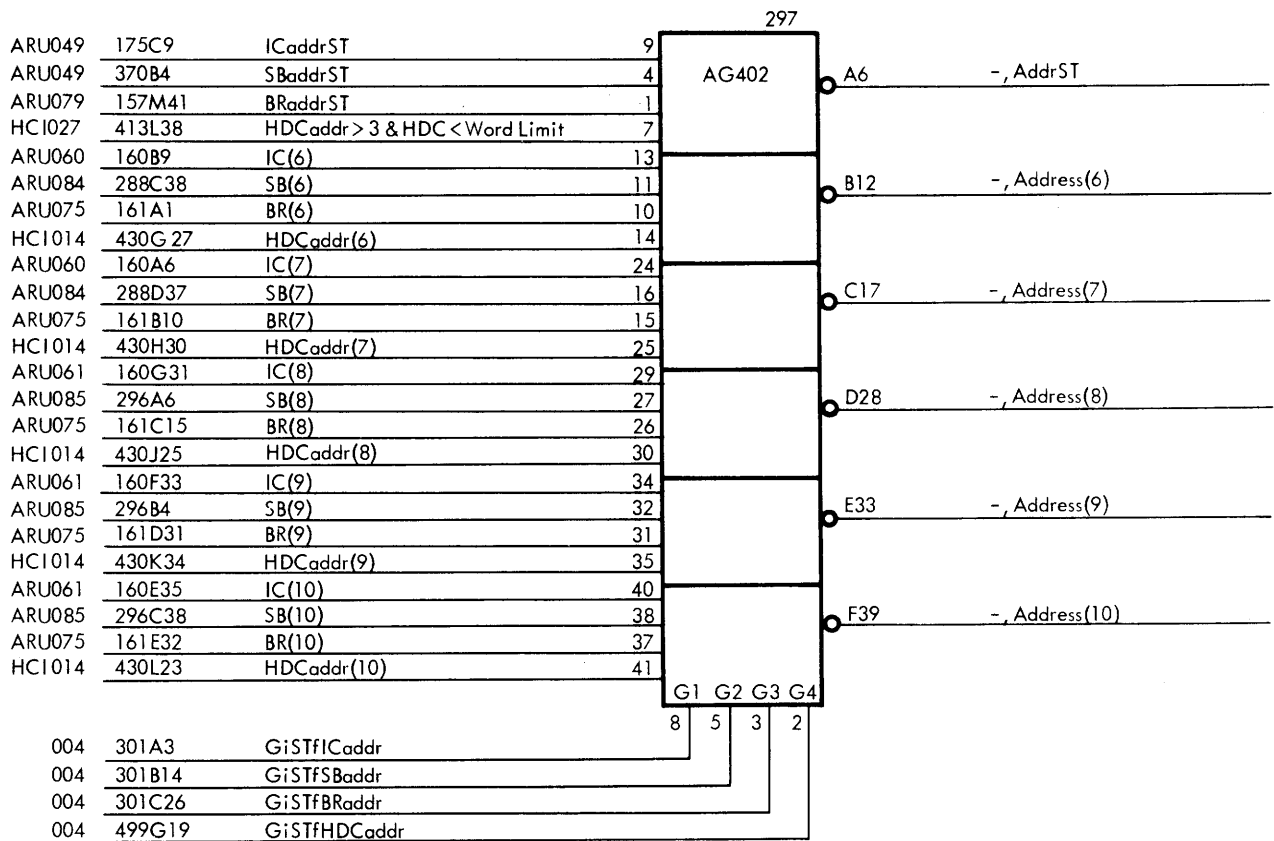


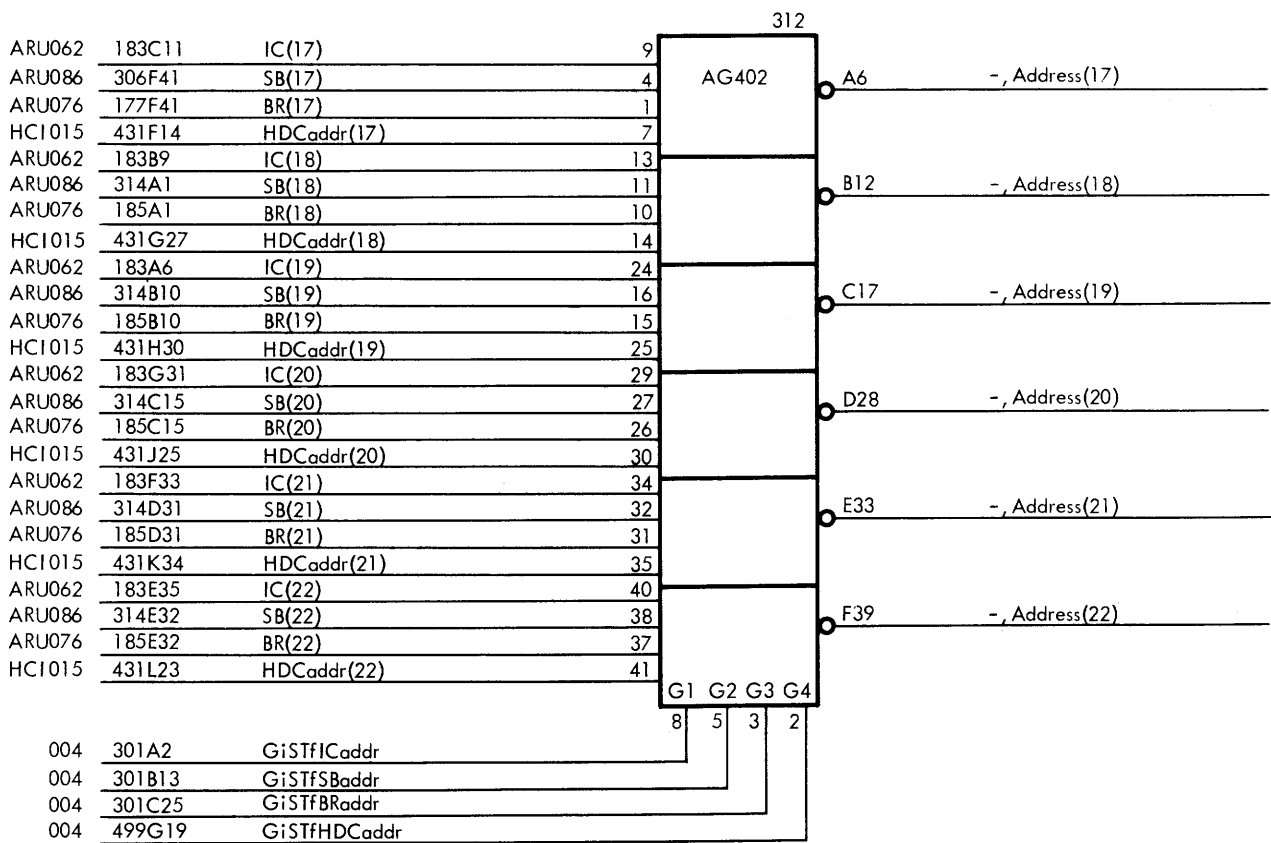


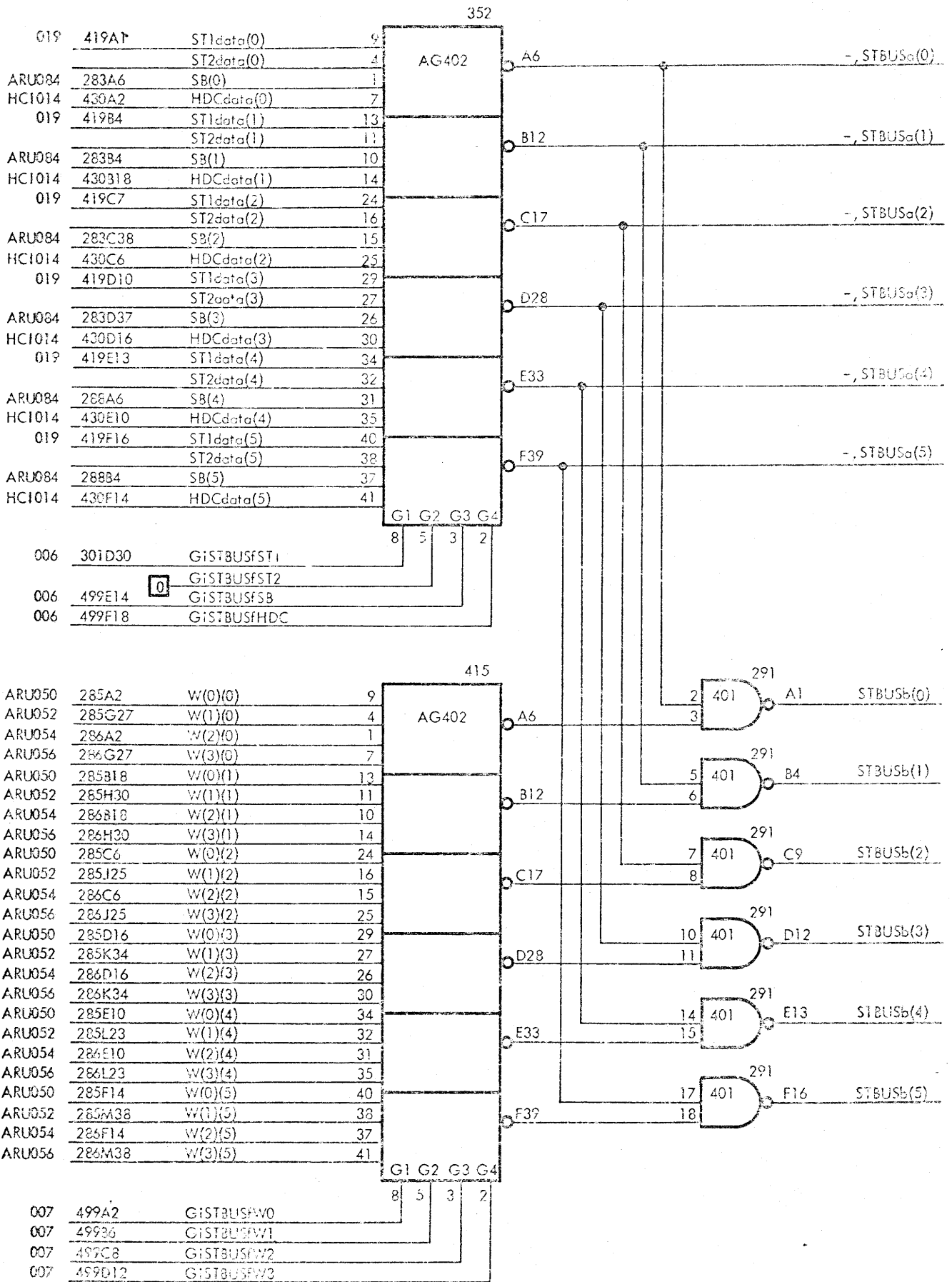


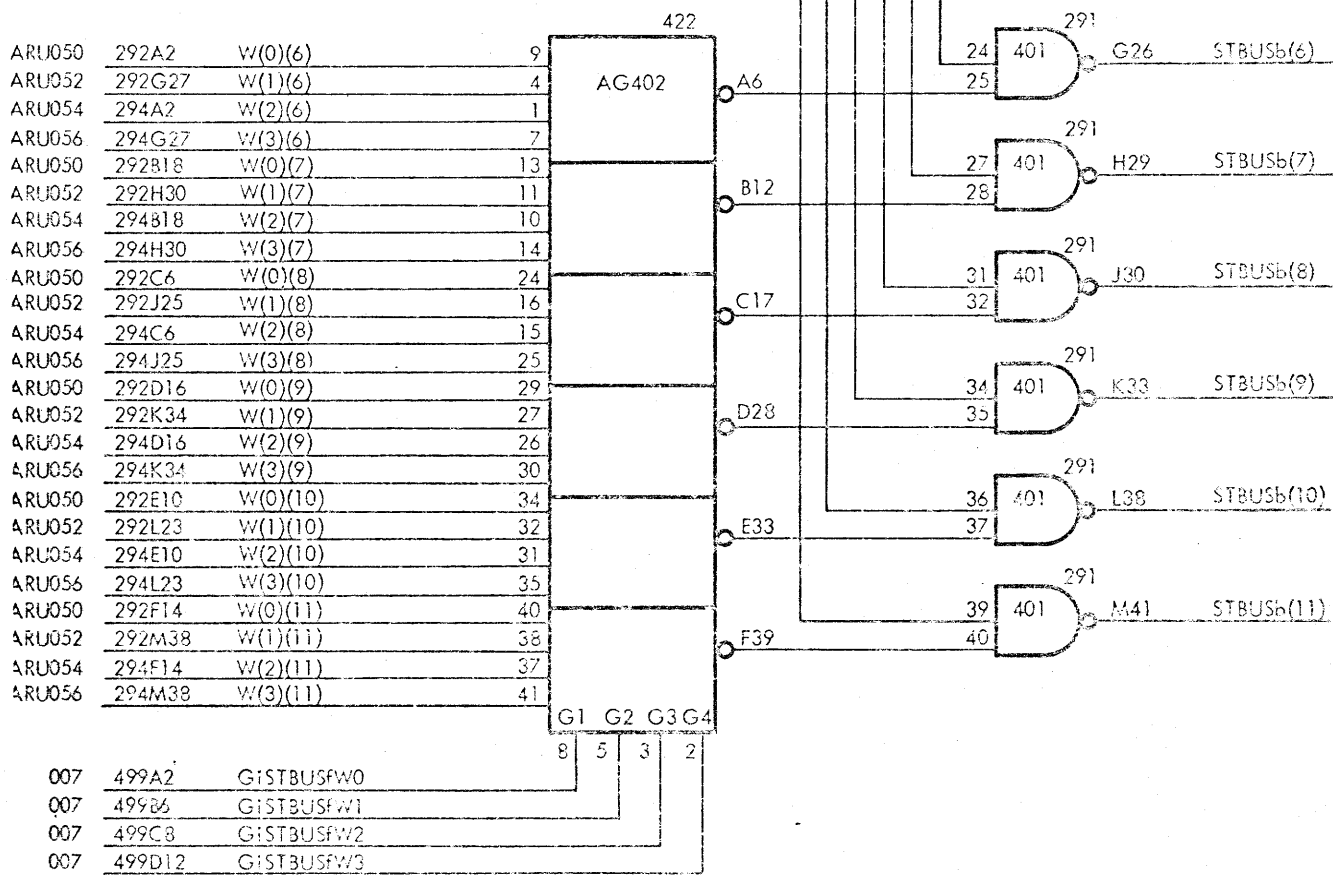
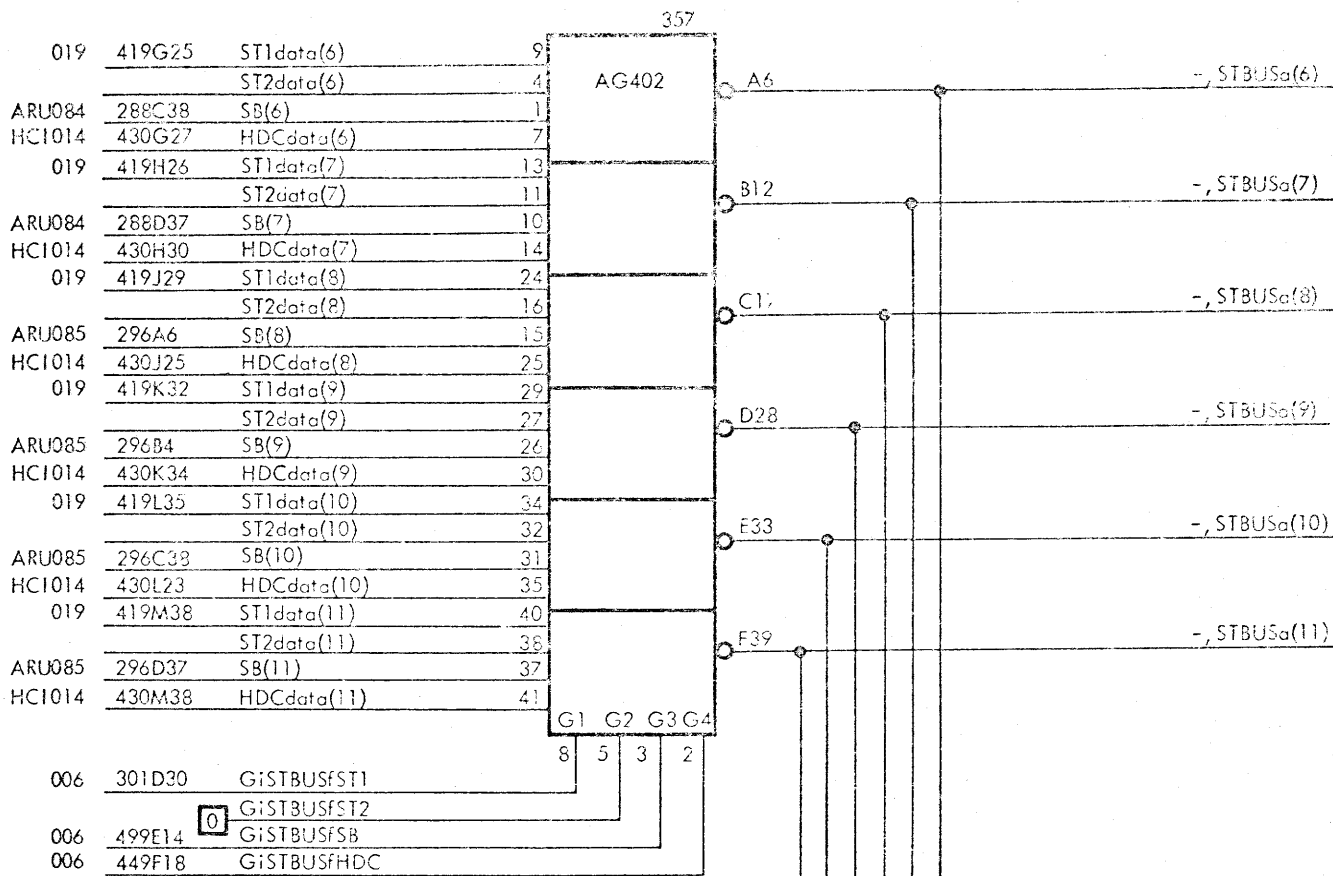


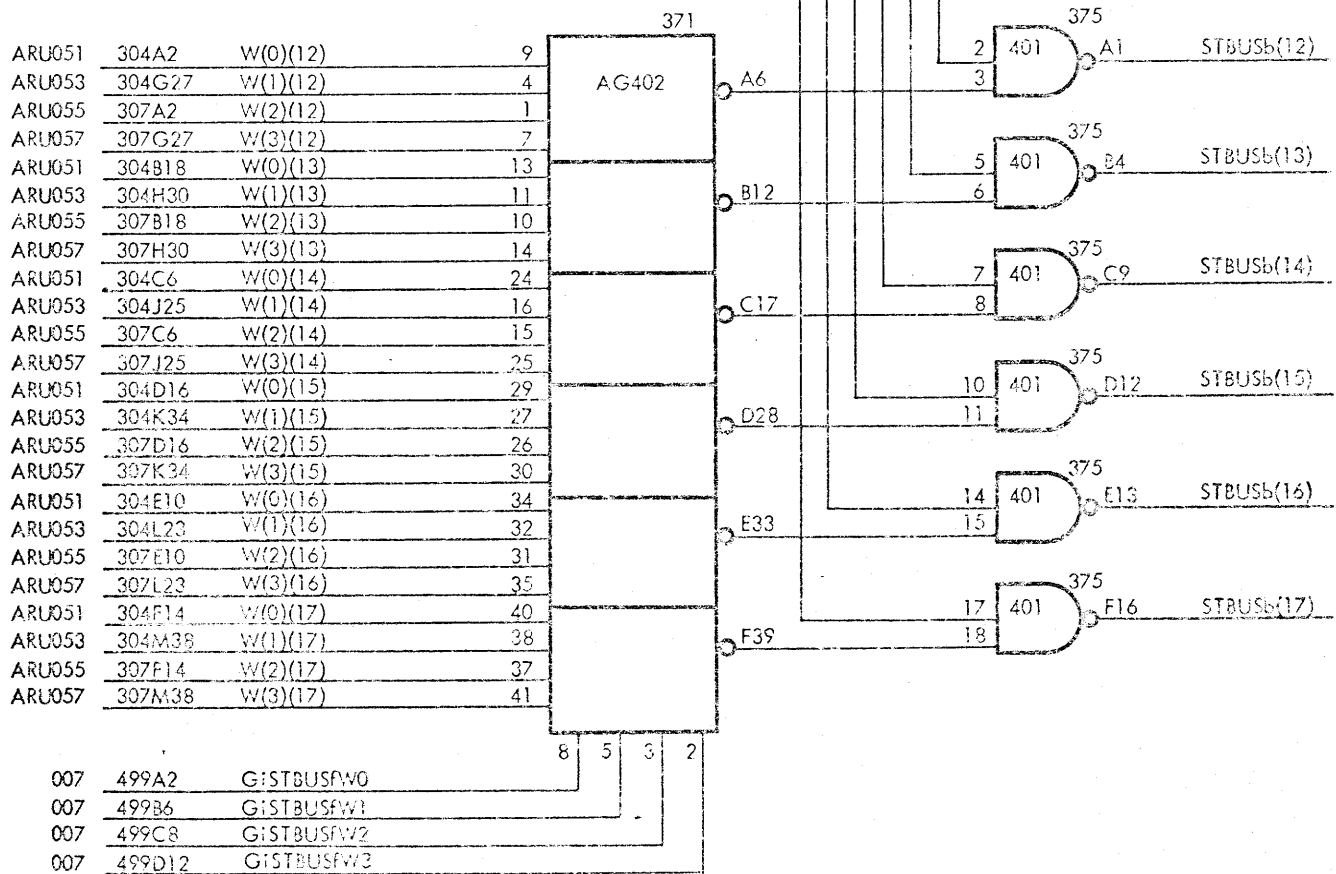
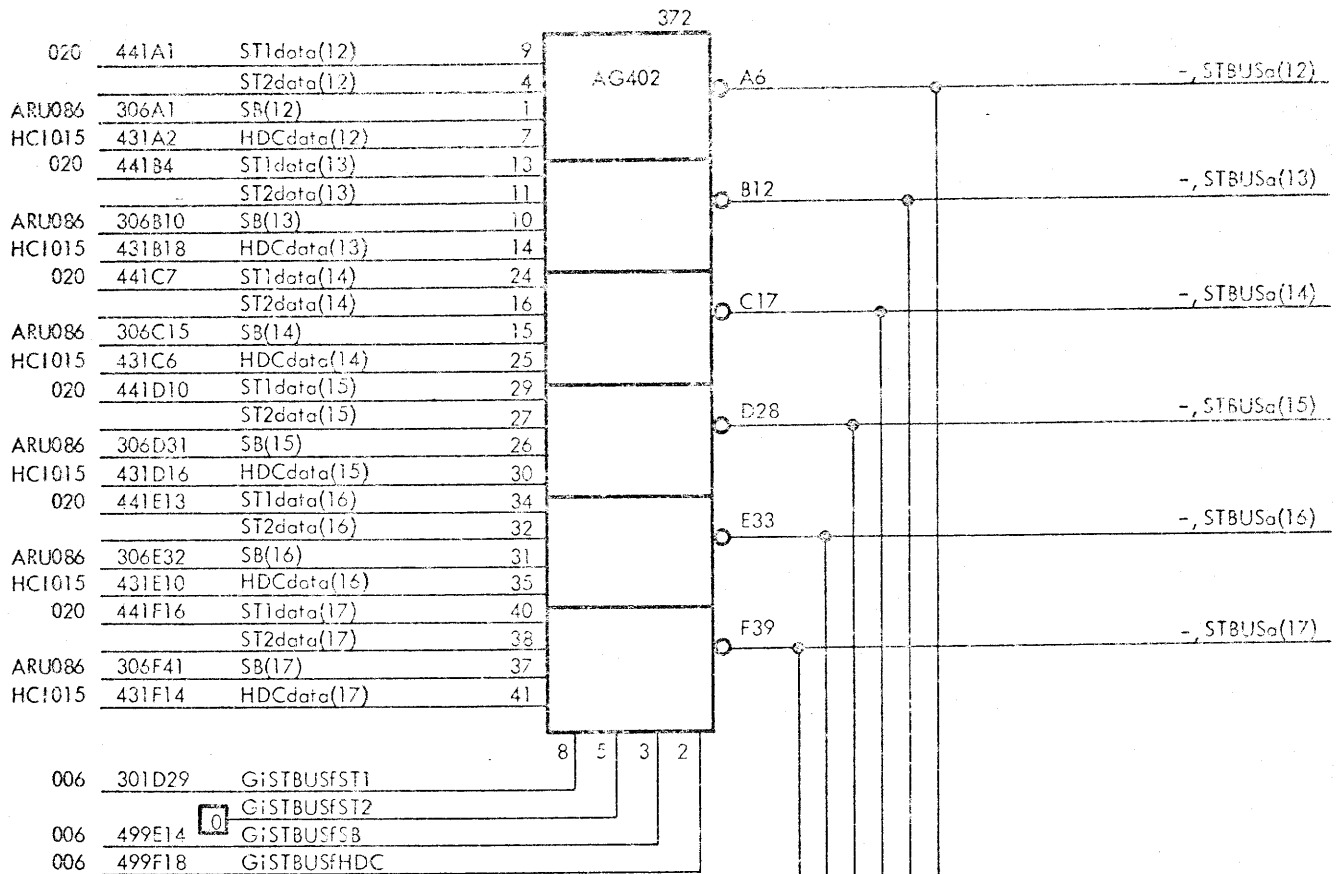


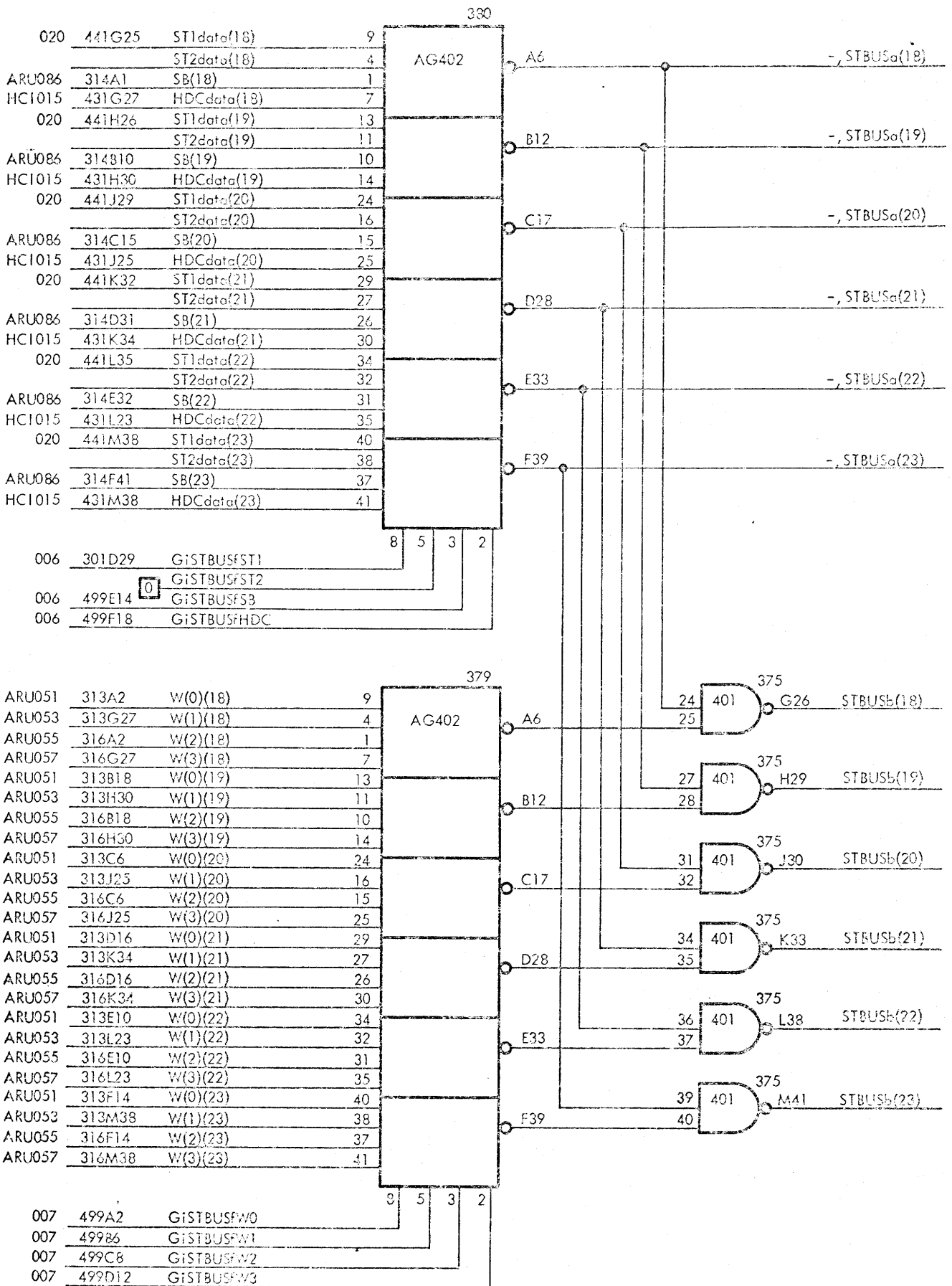


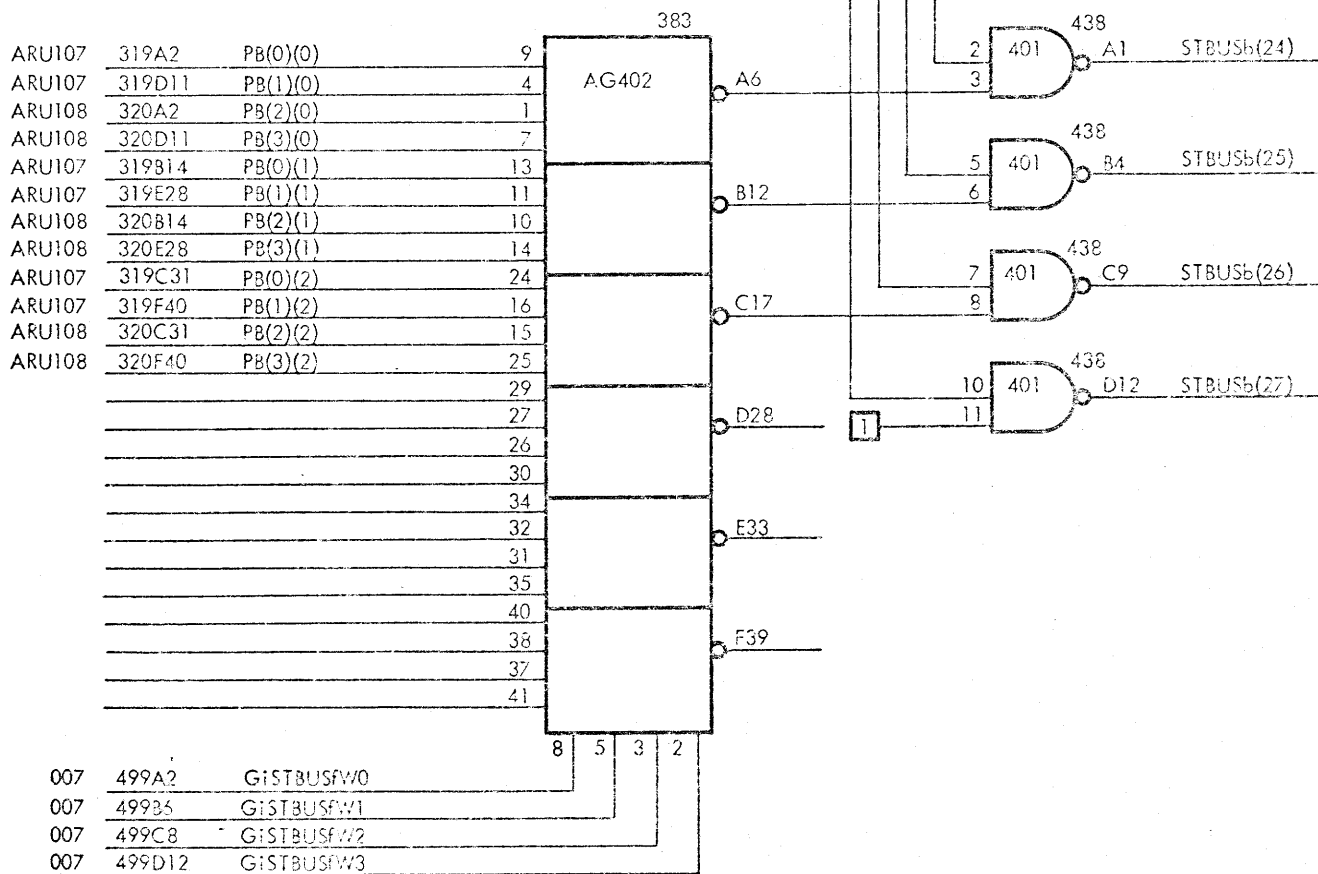
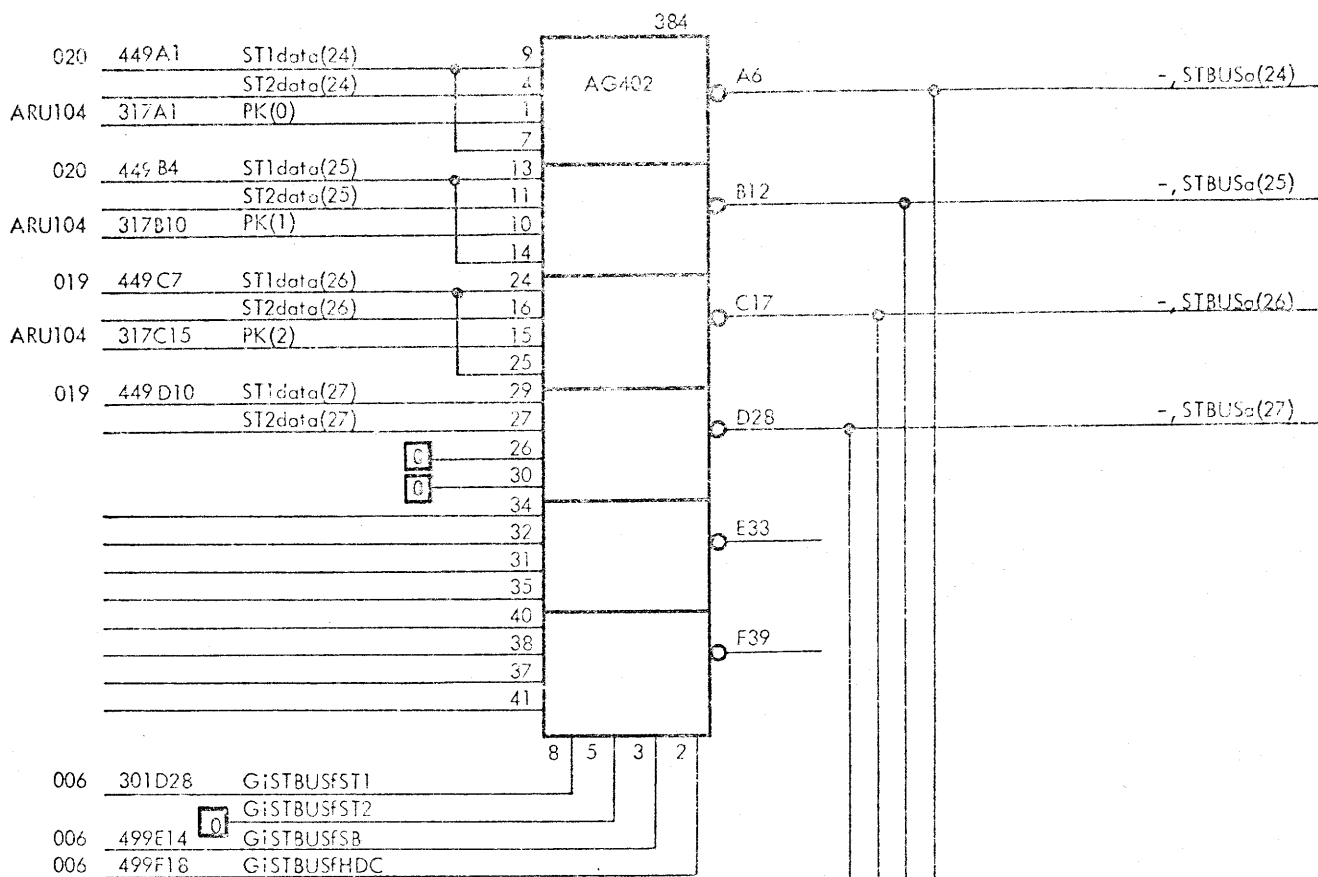


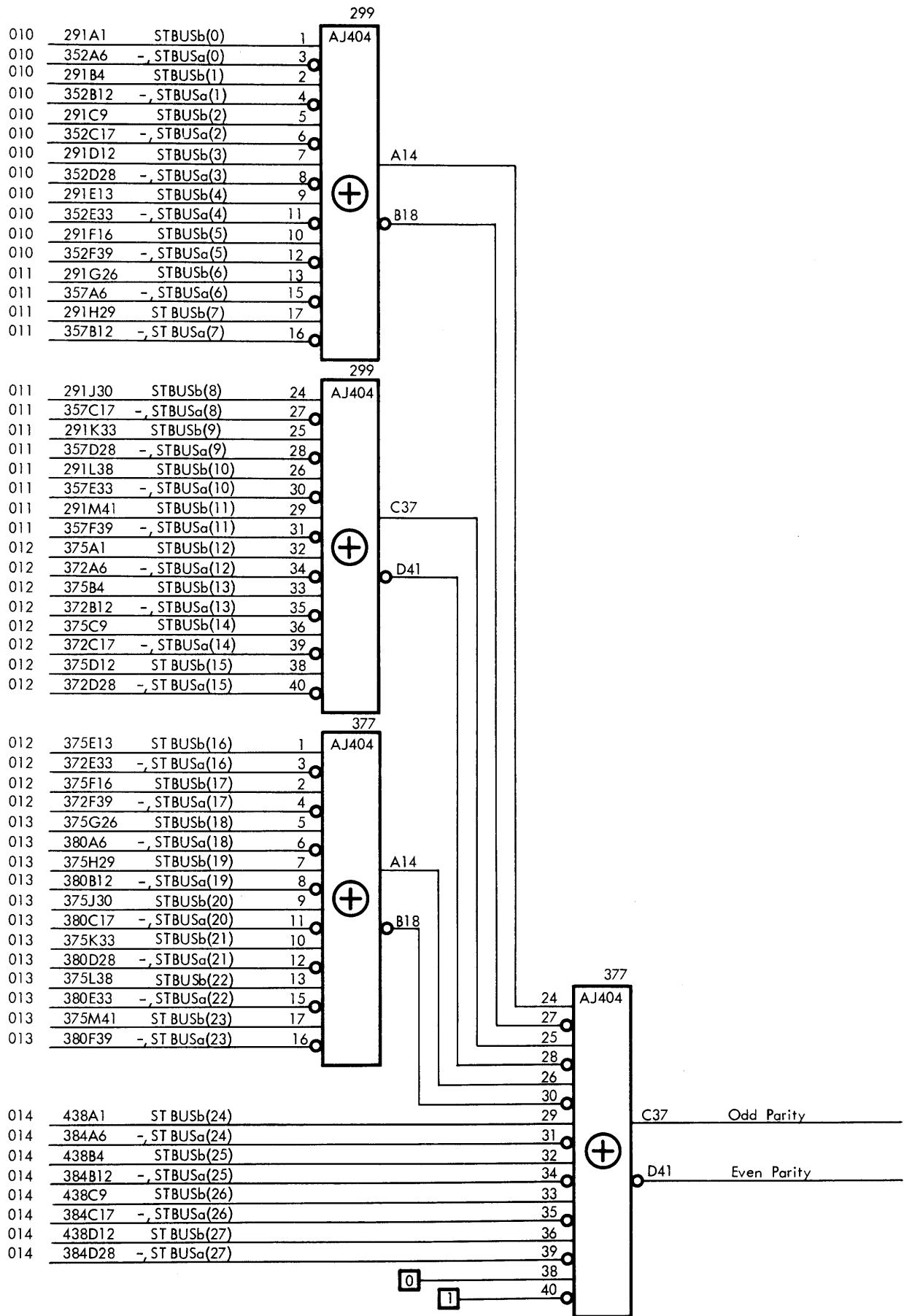


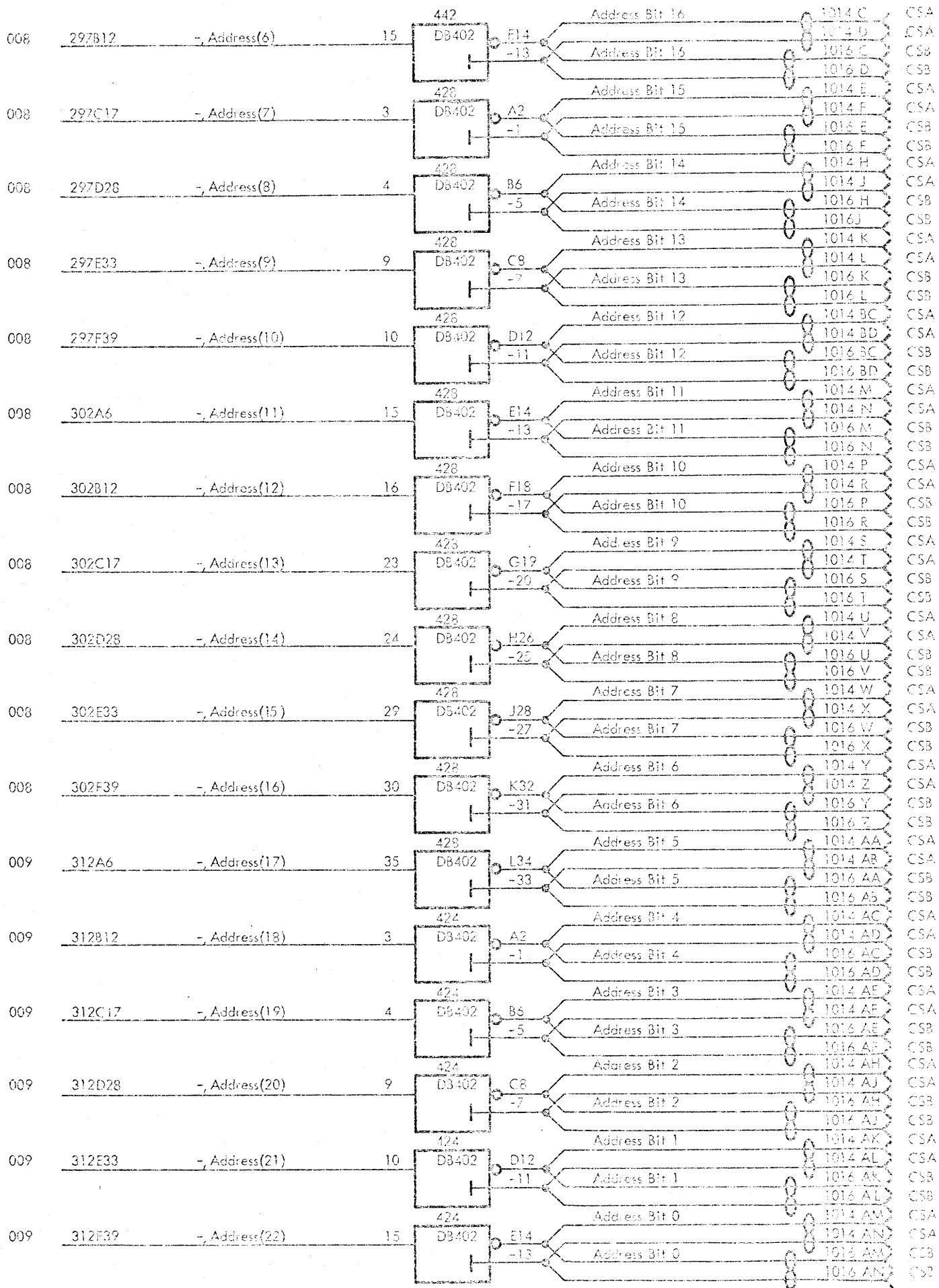


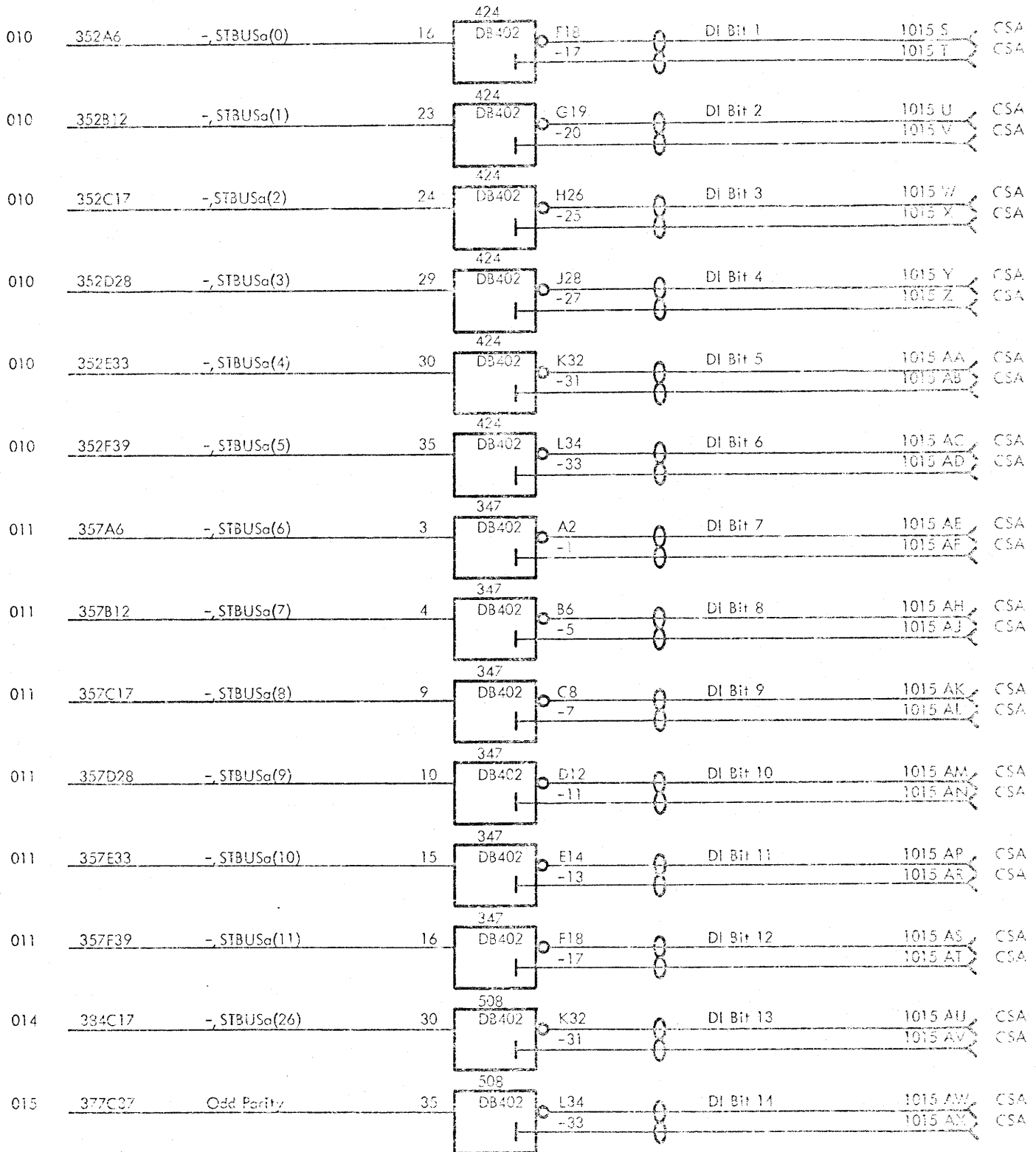


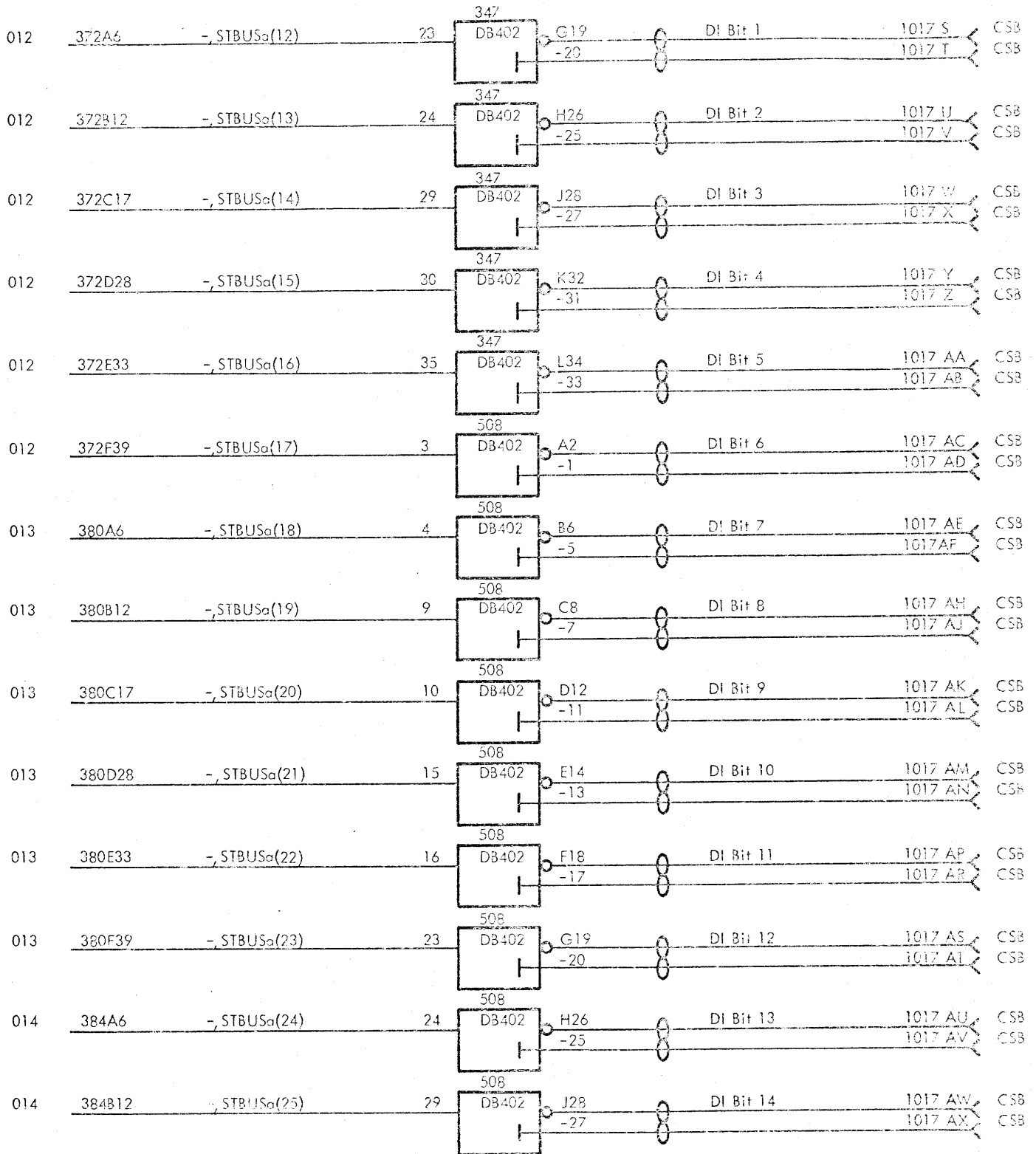


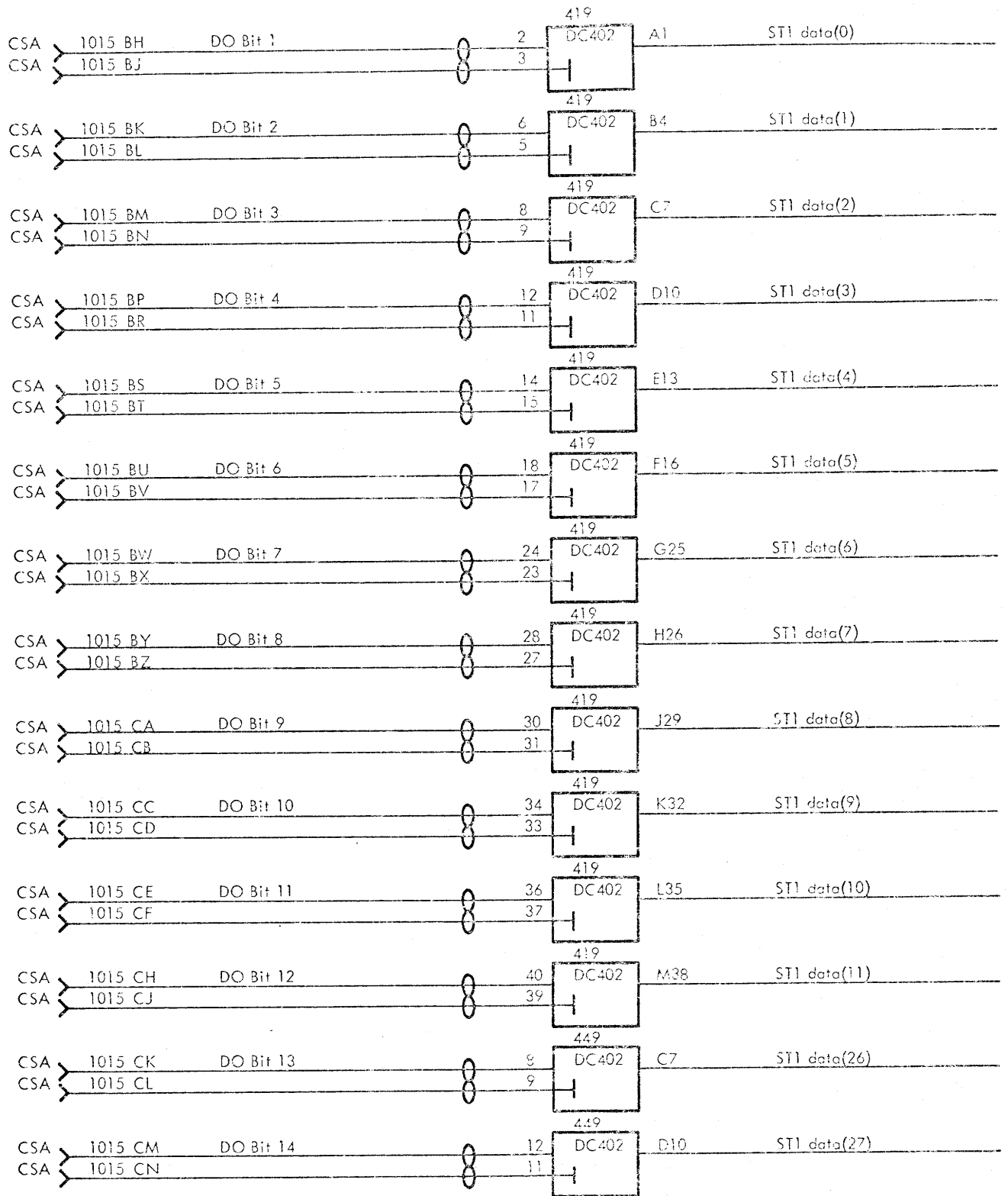


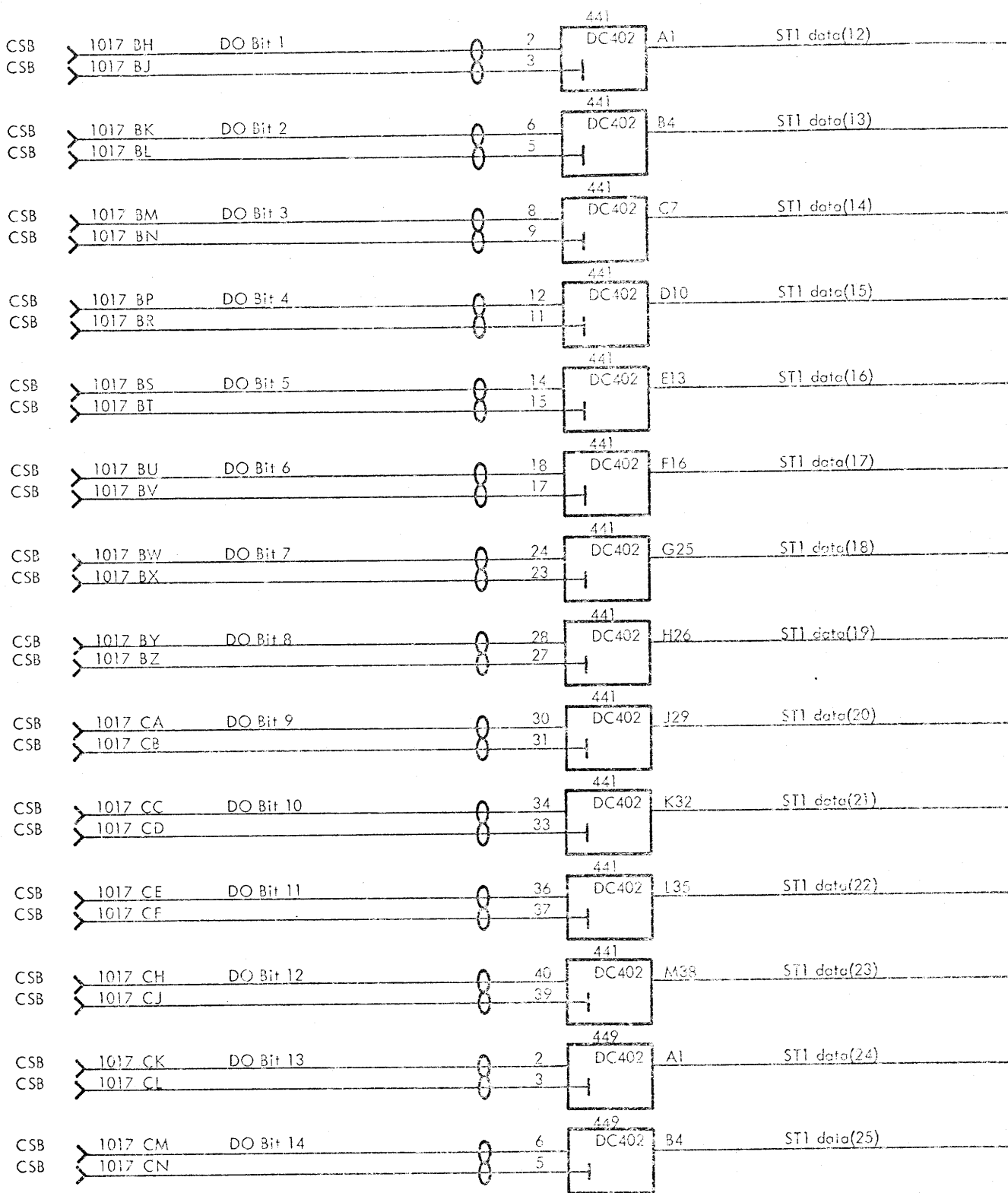


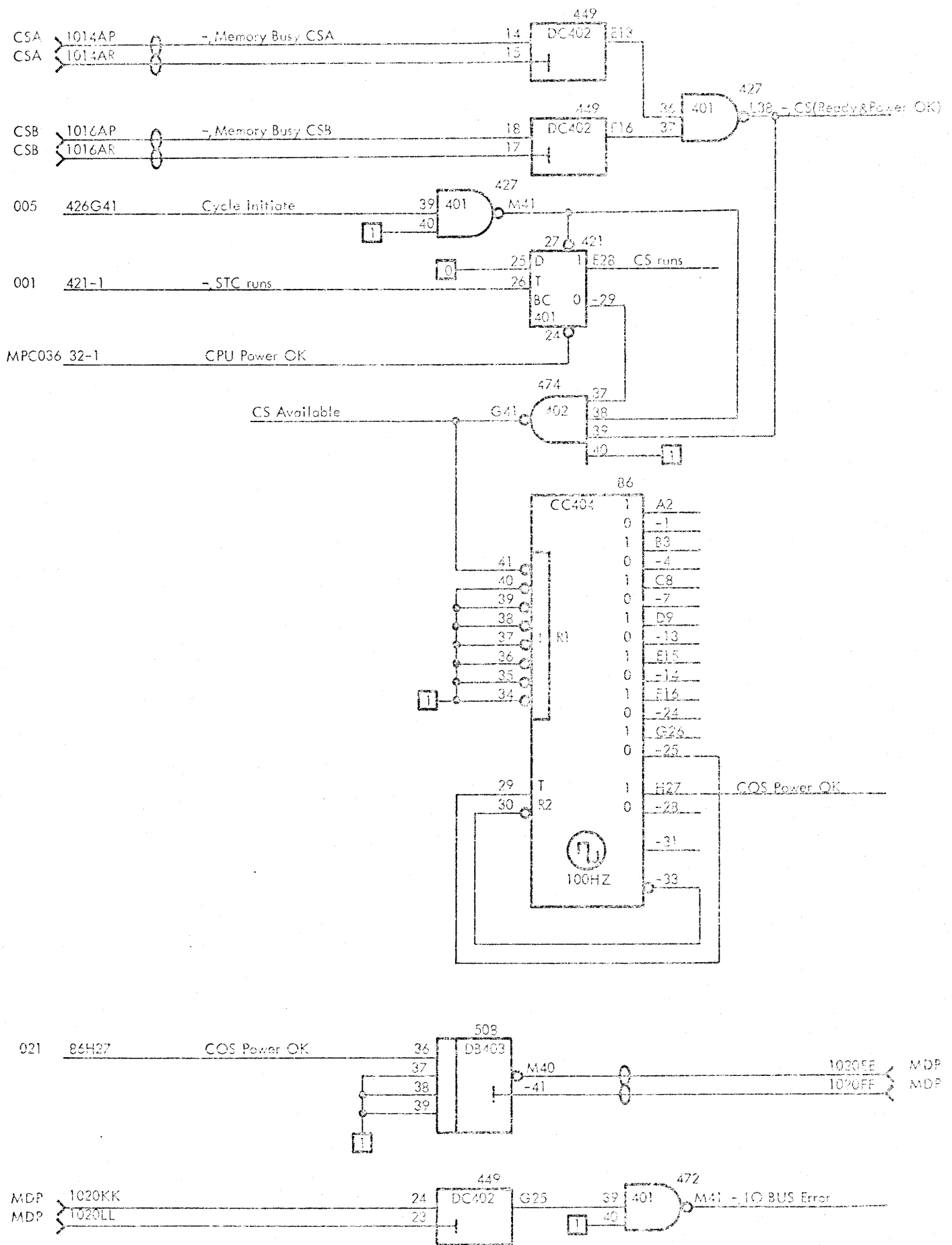










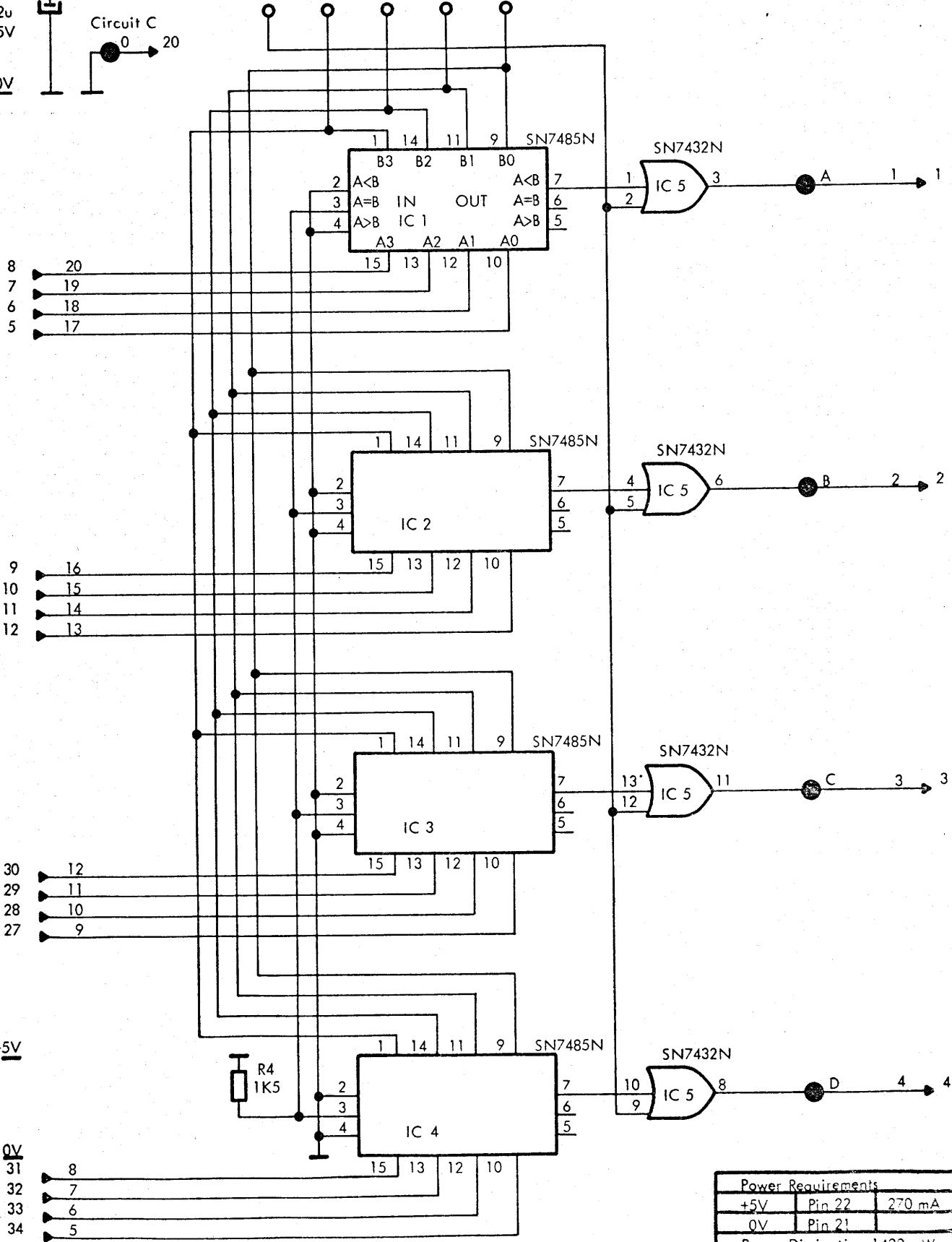
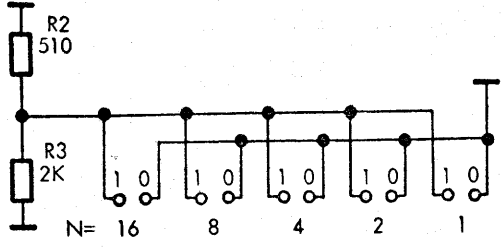
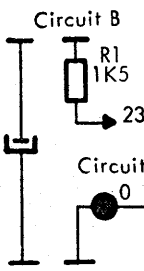


				425				
				AK403				
ARU060	160B9	IC(6)	5	8	A	A<N	A1	IC(6:9)<Word Limit
ARU060	160A6	IC(7)	6	4				
ARU061	160C31	IC(8)	7	2				
ARU061	160F33	IC(9)	8					
ARU084	288C38	SB(6)	9	8	B	B<N	B2	SB(6:9)<Word Limit
ARU084	288D37	SB(7)	10	4				
ARU085	296A6	SB(8)	11	2				
ARU085	296B4	SB(9)	12					
			34	8				
			35	4	C	C<N	C3	
			36	2				
			37					
014	430G27	HDCBF(6)	38	8	D	D<N	D4	HDCBF(6:9)<Word Limit
014	430H30	HDCBF(7)	39	4				
014	430J25	HDCBF(8)	40	2				
014	430K34	HDCBF(9)	41					
				N				
				16 8 4 2 1				

N := number of installed
8 Word Modules

				450				
				AK404				
008	297B12	- Address(6)	2 12	8			} module number	
008	297C17	- Address(7)	3 13	4				
008	297D28	- Address(8)	4 14	2				
008	297E33	- Address(9)	5 15	1				
008	297F39	- Address(10)	6 16	4k				
008	302A6	- Address(11)	7 17	2k				
008	302B12	- Address(12)	8 18	1k				
008	302C17	- Address(13)	9 19	512				
008	302D28	- Address(14)	10 20	256				
008	302E33	- Address(15)	11 21	128				
008	302F39	- Address(16)	12 22	64				
009	312A6	- Address(17)	13 23	32				
009	312B12	- Address(18)	14 24	16				
009	312C17	- Address(19)	15 25	8				
009	312D28	- Address(20)	16 26	4				
009	312E33	- Address(21)	17 27	2				
009	312F39	- Address(22)	18 28	1				
005	426D16	- HDC Call	5 9					Cycle Stealing
005	426A1	- IC Call	3 5					
005	426B10	- SB Call	4 6					
005	426C11	- BR Call	5 7					
MPC032	443-12	- Core Store Parity Error	6 40					Enable Register Control

+5V
0V
+5V
0V
C1
22u
15V
0V



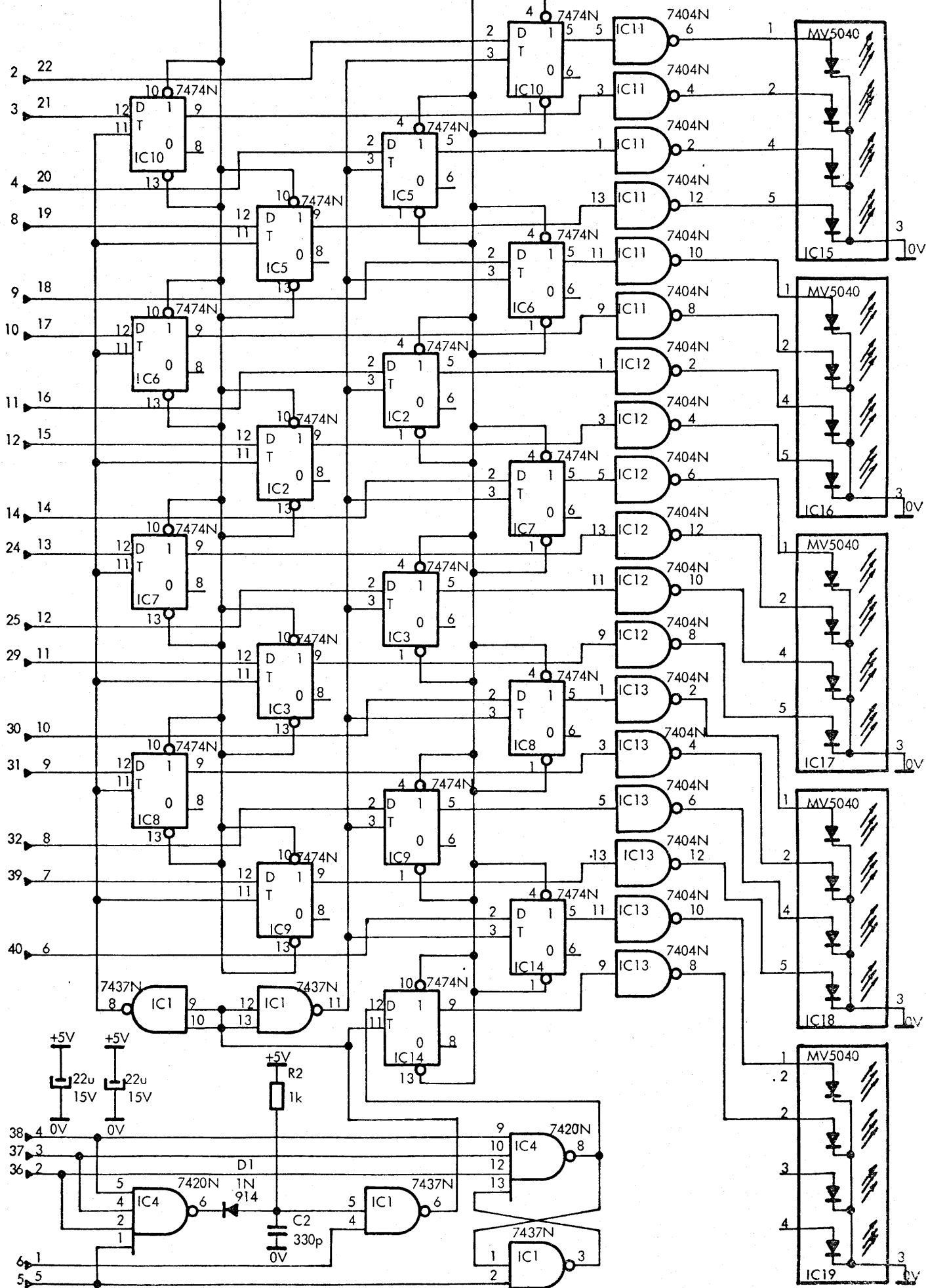
061172 PEP 7301 03 BA

+5V
0V
31
32
33
34

Power Requirements		
+5V	Pin 22	270 mA
0V	Pin 21	
Power Dissipation 1420 mW		

+5V R1 1k5

Circuit A



090173BA
151272AL
010572PEP

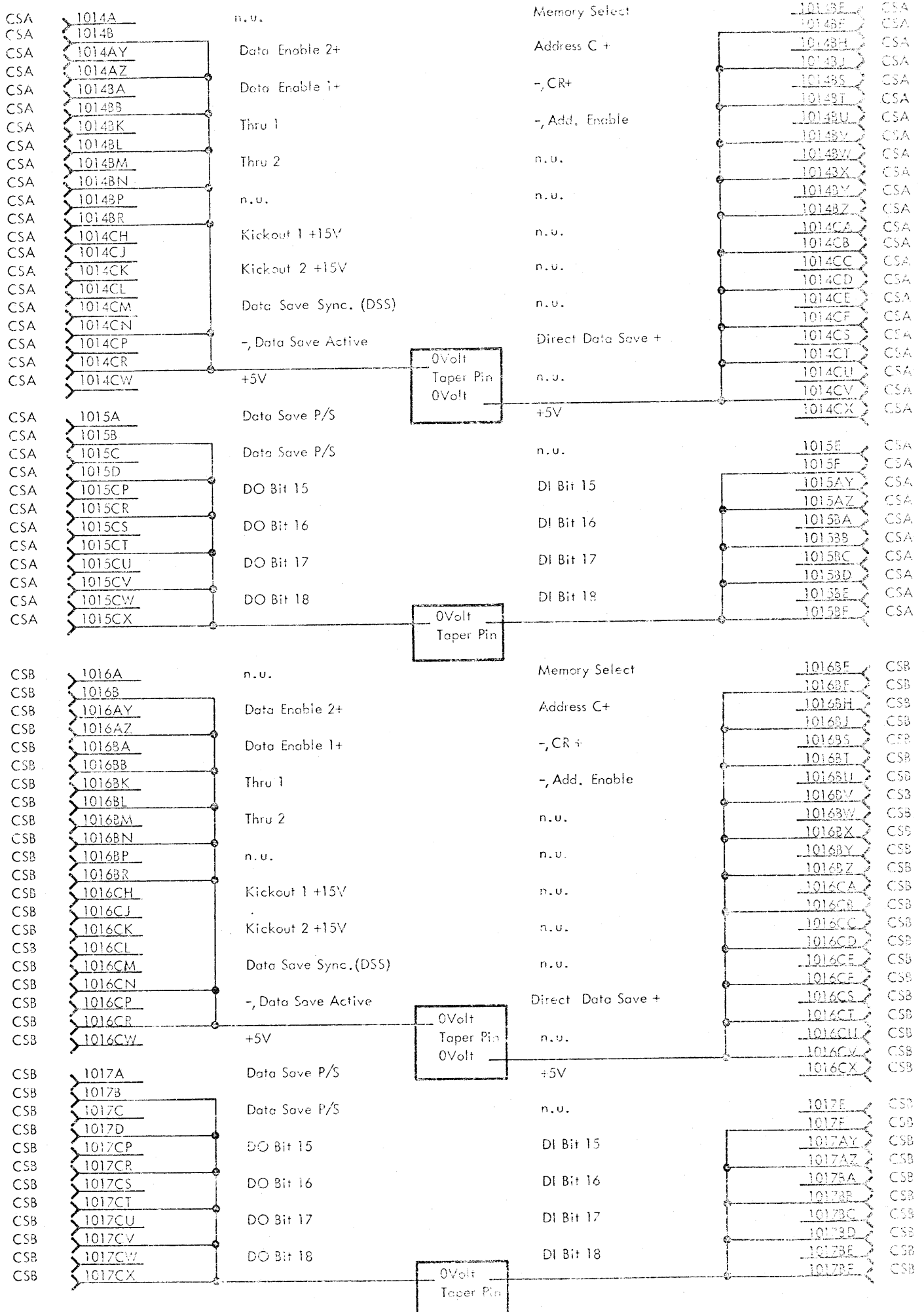
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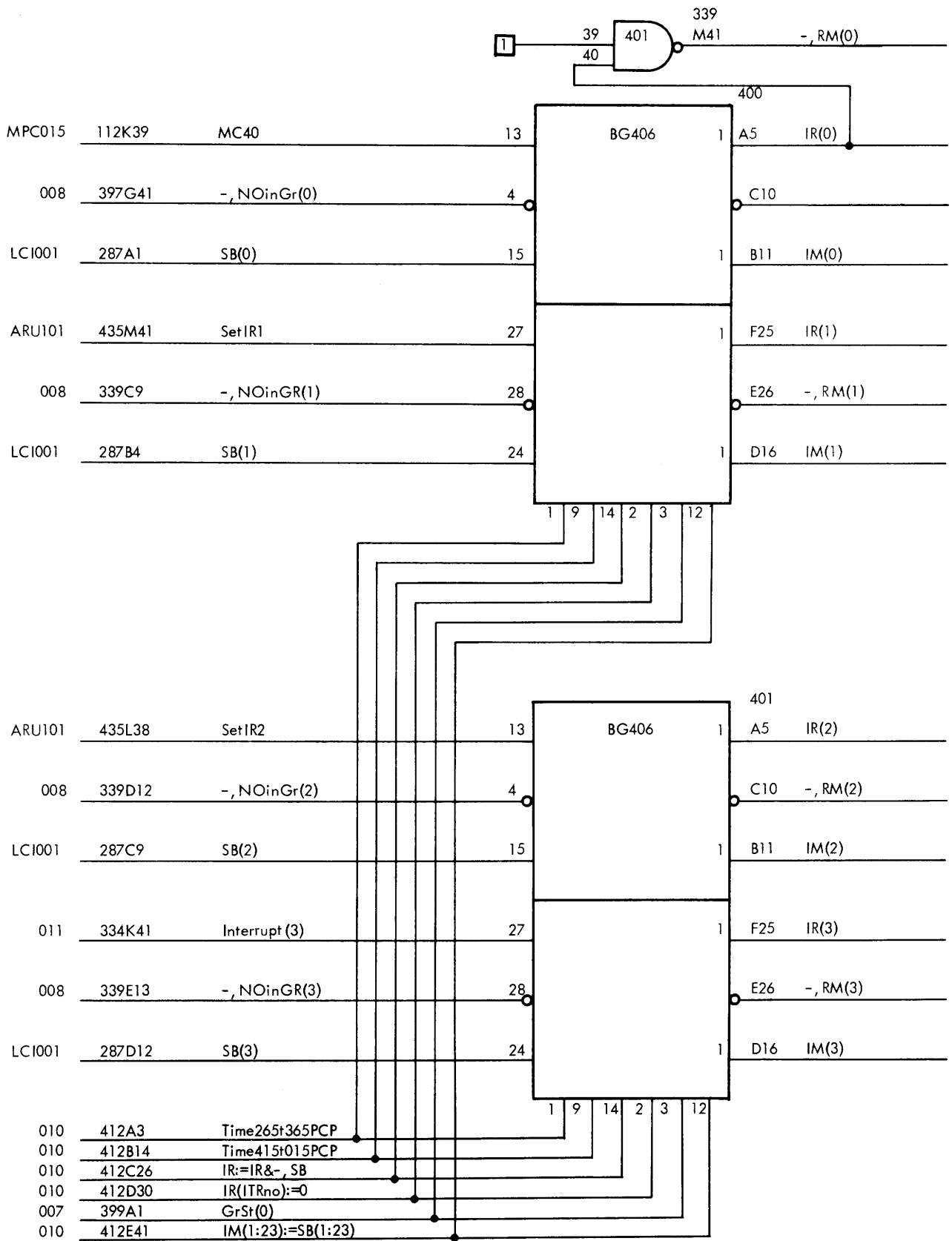
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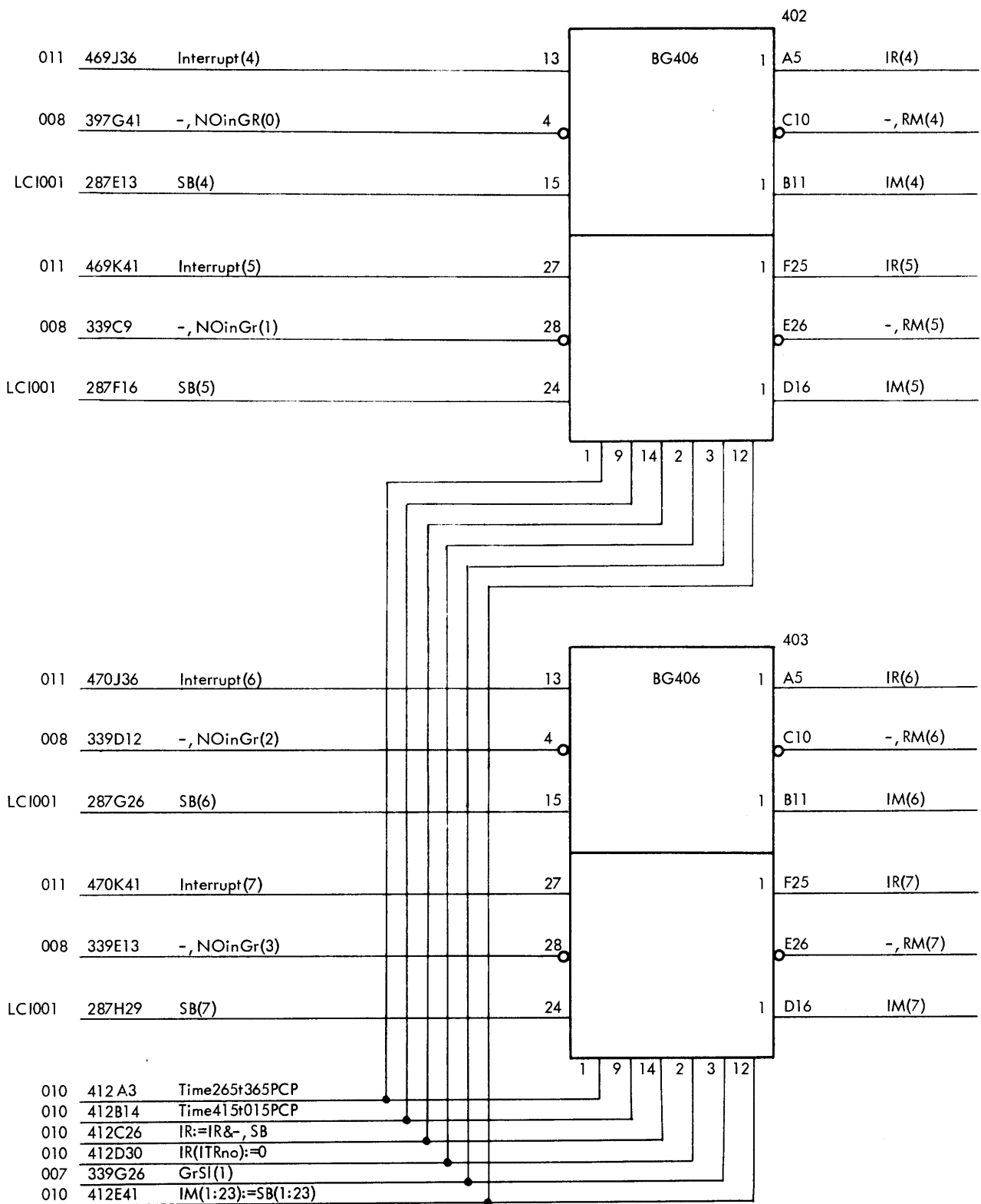
RC2073 - 1

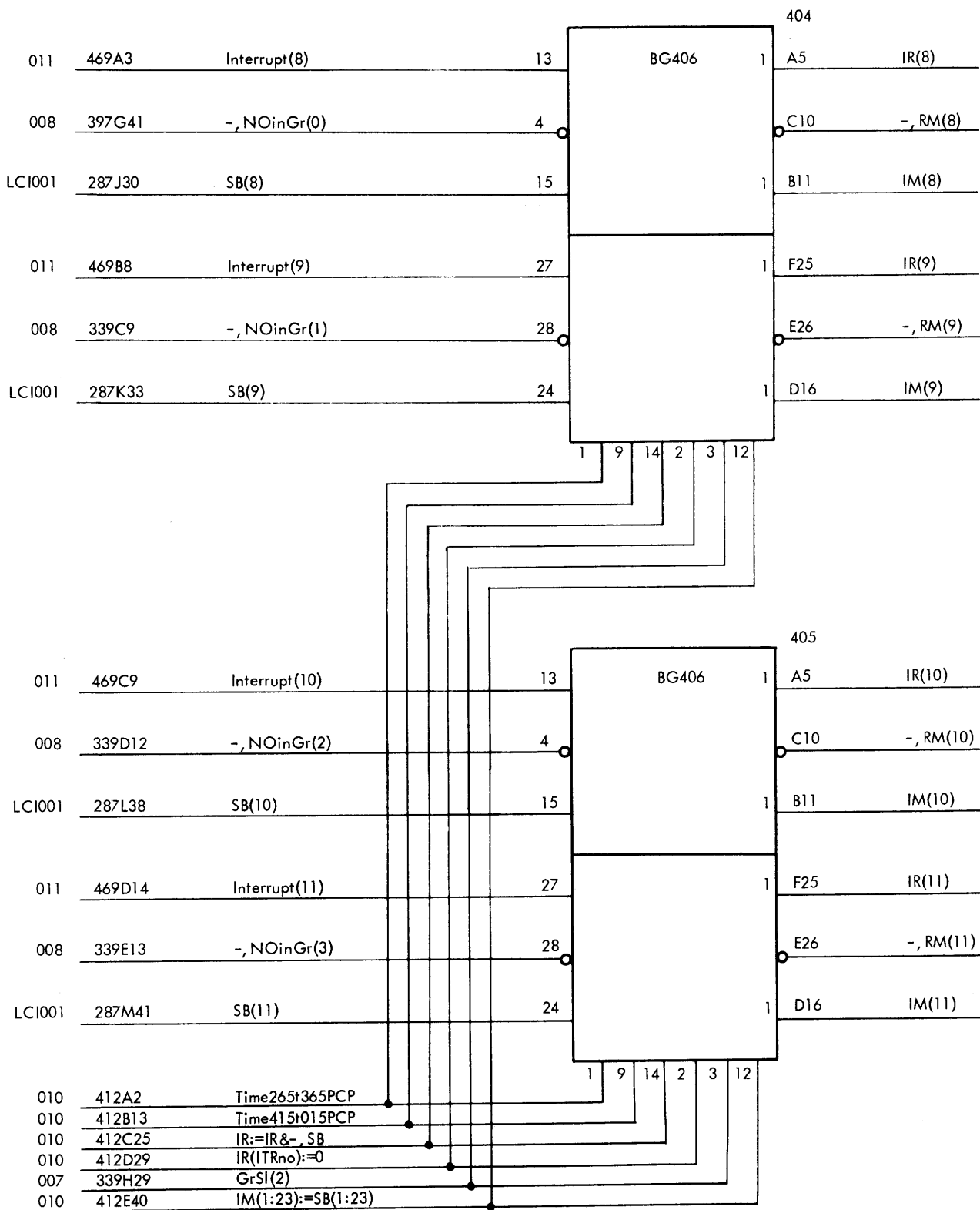
V13572

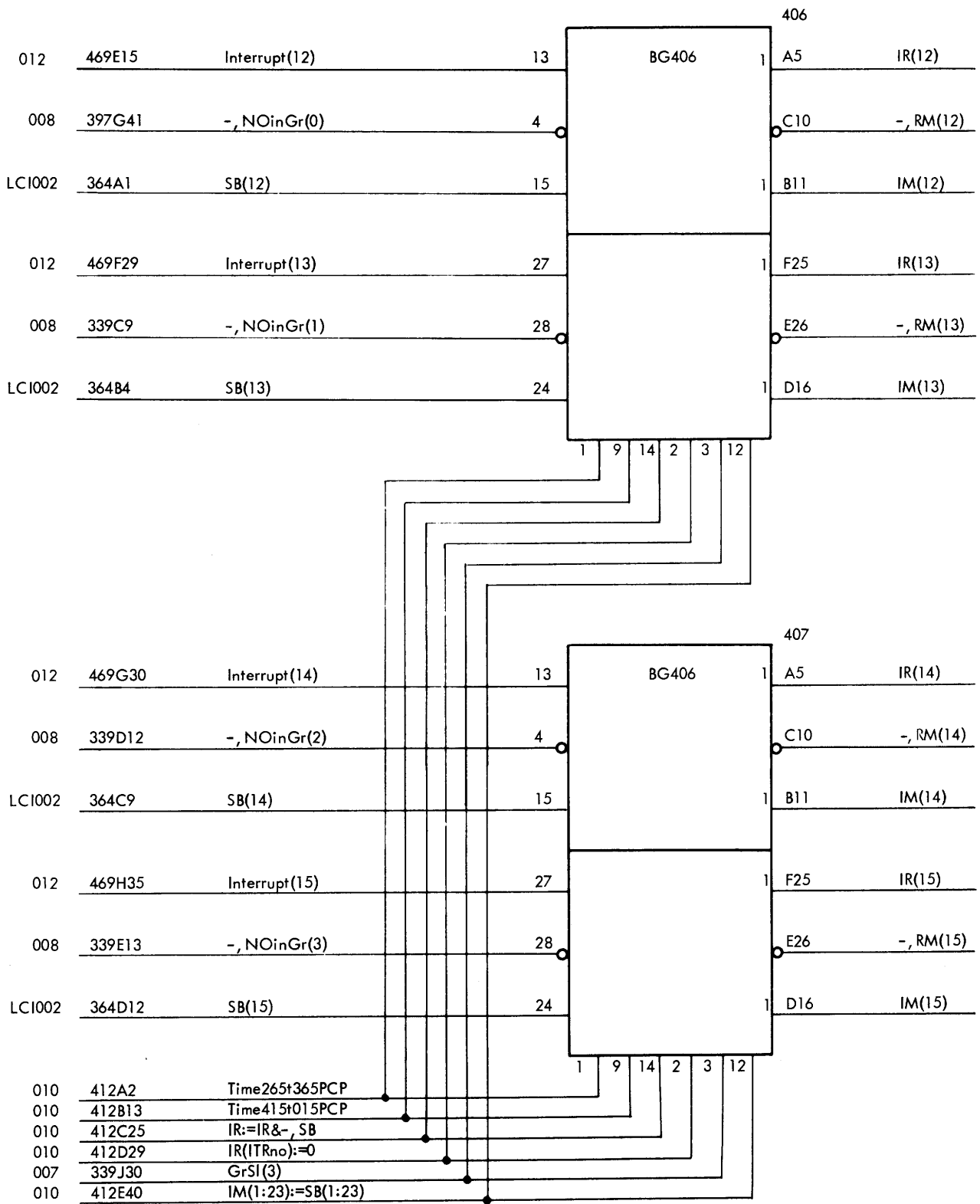
PCBA Circuit Diagram

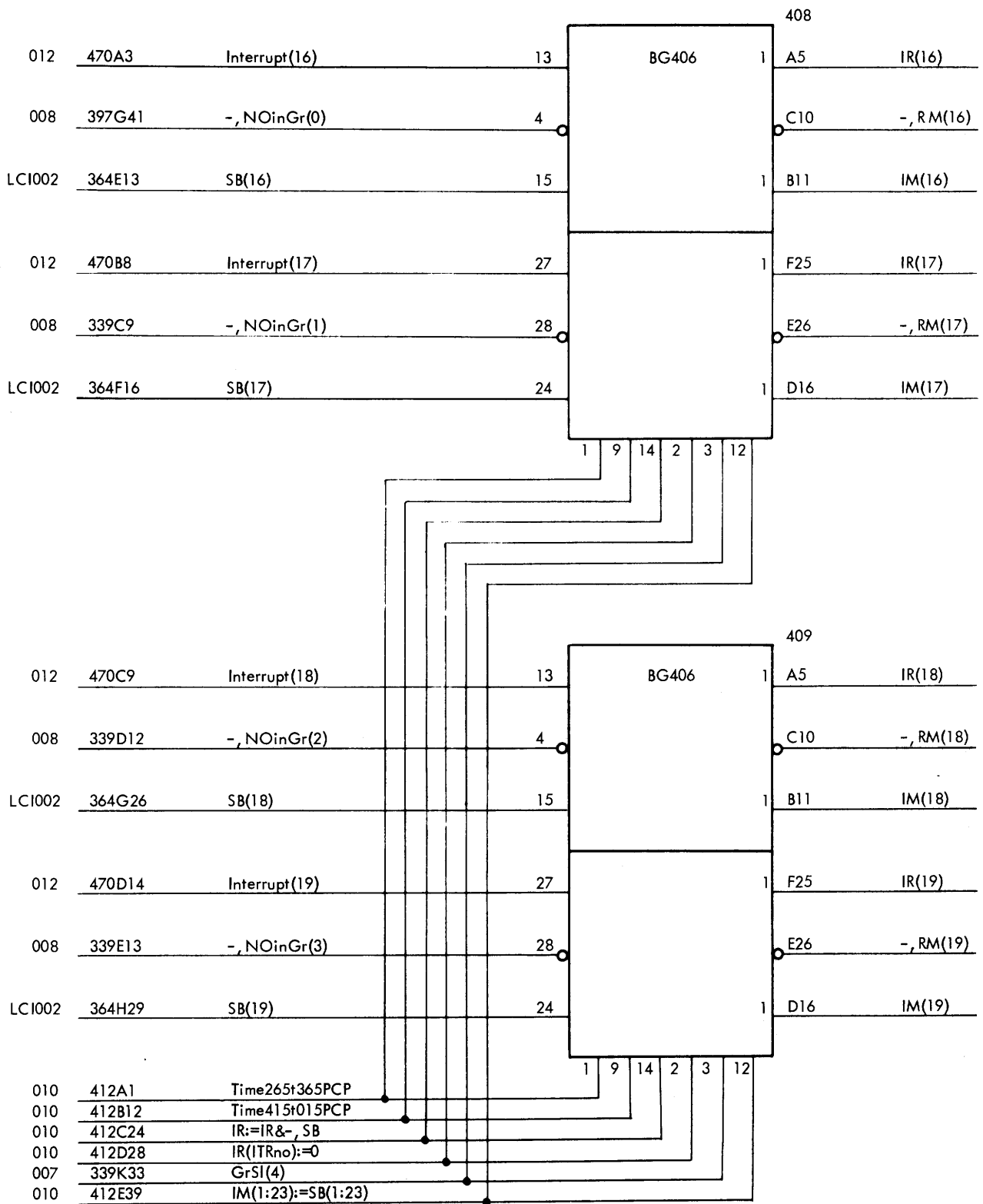


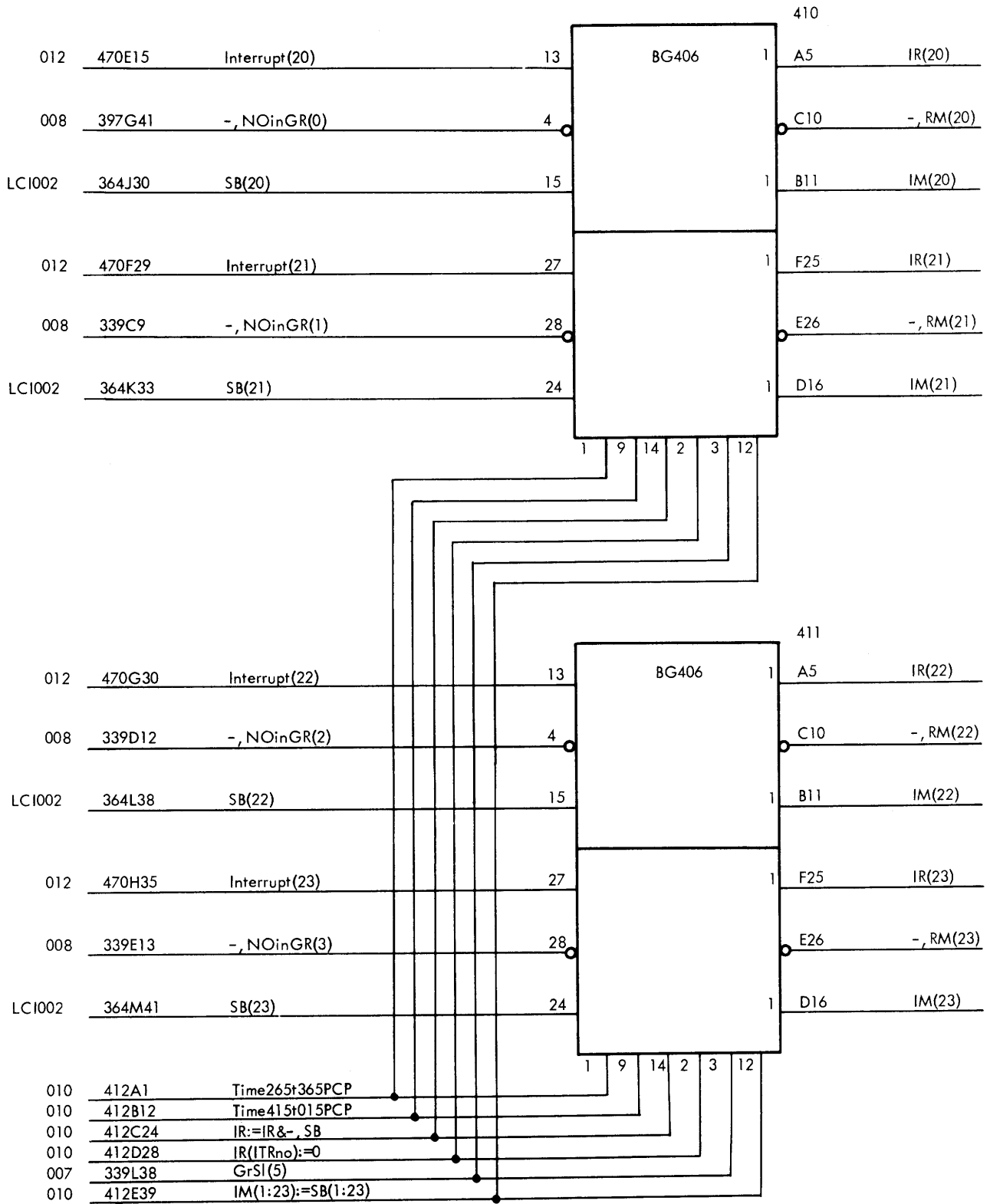


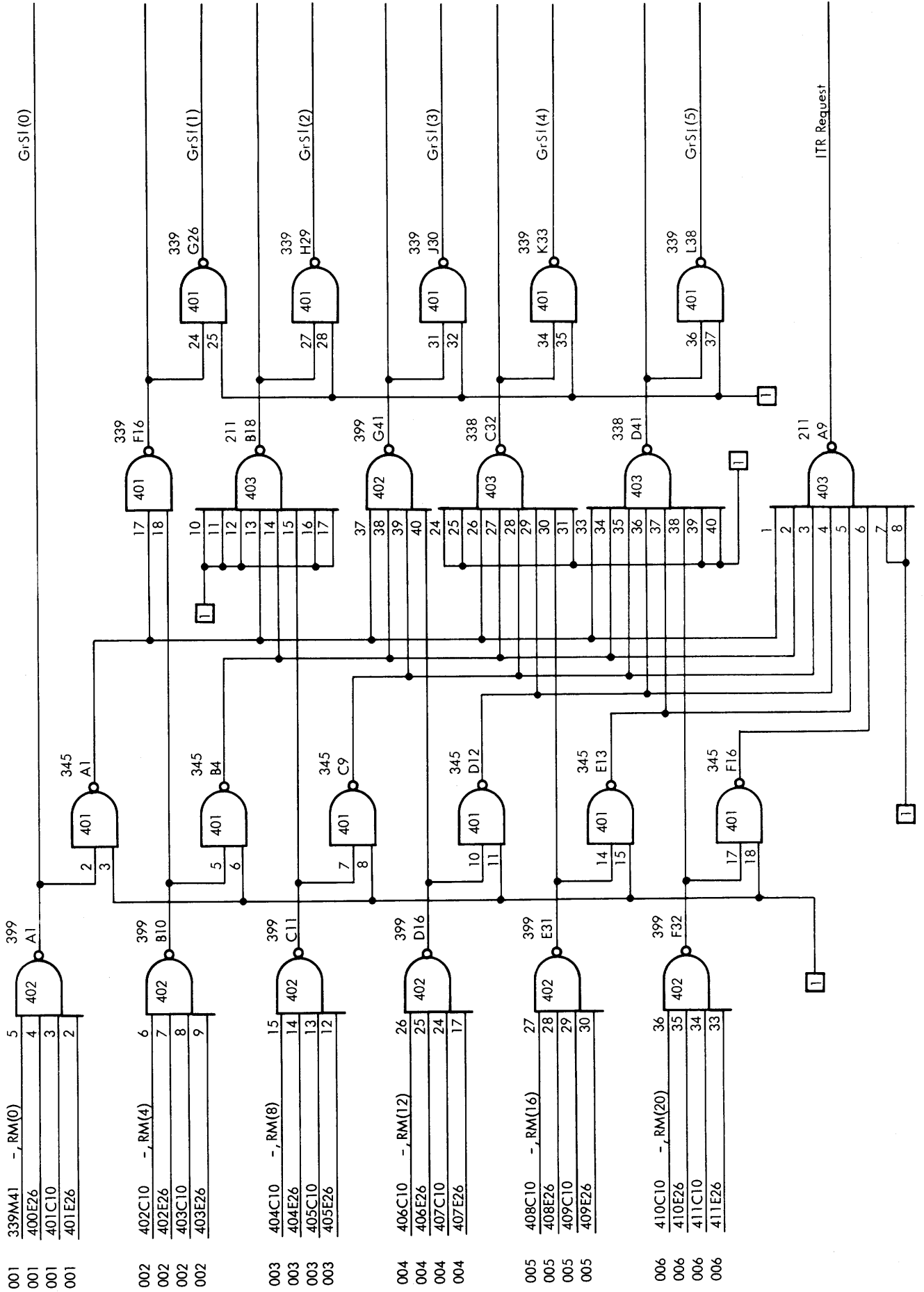


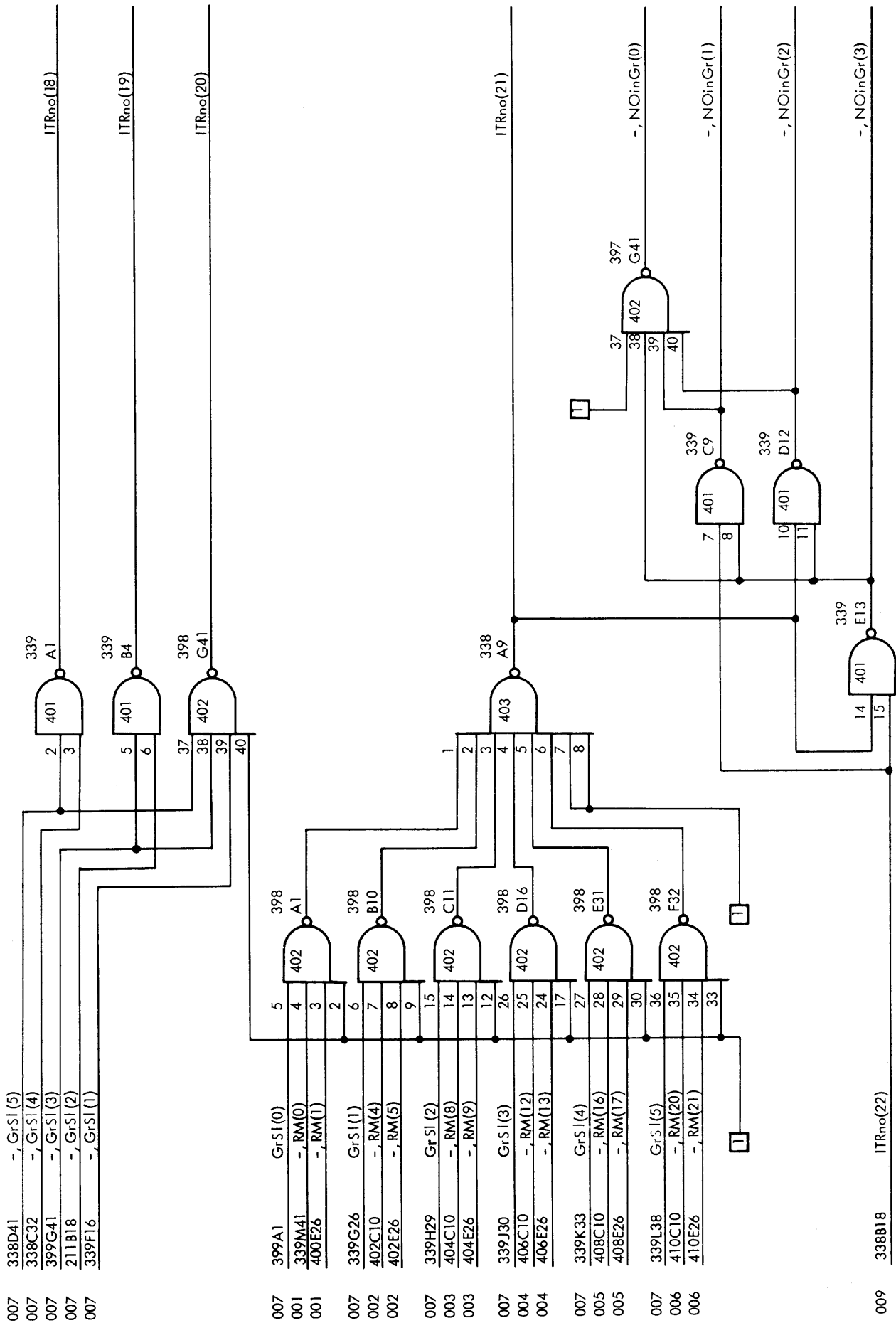












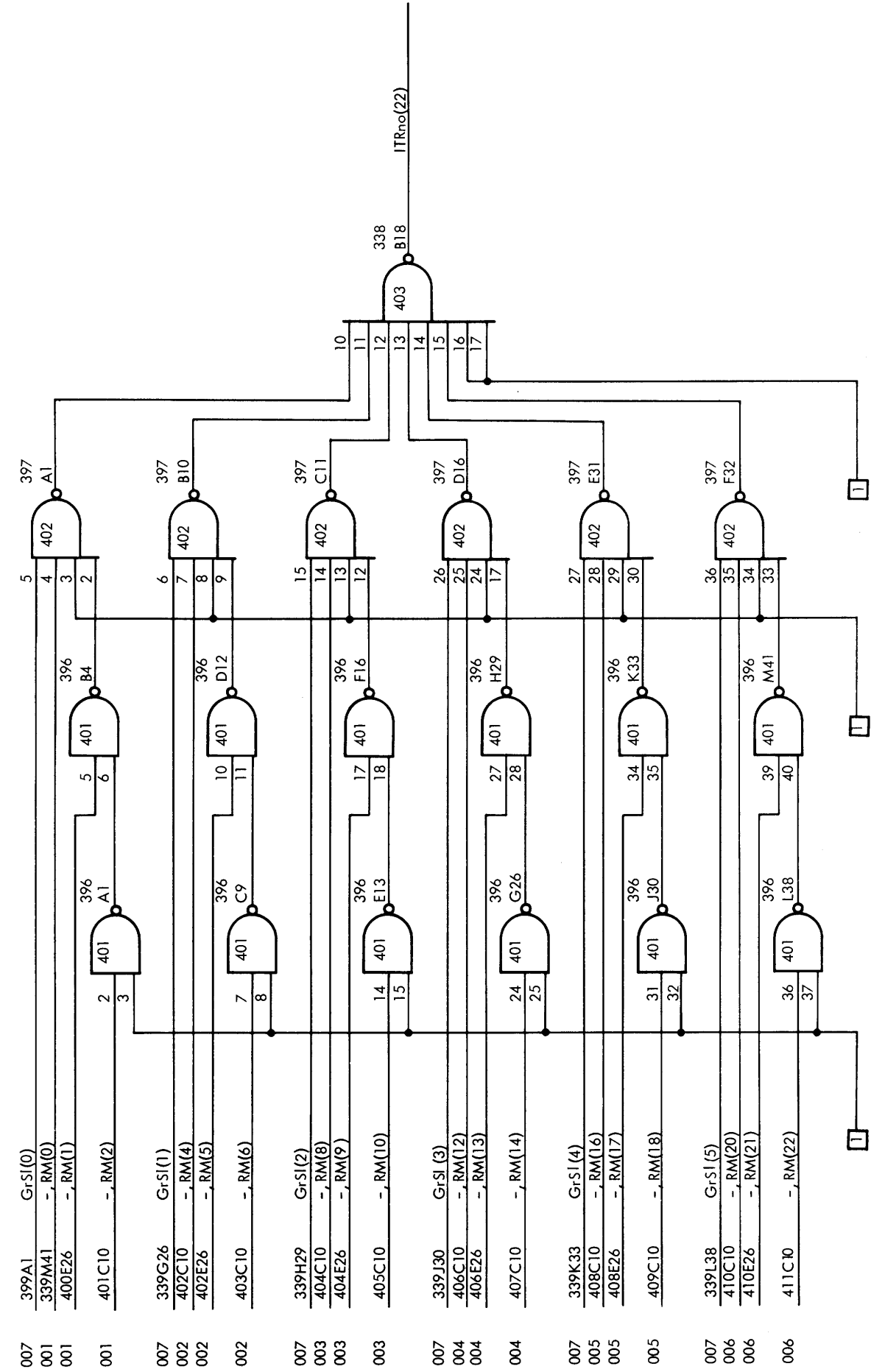
RC4000

ITRno(18:21), NOinGr(0:3)

V10649

Logic Diagram

ITR008



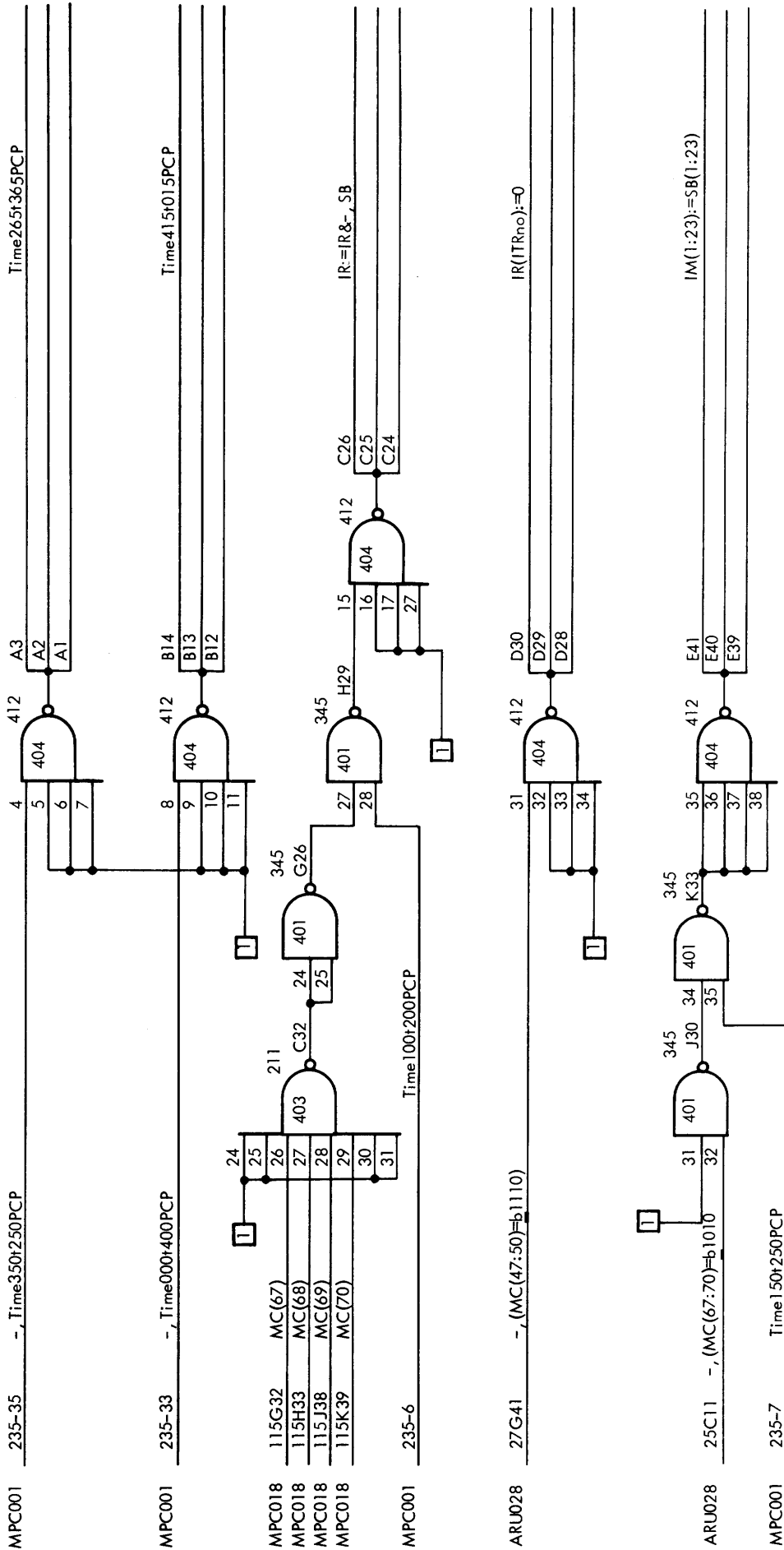
RC4000
V10650

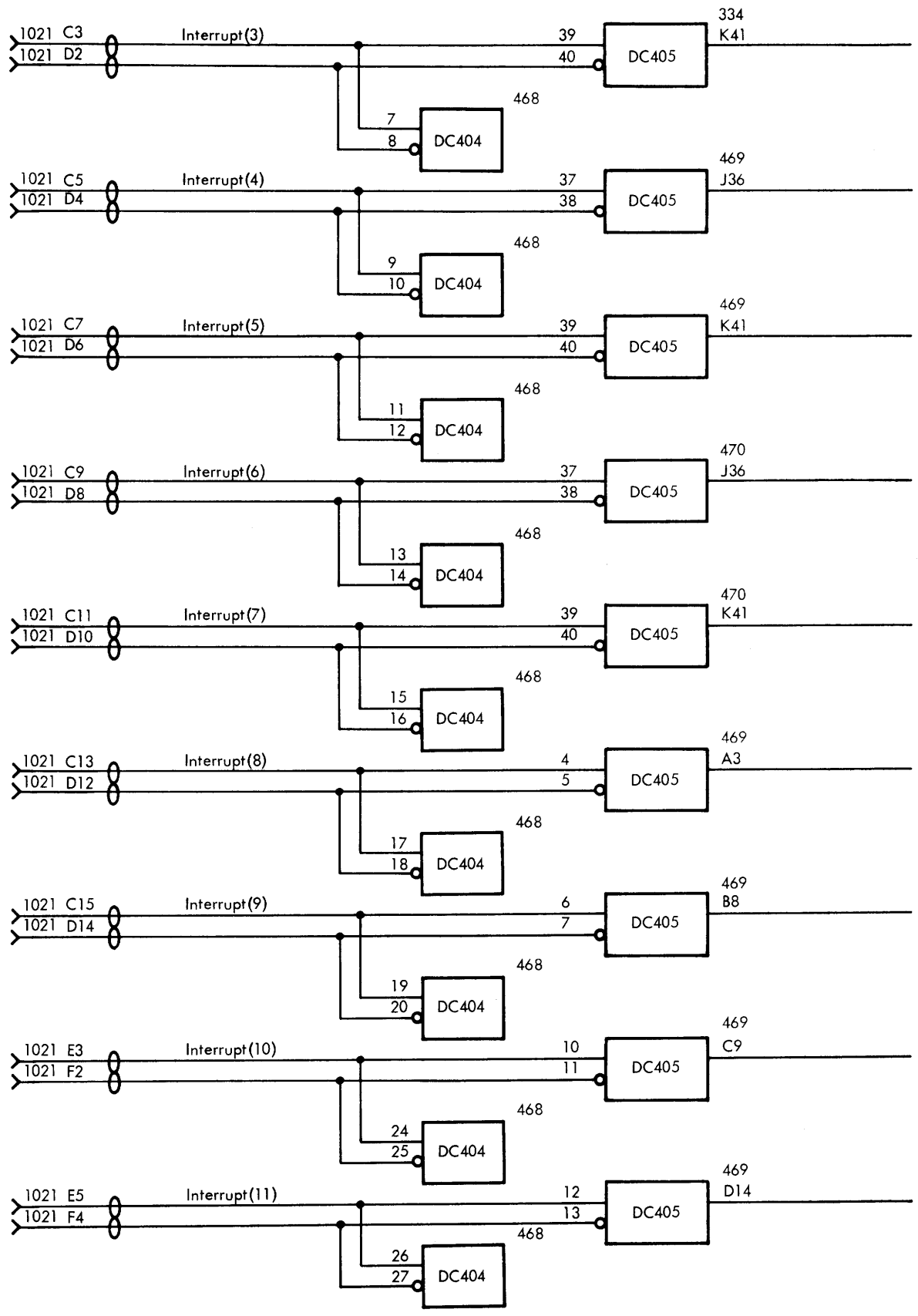
ITRno(22)
Logic Diagram

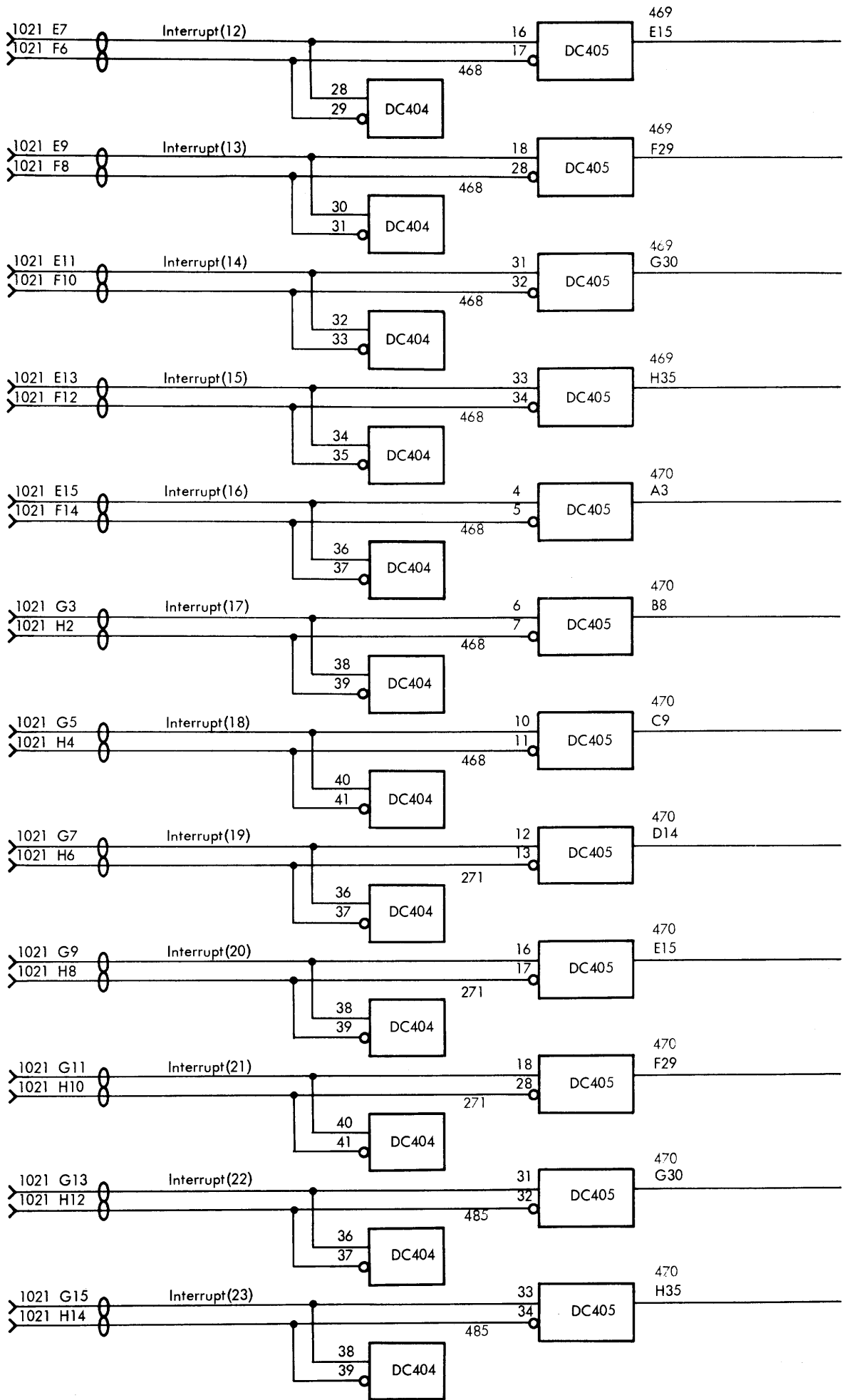
ITR009

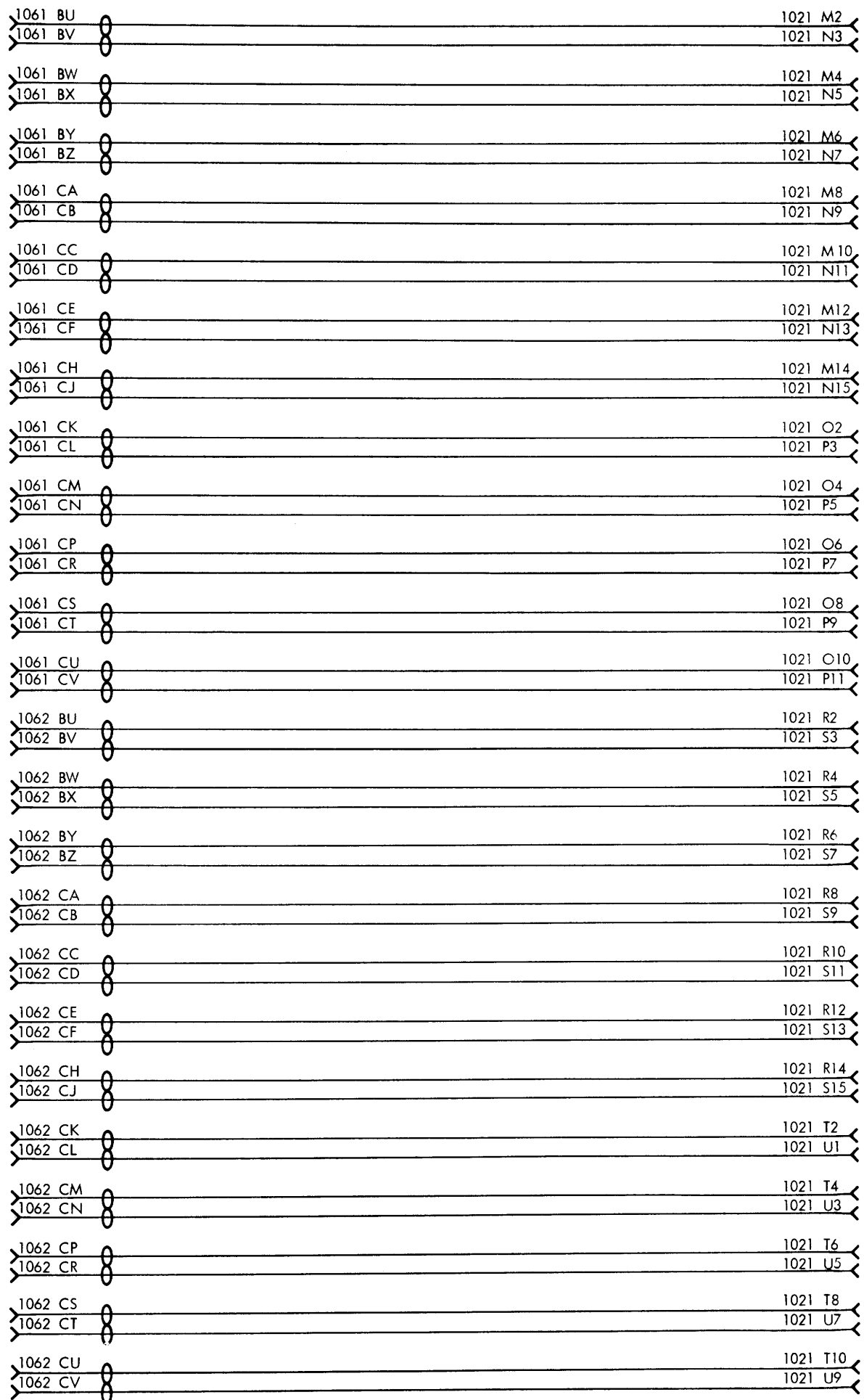
CONTROL AND TIMING SIGNALS

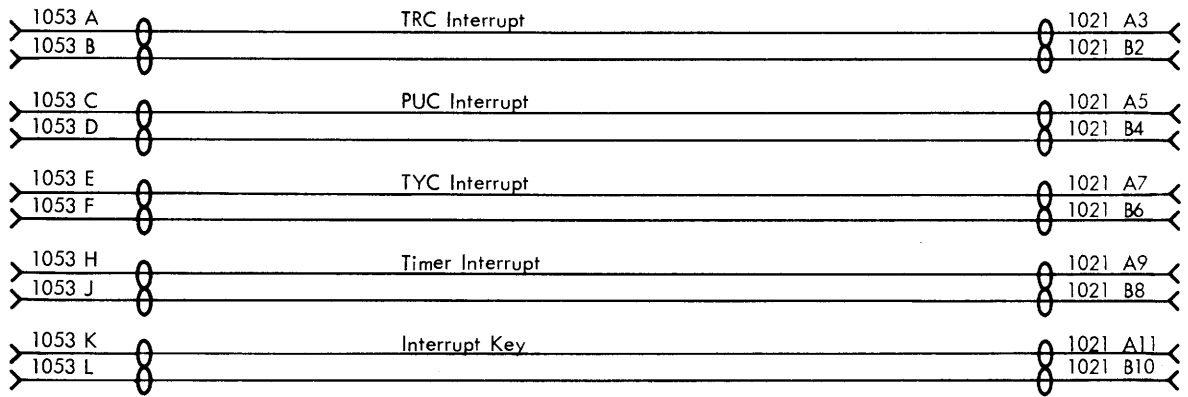
Logic Diagram

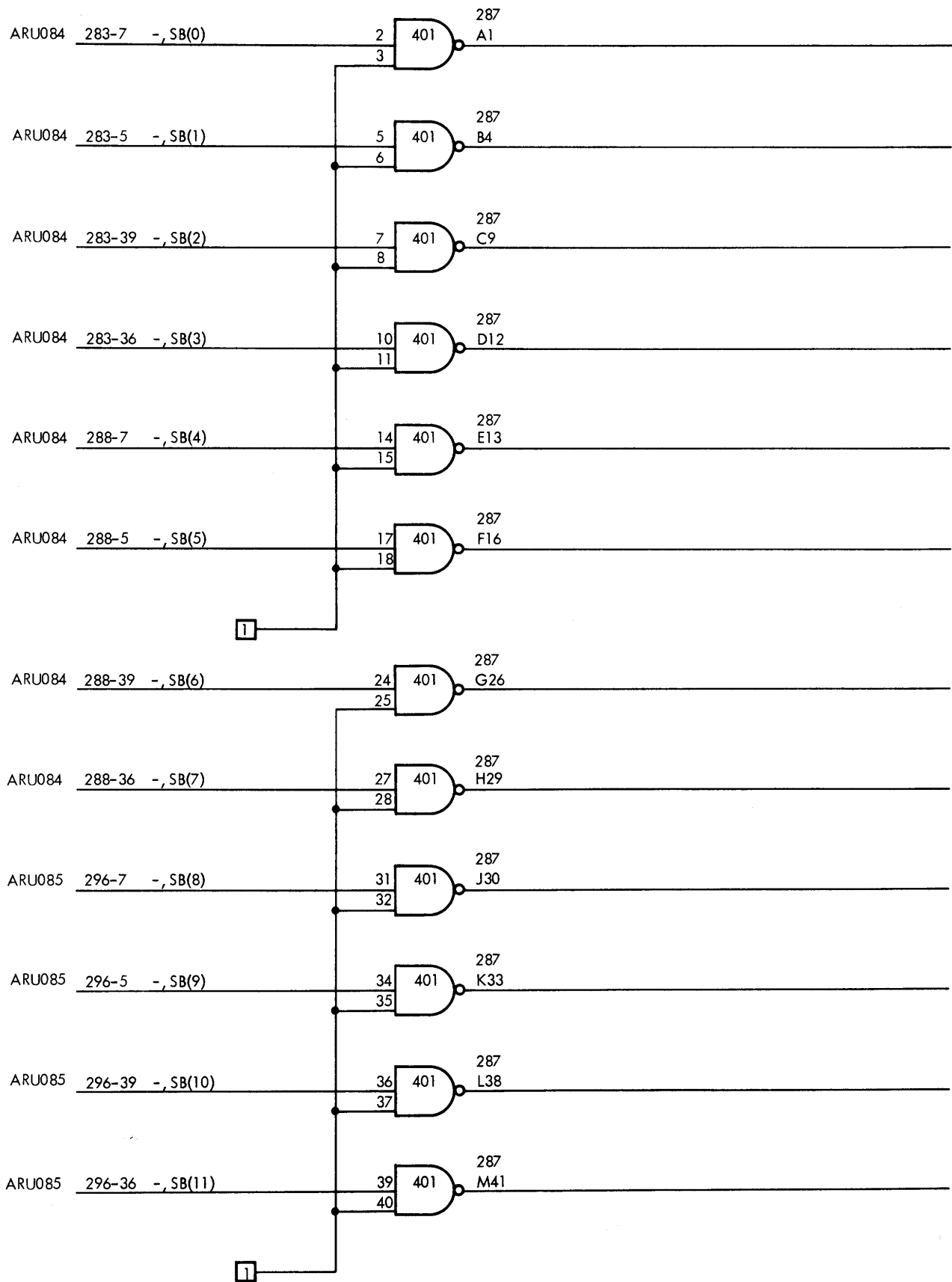


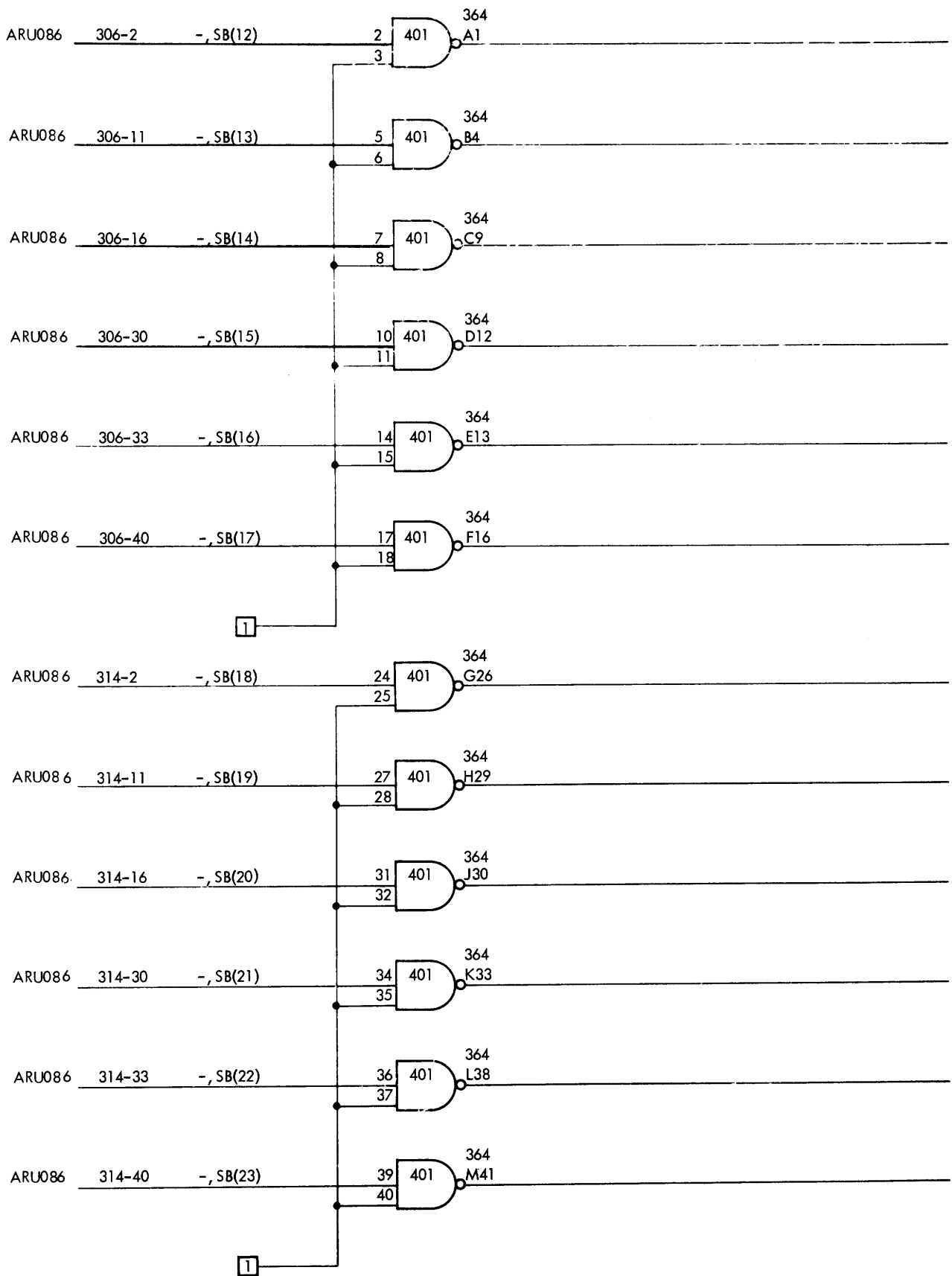


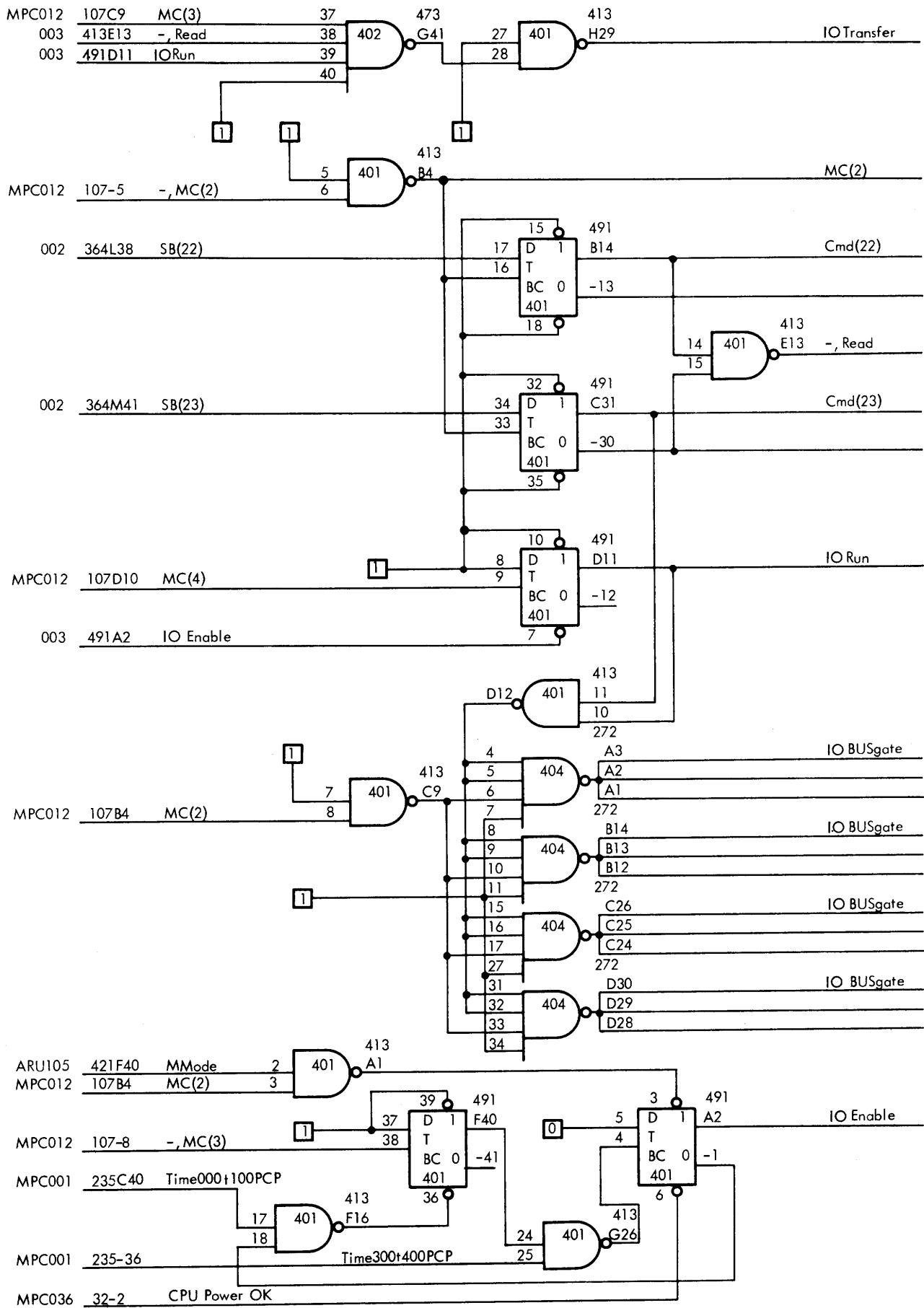


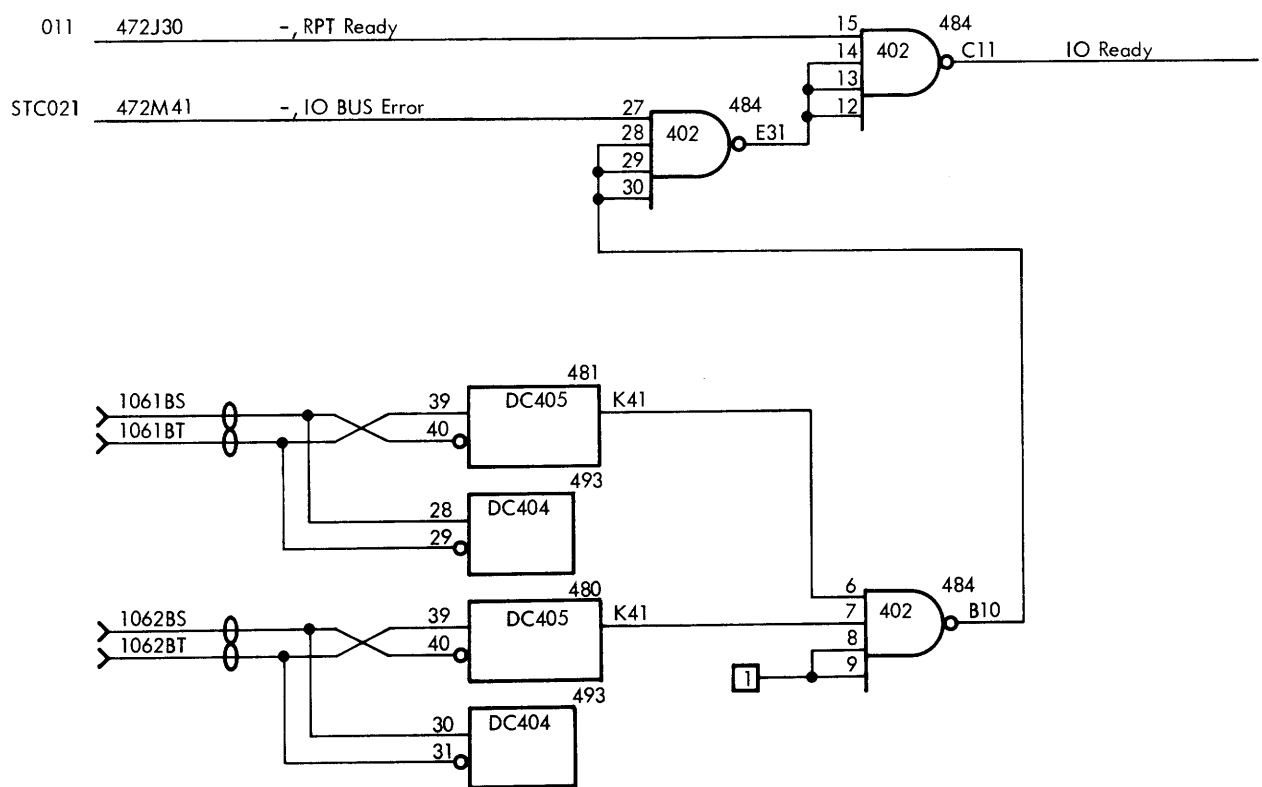
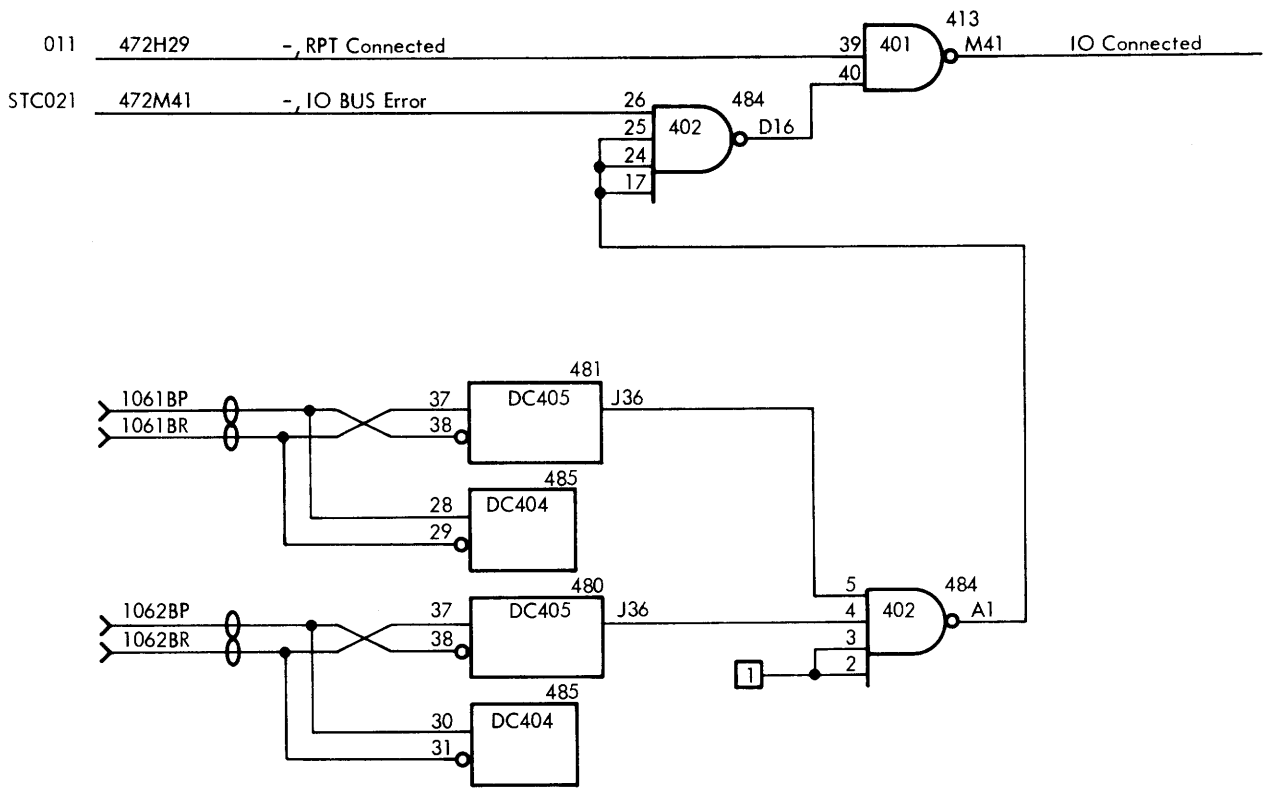


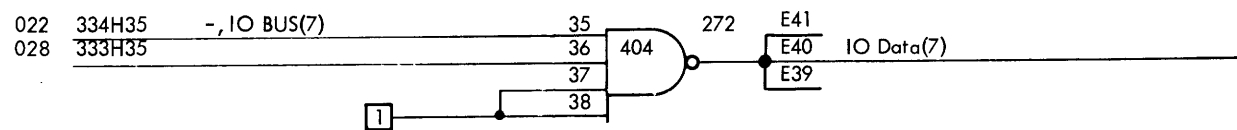
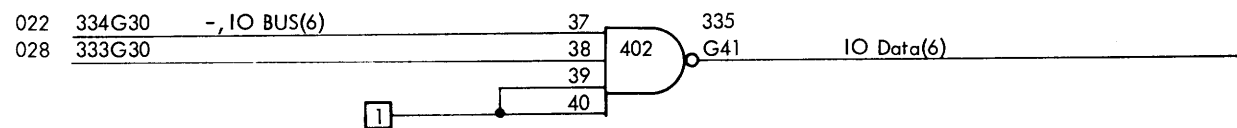
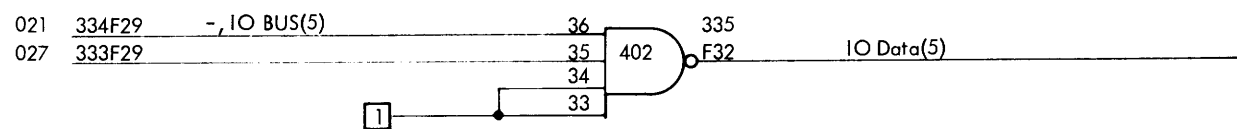
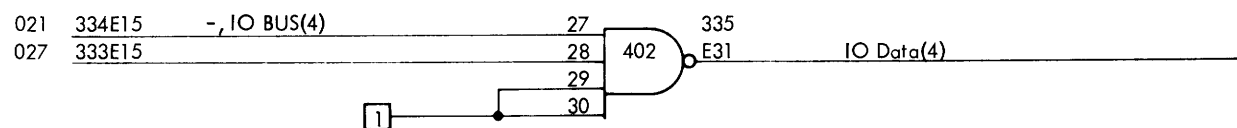
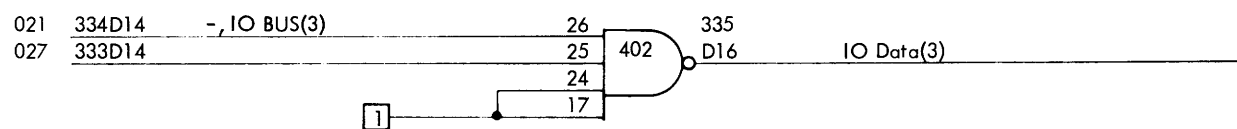
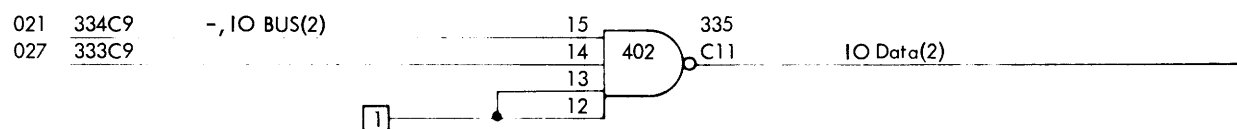
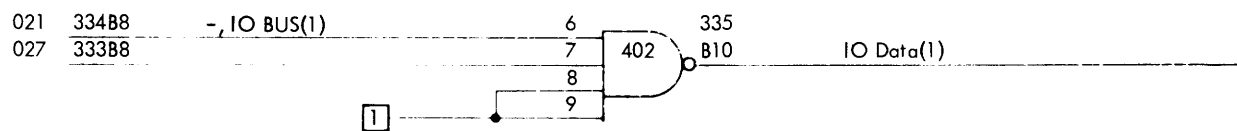
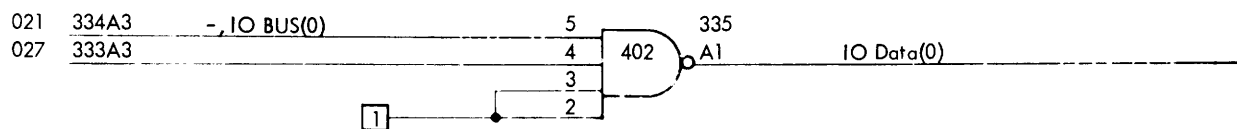


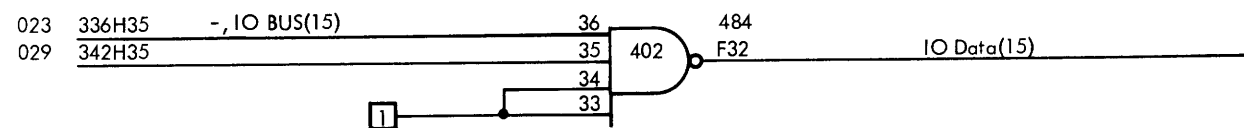
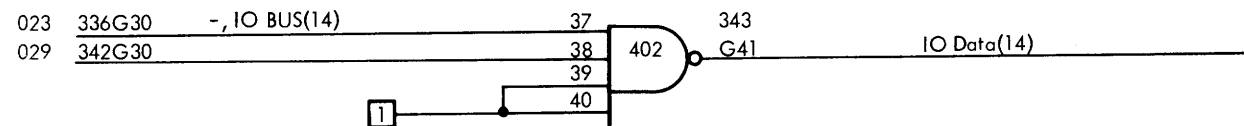
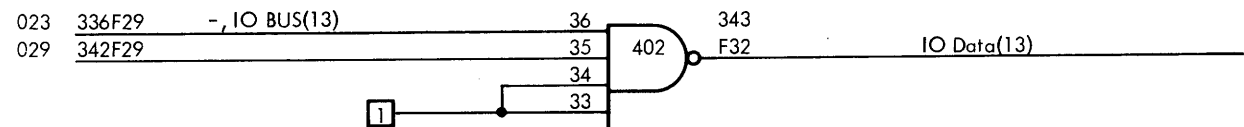
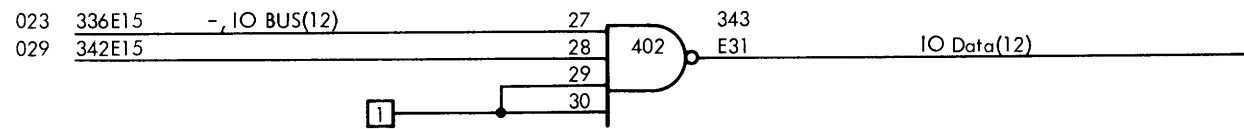
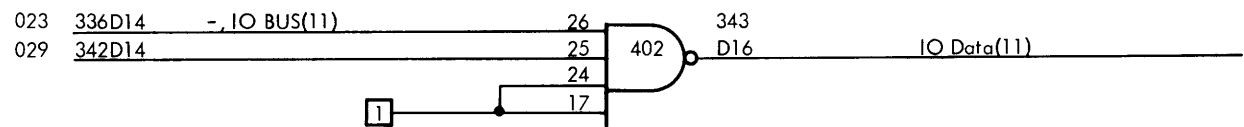
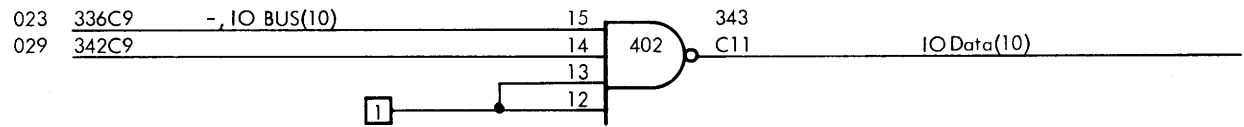
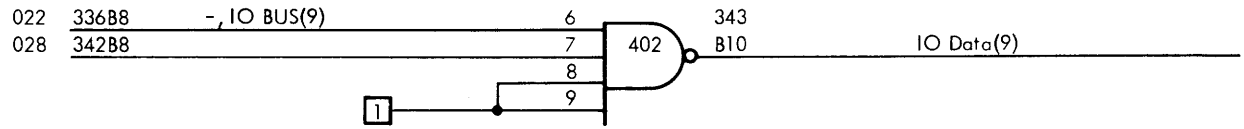
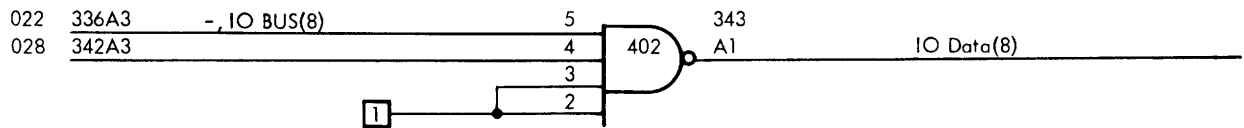


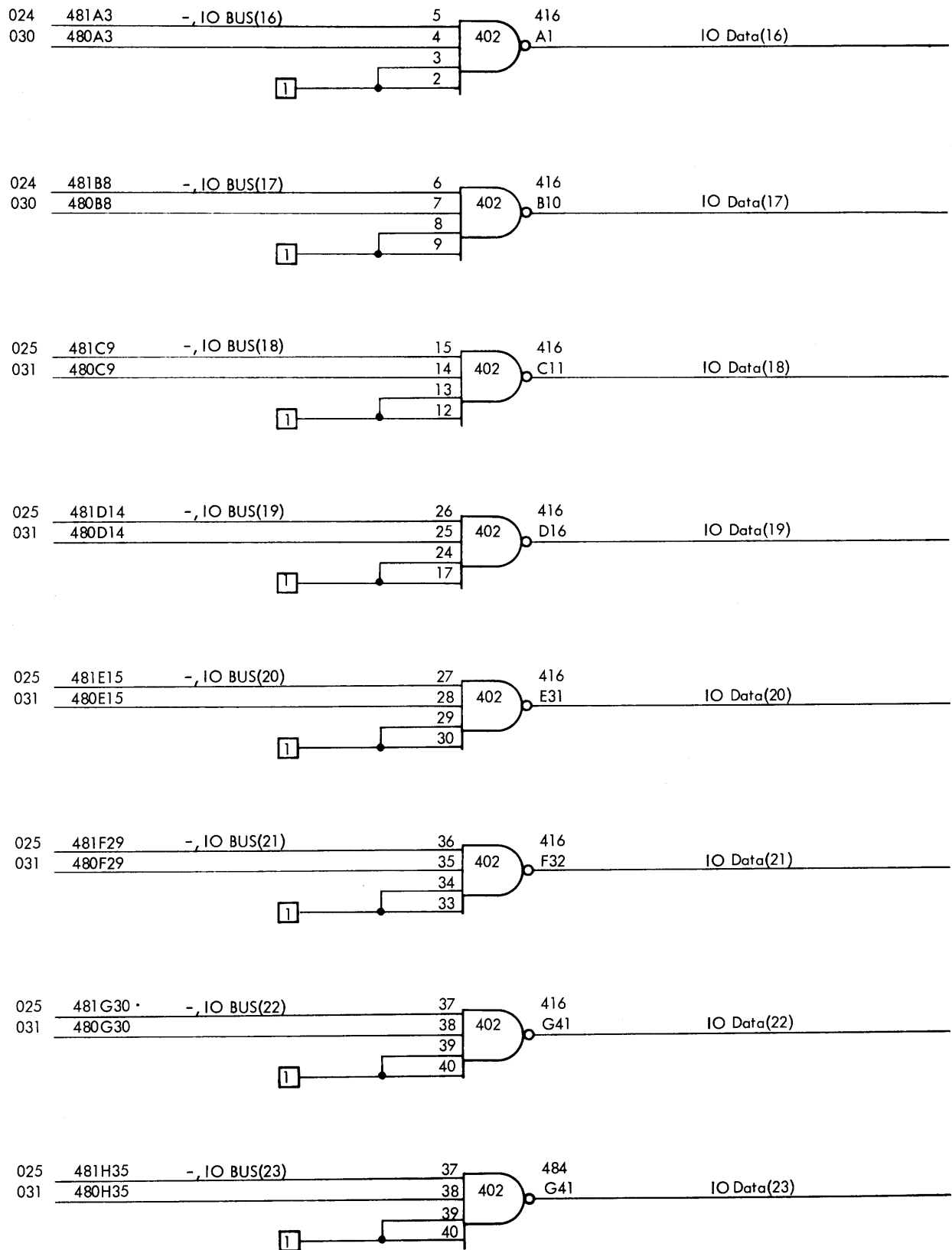


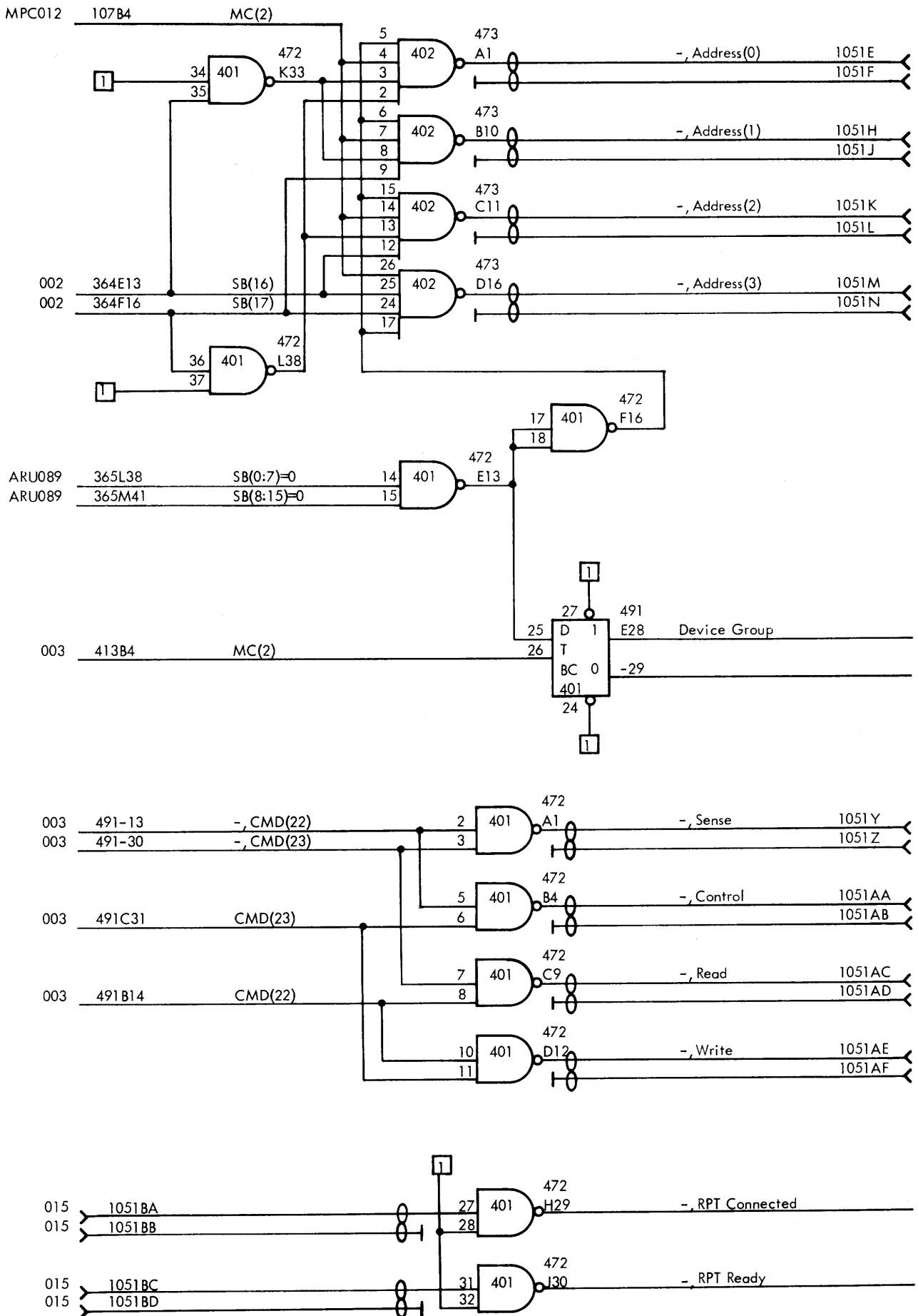


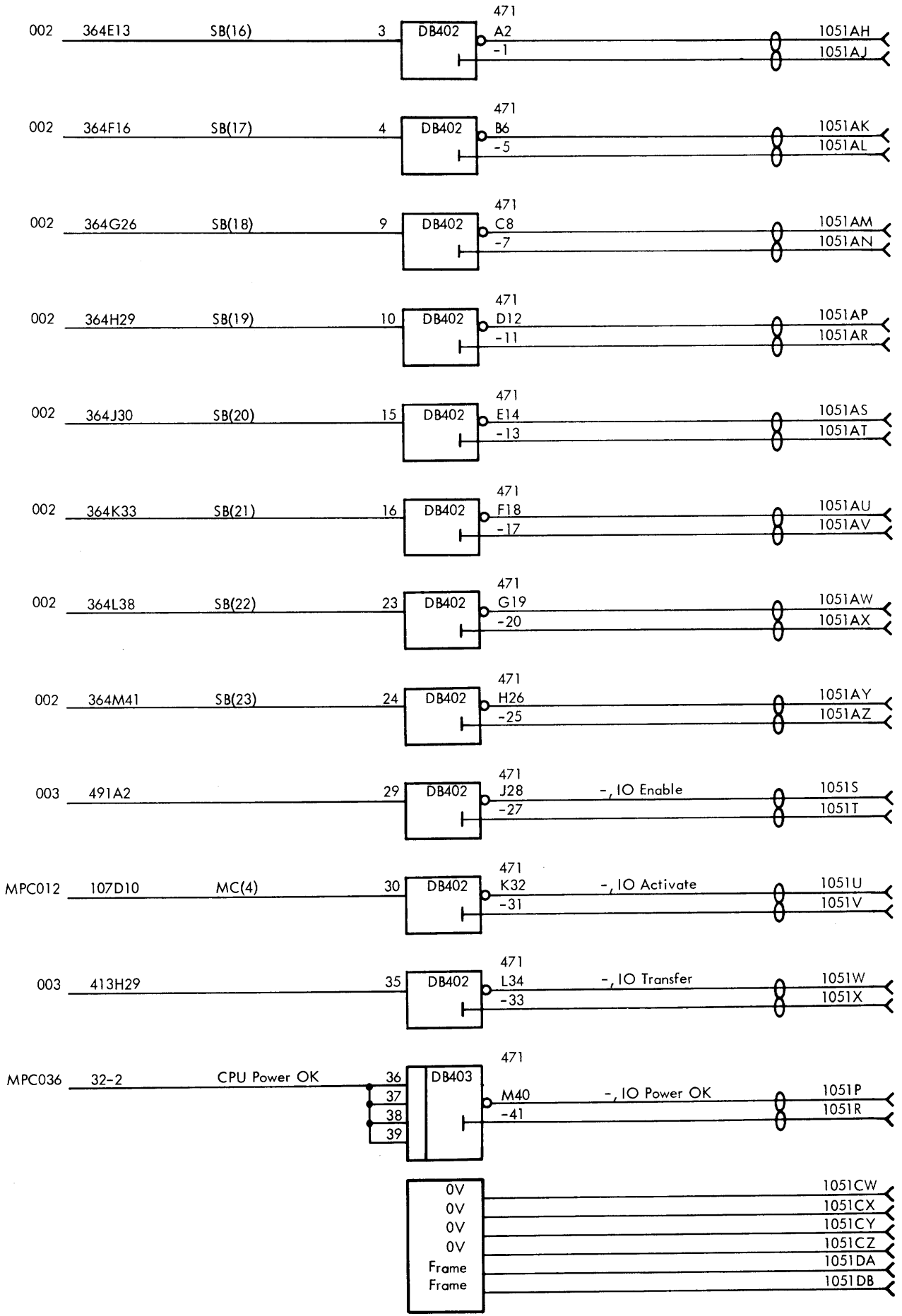


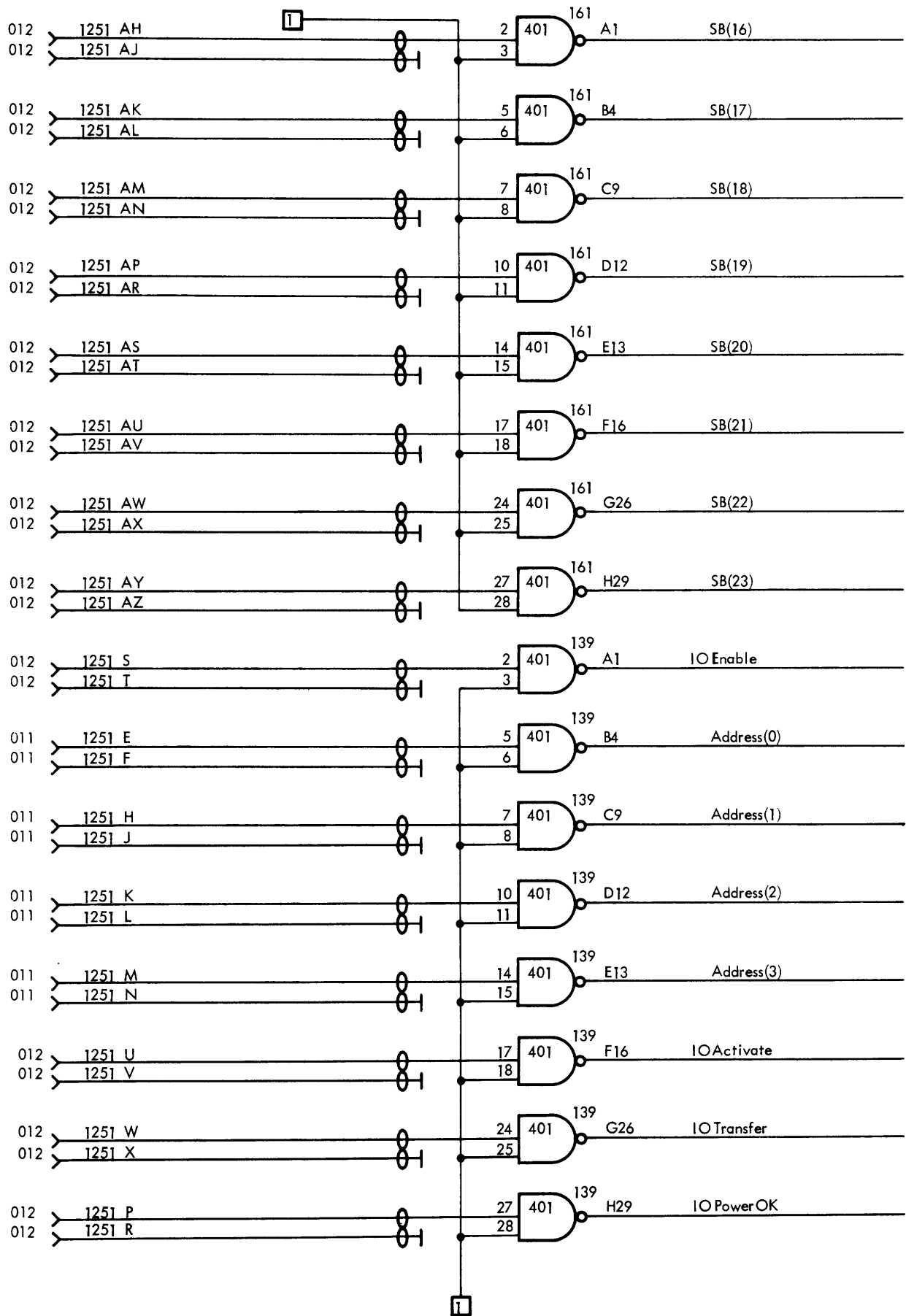


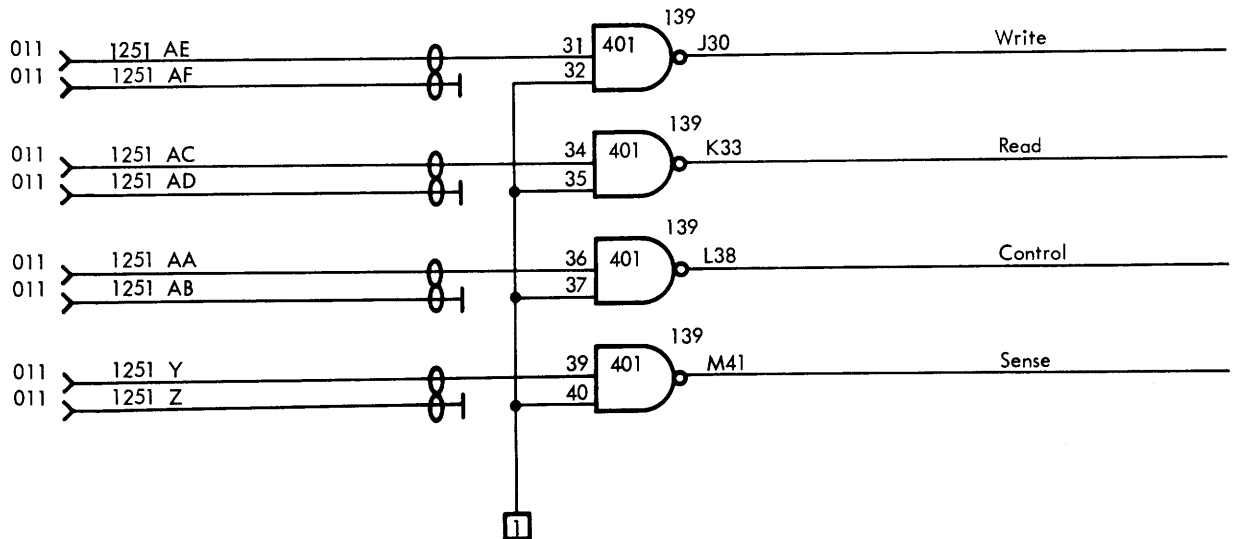
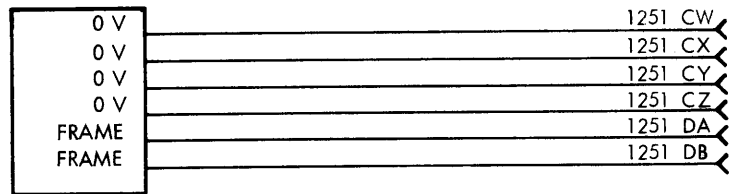
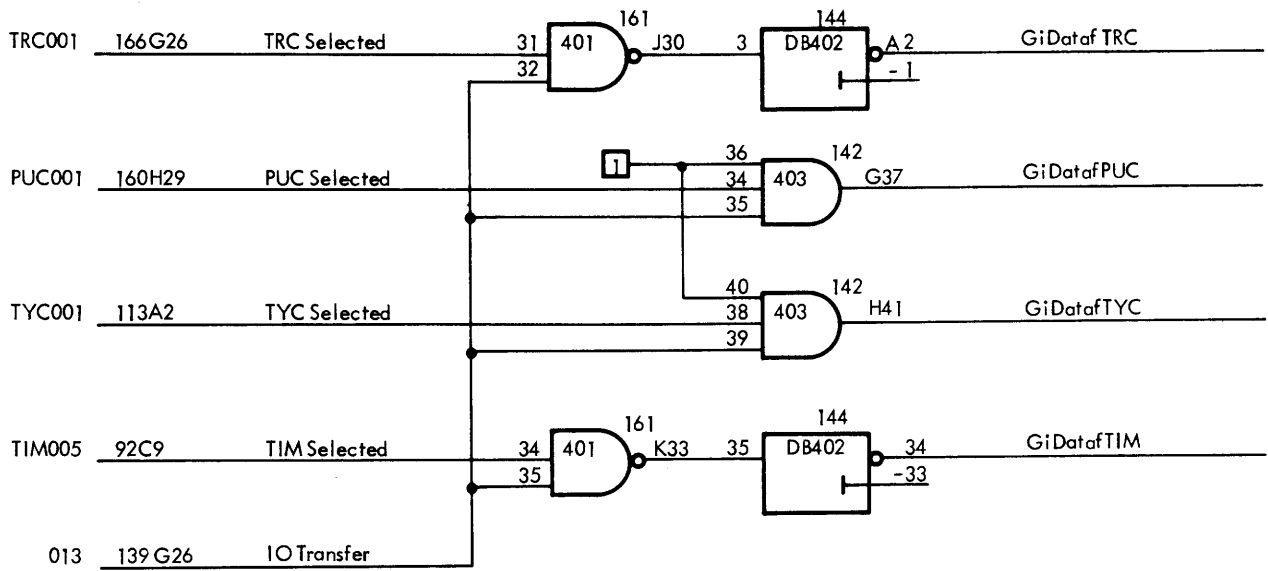


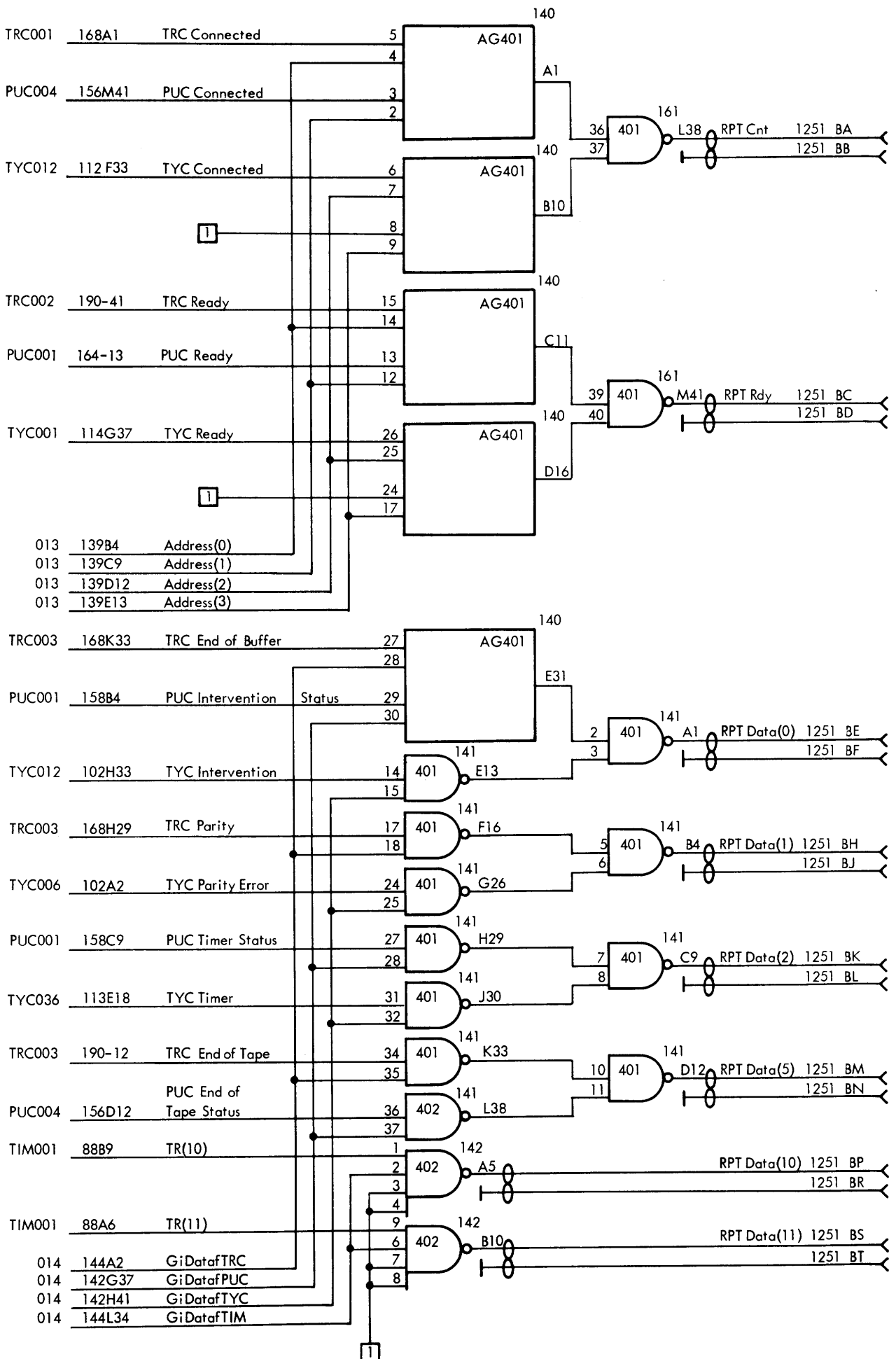


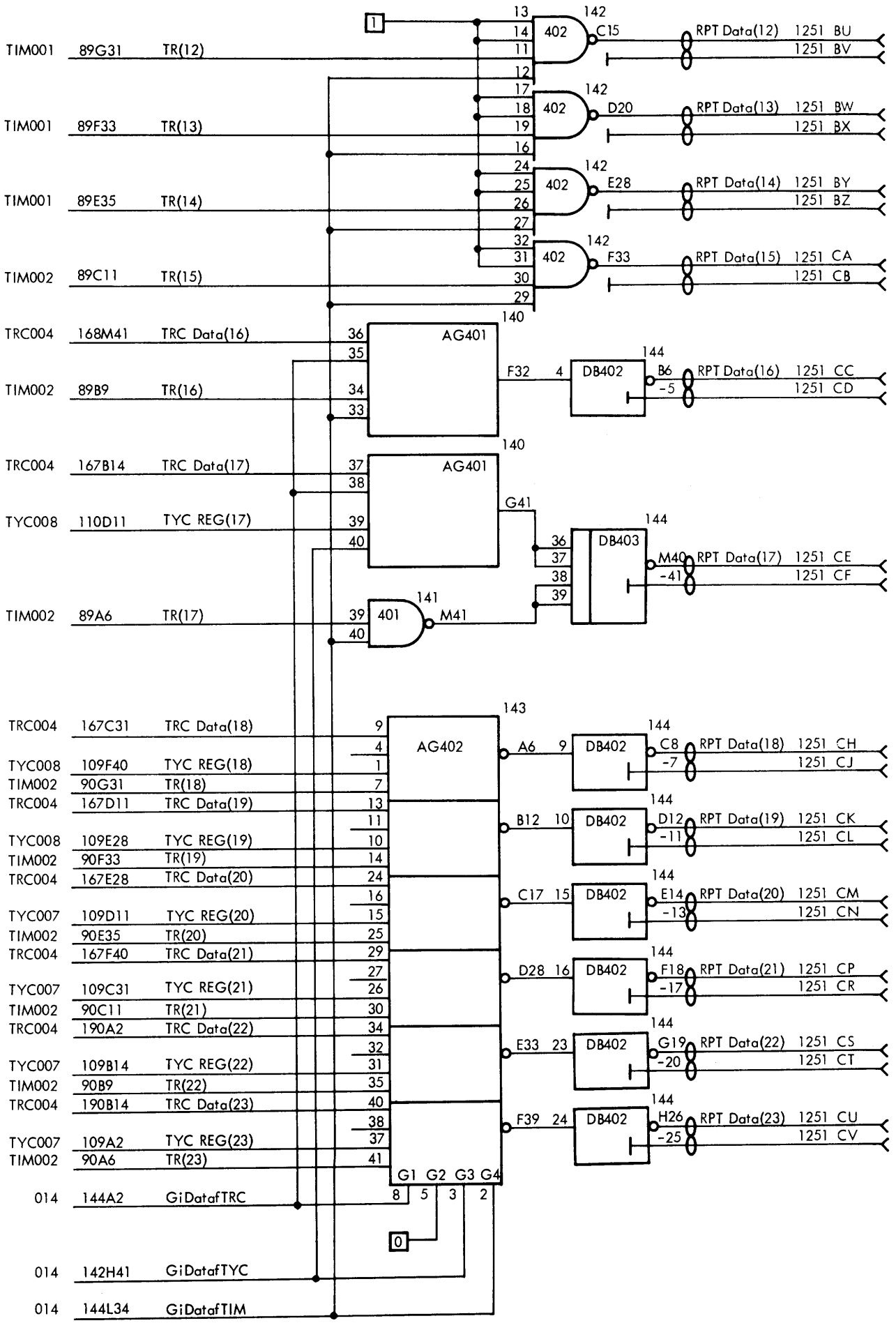


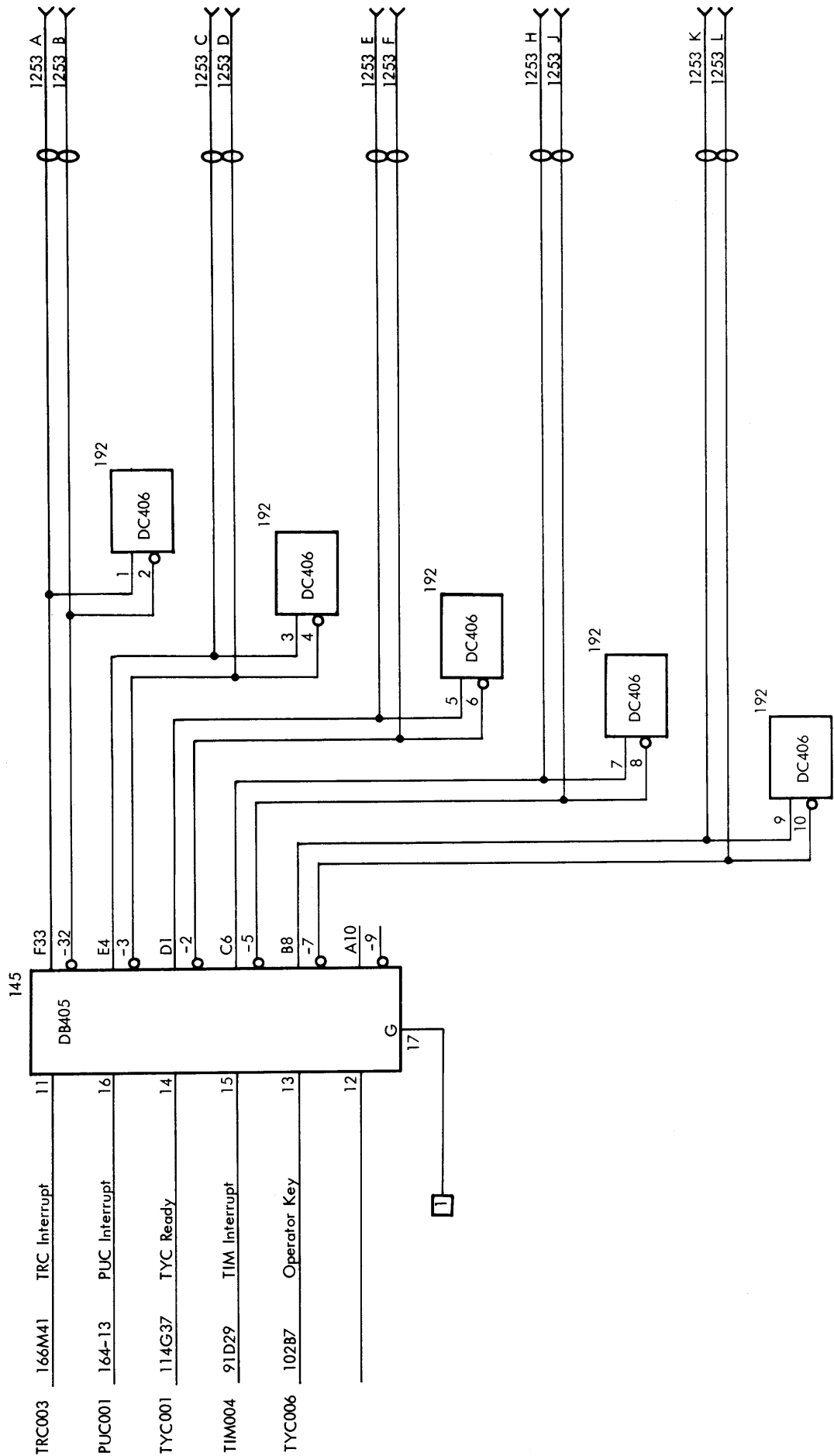


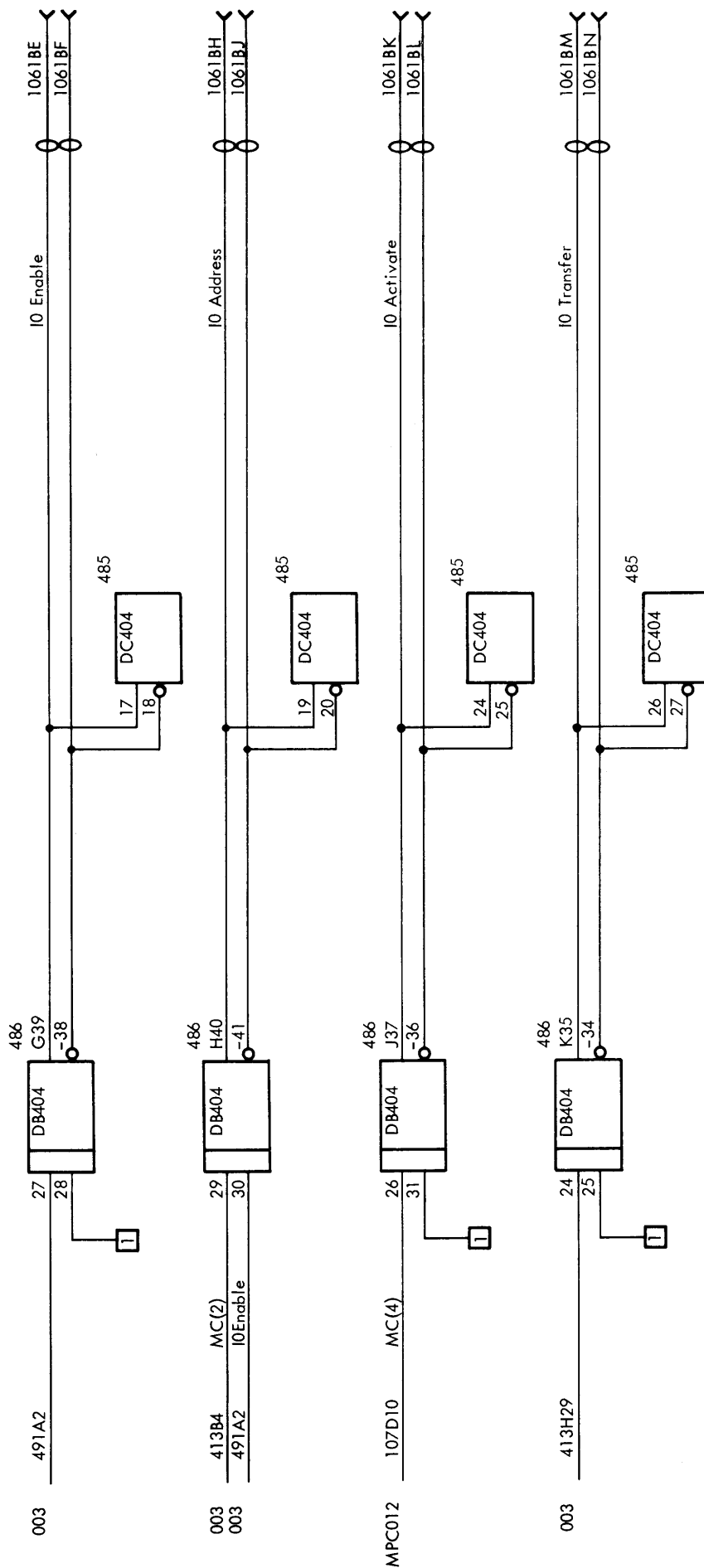


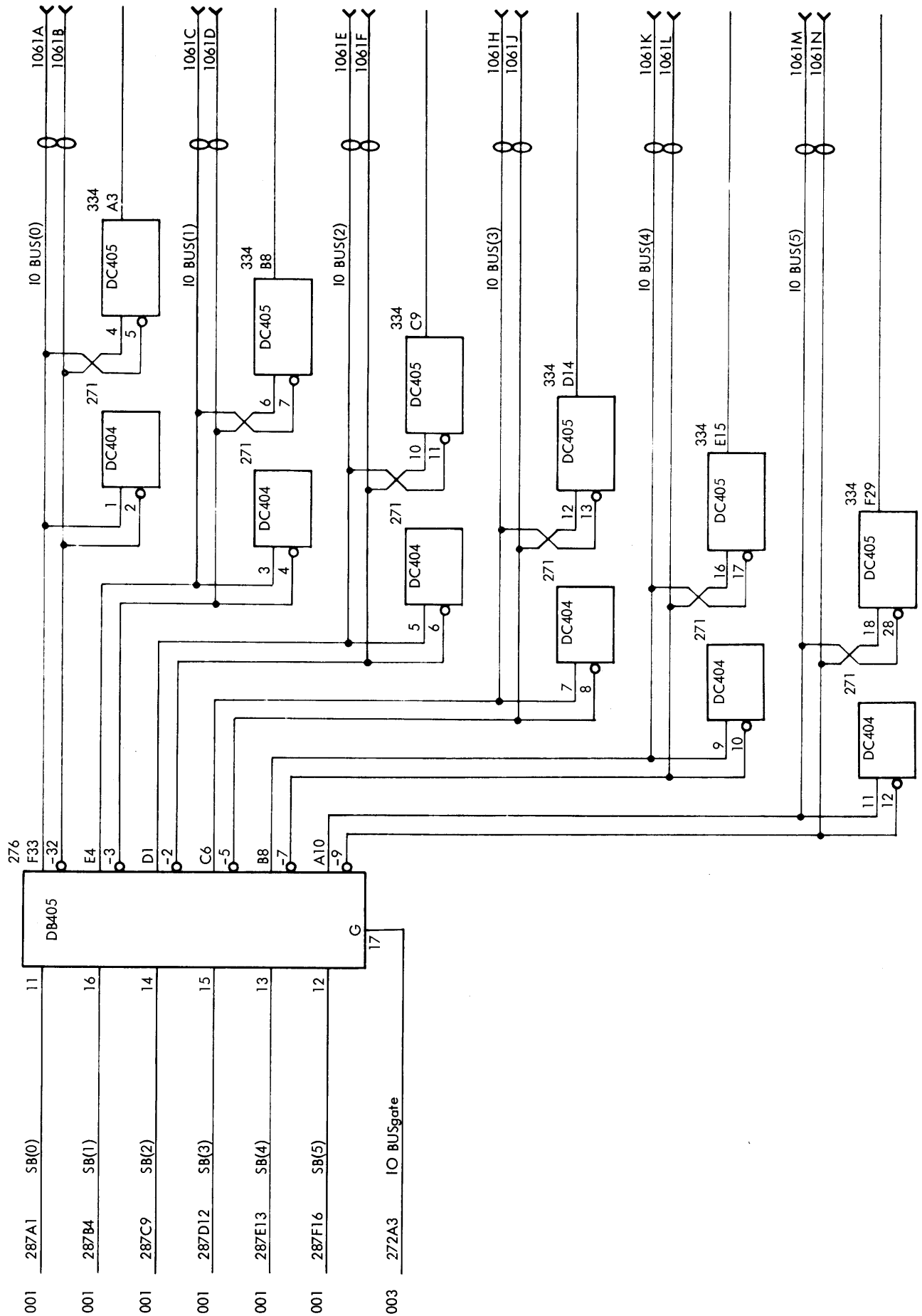


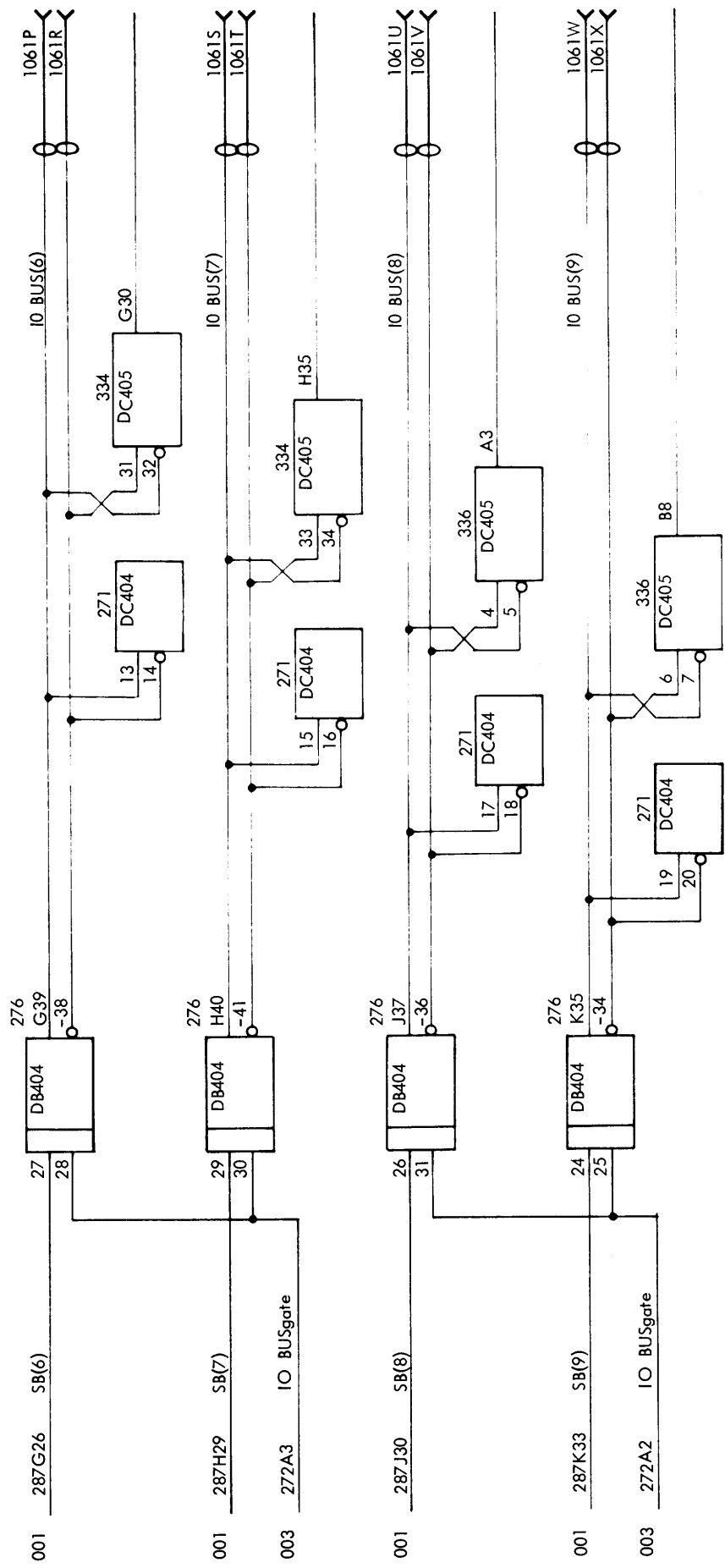


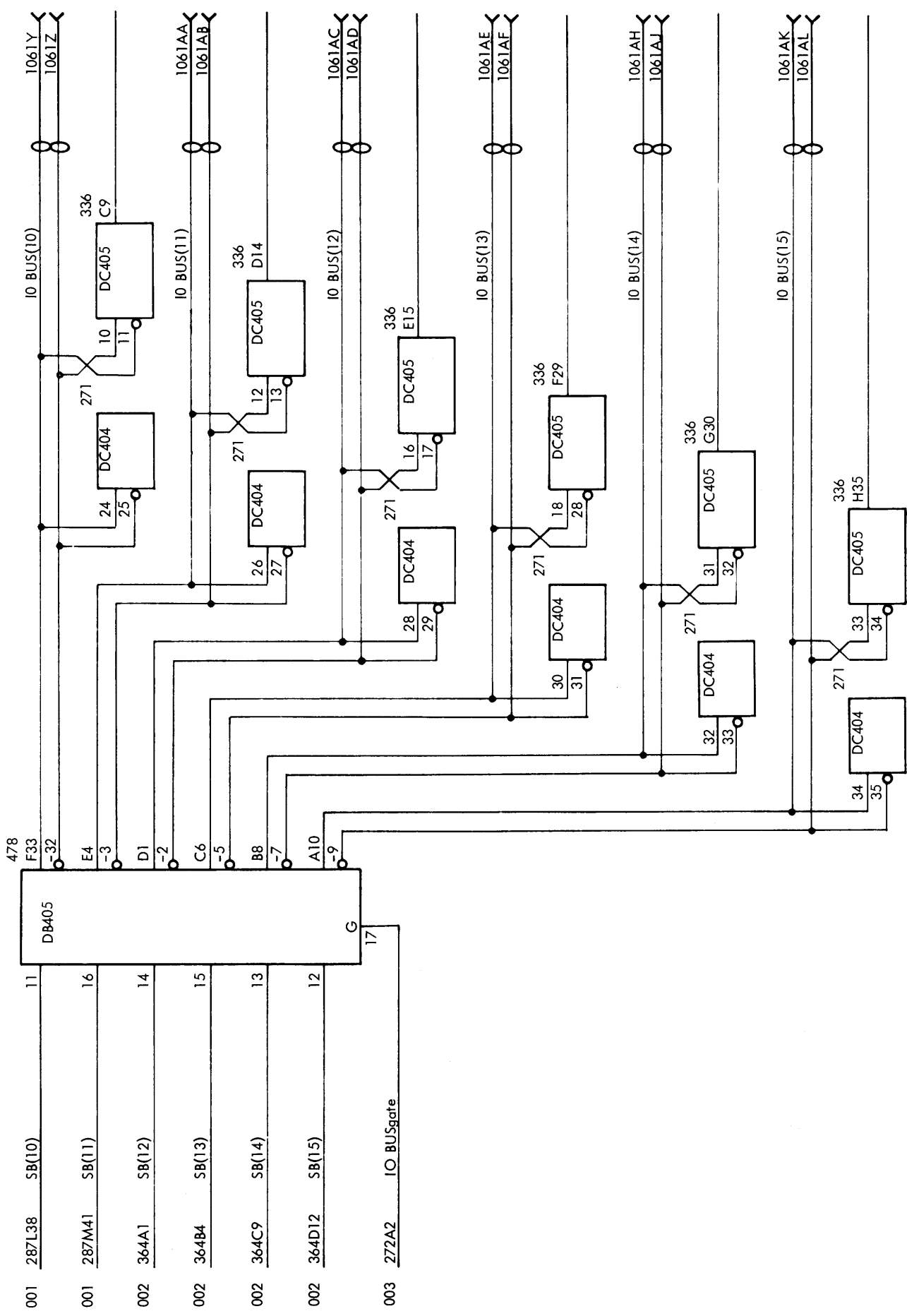


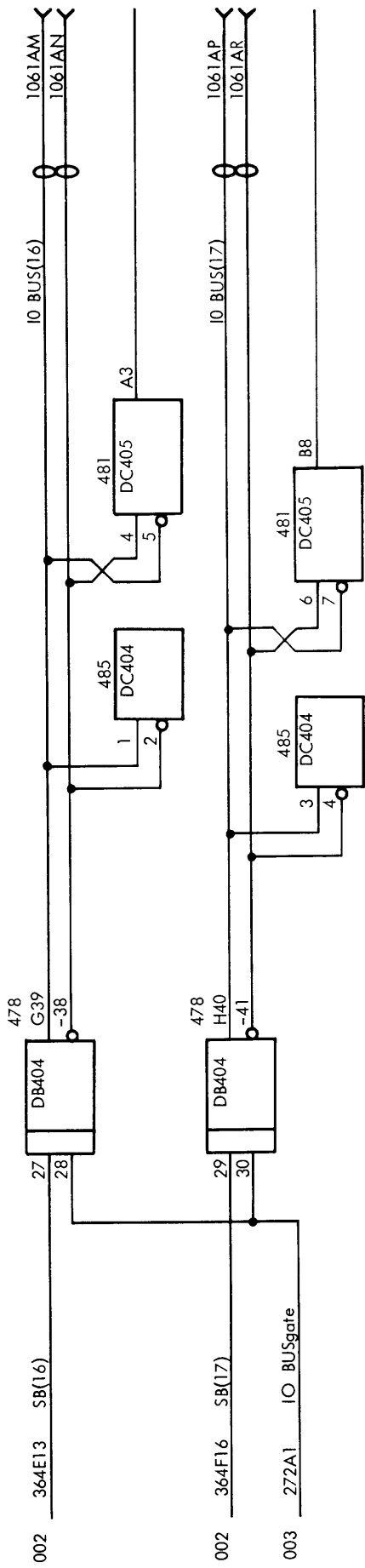


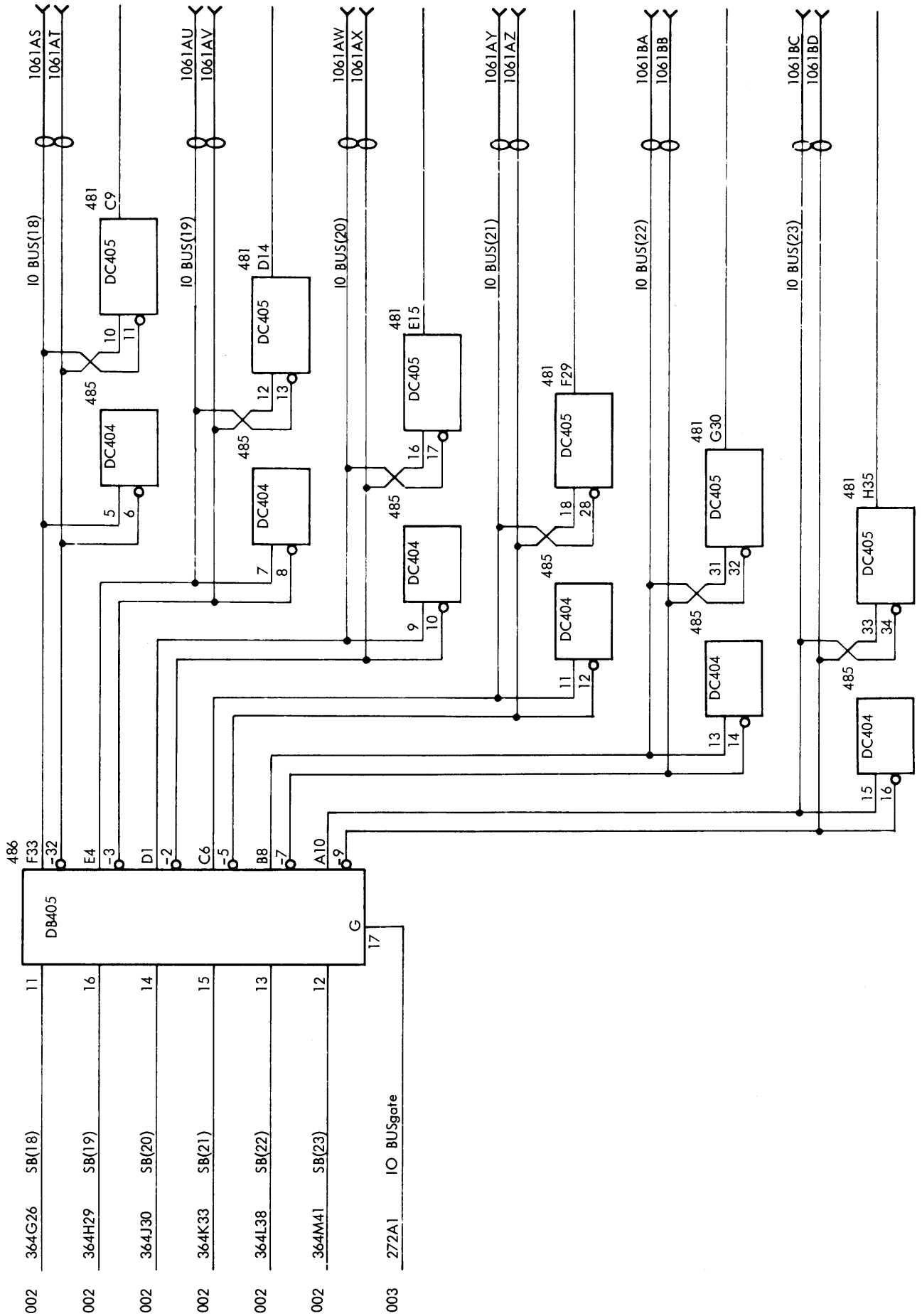


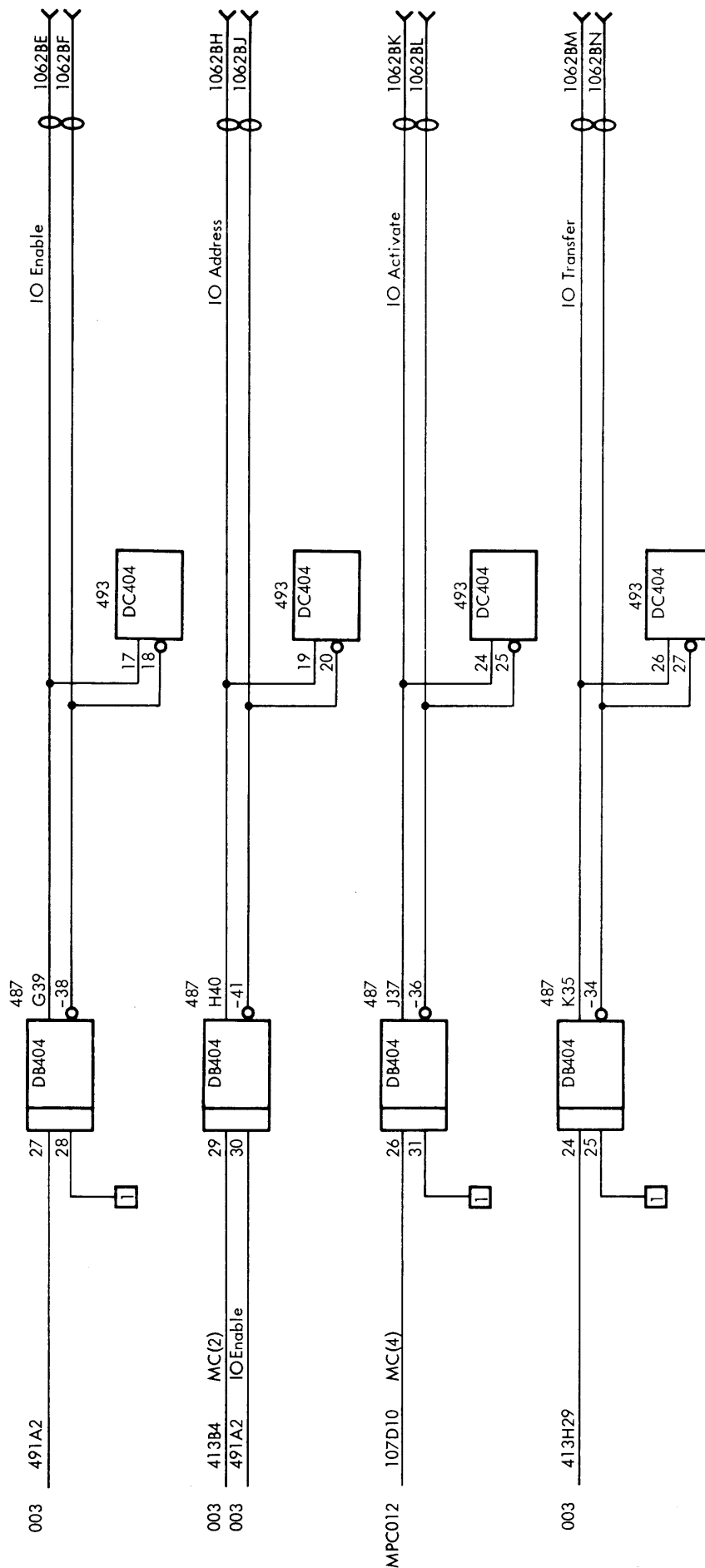


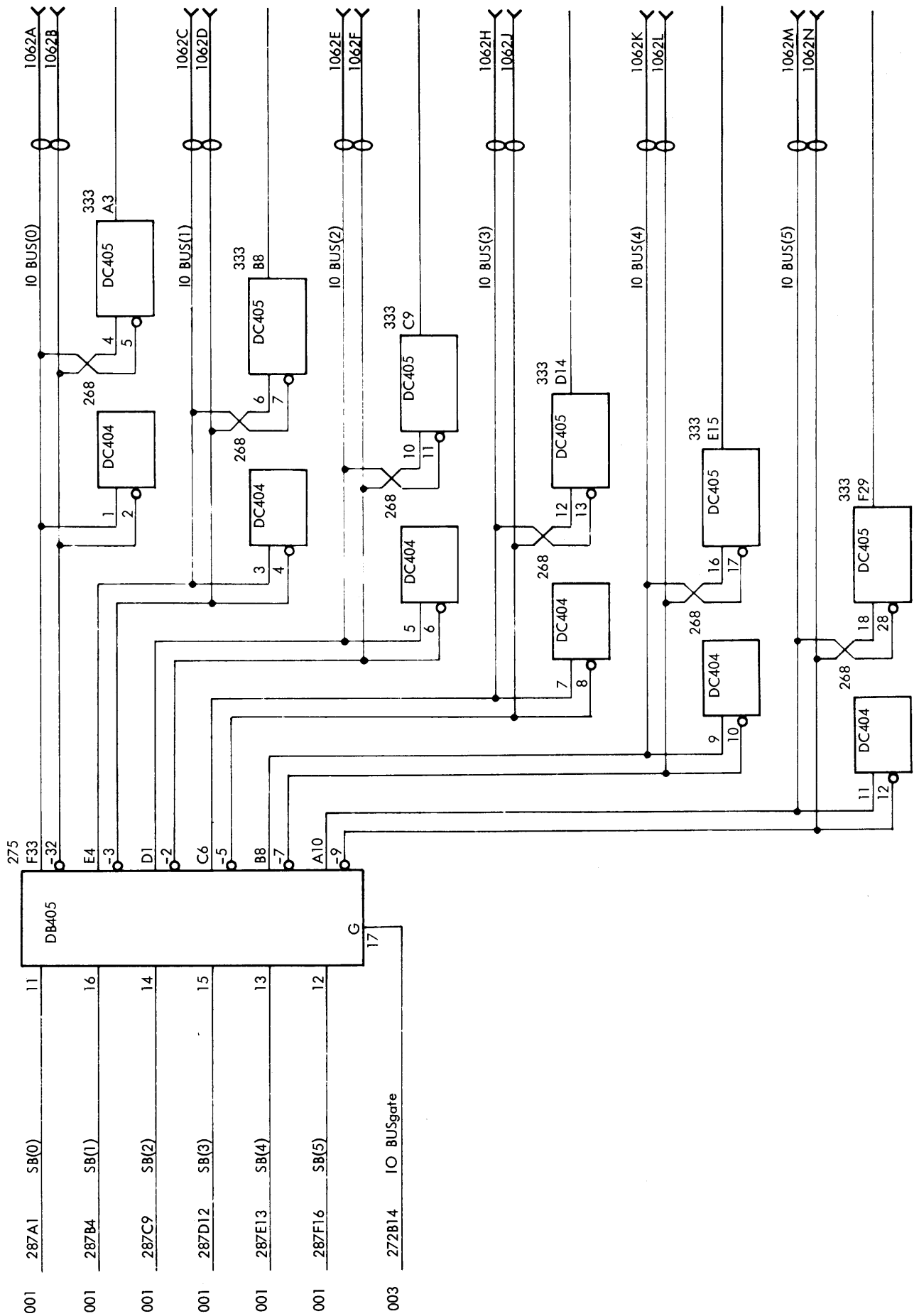


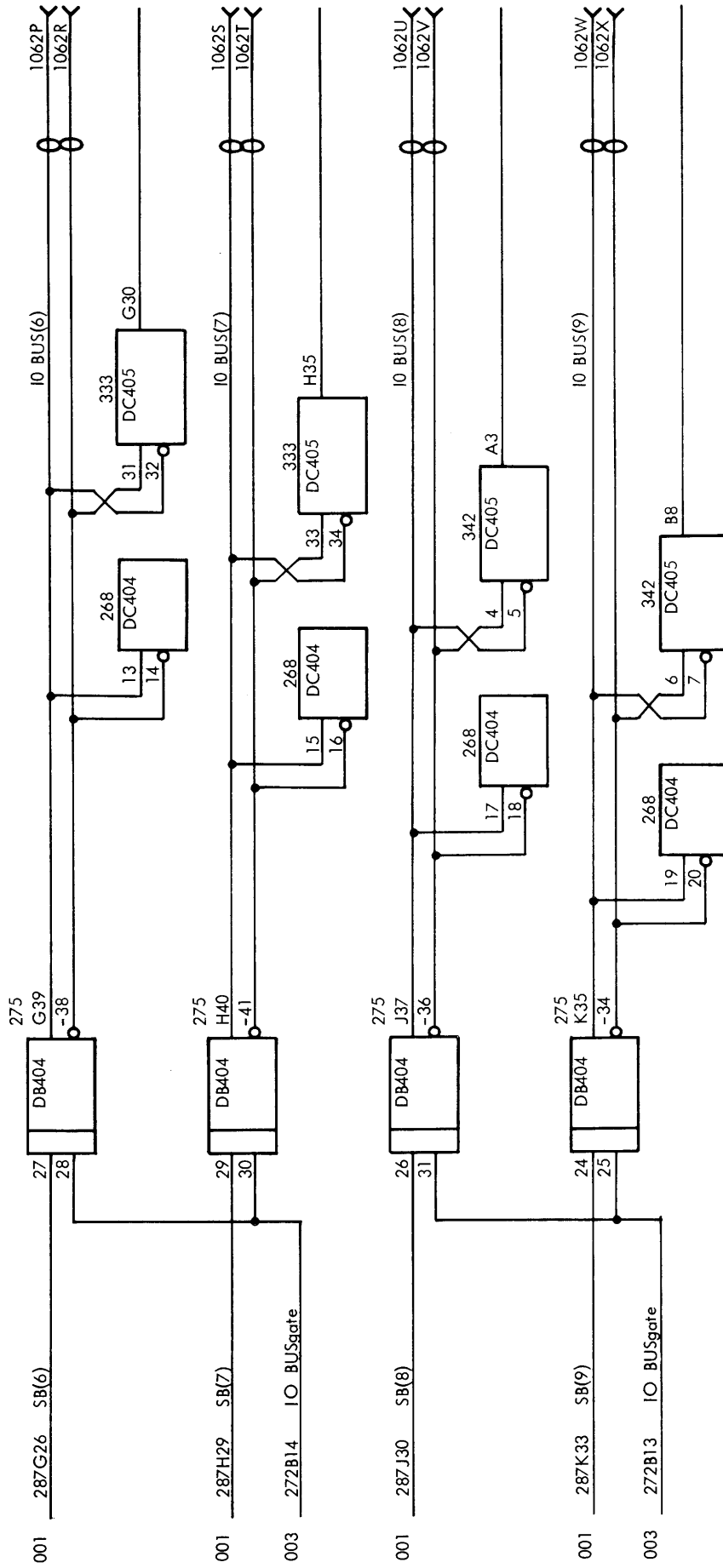


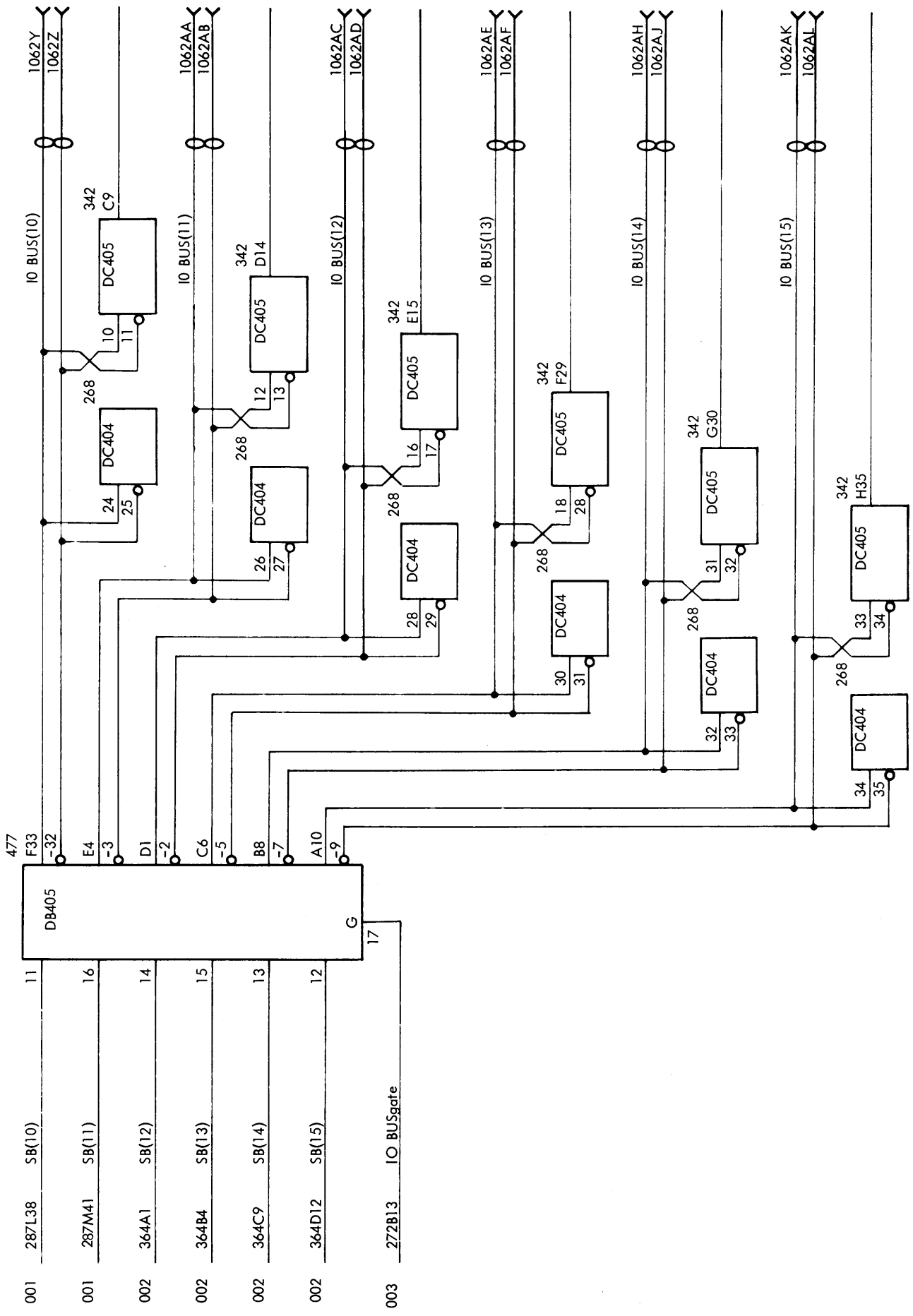








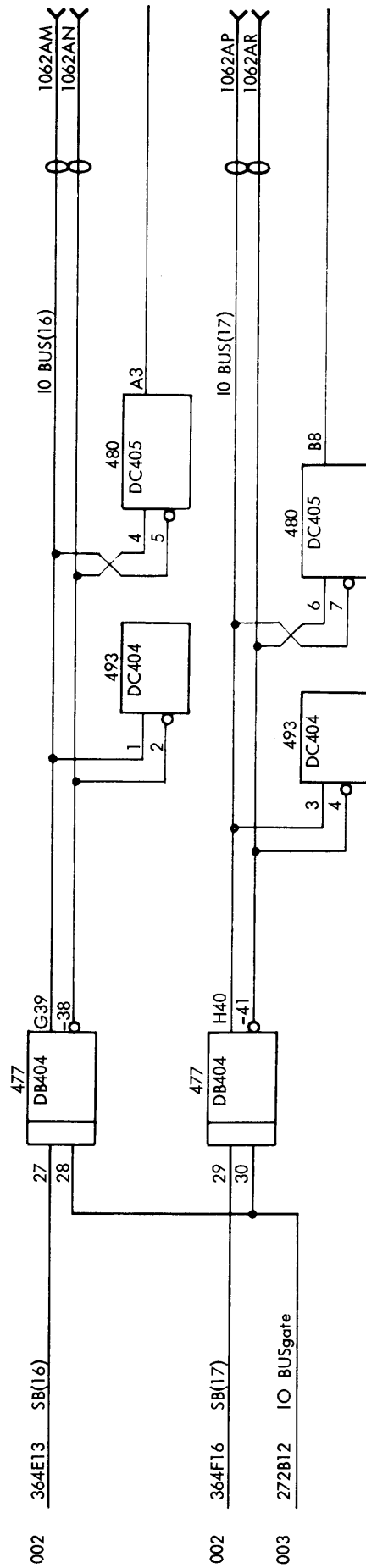


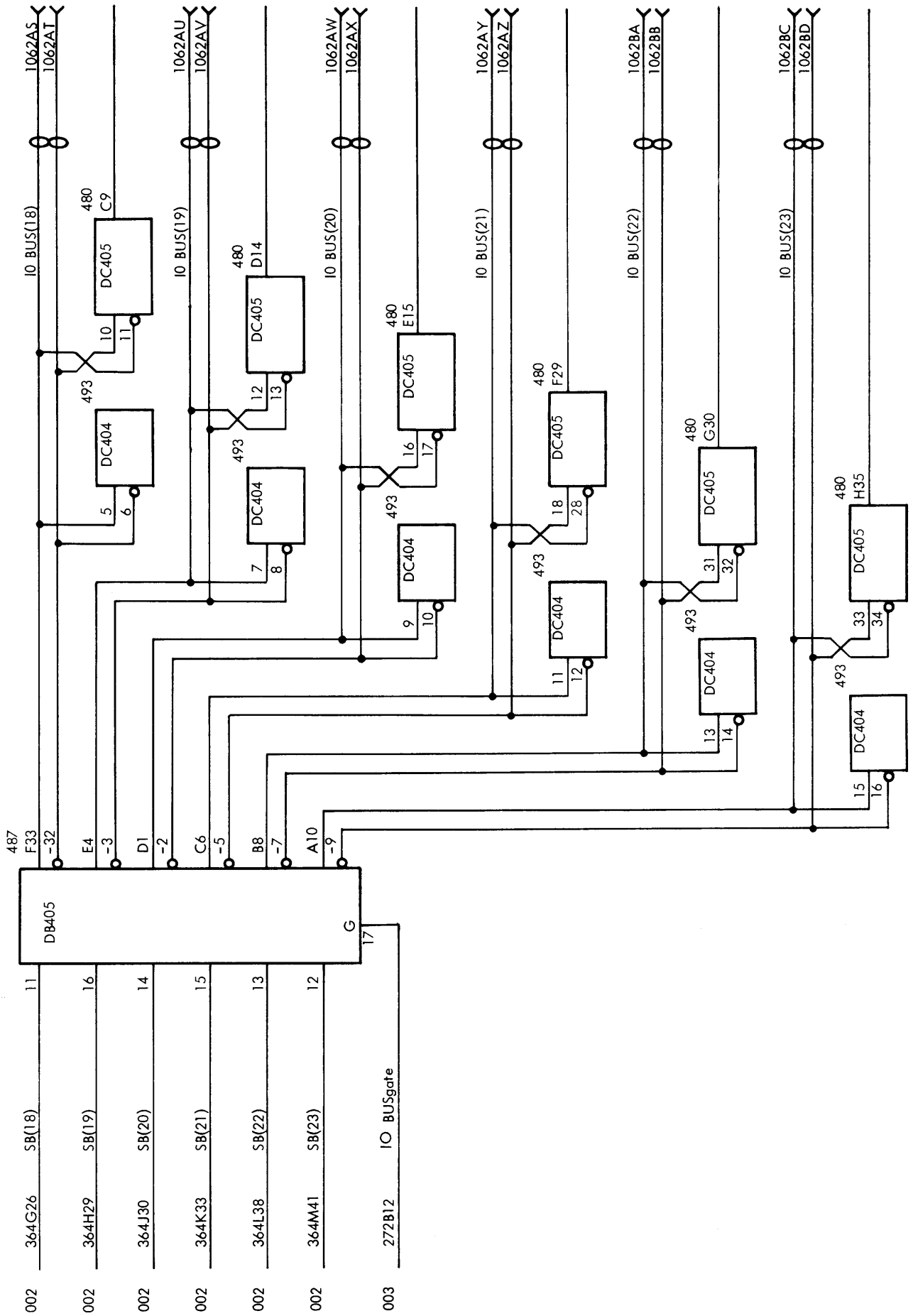


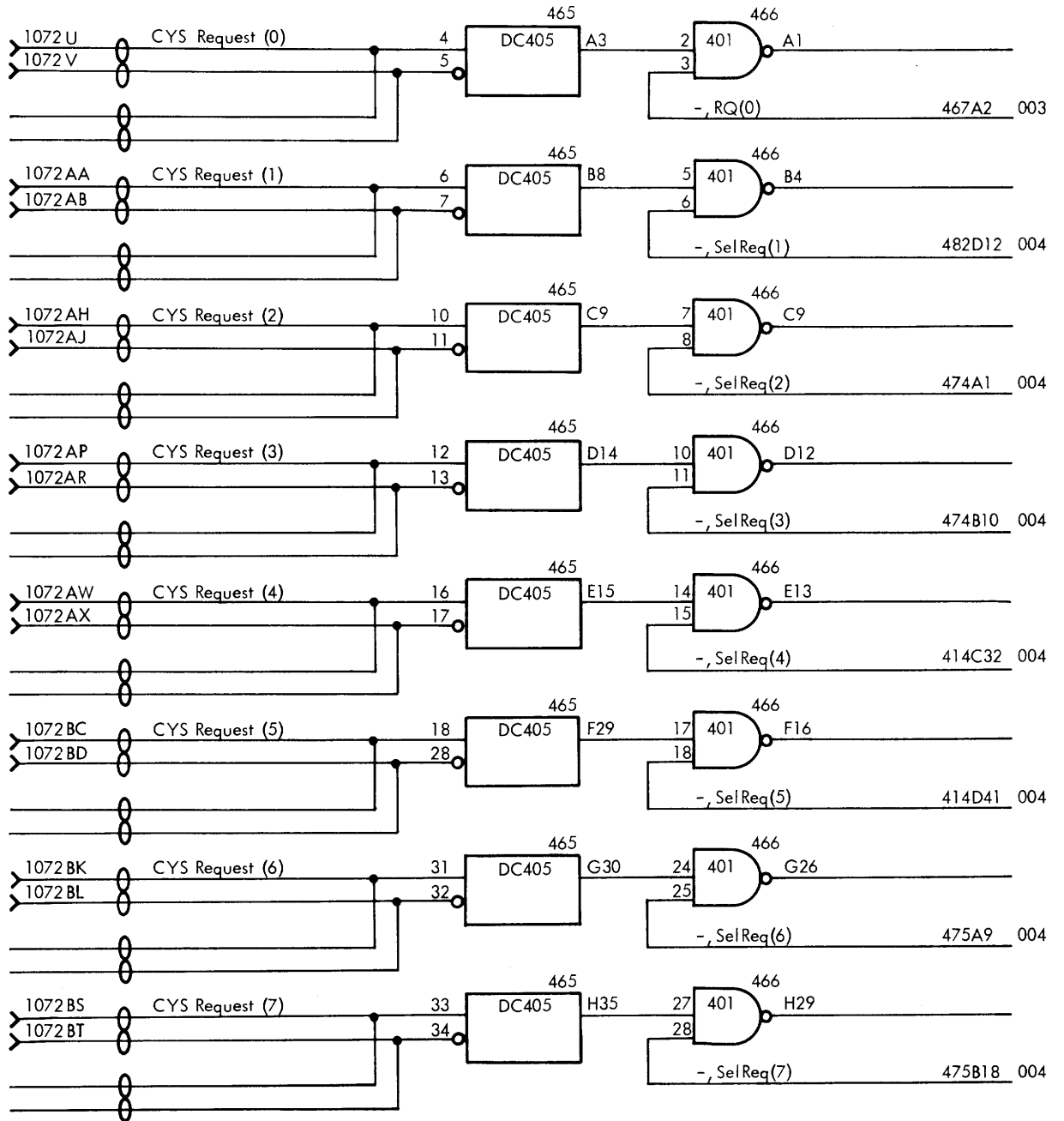
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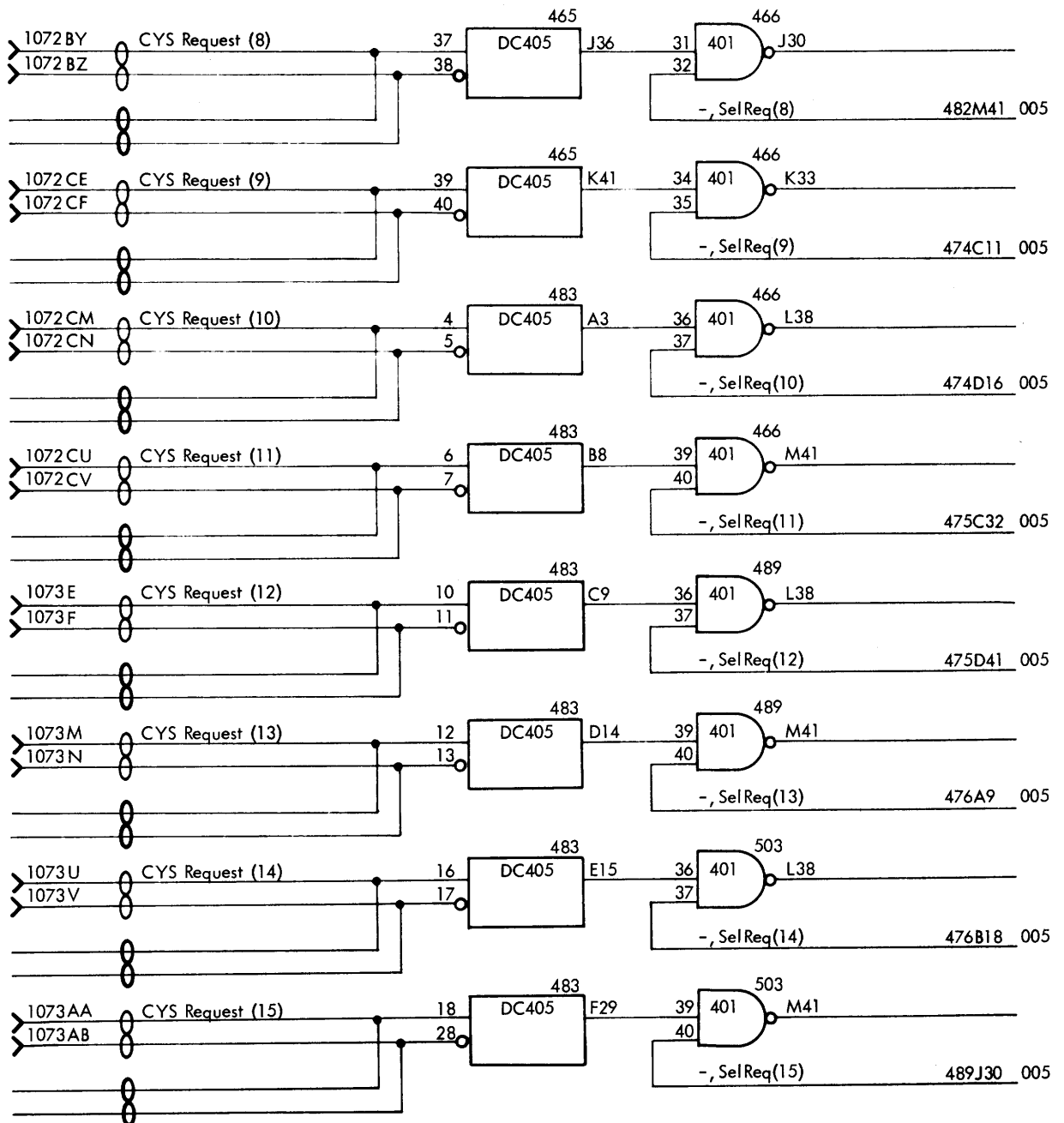
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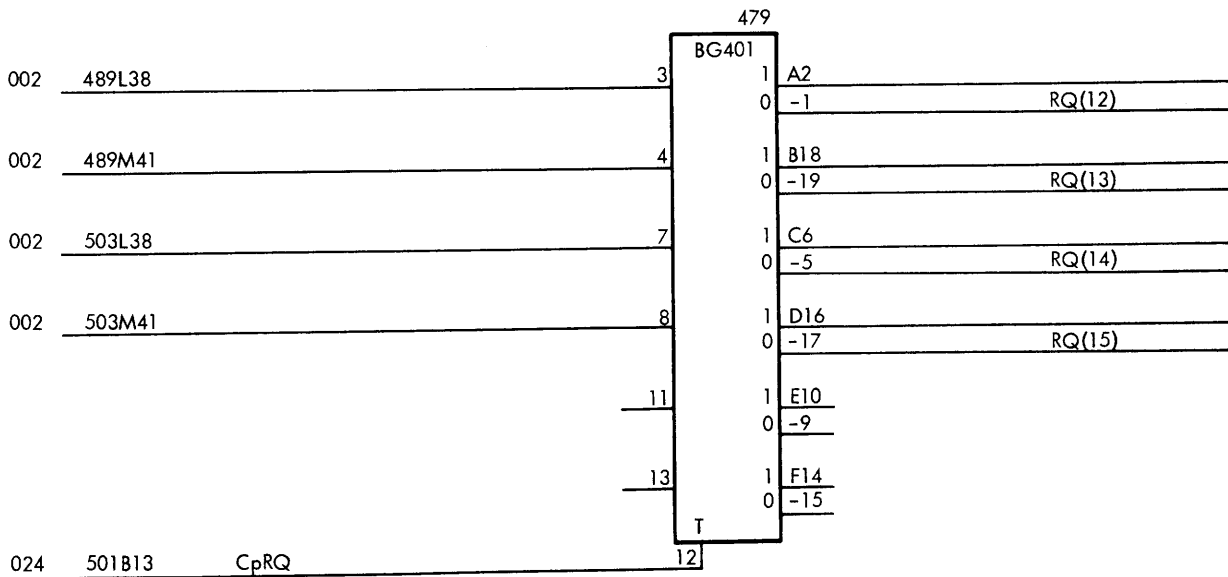
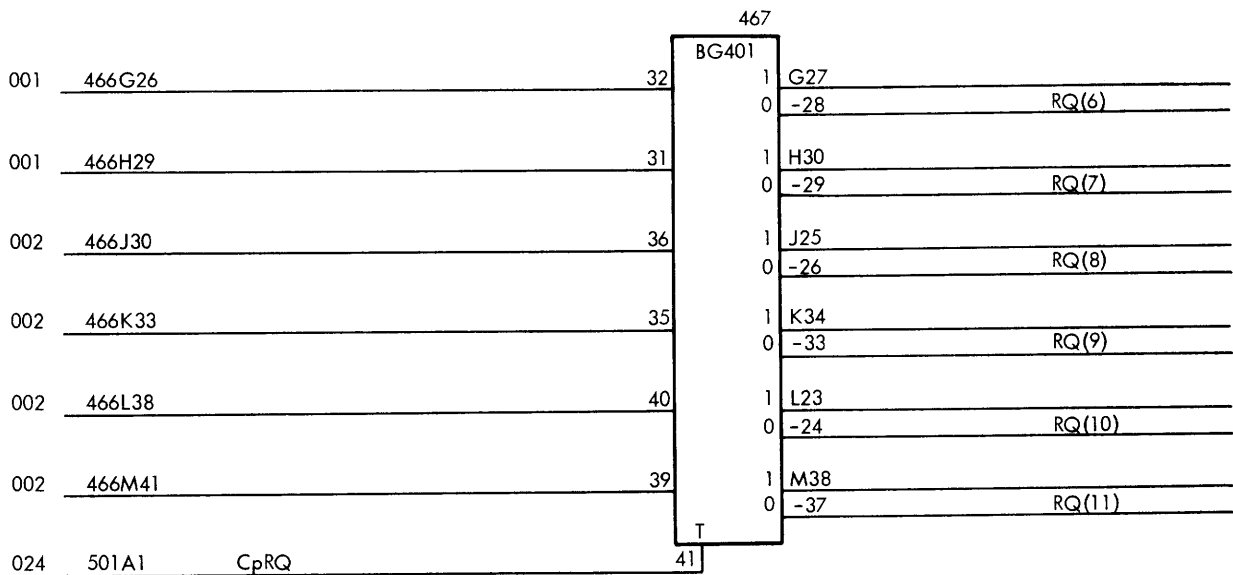
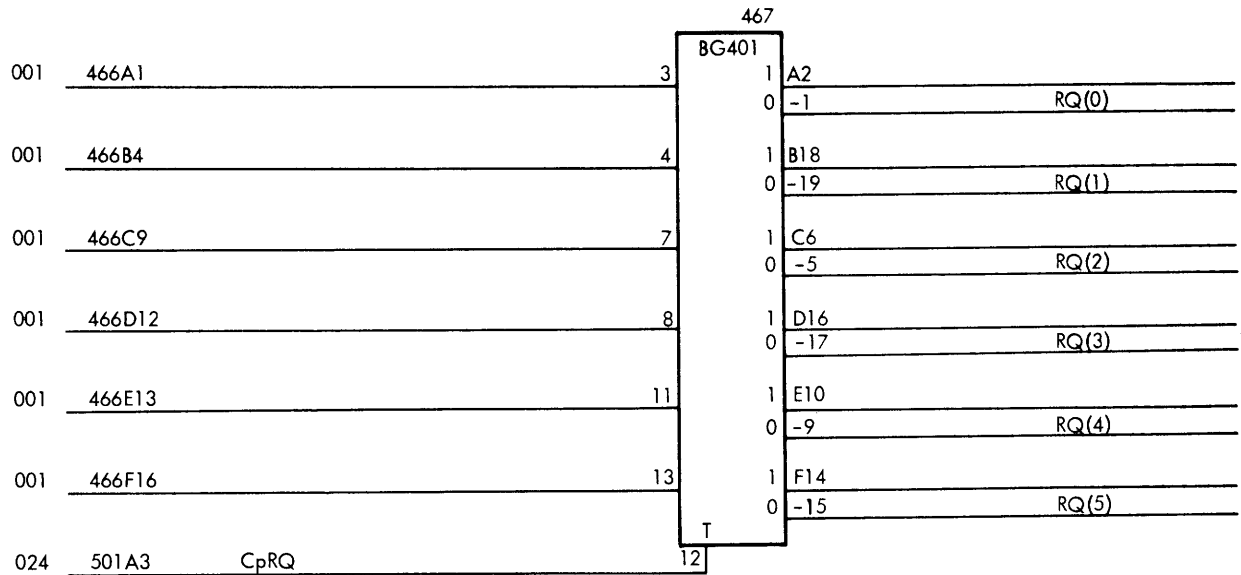
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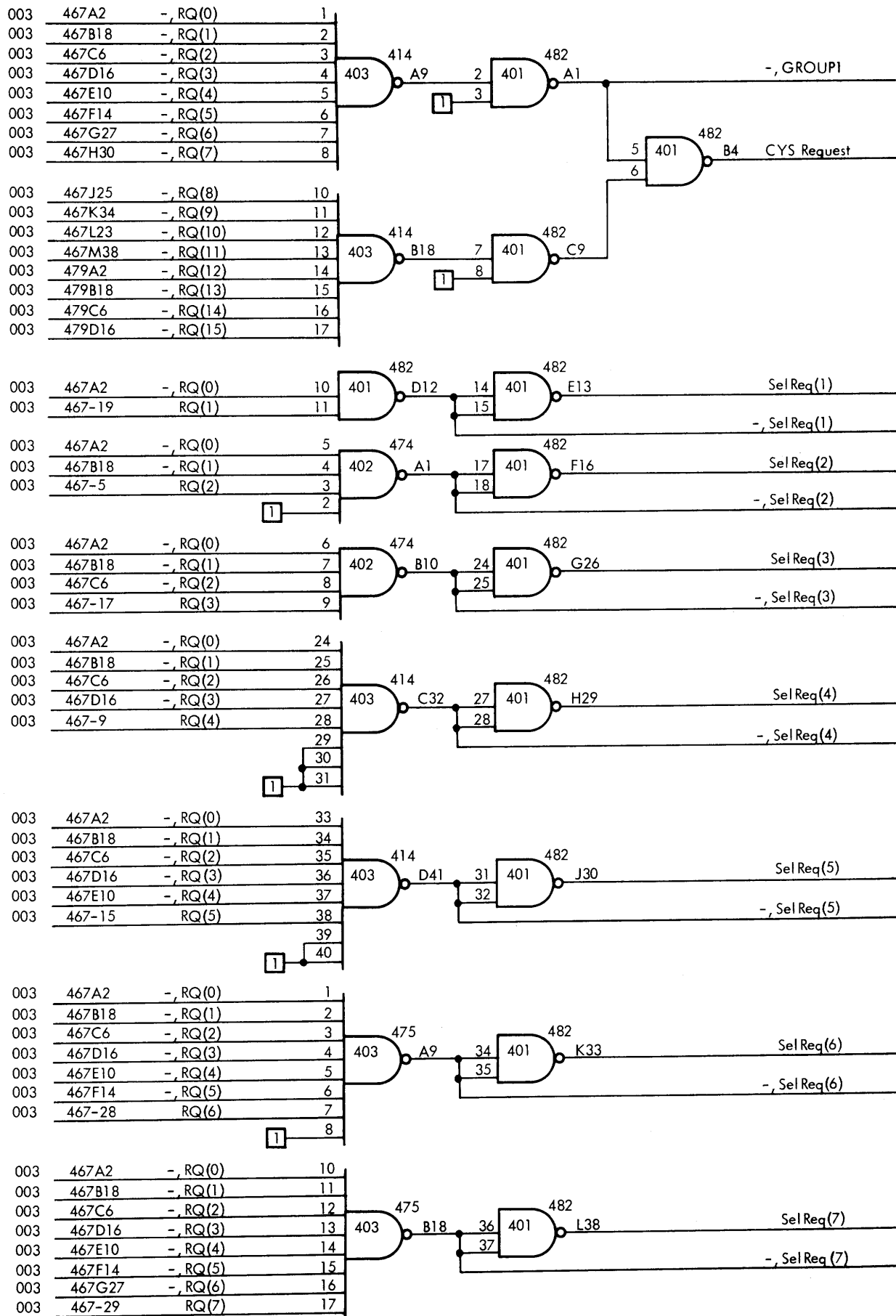


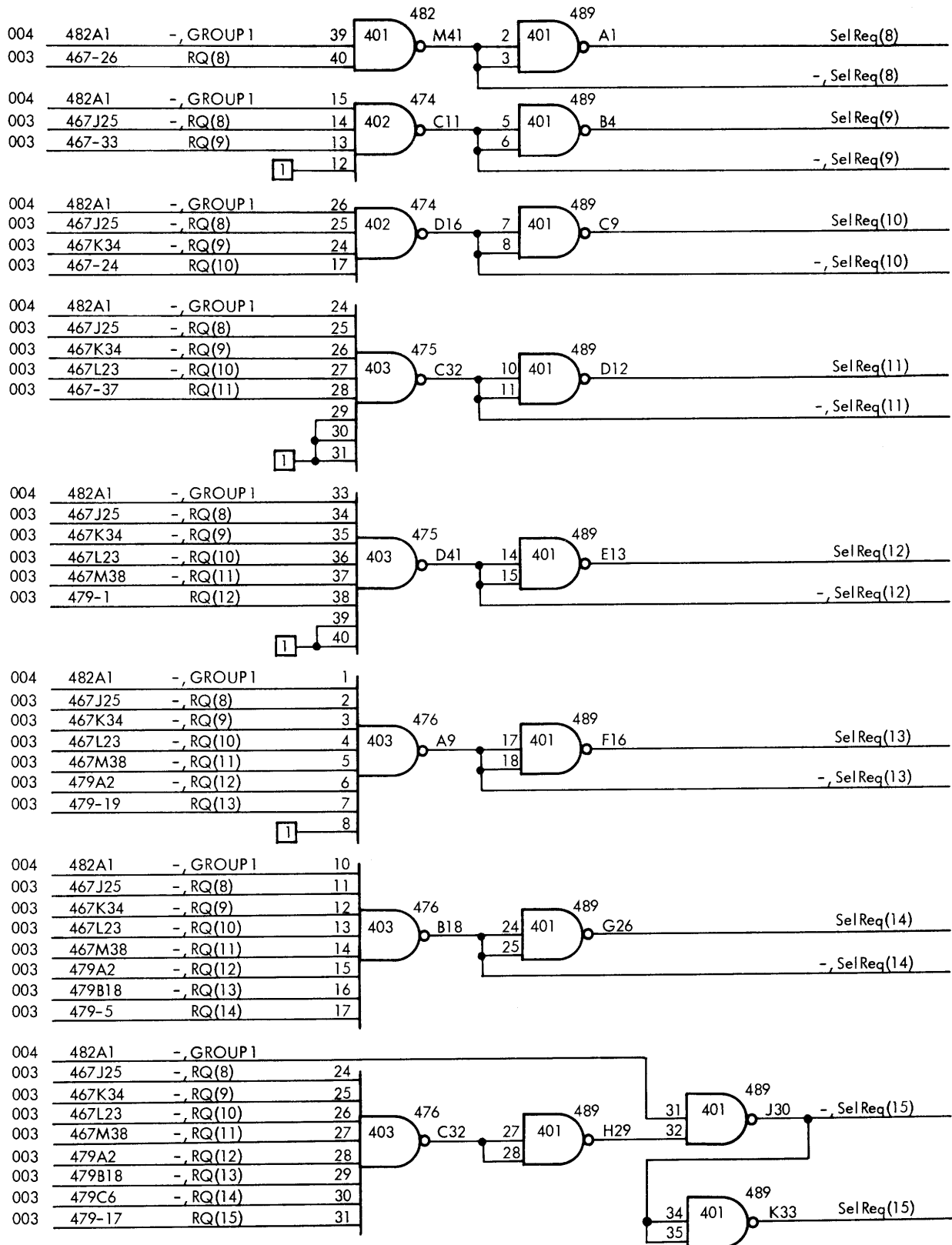


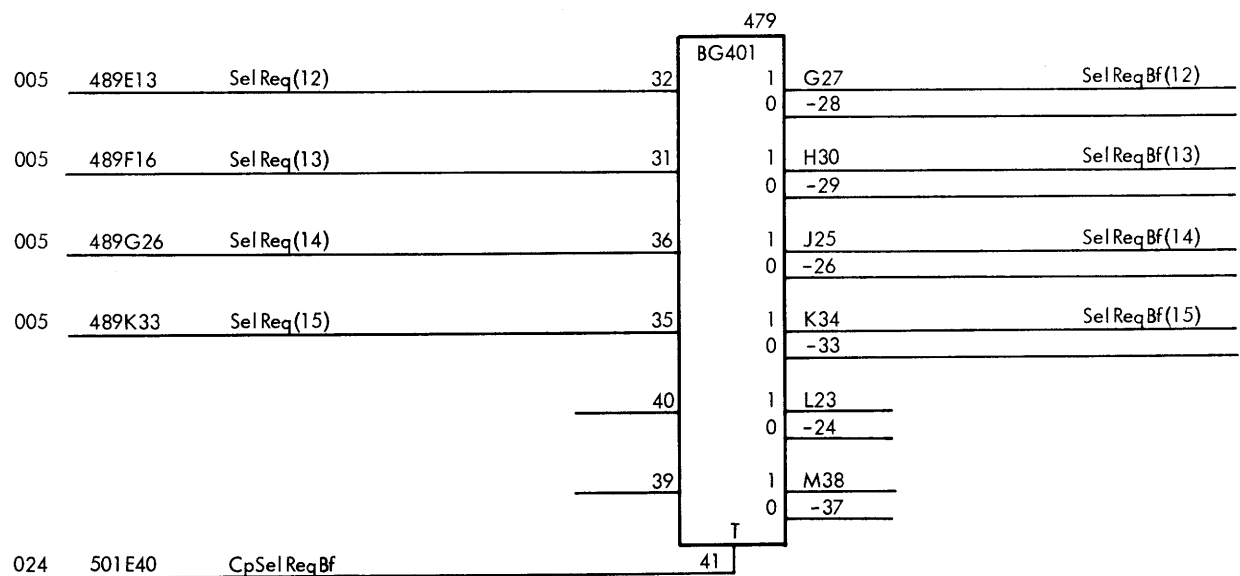
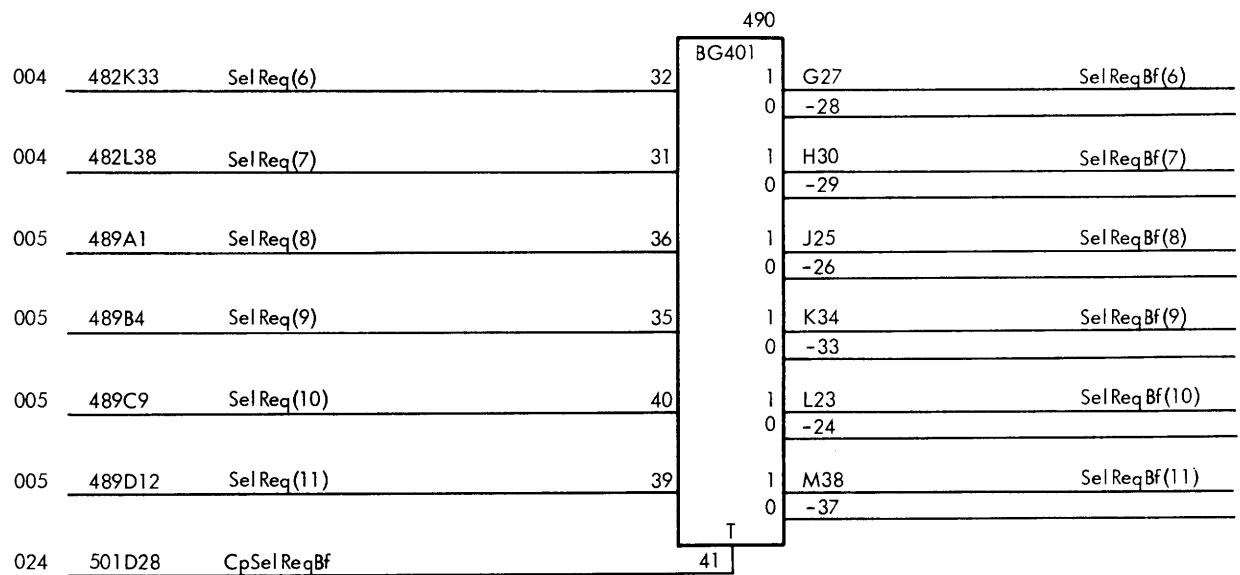
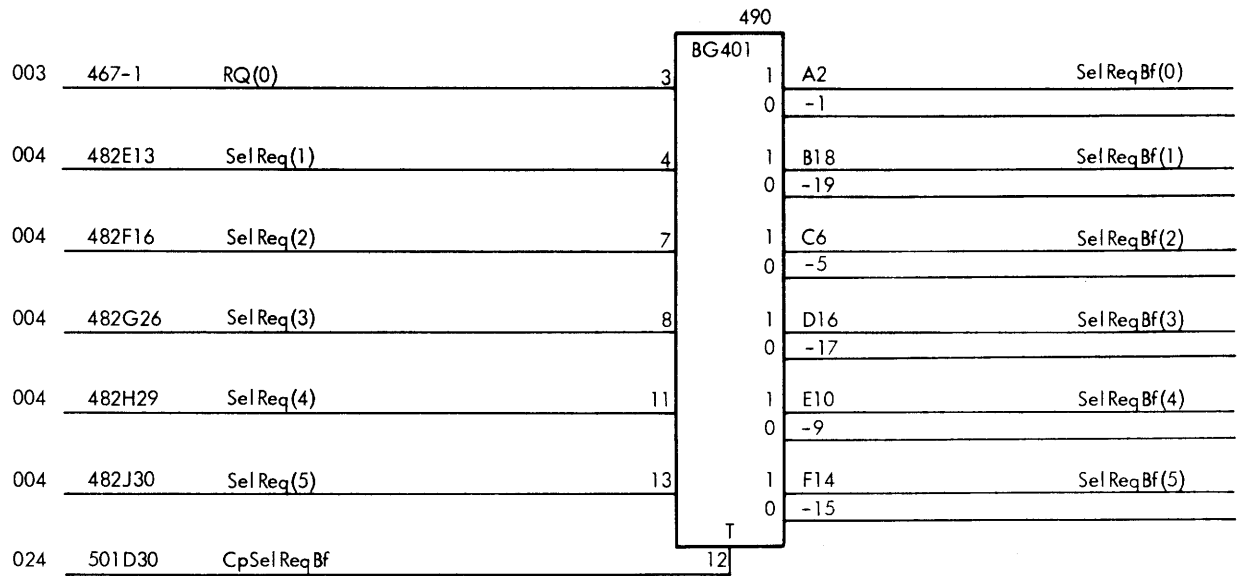


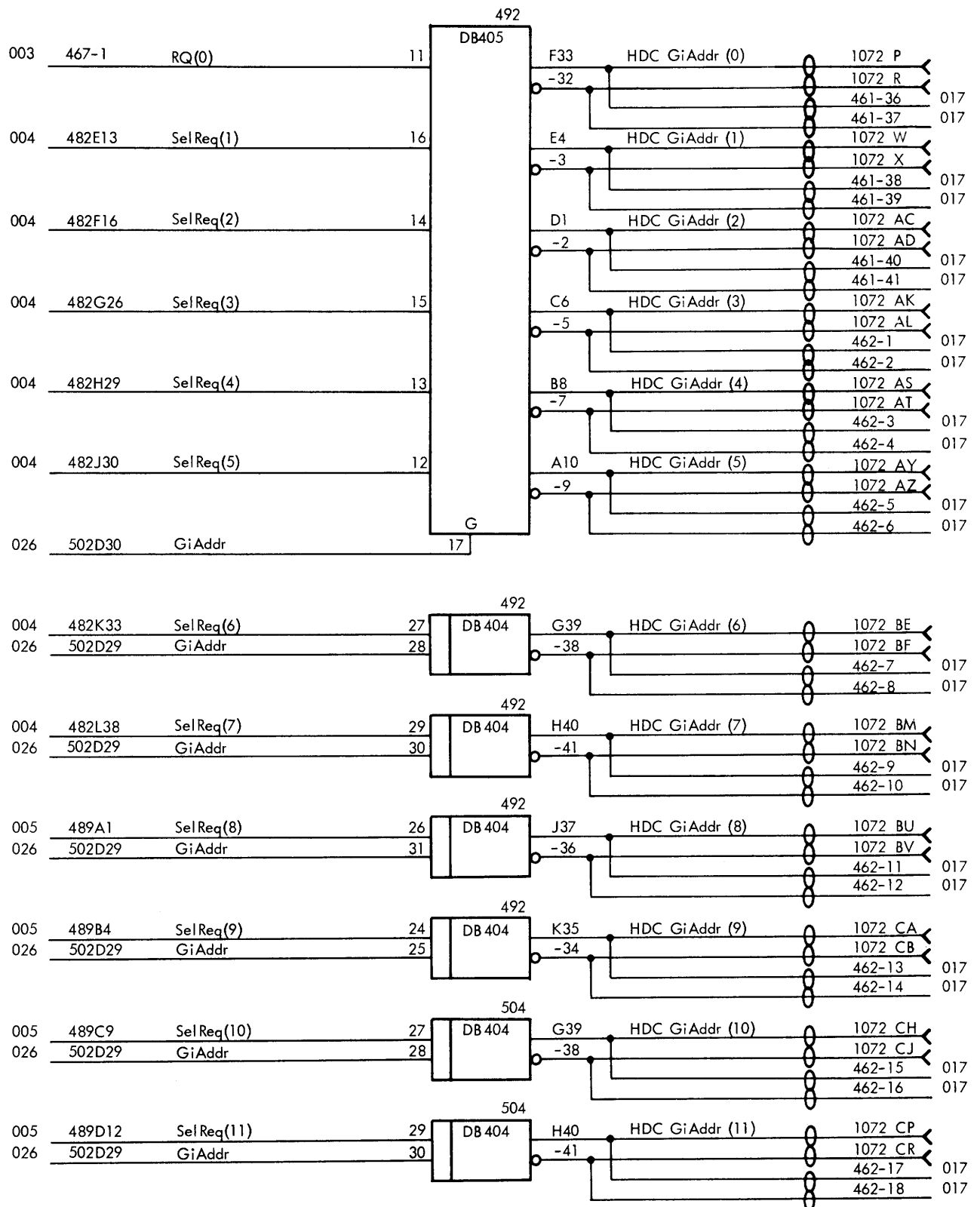


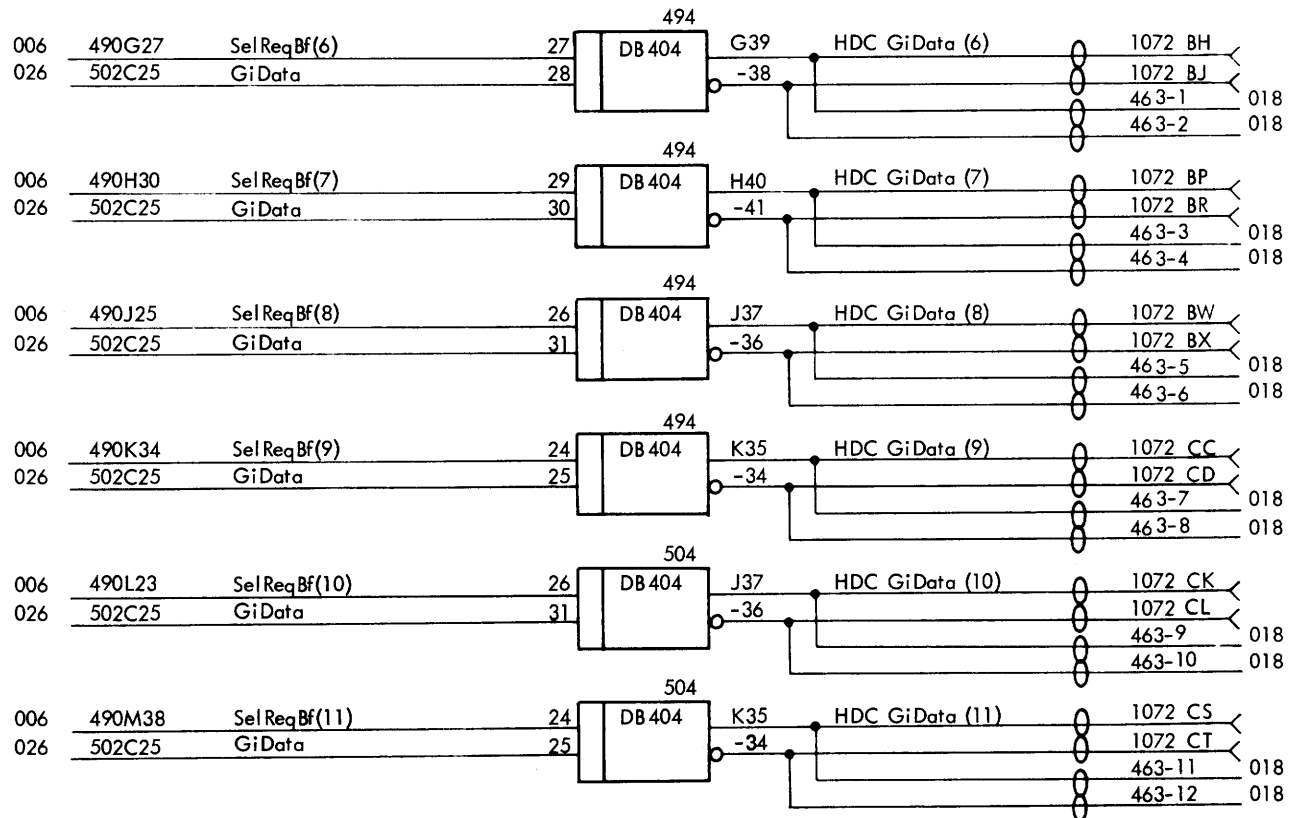
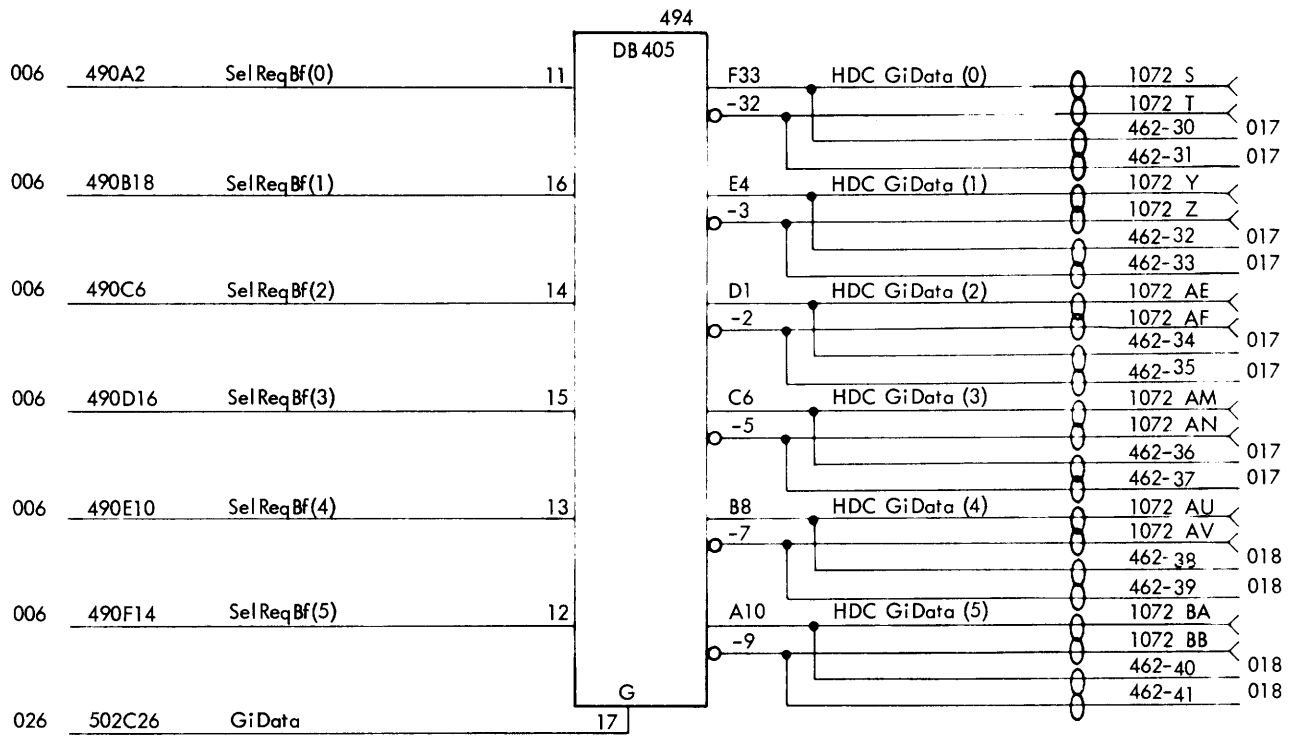


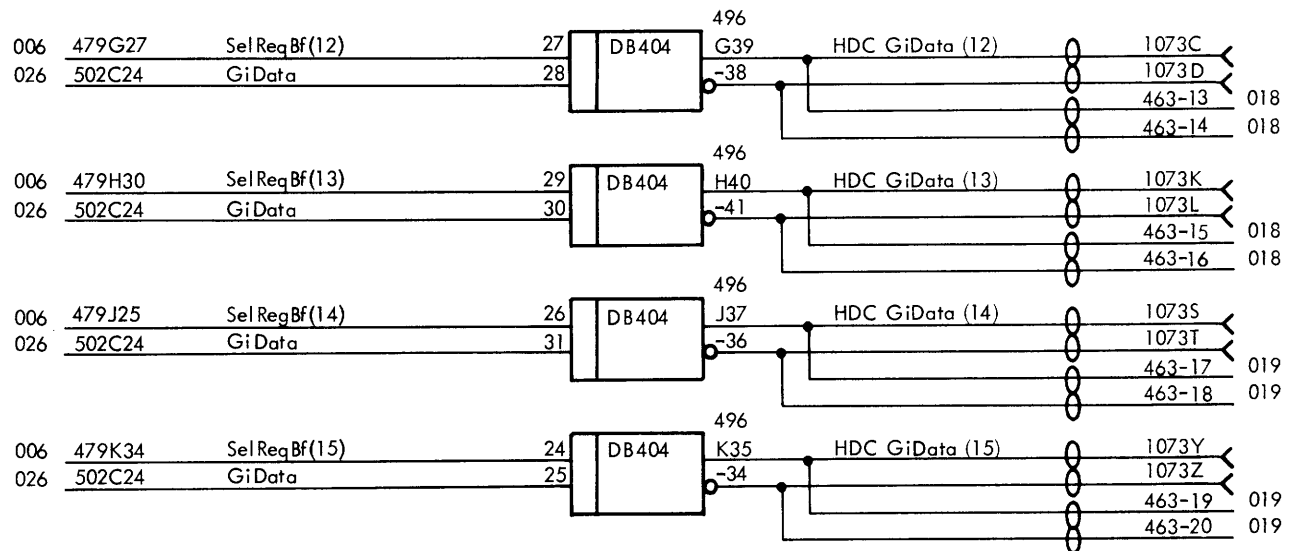
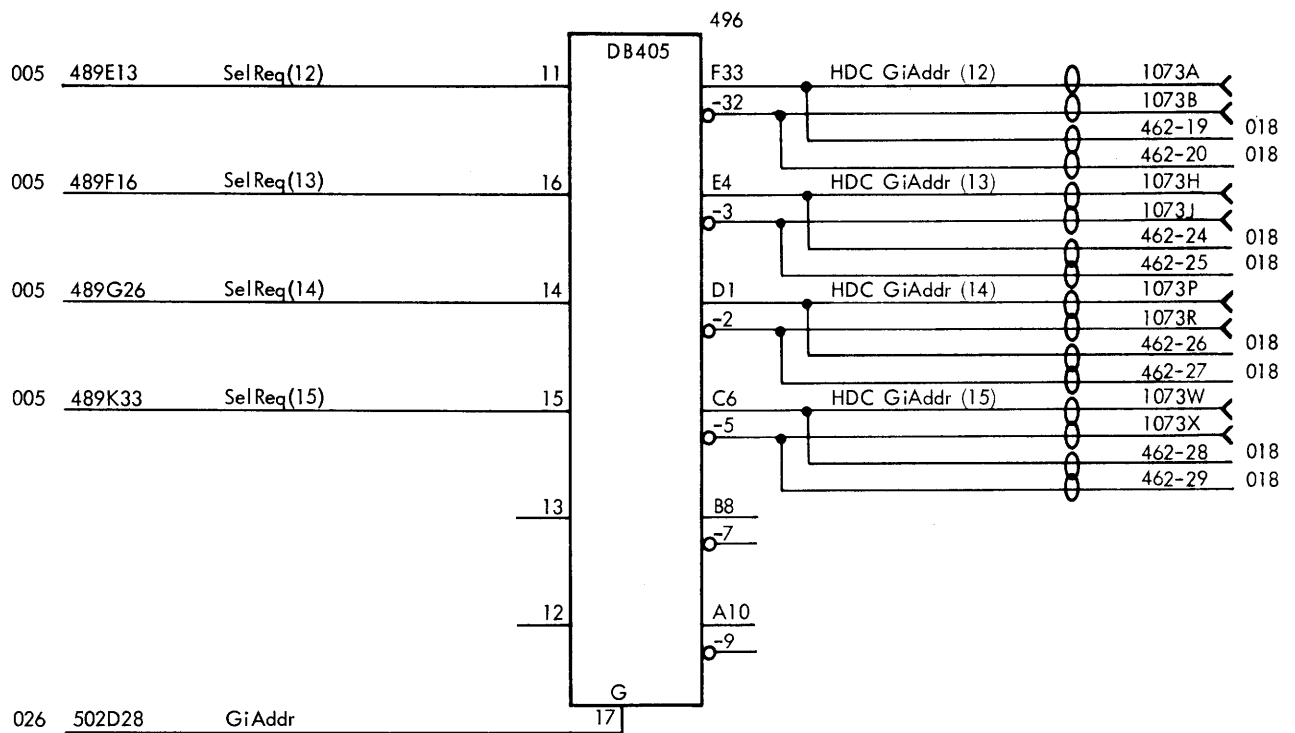


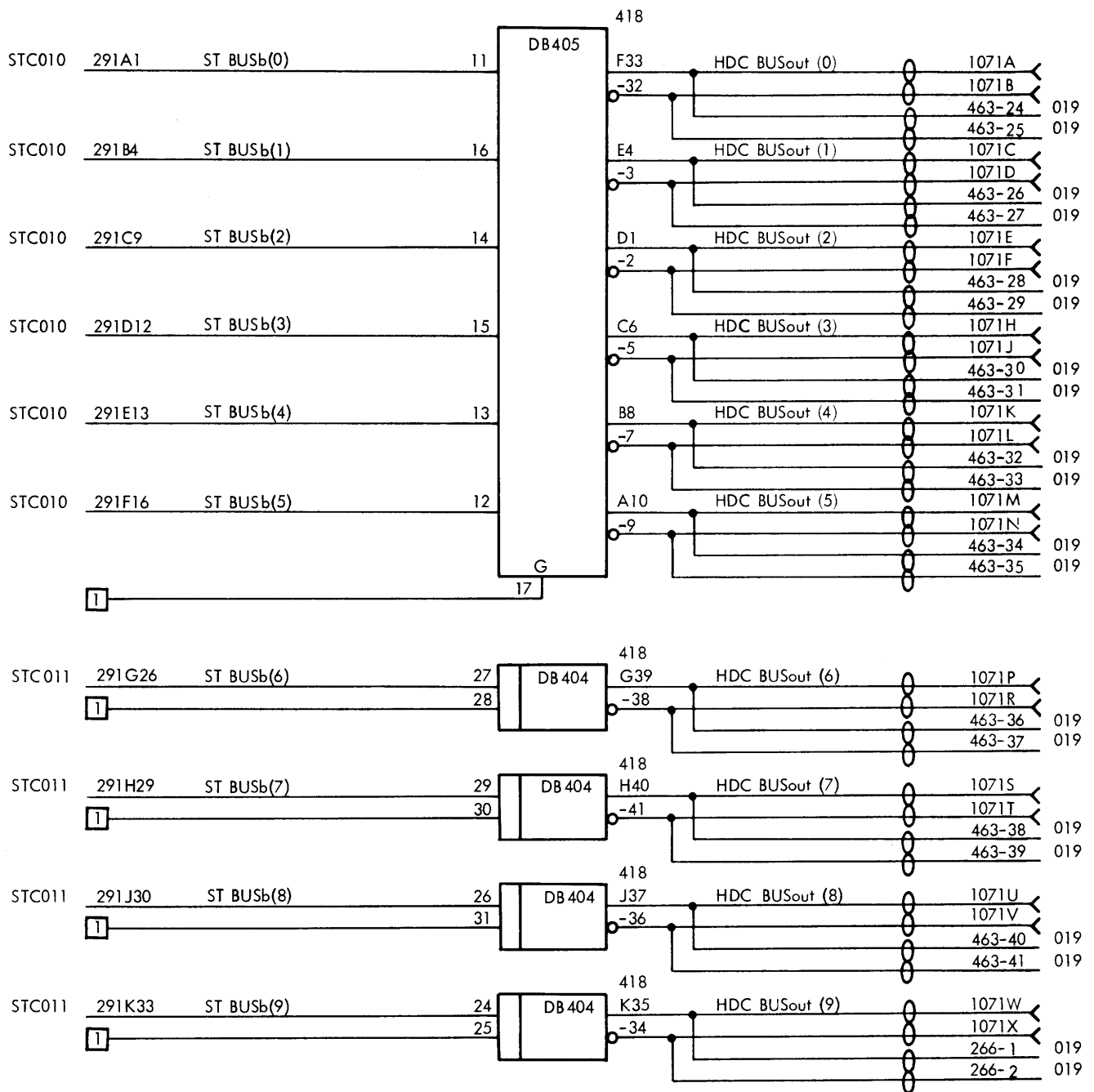


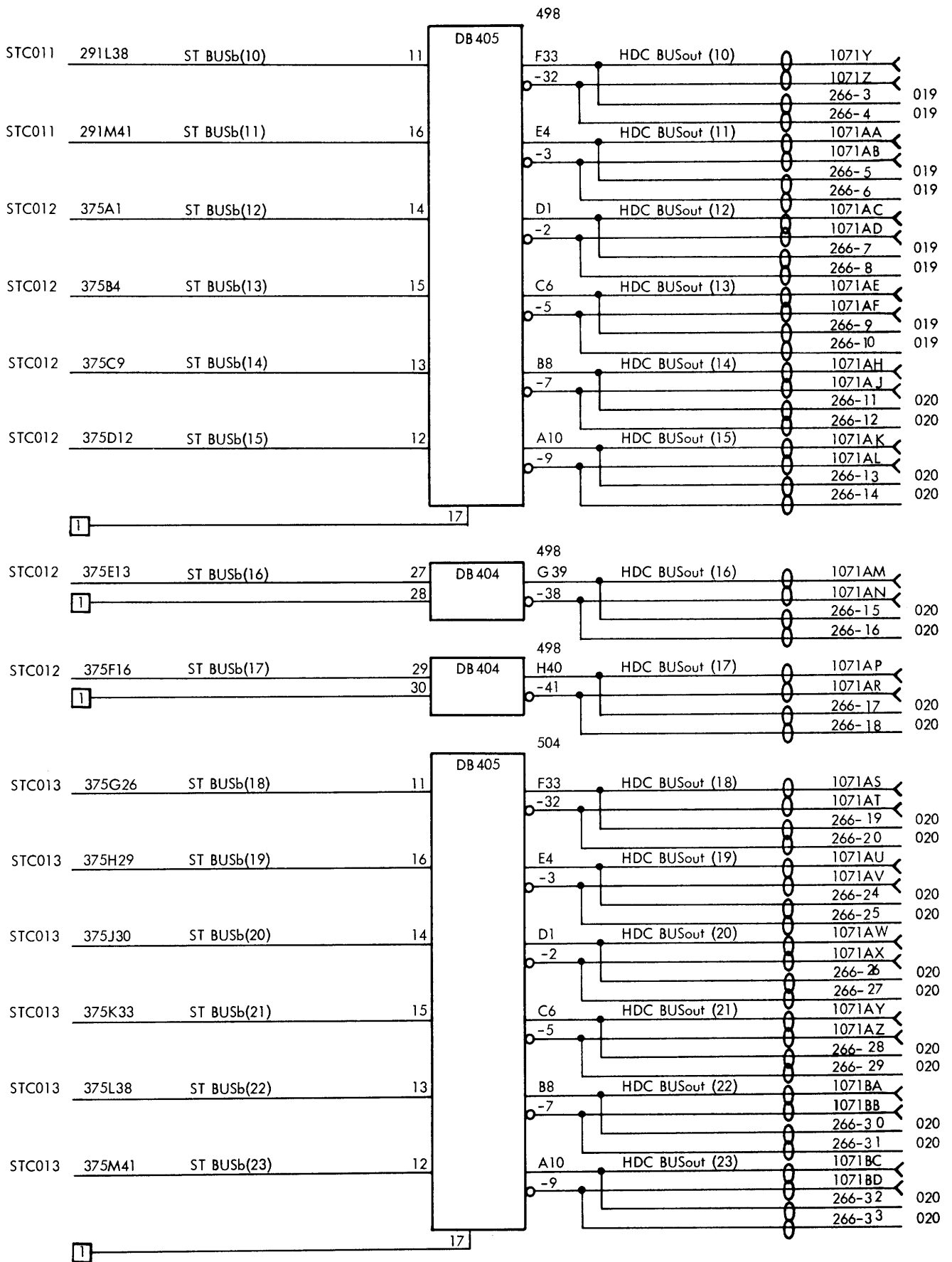


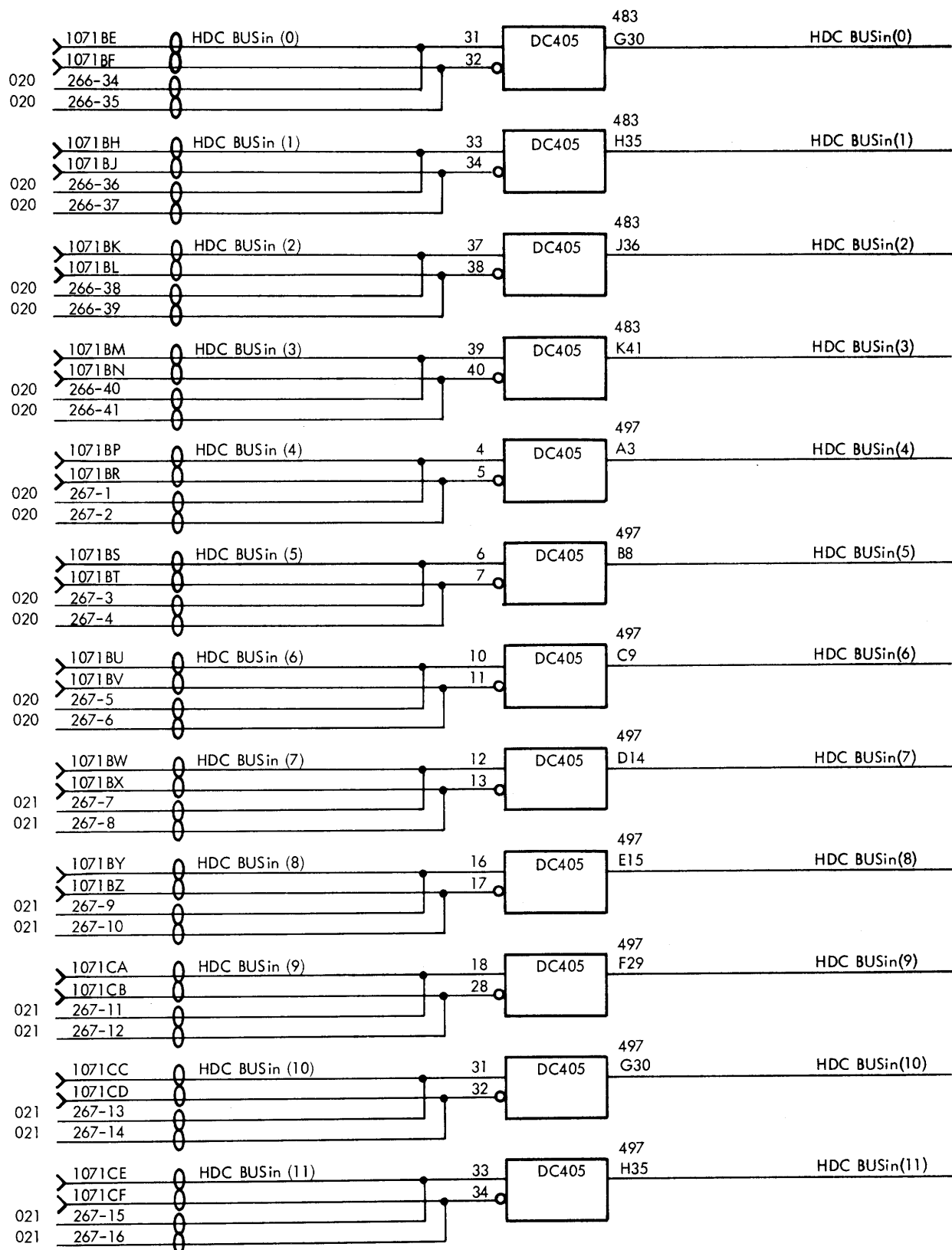


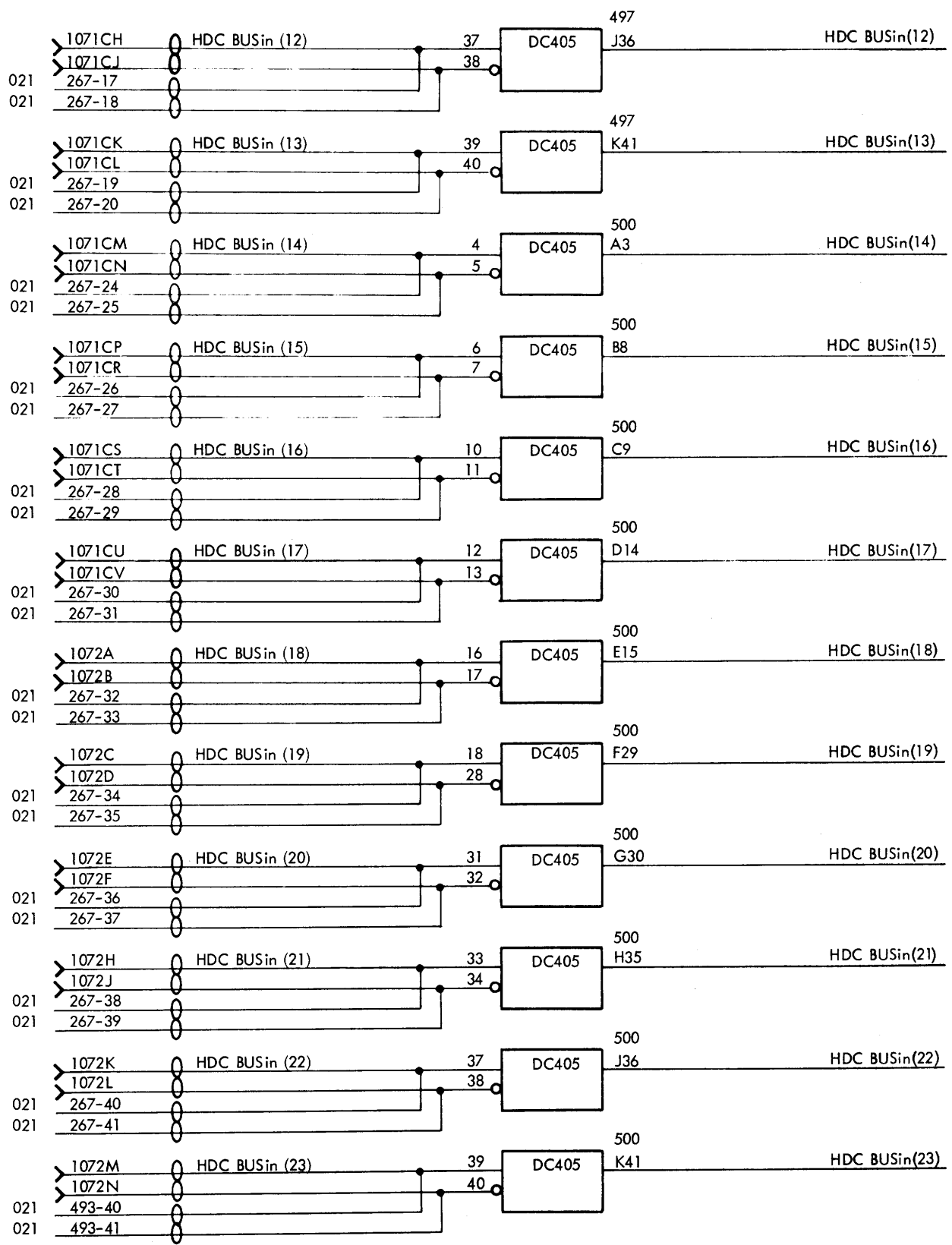


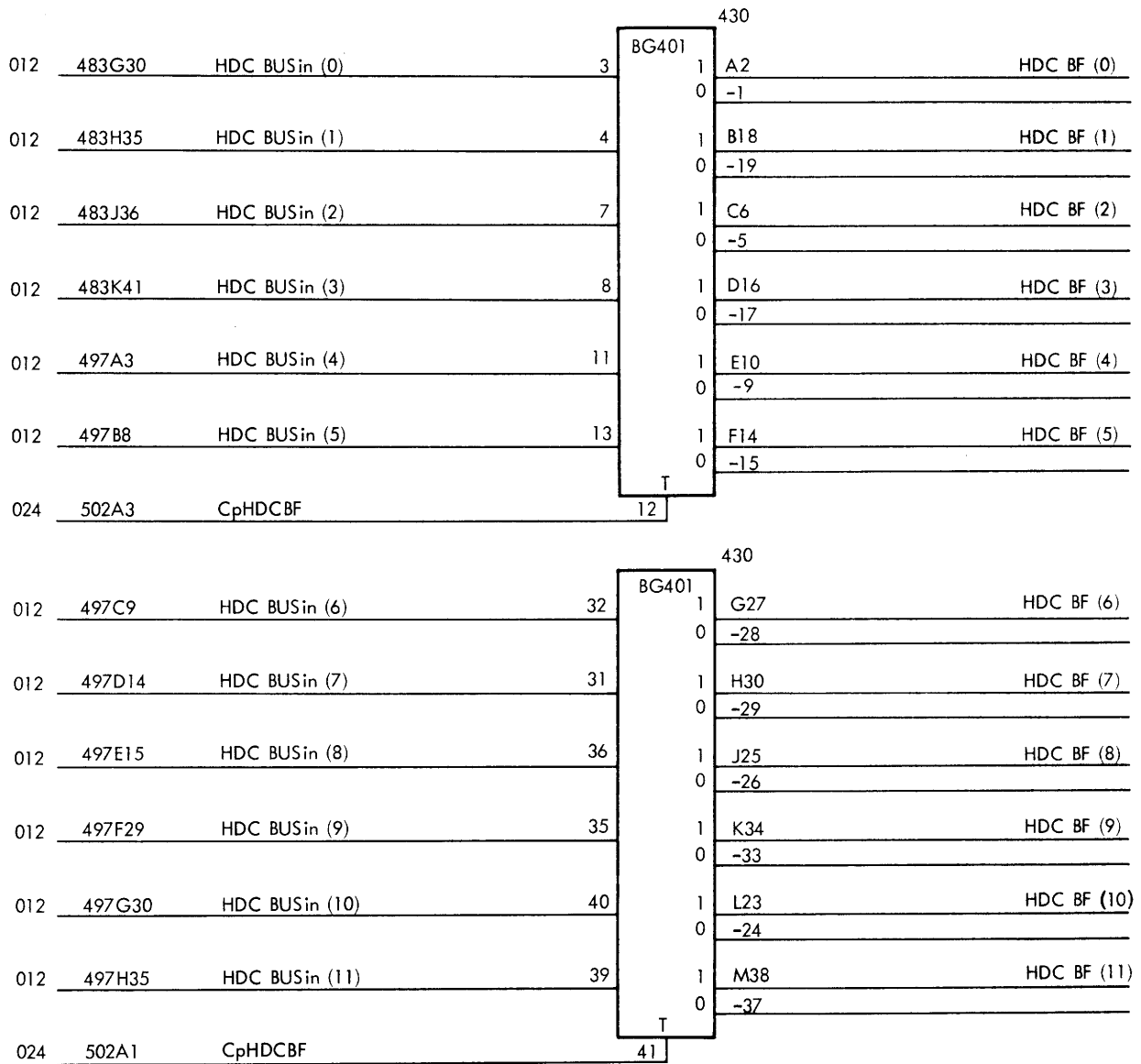


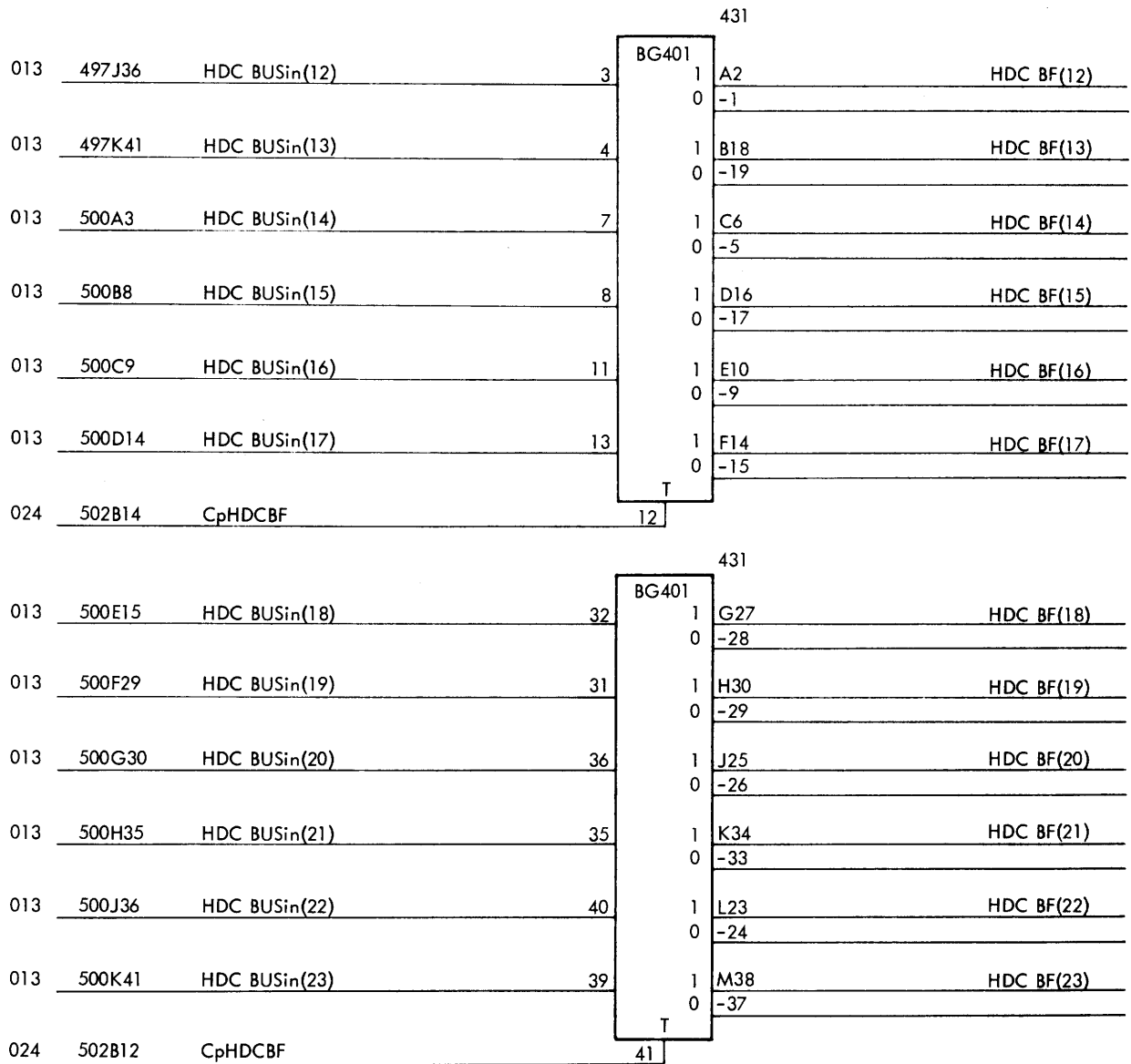


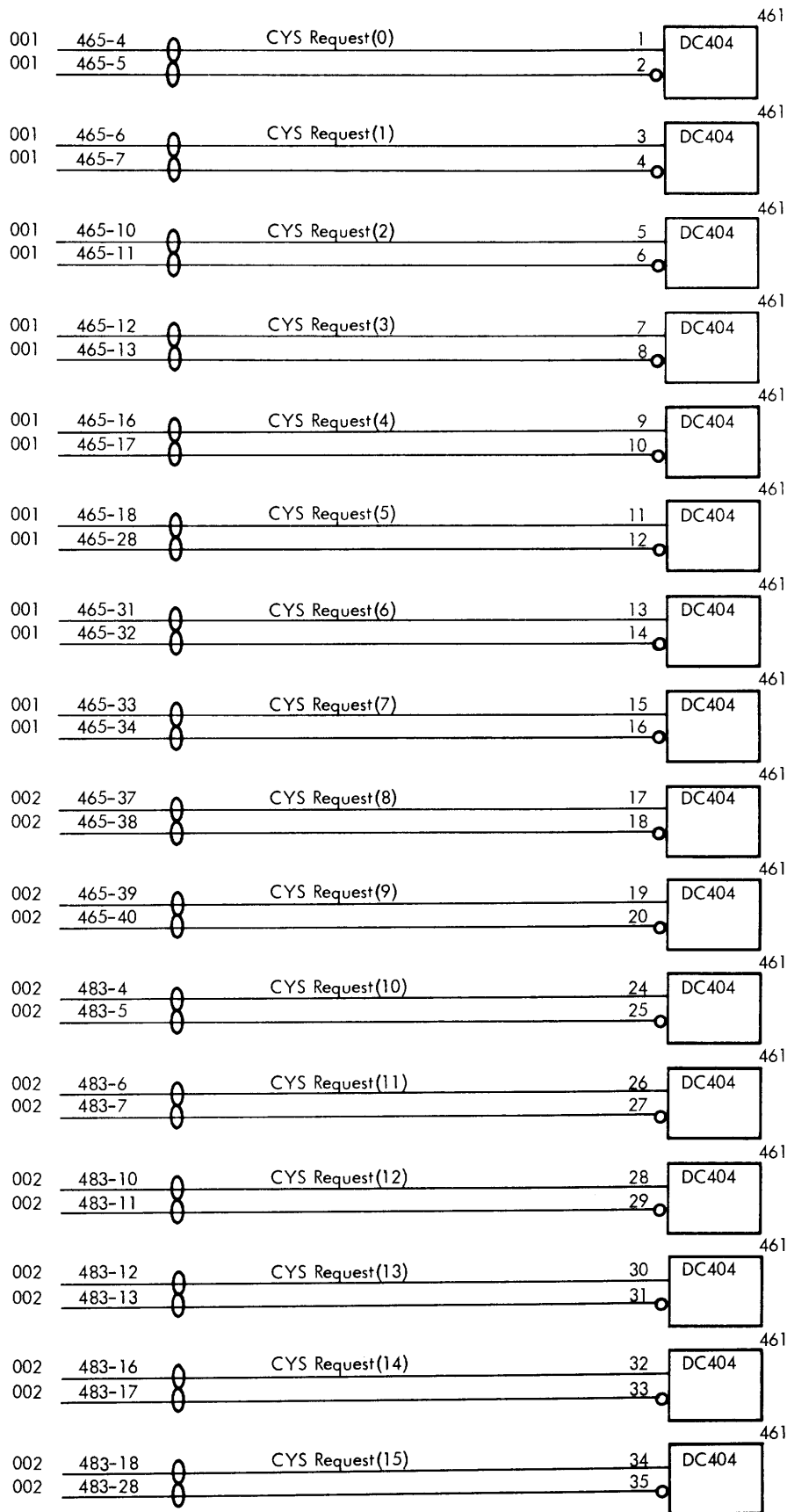


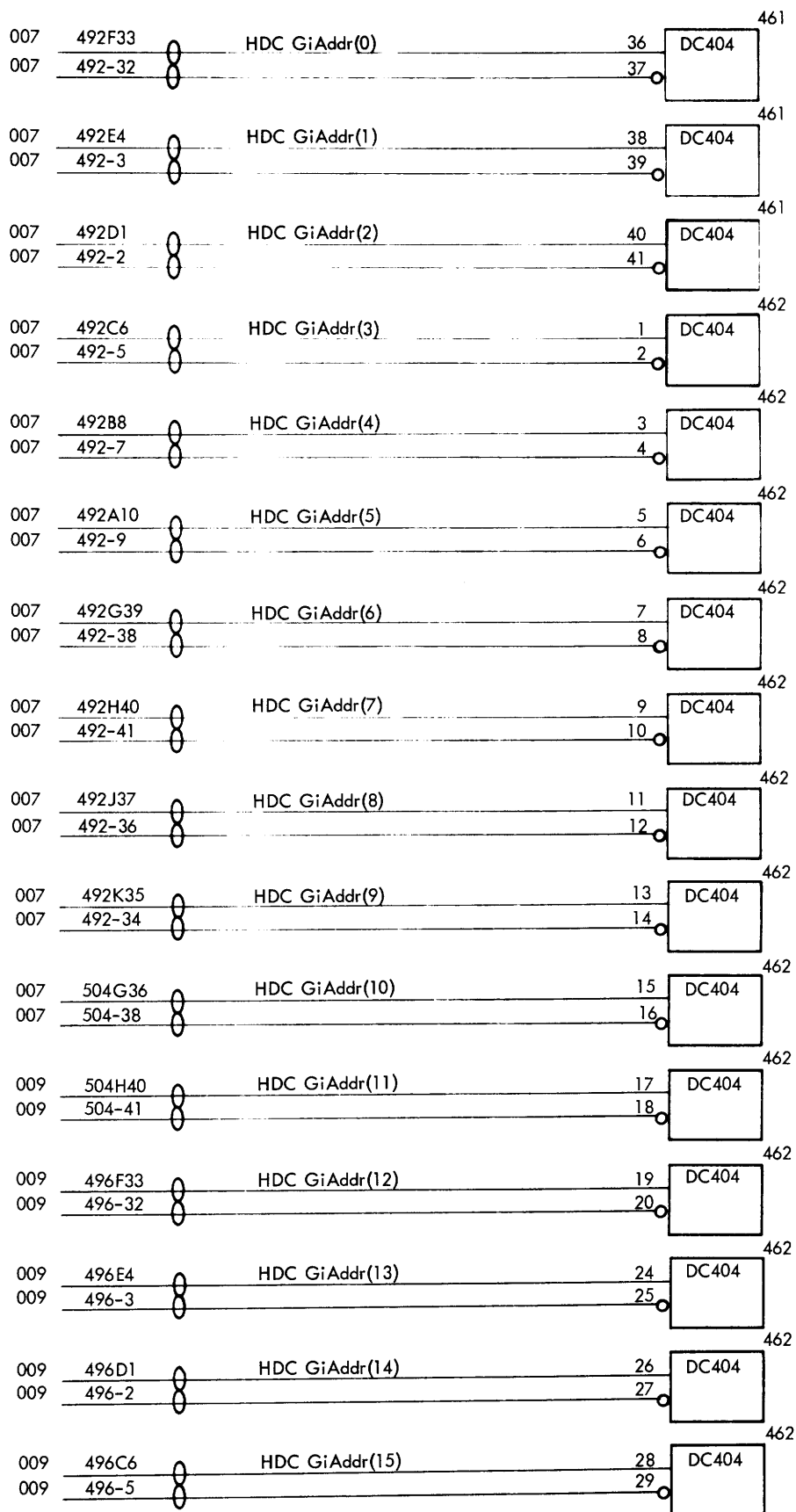


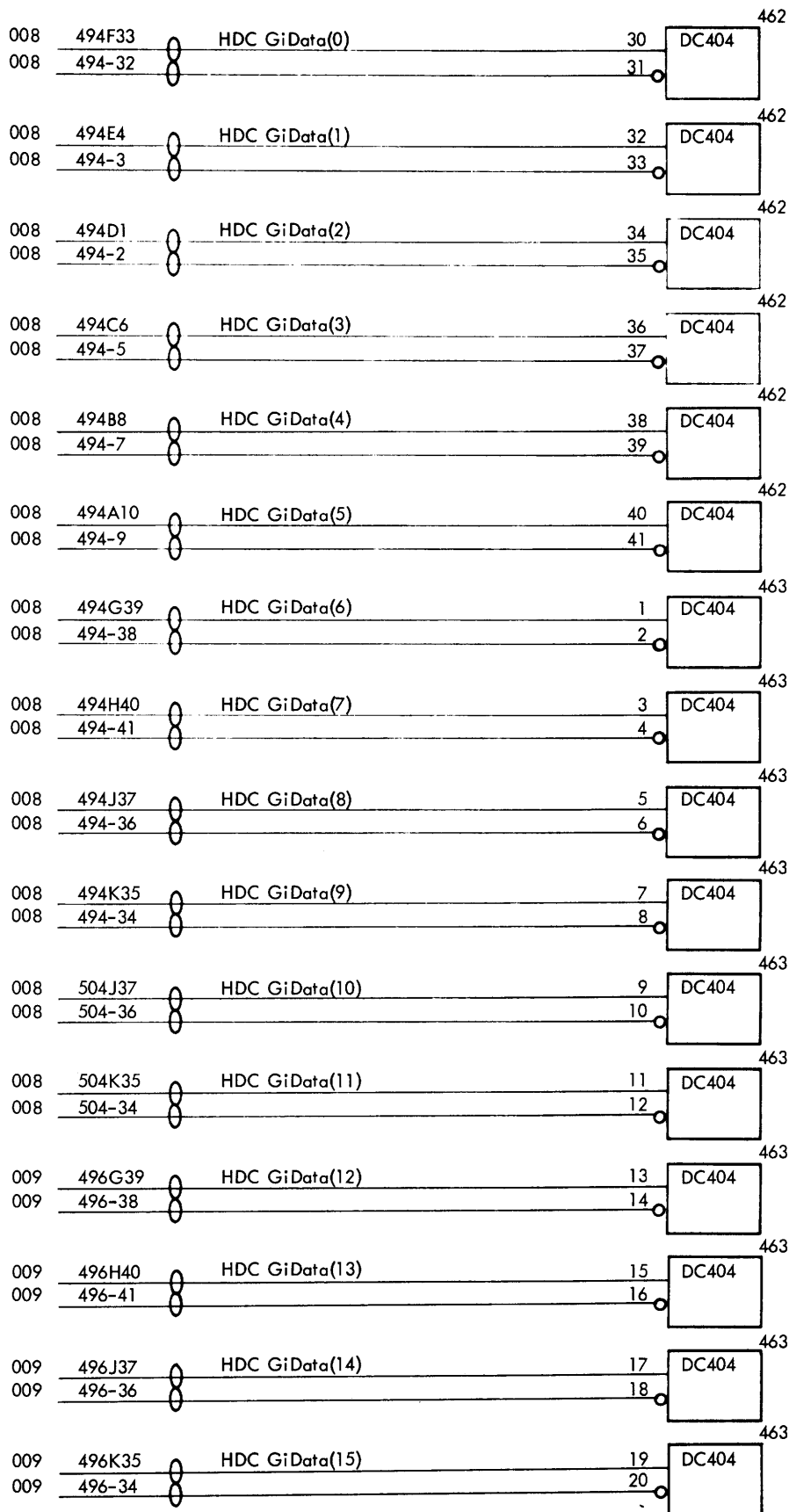


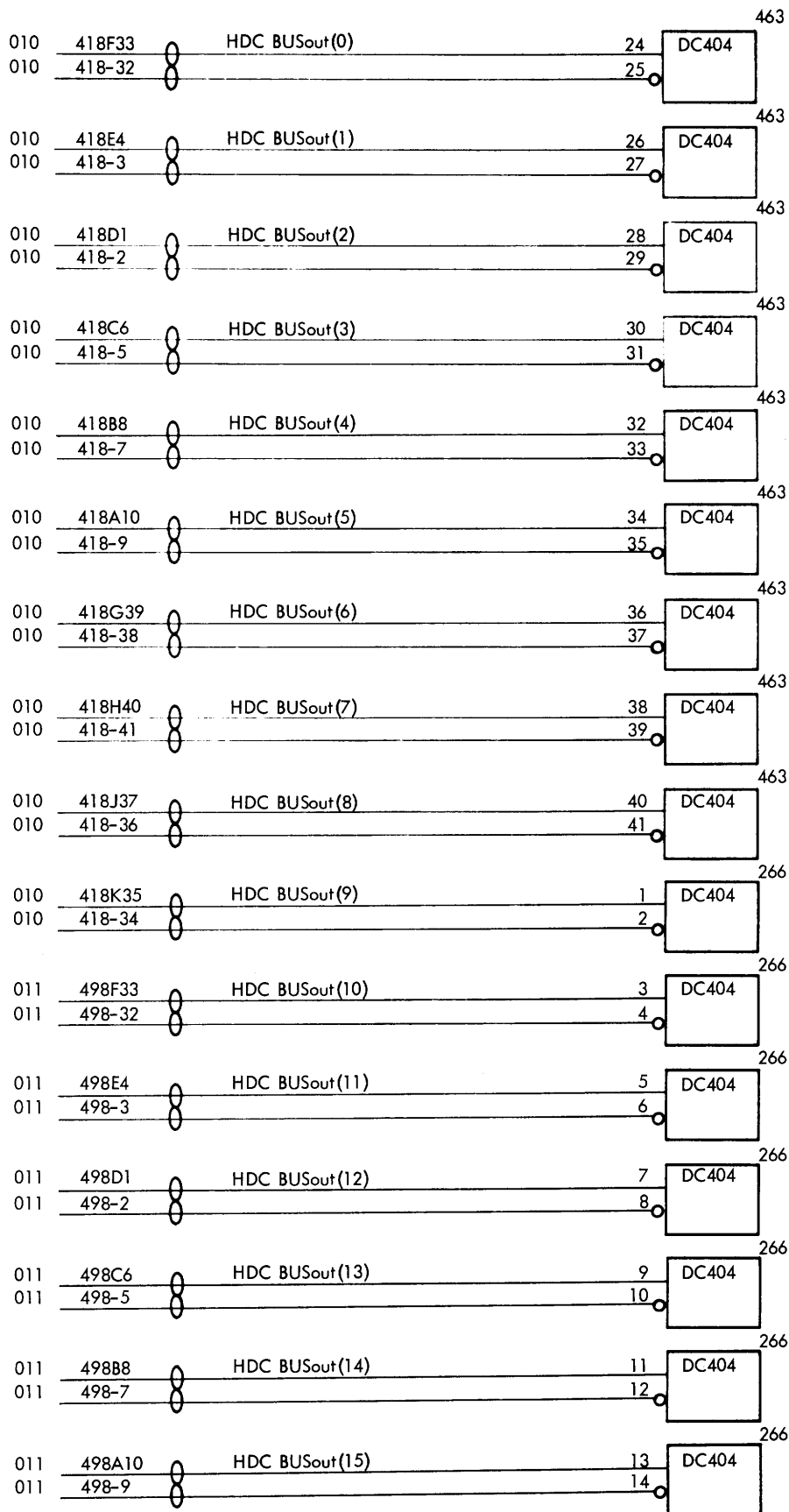


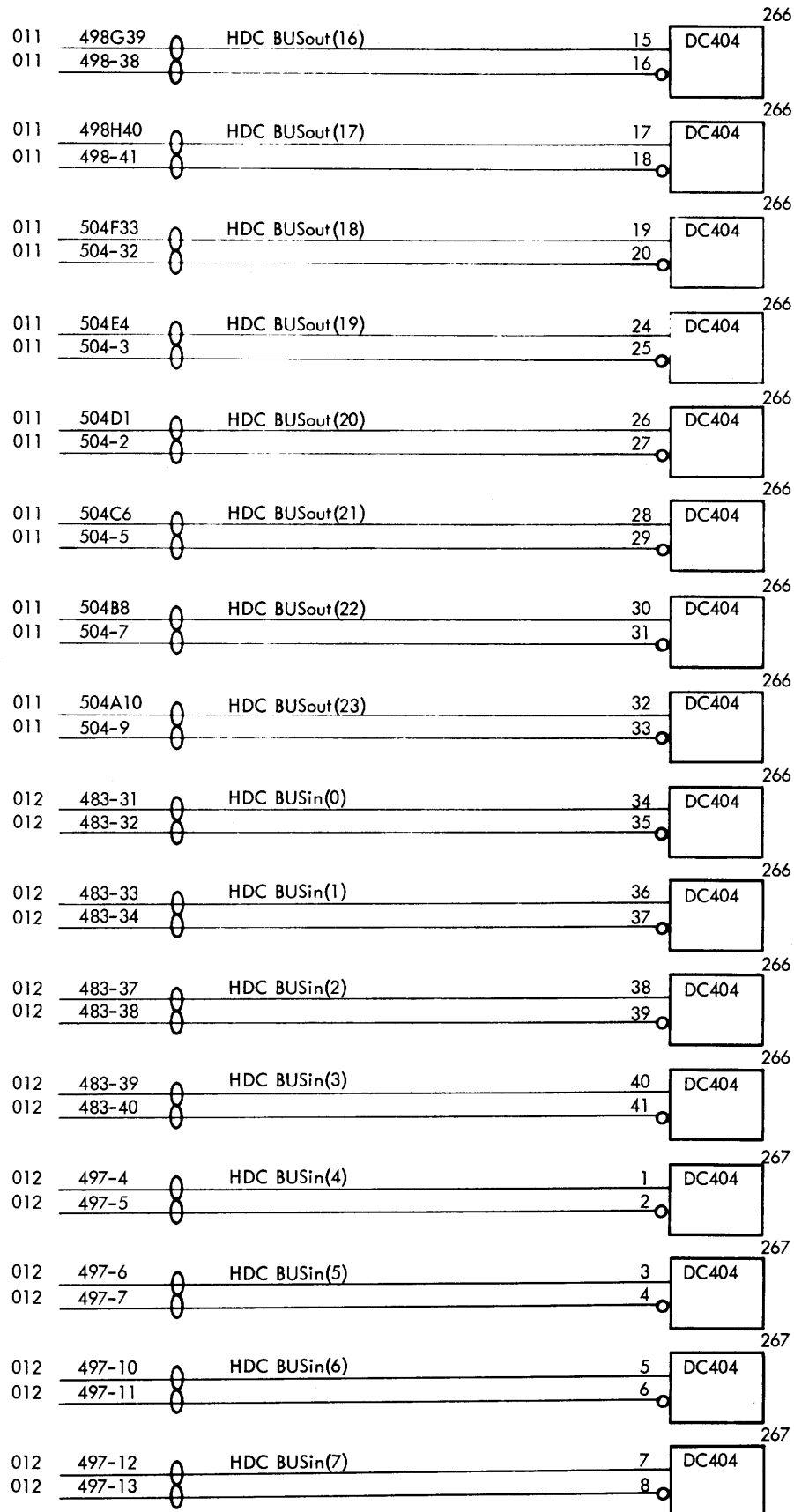


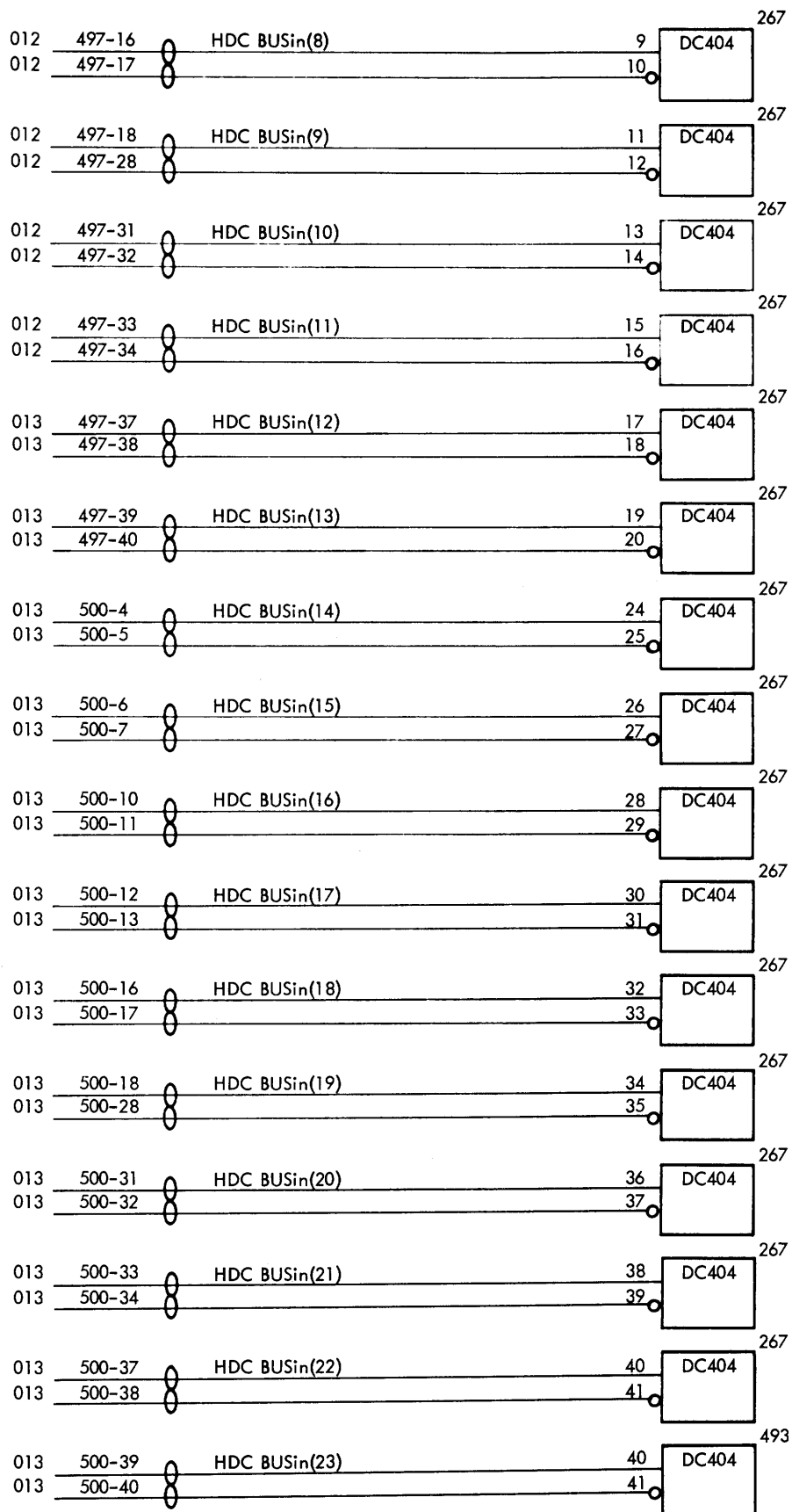


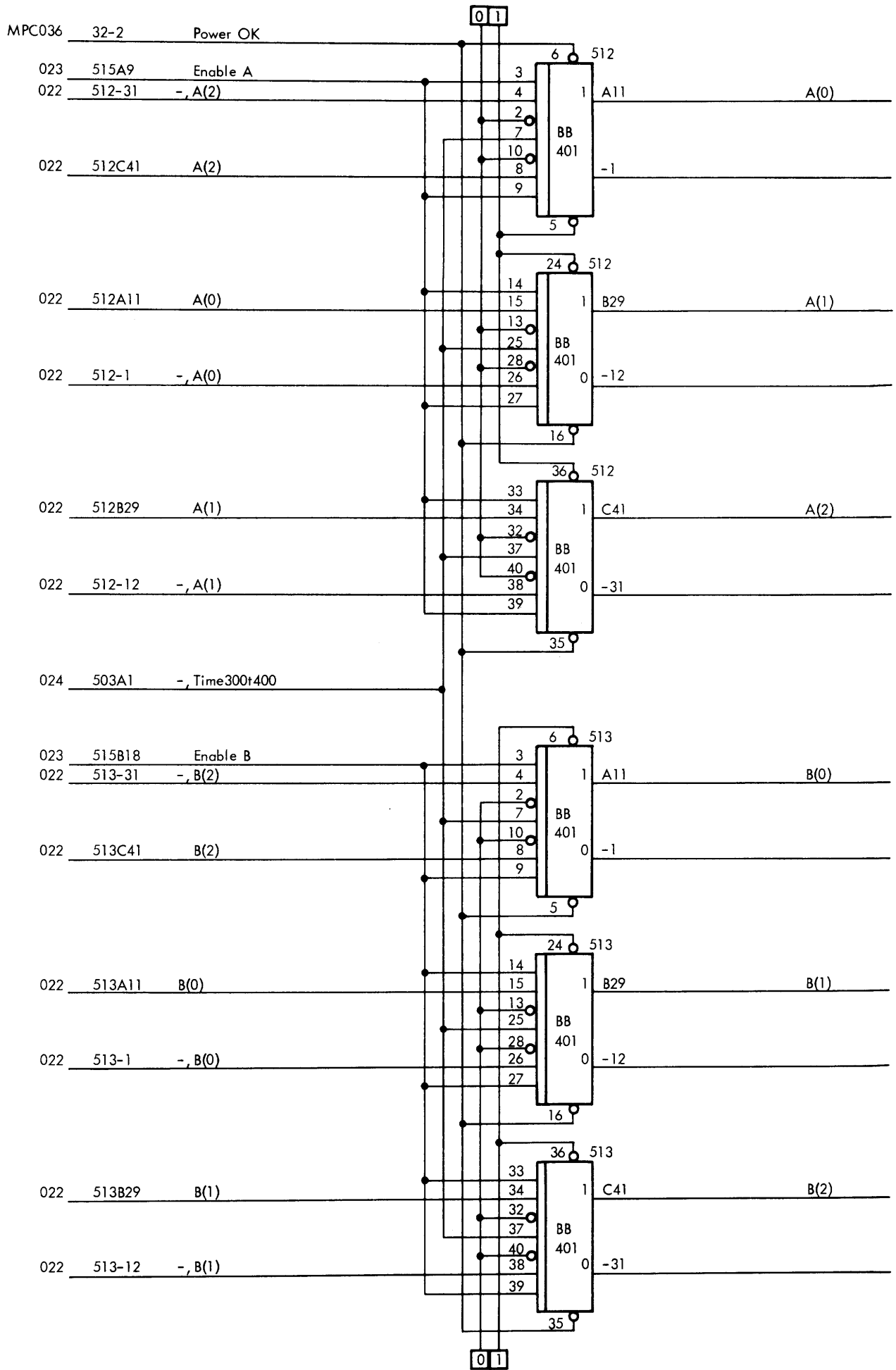


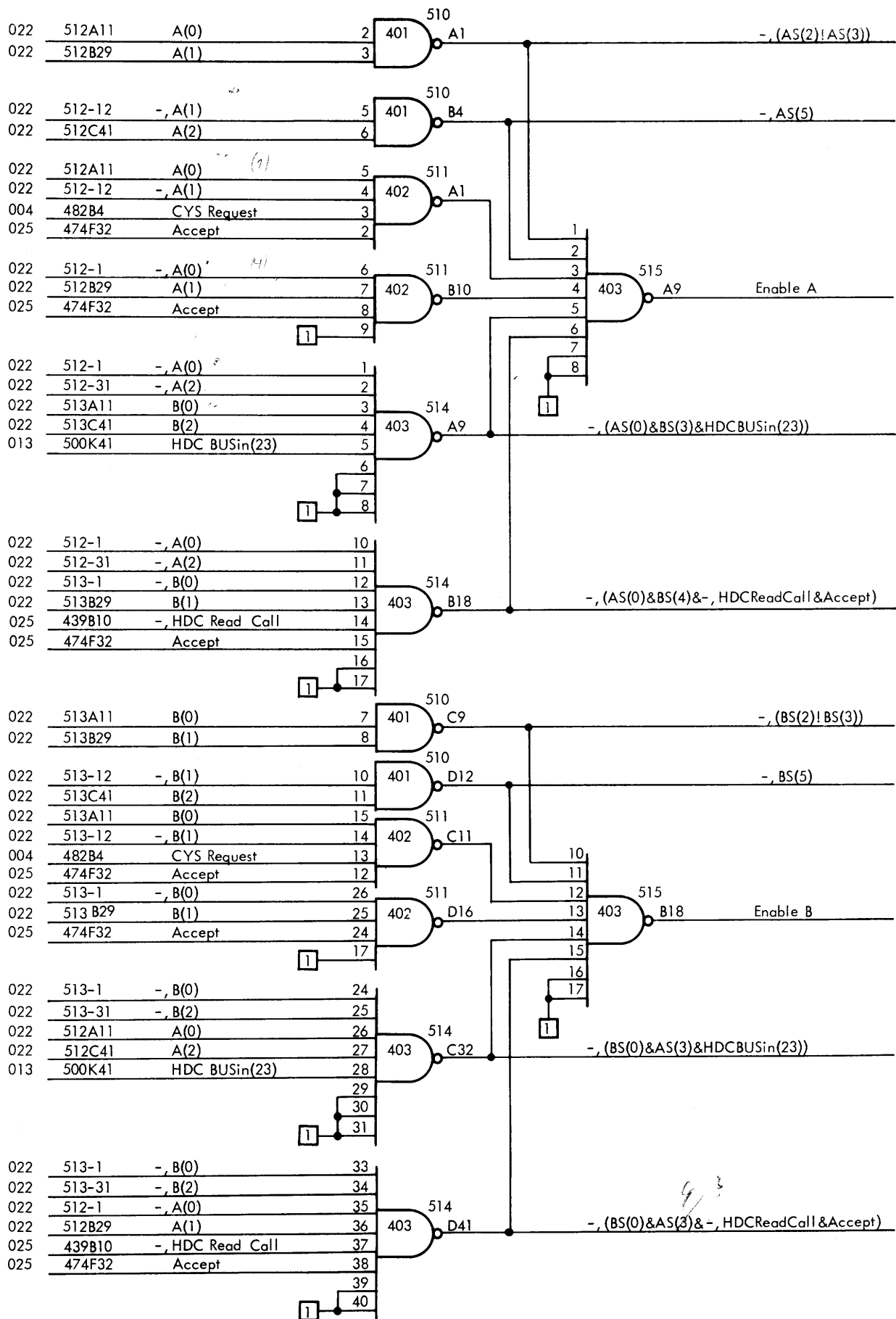


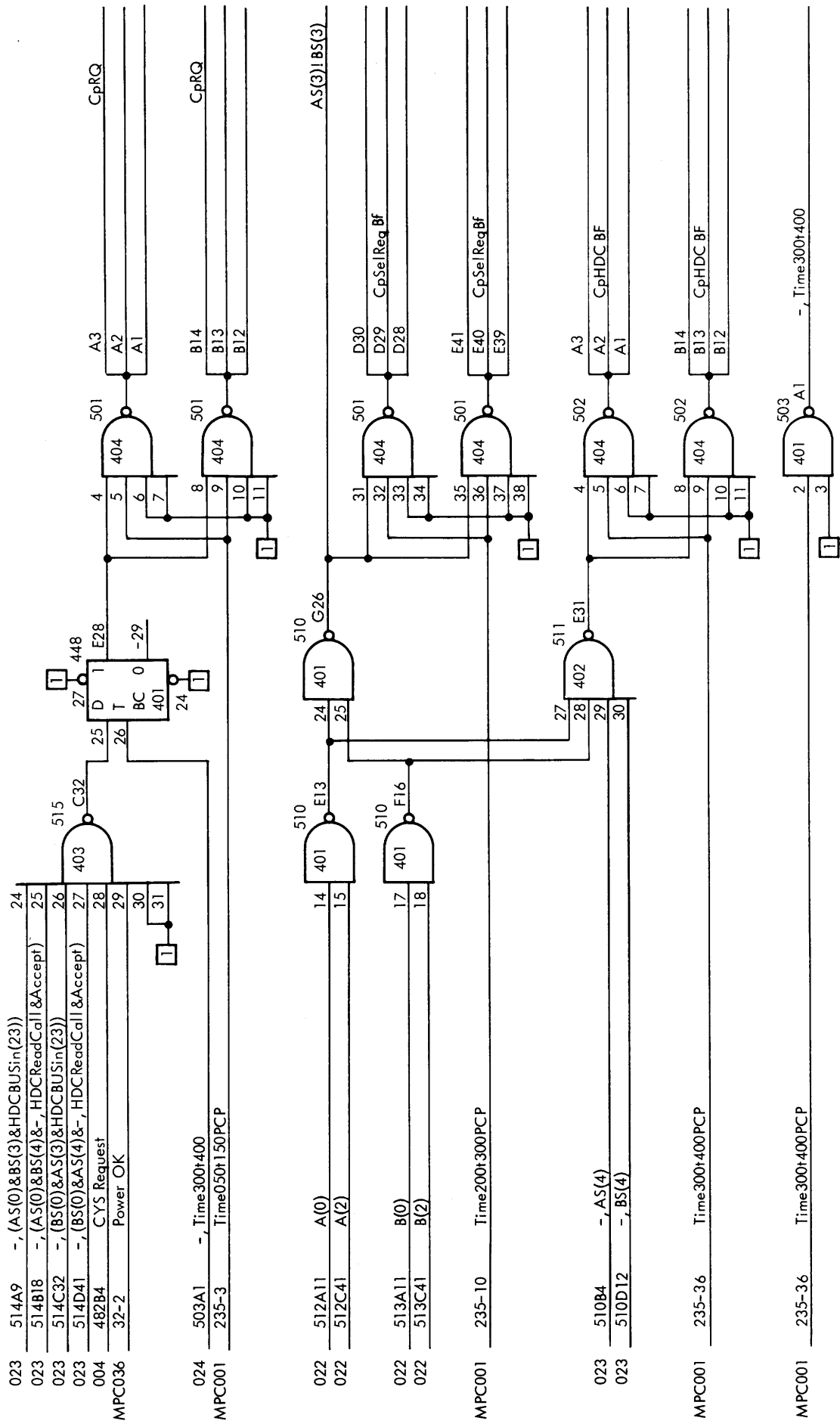


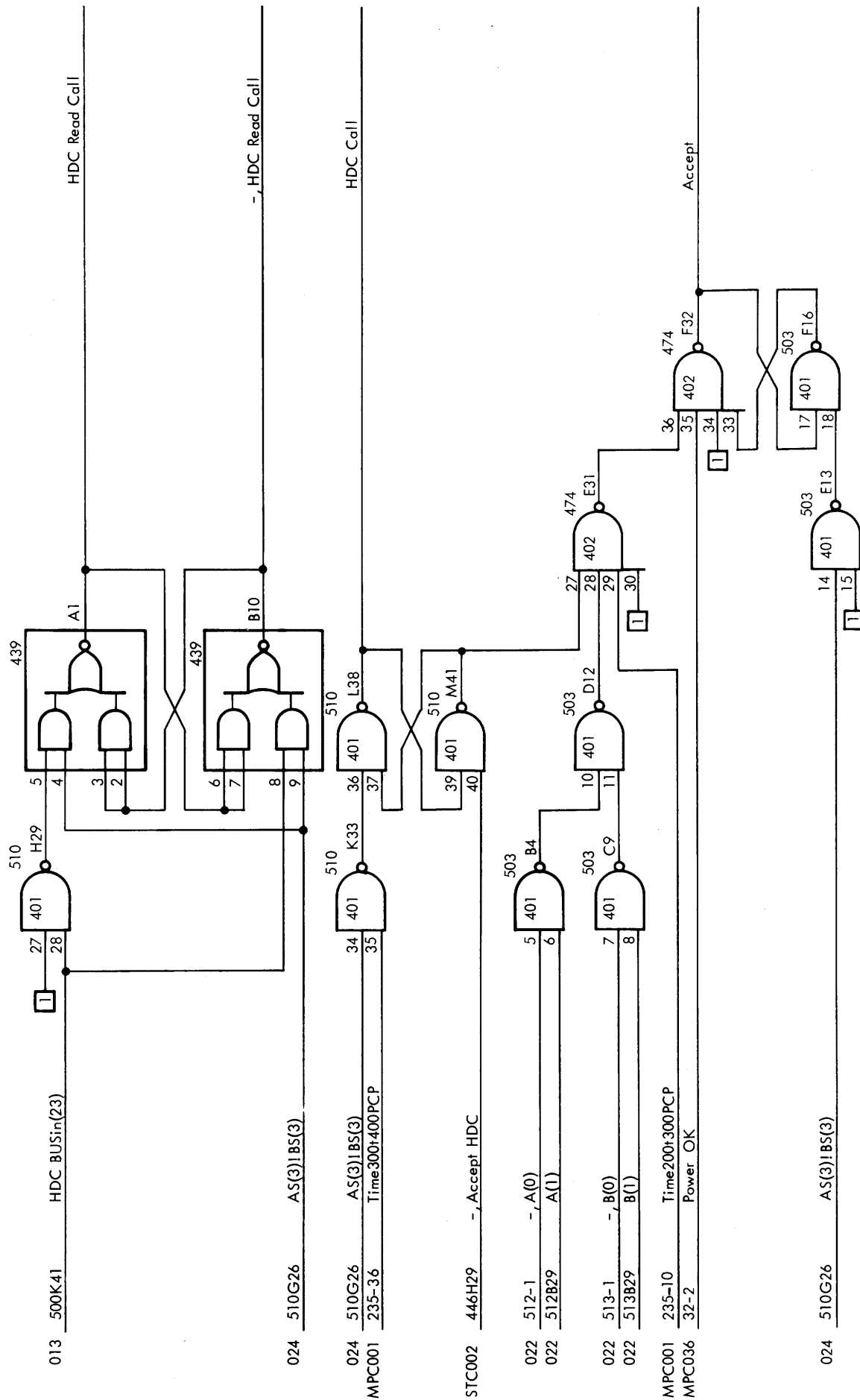


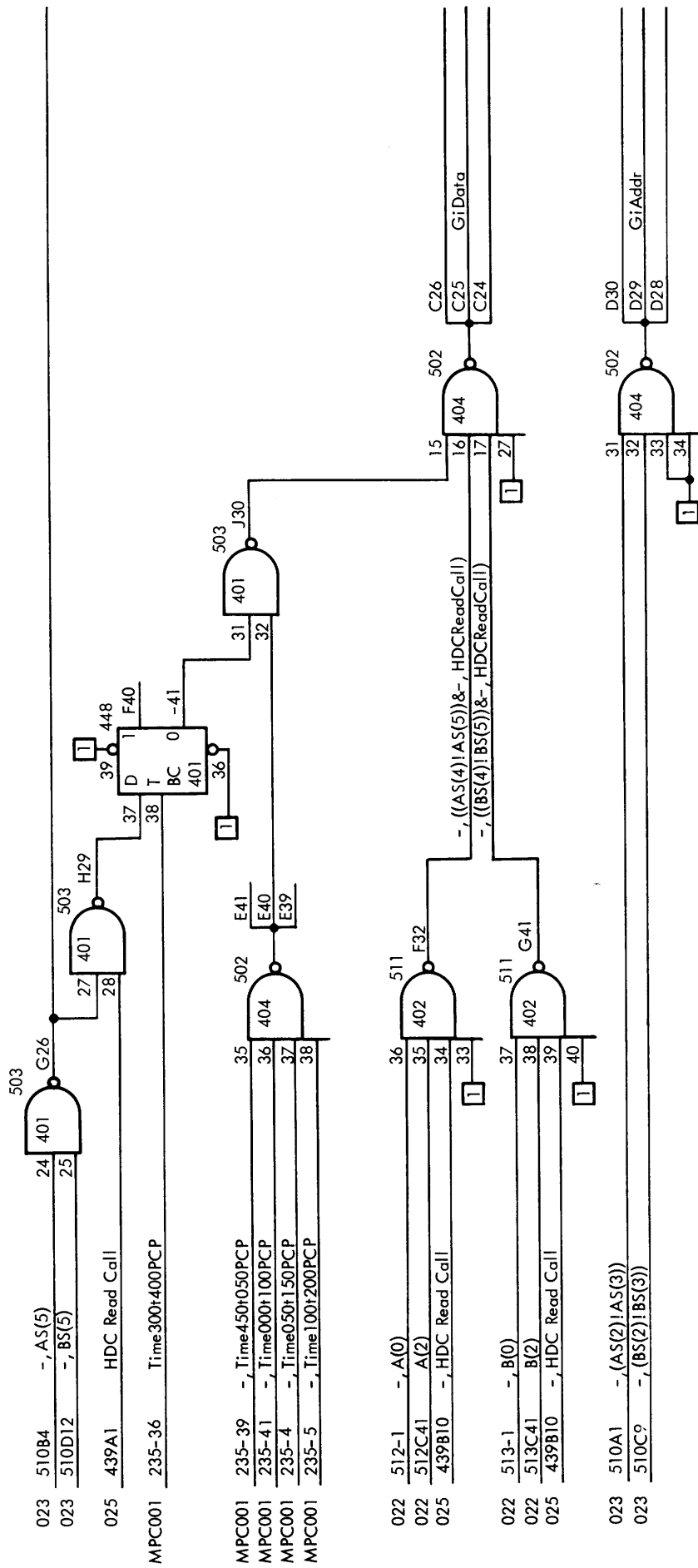








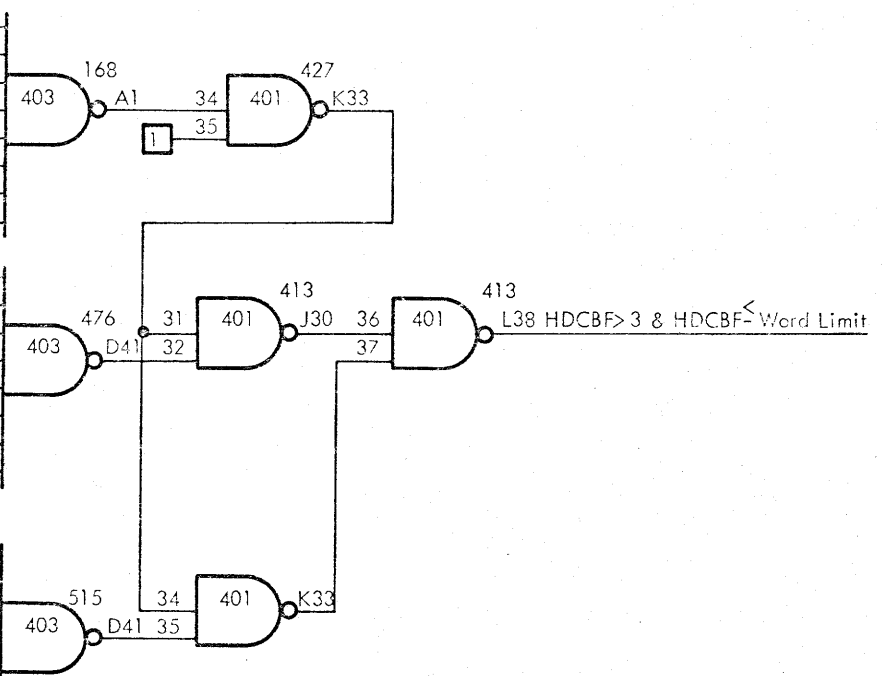


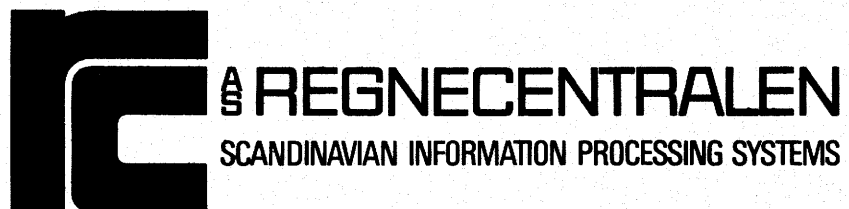


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STC022	425D4	HDCBF(6:9) < Word Limit	8

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REGNECENTRALEN

SCANDINAVIAN INFORMATION PROCESSING SYSTEMS

FALKONERALLE 1 · DK 2000 COPENHAGEN F
DENMARK — TELEPHONE: (01) 10 53 66
CABLES: REGNECENTRALEN · TELEX: 6282 RC HQ DK

ringfølge $\left. \begin{matrix} 572 \\ 573 \end{matrix} \right\} A, B, C = 0$

Accept 474 F $= 7$

7 accept HX = 446 H

HDC call = 410 L

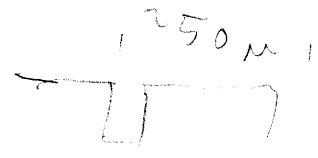
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$= 7$

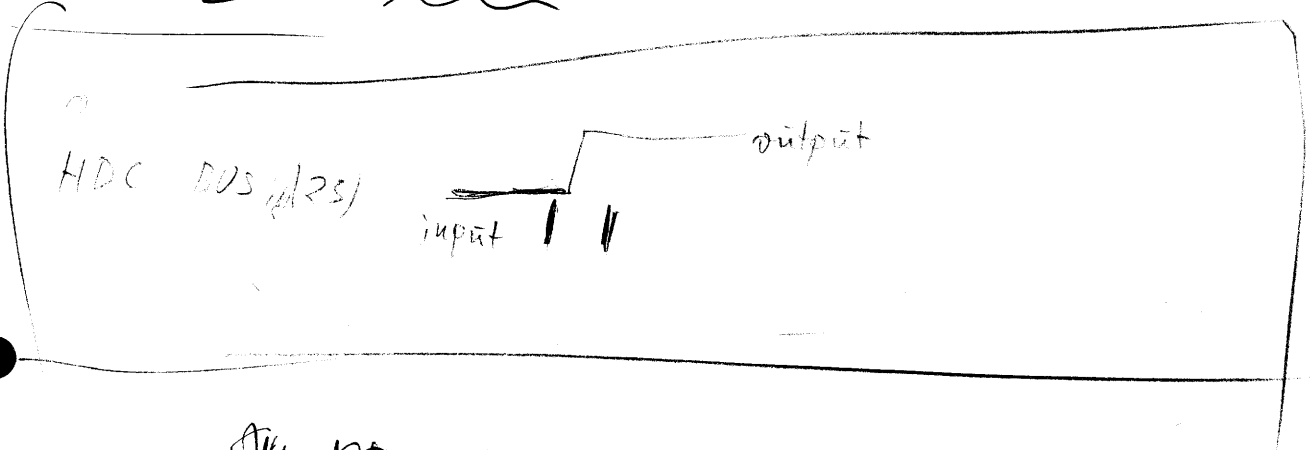
$=$

$= 0$

$= 7$



read ~~read~~ store = output



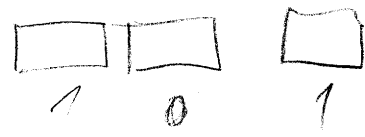
~~Sty DPS~~

(YS Request = 482 B4 = 1

Un 04-653

~~111~~

000
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011
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110
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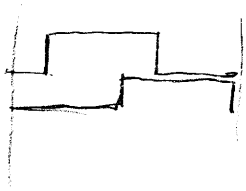
010
101

Hvordan der HDC
og svarer ikke accept



Hvis HDC blev det, så der svares accept:
se om ringtællere hvor

Hvis HDC ikke blev det?



skriv

