LOG LIST

UNIT ..... MODEL ..... NO .....

This LOG LIST contains information on modifications of the basic unit, due to Options, Engineering Change Notes, and Field Change Orders.

Do not forget to list all future modifications on this page.

OPTION ECN or FCO No.	DATE of Installation	SIGN	SHORT DESCRIPTION
[illegible]	5.12.78	SP	[illegible]
ALLE LOW-SPEED BEN T. ENDAST DE 75 BAUD/Sekunden			ALLE SO BAUD ENDAST DE 300 BAUD
J1536-J1536	21.1.79	SP	DESS ENDAST FRÅN 100 KL 600 BAUD
J1520-J1536	29.12.79	ÅLK	alla low-speed ben är ändrat från 100 till 600 baud
[illegible]	2.3.81	JMM	alla [illegible] ändrat [illegible]

RCSL 44 - RT 23

KABEL MELLEM DATA 100 & RC 4000 TMX 24.02.26 LA

RC 4000 TMX ELCO-STIK	KABEL	DATA 100 CANNON
X	hvid	1
A	blå	2
C	grøn	3
E, H, K	brun	5, 6, 8, 20
B-, D-, F-	SORT	7

S, T: STRAP FOR 300 BAUD

P, R: STRAP FOR FULL DUPLEX

B, D og F skal være parsnoede med A, C og E

Cable name: RCMODEM cable wires: 6x2x0,6 cable length: 10 meter

common		start station: RC4000 TMX		finish station: MODEM		common
wire no.	wire description	signal description	con. type: ELCO 8016	con. type: Cannon 25 pdet	signal description	remarks
1-2	blå/sort	received data /gnd	A/B	3/7		
3-4	grøn/sort	transmitted data /gnd	C/D	2/7		
5-	brun	ready for sending	E	5		
7-	grå	data set ready	H	6		
9-	orange	carier detector	K	8		
11-12	blå/hvid	power ground	X/A	1		
	i stikket chappes:	halfduplex ≠ gnd, clock ≠ 3520	P≠R, S≠V	~~10≠11, 7≠4≠20~~	~~+spænd ≠ frekv.sel., +spænd ≠ rts ≠~~ dtr.	
				9≠11≠4≠20	+ sp. til frekvsel, rts, dtr	
					OL 15-1-74	

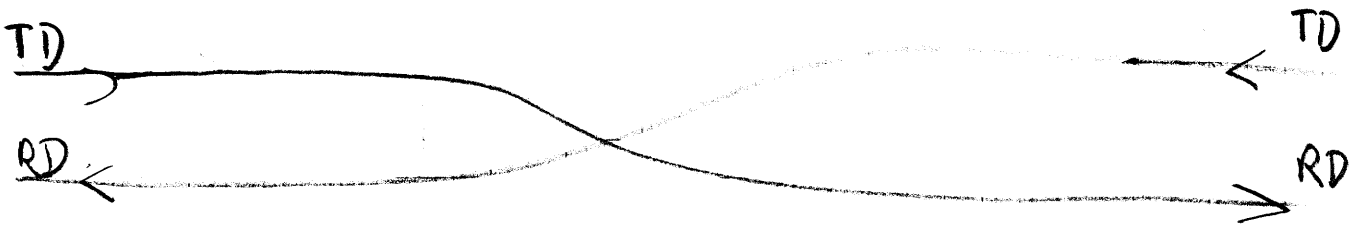
OL. 23-3-73

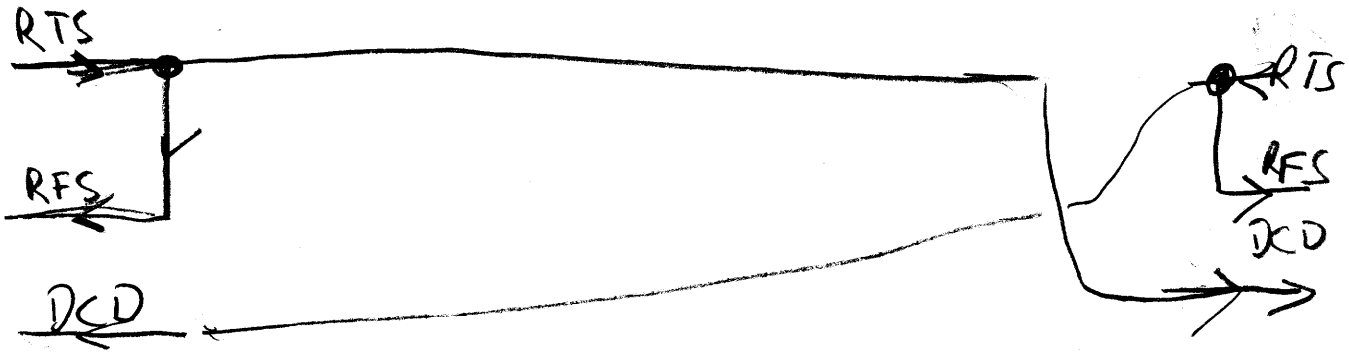
Cable name: RCOLIVETTI cable wire: 6×2×0,6 cable length: 10 meter.

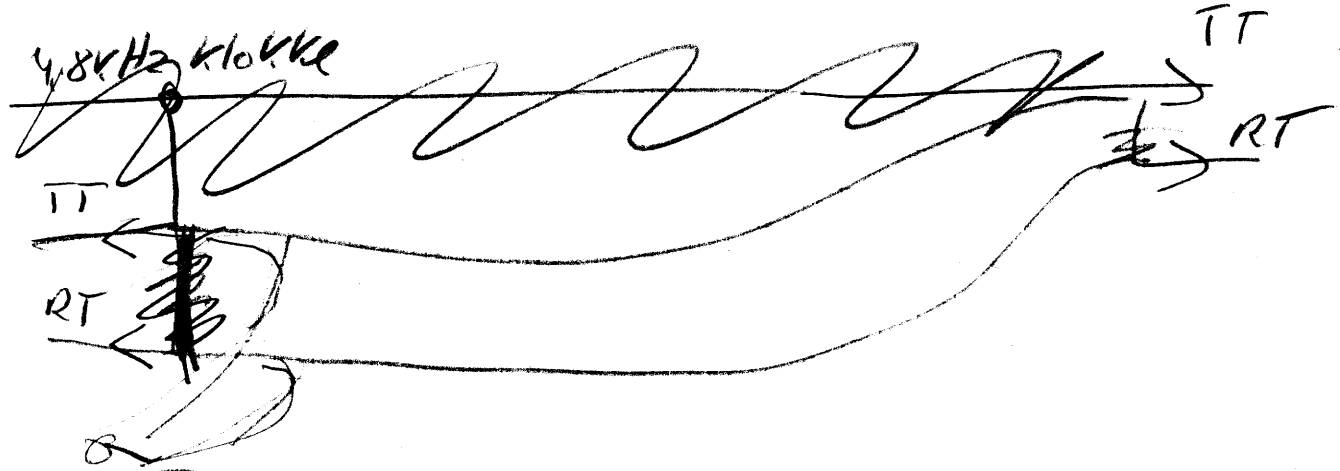
common		start station: RC4000 TMK		finish station: Olivetti terminal		common
wire no.	wire description	signal description	con. type:	con. type:	signal description	remarks.
1-2	blå/sort	received data/gnd	A/B	C/D	transmitted data/gnd	
3-4	grøn/sort	transmitted data/gnd	C/D	A/B	received data/gnd	
5	brun	ready for sending	E	M≠S≠T≠U	ready for sending	
7	grå	data set ready	H	N	data set ready	
9	orange	carier detector	K	P	carier detect.	
11-12	blå°/hvid	power ground.	X/X	X/X	power ground	
	i stikket strappes	half duplex ≠ gnd, clock ≠ 3520	P≠R, S≠V			
					OL 15-1-74	

OL 23-3-73

RC4000

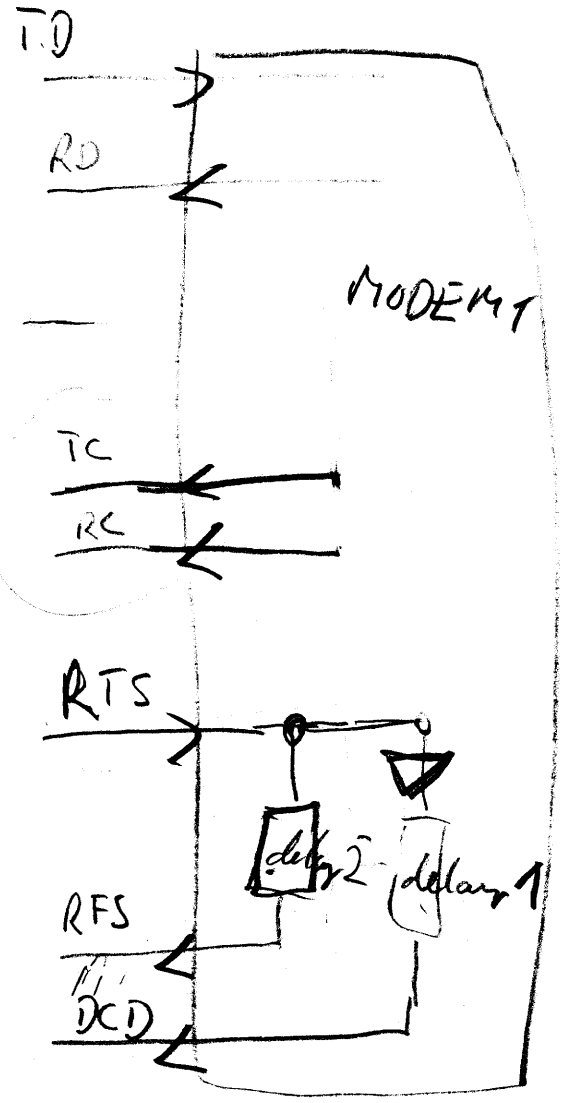




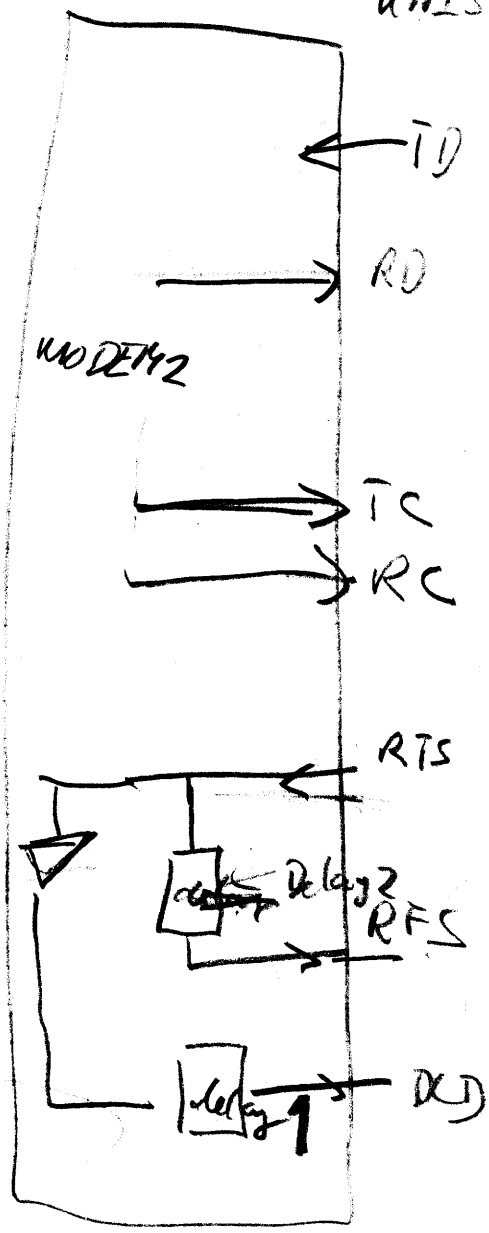


V24 EIA - RS 232 C

HP2100



UNISCOPE



1/ HP hæver RTS
modtager RFS
sender sin meddelelse.
sender RFS.

2/ Univac hæver RTS
modtager RFS
~~Delay~~
nu skal DCD være klar på RC4000
Dvs Delay 1 < Delay 2.

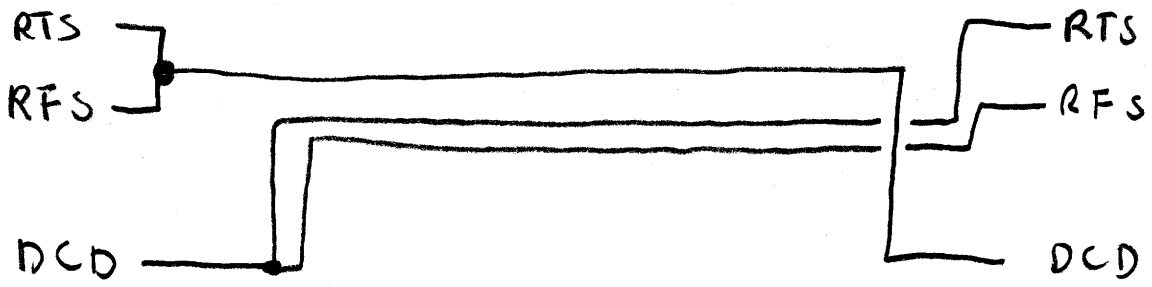
Kabel til asynkron transmission RC 4000 THX – Uniscope 100

24.02.0
LA

U-100

;

RC4000

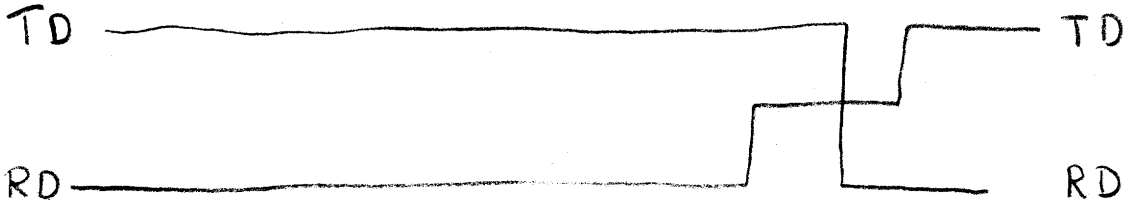


BLÅ (17-U) RECIEVE CLOCK

RØD (15-S) TRANSMIT CLOCK

0

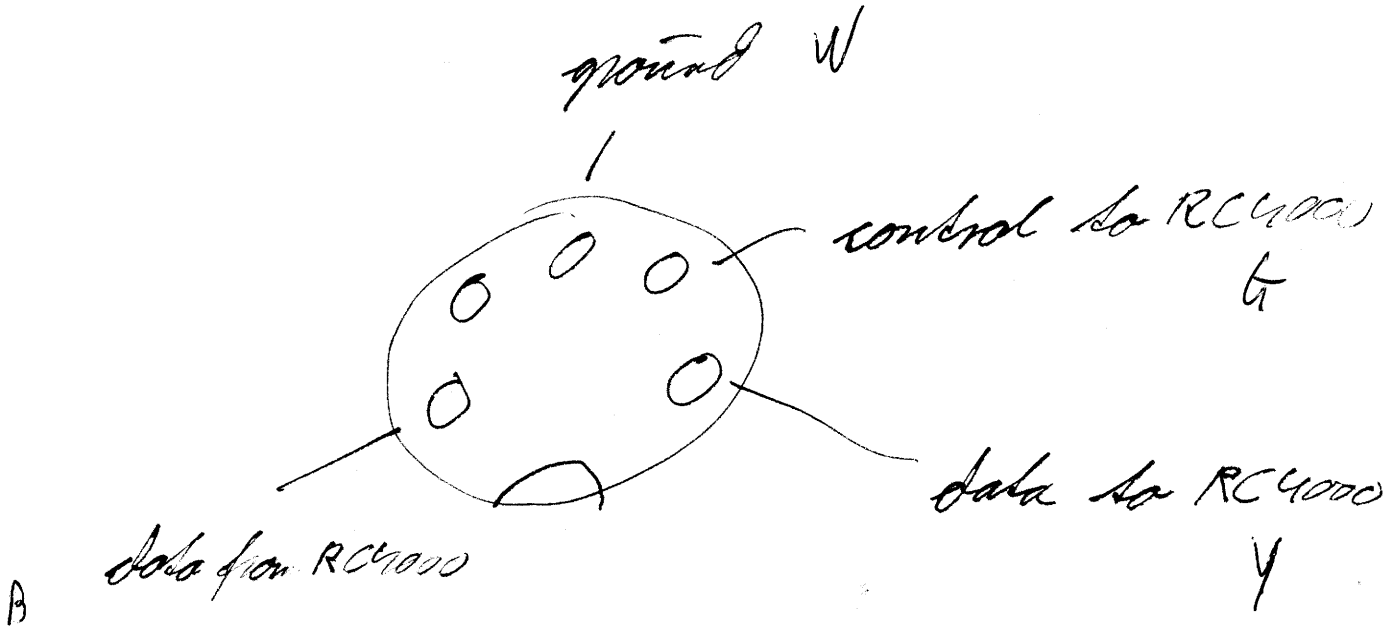
Ledninger for udvendig forbindelse af clock-generator



MM
NN

PP
RR

	ground	to 4000	from 4000	connected
[illegible]	orange hvid grå	mørk brun lys brun sort	lys blå rød gul	blå lys rød violet
[illegible]	blå brun sort	gul hvid	violet rød orange	grøn grå hvid/brun



panel front view


DATAMATICS

RCSL : 44-RT 606
Editor : Knud Sørensen
Edited : April 1973

TECHNICAL MANUAL FOR TMX 425 LOW/MEDIUM-SPEED TELEMULTIPLEXER.

Keywords: RC 4000, TMX 425 Telemultiplexer, Technical manual.

Abstract: This manual contains a complete set of technical papers for the RC 4000 telemultiplexer, TMX 425, RC 4124.

CONTENTS

RCSL : 44-RT 607
pp : 1:26
Editor : Knud Sørensen
Edited : June 1972

GENERAL INFORMATION
TMX 425
LOW/MEDIUM-SPEED TELEMULTIPLEXER

Keywords: RC 4000, TMX 425 telemultiplexer, general information

Abstract: General information TMX 425 Low/Medium - Speed Telemultiplexer.

CONTENTS PAGE

SHORT DESCRIPTION

The TMX425 Low/Medium Speed Telemultiplexer enables the connection of up to 16 Low - speed and 4 medium - speed terminal controllers to the Low - speed data channel of the RC4000 Computer. The Low - speed controllers can be individually set up for asynchronous transmission speeds of 50, 100, 110 and 200 bits/sec. The medium - speed controllers can be set up for asynchronous speeds of 600 and 1200 bits/sec. as well as synchronous speeds of up to 4800 bits/sec. Synchronous transmission requires receive and transmit clock pulses from the modem.

The system complies with the following standards where applicable : CCITT Recommendations V3, 4, 22, 24 and 26; ISO Recommendation R646; and ISO Draft Recommendations 1732 and 1734.

OPERATIONAL DESCTIPTION

General

The teletypewriter may be used in OFF-line status or ON-line status. In OFF-line status the teletypewriter may be operated without interfering with RC4000. In ON-line status RC4000 controls the communication with the terminal. A full duplex connection is mandatory, if the connection is established via modems .

The terminals are connected to the RC4000 low speed data channel via a controller/multiplexer, which will serve a maximum of 16 low-speed-terminals. It consists of one character register with associated control circuits per terminal to control transmission and reception of characters. Associated with these are the two Interrupt registers of max. 24 bits, which store the interrupts from input/output operations and operator interrupts respectively. Each of these operations is terminated by sending one of the interrupt signals to RC4000. The contents of the corresponding interrupt register is then sensed by a Sense Command to find the number of the terminals causing the interrupt. The interrupt register is cleared by the Sense Command.

Addressing

All terminals on a multiplexer have addresses in sequence. Calling the base address B the terminals are addressed as follows:

B:	Interruptregister for input/output operations
B+1:	Interruptregister for operator interrupts
B+2 to B+17 :	Low - Speed Terminals

B and B+1 respond to a Sense Command only.

Sense Command

The terminals respond to one modification of the Sense Command.

Modification 0: Transfer Data, Transmission Error, Status and Time Out Status.

If available, i.e. not transmitting or receiving, the terminals respond to Read, Write and one modification of Sense Command.

The Data character transferred to the working register depends upon the type of terminal and which command caused the latest interrupt, as indicated below.

pos.	17	18	19	20	21	22	23
Write Command	0	0	0	0	0	0	0
Read Comm. 8-bit code	b7	b6	b5	b4	b3	b2	b1
Read Comm. 5-bit code	0	0	b5	b4	b3	b2	b1

Status Bits:

Parity Error : Indicates that the parity of the caracter is odd, i. e. wrong in the case of 8-bit code character.

Time out : Indicates that a Write or Read Operation has been terminated because it could not be completed within 0.65 to 1.3 seconds.

Read Command

The Read Command clears the status bits, and enables the buf-ferregister to receive on character. A Read operation is ter-minated by :

Stopelement of Charater Sensed or by Time Out.

Upon termination an interrupt is sent to RC4000. In order to be sure to receive the next character from the terminal RC4000 should respond with a Sense Command and a new Read Command in less

than 15 mS (100 baud, 11-element) or 20 mS (50 Baud, 7-element).

For terminals where a separation between keyboard and printer is possible, the received character is retransmitted with a delay of one half element duration if a full duplex connection is provided. The retransmitted signal controls the printer, so that at least two errors must occur to leave a difference between keyboard character and printed character undetectable to the operator.

The retransmission will only take place when a Read Operation has been set up before the startelement of the next character is received. If the startelement of a character is received at a time when no Read Operation has been set up a synchronization curcuit is activated with the purpose of blocking the reception. (Recepition of a character may only begin in a startelement). The reception of characters will remain blocked until a stopelement of duration min. 167 mS - max. 335 mS has been received, i. e. the operator has stopped his input for a moment.

Operator Interrupt

If no Read operation is set up in the situation described above, a counting circuit is enabled to count the numbers of 0 to 1 transitions in the characters received from the terminal. The counting is disabled if a Read operation is set up.
When the count reaches 12 the counting is stopped. When a stop-element of duration as indicated above is sensed thereafter the counter is again reset to 0. The transistion from counter state 12 to state 0 generates an interrupt to RC4000. It is thus possible to generate an interrupt by transmitting a number of characters from the terminal at a time when no Read operation has been set up, f. ex. by depressing a repeating key for duration of say 1 second.

Write Command

The Write Command clears the status bits and transfers one character from the working register to the bufferregister and initiates transmission. The transmission is terminated upon sensing the stop-element of the transmitted character or by time out, and an interrupt is sent to RC4000. In order to continue transmission at maximum speed RC4000 should respond with a new Write Command in less than 20mS (100 baud 11-element) or 30mS (50 baud 7-element).

ON-line/OFF-line Switch

When the modem of the transmission medium indicates some status of no connection the terminal is regarded disconnected. This may be due to transmission failure or due to the terminal being in OFF-line status.

OPERATION

Since the terminals used on the TMX425 are standard teletypewriters the manufacturers orginal operation instruction is still valid. However the use of the unit as a communication terminal introduces the following additions.

ON-line/OFF-line Button and Lamp.

In order to connect the terminal on line to RC4000 the operator must press the ON-line/OFF-line button. When established, the ON-line connection will be indicated by the ON-line lamp.

When ON-line, the terminal can be disconnected by activating the same button. When disconnected the terminal is available for OFF-line use.

Operator Interrupts

If the operator wants to send an interrupt during a non input situation, he must press the automatic answer back button.

The interface between the telemultiplexer, and the 16 terminals fulfils the CCITT recommendation V24.

The circuits actually used are :

No. 101
- 102
- 103
- 104
- 105
- 106
- 107
- 109

These circuits are necessary to control the modems performing the transmission over telephone lines. However, they also allow the multiplexer and the terminals to be directly connected via cables.

INSTALLATION

See Appendix A and B.

LOCAL CONNECTION

For connection without modems the RC cable No. 32 is used.

NOTE : Different speeds and modes may be selected by inter-connections in the ELCO plug CON 2. SEE PLUGLIST.

REMOTE CONNECTION

For connections including modens the RC cable No. 30 is used at the RC4000 end.

NOTE : Same as above.

MEDIUM SPEED TERMINAL CONTROLLER (MSTC).

General.

Each TMX can have 4 MSTC's installed instead of 8 of the Low Speed Terminal Controllers.

Each MSTC has two alternating serial buffers of 128 bits each. (16 characters).

Input to the buffer system is performed by a 8 bits serial/parallel - input to serial - output shiftregister - in the following description called INPUT REGISTER.

Output from the buffer - system is performed by a 8 bit serial - input to serial/parallel - output shiftregister - in the following description called OUTPUT REGISTER.

During transmission one buffer is transmitting while the other receives data from RC4000. The buffers are interchangedwhen the transmitting buffer has been emptied and the other contains at least one character.

During reception one buffer is receiving while the other can be emptied by RC4000.

The MSTC operates half - Duplex, and the transmission direction is Controlled by READ andWRITE commands.

ADDRESSING.

All MSTC terminals have addresses in sequence following the LSTC terminals.

B : Interruptregister for Character Interrupt, generated when :

1) the buffers are interchanged during input or output.
2) no input from the telephone line has occurred within time out status 1 sec. after the set up of a READ command.
3) the buffer - OVERRUN situation occurs in Receive Mode.
4) the END BUFFER situation occurs in Transmit Mode.
5) the attached modem fails to connect within 300 msec.
6) the modem has been disconnected for 300 msec.

B+1 Interruptregister for Line Call, generated whenever the attached modem receives a call.

B+18 to MSTC terminals.

B+21

B respond to a SENSE 0 command only.

B+1 respond to a SENSE 0 command only.

OPERATION.

The MSTC terminal operates in one out of three modes, controlled by commands issued by RC4000.

A SENSE 1 selects NEUTRAL mode

" READ " RECEIVE "

" WRITE " TRANSMIT "

RECEIVE mode.

This mode is set op by a READ command from RC4000.

When set to this mode a 500 usec. CLEAR - timer is started to clear the buffers. In this period the MSTC terminal is BUSY. When switching from NEUTRAL - to RECEIVE mode a CONNECT TO LINE signal is send to the attached modem and at the same time a 300 msec timer is started. If this timer terminates without a ready signal from the modem, an interrupt is send to RC4000. This situation is indicated by DATA SET NOT READY Status. The correct response to this status is a SENSE 1 command to reset the DATA SET NOT READY status register. The serial-information on the telephone line is shifted serial into the INPUT REGISTER and whenever a whole character is ready the contents of the INPUT REGISTER is shifted into the input buffer by help of a High Speed Write - Clock (420 KHz). During this operation (a period of 20 usec) the MSTC terminal is BUSY. The buffer will now store the incoming data character by character.

When the input buffer has been filled, an interchange takes place causing an interrupt to be send to RC4000, indicated by not END BUFFER status. A full output buffer is now ready to be emptied by RC4000.
A Read command will transfer a character from output buffer to the OUTPUT REGISTER. The contents of the OUTPUT REGISTER is transferred to RC4000 by a SENSE 0 command.
The output buffer is now emptied by succeeding READ - SENSE 0 command sequences.
The buffer - empty situation will be signalled by END BUFFER status.
An undefined character is transferred to RC4000 together with END BUFFER. When a pause in the input lasts more than 100 msec a monostable circuit terminates, starting a 500 usec timer. This timer will open for High Speed Shift in the input buffer to look after same valid data.
The 100 msec timer is retriggered every time a valid character is ready from the communication line.
When no input has occurred within 1 sec after the set up of a READ command, a 1 sec Time - Out circuit is terminated giving interrupt to RC4000. This situation is indicated by TIME OUT status. If OVERRUN occurs (RC4000have missed to empty the output buffer faster than the input buffer is filled form the communication line), an interrupt is send to RC4000, indicated by OVERRUN status. Some characters will in this case be lost.

WRITE and SENSE 1 commands are accepted and immediately executed in this mode.
In synchronous mode the MSTC opens for input to the buffer - system after having established synchronization (minimum 2 consecutive SYN characters has been decoded).
A synchronization - phase can be started by a WRITE - READ command-sequence (or SENSE 1 - READ).

TRANSMIT mode.

The MSTC terminal is set to this mode by a WRITE command.
When set to this mode the buffers are cleared by the same 500 usec CLEAR - timer as in RECEIVE - mode, and the MSTC opens for input from RC4000.

No valid data character can be transferred by the WRITE command setting up Transmit mode.
Character by character is now by WRITE - commands parallel - loaded into the INPUT - REGISTER and then High Speed transferred into the input buffer. The situation, full input buffer and empty output buffer will give buffer interchange and interrupt to RC4000.
The buffer contents will now automatically be transmitted.
Both buffers filled will be signalled by OVERRUN status, transferred to RC4000 by a SENSE 0 command.
When the contents of the output buffer has been transmitted and the input buffer is filled by RC4000, an interchange takes place given interrupt to RC4000. The OVERRUN status bit is reset 16 characters can be transferred from RC4000 to the MSTC by WRITE commands. No data in any of the buffers will give interrupt to RC4000 with END BUFFER status bit set up.
READ and SENSE 1 commands are accepted in this mode, but they are not executed until the buffers have been emptied.

When switching from NEUTRAL - to TRANSMIT mode, a not ready signal from the attached modem lasting more than 300 msec will interrupt RC4000. This situation is indicated by the DATA SET NOT READY status. The correct response to this status is a SENSE 1 command to reset the DATA SET NOT READY status register.

In synchronous systems the transmission will open 6 SYN characters. When the buffer is empty, MSTC will transmit SYN for synchronous lines and logical ones for start/stop lines.

NEUTRAL mode.

In this mode the attaches modem is disconnected from the line. A WRITE command will connect the modem and set MSTC to TRANSMIT mode.

The MSTC is set to NEUTRAL mode by a SENSE 1 command. An incoming call on the line will interrupt RC4000. The correct response to this interrupt is Setting the device to Receive mode by a READ Command.

Timer - Circuits.

Short description of the Timer - Circuits used in the MSTC terminal.

CLEAR - timer.

Used in TRANSMIT - and RECEIVE mode. Started when one of these modes is set up. The length of the CLEAR - period is 500 usec.

100 msec Timer.

Used only in RECEIVE mode.

It consists of a monostable circuit. This timer is retriggered every time a valid character is ready from the communication line. When a pause in the input lasts more than 100 msec this circuit will be terminated. If the MSTC terminal is not in RECEIVE mode this circuit is disabled.

1 sec. Timer

Only used in Receive mode.

This circuit consists of a x8 counter with a input clock - frequency of 6,25.Hz.

The counter is started :

By a READ command, only if the 100 msec timer is not triggered.

The counter is reset before terminating if :

1) a command different from READ is set up.
2) A valid character is available from the communication line.
3) Blocked if RECEIVE mode is not selected.

Shift in input buffer Timer.

Used both in Transmit and Receive mode. The length of the shift - period is max. 500 msec.

The timer started :

1) in RECEIVE - mode by termination of the 100 msec timer.
2) in TRANSMIT - mode, when the output buffer is emptied and the input buffer is not yet filled,

The timer is reset before termination if some valid data is found in input buffer.

300 msec timer.

Used both in TRANSMIT - and RECEIVE mode. The timer is started, when the MSTC leaves NEUTRAL - mode, and if the modem goes disconnected during a receive or transmit operation.
The timer is reset after termination by a SENSE 1 Command.

STATUS.

In all three modes the SENSE 0 command can access the status - register, in which the following information is stored:

Pos.	STATUS	VALID IN
0	END BUFFER	Transmit and Receive mode.
1	PARITY ERROR	Receive mode.
2	TIME OUT	Receive mode.
3	OVERRUN	Transmit and Receive mode.
4	CARRIER DOWN	Receive mode
5	DATA SET NOT READY	Transmit and Receive mode
16 : 23	CHARACTER READ	Receive mode.

END BUFFER.

Status bit 0.
Indicates in RECEIVE mode that the output is empty and the input buffer is empty too or not yet total filled. This condition is delayed, so END BUFFER is not transferred together with the last valid data character, but first in the next Status - Word. In TRANSMIT mode it indicates that both input - and output buffer empty.

PARITY ERROR

Status bit 1.
Indicates that the parity of the character received is wrong. The correct parity is ODD (EVEN) in synchronous (Asynchronous) transmission mode.

TIME OUT.

Status bit 2.

Indicates that no input has occurred within 1 sec after the set up of a READ command. It is set by termination of the 1 sec. timer.

OVERRUN.

Status bit 3.

Indicates that the input buffer is full and the output buffer is full or not yet total emptied.

CARRIER DOWN

Status bit 4

Indicates that the modem signal data carrier detector has been switched off.

DATA SET NOT READY.

Status bit 5.

Indicates that the modem is not ready within 300 mS after setting up transmit or receive mode, or that the modem has been disconnected for 300 msec during a receive or transmit operation.

CHARACTER READ.

Status bit 16 : 23.

The character transferred to the I/O Datachannel has always EVEN parity.

Status bit 16 transfer the data - bit of higest - order.

The interface between the telemultiplexer and the 4 Medium Speed Terminals fulfils the CCITT V24 recommendation. The circuits actually used are :

CIRCUIT NAME AND NO.		DIRECTION	
		FROM MSTC	TO MSTC
103	TRANSMITTED DATA	x	
104	RECEIVED DATA		x
105	REQUEST TO SEND	x	
106	READY FOR SENDING		x
107	DATA SET READY		x
108	CONNECT DATA SET TO LINE	x	
109	DATA CARRIER DETECTOR		x
114	TRANSMIT CLOCK		x
115	RECEIVE CLOCK		x
125	CALLING INDICATOR		x

The circuits are further described in the following sections.

103 TRANSMITTED DATA.

The data signals originated by the MSTC to be transmitted via the data channel to one or more remote data stations are passed on this circuit to the modem. The MSTC will hold circuit 103 in the binary 1 condition during any time interval between characters or words, and at all other times when no data are to be transmitted via the data channel. The MSTC will not transfer data on circuit 103 unless an ON condition is present on

all of the following four circuits :

105 Request to Send

106 Ready for Sending

107 Data Set Ready

108 Connect Data Set to Line.

104 RECEIVED DATA.

The data signals generated by the modem in response to data channel line signals received from a remote data Station are passed on this circuit to the MSTC.

105 REQUEST TO SEND

Signals on this circuit control the direction of the transmission.

The on condition causes the modem to assume the data channel to transmit mode, provided that circuit 107 (Data Set Ready) is ON.

The ON condition will be maintained as long as MSTC desires to transmit or is transferring data on circuit 103 (Transmitted Data).

The OFF condition causes the modem to assume the data channel non - transmit mode, when all data transferred on circuit 103 have been transmitted. When circuit 105 is turned OFF it shall not be turned ON again until circuit 106 (Ready For Sending) is turned OFF by the modem.

106 READY FOR SENDING

Signals on this circuit indicate whether the modem is conditioned to transmit data on the data channel.

The ON condition indicates that the modem is conditioned to transmit data on the data channel.

The OFF condition indicates that the modem is not prepared to transmit data on the data channel.

The ON and OFF conditions of circuit 106 shal be responses to the ON and OFF condition of circuit 105 (Request to Send). For the appropriate response time of circuit 106 refer to the relevant Recommendation for the used modem.

107 DATA SET READY

Signals on this circuit indicate whether the modem is ready to operate. The ON condition indicates that the signal - conversion is connected to the line and that the modem is ready to exchange further control signals with the MSTC to initiate the exchange of data.

The conditioning of a data channel will not take place before circuit 107 is turned ON.

The OFF condition indicates that the modem is not ready to operate. The OFF condition on this circuit shall not inpair the operation of circuit 125 (Calling Indicator).

The ON and OFF conditions of circuit 107 shall be responses to the ON and OFF conditions of circuit 108 (Connect Data Set to Line).

108 CONNECT DATA SET TO LINE.

Signals on this circuit control switching of the signal - conversion to or from the Line. The ON condition causes the modem to connect the signal conversion to the Line. The OFF condition causes the modem to remove the signal conversion from the Line, when the transmission of all data previously transferred on circuit (Transmitted Data) has been completed. The OFF condition shall not disable the operation of circuit 125 (Calling Indicator).

When circuit 108 is turned OFF it will not be turned ON again until circuit 107 (Data Set Ready) is turned OFF by the modem MSTC. Whenever the MSTC is in NEUTRAL MODE this circuit is turned OFF.

114 TRANSMIT CLOCK.

Signals on this circuit provide the MSTC with signal element timing information. The condition on this circuit shall be ON and OFF for nominally equal periods of time. The MSTC will present a signal on circuit 103 (Transmitted Data) in which the transitions between signal elements nominally occur at this time of the transitions from OFF to ON condition of circuit 114. Timing information on circuit 114 shall be provided at all times when circuit 107 (Data Set Ready) is in the ON condition.

115 RECEIVE CLOCK.

Signals on this circuit provide the MSTC with signal element timing information. The condition on this circuit shall be ON and OFF for nominally equal periods of time, and a transition from ON to OFF condition shall nominally indicate the centre of each signal element on circuit 104 (Received Data).

125 CALLING INDICATOR.

Signals on this circuit indicate whether a calling is being received by the modem. The ON condition indicates that a calling signal is being received. The OFF condition indicates that no calling signal is being received.

INSTALLATION

See Appendix F and G.

LOCAL CONNECTION

For connection without modems the RC cable No. 55 is used.

NOTE : Different speeds and modes may be selected by interconnections in the ELCO plug CON, 2 SEE PLUGLIST and Appendix K and L.

REMOTE CONNECTION.

For connection including modems the RC cable No. 56 is used at the RC4000 end.

NOTE : same as above.

MAINTENANCE

The only maintenance necessary in connection with the MSTC controllers is a check and a possible adjustment of the DC voltages for the buffer - units. Check and adjustment are performed in the DC - DC converter on the PC BOARD in POS 104. Adjustment is performed by the potentiometer on the PC BOARD in POS. 104.

CAUTION : Before removing or replacing any PC board in the TMX425, disconnect the power from the I/O Cabinet. Failure to do so may result in damage to components on the PC boards.

P , ELCO Varilock Receptacle, type 8016-020, code -
P Cannon Plug type DB-25P

P PIN	I*	T*	GEN. ADR.	SIGNAL NAME	44 T*	P PIN
A		B		RECEIVED DATA X		3
B		A		0V	7	
C		D		TRANSMITTED DATA X		2
D		C		0V	7	
E		F		106 READY FOR SENDING DEV X		5
F		E		0V	7	
H		J		107 DATA SET READY DEV X		6
J		H		0V	7	
K		L		109 DATA CARRIER DETECTOR DEV X		8
L		K		0V	7	
M						
N					9	4
P					11	9
R					12	11
S					20	12
T						
U						
V						
W						
X				SHIELD		1

I* : Interconnection. T* : Twisted pairs.

Length of cable: 10 m

Different speeds and modes may be selected by interconnections in the ELCO plug according to the following list.

Select :	Strap
50 baud (300)	S-T
100 -	S-U
110 -	S-V
200 -	S-W
5 bit codes	M-N
full duplex transmission	P-R

P , ELCO Varilock Receptacle, type 8016-038, code -
P CANNON PLUG, TYPE DB 25P

P PIN	I*	T*	GEN. ADR.	SIGNAL NAME	I*	P PIN
A		B		103 TRANSMITTED DATA X		2
B		A		0V	7	
C		D		104 RECEIVED DATA X		3
D		C		0V	7	
E		F		105 REQUEST TO SEND X		4
F		E		0V	7	
H		J		106 READY FOR SENDING X		5
J		H		0V	7	
K		L		107 DATA SET READY X		6
L		K		0V	7	
M		N		108 CONNECT TO LINE X		20
N		M		0V	7	
P		R		109 DATA CARRIER DETECTOR X		8
R		P		0V	7	
S		T		114 TRANSMIT CLOCK X		15
T		S		0V	7	
U		V		115 RECEIVE CLOCK X		17
V		U		0V	7	
W		X		125 CALLING INDICATOR X		22
X		W		0V	7	
Y						
Z						
AA						
BB						
CC						
DD						
EE						
FF						
HH						
JJ						
KK						
LL						
MM						
NN						
PP						
RR						
SS				SHIELD		1
TT				SHIELD		1

I* : Interconnections. T* : Twisted pairs.

Length of cable: 10 m

Different speeds and modes may be selected by interconnections in the ELCO plug according to the list in section.

Mode	Straps in PLUG'CON 2 for cable no.55 and PLUG'CON 1 for cable no. 56		
	KK-LL	MM-NN	PP-RR
Synchronous transmission	NO	YES	YES
Asynchronous transmission			
600 band	YES	NO	YES
1200 band	YES	YES	NO

RCSL : 44-RT 608
PP : 1:27
Editor : Knud Sørensen
Edited : April 1973

FUNCTIONAL DESCRIPTION
TMX 425
LOW/MEDIUM SPEED TELEMULTIPLEXER

Keywords : RC 4000, TMX 425 telemultiplexer, Functional description.
Abstract : This paper contains a functional description with block diagrams for the telemultiplexer TMX 425.

CONTENTS PAGE

FUNCTIONAL DESCRIPTION OF TMX425

The TMX425 is designed to multiplex the information flowing to and from the terminals connected to RC4000, and to perform the functions necessary to control the individual terminals.

Therefore the TMX425 can be divided into the following 3 main parts.

1. The multiplexing part, which transfers the information between the LSD and the internal bus - system within the TMX425.
2. The LOW speed Terminal Controllers (LSTC)
3. The Medium Speed Terminal Controllers. (MSTC).

The multiplexing part.

As seen from fig. 1, some of the circuits mainly deals with the transfer to the TCs, while others mainly deals with the transfers from the TCs. The two groups are as follows.

Sending Circuits :

- Receivers for LSD
- Address decoder
- Command decoder
- Drivers for internal output bus
- Clock system

Receiving Circuits :

- Receivers for internal input bus
- Interrupt expander
- Drivers for LSD.

Receivers for LSD.

See diagram TMX01.

The receivers are connected to the LSD IO BUS and transform into RCLM400 standard levels all the control signals and the bus lines 10 to 23.

A parity generator will generate a high level on the output when the character transferred on bus 17 to 23 has odd parity.

Address Decoder.

See diagram TMX02.

The TMX425 contains 22 separate devices which can be addressed from RC4000.

These are the 2 interrupt registers and the 20 terminal controllers. The devices are addressed by 22 separate select signals which are generated by the address decoder in accordance with the device address placed on LSD IO BUS 10 to 17.

The lowest possible address, i.e. the address of interrupt register 0, is wired on soldering terminals in the circuit. When a device address is signaled on the bus, the correct device no. is found simply by subtracting the wired address from the incoming. A one out of 22 decodings will then generate the select signal for the addressed device.

The signal ACTIVE is generated if any of the 22 devices is selected.

Command Decoder.

See diagram TMX03.

The command decoder senses and stores the four valid commands : Sense, modified sense, read, and write. The two sense commands are cleared when enable is removed, while the read and write command is kept till the TMX425 is again addressed.

Drivers for Internal Output Bus.

See diagram TMX04.

The internal output bus running from the multiplexer to all 20 TCs carriers two kinds of information.

a. A fixed bit pattern which has to be loaded into the data register in the LSTC prior to the execution of each read operation.

b. The character which shall be transmitted during a write operation.

The problem of generating these two kinds of information has been solved so that the a-information is sent always during the presence of the address signal, while the b-information is sent at all other times. It is possible not to distinguish between read and write commands because the TC uses either the activate or transfer signal to read in the information. Fig. 2 shows the contents of the output bus when it transmits the a - and b - information. Both a and b has separate configurations for 8 bit terminals and 5 bit terminals.

Clock System.

See diagrams TMX30 and TMX31.

The clock system has one single 6,7584 MHz oscillator which trough a number of frequency dividers produces clock frequencies for all purposes.

a. A 1,56 cycles clock for the time out circuits. (LSTC).

b. A 6,25 cycles clock used to inhibit input from the terminal when RC4000 has failed to keep up with the incoming data.(LSTC). And clock frequency for the time out counter in the MSTCs.

c. Four device clocks 1600 cps, 3200 cps, 3520 cps, and 6400 cps used to run the LSTCs at the telegraph speed 50-100-110 and 200 baud.

d. Four device clock 19,2 KHz (32 x 600 Hz), 38,4 KHz (32 x 1200 Hz), 76,8 (32 x 2400 Hz) and 153,6 KHz (32 x 4800 Hz) for asynchronous transmission mode in the MSTCs.

e. A 844,8 KHz Clock for the buffer units in the MSTCs.

f. A 3,3792 MHz High Speed Clock for the MSTCs.

Receivers for internal Input Bus.

See diagrams TMX13, TMX14 and TMX15.

The internal input bus takes care of all information form the TCs to the multiplexer except the interrupt signals. It consists of 16 wires of which 8 transmit the incoming data, while 6 transmit the status of the terminal. The 2 last wires tell whether the Terminal is READY and CONNECTED or not.

The input bus is actually 16 wired or gates, so that all transmitters placed in the TCs are gates with open collector output, while the receivers are AA451 and AD401 gates with a load resistor connected to the input.

The information transferred on the bus lines is shown on Fig. 3.

Interrupt Expander.

See diagrams TMX11 and TMX12.

TMX425 has 2 interrupt expanders,one CHAR ITR, and one for KEY ITR. Each expander contains two 24 bits registers A and B. The A register is an input register and has the triggerinput of each flip - flop connected to the interrupt output of the corresponding TC.

The B register is the output register through which the contents of A is transferred when the expander is sensed.

TCs wanting to send interrupts set their corresponding bits in the A register. The leading edge of the first flip - flop being set in the A register produces an interrupt for the RC4000, which then issues a sense command for the expander. During theis sense, the contents of the A register is moved to B, from where it is sent to RC4000 indicating which terminals wanted to interrupt.

Drivers for LSD.

See diagrams TMX16, and TMX17.

The 28 drivers transform the outgoing signals form RCLM400 standard levels into the balanced signals used on the lowspeed bus.

24 of the drivers are connected to the input bus lines, while the remaining 4 transmit the ready and connected signals plus the two interrupts. The information transferred on the bus lines is shown on Fig. 4.

LSTC TERMINALS CONTROLLERS.

The TCs perform the control of, and syncronization with each terminal connected to the multiplexer. They also transform the characters from parallel form into serial form or vice versa. They generate interrupt on termination of write and read operations, and on the operator intervention. If a TC senses input without a read command set up, it blocks for input and will not open until the line has been steady for a period of 160 - 320 msec.

The circuits in a TC can be divided into two parts : The transmit/ receive register, and the control circuits.

Transmit/Receive Register.

See diagram TMX05 and circuit diagram for PCBA 3128-1.

The transmit/receive register is a 12 bit shift register able to operate in either serial or parallel mode.

Prior to each read operation the register is loaded with a certain bit pattern by the signal INTRANSFER. The bit pattern is the contents of the internal output bus IOB 1 - 10 (See section 4.1.4).

On the startelement of an incoming character the control circuits will start the generation of shiftpulses and at the selected telegraph speed shift the incoming data into the register until the preloaded bit pattern places a logical one at testpoint B. The signal ~ End Receive now generated at pin 39 will cause the control circuits to stop the shiftpulses and interrupt RC4000 to indicate the completion of the read operation.

The received characters is now placed in the shift register and will be sent to the internal input bus when RC4000 issues a sense command, causing the control circuits to generate the OUTGATE pulse.

For the bit configuration at the input bus see section 4.1.6.

Prior to the write operation the INTRANSFER pulse loads the register with the contents of IOB 1 - 10, thus placing the character to be transmitted in the lower part of the register (see section 4.1.4)
When the shiftpulse is startet, the contents of the register is shifted pass testpoint B, from where it controls the output named
-,TRANSMITTED DATA A.
When the lower 9 bit contains a one and 8 zeroes, the transmission is stopped by the generation of -,End Transmit. Simultaneously the oneshot is triggered in order to ensure a sufficient duration of the stopelement.

Control Circuits.
See diagram TMX06 and circuit diagram for PCBA 3041-1.
When a TC is selected (by Enable and -,Select) a select flip - flop made by two 7400 gates is set. This causes the outgate signal to transfer the contents of the Transmit/Receive register to the input bus. From there it will be transferred to RC4000 if the selecting command is a Sense.
The select flip - flop also opens for the buslines IBA 11 to IBA 14 to inform on the status and type of terminal.
If the selecting command is a Read or Write the signals Read & Activate or Write & Transfer will generate the Intransfer signal to preload the Transmit/Receive register. They also presets or preclears the shiftpulse generator to the right start position for either read or write.
The TC is now set up for an input/output operation, which will start on the trailing edge of Enable.
This edge sets the read or write flip - flops whereupon the Rec ! TR signal conditions the Transmit/Receive register to serial mode.
In case of a write command, the signal -,Write will, after completion of the stopelement of the previous character, enable the counter IC 11, and thus start the shift pulse.

In case of a read command the signal Receive will release the flip - flop having output at testpoint D. The incoming data (-Data rec) then sets the flip - flop which enables the counter IC11, and thereby syncronizes the shift pulse generator with the incoming data.

If the receive signal is not set up when the incoming data arrive a low output from IC 4 pin 3 will clear the flip - flop in IC 5.

Controlled by the 6 cps clock, the two flip - flops in IC 5 prevent the incoming data from starting the shift pulse generator, till the input has stopped for a period of 160 - 300 mS.

If the number of shifts from 1 to 0 exceeds 12, the INTV signal will go low, and stay so till the input stops, and the flip - flops in IC5 again open for syncronization with data input. The trailing edge of the INTV gives the operator interrupt.

If a read or write operation is not terminated within a period of 0.65 to 1.3 secs, it will be terminated by the time out circuit.

The two flip - flops in IC12 will generate the time out signal if the Rec ! TR signal exists for more than the mentioned period.

Time out will generate -, End transmit and -,End receive, and signal on IBA 10 gives TIME OUT status.

MSTC TERMINAL CONTROLLERS.

The Medium Speed Terminal Controller consists of 4 PC Board each with its own independent function. See Fig. 5.

Therefore the MSTC can be divided into the following 4 main parts.

1. TRANSMITTER UNIT
2 RECEIVER UNIT
3. BUFFER UNIT
4. CONTROL UNIT

TRANSMITTER UNIT.

For details refer to TMX08, circuit diagram for PCBA 2066-1, TC3, TC4, TC5 and TC6.

The function of the Transmitter Unit is to request for information bit by bit from the buffer unit and to transmit this information serially. In asynchronous mode the transmitter unit must divide the information up in characters and put on START - and STOP elements. When no serial data is ready from the buffer, the transmitter will transmit STOP - Level.

In synchronous mode a transmission will always start with transmitting of 6 SYN - characters, then the data - information is transmitted. If no serial data is ready the transmitter will transmit SYN - characters.

Transmit synchronous.

The trailing edge of -;WR & TR from the Control Unit will set IC24 giving the signal REQTS; by this signal the value 6 is parallel - loaded into the counter IC6. When the modem send RDYFS (Ready For Sending) as response to REQTS (Request to Send), the first coming leading edge of TRMCL will set IC7, the following trailing edge IC15 giving the signal X23.

The signals X33 and X32 is generated by setting IC15.

X34 will parallel - load the bitnumbers of the SYN - character (always 8) into the counter IC9. Then this counter count down on the leading edge of TRMCL. The outputs (X2,X3,X4 and X38) from this counter control an eight bit multiplexer IC1. On the eight data inputs on this multiplexer the bit - pattern for the SYN - Character is strapped.

From the multiplexer output the SYN - character is transferred bit by bit to the Output FF IC3. From this FF the information is transferred to a modemdriver by the signal TRMTD DA.

When the counter IC9 is count down to zero the signals END DATA and END CH are generated.

END CH reset IC15 (X23 : = 0) and count one step down in the counter IC6.

This loap is repeated until counter IC6 is count down to zero, giving the signal X27, indicating that 6 SYN characters are transmitted.
The first leading edge of TRMCL will then generate the signal X28 enabling the monostable circuit IC17 (T = 35 uS). At the same time X19 switch to logical 0 triggering the monostable circuit (REQ CH : = 1). If serial data is ready (¬SER DA RDY : = 0) from the buffer unit, the trailing edge of REQ CH will set IC7 giving the signal TRMTG DA. On the trailing edge of TRMTG DA X28 is reset. The leading edge of the output from IC7 will generate the signals X33 and X34. X32 will on the trailing edge of X28 force a setting of IC18, so the signal ¬ GI BIT is simply the inversion of the signal TRMCL.
¬ GI BIT will transfer the information from the buffer bit by bit to the transmitter unit on the signal SERIAL DATA.
¬ GI BIT will pulsate until the counter IC9 is count down to zero generating the signal END DATA. This signal will reset IC18 blocking the ¬ GI BIT generator.

NOTE :
Strap D1 and strap M2 is used in synchronous mode.
If no serial data is ready from the buffer unit before the trailing edge of REQ CH, IC7 a is not set; instead the next trailing edge of TRMCL will give signal TRMTG SYN causing SYN Characters to be transmitted until data is ready again.

Transmit asynchronous.
The asynchronous transmission takes place very similar to the synchronous transmission. The only deviations are :

1. The transmission is not started with SYN characters. The signal ASYNCR will keep the counter IC6 reset, so the transmitter at once go on to transmit data.
2. Every character is started with a START element (logical 0) and followed by a STOP element (logical 1). In asynchronous mode a flip - flop more IC3 is put in the transmission route. The signal ¬X8 will set a STOP - element into the last IC3 and a START - element into the first IC3.

3. Every character is increased by two bits, because the signal END CH is first generated when the counter IC9 is count down - 2.
4. Possible spaces between characters is filled with stop -- elements, and not with SYN characters.
5. Strap M2 and Strap D1 are used in asynchronous mode. Then transmission is possible with 8 data bits per. character.

RECEIVER UNIT.

For details refer to TMX07, circuit diagram for PCBA 2065-1, TC7, TC8, TC9, TC10 and TC11.

The receiver unit receivers the serial information from the transmission line, an ' divides this information up in characters to the buffer unit.

The receiver unit receives both asynchronous and synchronous information.

The character length is always 8 databits.

The Receiver Unit is divided into the following main parts :

Character divider Circuit.

Character Synchronization Circuit.

Bit Synchronization Circuit.

Bit Synchronization Circuit.

This Circuit produces the internal bit - rate clock both in transmit and receive mode and both in asynchronous and synchronous mode. In synchronous mode (¬ASYNCR : = 1) a logical 0 is delivered to IC23 - 10. This flip - flop will then operate as an inverter from pin 13 to pin 8. The bit frequency clocks are delivered from the modem by the signals RECV CL (Received Clock) and TRANSM CL (Transmit Clock). Switching between these two clock signals is performed in IC8 controlled by the signal RDYFS.

In asynchronous mode (¬ASYNCR : = 0) the receiver will start the bitsynchronization on the leading edge of a START - element. (X16). To do this a clock frequency of 32 times fastere than the bit frequency is used. Two such clock frequencies are available, MSCLA (normally 32 x 600 Hz) and MSCLB (normally 32 x 1200 Hz). Switching between these clockfrequencies is performed by IC8, controlled by the signals SEL CLA and SEL CLB (Strapped in the device cable). The leading edge of ¬RECVD DA (the beginning of a possible START - element) will set IC10 releasing the counter IC22 and the flip - flop IC23. When IC22 has count to eight IC23 a is triggered , if the START - element is still on the line. This operation blocks the resetting of IC10 trough IC21. On the center of the START - element IC22 has count to 16, causing IC23 to switch. The output from IC23 is now MSCLA (or MSCLB) divided by 32. If the START - element has disappeared, when IC22 has count to 8, the flip - flop IC10 is reset on count 9; and the bit synchronization circuit is ready to Start on a new possible START - element.

Character Synchronization Circuit.

The Character Synchronization Circuit performs a recognition and synchronization on the SYN characters, starting every message in synchronous mode.

IC1 performs a decoding of the wanted SYN - bitpattern. If this pattern is recognized IC10 is set, releasing the counter IC9.

When this counter has count eight bit together with a new recognized SYN - bitpattern, IC15 a is set (X14 := 0). The circuit blocks itself in this situation. Only a -,CLEAR pulse can restart the circuit to a new recognization sequence. If no SYN - bitpattern is recognized, when IC9 has count eight bit, IC15 a is not set and IC10 is reset. The circuit is ready to a new recognization sequence.

Normaily each message is started with 6 SYN; X14 := 0 is established on minimum 2 SYN characters.

To restart the character synchronization circuit, a WRITE-READ or SENSE 1 - READ command sequence must be issued from RC4000.

Character Divider Circuit.

In synchronous mode the signal X14 is true when the character synchronization is established (section 4.3.2.2).

Before this happens, the signal has parallel loaded the number of bits per character into counter IC17 (always 8 bits). A logical 1 is placed on the serial inputs to the shift - register IC5. When X14 := 0 RECEV CL count down in IC17 and shift a logical 1 trough IC5.

Afetr 8 shift pulses the logical 1 appears on IC5 - 13 giving the Received Data Ready (RECVD DA RDY) to the Buffer Unit.

The Buffer Unit responses with the signal ¬WRITING, clearing IC5 and loading IC17 again. The described cyklus takes place again.
In asynchronous mode a flip - flop IC11 is connected to the serial inputs to IC5. 9 shift pulses are now necessary to give RECVD DA RDY. On this way only databits (not the START - element) are stored in the buffer .

BUFFER UNIT.

For details refer TMX09, circuit diagram for PCBA 2064-1, TC13, TC14, TC15 TC16 and TC17.
The buffer is a dual 16 characters buffer performed by two dual 128 bits serial shiftregisters.
In each buffer one bit is used as datainformation carrier, while the other is used as a mark - bit, marking cells carrying valid databits. The Buffer Unit is divided into the following main parts :
Input - Circuits.
Buffer - Circuit.
Buffer Exchange Circuit.
Output Circuits.

Input Circuits.

The Input Circuits receive parallel - data from IOB (Internal Output Bus) or serial data from the transmission Line (RECVD DA) and transfer this information to one of the store - registers.
Parallel data is written into the Input Register IC7 on trailing edge of ¬WR & TR (from Control Unit). Serial data are shifted into the Input Register by SERIAL CL (from Receiver Unit.
On the trailing edge of ¬RECVD DA RDY or the leading edge of ¬WR & TR a cyklus of 8 shifts is started, transferring the contents of the Input Register into the store register, selected as INPUT BUFFER.

8 WRITE CL pulses (422 KHz) are generated to shift the INPUT BUFFER. During this operation the signal ¬WRITING is true. The WRITE CL is too generated by ¬FILL CLOCK during the CLEAR - period (500 uS).

Buffer Circuit.

The buffer circuit consists of two dual 128 bits MOS - shiftregisters IC1 and IC2. Each buffer sonsists of two parallel working 128 bits shiftregisters. One of these registers is used as data - store, while the other is used as mark - store; A Logical 0 is written in the mark - buffer, whenever a valid databit is written into the databuffer.

The two MOS - devices IC1 and IC2, called Buffer 1 and Buffer 0, take turns at working as Input Buffer, so when one buffer is filled (X7 : = 0 or X8 : = 0) it is changed to work as Output Buffer, while the Output Buffer up till now takes over the job as Input Buffer. Shiftpulses to the Input Buffer are supplied from the Input Circuits.

Shiftpulses to the Output Buffer are supplide from the Output Circuits.

So when the buffers are changed the shiftpulses are changed by the multiplexer IC9, in accordance to the following table :

X6	X5	IC9 - 7	IC9 - 9
0	0	Logical 0	Logical 0
0	1	X2	X3
1	0	X3	X2
1	1	X4	X4

When the buffers are changed the signal X1 is shifted to the new Input Buffer and the signal X9 is shifted to the new Output Buffer.

Buffer Exchange Circuit.

The Buffer Exchange Circuit determines which of the two buffers is working as Input Buffer, and when the exchange of the buffers takes place.

The output signals from the two mark - buffers (X7 and X8) and the information about which buffer is Input Buffer. (X5 and X6) is gated together in IC3 giving the signals INPUT FLAG and OUTPUT FLAG.

In a dual 2 - line - to - 4 - line decoder (IC8) the INPUT FLAG and the OUTPUT FLAG is decoded to 4 signals.

The exchange of the buffers is provocated on different ways in receive mode and transmit mode. The decoding mentioned above is of this reason performed separately for each mode of operation.

The possible situations and the correct things to do are mentioned in the following tables :

Transmit Mode.

INPUT FLAG	OUTPUT FLAG	Situation	What happens
0	0	Both buffers are perhaps empty	Shift in Input Buffer (max. 500 uS) and then END BUFFER
1	0	Output Buffer is now empty	Exchange buffers.
0	1	The buffers is just exchanged.	nothing
1	1	Both buffers are filled	OVERRUN

Receive Mode.

INPUT FLAG	OUTPUT FLAG	Situation	What happens
0	0	Both buffers are perhaps empty.	END BUFFER
1	0	Input Buffer is just filled	Exchange buffers
0	1	Input Buffer is perhaps empty	nothing
1	1	Both Buffers are filled	OVERRUN

The signal SHIFT OUT is used in the Control Unit to generate a ¬FILL BUFFER pulse (max.500 uS). In this period high speed shifts take place in the Input Buffer to look after valid data bits.

The signal CLEAR is generated by the Control Unit (500 uS). When CLEAR is true both buffers are selected as Input Buffers and a Logical 1 is placed in all positions of the two Mark - buffers by the X4 connected to both device (IC1 and IC2) in this situation. The result is a clearing of the buffers.

Output Circuit.

The output circuits transfer information from the OUTPUT REGISTER (IC11) to the Internal Input Bus (IBA) and synchronize the transfer of information bit by bit to the Transmitter Unit.

Parallel transfer of information to the Internal Input Bus is performed by the signal OUTGATE. The trailing edge of READ & ACTIVATE will start a cyklus of 8 READ CLOCK pulses (X2) to the Output Buffer, shifting a whole character into the Output Register (IC11) . In transmit mode (RQTS : = 1) X2 is the inversion of ¬BIT REQ from the transmitter unit.

CONTROL UNIT.

For details refer to TMX10, circuit diagram for PCBA2067-1, TC12,TC13, TC14, TC15,TC16 and TC17.

The Control Unit consists of circuits controlling the three other units.

The Control Unit is divided into the following main parts :

Device Select and Mode control circuits.

Interrupt circuits.

Time out circuits.

Status and Exception Registers.

Device Select and Mode - control circuits.

Selection of a MSTC controller takes place just as a selection of a LSTC controller. The address - decoder in the TMX sends a ¬SEL signal to the controller in question.

When ENABLE is true, SEL set the flip - flop IC17 giving the signal OUTGATE to connect the outputs from the status - register in the Control Unit and the dataoutputs from the Buffer Unit to the Internal Input Bus.

The MSTC controller can operate in one of the following three modes : Receive, Transmit or Neutral.

A WRITE - command generates the signal ¬WR & TR. The leading edge of ¬WR & TR gives from the Transmitter Unit REQTS (REQUST TO SEND) to activate the connected modem. If the modem is not already activated to transmit (REQTS : = 0), the trailing edge of ¬WR & TR starts a 500 uS CLEAR-pulse to the Buffer Unit.

On response, to REQTS the modem sends the signal RDYFS (Ready For Sending), and the next leading edge of TRMCL set IC18 (X31 : = 1) to indicate that the controller is in Transmit Mode.REQTS is reset by ¬RREQTS, generated in 3 situations :

1. A READ - command is decoded (IC22-9 : = 1) and the buffer is total empty (X13 : = 1).
2. A SENSE 1 - command to the controller in question is decoded, and the buffer is empty.
3. POW OK : = 0.

The result of 1. is , that the MSTC controller is set to Receive Mode, when ¬REQTS : = 1. The result of 2. and 3. is, that the MSTC is set to Neutral mode, when ¬REQTS : = 1.

A READ - command will set flip - flop IC22, when SEL : = 1, and the controller is then in Receive Mode (¬RECVM : = 0). In this mode both WRITE - and SENSE 1 commands are accepted and immediately executed. The trailing edge of ¬WR & TR reset IC22 (¬RECVM : = 1) .

A SENSE 1 command will reset IC22 - 9 and set IC22 - 5, when SEL : = 1 . ¬REQTS : = 1 gives then ¬NEUTRM : = 0 (Neutral Mode).

TIME OUT AND INTERRUPT CIRCUITS

An interrupt pulse from the monostable circuit IC4 is delivered in different situations :

1. Transmit mode (X32 : = 1).

   a. When a buffer exchange takes place. The buffer exchange signal (¬EXCHB) from the buffer unit will place a logical 1 on IC9 - 9 and the signal X41 trigger the monostable IC4.
   X55 on the other side clear IC9.

   b. When the signal DATA SET READY signal is not received from the attached modem within 300 msec after switching from neutral mode. The leading edge of X20 (¬NEUTRM) will set IC28 - 5 : = 1 releasing the counter IC26. Input frequency to this counter is 50 Hz. On count 15 a trigger - pulse on X41 will activate IC4. The response from RC4000 is a SENSE 1 - command (X36 : = 1) to clear IC28. If DATA SET READY appears within 300 mS, IC28 is too cleared, resetting IC26.

   c. When both input and output buffer is empty. IC18-9 is set to logical 1 on the leading edge of X13.

2. Receive mode (¬RECVM : = 0).

a. Same as 1. - a.

b. Same as 1. - b.

c. When both input and output buffer is total filled .

IC9 - 5 is set to logical 1 on the leading edge X49 (occurs when both INPUT FLAG : = 1 and OUTPUT R FLAG : = 1).

d. When the 1 sec. timer terminates.

TIME OUT CIRCUITS.

1. 100 mS input timer. This circuit consists of a monostable IC5 triggered by the signal ¬RECVD DA RDY from the receiver unit (true whenever a character is received).

If the time between two characters is longer than 100 mS, the monostable terminates (IC5 - 12 shift to logical 1) setting IC15 - 9. The monostable IC5 - 13 is started giving the signal ¬FILL BUFFER . ¬FILL BUFFER will in the buffer unit cause a shift in the input buffer. IC15 - 13 is cleared before termination, if valid databits are found in the input buffer (Input Flag shifts to logical 1).

IC5 - 13 is in transmit mode started by the signal SHIFT OUT (true when both INPUT FLAG : = 0 and OUTPUT FLAG : = 0) and the termination of IC5 - 13 will set IC24 if the condition INPUT FLAG : = 0 & OUTPUT FLAG : = 0 (IC10 - 10 : = 1).

2. 1 sec. timer.

This circuit consists of a counter IC19. The input frequency to this counter is 6,25 HZ.

This counter is started by a READ - command ; the leading edge of IC27 - 10 will set IC24 - 8 : = 0 if IC5 - 12 : = 1.

STATUS REGISTER.

The contents of the Status Register is transferred to RC4000 by a SENSE 0 command.

1. Status bit 0 : END BUFFER . In receive mode this status bit indicates that the output buffer is empty and the input buffer perhaps is empty too. When the last character is read out from the output buffer by a READ command the signal OUTPUT FLAG switches to logical 0; if INPUT FLAG is 0 X46 switches to logical 1 releasing IC8; on the next READ command IC8 - 9 is set to logical 1. A SENSE 0 command will then set IC8 - 5, given END BUFFER status to RC4000. The END BUFFER is so not transferred together with a valid datacharacter. The END Buffer is reset again when X46 : = 0 (INPUT FLAG : = 1 or OUTPUT - FLAG : = 1).

   In transmit mode this status bit indicates that both input buffer and output buffer is total empty. When the situation INPUT FLAG : = 0 and OUTPUT FLAG : = 0 occurs the timer IC5 - 13 is started to look after valid data in the input buffer ; if this timer terminates and the situation mentioned above is still true X13 switches to logical 1 given END BUFFER status.

2. STATUS bit 1 : PARITY ERROR.

   (refer to logical diagram TMX13) . Indicates that the parity of the character received is wrong. The parity check circuit on POS.17 (AJ451) checks always EVEN parity. The correct parity is ODD (EVEN) in synchronous (Asynchronous) transmission mode. Of this reason the received parity bit is always inverted in synchronous mode (in the buffer unit).

3. STATUS bit 2 : TIME OUT.

   Indicates that no input has occurred within 1 sec after the set up a READ command. The signal X40 is true when the 1 sec timer terminates (IC19). A SENSE 0 command will then set IC2 given TIME OUT status IC2 is reset by the signal X2 (ENABLE).

4. STATUS BIT 3 : OVERRUN

Indicates that the input buffer is full and the output buffer is full or not yet total emptied.

INPUT FLAG : = 1 and OUTPUT FLAG : = 1 gives true condition to IC2 - 12. A SENSE 0 command will set IC2 - 5 given OVERRUN status.

5. STATUS BIT 4 : CARRIER DOWN.

Indicates that the modem has detected that no carrier is being received. This status bit is allways set in transmit mode, while in receive mode it follows the modem signal DATA CARRIER DETECTOR.

6. STATUS BIT 5 : DATA SET NOT READY.

Indicates that the modem is not ready within 300 mS after setting up transmit or receive mode, or that a fall-out of the modem has lasted more than 300 msec. This status bit is stored in IC28 - 9. IC28 - 9 is set by the signal X53, true when the counter IC26 reaches count 15. IC28 - 9 is reset by X37, true when a SENSE 1 command is set up.

7. IO READY (IC6 - 8).

Indicates whether the device is busy or not.

The device is busy in three situations :

a. When a character is written into the buffer (¬WRITING : = 0)

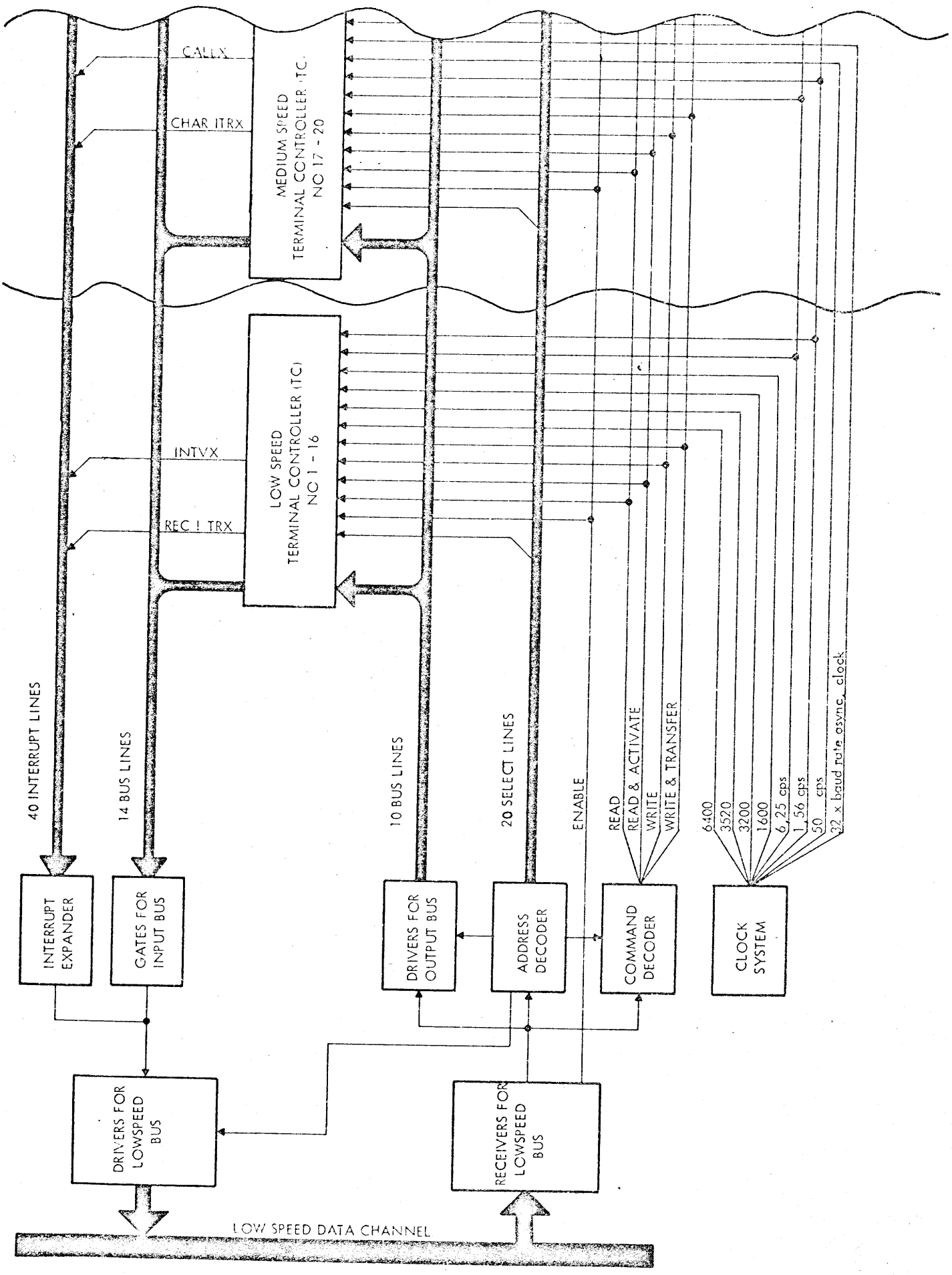
b. When a character is read out from the buffer (¬READING : =0)

c. In clear buffer situations (¬FILL BUFFER : = 0).

8. IO CONNECTED (IC6 - 3).

This signal is simply an inversion of outgate. A medium speed terminal controller is always connected.

DEPENDING ON THE NO. OF TERMINALS INSTALLED THE TMX425 WILL HAVE FROM 1 TO 20 TERMINAL CONTROLLERS .



TMX425

R 20848

TELEMULTIPLEXER 425
Block Diagram
Figure

Fig. 1

TMX425

R 20849

SIGNALS ON INTERNAL OUTPUT BUS

Figure Fig. 2

IOB no.	To LOW SPEED TERMINAL CONTROLLER				To MEDIUM SPEED TERMINAL CONTROLLER			
	IO ADDRESS		NOT IO ADDRESS		IO ADDRESS		NOT IO ADDRESS	
	8 Bit	5 Bit	8 Bit	5 Bit	8 Bit		8 Bit	
10	1	1	0	0	×		0	
9	0	1	1	0	×		1	
8	0	1	BUS P	0	×		BUS P	
7	0	1	BUS 17	0	×		BUS 17	
6	0	0	BUS 18	1	×		BUS 18	
5	0	0	BUS 19	BUS 19	×		BUS 19	
4	0	0	BUS 20	BUS 20	×		BUS 20	
3	0	0	BUS 21	BUS 21	×		BUS 21	
2	0	0	BUS 22	BUS 22	×		BUS 22	
1	0	0	BUS 23	BUS 23	×		BUS 23	

BUS No.	From LSTC's OUTGATE = 1		From MSTC's OUTGATE = 1	inf. is transferred to LSD by	
	8 bit	5 bit		SENSEOX transfer	IO address
1	b 1	1	b 1	x	
2	b 2	1	b 2	x	
3	b 3	0	b 3	x	
4	b 4	b 1	b 4	x	
5	b 5	b 2	b 5	x	
6	b 6	b 3	b 6	x	
7	b 7	b 4	b 7	x	
8	bP	b 5	bP	x	
9	0		0		
10	Time Out		Time Out	x	
11	Connected		Connected		x
12	Ready		Ready		x
13	HALF DUPLEX		End Buffer	x	
14	8 bit	8 bit	8 bit		
15	0		OVERRUN	x	
16	0		Carrier down	x	
17	0		DATA SET NOT READY	x	

TMX425

R 20691

Signal on the internal input BUS

Fig. 3

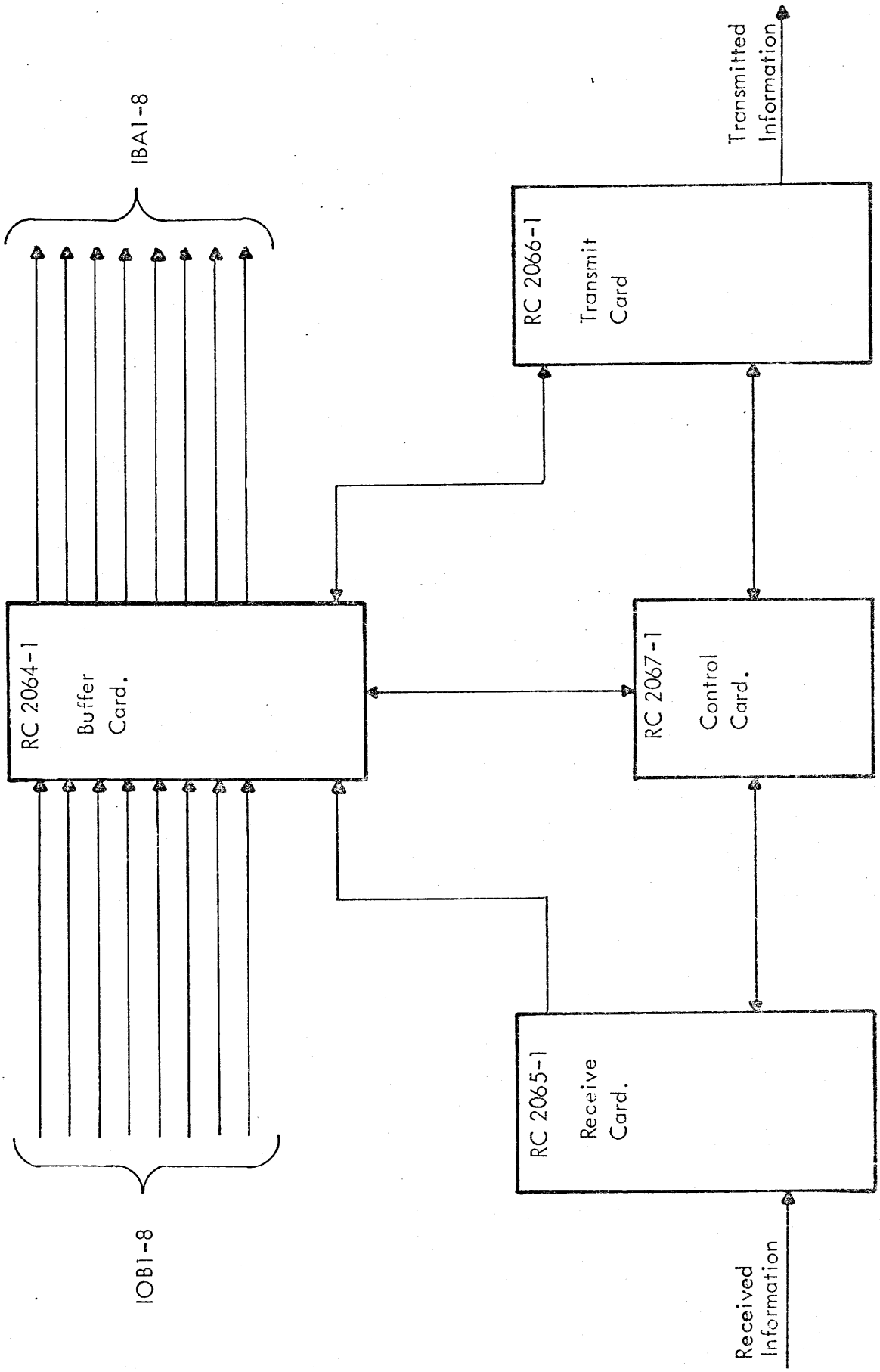
Figure

IC BUS	DATA 8 bit senseoxtranf	DATA 5 bit	STATUS SENSEO	DEV. ITR. A ITR. REG. 0 CHAR ITR	DEV. ITR. B ITR. REG. 1 KEY ITR
0			END BUFFER	FIN DEV 1	INTV DEV 1
1	Parity Error			FIN DEV 2	INTV DEV 2
2			Time Out	FIN DEV 3	INTV DEV 3
3			OVERRUN	FIN DEV 4	INTV DEV 4
4			Carrier down	FIN DEV 5	INTV DEV 5
5			DATA SET NOT READY	FIN DEV 6	INTV DEV 6
6				FIN DEV 7	INTV DEV 7
7				FIN DEV 8	INTV DEV 8
8				FIN DEV 9	INTV DEV 9
9				FIN DEV 10	INTV DEV 10
10				FIN DEV 11	INTV DEV 11
11				FIN DEV 12	INTV DEV 12
12				FIN DEV 13	INTV DEV 13
13				FIN DEV 14	INTV DEV 14
14				FIN DEV 15	INTV DEV 15
15				FIN DEV 16	INTV DEV 16
16	IBB 8			CHAR ITR 17	
17	IBB 7				CALL ITR 17
18	IBB 6			CHAR ITR 18	
19	IBB 5	IBB 8			CALL ITR 18
20	IBB 4	IBB 7		CHAR ITR 19	
21	IBB 3	IBB 6			CALL ITR 19
22	IBB 2	IBB 5		CHAR ITR 20	
23	IBB 1	IBB 4			CALL ITR 20

TMX425
R 20692

SIGNALS GENERATED IN THE MTMX
TO THE LOW SPEED DATA CHANNEL
Figure

Fig. 4



TMX425 MSTC Block Diagram Fig. 5

R 20850 Figure

RCSL : 44-RT 609
PP : 1:15
Editor : Knud Sørensen
Edited : April 1973

TIMING CHARTS
TMX 425
LOW/MEDIUM TELEMULTIPLEXER

Keywords: RC 4000, TMX 425 telemultiplexer, timing charts.

Abstracts: This paper contains a number of timing diagrams for some typical operations of the RC 4000 telemultiplexer, TMX 425.

CONTENTS DWG.NO.

TMX425

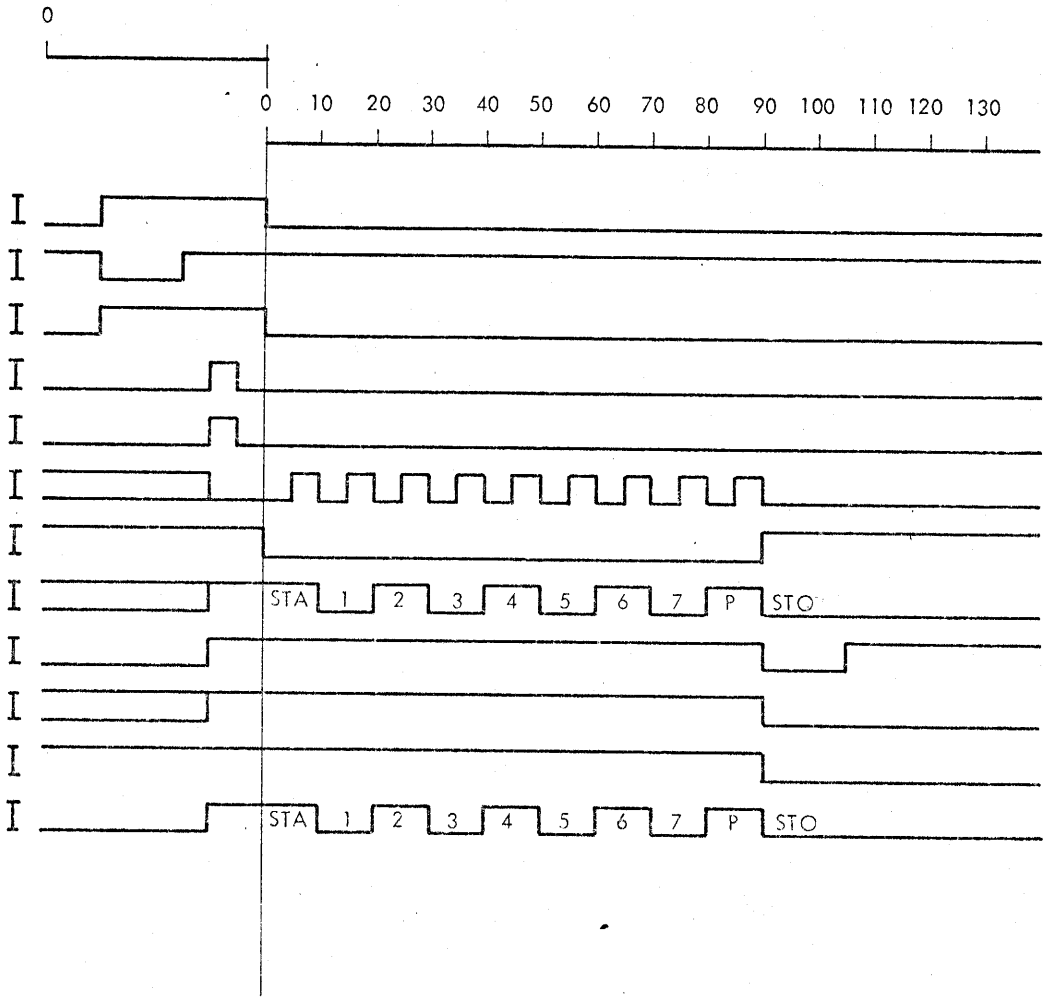
A11191

TIMING FOR OUTPUT OF THE LETTER U (ISO NO 5) TO TERMINAL NO 1

100 BSP

Timing Chart

TIME	
TIME mS	
IO ENABLE	TMX 01, 1H26
⁻SEL DEV 1	TMX 02, 6-7
OUTGATE 1	TMX 06, 53-16
WRITE ! TRANSFER	TMX 03, 1M40
IN TRANSFER 1	TMX 06, 53C15
SHIFT PULSE 1	TMC 06, 53M37
⁻(REC ! TR) 1	TMX 06, 53-10
⁻TRANSMITTED DATA A1	TMX 05, 27G41
⁻STOP 1	TMX 05, 27-29
⁻END TRANSMIT 1	TMX 05, 27-38
⁻TRANSMITTED DATA B1	TMX 05, 27H35
TRANSMITTED DATA 1	TMX 23, 89A4

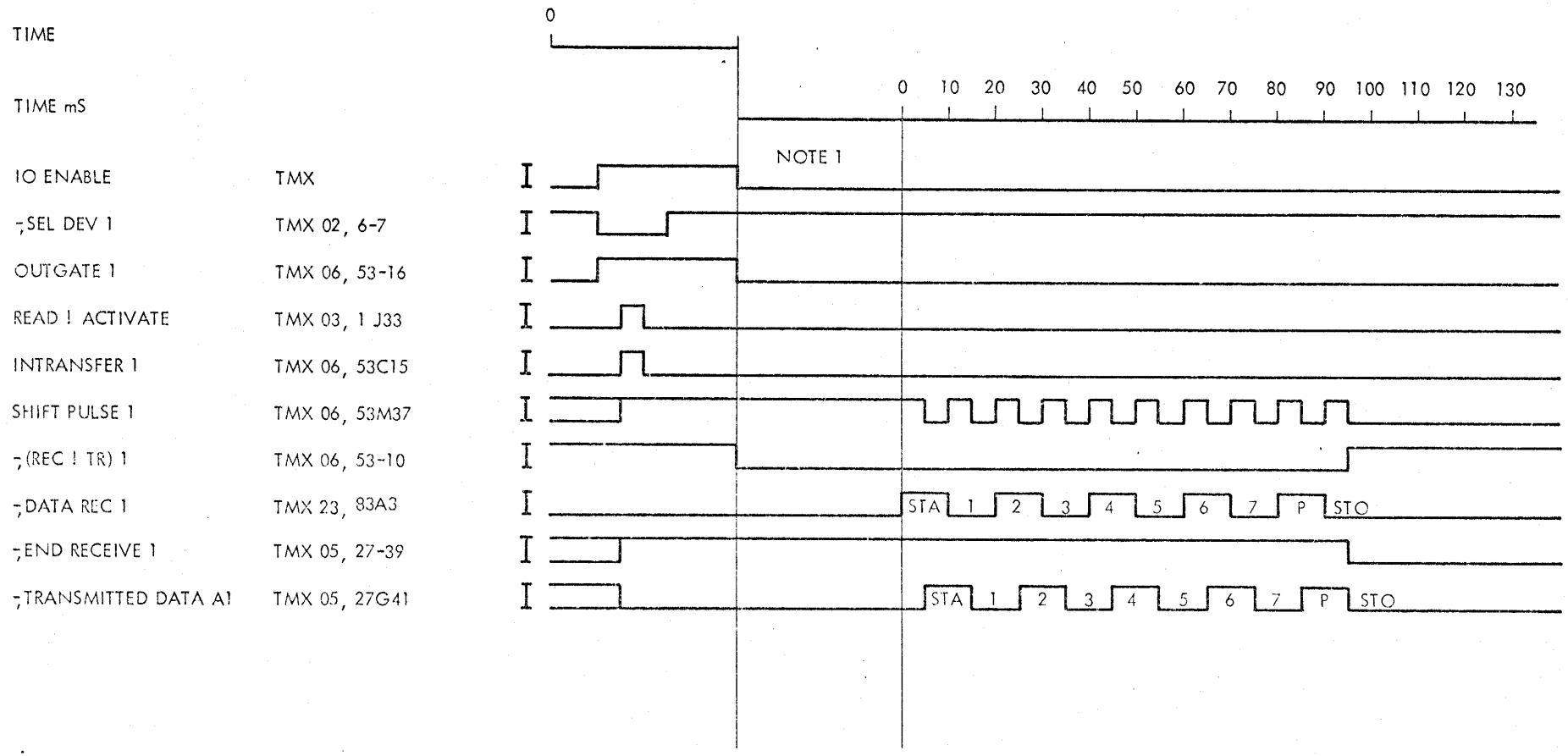


TC1

TMX425

A11192

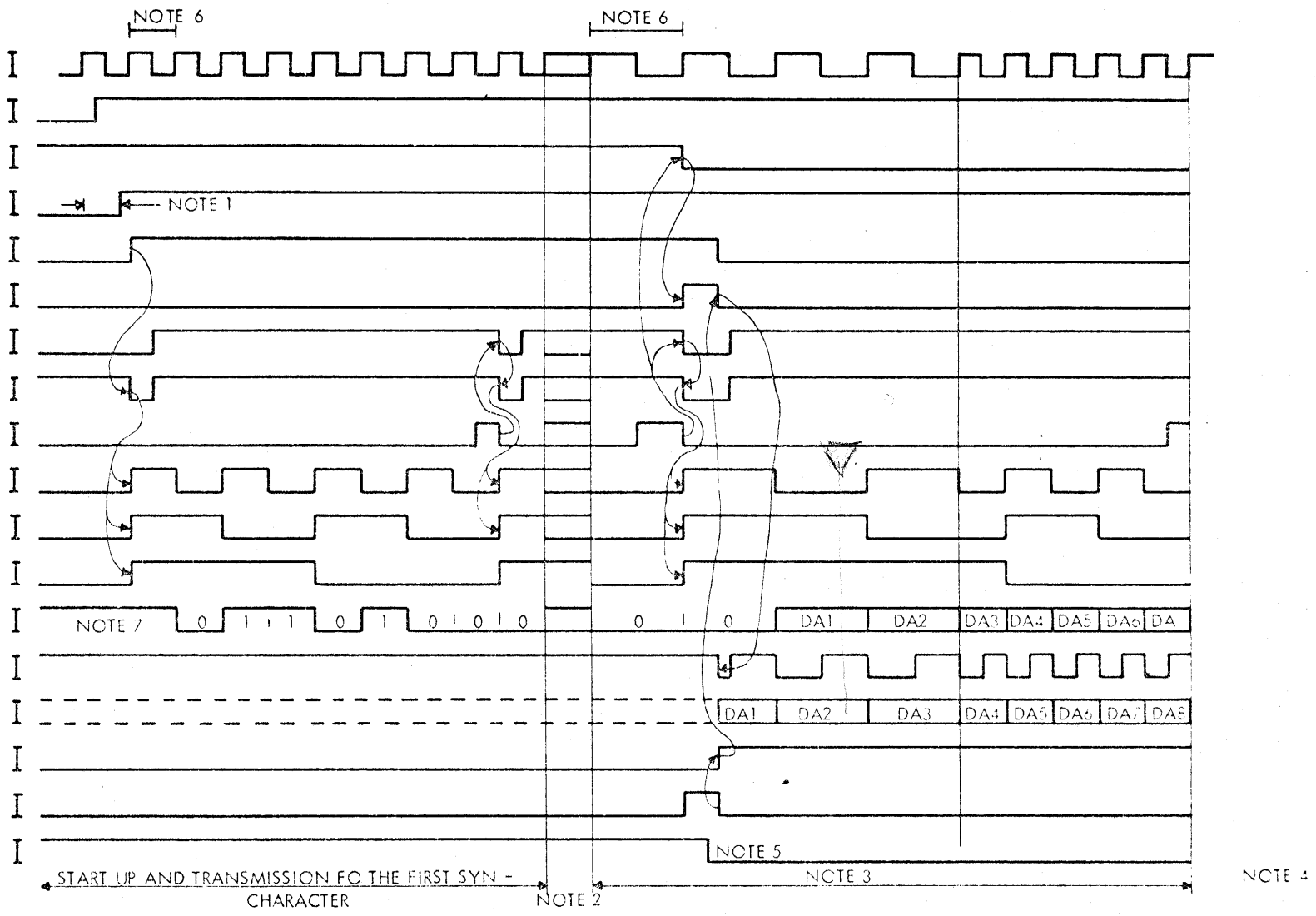
TIMING FOR INPUT OF LETTER U (ISO NO 5) FROM TERMINAL NO 1
100 BSP
Timing Chart



NOTE 1 : This time is variable, and determined by the arrival of the leading edge of incomming data.

TC2

TRANSFER OF CHARACTERS IN SYNCHRONEOUS MODE
PART 1
Timing Chart



NOTE 1 : Time depending of the used modem (typ. 200mS).

NOTE 2 : After start up 6 SYN characters at all are transmitted.

NOTE 3 : Transmission of data characters from the buffer is started.

NOTE 4 : continue on TC4.

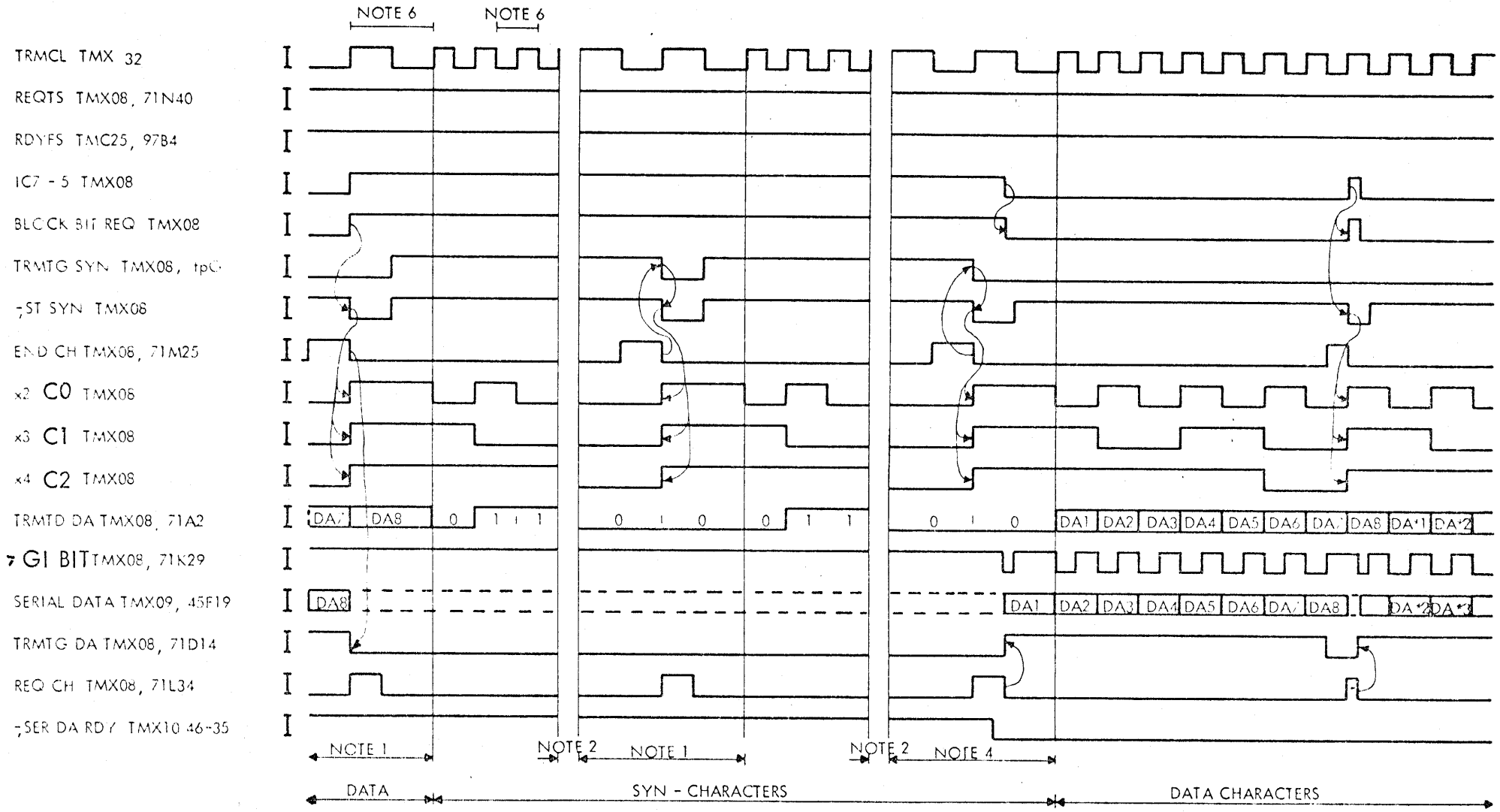
NOTE 5 : Serial data must be ready before the trailing edge of REQ CH. (a 35 uS pulse).

NOTE 6 : DURATION OF TIME STEPS IS BY :

2400 bps	417 uS
4800 bps	208 uS

NOTE 7 : The bit pattern for the ISO - SYN characters is shawn.

TRANSFER OF CHARACTERS IN SYNCHRONOUS MODE
PART 2
Timing Chart



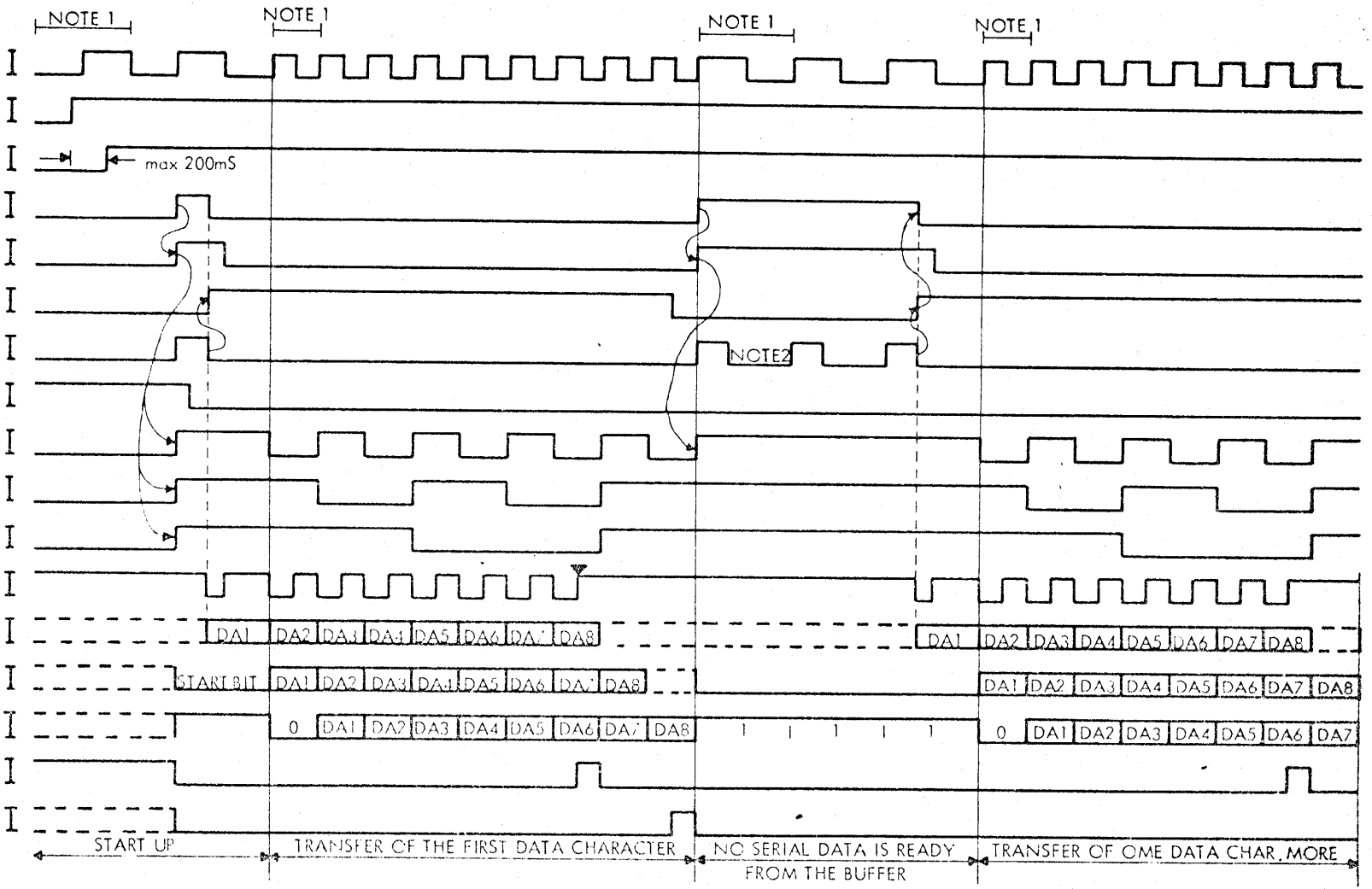
NOTE 1 : No valid ¬SER DA RDY is received before the trailing edge of REQ CH. Therefore SYN - characters will be transferred until a valid ready signal is received.

NOTE 2 : Bit 4 - 5 - 6 of the SYN - character are transferred in this period.

NOTE 4 : A valid ¬SER DA RDY is received and transmission of data characters form the buffer is started.

NOTE 5 : Serial data must be ready before the trailing edge of REQ CH (a 35 uS pulse).

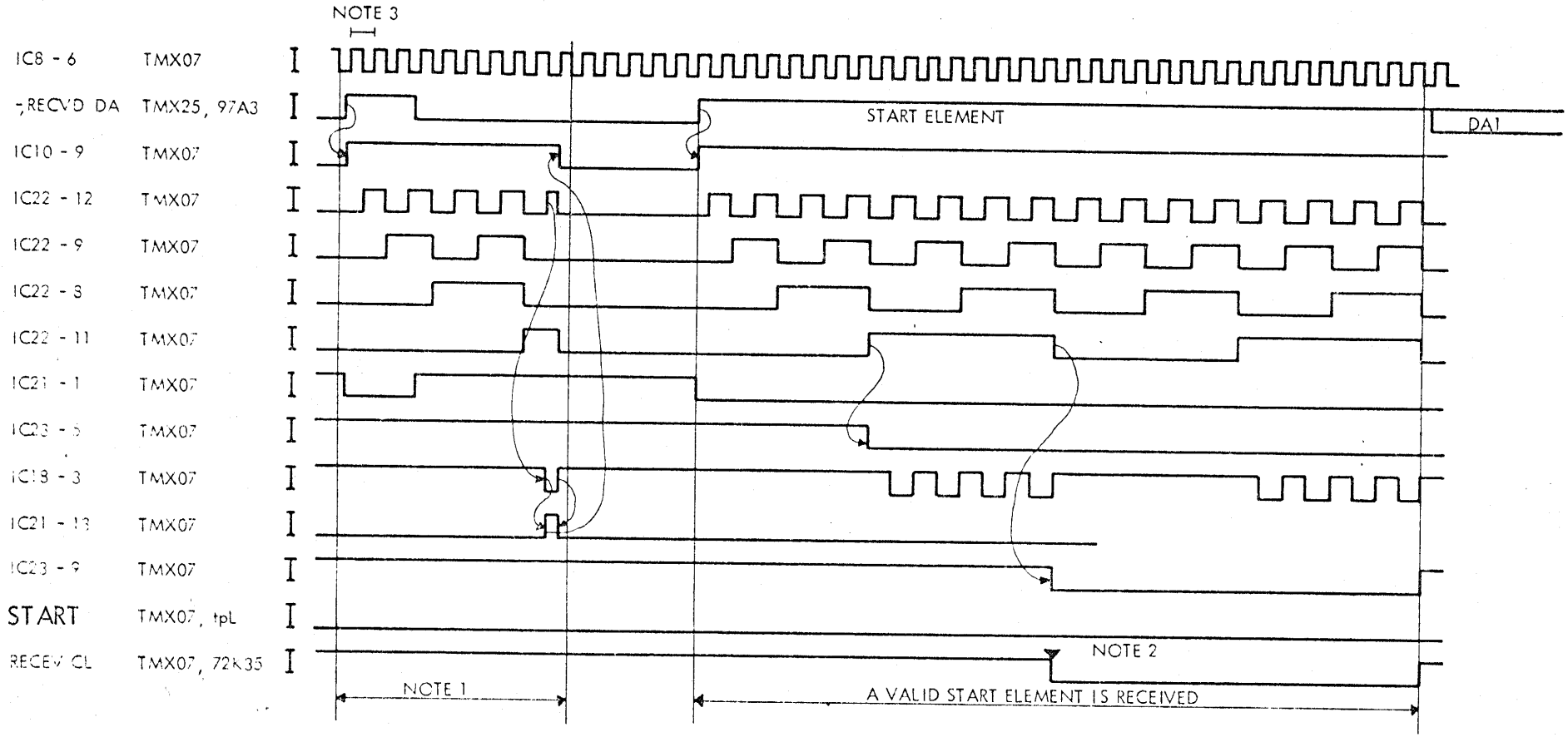
NOTE 6 : DURATION OF TIME STEPS IS BY :
2400 bps - 417 uS
4800 bps - 208 uS



NOTE 1 : Duration of steps is by :
600 bps 1667 uS
1200 bps 834 uS

NOTE 2 : If no serial data is ready from the buffer card the REQ CH (REQuest CHaracter) pulse comes on every trailing edge of TRMCL.
The length of REQ CH is about 35 uS.

BIT - SYNCHRONIZATION IN ASYNCHRONOUS MODE
RECEIVER UNIT
Timing Chart

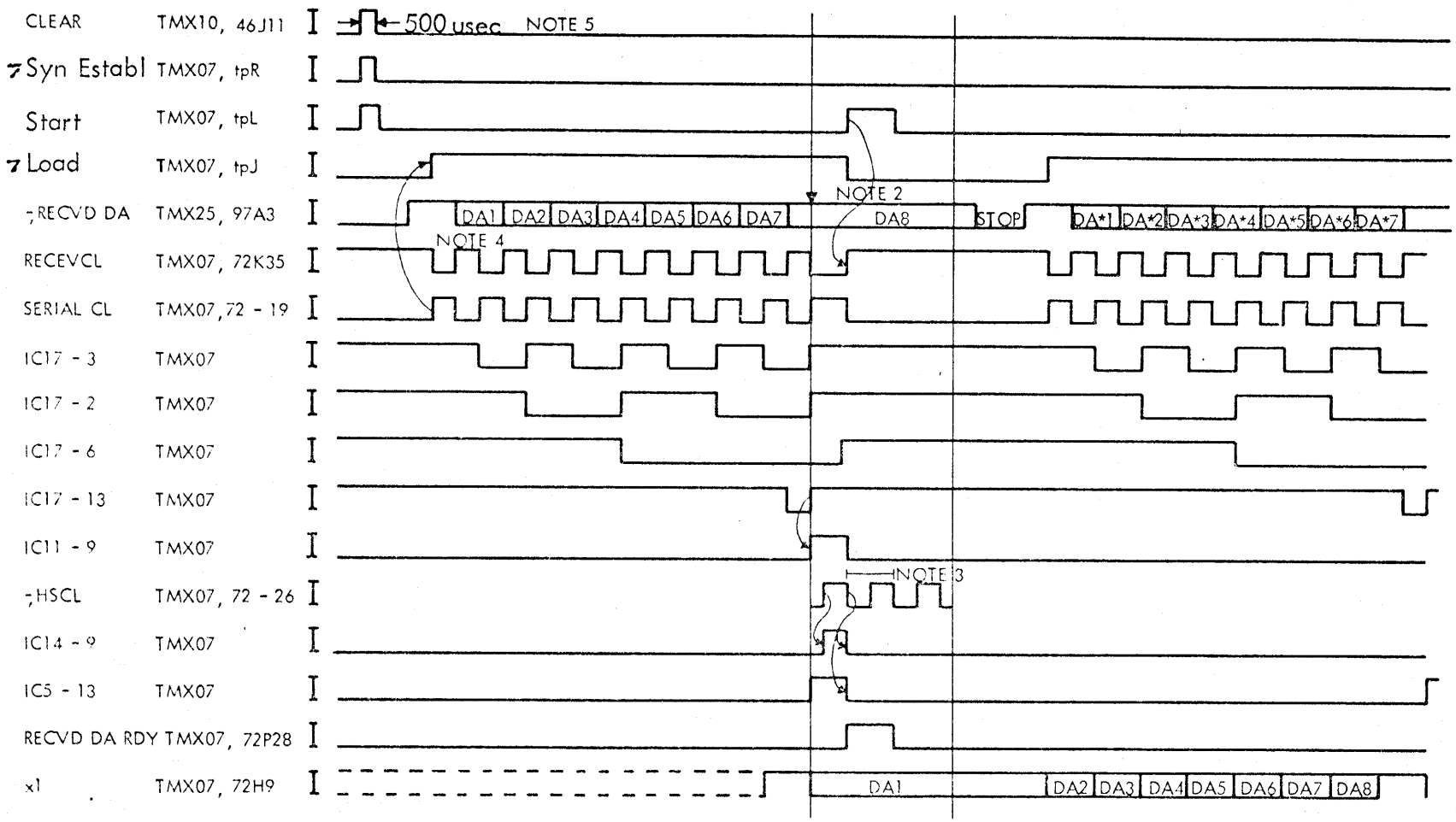


NOTE 1 : If a START ELEMENT SHORTER THAN A 1.4 bit-period is received, it will be ignored as shown.

NOTE 2 : This edge of RECVCL represent the bit - center.

NOTE 3 : Duration of steps is by :
600 bps = 52 uS
1200 bps = 26 uS.

INPUT OF DATA CHARACTERS IN ASYNCHRONOUS MODE
RECEIVER UNIT
Timing Chart



NOTE 1 : The time between the trailing edge of CLEAR and the trailing edge of START is max. 1 period. of ⏊HSCL (High Speed Clock = 3,3792 MC).

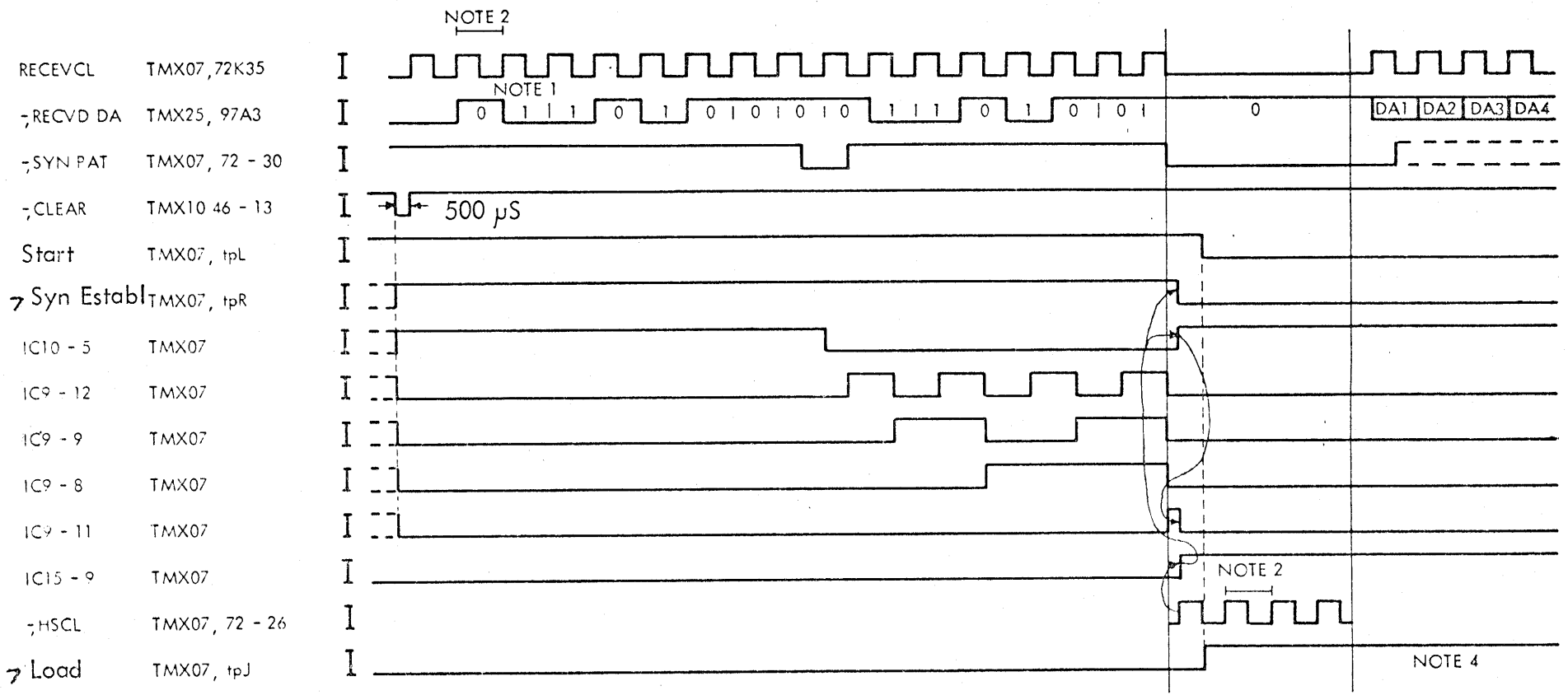
NOTE 2 : The Center of bit no. 8

NOTE 3 : 1 period of ⏊HSCL (3,3792 MC)

NOTE 4 : The duration of the time steps for RECVCL is by :
600 bps = 1667 uS
1200 bps = 834 uS

NOTE 5 : CLEAR is generated when the MSTC is switched to receive mode.

CHARACTER SYNCHRONIZATION IN SYNCHRONOUS MODE
RECEIVER UNIT
Timing Chart



NOTE 1 : The bitpattern for ISO - SYN character is shown.

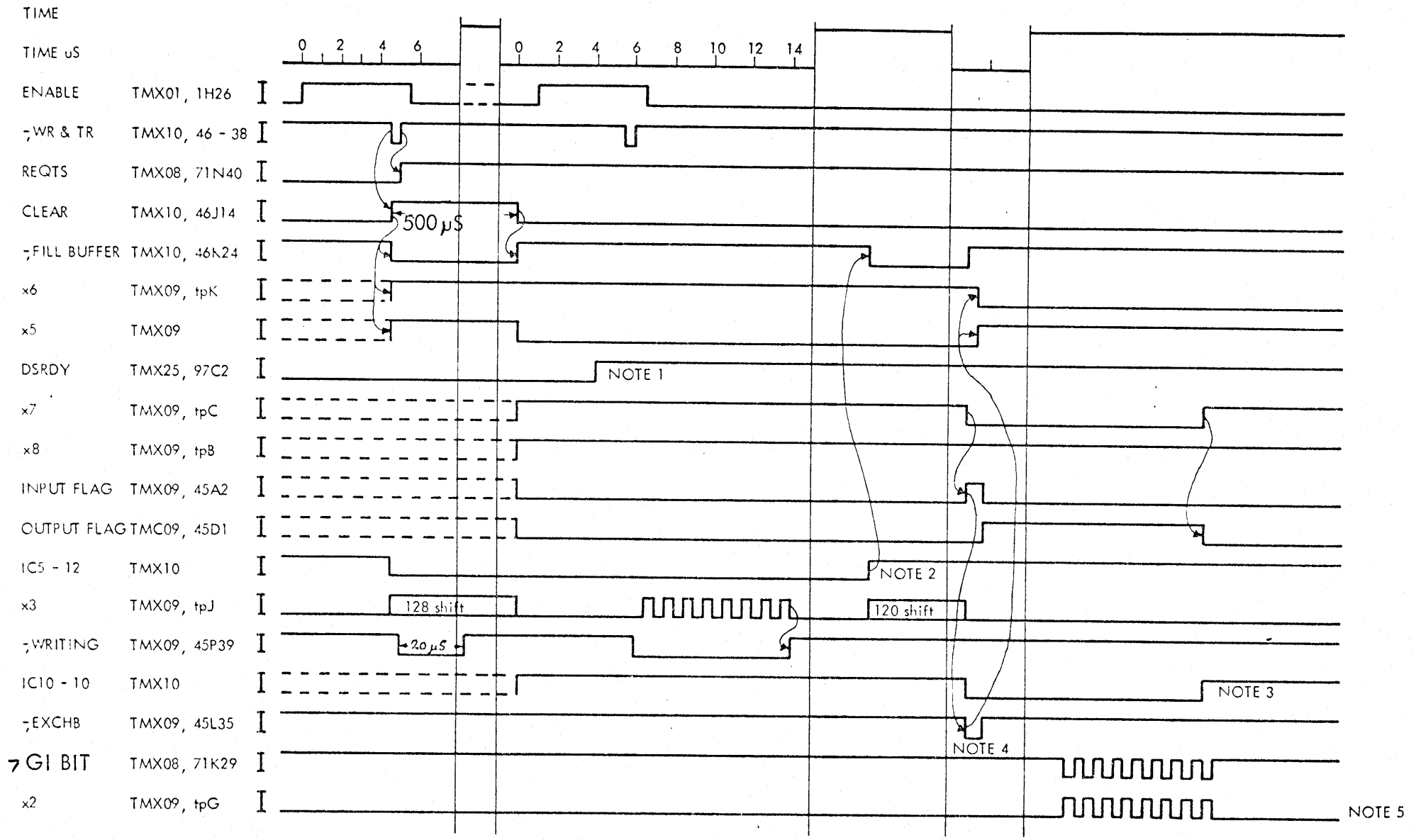
NOTE 2 : The duration of the time steps for RECVCL is by :
2400 bps - 417 uS
4800 bps - 208 uS

This clock is supplied from the connected modem.
The trailing edge corresponds to the bitcenter, and the leading edge to data shift.

NOTE 3 : 1 period of the High Speed Clock (3,3792 MC).

NOTE 4 : The timing chart is continued on TC11.

TRANSMITTING OF ONLY ONE CHARACTER
CONTROL UNIT AND BUFFER UNIT
Timing Chart



NOTE 1 : max 200mS after REQTS

NOTE 2 : 100mS after the last WRITE- command, starts a 500uS shift in the input buffer to look after same valid

NOTE 3 : This situation interrupts RC4000 with STATUS bit 0 END BUFFER true

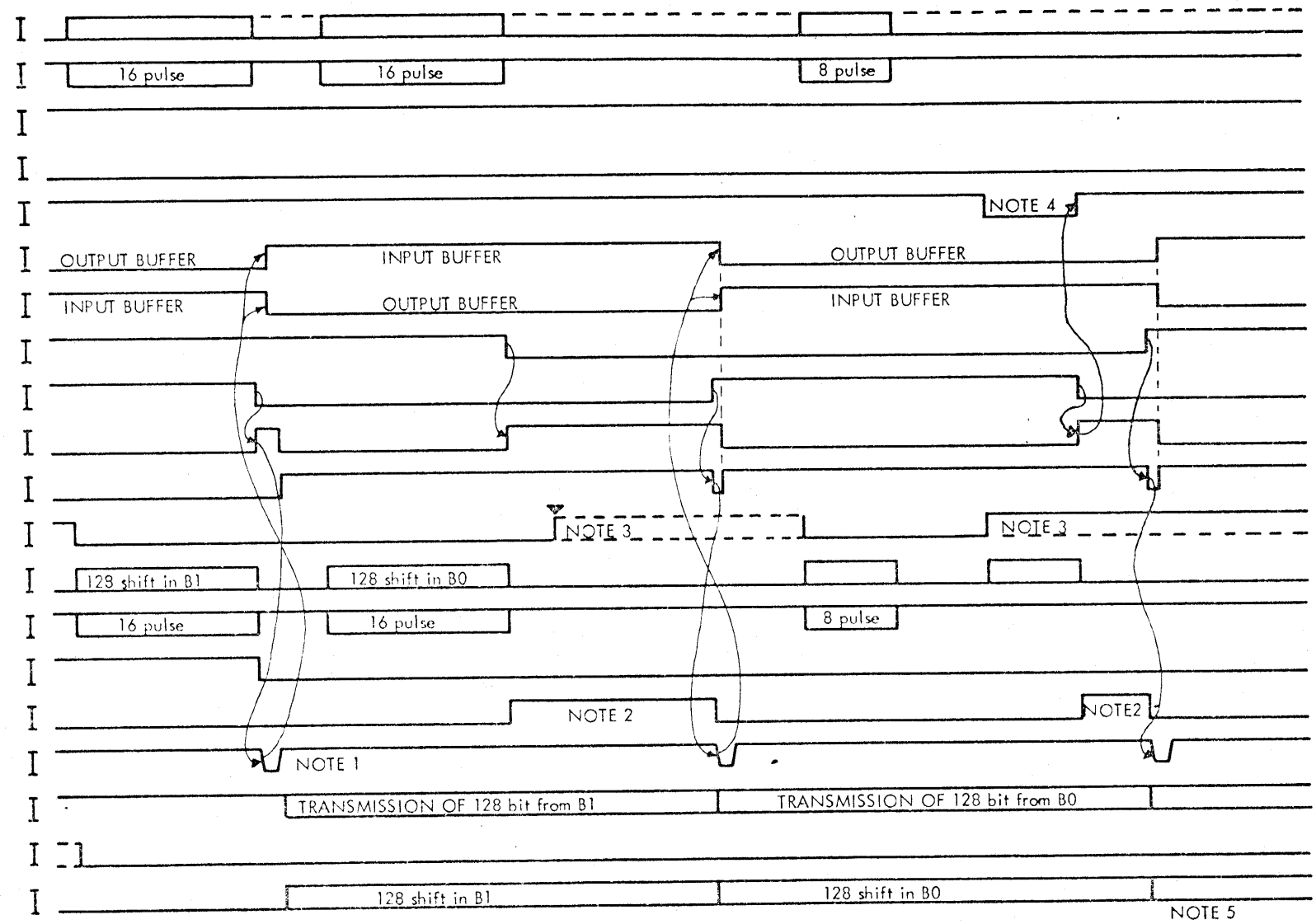
NOTE 4 : Interrupt with STATUS bit END BUFFER false.

NOTE 5 : Continue on TC14

TMX425

TRANSMISSION OF CHARACTERS CONTROL UNIT AND BUFFER UNIT

Timing Chart



NOTE 1 : Interrupt with status bit 0 END BUFFER false and status bit 3 OVERRUN false.

NOTE 2 : This situation is indicated by STATUS bit 3 OVERRUN true

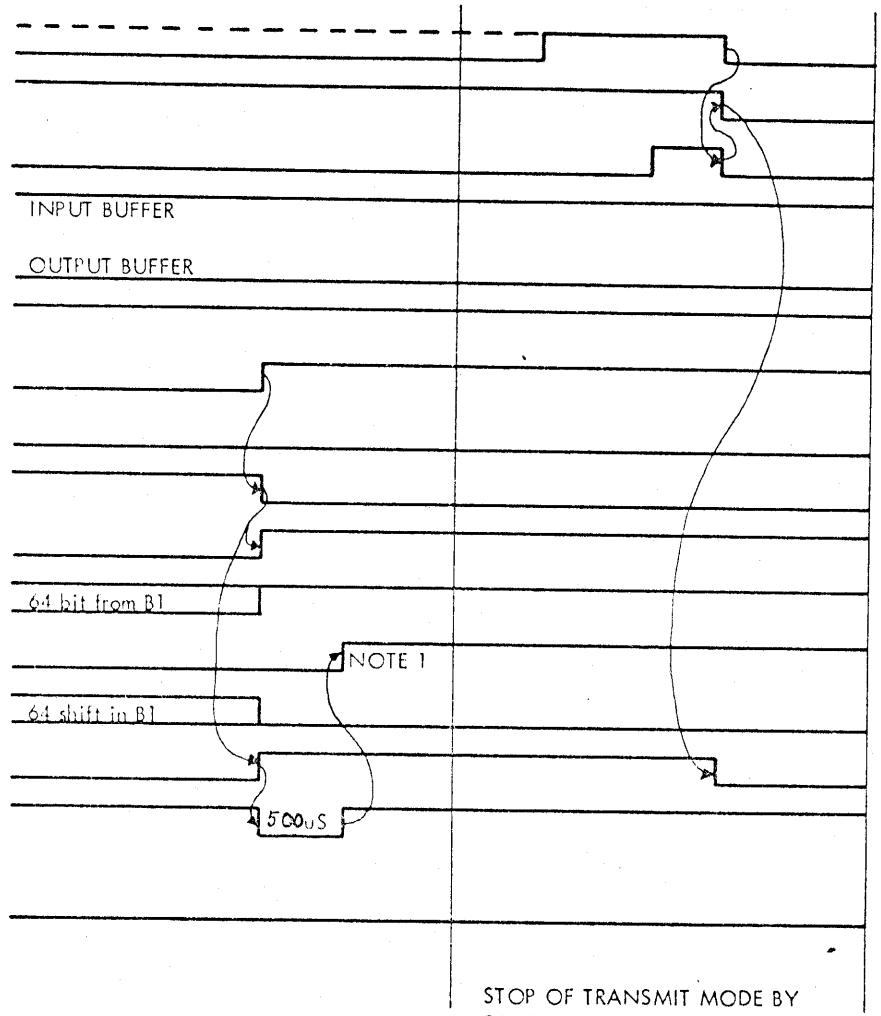
NOTE 3 : Depending upon the transmission speed

NOTE 4 : Shift in the Input Buffer to look after some valid data bits, Is started by 100 msec. Timer or by SHIFT OUT depending upon The transmission speed.

NOTE 5 : Continue on TC15

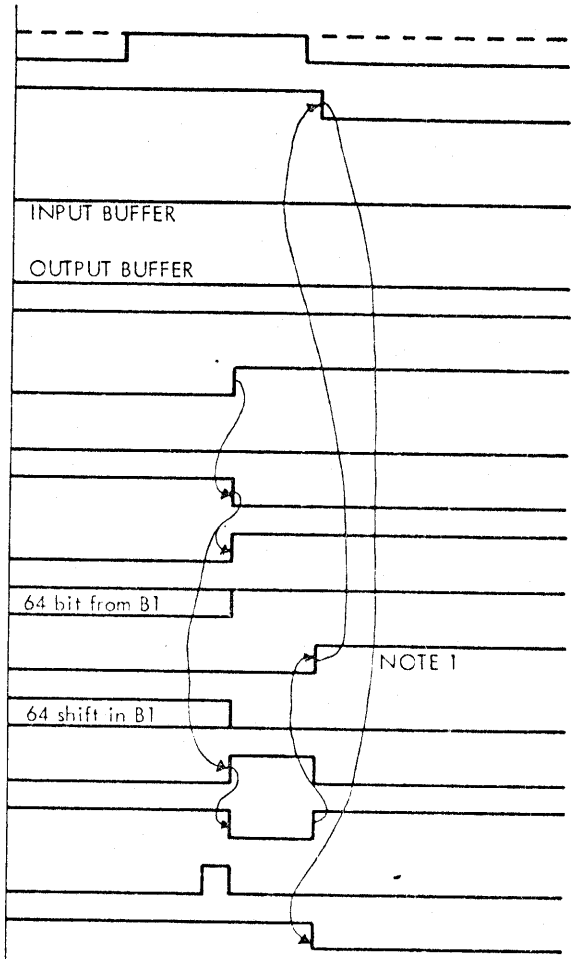
STOP OF TRANSMIT MODE BY SENSE 1 AND READ COMMANDS
CONTROL UNIT AND BUFFER UNIT
Timing Chart

ENABLE	TMX01, 1H26
REQTS	TMX08, 71N40
SENSE 1	TMX03, 5B14
x6	TMX09, tpK
x5	TMX09
x7	TMX09, tpC
x8	TMX09, tpB
INPUT FLAG	TMX09, 45A2
OUTPUT FLAG	TMX09, 45D1
IC10 - 10	TMX10
¬G1 BIT	TMX08, 71K29
IC24 - 5	TMX10
x2	TMX09, tpG
SHIFT OUT	TMX09, 45N38
¬FILL BUFFER	TMX10, 46K24
READ & ACTIVATE	TMX03, 1J38
¬RECVM	TMX10, 46H18



NOTE 1 : Interrupt with status bit 0 END BUFFER true.

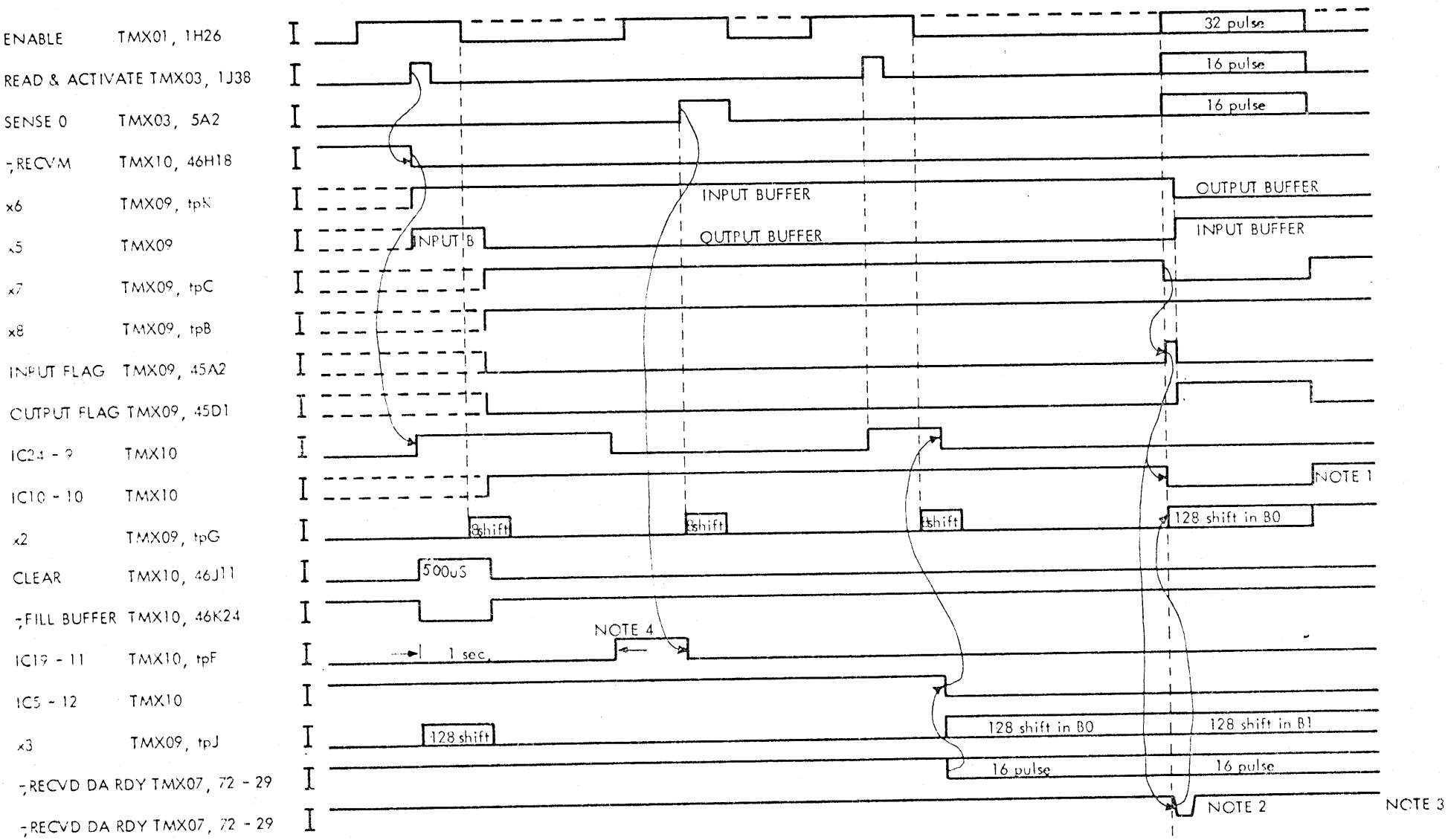
STOP OF TRANSMIT MODE BY SENSE 1 - COMMAND.
The controller switches to neutral mode.



STOP OF TRANSMIT MODE BY READ - COMMAND
The controller switches to Receive - mode.

START OF RECEIVE - MODE CONTROL UNIT AND BUFFER UNIT

Timing Chart



NOTE 1 : This situation is indicated by status bit 0 END BUFFER true No valid data character is transferred in this STATUS - WORD.

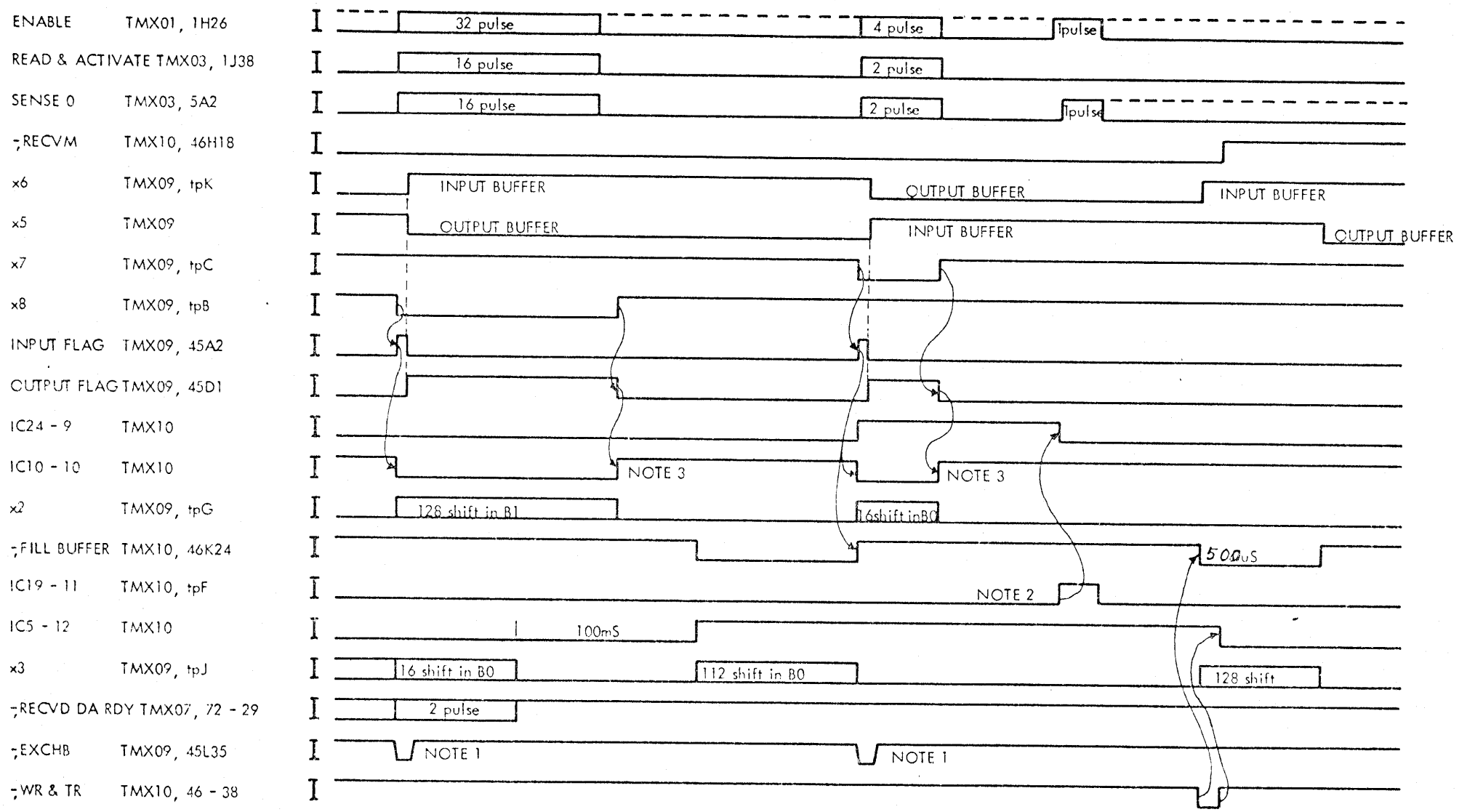
NOTE 2 : Interrupt with status bit 0 END BUFFER false.

NOTE 3 : Continue on TC17

NOTE 4 : Interrupt with Status bit 2 TIME OUT true.

RECEIVE MODE CONTROL UNIT AND BUFFER UNIT

Timing Chart



NOTE 1 : Interrupt with Status bit 0
END BUFFER false

NOTE 2 : Interrupt with Status bit 2
TIME OUT true.

NOTE 3 : Interrupt with Status bit 0
END BUFFER true.

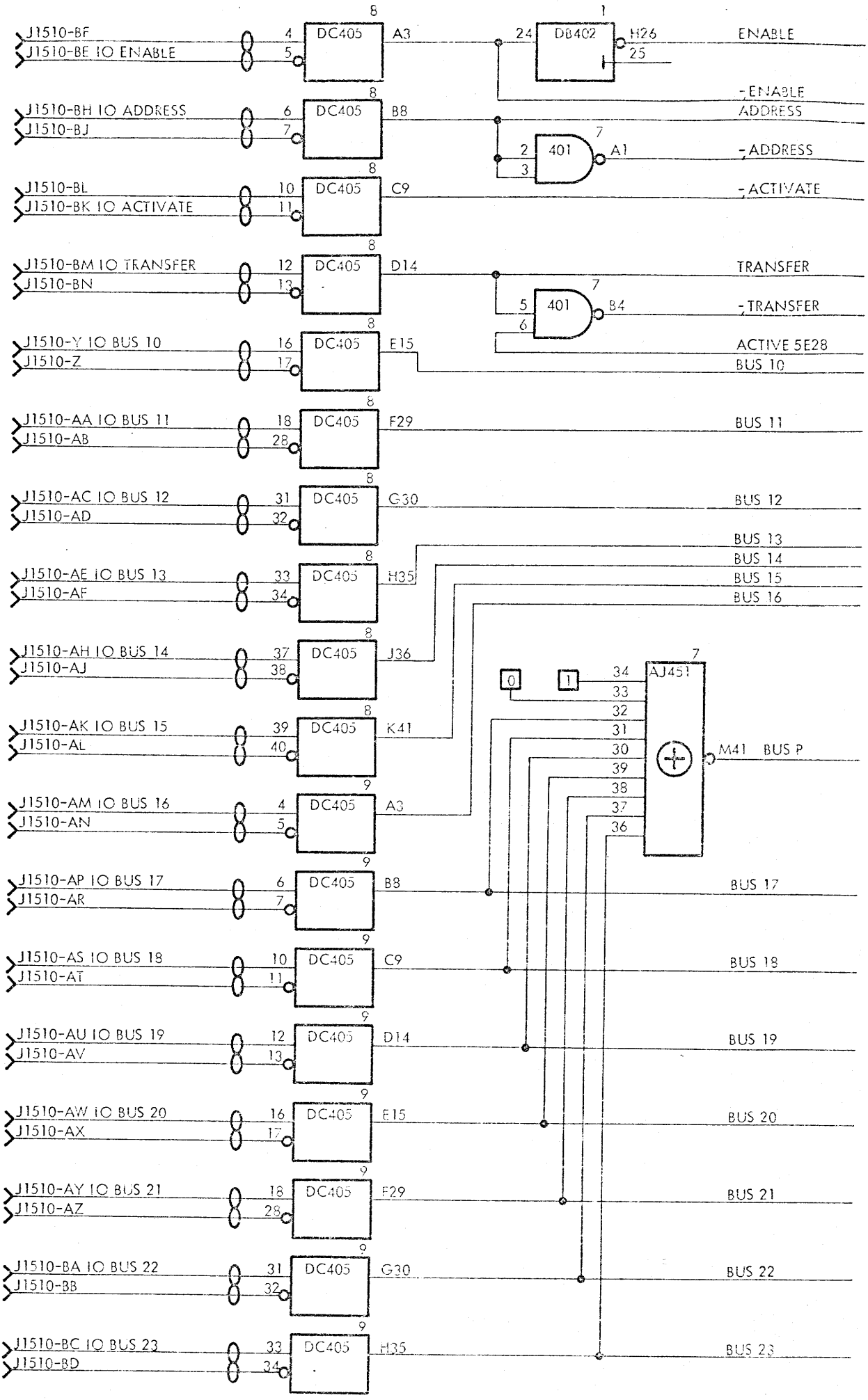
RCSL : 44-RT 610
PP : 1:35
Editor : Knud Sørensen
Edited : April 1973

LOGIC DIAGRAMS
TMX 425
LOW/MEDIUM SPEED TELEMULTIPLEXER

Keywords: RC 4000, TMX 425 telemultiplexer, logic diagrams

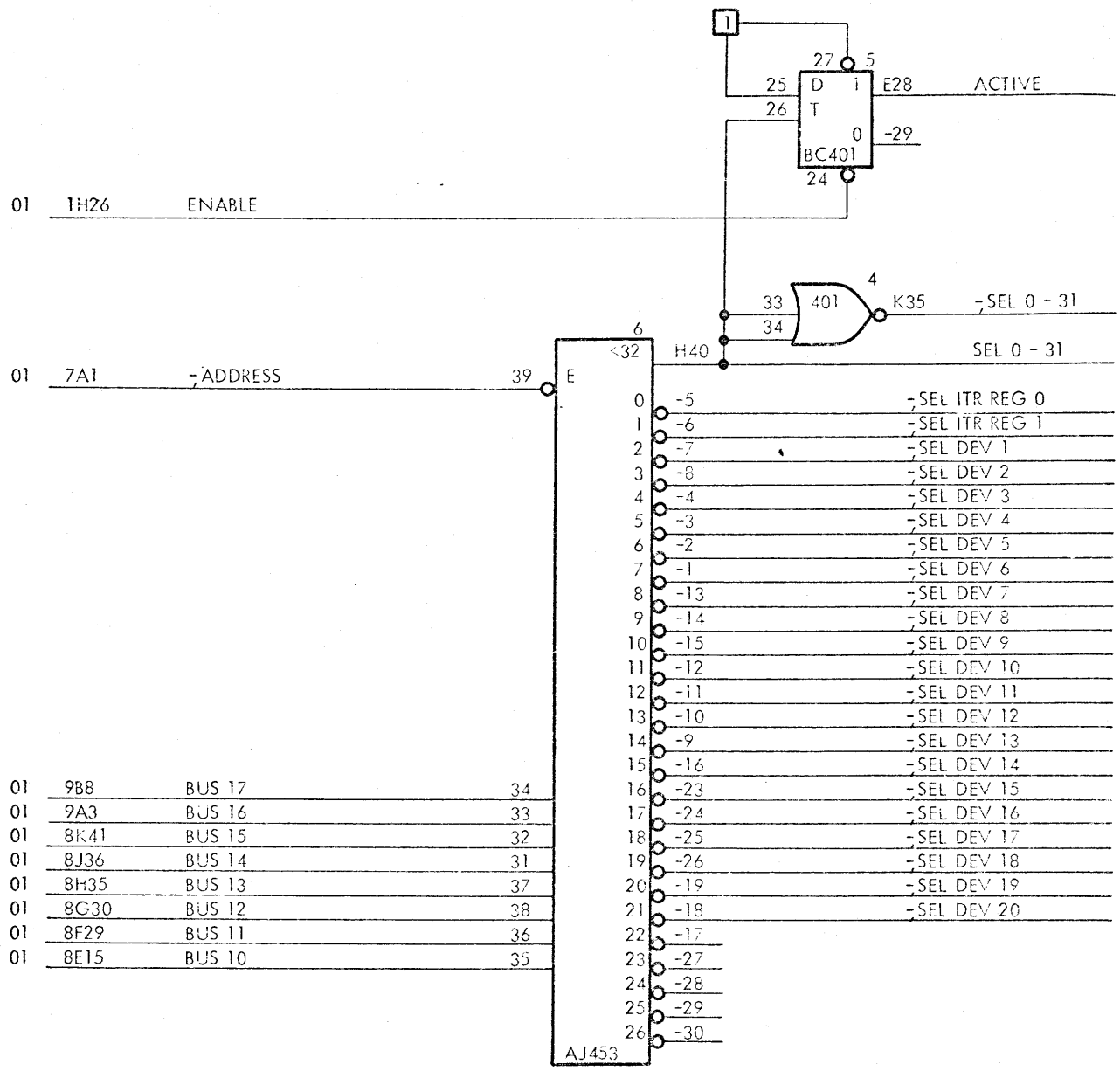
Abstract : This paper contains a complete set of Logic diagrams for the RC 4000 telemultiplexer, TMX 425.

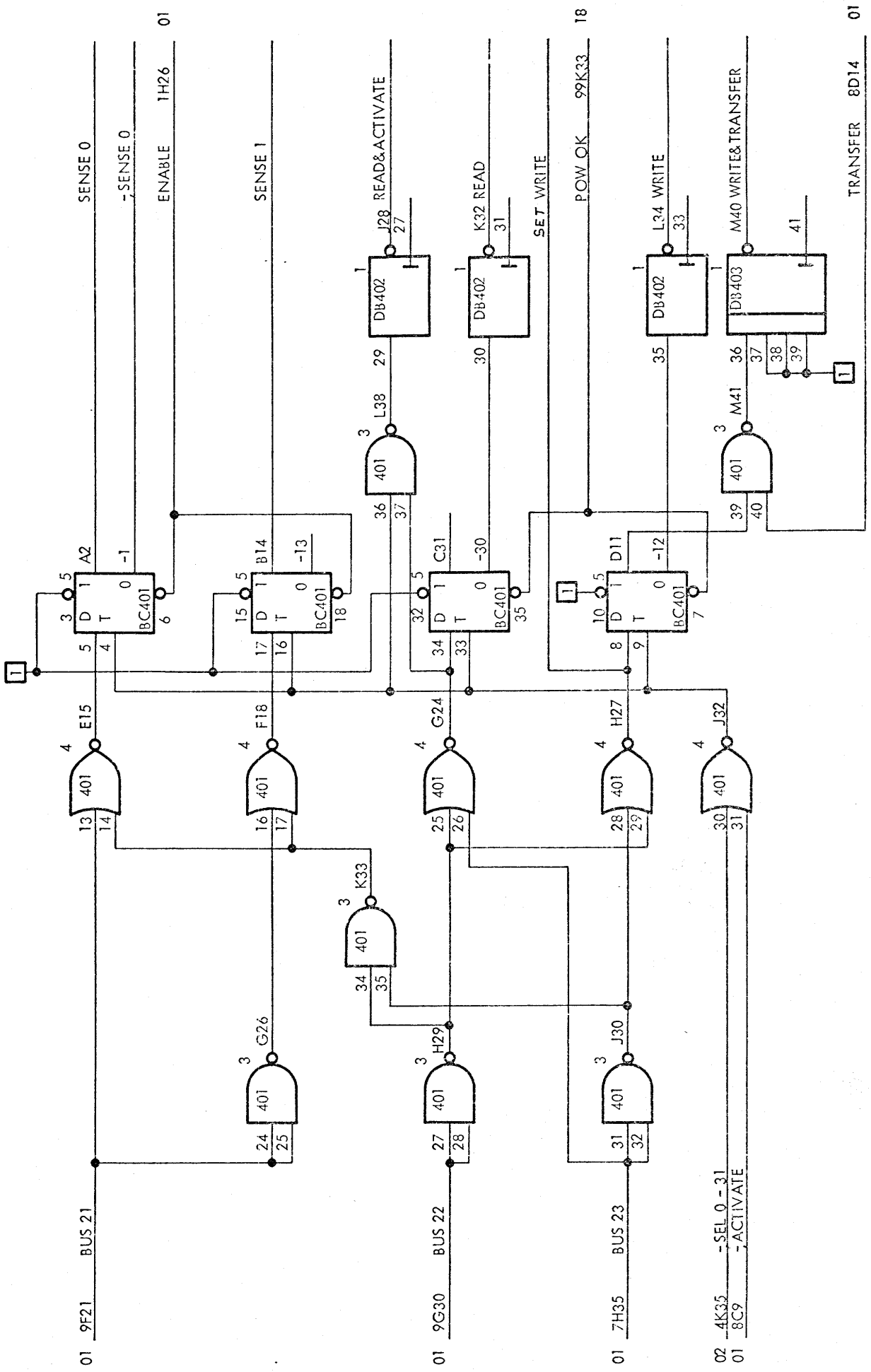
CONTENTS DWG.NO.

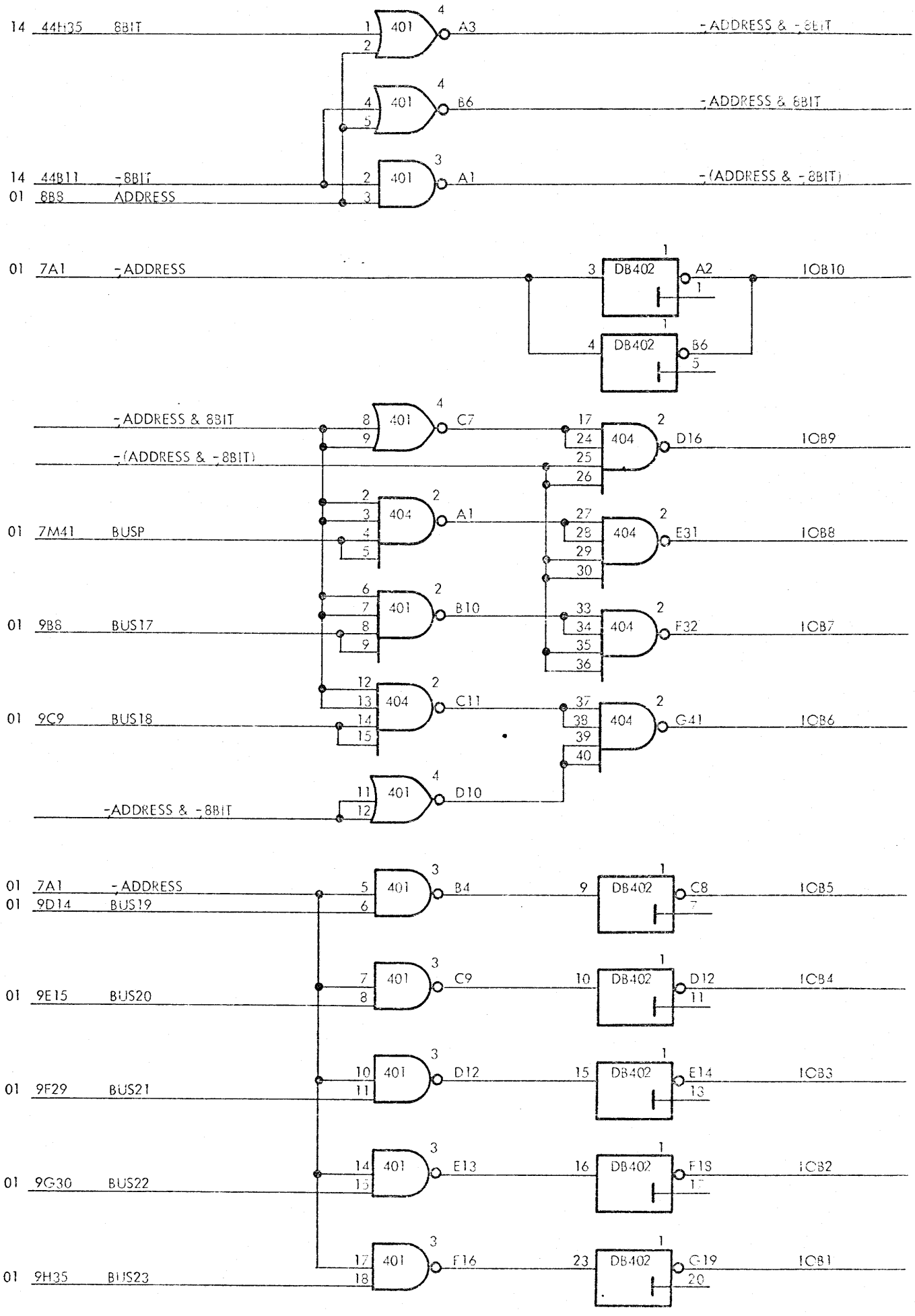


TMX425 RECEIVERS FOR I/O - BUS SIGNALS TMX01

A10977 Logic Diagram


1
27
5
25
D
1
E28
ACTIVE
26
T
0
-29
BC401
24
01 1H26 ENABLE
4
33
401
K35
-SEL 0 - 31
34
6
<32
H40
SEL 0 - 31
01 7A1 -ADDRESS 39
E
0 -5 -SEL ITR REG 0
1 -6 -SEL ITR REG 1
2 -7 -SEL DEV 1
3 -8 -SEL DEV 2
4 -4 -SEL DEV 3
5 -3 -SEL DEV 4
6 -2 -SEL DEV 5
7 -1 -SEL DEV 6
8 -13 -SEL DEV 7
9 -14 -SEL DEV 8
10 -15 -SEL DEV 9
11 -12 -SEL DEV 10
12 -11 -SEL DEV 11
13 -10 -SEL DEV 12
14 -9 -SEL DEV 13
15 -16 -SEL DEV 14
16 -23 -SEL DEV 15
17 -24 -SEL DEV 16
18 -25 -SEL DEV 17
19 -26 -SEL DEV 18
20 -19 -SEL DEV 19
21 -18 -SEL DEV 20
22 -17
23 -27
24 -28
25 -29
26 -30
AJ453
01 9B8 BUS 17 34
01 9A3 BUS 16 33
01 8K41 BUS 15 32
01 8J36 BUS 14 31
01 8H35 BUS 13 37
01 8G30 BUS 12 38
01 8F29 BUS 11 36
01 8E15 BUS 10 35

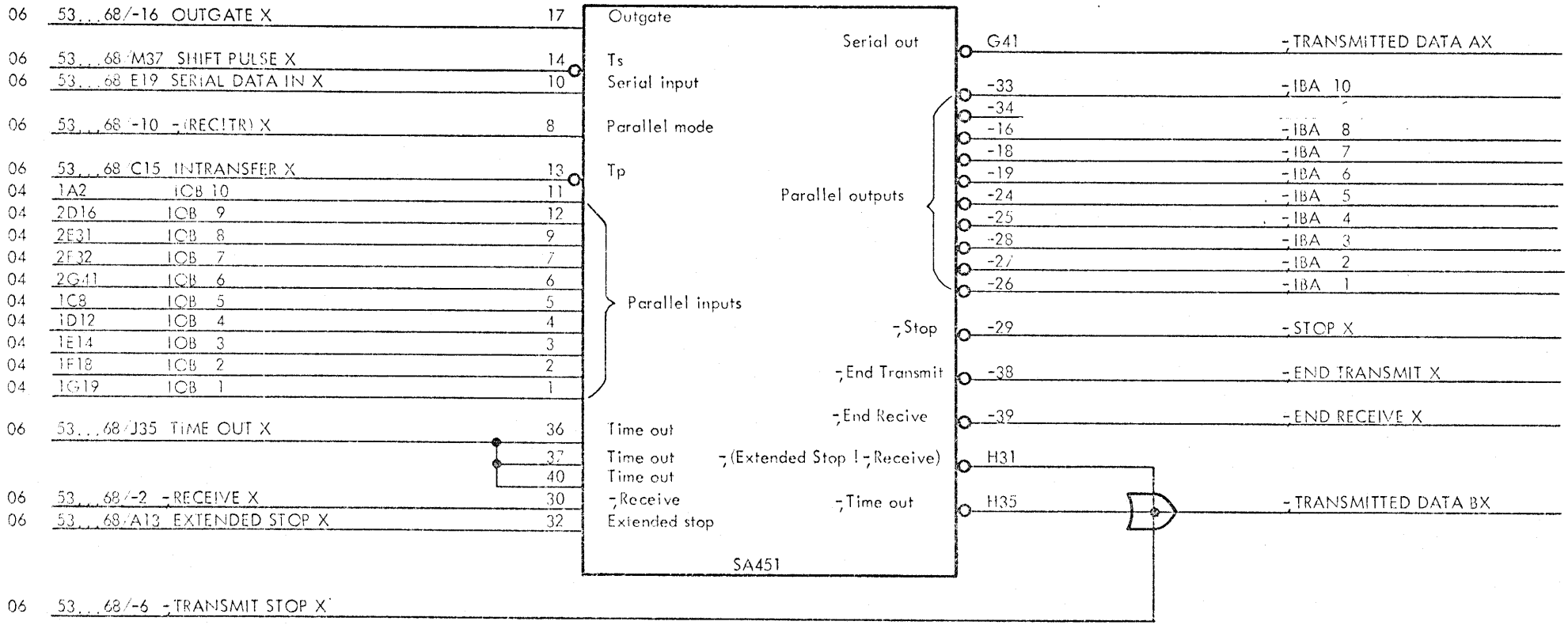

SENSE 0
-SENSE 0
ENABLE 1H26
SENSE 1
READ&ACTIVATE J28
K32 READ
SET WRITE
POW OK 99K33
L34 WRITE
M40 WRITE&TRANSFER
TRANSFER 8D14
A2
B14
C31
D11
BC401
DB402
DB403
L38
M41
E15
F18
G24
H27
J32
K33
G26
H29
J30
BUS 21
BUS 22
BUS 23
-SEL 0 - 31
-ACTIVATE
9F21
9G30
7H35
4K35
8C9



TMX425 INTERNAL OUTPUT BUS 1 - 10 TMX04

A10980 Logic Diagram

27-28-29-30-31-32-33-34
35-36-37-38-39-40-41-42

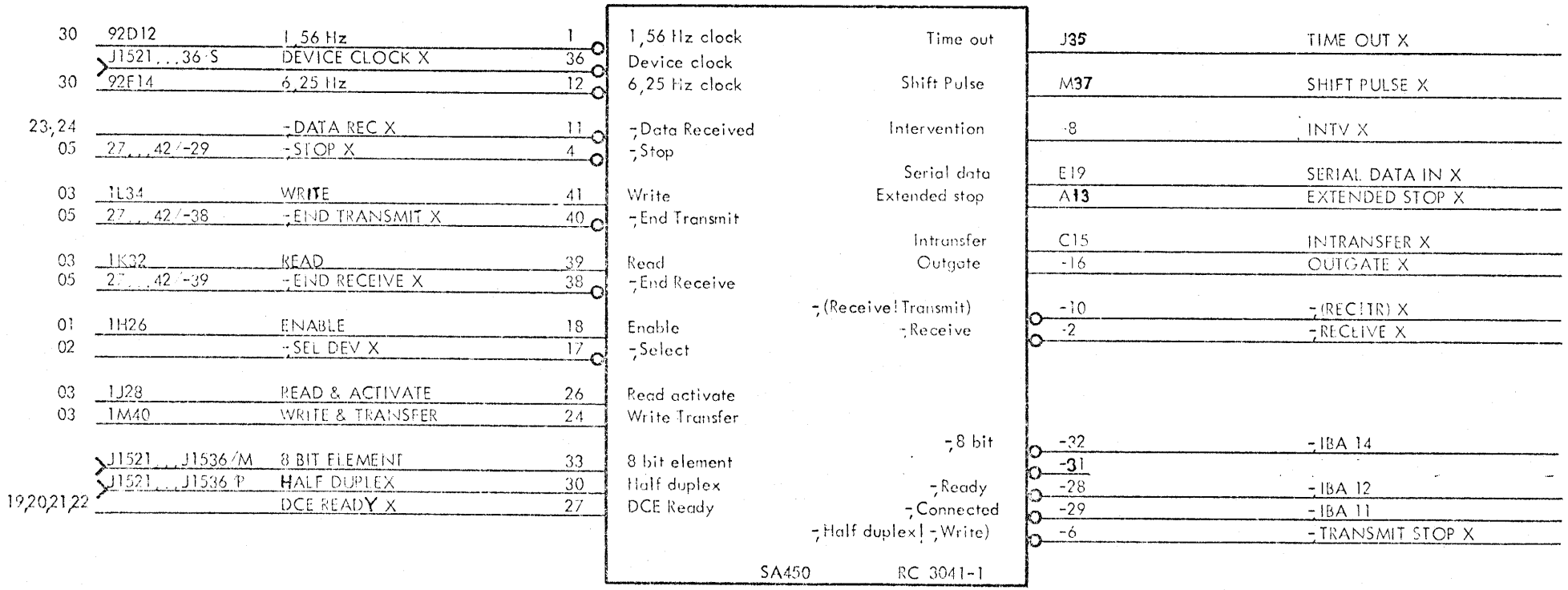


This logic diagram is valid for any of the 16 set of LSTC registers, if the letter X is replaced by the terminal No. (1 to 16).

TELETYPE CONTROL CIRCUITS

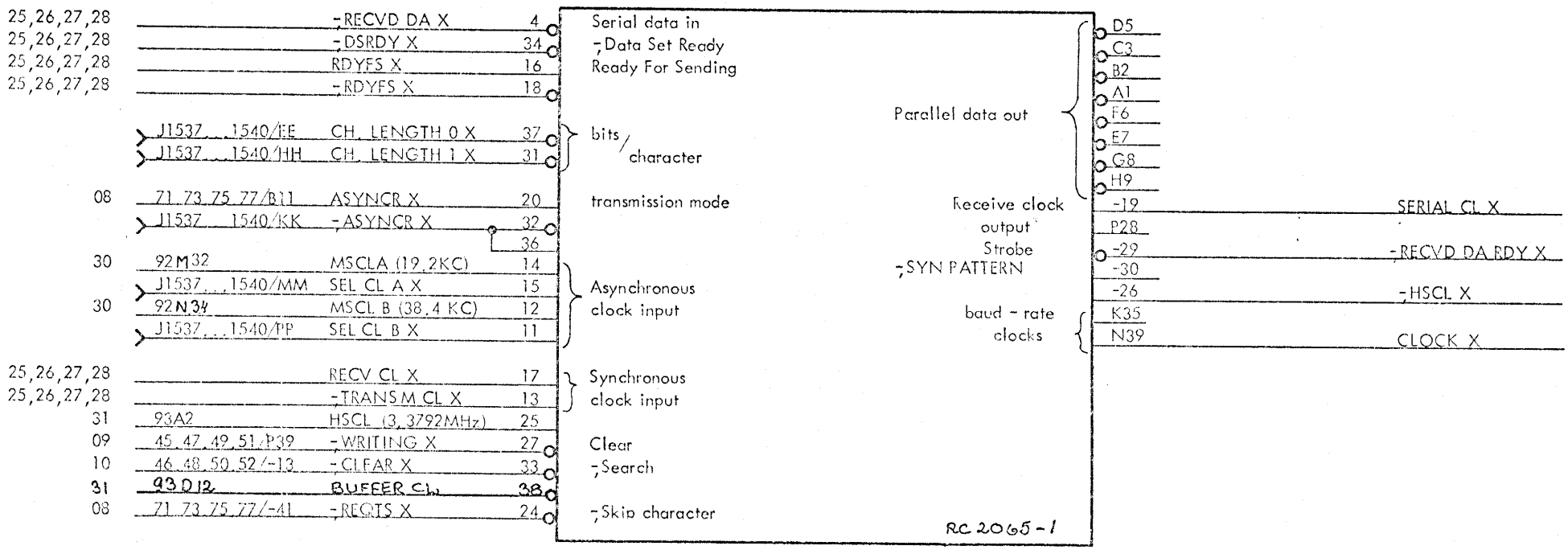
Logic Diagram

53-54-55-56-57-58-59-60
61-62-63-64-65-66-67-68

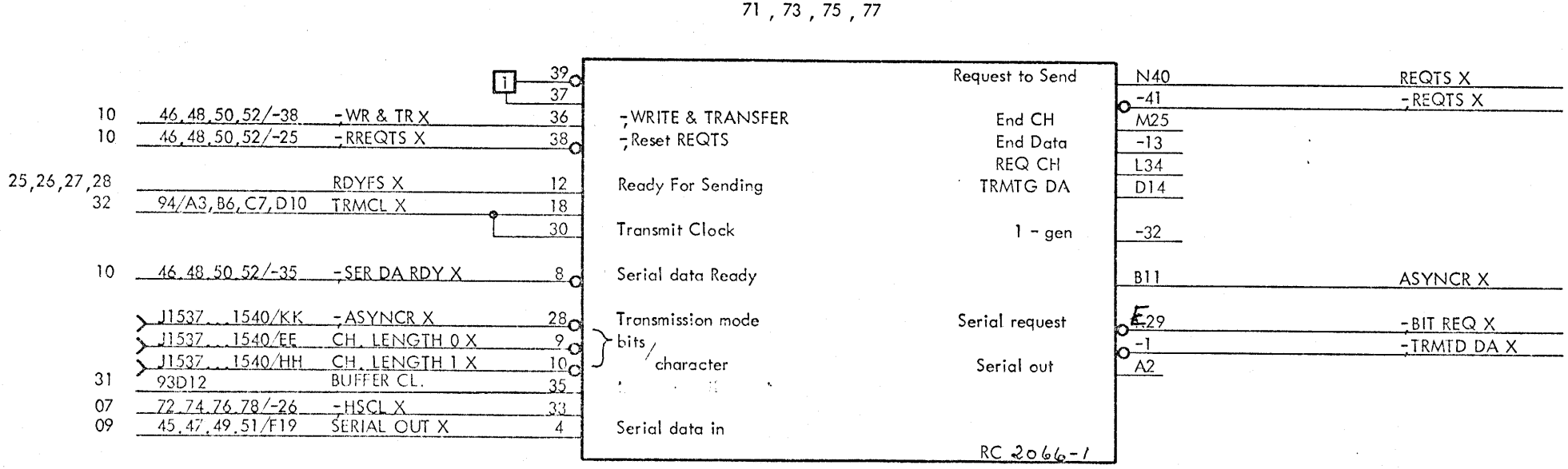


This logic diagram is valid for any of the 16 LSTC control circuits if the letter X is replaced by the terminal No. (1 - 16).

72 , 74 , 76 , 78

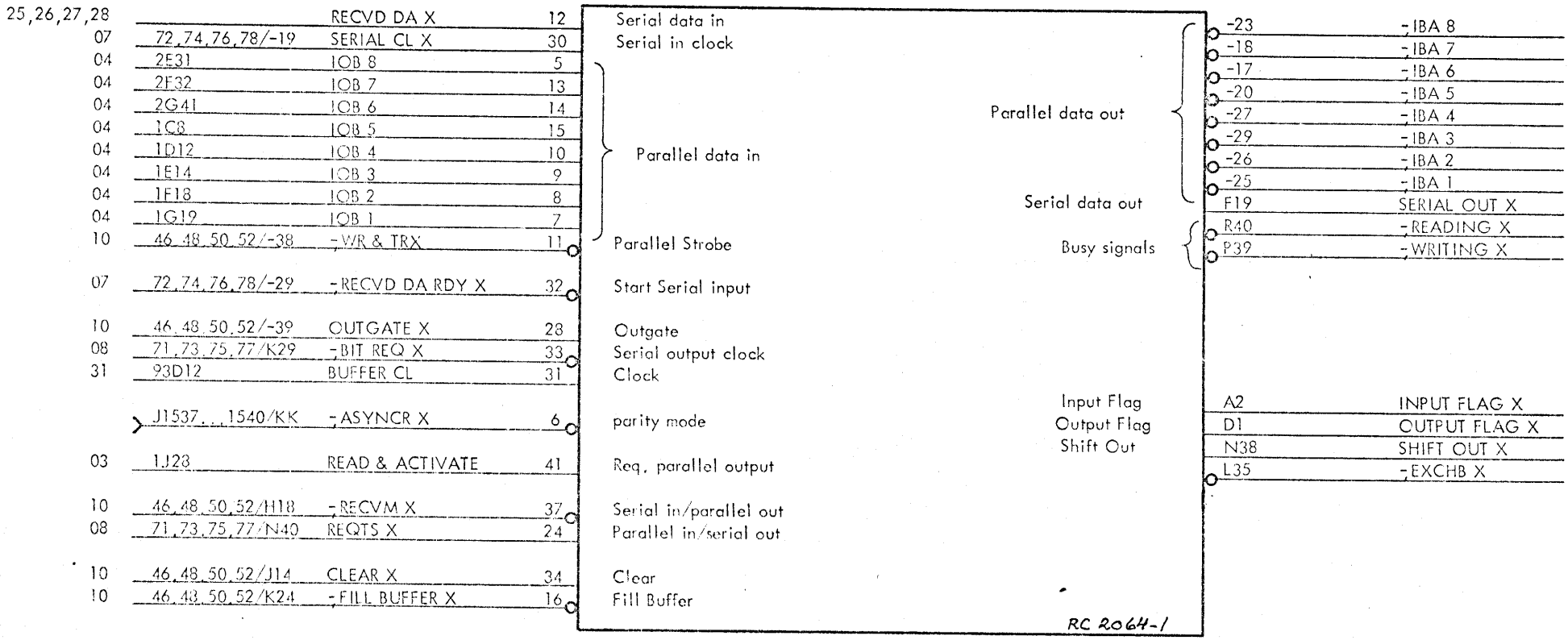


This Logic diagram is valid for any of the 4 MSTC terminal controllers if the letter X is replaced by the terminal no. (17 to 20).



This Logic diagram is valid for any of the 4 MSTC terminal controllers, if the letter X is replaced by the terminal no. (17 to 20).

45 , 47 , 49 , 51



This Logic diagram is valid for any of the 4 MSTC terminal controllers, if the letter X is replaced by the terminal no. (17 to 20).

MSTC BUFFER CARD

Logic Diagram

MSTC CONTROL CARD

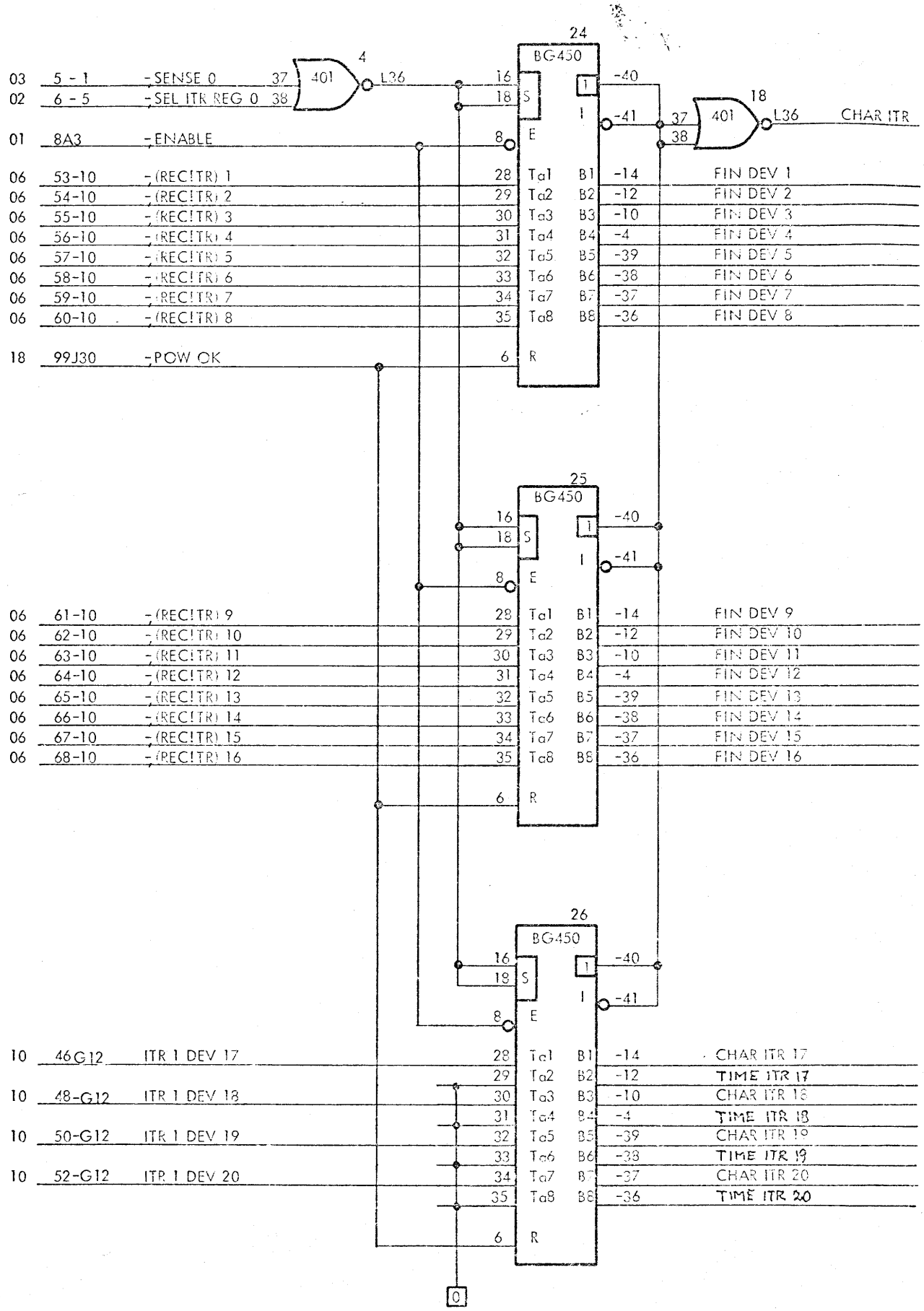
Logic Diagram

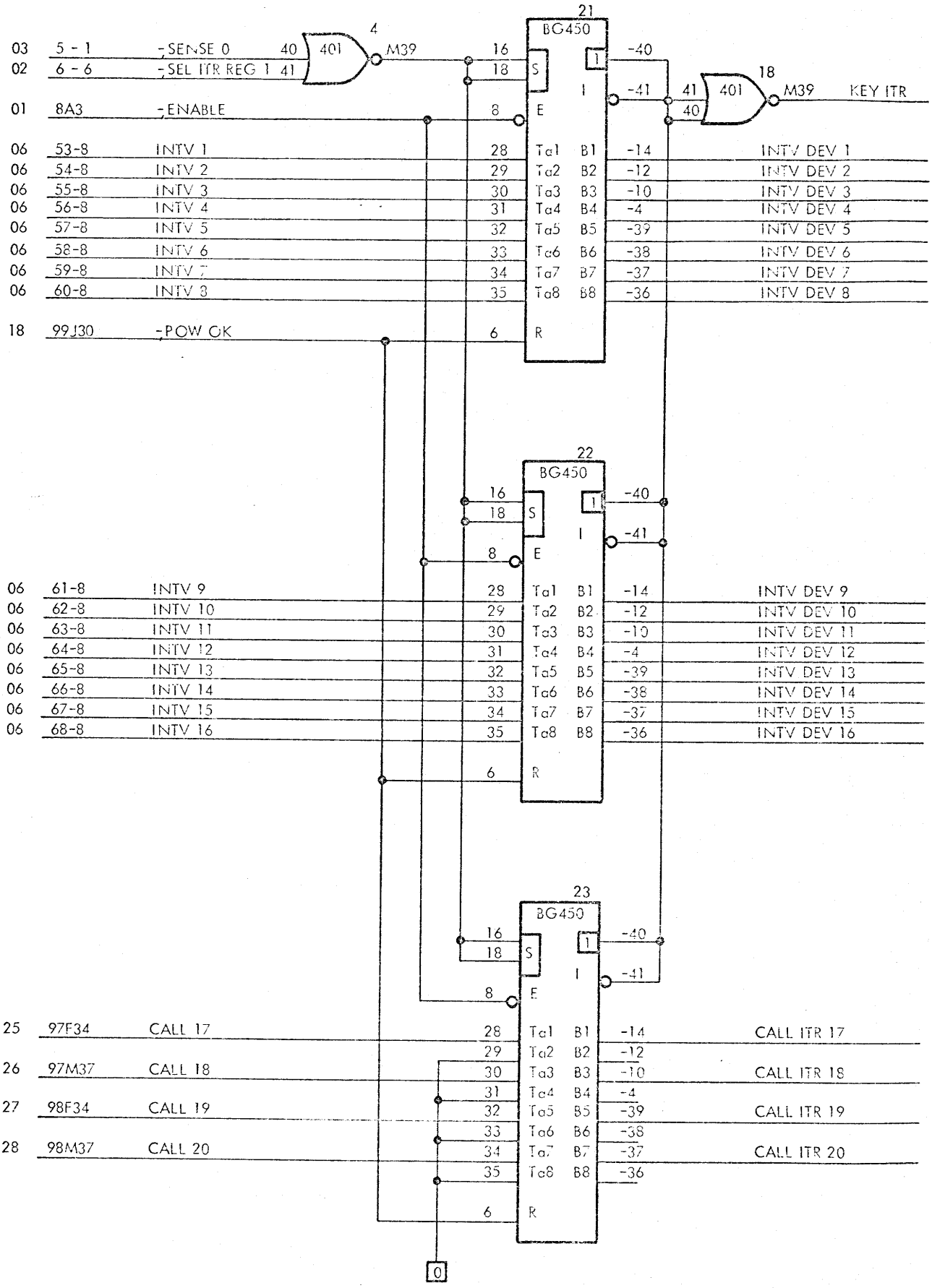
46 , 48 , 50, 52

02		⁻SEL DEV X	31	⁻Select			-5	⁻IBA 11
01	1H26	ENABLE	2	Enable		Connected	D7	⁻IBA 12
03	1M40	WRITE&TRANSFER	40	Write & transfer		Busy	B4	⁻IBA 13
03	1J28	READ & ACTIVATE	32	Read & Activate	Status	End Buffer	-10	⁻IBA 14
03	5A2	SENSE 0	15	transfer status		8 bit	A3	⁻IBA 15
03	5B14	SENSE 1	34	Set neutral mode		Overrun		
30	92F14	6.25HZ	29	Clock				
08	71,73,75,77/-41	⁻REQTS X	16	Request to Send		Data Set not Ready	-8	⁻IBA 17
25,26,27,28		RDYFS X	26	Ready For Sending		Time Out	E9	⁻IBA 10
32	94/A3, B6, C7, D10	TRMCL X	27	Transmit Clock		output strobe	-39	OUTGATE X
25,26,27,28		DSRDY X	37	Data Set Ready			-38	⁻WR&TR X
08	71,73,75,77/N40	REQTS X	1			Receive mode	H18	⁻RECVM X
07	72,74,76,78/-29	⁻RECVD DA RDY X	36	Received Data Ready		Neutral mode	M33	⁻NEUTRM X
09	45,47,49,51/R40	⁻READING X	41	Busy from Buffer		Reset Req. to Send	-25	⁻RREQTS X
09	45,47,49,51/P39	⁻WRITING X	17			Clear	J11	CLEAR X
30	92 - 10	50 HZ	30	Clock			-13	⁻CLEAR X
09	45,47,49,51/N38	SHIFT OUT X	28	Buffer perhaps empty		Fill Buffer	K24	⁻FILL BUFFER X
09	45,47,49,51/A2	INPUT FLAG X	23	Full input buffer		Char interrupt	G12	INTR 1 X
09	45,47,49,51/D1	OUTPUT FLAG X	20	Full output buffer		Serial data ready	-35	⁻SER DA RDY
09	45,47,49,51/L35	⁻EXCHB X	19	Exchange buffer				
18	99K33	POW OK	14	Power OK				
34		-, INHIBIT SHIFT OUT	6	-, Search				

RC 2067-1

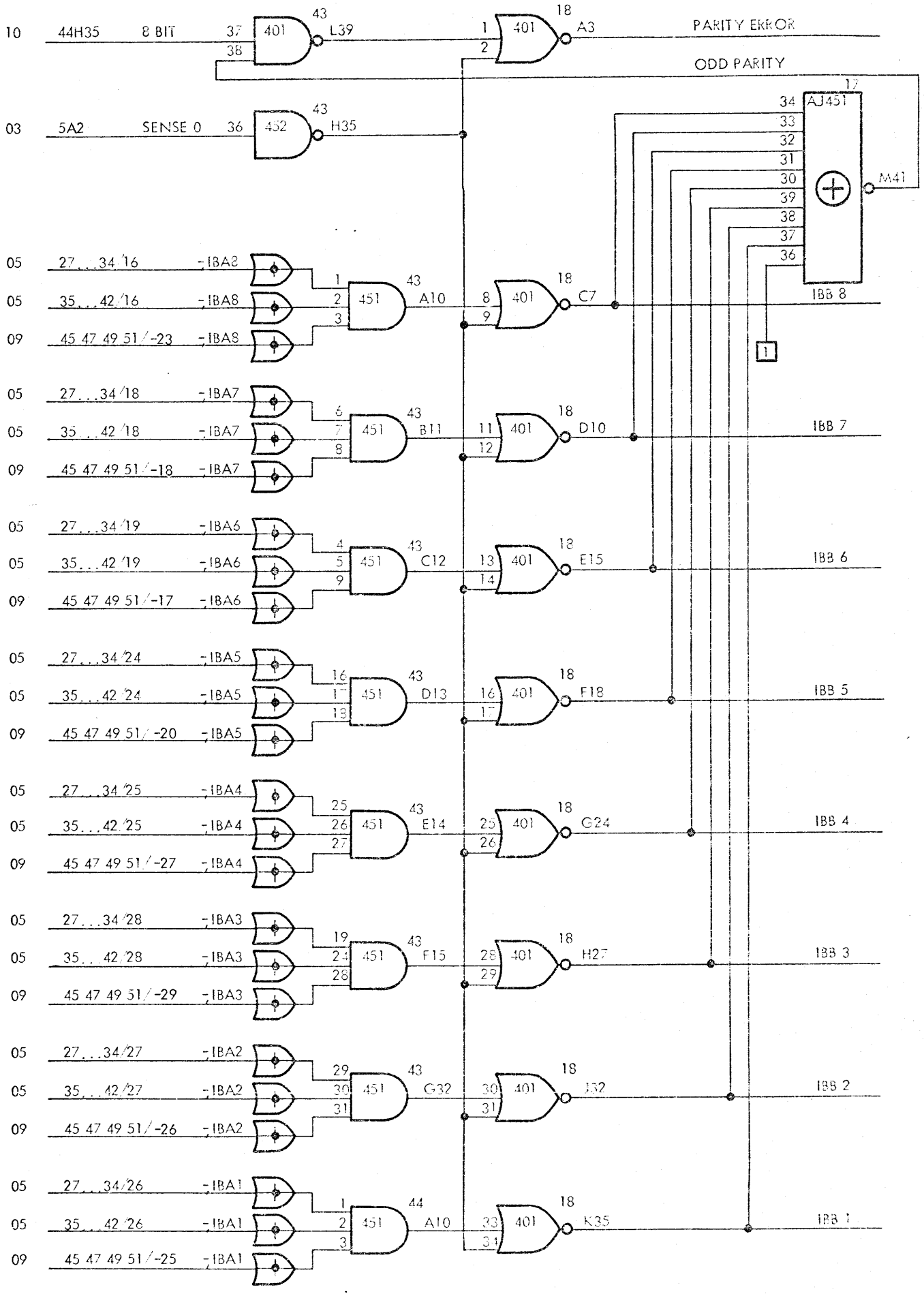
This Logic diagram is valid for any of the 4 MSTC terminal controllers if the letter X is replaced by the terminal no. (17 to 20).

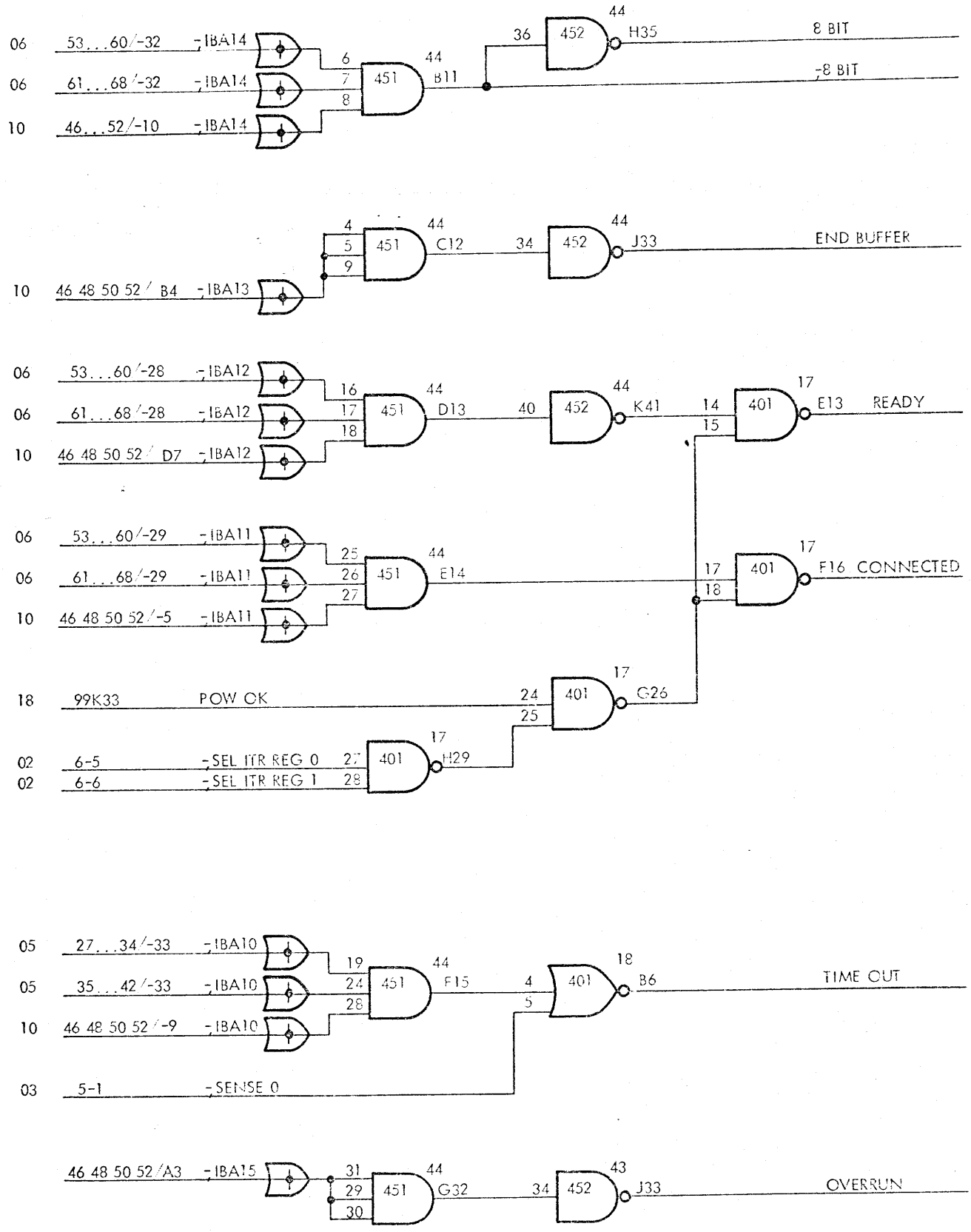

24
BG450
25
BG450
26
BG450
4
401
L36
18
401
L36
CHAR ITR
03 5-1 -SENSE 0 37
02 6-5 -SEL ITR REG 0 38
01 8A3 -ENABLE
18 99J30 -POW OK
06 53-10 -(REC!TR) 1
06 54-10 -(REC!TR) 2
06 55-10 -(REC!TR) 3
06 56-10 -(REC!TR) 4
06 57-10 -(REC!TR) 5
06 58-10 -(REC!TR) 6
06 59-10 -(REC!TR) 7
06 60-10 -(REC!TR) 8
FIN DEV 1
FIN DEV 2
FIN DEV 3
FIN DEV 4
FIN DEV 5
FIN DEV 6
FIN DEV 7
FIN DEV 8
06 61-10 -(REC!TR) 9
06 62-10 -(REC!TR) 10
06 63-10 -(REC!TR) 11
06 64-10 -(REC!TR) 12
06 65-10 -(REC!TR) 13
06 66-10 -(REC!TR) 14
06 67-10 -(REC!TR) 15
06 68-10 -(REC!TR) 16
FIN DEV 9
FIN DEV 10
FIN DEV 11
FIN DEV 12
FIN DEV 13
FIN DEV 14
FIN DEV 15
FIN DEV 16
10 46G12 ITR 1 DEV 17
10 48-G12 ITR 1 DEV 18
10 50-G12 ITR 1 DEV 19
10 52-G12 ITR 1 DEV 20
CHAR ITR 17
TIME ITR 17
CHAR ITR 18
TIME ITR 18
CHAR ITR 19
TIME ITR 19
CHAR ITR 20
TIME ITR 20
16
18
S
8
E
6
R
1
I
-40
-41
28
29
30
31
32
33
34
35
Ta1 B1 -14
Ta2 B2 -12
Ta3 B3 -10
Ta4 B4 -4
Ta5 B5 -39
Ta6 B6 -38
Ta7 B7 -37
Ta8 B8 -36
0

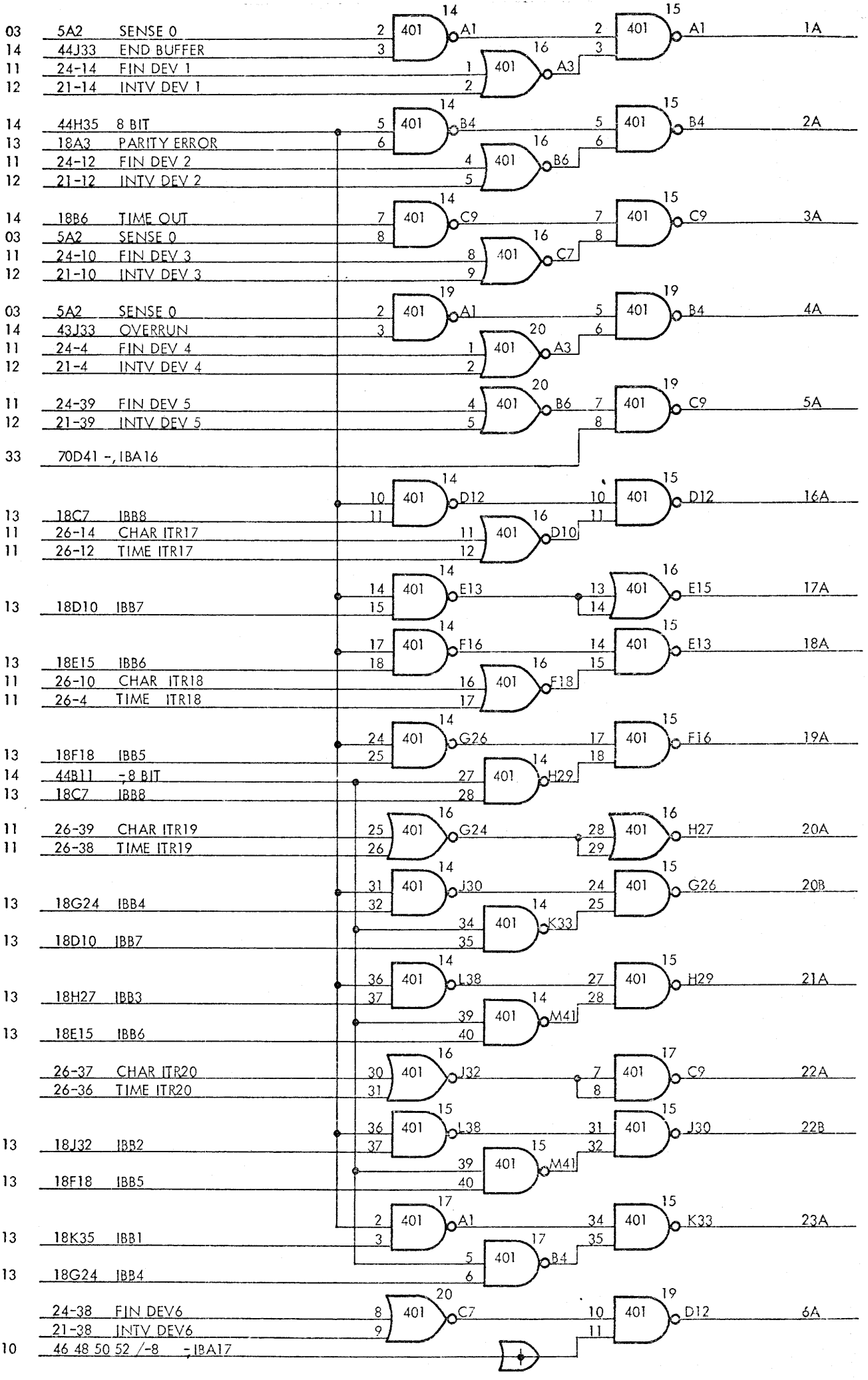


TMX425 INTERRUPT EXPANDER FOR INTERVENTION ITR TMX12

A10988 Logic Diagram


10 44H35 8 BIT 37 38 401 43 L39
1 2 401 18 A3 PARITY ERROR
ODD PARITY
03 5A2 SENSE 0 36 452 43 H35
17 AJ451 34 33 32 31 30 39 38 37 36 M41
1
05 27...34/16 -IBA8
05 35...42/16 -IBA8
09 45 47 49 51/-23 -IBA8
1 2 3 451 43 A10
8 9 401 18 C7 IBB 8
05 27...34/18 -IBA7
05 35...42/18 -IBA7
09 45 47 49 51/-18 -IBA7
6 7 8 451 43 B11
11 12 401 18 D10 IBB 7
05 27...34/19 -IBA6
05 35...42/19 -IBA6
09 45 47 49 51/-17 -IBA6
4 5 9 451 43 C12
13 14 401 18 E15 IBB 6
05 27...34/24 -IBA5
05 35...42/24 -IBA5
09 45 47 49 51/-20 -IBA5
16 17 13 451 43 D13
16 17 401 18 F18 IBB 5
05 27...34/25 -IBA4
05 35...42/25 -IBA4
09 45 47 49 51/-27 -IBA4
25 26 27 451 43 E14
25 26 401 18 G24 IBB 4
05 27...34/28 -IBA3
05 35...42/28 -IBA3
09 45 47 49 51/-29 -IBA3
19 24 28 451 43 F15
28 29 401 18 H27 IBB 3
05 27...34/27 -IBA2
05 35...42/27 -IBA2
09 45 47 49 51/-26 -IBA2
29 30 31 451 43 G32
30 31 401 18 J32 IBB 2
05 27...34/26 -IBA1
05 35...42/26 -IBA1
09 45 47 49 51/-25 -IBA1
1 2 3 451 44 A10
33 34 401 18 K35 IBB 1


06 53...60/-32 -IBA14
06 61...68/-32 -IBA14
10 46...52/-10 -IBA14
6
7
8
451
44
B11
36
452
44
H35
8 BIT
-8 BIT
10 46 48 50 52/B4 -IBA13
4
5
9
451
44
C12
34
452
44
J33
END BUFFER
06 53...60/-28 -IBA12
06 61...68/-28 -IBA12
10 46 48 50 52/D7 -IBA12
16
17
18
451
44
D13
40
452
44
K41
14
15
401
17
E13
READY
06 53...60/-29 -IBA11
06 61...68/-29 -IBA11
10 46 48 50 52/-5 -IBA11
25
26
27
451
44
E14
17
18
401
17
F16 CONNECTED
18 99K33 POW OK
24
25
401
17
G26
02 6-5 -SEL ITR REG 0
02 6-6 -SEL ITR REG 1
27
28
401
17
H29
05 27...34/-33 -IBA10
05 35...42/-33 -IBA10
10 46 48 50 52/-9 -IBA10
19
24
28
451
44
F15
4
5
401
18
B6
TIME OUT
03 5-1 -SENSE 0
46 48 50 52/A3 -IBA15
31
29
30
451
44
G32
34
452
43
J33
OVERRUN



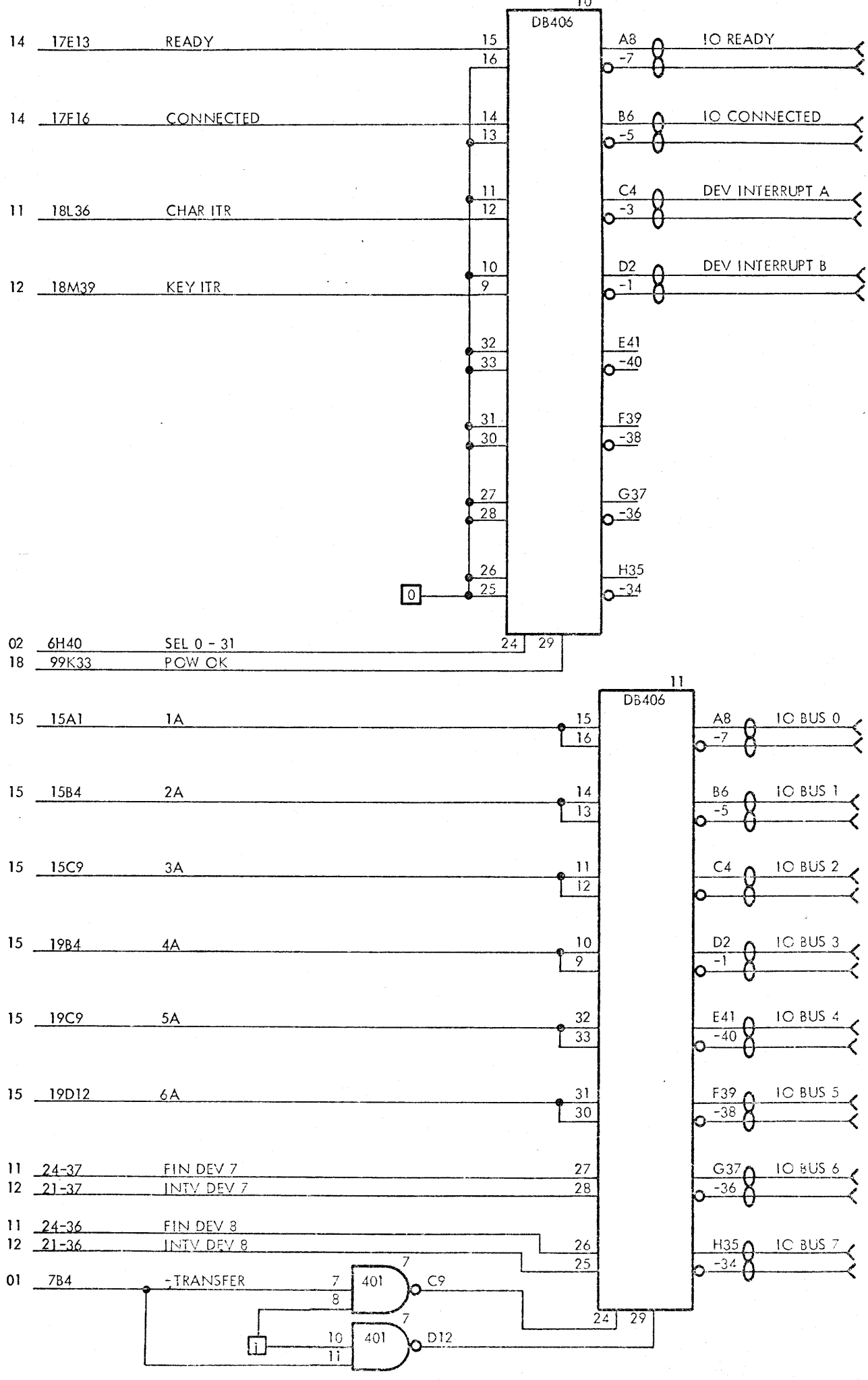
TMX425

R 10387

MULTIPLIER

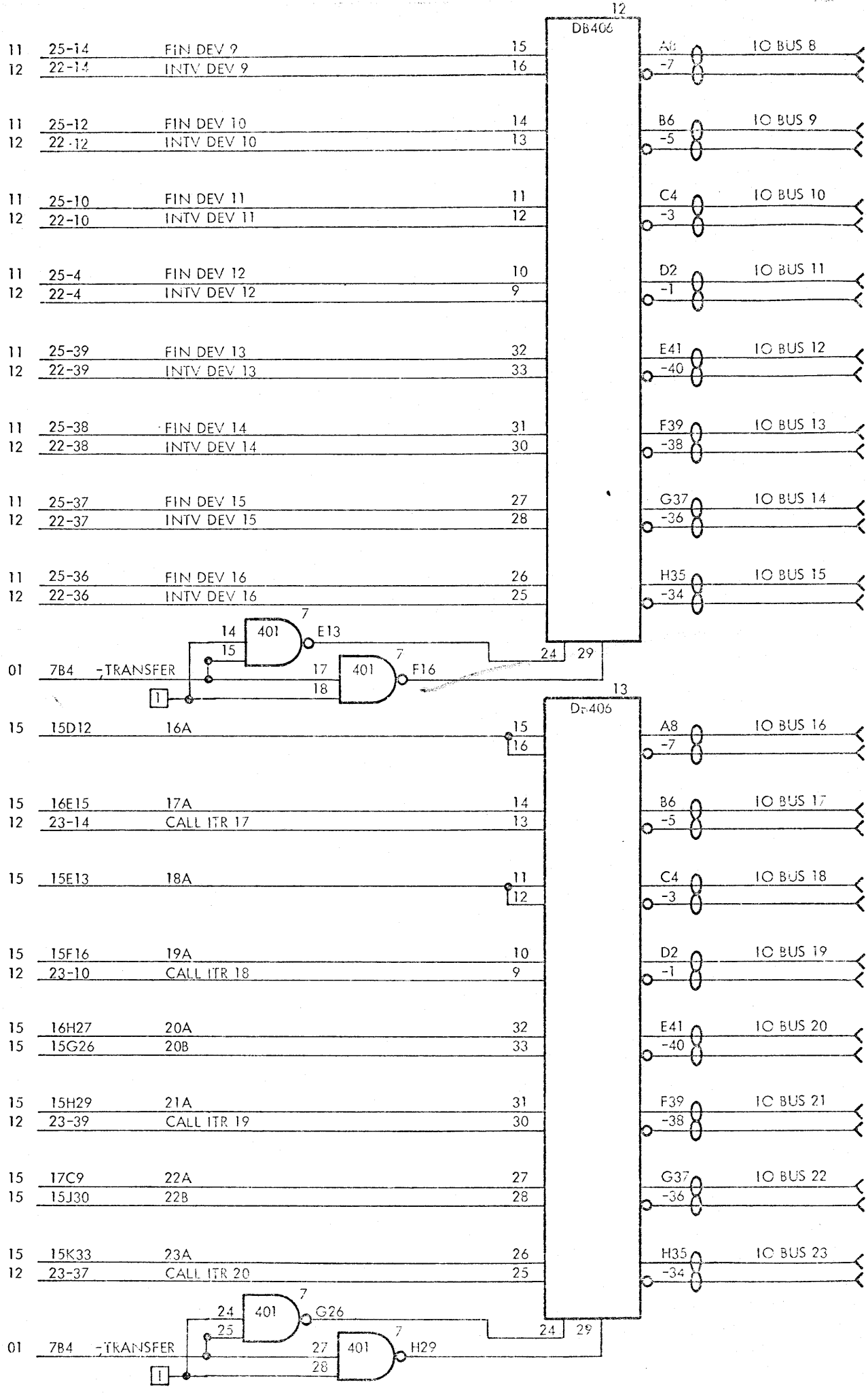
Logic Diagram

TMX15



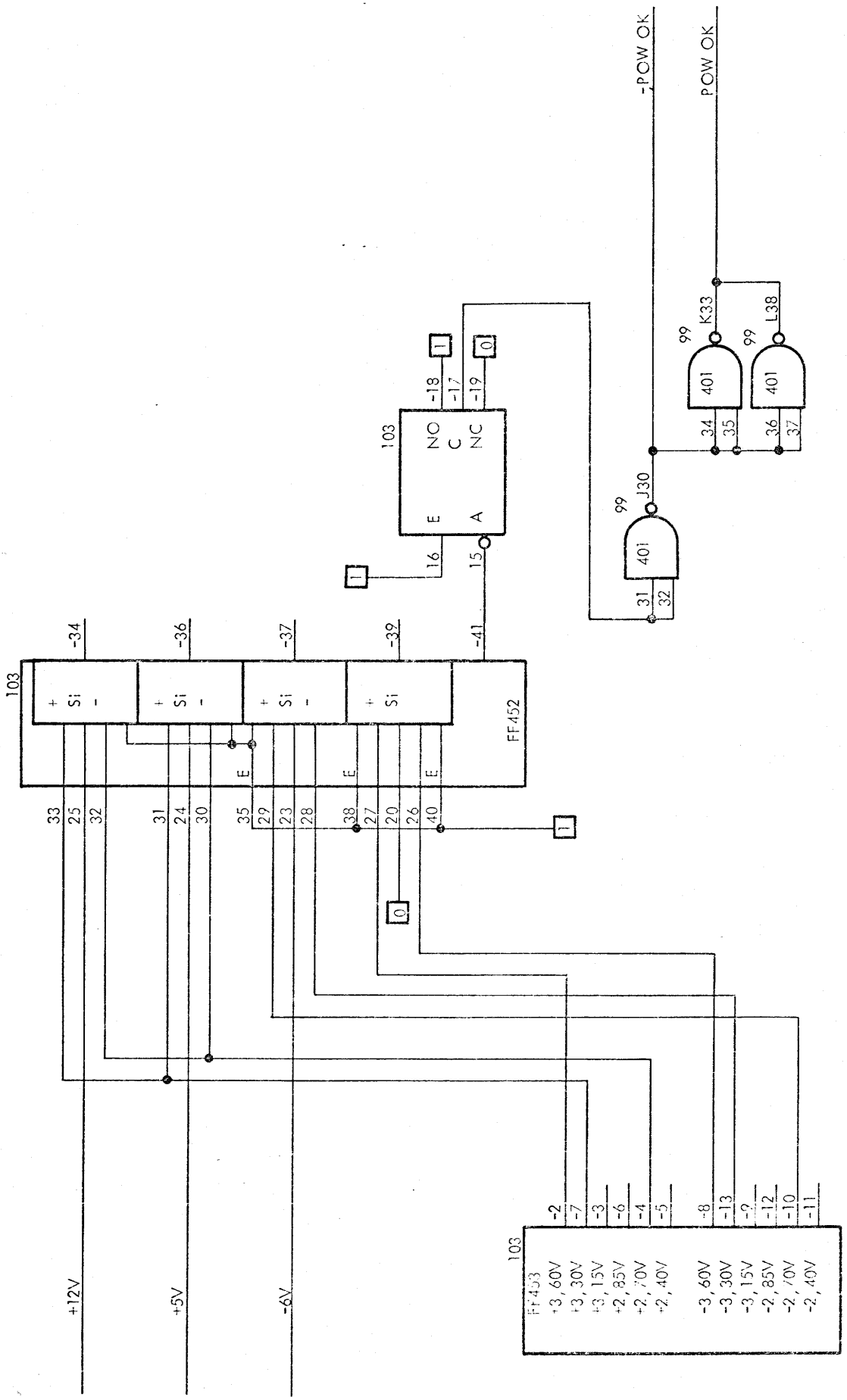
TMX425 DRIVERS FOR IO BUS SIGNALS TMX16

R 10386 Logic Diagram



TMX425 DRIVERS OF IO BUS SIGNALS TMX17

A10993 Logic Diagram

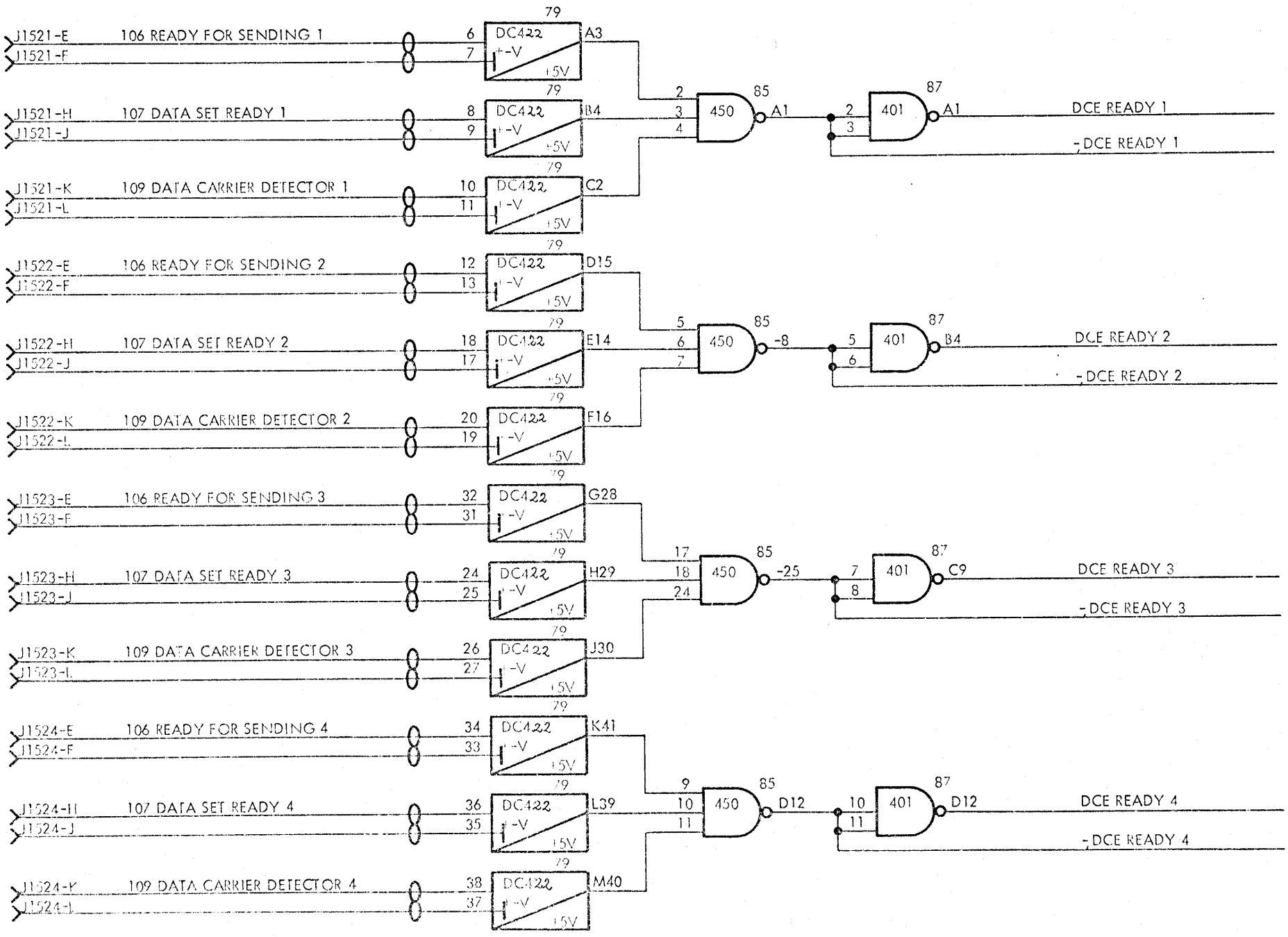


TMX425 POWER CHECKING CIRCUITS TMX18

A10994 Logic Diagram

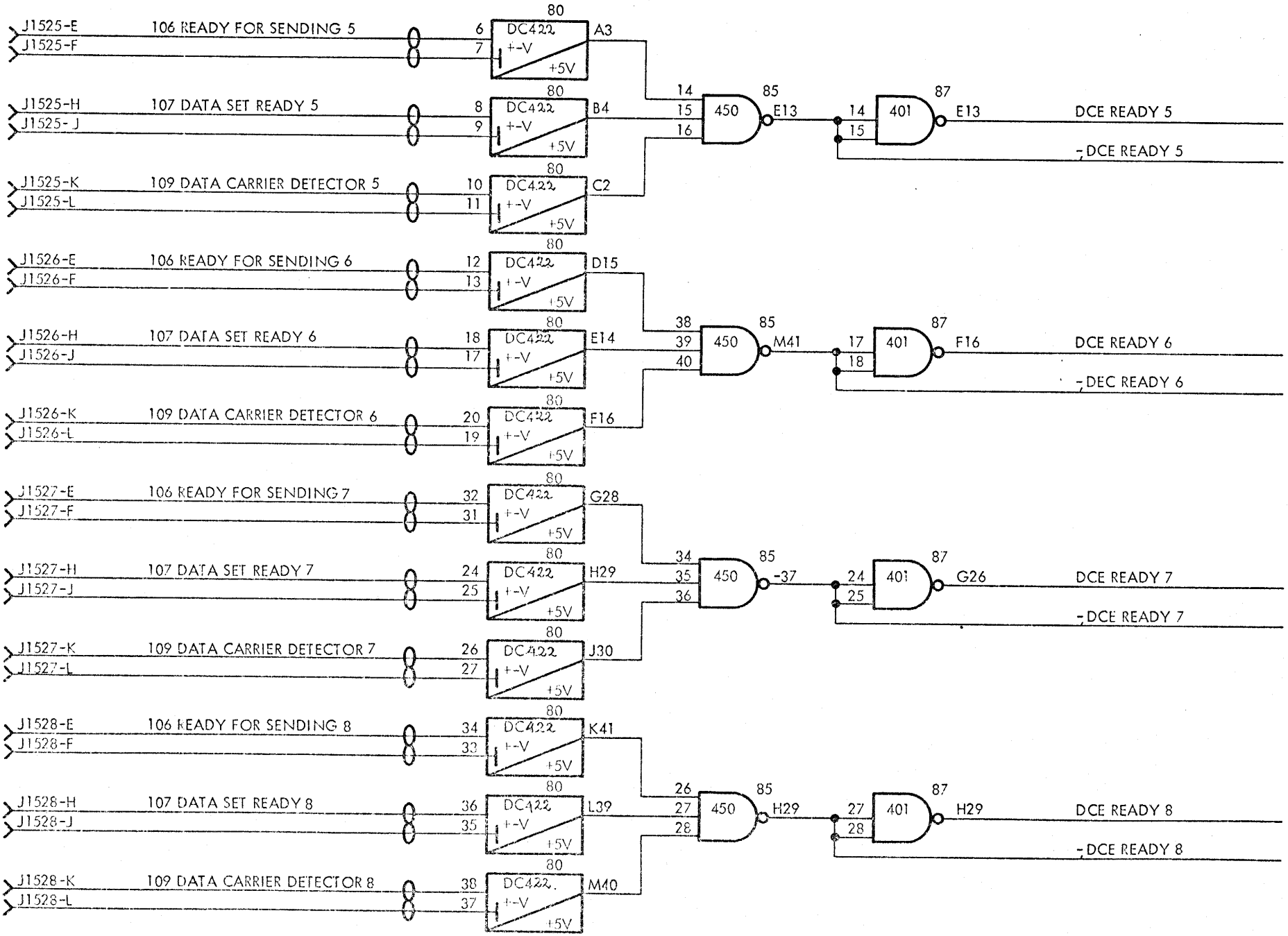
LINE RECEIVERS FOR CONTROL SIGNALS

Logic Diagram



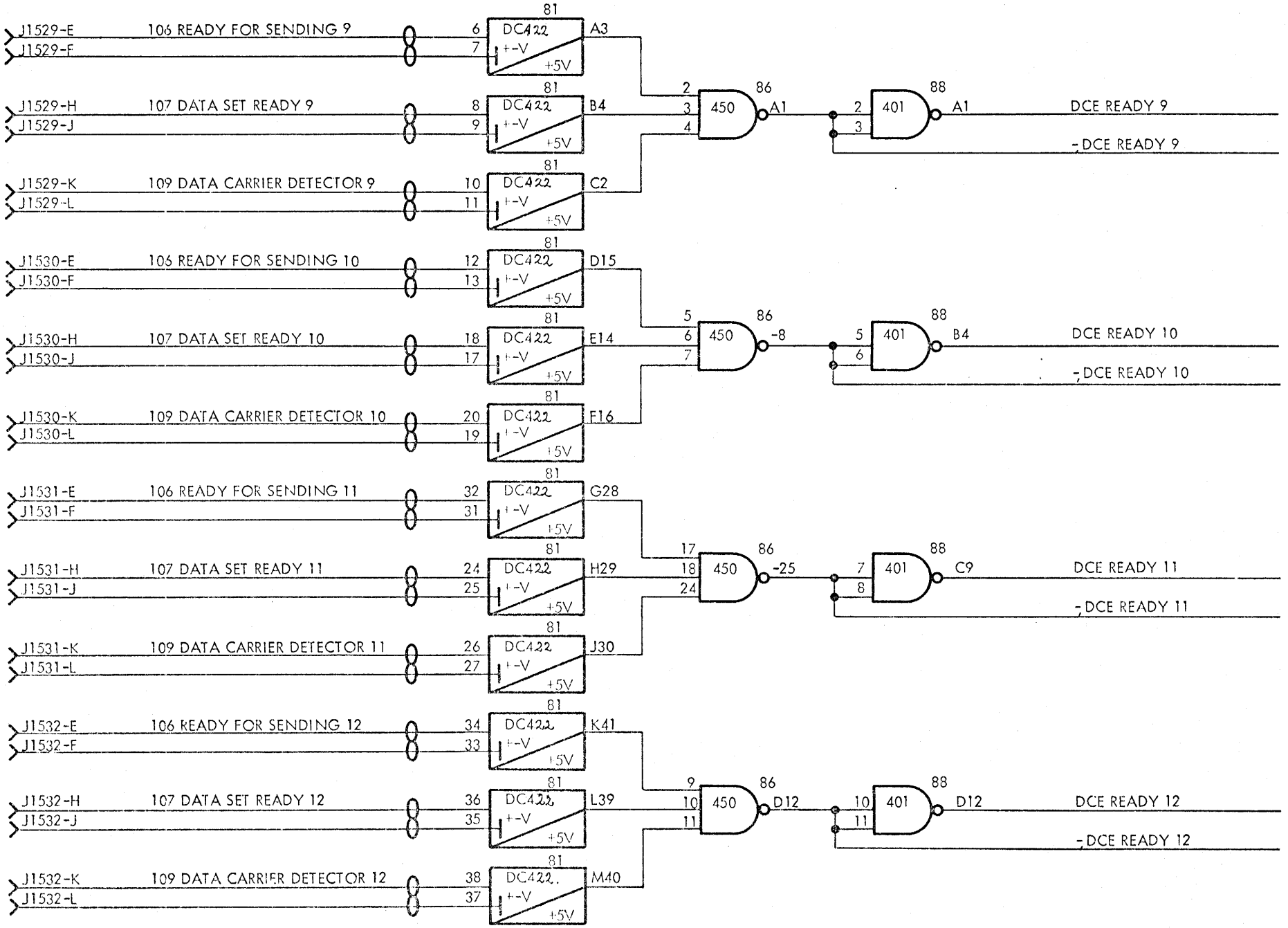
LINE RECEIVERS FOR CONTROL SIGNALS

Logic Diagram



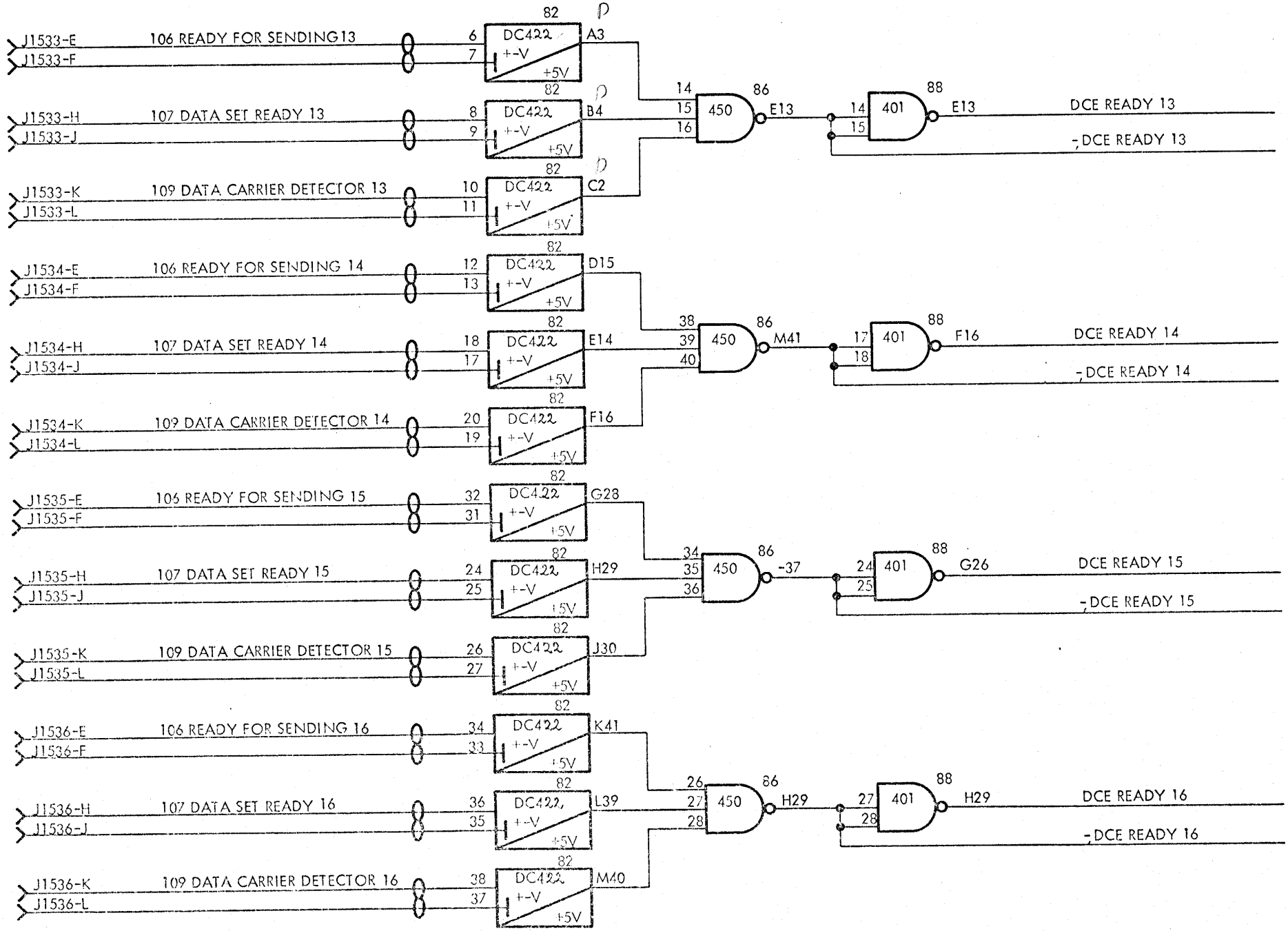
LINE RECEIVERS FOR CONTROL SIGNALS

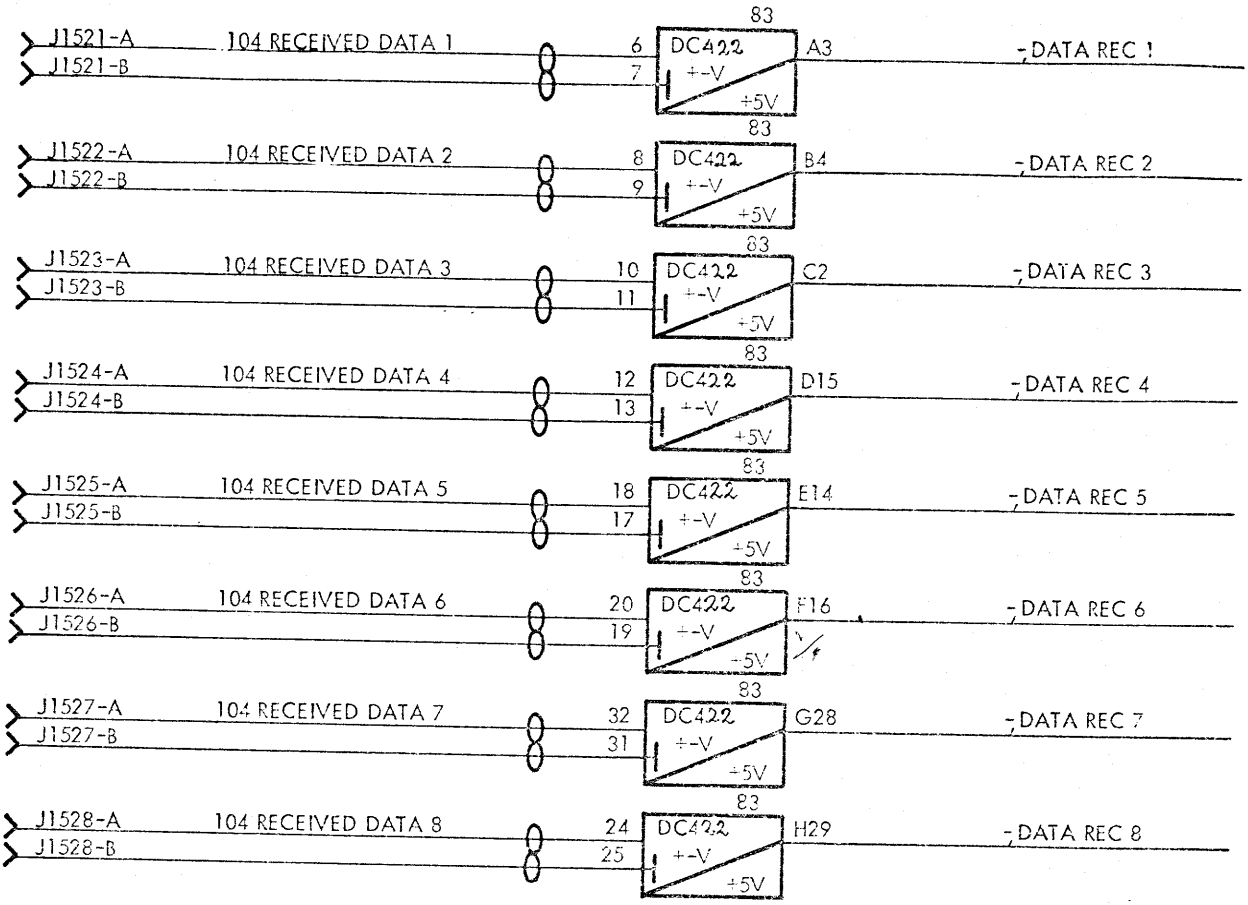
Logic Diagram

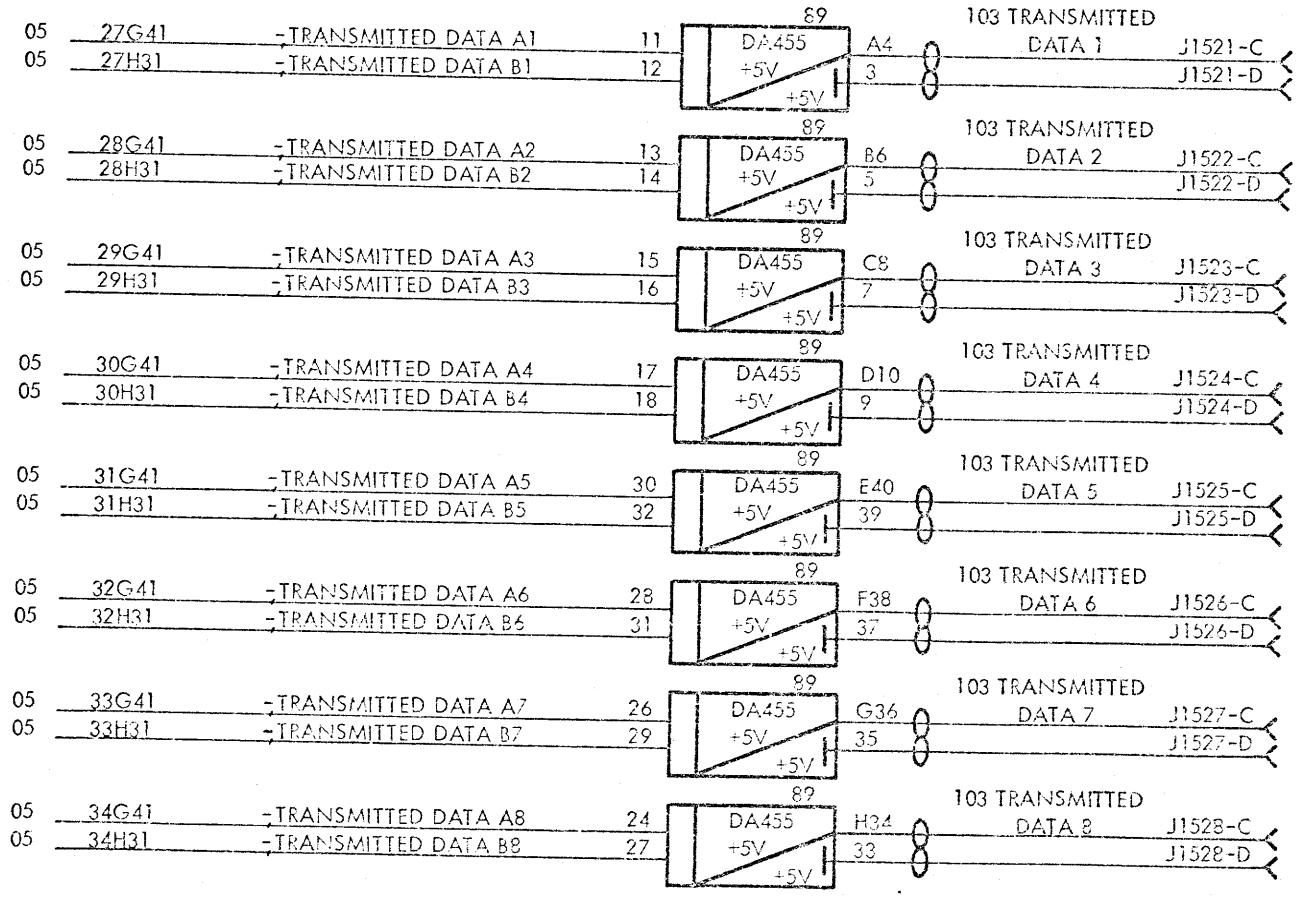


LINE RECEIVERS FOR CONTROL SIGNALS

Logic Diagram







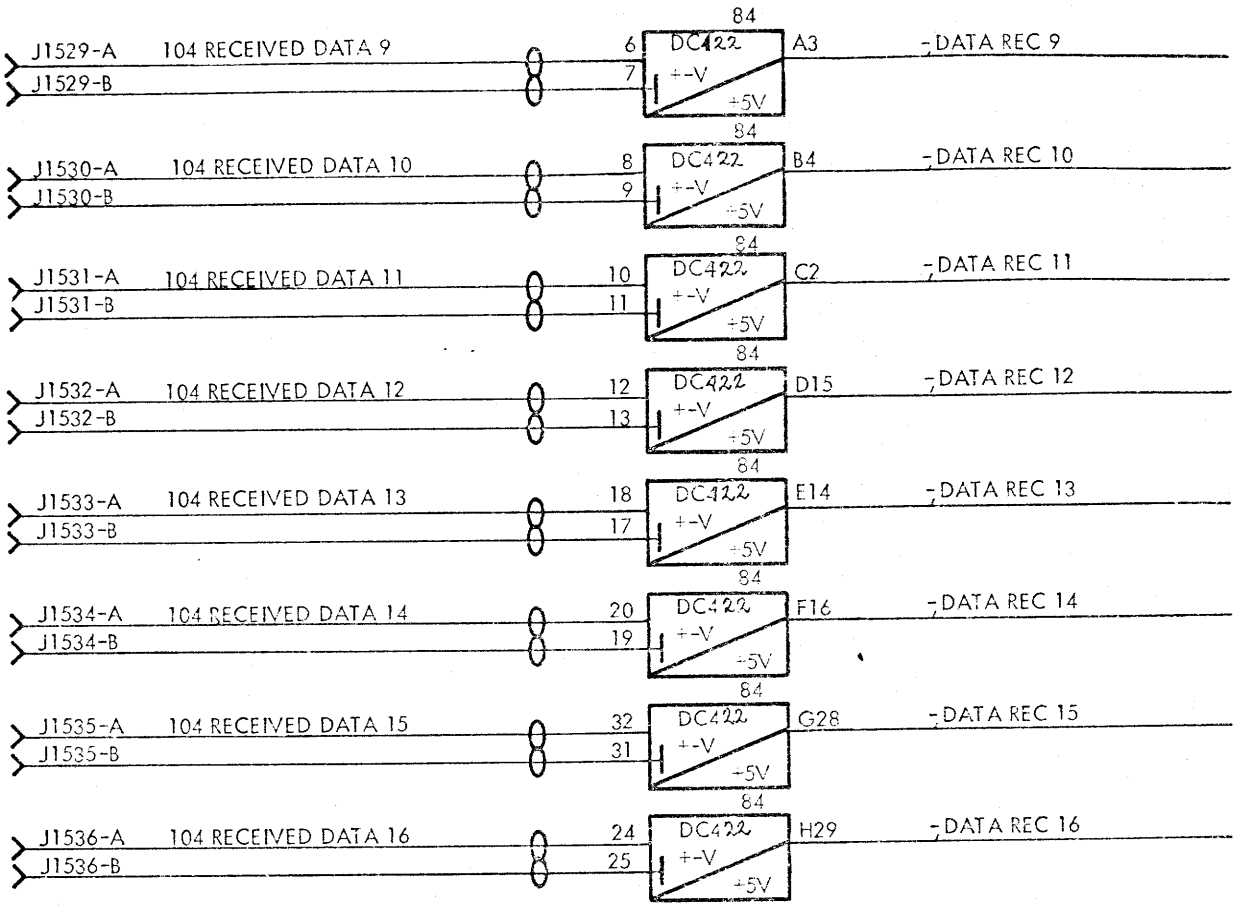
MX425

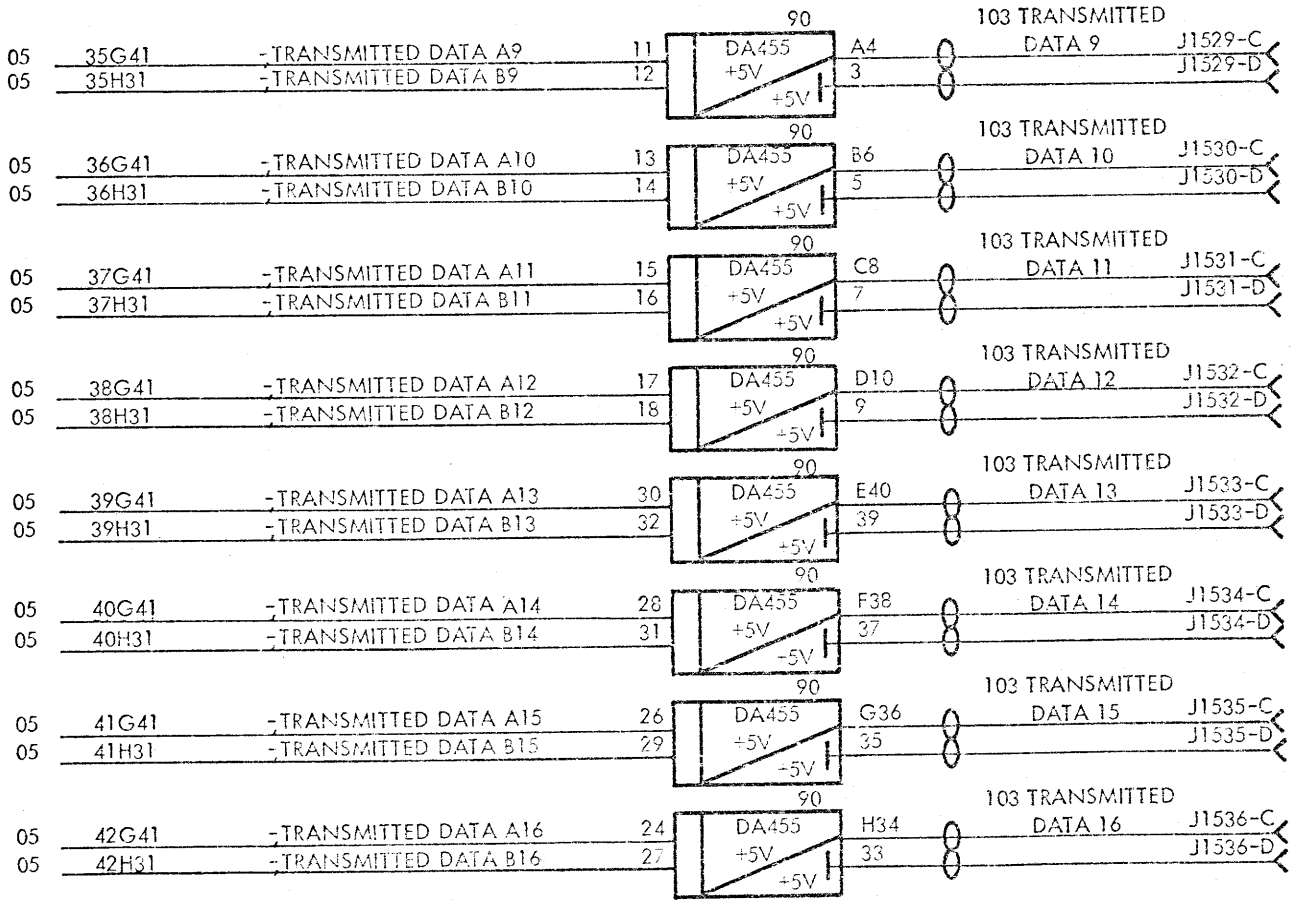
LINE RECEIVERS AND LINE TRANSMITTER FOR DATA SIGNALS DEV 1 - 8

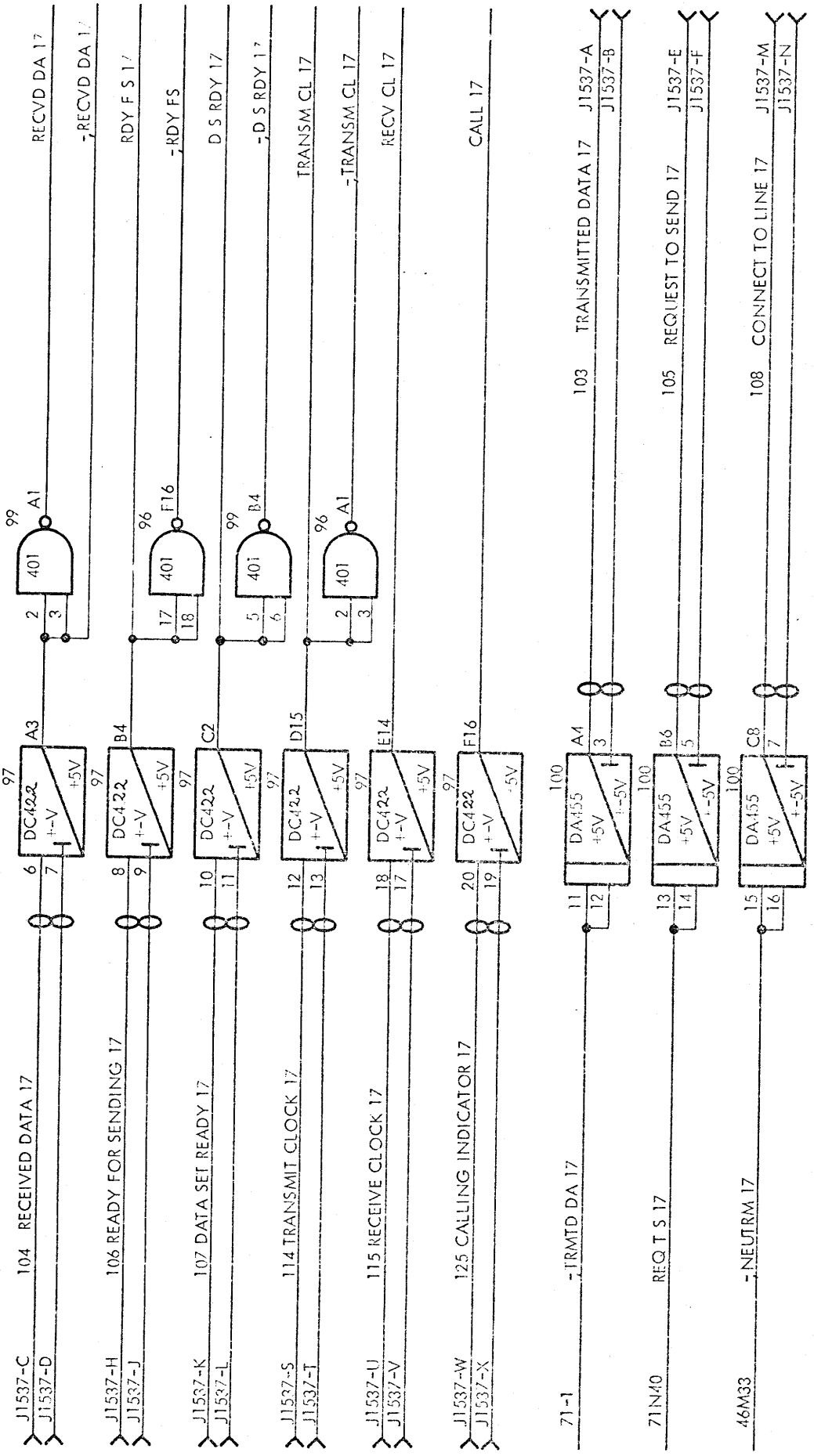
TMX23

R 20879

Logic Diagram


84
J1529-A
J1529-B
104 RECEIVED DATA 9
6
7
DC422
+-V
+5V
A3
-DATA REC 9
84
J1530-A
J1530-B
104 RECEIVED DATA 10
8
9
DC422
+-V
+5V
B4
-DATA REC 10
84
J1531-A
J1531-B
104 RECEIVED DATA 11
10
11
DC422
+-V
+5V
C2
-DATA REC 11
84
J1532-A
J1532-B
104 RECEIVED DATA 12
12
13
DC422
+-V
+5V
D15
-DATA REC 12
84
J1533-A
J1533-B
104 RECEIVED DATA 13
18
17
DC422
+-V
+5V
E14
-DATA REC 13
84
J1534-A
J1534-B
104 RECEIVED DATA 14
20
19
DC422
+-V
+5V
F16
-DATA REC 14
84
J1535-A
J1535-B
104 RECEIVED DATA 15
32
31
DC422
+-V
+5V
G28
-DATA REC 15
84
J1536-A
J1536-B
104 RECEIVED DATA 16
24
25
DC422
+-V
+5V
H29
-DATA REC 16


90
05 35G41 -TRANSMITTED DATA A9 11
05 35H31 -TRANSMITTED DATA B9 12
DA455
+5V
+5V
A4
3
103 TRANSMITTED DATA 9
J1529-C
J1529-D
90
05 36G41 -TRANSMITTED DATA A10 13
05 36H31 -TRANSMITTED DATA B10 14
DA455
+5V
+5V
B6
5
103 TRANSMITTED DATA 10
J1530-C
J1530-D
90
05 37G41 -TRANSMITTED DATA A11 15
05 37H31 -TRANSMITTED DATA B11 16
DA455
+5V
+5V
C8
7
103 TRANSMITTED DATA 11
J1531-C
J1531-D
90
05 38G41 -TRANSMITTED DATA A12 17
05 38H31 -TRANSMITTED DATA B12 18
DA455
+5V
+5V
D10
9
103 TRANSMITTED DATA 12
J1532-C
J1532-D
90
05 39G41 -TRANSMITTED DATA A13 30
05 39H31 -TRANSMITTED DATA B13 32
DA455
+5V
+5V
E40
39
103 TRANSMITTED DATA 13
J1533-C
J1533-D
90
05 40G41 -TRANSMITTED DATA A14 28
05 40H31 -TRANSMITTED DATA B14 31
DA455
+5V
+5V
F38
37
103 TRANSMITTED DATA 14
J1534-C
J1534-D
90
05 41G41 -TRANSMITTED DATA A15 26
05 41H31 -TRANSMITTED DATA B15 29
DA455
+5V
+5V
G36
35
103 TRANSMITTED DATA 15
J1535-C
J1535-D
90
05 42G41 -TRANSMITTED DATA A16 24
05 42H31 -TRANSMITTED DATA B16 27
DA455
+5V
+5V
H34
33
103 TRANSMITTED DATA 16
J1536-C
J1536-D



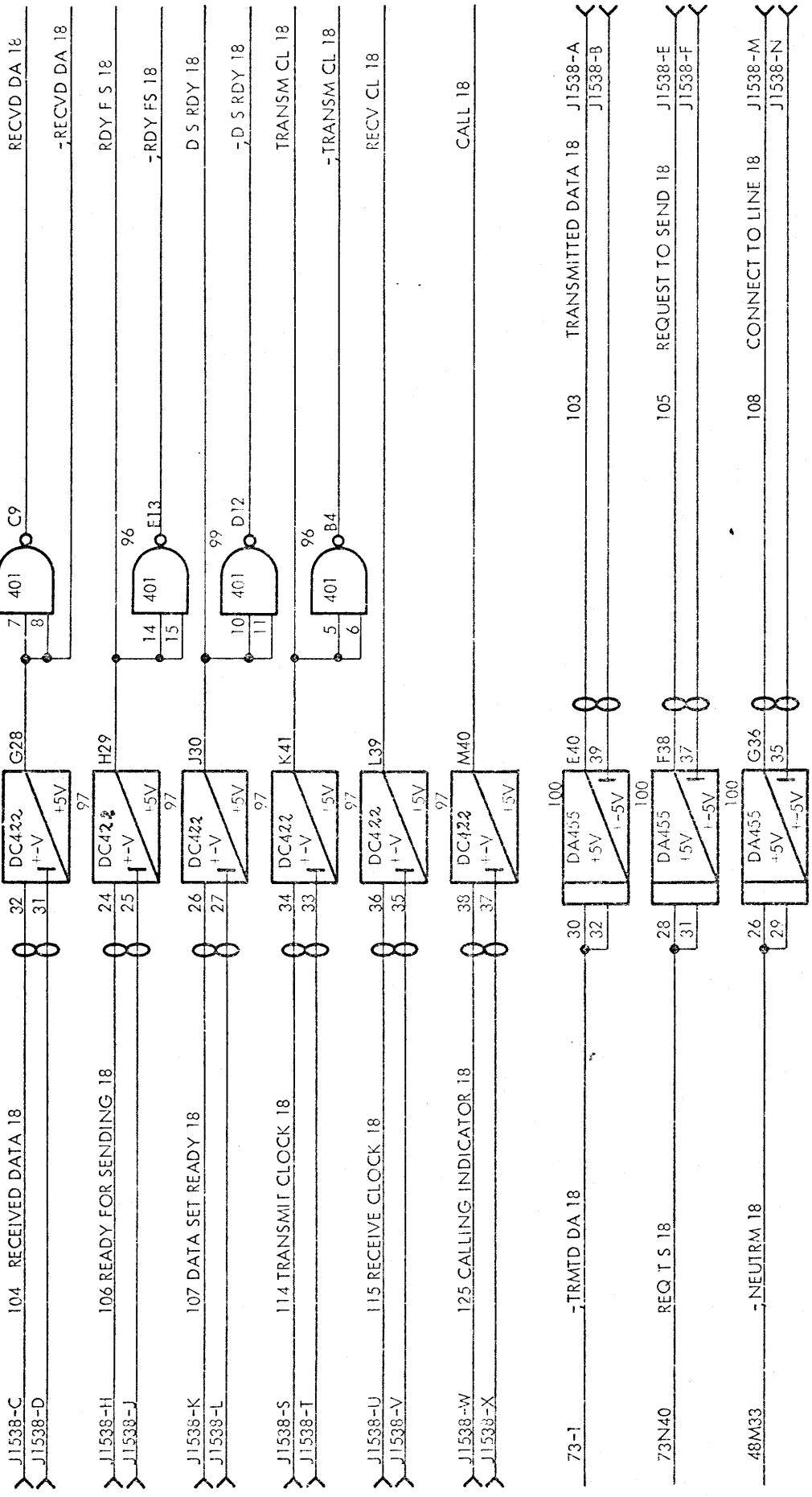
TMX425

R 20881

LINE RECEIVERS AND LINE DRIVERS FOR DATA AND CONTROL SIGNALS

Logic Diagram

TMX25



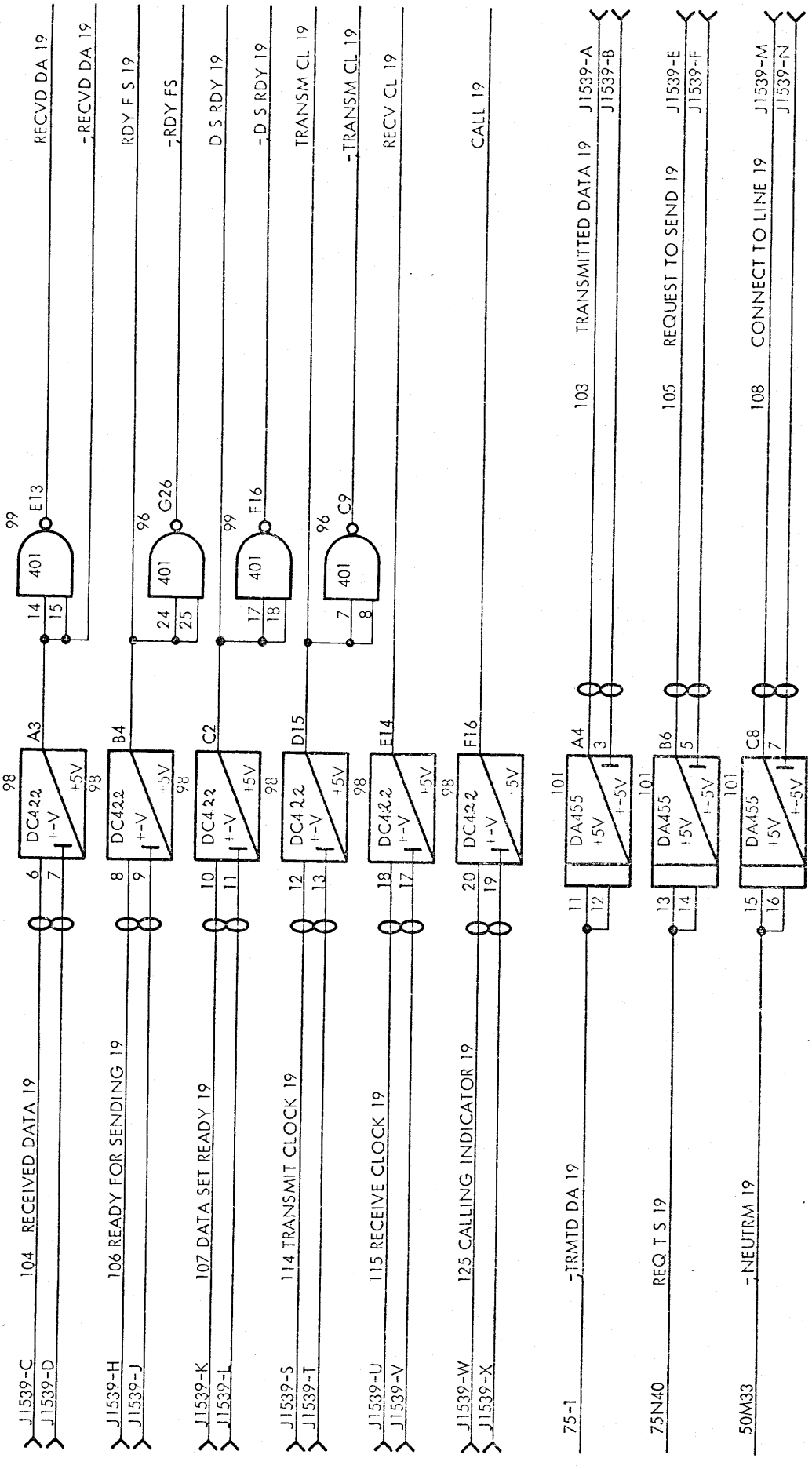
TMX425

LINE RECEIVERS AND LINE DRIVERS FOR DATA AND CONTROL SIGNALS

TMX26

R 20882

Logic Diagram



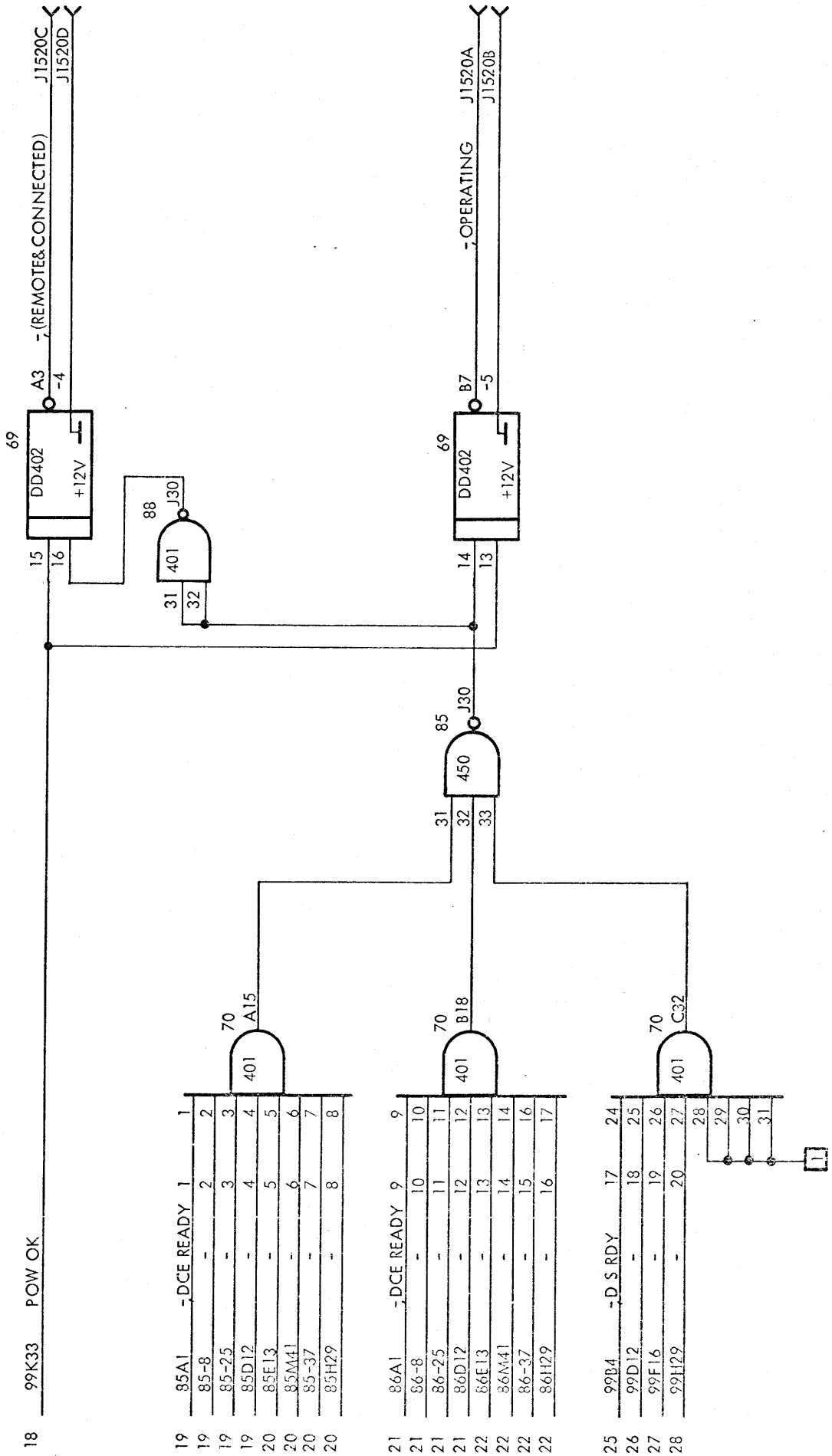
TMX425

R 20883

LINE RECEIVERS AND LINE DRIVERS FOR DATA AND CONTROL SIGNALS

TMX27

Logic Diagram



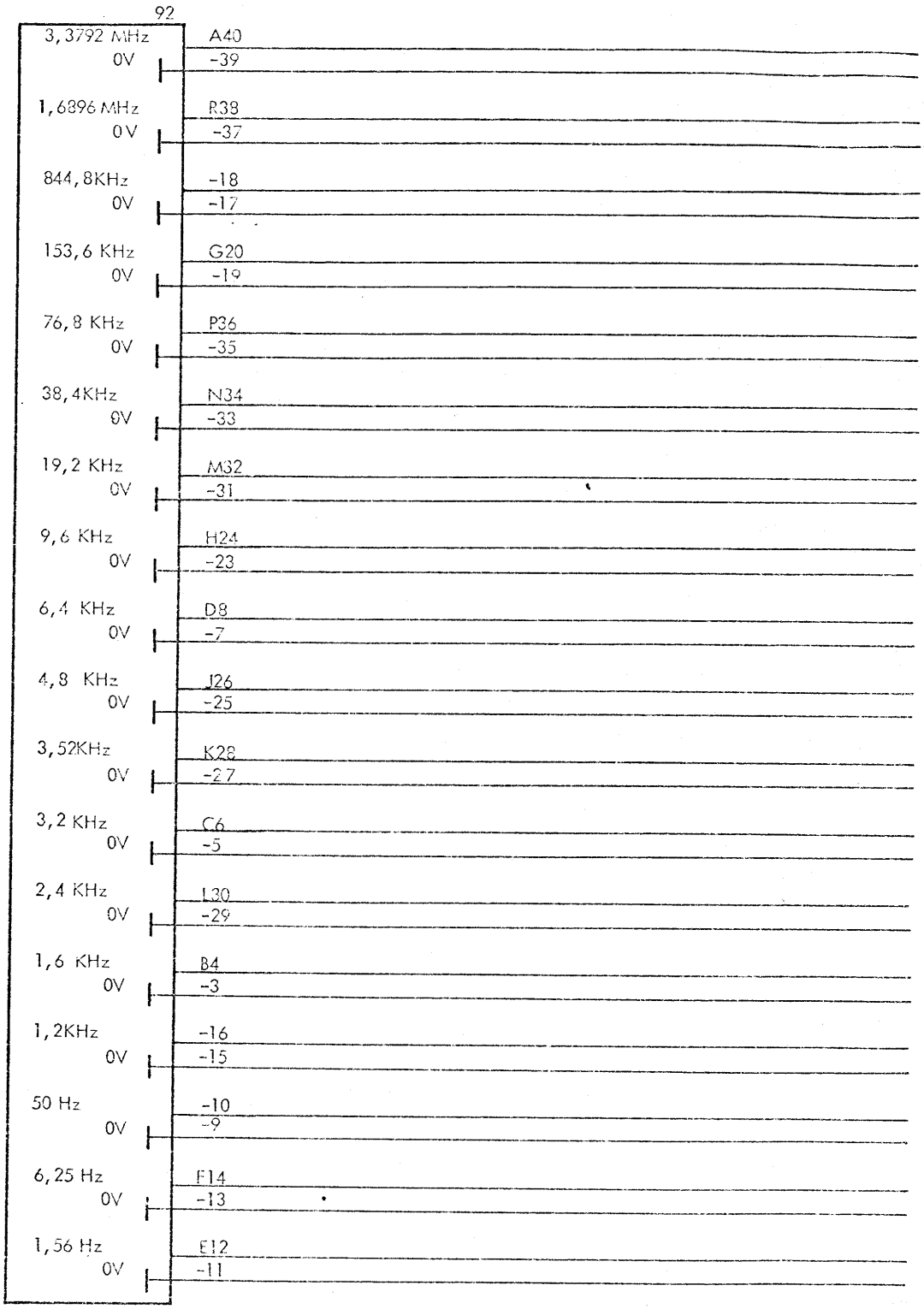
TMX425

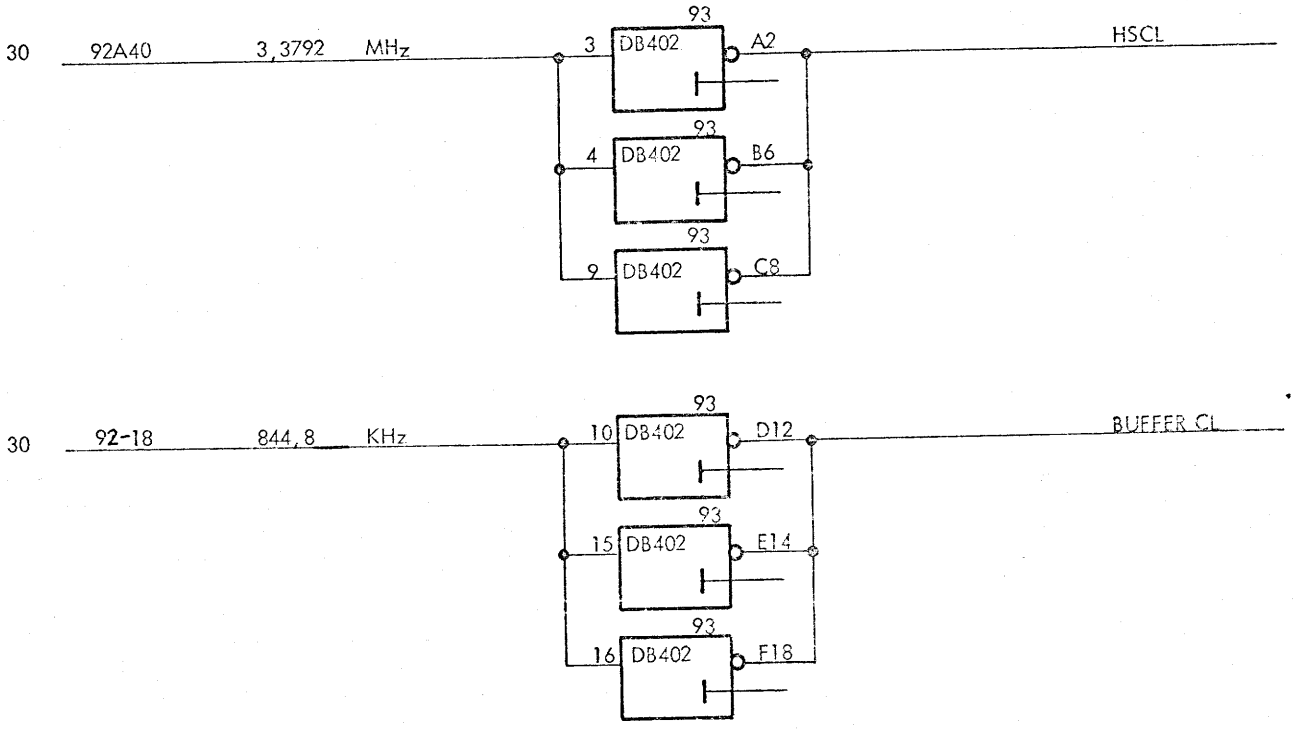
R 10385

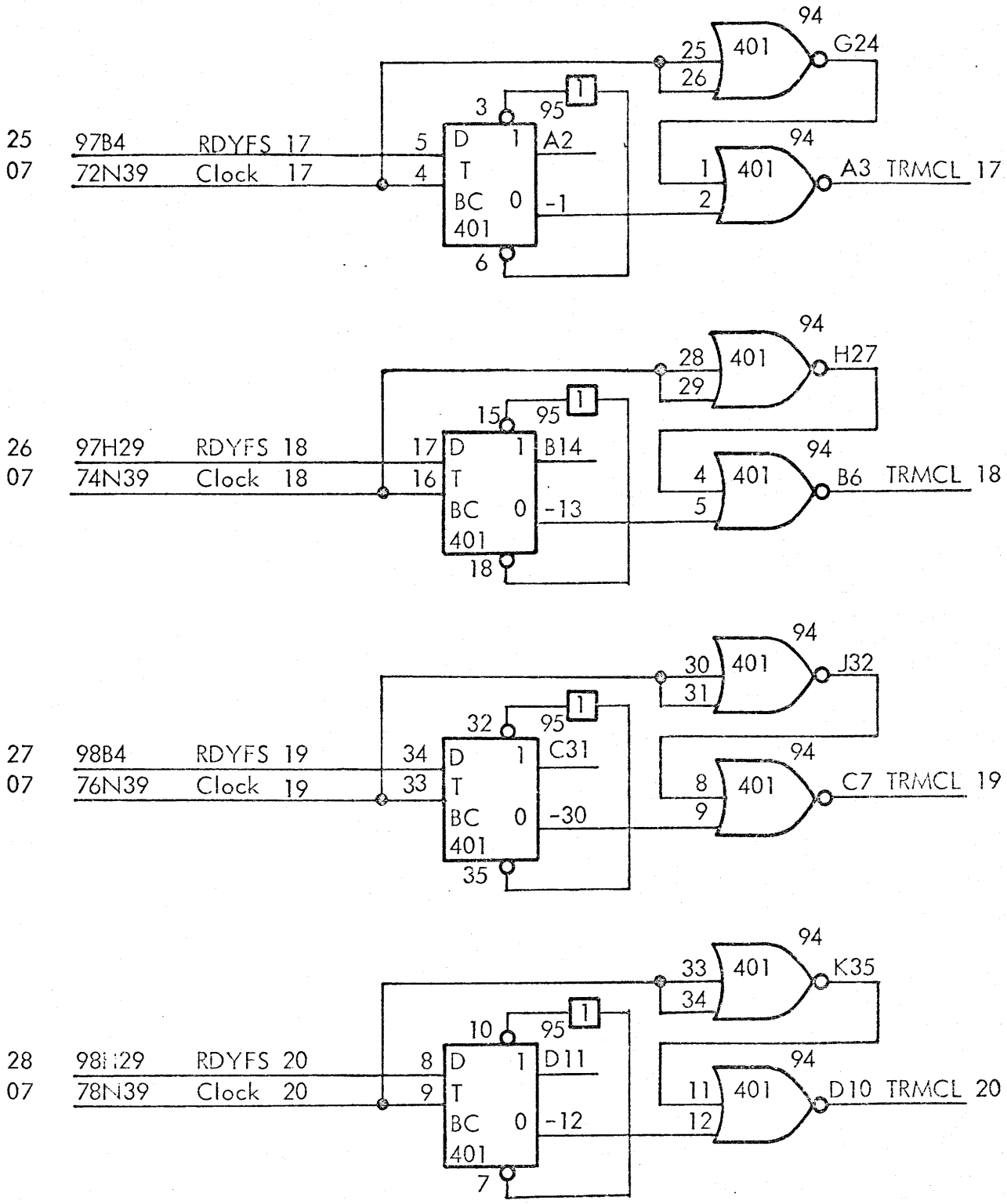
CONTROL CIRCUITS FOR OPERATORS INDICATORS

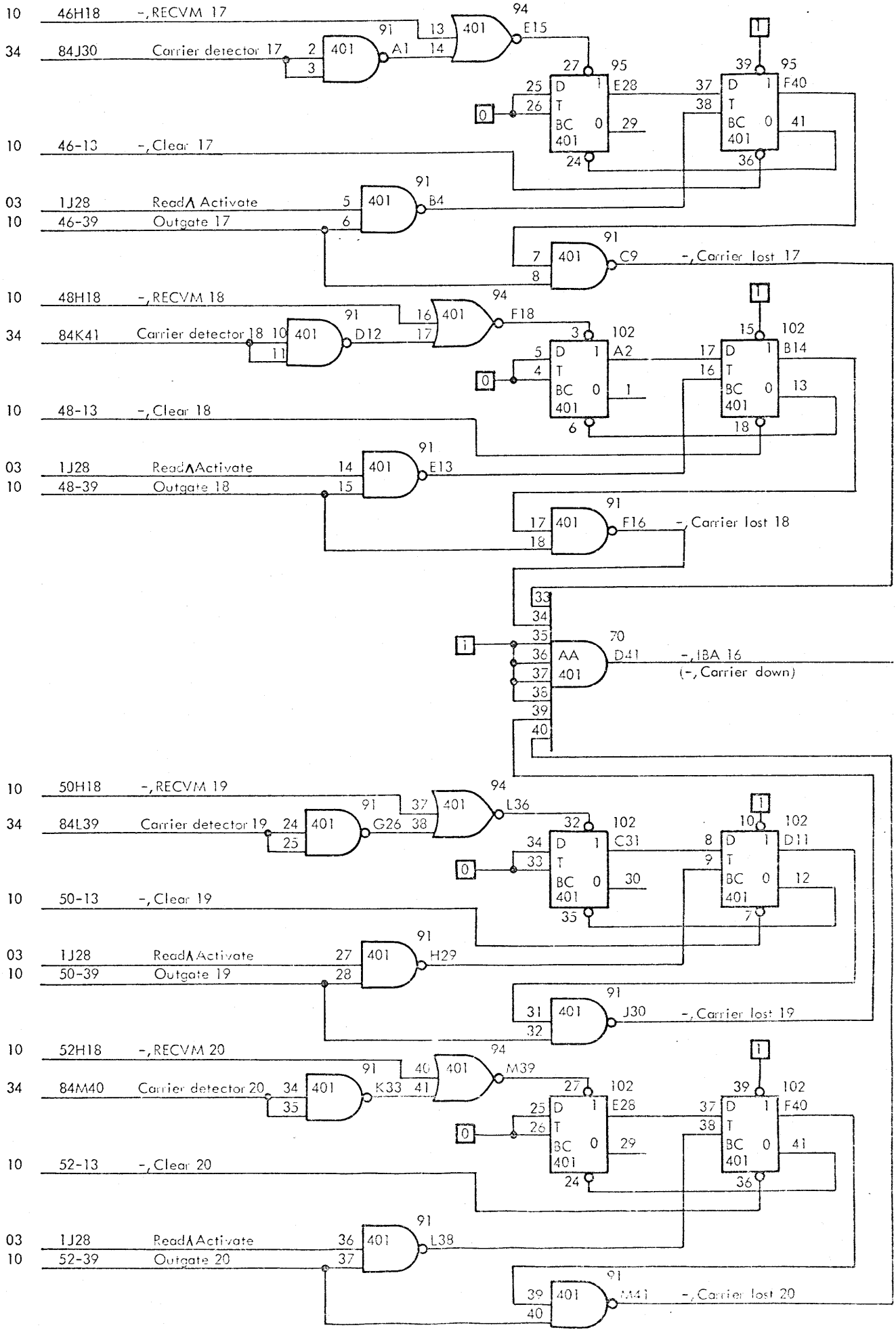
Logic Diagram

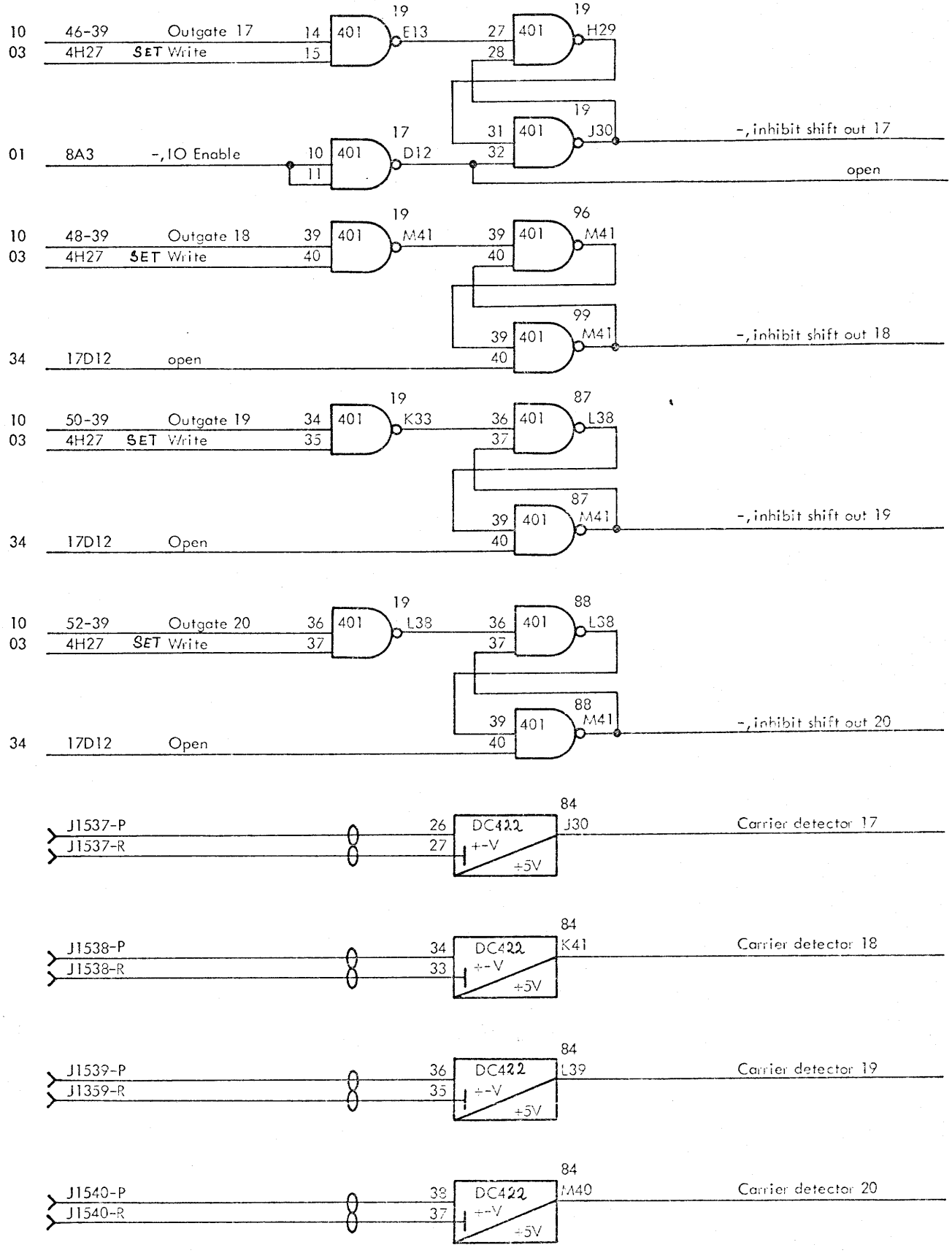
TMX29


92
3,3792 MHz
0V
A40
-39
1,6896 MHz
0V
R38
-37
844,8KHz
0V
-18
-17
153,6 KHz
0V
G20
-19
76,8 KHz
0V
P36
-35
38,4KHz
0V
N34
-33
19,2 KHz
0V
M32
-31
9,6 KHz
0V
H24
-23
6,4 KHz
0V
D8
-7
4,8 KHz
0V
J26
-25
3,52KHz
0V
K28
-27
3,2 KHz
0V
C6
-5
2,4 KHz
0V
L30
-29
1,6 KHz
0V
B4
-3
1,2KHz
0V
-16
-15
50 Hz
0V
-10
-9
6,25 Hz
0V
F14
-13
1,56 Hz
0V
E12
-11


30
92A40
3,3792
MHz
3
DB402
93
A2
HSCL
4
DB402
93
B6
9
DB402
93
C8
30
92-18
844,8
KHz
10
DB402
93
D12
BUFFER CL
15
DB402
93
E14
16
DB402
93
F18


25 97B4 RDYFS 17
07 72N39 Clock 17
D
T
BC
401
A2
-1
95
94
401
G24
A3 TRMCL 17
26 97H29 RDYFS 18
07 74N39 Clock 18
B14
-13
B6 TRMCL 18
27 98B4 RDYFS 19
07 76N39 Clock 19
C31
-30
C7 TRMCL 19
28 98H29 RDYFS 20
07 78N39 Clock 20
D11
-12
K35
D10 TRMCL 20


10 46H18 -,RECVM 17
34 84J30 Carrier detector 17
10 46-13 -,Clear 17
03 1J28 Read Λ Activate
10 46-39 Outgate 17
-,Carrier lost 17
10 48H18 -,RECVM 18
34 84K41 Carrier detector 18
10 48-13 -,Clear 18
03 1J28 Read Λ Activate
10 48-39 Outgate 18
-,Carrier lost 18
-,IBA 16
(-,Carrier down)
10 50H18 -,RECVM 19
34 84L39 Carrier detector 19
10 50-13 -,Clear 19
03 1J28 Read Λ Activate
10 50-39 Outgate 19
-,Carrier lost 19
10 52H18 -,RECVM 20
34 84M40 Carrier detector 20
10 52-13 -,Clear 20
03 1J28 Read Λ Activate
10 52-39 Outgate 20
-,Carrier lost 20


10 46-39 Outgate 17
03 4H27 SET Write
01 8A3 -,IO Enable
34 17D12 open
34 17D12 Open
34 17D12 Open
401
E13
H29
D12
J30
M41
K33
L38
L38
M41
M40
-, inhibit shift out 17
open
-, inhibit shift out 18
-, inhibit shift out 19
-, inhibit shift out 20
J1537-P
J1537-R
J1538-P
J1538-R
J1539-P
J1359-R
J1540-P
J1540-R
DC422
+-V
+5V
K41
L39
Carrier detector 17
Carrier detector 18
Carrier detector 19
Carrier detector 20

RCSL : 44-RT 611
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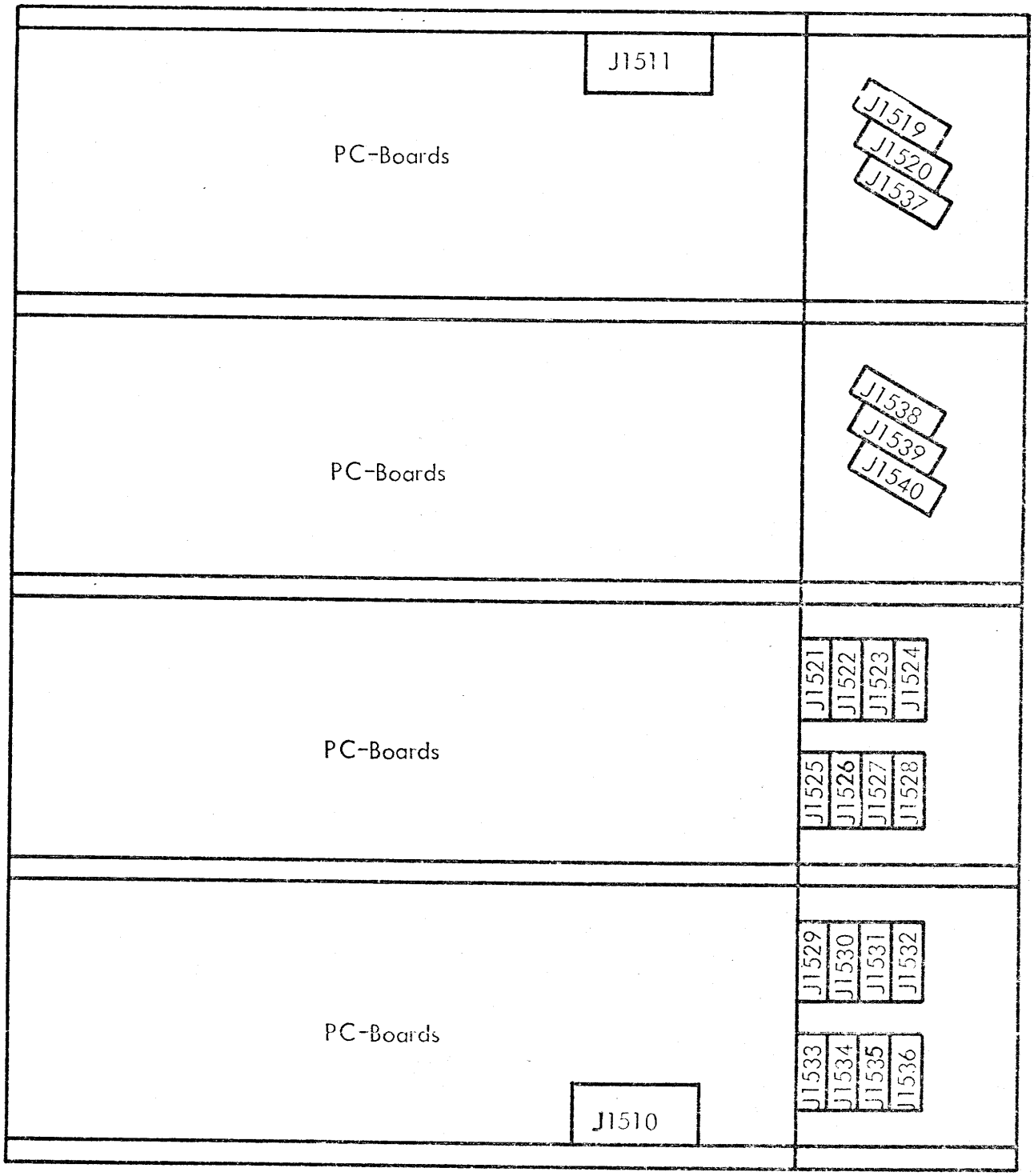
PCBA LOCATION SURVEY AND WIRING OF PLUGS FOR TMX 425

LOW/MEDIUM SPEED TELEMULTIPLEXER.

Keywords : RC 4000, TMX 425 telemultiplexer, PCBA list, wiring list.

Abstract : This paper contains a PCBA location survey and a wiring list for the I/O BUS plugs and for the modem plugs for the RC 4000 telemultiplexer, TMX 425.

CONTENTS DWG.NO.



TMX425

A214/2

PLACEMENTS OF JACKS
REAR WIEV
Figure

Fig. 6

POS. NO.	PCBA NO.	CIRCUITS ON THE PCBA
1	RC0890-1	11 DB402 - 1 DB403
2	RC0839-40	7 AC404
3	RC 0834-1	12 AC401
4	RC3032-1	12 AD401
5	RC0835-1	6 BC401
6	RC3051-1	1 AJ453
7	RC0834-44	8 AC401 - 1 AJ451
8	RC0897-1	10 DC405
9	RC0897-1	10 DC405
10	RC0898-1	1 DB406
11	RC0898-1	1 DB406
12	RC0898-1	1 DB406
13	RC0898-1	1 DB406
14	RC0834-1	12 AC401
15	RC0834-1	12 AC401
16	RC3032-1	12 AD401
17	RC0834-44	8 AC401 - 1 AJ451
18	RC3032-1	12 AD401
19	RC0834-1	12 AC401
20	RC3032-1	12 AD401
21	RC3054-1	1 BG450
22	RC3054-1	1 BG450
23	RC3054-1	1 BG450
24	RC3054-1	1 BG450
25	RC3054-1	1 BG450
26	RC3054-1	1 BG450

POS. NO.	PCBA NO.	CIRCUITS ON THE PCBA
27	RC3128-1	1 SA451
28	RC3128-1	1 SA451
29	RC3128-1	1 SA451
30	RC3128-1	1 SA451
31	RC3128-1	1 SA451
32	RC3128-1	1 SA451
33	RC3128-1	1 SA451
34	RC3128-1	1 SA451
35	RC3128-1	1 SA451
36	RC3128-1	1 SA451
37	RC3128-1	1 SA451
38	RC3128-1	1 SA451
39	RC3128-1	1 SA451
40	RC3128-1	1 SA451
41	RC3128-1	1 SA451
42	RC3128-1	1 SA451
43	RC3125-1	7 AA451 - 3 AH452 - 1 AC401
44	RC3125-1	7 AA451 - 3 AH452 - 1 AC401
45	RC2064-1	Medium speed BUFFER
46	RC2067-1	Medium speed CONTROL
47	RC2064-1	Medium speed BUFFER
48	RC2067-1	Medium speed CONTROL
49	RC2064-1	Medium speed BUFFER
50	RC2067-1	Medium speed CONTROL
51	RC2064-1	Medium speed BUFFER
52	RC 2067-1	Medium speed CONTROL

POS. NO.	PCBA NO.	CIRCUITS ON THE PCBA
53	RC3041-1	1 SA450
54	RC3041-1	1 SA450
55	RC3041-1	1 SA450
56	RC3041-1	1 SA450
57	RC3041-1	1 SA450
58	RC3041-1	1 SA450
59	RC3041-1	1 SA450
60	RC3041-1	1 SA450
61	RC3041-1	1 SA450
62	RC3041-1	1 SA450
63	RC3041-1	1 SA450
64	RC3041-1	1 SA450
65	RC3041-1	1 SA450
66	RC3041-1	1 SA450
67	RC3041-1	1 SA450
68	RC3041-1	1 SA450
69	RC0860-2	4 DD402
70	RC0849-1	1 AA401
71	RC2066-1	Medium speed TRANSMITTER
72	RC2065-1	Medium speed RECEIVER
73	RC2066-1	Medium speed TRANSMITTER
74	RC2065-1	Medium speed RECEIVER
75	RC2066-1	Medium speed TRANSMITTER
76	RC2065-1	Medium speed RECEIVER
77	RC2066-1	Medium speed TRANSMITTER
78	RC2065-1	Medium speed RECEIVER

POS. NO.	PCBA NO.	CIRCUITS ON THE PCBA
79	RC2070-1	12 DC 422
80	RC2070-1	12 DC 422
81	RC2070-1	12 DC 422
82	RC2070-1	12 DC 422
83	RC2070-1	12 DC 422
84	RC2070-1	12 DC 422
85	RC0834-45	9 AC450
86	RC0834-45	9 AC450
87	RC0834-1	12 AC401
88	RC0834-1	12 AC401
89	RC3052-2	8 DA455
90	RC3052-2	8 DA455
91	RC0834-1	12 AC401
92	RC3140-1	
93	RC0890-1	11 DB402 - 1 DB403
94	RC3032-1	12AD401
95	RC0835-1	6BC401
96	RC0834-1	12 AC401
97	RC2070-1	12 DC422
98	RC2070-1	12 DC422
99	RC0834-1	12 AC401
100	RC3052-2	8 DA455
101	RC3052-2	8 DA455
102	RC0835-1	6 BC401
103	RC3066-6	1 FF453 - 1 FF452 - 1 DD451
104	RC2069-1 ~~RC3160-1~~	DC - DC Converter *

*) Note : PCBA RC 3160-1 in position 104 has in the later multiplexers been replaced by PCBA RC 2069-1. The two PCBA's are directly interchangable, and the RC 3160-1 should be replaced by RC 2069-1 in case of troubles.

J 1510 ELCO Varilock Receptacle type 8016-090 code -		
PIN	GEN.ADR	SIGNAL NAME
A	11A8	IO BUS 0
B	11-7	
C	11B6	IO BUS 1
D	11-5	
E	11C4	IO BUS 2
F	11-3	
H	11D2	IO BUS 3
J	11-1	
K	11E41	IO BUS 4
L	11-40	
M	11F39	IO BUS 5
N	11-38	
P	11G37	IO BUS 6
R	11-36	
S	11H35	IO BUS 7
T	11-34	
U	12A8	IO BUS 8
V	12-7	
W	12B6	IO BUS 9
X	12-5	
Y	12C4	IO BUS 10
Z	12-3	
AA	12D2	IO BUS 11
AB	12-1	
AC	12E41	IO BUS 12
AD	12-40	
AE	12F39	IO BUS 13
AF	12-38	
AH	12G37	IO BUS 14
AJ	12-36	
AK	12H35	IO BUS 15
AL	12-34	
AM	13A8	IO BUS 16
AN	13-7	
AP	13B6	IO BUS 17
AR	13-5	
AS	13C4	IO BUS 18
AT	13-3	
AU	13D2	IO BUS 19
AV	13-1	
AW	13E41	IO BUS 20
AX	13-40	
AY	13F39	IO BUS 21
AZ	13-38	
BA	13G37	IO BUS 22
BB	13-36	

PIN	GEN. ADR	SIGNAL NAME
BC	13H35	IO BUS 23
BD	13-34	
BE	8-5	IO ENABLE
BF	8-4	
BH	8-6	IO ADDRESS
BJ	8-7	
BK	8-11	IO ACTIVATE
BL	8-10	
BM	8-12	IO TRANSFER
BN	8-13	
BP	10B6	IO CONNECTED
BR	10-5	
BS	10A8	IO READY
BT	10-7	
BU	10C4	DEV INTERRUPT A
BV	10-3	
BW	10D2	DEV INTERRUPT B
BX	10-1	
BY	1511-BU	
BZ	1511-BV	
CA	1511-BW	
CB	1511-BX	
CC	1511-BY	
CD	1511-BZ	
CE	1511-CA	
CF	1511-CB	
CH	1511-CC	
CJ	1511-CD	
CK	1511-CE	
CL	1511-CF	
CM	1511-CH	
CN	1511-CJ	
CP	1511-CK	
CR	1511-CL	
CS	1511-CM	
CT	1511-CN	
CU	1511-CP	
CV	1511-CR	
CW		0V
CX		0V
CY		0V
CZ		0V
DA		SHIELD
DB		SHIELD

J 1511

ELCO Varilock Receptacle type 8016-090 code –

PIN	GEN ADR	SIGNAL NAME
A	11A8	IO BUS 0
B	11-7	
C	11B6	IO BUS 1
D	11-5	
E	11C4	IO BUS 2
F	11-3	
H	11D2	IO BUS 3
J	11-1	
K	11E41	IO BUS 4
L	11-40	
M	11F39	IO BUS 5
N	11-38	
P	11G37	IO BUS 6
R	11-36	
S	11H35	IO BUS 7
T	11-34	
U	12A8	IO BUS 8
V	12-7	
W	12B6	IO BUS 9
X	12-5	
Y	12C4	IO BUS 10
Z	12-3	
AA	12D2	IO BUS 11
AB	12-1	
AC	12E41	IO BUS 12
AD	12-40	
AE	12F39	IO BUS 13
AF	12-38	
AH	12G37	IO BUS 14
AJ	12-36	
AK	12H35	IO BUS 15
AL	12-34	
AM	13A8	IO BUS 16
AN	13-7	
AP	13B6	IO BUS 17
AR	13-5	
AS	13C4	IO BUS 18
AT	13-3	
AU	13D2	IO BUS 19
AV	13-1	
AW	13E41	IO BUS 20
AX	13-40	
AY	13F39	IO BUS 21
AZ	13-38	
BA	13G37	IO BUS 22
BB	13-36	

PIN	GEN. ADR.	SIGNAL NAME
BC	13H35	IO BUS 23
BD	13-34	
BE	8-5	IO ENABLE
BF	8-4	
BH	8-6	IO ADDRESS
BJ	8-7	
BK	8-11	IO ACTIVATE
BL	8-10	
BM	8-12	IO TRANSFER
BN	8-13	
BP	10B6	IO CONNECTED
BR	10-5	
BS	10A8	IO READY
BT	10-7	
BU	1510-BY	
BV	1510-BU	
BW	1510-CA	
BX	1510-CB	
BY	1510-CC	
BZ	1510-CD	
CA	1510-CE	
CB	1510-CF	
CC	1510-CH	
CD	1510-CJ	
CE	1510-CK	
CF	1510-CL	
CH	1510-CM	
CJ	1510-CN	
CK	1510-CP	
CL	1510-CR	
CM	1510-CS	
CN	1510-CT	
CP	1510-CU	
CR	1510-CV	
CS	10C4	DEV INTERRUPT A
CT	10-3	
CU	10D2	DEV INTERRUPT B
CV	10-1	
CW		0V
CX		0V
CY		0V
CZ		0V
DA		SHIELD
DB		SHIELD

J1520 ELCO Varilock Receptacle, type 8016-038, code -		
PIN	GEN.ADR	SIGNAL NAME
A	69B7	-, OPERATING
B	69-5	0V
C	69A3	-, (REMOTE & CONNECTED)
D	69-4	0V
E		
F		
H		
J		
K		
L		
M		
N		
P		
R		
S		
T		
U		
V		
W		
X		
Y		
Z		
AA		
BB		
CC		
DD		
EE		
FF		
HH		
JJ		
KK		
LL		
MM		
NN		
PP		
RR		
SS		SHIELD
TT		SHIELD

J1521 ELCO Varilock Receptacle, type S016-020, code -		
PIN	GEN. ADR.	SIGNAL NAME
A		104 RECEIVED DATA 1
B		0V
C	89A4	103 TRANSMITTED DATA
D	89-3	0V
E		106 READY FOR SENDING 1
F		0V
H		107 DATA SET READY 1
J		0V
K		109 DATA CARRIER DETECTOR 1
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 1
T	92~~B4~~H 24	1600 ~~HZ~~ 9600 HZ
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J1522 ELCC Varilock Receptacle, type 8016-020, code -		
PIN	GEN ADR	SIGNAL NAME
A		104 RECEIVED DATA 2
B		0V
C	89B6	103 TRANSMITTED DATA 2
D	89-5	0V
E		106 READY FOR SENDING 2
F		0V
H		107 DATA SET READY 2
J		0V
K		109 DATA CARRIER DETECTOR 2
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 2
T	92~~B4~~ H 24	~~1600~~ HZ 9600 Hz
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

ASI

J 1523 ELCC Varilock Receptacle, type 8016-020, code -		
PIN	GEN. ADR.	SIGNAL NAME
A		104 RECEIVED DATA 3
B		0V
C	89C8	103 TRANSMITTED DATA 3
D	89-7	0V
E		106 READY FOR SENDING 3
F		0V
H		107 DATA SET READY 3
J		0V
K		109 CARRIER DETECTOR 3
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 3
T	~~93B4~~ 92H24	~~1600~~ HZ 9600 Hz
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J1524
ELCO Varilock Receptacle, type 8016-020, code -

PIN	GEN. ADR	SIGNAL NAME
A		104 RECEIVED DATA 4
B		0V
C	89D10	103 TRANSMITTED DATA 4
D	89-9	0V
E		106 READY FOR SENDING 4
F		0V
H		107 DATA SET READY 4
J		0V
K		109 DATA CARRIER DETECTOR 4
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 4
T	92~~B4~~ H24	~~1600~~ HZ 9600 H2
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J1525 ELCO Varilock Receptacle, type 8016-020 code -		
PIN	GEN ADR	SIGNAL NAME
A		104 RECEIVED DATA 5
B		0V
C	89E40	103 TRANSMITTED DATA 5
D	89-39	0V
E		106 READY FOR SENDING 5
F		0V
H		107 DATA SET READY 5
J		0V
K		109 DATA CARRIER DETECTOR 5
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 5
T	92B41H24	~~1600 HZ~~ 9600 1/2
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J1526 ELCO Varilock Receptacle, type 8016-020, code -		
PIN	GEN. ADR.	SIGNAL NAME
A		104 RECEIVED DATA 6
B		0V
C	89F38	103 TRANSMITTED DATA 6
D	89-37	0V
E		106 READY FOR SENDING 6
F		0V
H		107 DATA SET READY 6
J		0V
K		109 DATA CARRIER DETECTOR 6
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 6
T	9284424	~~1600~~ HZ 9600 HZ
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J1527 ELCO Varilock Receptacle, type 8016-020 code -		
PIN	GEN. ADR.	SIGNAL NAME
A		104 RECEIVED DATA 7
B		0V
C	89G36	103 TRANSMITTED DATA 7
D	89-35	0V
E		106 READY FOR SENDING 7
F		0V
H		107 DATA SET READY 7
J		0V
K		109 DATA CARRIER DETECTOR 7
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 7
T	92~~B4~~ H 24	~~1600~~ HZ 9600 Hz
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J1528 ELCO Varilock Receptacle, type 8016-020, code -		
PIN	GEN. ADR.	SIGNAL NAME
A		104 RECEIVED DATA 8
B		0V
C	89H34	103 TRANSMITTED DATA 8
D	89-33	0V
E		106 READY FOR SENDING 8
F		0V
H		107 DATA SET READY 8
J		0V
K		109 DATA CARRIER DETECTOR 8
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 8
T	92~~B~~4424	1600 HZ 9600 HZ
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J1529 ELCC Varilock Receptacle, type 8016-020, code -		
PIN	GEN. ADR.	SIGNAL NAME
A		104 RECEIVED DATA 9
B		0V
C	90A4	103 TRANSMITTED DATA 9
D	90-3	0V
E		106 READY FOR SENDING 9
F		0V
H		107 DATA SET READY 9
J		0V
K		109 DATA CARRIER DETECTOR 9
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 9
T	92B4 #24	~~1600~~ HZ 96.2 HZ
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J 1530 ELCO Varilock Receptacle, type 8016-020 code -		
PIN	GEN. ADR	SIGNAL NAME
A		104 RECEIVED DATA 10
B		0V
C	90B6	103 TRANSMITTED DATA 10
D	90-5	0V
E		106 READY FOR SENDING 10
F		0V
H		107 DATA SET READY 10
J		0V
K		109 DATA CARRIER DETECTOR 10
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 10
T	92B4 1124	1600 HZ 9Ccv 112
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J1531 ELCO Varilock Receptacle, type 8016-020, code -		
PIN	GEN. ADR.	SIGNAL NAME
A		104 RECEIVED DATA 11
B		0V
C	90C8	103 TRANSMITTED DATA 11
D	90-7	0V
E		106 READY FOR SENDING 11
F		0V
H		107 DATA SET READY 11
J		0V
K		109 DATA CARRIER DETECTOR 11
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 11
T	92~~B4~~ HZ4	~~1600~~ HZ 9600 HZ
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J1532 ELCO Varilock Receptacle, type 8016-020, code -		
PIN	GEN. ADR.	SIGNAL NAME
A		104 RECEIVED DATA 12
B		0V
C	90D10	103 TRANSMITTED DATA 12
D	90-9	0V
E		106 READY FOR SENDING 12
F		0V
H		107 DATA SET READY 12
J		0V
K		109 DATA CARRIER DETECTOR 12
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 12
T	92~~B4~~ H24	~~1600~~ HZ Given H2
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J 1533 ELCO Varilock Receptacle, type 8016-020, code -		
PIN	GEN. ADR	SIGNAL NAME
A		104 RECEIVED DATA 13
B		0V
C	90E40	103 TRANSMITTED DATA 13
D	90-39	0V
E		106 READY FOR SENDING 13
F		0V
H		107 DATA SET READY 13
J		0V
K		109 DATA CARRIER DETECTOR 13
L		0V
M		8 BIT ELEMENTS
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 13
T	92~~B4~~H24	~~1600~~ HZ 9600 Hz
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J1534 ELCO Varilock Receptacle, type 8016-020, code -		
PIN	GEN. ADR.	SIGNAL NAME
A		104 RECEIVED DATA 14
B		0V
C	90F38	103 TRANSMITTED DATA 14
D	90-37	0V
E		106 READY FOR SENDING 14
F		0V
H		107 DATA SET READY 14
J		0V
K		109 DATA CARRIER DETECTOR 14
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 14
T	92~~B4~~ H24	~~1600~~ HZ 960 HZ
U	92C6	3200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J1535 ELCO Varilock Receptacle, type 8016-020, code -		
PIN	GEN. ADR.	SIGNAL NAME
A		104 RECEIVED DATA 15
B		0V
C	90G36	103 TRANSMITTED DATA 15
D	90-35	0V
E		106 READY FOR SENDING 15
F		0V
H		107 DATA SET READY 15
J		0V
K		109 DATA CARRIER DETECTOR 15
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 15
T	92B4 ~~H2+~~	~~1600~~ HZ ~~Sixty H2~~ 153.6 KHz 9600 Hz
U	92~~C~~6M32	~~3200~~ HZ 19.200 H2
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J1536

ELCO Varilock Receptacle, type 8016-020, code -

PIN	GEN ADR	SIGNAL NAME
A		104 RECEIVED DATA 16
B		0V
C	90H34	103 TRANSMITTED DATA 16
D	90-33	0V
E		106 READY FOR SENDING 16
F		0V
H		107 DATA SET READY 16
J		0V
K		109 DATA CARRIER DETECTOR 16
L		0V
M		8 BIT ELEMENT
N		0V
P		HALF DUPLEX
R		0V
S		DEVICE CLOCK 16
T	92B4 ~~HZ~~	~~1600~~ HZ ~~9600 HZ~~ 153.6 kHz 9600 Hz
U	92~~86~~ M32	~~3200~~ HZ 19200 HZ
V	92K28	3520 HZ
W	92D8	6400 HZ
X		SHIELD

J 1537 ELCO Varilock Receptacle, type 8016-038, code -		
PIN	GEN.ADR	SIGNAL NAME
A	100A4	103 TRANSMITTED DATA 17
B	100-3	0V
C		104 RECEIVED DATA 17
D		0V
E	100B6	105 REQUEST TO SEND 17
F	100-5	0V
H		106 READY FOR SENDING 17
J		0V
K		107 DATA SET READY 17
L		0V
M	100C8	108 CONNECT DATA SET TO LINE 17
N	100-7	0V
P		109 DATA CARRIER DETECTOR 17
R		0V
S		114 TRANSMIT CLOCK 17
T		0V
U		115 RECEIVE CLOCK 17
V		0V
W		125 CALLING INDICATOR 17
X		0V
Y		
Z		
AA		
BB		
CC		
DD		
EE		
FF		0V
HH		
JJ		0V
KK		- ASYNCR 17
LL		0V
MM		SEL CLA 17
NN		0V
PP		SEL CLB 17
RR		0V
SS		SHIELD
TT		SHIELD

J 1538 ELCO Varilock Receptacle, type 8016-038, code -		
PIN	GEN.ADR	SIGNAL NAME
A	100E40	103 TRANSMITTED DATA 18
B	100-39	0V
C		104 RECEIVED DATA 18
D		0V
E	100F38	105 REQUEST TO SEND 18
F	100-73	0V
H		106 READY FOR SENDING 18
J		0V
K		107 DATA SET READY 18
L		0V
M	100G36	108 CONNECT DATA SET TO LINE 18
N	100-35	0V
P		109 DATA CARRIER DETECTOR 18
R		0V
S		114 TRANSMIT CLOCK 18
T		0V
U		115 RECEIVE CLOCK 18
V		0V
W		125 CALLING INDICATOR 18
X		0V
Y		
Z		
AA		
BB		
CC		
DD		
EE		
FF		0V
HH		
JJ		0V
KK		- ASYNCR 18
LL		0V
MM		SEL CLA 18
NN		0V
PP		SEL CLB 18
RR		0V
SS		SHIELD
TT		SHIELD

J 1539 ELCO Varilock Receptacle, type 8016-038, code -		
PIN	GEN.ADR	SIGNAL NAME
A	101A4	103 TRANSMITTED DATA 19
B	101-3	0V
C		104 RECEIVED DATA 19
D		0V
E	101B6	105 REQUEST TO SEND 19
F	101-5	0V
H		106 READY FOR SENDING 19
J		0V
K		107 DATA SET READY 19
L		0V
M	101C8	108 CONNECT DATA SET TO LINE 19
N	101-7	0V
P		109 DATA CARRIER DETECTOR 19
R		0V
S		114 TRANSMIT CLOCK 19
T		0V
U		115 RECEIVE CLOCK 19
V		0V
W		125 CALLING INDICATOR 19
X		0V
Y		
Z		
AA		
BB		
CC		
DD		
EE		
FF		0V
HH		
JJ		0V
KK		-, ASYNCR 19
LL		0V
MM		SEL CLA 19
NN		0V
PP		SEL CLB 19
RR		0V
SS		SHIELD
TT		SHIELD

J1540 ELCO Varilock Receptacle, type 8016-038, code -		
PIN	GEN.ADR	SIGNAL NAME
A	101E40	103 TRANSMITTED DATA 20
B	101-39	0V
C		104 RECEIVED DATA 20
D		0V
E	101F38	105 REQUEST TO SEND 20
F	101-37	0V
H		106 READY FOR SENDING 20
J		0V
K		107 DATA SET READY 20
L		0V
M	101G36	108 CONNECT DATA SET TO LINE 20
N	101-35	0V
P		109 DATA CARRIER DETECTOR 20
R		0V
S		114 TRANSMIT CLOCK 20
T		0V
U		115 RECEIVE CLOCK 20
V		0V
W		125 CALLING INDICATOR 20
X		0V
Y		
Z		
AA		
BB		
CC		
DD		
EE		
FF		0V
HH		
JJ		0V
KK		-, ASYNCR 20
LL		0V
MM		SEL CLA 20
NN		0V
PP		SEL CLB 20
RR		0V
SS		SHIELD
TT		SHIELD

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DESCRIPTION OF SIGNALNAMES
TMX 425
LOW/MEDIUM SPEED TELEMULTIPLEXER

Keywords : RC 4000, TMX 425 telemultiplexer, signal list.

Abstract : This paper contains a complete list of the names used for signals in the logic diagrams for the RC 4000 telemultiplexer, TMX 425, together with a short explanation for each signal name.

SIGNAL NAME	REFERENCE	DESCRIPTION
103 TRANSMITTED DATA X	TMX 23 TMX 24 TMX 25 TMX 26 TMX 27 TMX 28 J 1521 to J 1540	This name represents the 20 data signals which are sent to the terminals. The data terminal equipment will hold circuit 103 in the binary 1 condition during any time interval between characters, and at all other times when no data are to be transmitted via the data channel. The data terminal will not transfer data on circuit 103 unless an ON condition is present on all of the following four circuits: 105 - Request to Send 106 - Ready For Sending 107 Data Set Ready 108 Connect to Line
104 RECEIVED DATA X	J 1521 to J 1540 TMX 23 TMX 24 TMX 25 TMX 26 TMX 27 TMX 28	This name represents 20 signals. One from each of the 20 modems. Namely, the incoming data from 20 terminals before they reach the level converters. Low level corresponds to a logical "1". High level corresponds to a logical "0".

SIGNAL NAME	REFERENCE	DESCRIPTION
105 REQUEST TO SEND X	TMX 25 TMX 26 TMX 27 TMX 28 J1537-J1540	This name represents four signals. One to each of the four MSTC-modems. In the cables to LSTC-modems this signal is strapped to logical 1. High level causes the modem to transmit carrier signal Low level blocks the carrier signal.
106 READY FOR SENDING X	J 1521 .... J 1540 TMX 19 TMX 20 TMX 21 TMX 22 TMX 25 TMX 26 TMX 27 TMX 28	This name represents 20 signals. One from each of the 20 modems. They indicate that the modem is ready to transmit on the line.
107 DATA SET READY X	J 1521 .... J 1540 TMX 19 TMX 20 TMX 21 TMX 22 TMX 25 TMX 26 TMX 27 TMX 28	This name represents 20 signals. One from each of the 20 modems. They indicate that the modems are connected to the line.

SIGNAL NAME	REFERENCE	DESCRIPTION
108 CONNECT TO LINE X	TMX 25 TMX 26 TMX 27 TMX 28 J 1537 to J 1540	This name represents four signals. One from each MSTC. Signals on this circuit control switching of the signal conversion to or from the line. High level causes the modem to connect to the communication channel. Low level causes the modem to disconnect from the communication channel.
109 DATA CARRIER DETECTOR X	J 1521 .... J 1540 TMX 19 TMX 20 TMX 21 TMX 22 TMX 34	This name represents 20 signals. One from each of the 20 modems They indicate that the modem receives the carrier frequency from the other end.
114 TRANSMIT CLOCK X	J 1537 to J 1540 TMX 25 TMX 26 TMX 27 TMX 28	This name represents four signals. One from each MSTC-modem. The condition on this circuit is ON and OFF for nominally equal periods of time. A data signal shall be present on circuit 103 (Transmitted Data) in which the transitions between signal elements nominally occur at the time of thetransitions from OFF to ON condition of circuit 114. The transitions from ON to OFF corresponds to the centre of the signal elements.

SIGNAL NAME	REFERENCE	DESCRIPTION
115 RECEIVE CLOCK X	J 1537 to J 1540 TMX 25 TMX 26 TMX 27 TMX 28	This name represents four signals. One from each MSTC-modem. The condition on this circuit will be ON and OFF for nominally equal periods of time, and a transition from ON to OFF condition shall nominally indicate the centre of each signal element on circuit 104 (RECEIVED DATA).
125 CALLING INDICATOR X	J 1537 to J 1540 TMX 25 TMX 26 TMX 27 TMX 28	MSTC-modem signals. Signals on this circuit indicate whether a calling signal is being received by the modem. The ON condition indicates that a calling signal is being received. The OFF condition indicates that no calling signal is being received.
1 A	TMX 15 TMX 16	Transfer status END BUFFER and INTERRUPT INFORMATION for DEV 1 on IO BUS 0.
2 A	TMX 15 TMX 16	Transfer status PARITY ERROR and INTERRUPT INFORMATION for DEV 2 on IO BUS 1.

SIGNAL NAME	REFERENCE	DESCRIPTION
3 A	TMX 15 TMX 16	Transfer status TIME OUT and INTERRUPT INFORMATION for DEV 3 on IO BUS 2.
4 A	TMX 15 TMX 16	Transfer status OVERRUN and INTERRUPT INFORMATION for DEV 4 on IO BUS 3.
5 A	TMX 15 TMX 16	Transfer INTERRUPT INFORMATION for DEV 5 on IO BUS 4.
16 A	TMX 15 TMX 17	Transfer of INTERRUPT INFORMATION for DEV 17 and IBB8 (for 8 BIT : = 1) on IO BUS 16.
17 A	TMX 15 TMX 17	Transfer of IBB7 (for 8 BIT : = 1) on IO BUS 17.
18 A	TMX 15 TMX 17	Transfer of INTERRUPT INFORMATION for DEV 18 and IBB6 (for 8 BIT : = 1) on IO BUS 18.

SIGNAL NAME	REFERENCE	DESCRIPTION
19 A	TMX 15 TMX 17	Transfer of IBB5 (for 8 BIT : = 1) and IBB8 (for 8 BIT : = 0) on IO BUS 19.
20 A	TMX 15 TMX 17	Transfer of INTERRUPT INFORMATION for DEV 19 on IO BUS 20.
20 B	TMX 15 TMX 17	Transfer of IBB4 (for 8 BIT : = 1) and IBB7 (8 BIT : = 0) on IO BUS 20.
21 A	TMX 15 TMX 17	Transfer of IBB3 (for 8 BIT : = 1) and IBB6 (for 8 BIT : = 0) on IO BUS 21.
22 A	TMX 15 TMX 17	Transfer of INTERRUPT INFORMATION for DEV 20 on IO BUS 22.
22 B	TMX 15 TMX 17	Transfer of IBB2 (for 8 BIT : = 1) and IBB5 (for 8 BIT : = 0) on IO BUS 22.
23 A	TMX 15 TMX 17	Transfer of IBB1 (for 8 BIT : = 1) and IBB4 (for 8 BIT : = 0) on IO BUS 23.

SIGNAL NAME	REFERENCE	DESCRIPTION
3.3792 MHz	TMX 30 TMX 31	Clock-frequency.
1.6896 MHz	TMX 30 TMX 31	Clock-frequency.
1.6 KHz	TMX 30 J 1521 to J 1536	See below.
3.2 KHz	TMX 30 J 1521 to J 1536	See below.
3.52 KHz	TMX 30 J 1521 to J 1540	See below
6.4 KHz	TMX 30 J 1521 to J 1540	The signals 1.6 KHz to 6.4 KHz are clock frequencies for the LSTC controllers. They are sent to all controllers so that each terminal can select the speed by returning the proper clock as DEVICE CLOCK.

SIGNAL NAME	REFERENCE	DESCRIPTION
50 Hz	TMX 30 TMX 10	Clock frequency for the counter to look after that DSRDY is true before 300 ms after ⁻; NEUTRM goes high.
6.25 Hz	TMX 30 TMX 06 TMX 10	LSTC: Clock pulse for the circuit which inhibits input if input is not synchronized with RC 4000. MSTC: Clock pulse for the TIME OUT circuit.
1.56	TMX 30 TMX 06	Clock pulse for the TIME OUT circuit (LSTC).
8 BIT ELEMENT	J 1521 .... J 1536 TMX 06	When this line is left open in the cable for the terminal, the terminal must send and accept 8 bit codes. With the line shortened to ground, the terminal must send and accept 5 bit codes.
8 BIT	TMX 14 TMX 04 TMX 13 TMX 15	Indicates that the selected terminal uses 8 bit codes. Always true when a MSTC terminal is selected.

SIGNAL NAME	REFERENCE	DESCRIPTION
~ 8 BIT	TMX 14 TMX 04 TMX 15	Indicates that the selected terminal uses 5 bit codes.

SIGNAL NAME	REFERENCE	DESCRIPTION
ACTIVE	TMX 02 TMX 04	True when a device in TMX 425 has been addressed. Cleared on the trailing edge of ENABLE.
¬ ACTIVE	TMX 02 TMX 01	The internal representation of IO ACTIVATE. Used as strobe pulse in the Command Register.
ADDRESS	TMX 01 TMX 04	The internal representation of IO ADDRESS.
¬ ADDRESS	TMX 01 TMX 02 TMX 04	See above.
¬ ADDRESS & 8 BIT	TMX 04	True during the NOT IO ADDRESS PHASE when 8 bit codes are used.
¬ ADDRESS & ¬ 8 BIT	TMX 04	True during the NOT IO ADDRESS phase when 5 bit codes are used.
¬ (ADDRESS & ¬ 8 BIT)	TMX 04	True during the IO ADDRESS phase when 5 bit codes are used.

SIGNAL NAME	REFERENCE	DESCRIPTION
ASYNCR X	TMX 08 TMX 07	Same as above.
-, ASYNCR X	J 1537 .... J 1540 TMX 07 TMX 08 TMX 09	-, ASYNChRonous mode X. One signal in each MSTC. Strapped to ground if Asynchronous transmission mode is wanted.

SIGNAL NAME	REFERENCE	DESCRIPTION
⁻; BIT REQ X	TMX 08 TMX 09	This name represents four signals. One in each MSTC. ⁻; BIT REQuest. Whenever the buffer system has answered ⁻; SER DA RDY, this clock signal is started requesting a whole character bit for bit.
BUFFER CL	TMX 31 TMX 09	422,4 Khz clock
BUS 10	TMX 01 TMX 02	See below.
BUS 11	TMX 01 TMX 02	See below.
BUS 12	TMX 01 TMX 02	See below.
BUS 13	TMX 01 TMX 02	See below.

SIGNAL NAME	REFERENCE	DESCRIPTION
BUS 14	TMX 01 TMX 02	See below.
BUS 15	TMX 01 TMX 02	See below.
BUS 16	TMX 01 TMX 02	See below.
BUS 17	TMX 01 TMX 02 TMX 04	See below.
BUS 18	TMX 01 TMX 04	See below.
BUS 19	TMX 01 TMX 04	See below.
BUS 20	TMX 01 TMX 04	See below.
BUS 21	TMX 01 TMX 03 TMX 04	See below.

SIGNAL NAME	REFERENCE	DESCRIPTION
BUS 22	TMX 01 TMX 03 TMX 04	See below.
BUS 23	TMX 01 TMX 03 TMX 04	See below.
BUS P	TMX 01 TMX 04	The signals BUS 10 to BUS P are the internal representation of the IO BUS LINES 10 to 23. BUS P is the parity of BUS 17 to BUS 23. During IO ADDRESS BUS 10 to 17 carries the device address, while BUS 18 to 23 carries the command. Possible output data are carried on BUS 17 to 23 during IO TRANSFER.

SIGNAL NAME	REFERENCE	DESCRIPTION
CALL ITR X	TMX 12 TMX 17	CALLing InTeRrupt X. This name represents four signals. One from each MSTC. They are generated by the interrupt expander and indicate which terminals wanted to interrupt on calling indicator.
CALL X	TMX 25 TMX 26 TMX 27 TMX 28 TMX 12	This name represents four signals. One from each MSTC. The modem signal CALLING INDICATOR after passing the level converters.
CHAR ITR	TMX 11 TMX 16	CHARacter InTeRrupt. True if at least 1 bit is set up in the interrupt register 0. Reset on the trailing edge of ENABLE after the ITR REG 0 has been selected.
CHAR ITR X	TMX 11 TMX 15	CHARacter InTeRrupt X. This name represents four signals. One from each MSTC. They are generated by the interrupt expanders if the signal ITR 1 has set up 1 bit in these expanders.

SIGNAL NAME	REFERENCE	DESCRIPTION
CH LENGTH 0 X	J 1537 .... J 1540	This name represents four signals. One in each MSTC. The least significant bit in the 2 bit code used to select the wanted numbers of bits/character.
CH LENGTH 1 X	J 1537 .... J 1540 TMX 07 TMX 08	Same as above, but the most significant bit. bits/character : = 5 + (CH LENGTH 0 X x 2^0 + CH LENGTH 1 X x 2^1).
CLEAR X	TMX 10 TMX 07 TMX 09	This name represents four signals. One in each MSTC. True in a period of 500 us after setting up transmit or receive mode. Gives the signal ¬ FILL BUFFER.
¬ CLEAR X	TMX 10 TMX 07	Same as above. Used to bring the receiver in NOT SYN MODE.
CLOCK X	TMX 07 TMX 32	This name represents four signals. One in each MSTC. Used to generate the transmit clock in synchronons mode.
CONNECTED	TMX 14 TMX 16	LSTC: True when the selected LSTC has a terminal connected to it. MSTC: A MSTC is always connected The interrupt registers are always connected.

SIGNAL NAME	REFERENCE	DESCRIPTION
⁻, DA 1 X .. ⁻, DA 8 X	TMX 07	Represents parallel information outputs from the Receiver Unit. Must be strobed with the signal RECVD DA RDY.
⁻, DATA REC X	TMX 23 TMX 24 TMX 06	This name represents 16 signals, namely the incoming data from the 16 terminals after it has passed the level converters.
DCE READY X	TMX 19 TMX 20 TMX 21 TMX 22 TMX 06	See below.
⁻, DCE READY X	TMX 19 TMX 20 TMX 21 TMX 22 TMX 29	This name represents 16 ready signals from the modems. The three ready signals from each modem are ored together to give a DCE READY signal.
DEVICE CLOCK X	J 1521 ... J 1536 TMX 06	Clock frequency for a LSTC.

SIGNAL NAME	REFERENCE	DESCRIPTION
DEV INTERRUPT A	TMX 16 J 1510 J 1511	IO BUS signal for CHAR ITR.
DEV INTERRUPT B	TMX 16 J 1510 J 1520	IO BUS signal for KEY ITR.
DSRDY X	TMX 25 TMX 26 TMX 27 TMX 28 TMX 10	See below.
~ DSRDY X	TMX 25 TMX 26 TMX 27 TMX 28 TMX 07	This name represents four signals. One in each MSTC. Internal representation of the V-24 modem signal DATA SET READY.

SIGNAL NAME	REFERENCE	DESCRIPTION
ENABLE	TMX 01 TMX 02 TMX 03 TMX 06 TMX 10	See below.
¬ ENABLE	TMX 01 TMX 11 TMX 12	The internal representation of IO ENABLE.
END CH X	TMX 08	This name represents four signals. One in each MSTC. Indicates that the last bit of the character is being transmitted. In synchronous mode it is the same as END DATA, but in asynchronous mode it is delayed to bit-times because START-bit and STOP-bit are added to the character.
¬ END X	TMX 09	This name represents four signals. One in each MSTC. In receive mode (¬ RECVM : = 0) decoding of the situation: INPUT FLAG: = 0 OUTPUT FLAG : = 0 In transmit mode (REQTS : = 1) decoding of the situation: INPUT FLAG: = 1 OUTPUT FLAG: = 1.

SIGNAL NAME	REFERENCE	DESCRIPTION
END BUFFER	TMX 14 TMX 15	LSTC: True if the selected LSTC is strapped up to HALF DUPLEX. MSTC: In receive mode if the output is empty. In transmit mode if both buffers are empty.
END DATA X	TMX 08	This name represents four signals. One in each MSTC. When true no more valid data bits are requested from the output buffer.
⁻, END RECEIVE X	TMX 05 TMX 06	This name represents 16 signals. One in each LSTC. They indicate that the receive operation has been completed.
⁻, END TRANSMIT X	TMX 05 TMX 06	This name represents 16 signals. One in each LSTC. The indicate that the transmit operation has been completed.

SIGNAL NAME	REFERENCE	DESCRIPTION
¬ EXCHB X	TMX 09 TMX 10	¬ EXCHange Buffer X. This name represents four signals. One in each MSTC. True when the situation: INPUT FLAG: = 1 OUTPUT FLAG: = 0 appears. It will change the buffers and send interrupt to RC 4000.
EXTENDED STOP X	TMX 06 TMX 05	This name represents 16 signals. One in each LSTC. They generate the stop level between the write operations.

SIGNAL NAME	REFERENCE	DESCRIPTION
-, FILL BUFFER	TMX 10 TMX 09	This name represents four signals. One in each MSTC. True during CLEAR-time or when the CHA-TO (100 ms) monostable runs out. It starts the FILL CLOCK. During CLEAR both MARK buffers are filled with all "1"s. After CHA-TO the shifts take place only in the input buffer until INPUT FLAG: = 1 (or max. 500 us.).
FIN DEV X	TMX 11 TMX 15 TMX 16 TMX 17	This name represents 16 signals. One in each LSTC. One in each LSTC. They are generated by the interrupt expanders and indicate which terminal wants to interrupt on termination of an operation.

SIGNAL NAME	REFERENCE	DESCRIPTION
HALF DUPLEX	J 1521 .... J 1536 TMX 06	When true (i.e. floating) this signal indicates that the connected terminal is connected via a half duplex line.
HSCL	TMX 30 TMX 07	High Speed CLock. 3.3792 MC.
HSCL X	TMX 07 TMX 08	See above.

SIGNAL NAME	REFERENCE	DESCRIPTION
-, IBA 1	TMX 05 TMX 09 TMX 13	See below.
-, IBA 2	TMX 05 TMX 09 TMX 13	See below.
-, IBA 3	TMX 05 TMX 09 TMX 13	See below.
-, IBA 4	TMX 05 TMX 09 TMX 13	See below.
-, IBA 5	TMX 05 TMX 09 TMX 13	See below.
-, IBA 6	TMX 05 TMX 09 TMX 13	See below.

SIGNAL NAME	REFERENCE	DESCRIPTION
⁻₇ IBA 7	TMX 05 TMX 09 TMX 13	See below
⁻₇ IBA 8	TMX 05 TMX 09 TMX 13	The signals ⁻₇ IBA 1 to ⁻₇ IBA 8 are bus signals carrying data from the TCs to the multiplexer.
⁻₇ IBA 10	TMX 05 TMX 10 TMX 14	Bus signal for the TIME OUT from the TCs.
⁻₇ IBA 11	TMX 06 TMX 10 TMX 14	Bus signal for the CONNECTED from the TCs.
⁻₇ IBA 12	TMX 06 TMX 10 TMX 14	Bus signal for the READY from the TCs.
⁻₇ IBA 13	TMX 06 TMX 10 TMX 14	MSTC: Bus signal indicating END BUFFER situation.

SIGNAL NAME	REFERENCE	DESCRIPTION
⁻; IBA 14	TMX 06 TMX 10 TMX 14	Bus signal for the 8 BITs from the TCs. Always true when a MSTC is selected.
⁻; IBA 15	TMX 10 TMX 14	Bus signal for the OVERRUN from the MSTC.
⁻; IBA 16	TMX 15	Bus signal for the CARRIER DOWN status from the MSTC.
⁻; IBA 17 X	TMX 10 TMX 15	Bus signal for DATA SET NOT READY from the MSTC.
IBB 1 to IBB 8	TMX 13 TMX 15	These signals are the inversion of ⁻; IBA 1 to ⁻; IBA 8.
INPUT FLAG X	TMX 09 TMX 10	This name represents four signals. One in each MSTC. True when the input buffer is full.
INTRANSFER X	TMX 06 TMX 05	This name represents 16 signals. One in each LSTC. It transfers the contents of the IOB into the transmit/receive register.

SIGNAL NAME	REFERENCE	DESCRIPTION
INTV DEV X	TMX 12 TMX 15 TMX 16 TMX 17	INTerVention DEVice X. This name represents 16 signals. One from each LSTC. They are generated by the interrupt expander and indicate which terminal wants to interrupt on operator intervention.
INTV X	TMX 06 TMX 12	This name represents 16 signals. One in each LSTC. It sets a bit in the interrupt expander when the LSTC wants to interrupt on operator intervention.
IO ACTIVATE	J 1510 - BK J 1511 - BK TMX 01	IO ACTIVATE. Output from the Low Speed Data channel from RC 4000. This busline signal indicates that the addressed device has to be selected and that the device command code has to be stored.
IO ADDRESS	J 1510 - BH J 1511 - BH TMX 01	IO ADDRESS. Output from the Low Speed Data channel from RC 4000. The signal on this bus line indicates the selection phase. Device address and command are on bus lines IO BUS (0 : 23).

SIGNAL NAME	REFERENCE	DESCRIPTION
IOB 1 TO IOB 10	TMX 04 TMX 05 TMX 09	Internal output bus transferring information from the multiplexer to the TCs.
IO ENABLE	J 1510 - BE J 1511 - BE TMX 01	IO ENABLE. Output signal from the Low Speed Data channel from RC 4000. The signal indicates the period of the IO operation. When IO ENABLE = 1, the addressed device must reply to the bus line signals; when IO ENABLE = 0, no device must interfere with the channel.
IO TRANSFER	J 1510 - BM J 1511 - BM TMX 01	IO TRANSFER. Output from the Low Speed Data channel from RC 4000. The signal indicates the data phase. In output operation (WRITE) a Data Word is available on the bus lines IO BUS (0: 23). In input operations (SENSE) the data and status word from the selected device must be gated to the buslines IO BUS (0: 23).

SIGNAL NAME	REFERENCE	DESCRIPTION
ITR 1 X	TMX 10 TMX 11	This name represents four signals. One in each MSTC. InTeRrupt 1 sets a bit in the interrupt expander in the following situations: 1. The buffers are interchanged during input or output (-, EXCHB =0). 2. No input from the telephone line has occurred within 1 sec after the set up of a READ command, or the input has been stopped for 1 sec. 3. The buffer-OVERRUN occurs in receive mode. 4. The END BUFFER occurs in transmit mode. 5. The attached modem fails to connect within 300 ms, or the modem signal DATA SET READY disappears for at least 300 msec.

SIGNAL NAME	REFERENCE	DESCRIPTION
KEY ITR	TMX 12 TMX 16	KEY InTeRrupt. LSTC: Interrupt for RC 4000 on operator intervention. MSTC: Interrupt for RC 4000 on calling indicator signal from the modem.

SIGNAL NAME	REFERENCE	DESCRIPTION
MSCLA	TMX 30	Medium Speed CLock A.
(19.2 KC)	TMX 07	The frequency is 32 X baud rate A.
		Only used in asynchronous mode.
MSCL B	TMX 30	Medium Speed CLock B
(38.4 KC)	TMX 07	The frequency is 32 X baud rate B .
		Only used in asynchronous mode.

SIGNAL NAME	REFERENCE	DESCRIPTION
-; NEUTRM X	TMX 10	-; NEUTRal Mode X.
	TMX 25	This name represents four signals.
	TMX 26	One in each MSTC.
	TMX 27	The MSTC is set to this mode only by a
	TMX 28	SENSE 1 command.

SIGNAL NAME	REFERENCE	DESCRIPTION
ODD PARITY	TMX 13	True if the character transferred on the internal input bus (-, IBA 1 to -, IBA 8) has ODD parity.
-, OPERATING	TMX 29 J 1520	When low, this signal turns on the operating lamp and indicates to the operator that at least one terminal is using the multiplexer.
OUT GATE	TMX 06 TMX 05 TMX 10 TMX 09	This name represents 20 signals. One in each TC. When a TC is selected it gates the contents of the buffer register on to the internal input bus IBA.
OUTPUT FLAG X	TMX 09 TMX 10	This name represents four signals. One in each MSTC. True whenever an output buffer is full.

SIGNAL NAME	REFERENCE	DESCRIPTION
OVERRUN	TMX 14 TMX 15	True if both buffers are filled in the selected MSTC.

SIGNAL NAME	REFERENCE	DESCRIPTION
PARITY ERROR	TMX 13 TMX 15	True if the character transferred on the internal input bus has ODD parity.
POW OK	TMX 18 TMX 03 TMX 10 TMX 14 TMX 16	See below.
~ POW OK	TMX 18 TMX 11 TMX 12	Indicates that the supply voltages are within specified limits.

SIGNAL NAME	REFERENCE	DESCRIPTION
READ	TMX 03 TMX 06 TMX 10	True when a READ command has been received.
READ & ACTIVATE	TMX 03 TMX 06	Generates INTRANSFER during read operations.
READY	TMX 14 TMX 16	True when the selected TC has completed the previous operation. The interrupt registers are always ready.
; READING	TMX 09 TMX 10	This name represents four signals. One in each MSTC. True whenever a character (8 bit) is being read out from the output buffer. Gives NOT IO READY to RC 4000.
RDYFS X	TMX 25 TMX 26 TMX 27 TMX 28 TMX 08 TMX 10	This name represents four signals. One in each MSTC. The modem signal READY FOR SENDING after it has passed the level converters.

SIGNAL NAME	REFERENCE	DESCRIPTION
⁻ (REC & TR) X	TMX 06 TMX 05 TMX 11	This name represents 16 signals. One in each LSTC. They set a bit in the interrupt expander when a LSTC wants to interrupt on completion of an operation.
⁻ RECEIVE X	TMX 06 TMX 05	This name represents 16 signals. One in each LSTC. True when the LSTC holds a read command.
RECEV CL X	TMX 07	This name represents four signals. One in each MSTC. Internal RECEiVe CLock. The trailing edge corresponds to the bit center. The leading edge corresponds to the data shift.
RECV CL X	TMX 25 TMX 26 TMX 27 TMX 28	This name represents four signals. One in each MSTC. Indicates RECEIVE CLOCK from the connected modem after passing the level converters.

SIGNAL NAME	REFERENCE	DESCRIPTION
RECVD DA X	TMX 25 TMX 26 TMX 27 TMX 28 TMX 09	See below.
-; RECVD DA X	TMX 25 TMX 26 TMX 27 TMX 28 TMX 07	This name represents four signals. One in each MSTC. Namely, the incoming data from the four terminals after it has passed the level converters.
RECVD DA RDY X	TMX 07	See below.
-; RECVD DA RDY X	TMX 07 TMX 09 TMX 10	RECeiVeD DAta ReaDY. This name represents four signals. One in each MSTC. True whenever a Received Character is ready from the Receiver Unit. The length of the pulse is one period of MSCL.
-; RECVM X	TMX 10 TMX 09	RECeiVe Mode X. This name represents four signals. One in each MSTC. True when the MSTC is in Receive Mode, i.e. the MSTC is able to accept serial data from the modem.

SIGNAL NAME	REFERENCE	DESCRIPTION
⁻, (REMOTE & CONNECTED)	TMX 29 J 1519	Supply for the Remote Connected Lamp on the operator's panel.
REQ CH X	TMX 08 TMX 10	REQuest CHaracter X. This name represents four signals. One in each MSTC. A short pulse of 35 us. Request to the buffer unit. Is there an output buffer ready to be emptied.
REQTS X	TMX 08 TMX 07 TMX 09 TMX 25 TMX 26 TMX 27 TMX 28	This name represents four signals. One in each MSTC. Internal representation of the V 24 modem signal REQUEST TO SEND. Set by the trailing edge of ⁻, WR & TR. Reset either by a SENSE I command or by ⁻, RREQTS when the buffer is EMPTY.
⁻, REQTS X	TMX 08 TMX 07 TMX 10	Same as above.

SIGNAL NAME	REFERENCE	DESCRIPTION
¬ RREQTS X	TMX 10 TMX 08	This name represents four signals. One in each MSTC. ¬ Reset REQuest To Send X. A SENSE 1 command will give ¬ RREQTS, when the buffer is empty. A READ command gives ¬ RREQTS when the buffer is empty (EMPTY: = 1).

SIGNAL NAME	REFERENCE	DESCRIPTION
SEL 0-31	TMX 02 TMX 16	See below.
⁻; SEL 0-31	TMX 02 TMX 03	True when any of the 20 devices is being addressed.
SEL CL A X	J 1537 ... J 1540 TMX 07	SELect CLock A X. This name represents four signals. One in each MSTC. When true (i.e. floating) the MSCLA is selected.
SEL CL B X	J 1537 ... J 1540 TMX 07	SELect CLock B X. This name represents four signals. One in each MSTC. When true (i.e. floating) the MSCLB is selected.
⁻; SEL DEV X	TMX 02 TMX 06 TMX 10	This name represents 20 signals. A select signal for each TC. ⁻; SEL DEV 1-16 are Low Speed Terminal Controllers. ⁻; SEL DEV 17-20 are Medium Speed Terminal Controllers.

SIGNAL NAME	REFERENCE	DESCRIPTION
-; SEL ITR REG 0	TMX 02 TMX 11 TMX 14	Select signal for interrupt register 0.
-; SEL ITR REG 1	TMX 02 TMX 12 TMX 14	Select signal for interrupt register 1.
SENSE 0	TMX 03 TMX 10 TMX 13 TMX 15	See below.
-; SENSE 0	TMX 03 TMX 11 TMX 12 TMX 14	True when the multiplexer holds a SENSE command with modifier 0.
SENSE 1	TMX 03 TMX 10	True when the multiplexer holds a SENSE command with modifier 1.
-; SER DA RDY X	TMX 10 TMX 08	This name represents four signals. One in each MSTC. Response signal to REQ CH whenever a full OUTPUT BUFFER is ready (OUTPUT FLAG: = 1).

SIGNAL NAME	REFERENCE	DESCRIPTION
SERIAL CL X	TMX 07 TMX 09	This name represents four signals. One in each MSTC. Serial shift pulse to the input-register.
SERIAL DATA IN X	TMX 06 TMX 05	This name represents 16 signals. One in each LSTC. They control the serial inputs to the transmit/receive registers.
SERIAL OUT X	TMX 10 TMX 08	This name represents four signals. One in each MSTC. Serial data output from the output buffer.
SHIFT OUT X	TMX 09 TMX 10	This name represents four signals. One in each MSTC. Only valid in transmit mode (i.e. REQTS: = 1). True when both INPUT FLAG: 0 and OUTPUT FLAG: = 0. Starts shift in input buffer to look after some valid data bits.

SIGNAL NAME	REFERENCE	DESCRIPTION
SHIFT PULSE X	TMX 06 TMX 05	This name represents 16 signals. One in each LSTC. They are the shift pulses for the transmit/receive registers.
-; STOP X	TMX 05 TMX 06	This name represents 16 signals. One in each LSTC. They are the outputs from the STOP-one-shots.
-; SYN PAT X	TMX 07	-; SYN PATTERN X. This name represents four signals. One in each MSTC. True whenever the bit pattern of the used SYN-character is recognized in the received data stream.

SIGNAL NAME	REFERENCE	DESCRIPTION
TIME OUT	TMX 14 TMX 15	LSTC: True if a read or write operation exceeds 0.65 - 1.3 sec's. MSTC: True if no input from telephone line has occurred within 1 sec. after the set up of a read command, or when no input has been detected for 1 sec.
TIME OUT X	TMX 06 TMX 05	This name represents 16 signals. One in each LSTC. They terminate the read or write operations when their duration exceeds 0.65 - 1.3 sec's.
TRANSFER	TMX 01 TMX 03	The internal representation of IO TRANSFER.
-, TRANSFER	TMX 01 TMX 16 TMX 17	Same as above.

SIGNAL NAME	REFERENCE	DESCRIPTION
TRANSM CL X	TMX 25 TMX 26 TMX 27 TMX 28 TMX 07	This name represents four signals. One in each MSTC. Namely, the modem signal TRANSMIT CLOCK after it has passed the level converters.
⁻, TRANSMIT STOP X	TMX 06 TMX 05	This name represents 16 signals. One in each LSTC. They transmit stop on half duplex lines when the LSTC has no WRITE command stored.
⁻, TRANSMITTED DATA A X	TMX 05 TMX 23 TMX 24	This name represents 16 signals. One in each LSTC. Namely, data for the 16 terminals.
⁻, TRANSMITTED DATA B X	TMX 05 TMX 23 TMX 24	This name represents 16 signals. One in each LSTC. They transmit extended stop for the 16 terminals.
TRM CL X	TMX 32 TMX 08 TMX 10	This name represents four signals. One in each MSTC. Internal TRansMit CLock. The trailing edge corresponds to the bit center. The leading edge to data shift.

SIGNAL NAME	REFERENCE	DESCRIPTION
TRMTD DA X	TMX 08	See below.
-, TRMTD DA X	TMX 08 TMX 25 TMX 26 TMX 27 TMX 28	-, TRansMitTed DAta X. This name represents four signals. One in each MSTC. The modem signal TRANSMITTED DATA after it has passed the level converters.
TRMTG DA X	TMX 08	This name represents four signals. One in each MSTC. TRansMiT Gate Data X. Set by the trailing edge of REQ CH if there is -, SER DA RDY. Reset by END CH. True during the time a character is being transmitted.

SIGNAL NAME	REFERENCE	DESCRIPTION
WRITE	TMX 03 TMX 06	True when the multiplexer holds a WRITE Command.
WRITE & TRANSFER	TMX 03 TMX 06 TMX 10	Generates INTRANSFER during write operations (LSTC). Generates ¬ WR & TR during write operations (MSTC).
¬ WR & TR X	TMX 10 TMX 08 TMX 09	This name represents four signals. One in each MSTC. WRITE & TRANSFER gated with the OUTGATE X signal.
¬ WRITING X	TMX 09 TMX 10	This name represents four signals. One in each MSTC. True whenever a character (8 bit) is being written into the input buffer. Gives NOT IO READY to RC 4000.

RCSL: 44-RT 613
PP : 1:95
Editor: Knud Sørensen
Edited: April 1973

CARD SPECIFICATIONS, CIRCUIT DIAGRAMS AND PCBA ASSEMBLY DRAWINGS,

TMX 425

LOW/MEDIUM SPEED TELEMULTIPLEXER.

Keywords : RC 4000, TMX 425 telemultiplexer, PCBA specifications.

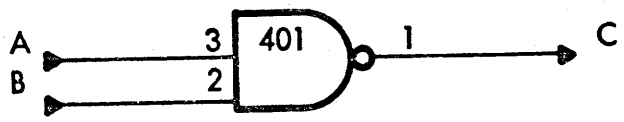
Abstract : This paper contains a complete set of documentation for the PCBA's used in the RC 4000 telemultiplexer, TMX 425.

CONTENTS DWG.NO. RCSL:

CONTENTS DGW.NO: RCSL:

CONTENTS DGW.NO. RCSL:

AC401



CIRCUIT DESCRIPTION

The AC401 is a 2-input NAND-element

C = -, (A & B)

SPECIFICATIONS

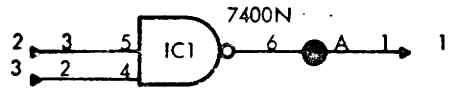
ELECTRICAL CHARACTERISTICS

Input Loading		1 unit load (each input)
Fan-Out		10 unit loads

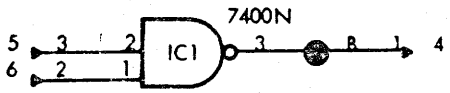
SWITCHING CHARACTERISTICS

Propagation Time	td(1)	Typ. 18 nS; Max. 29 nS
	td(0)	Typ. 8 nS; Max. 15 nS

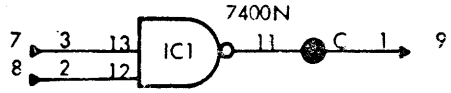
Circuit A



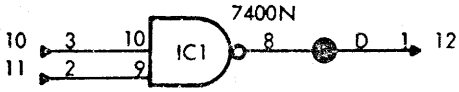
Circuit B



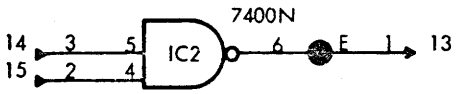
Circuit C



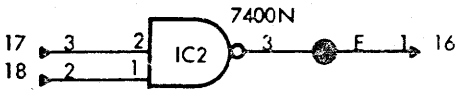
Circuit D



Circuit E



Circuit F



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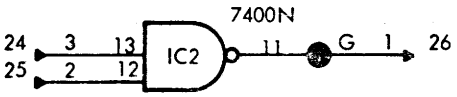
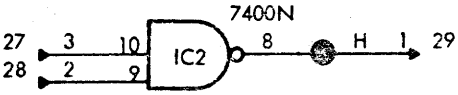


Circuit H



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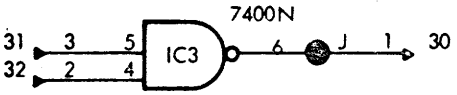
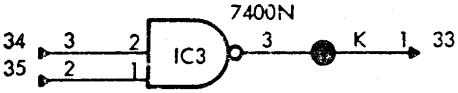
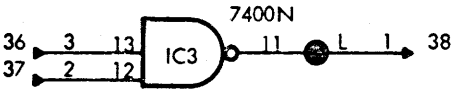


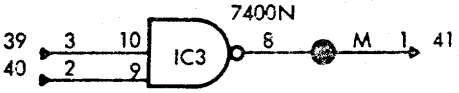
Circuit K



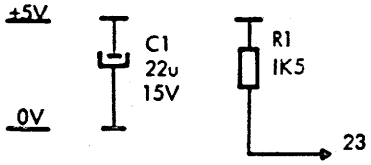
Circuit L



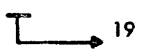
Circuit M



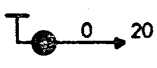
Circuit N



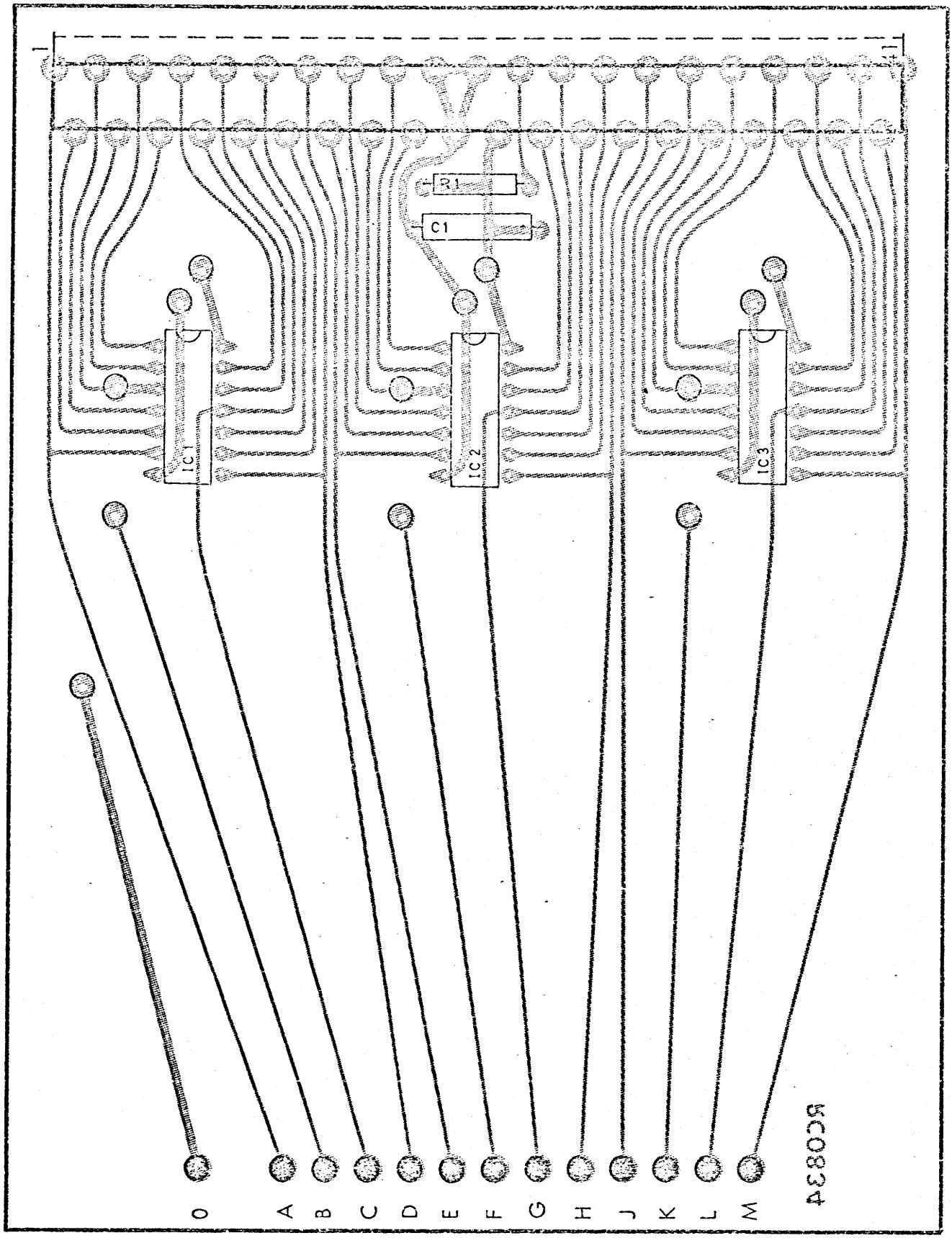
Circuit P



Circuit R



POWER REQUIREMENTS		
+5 V	PIN. 22	40 mA
0 V	PIN. 21	
POWER DISSIPATION: 210 mW		

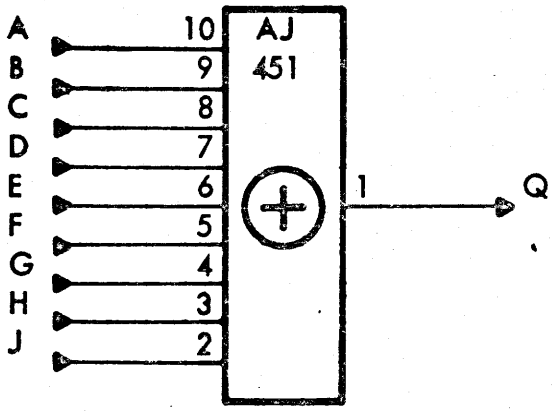


101167HC 120869CEM 120869JA 120869AAGR

RCLM400 12 AC401 RC0834-1

A20416 PCB Assembly Drawing

AJ451



CIRCUIT DESCRIPTION

The AJ451 is a 9 input parity generator or parity checker.

The output is determined by

$$Q = A \oplus B \oplus C \oplus D \oplus E \oplus F \oplus G \oplus H \oplus J$$

giving a high level at the output if an odd number of inputs are high.

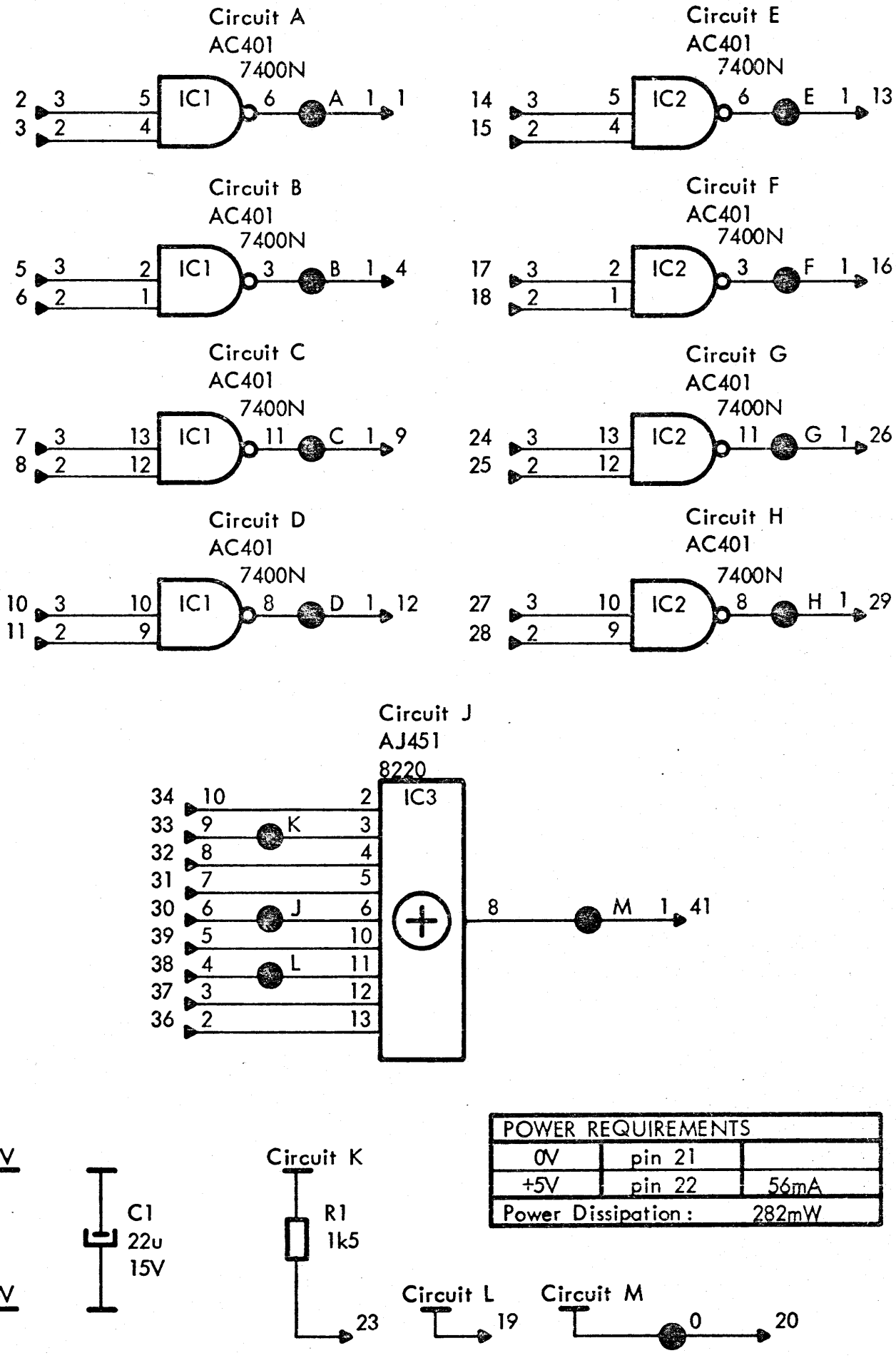
SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input levels	RCLM400 standard levels
Input Load	1 unit load (each input)
Fan Out	10 unit loads

SWITCHING CHARACTERISTICS

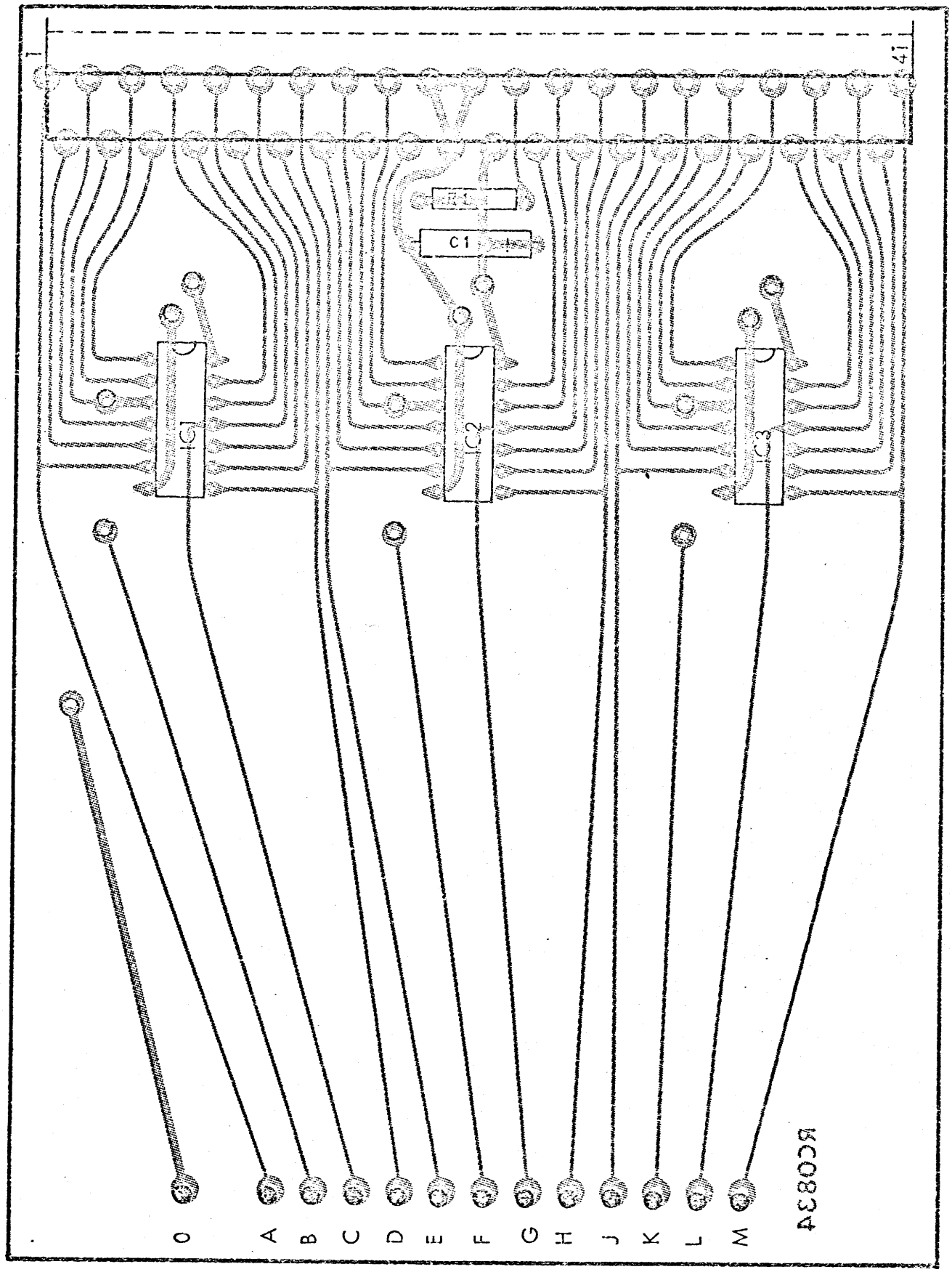
Transition to Logical 0	
from input A-B-C-D-E-F-G-H	max. 42 nS, min. 22 nS
from input J	max. 16 nS, min. 13 nS
Transition to Logical 1	
from input A-B-C-D-E-F-G-H	max. 48 nS, min. 28 nS
from input J	max. 30 nS, min. 27 nS



POWER REQUIREMENTS		
0V	pin 21	
+5V	pin 22	56mA
Power Dissipation :		282mW

RCLM400 1 AJ451, 8 AC401 RC0834-44

A20 173 PCBA Circuit Diagram

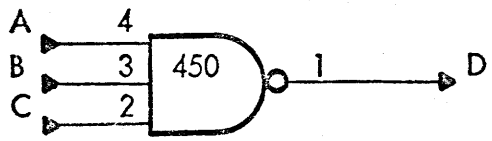


240269 BN 240869 KS 071069 JA 090170BN

RCLM400 1 AJ451 , 8 AC401 RC0834-44

A20199 PCB Assembly Drawing

AC450



CIRCUIT DESCRIPTION

The AC450 is a 3-input NAND-element.

C= -,(A & B & C).

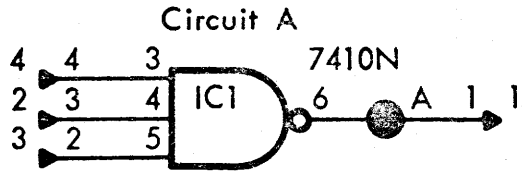
SPECIFICATIONS

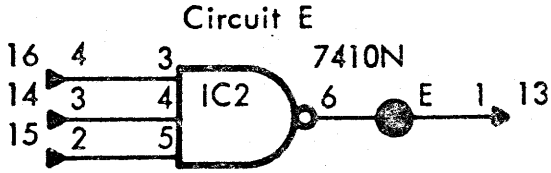
ELECTRICAL CHARACTERISTICS

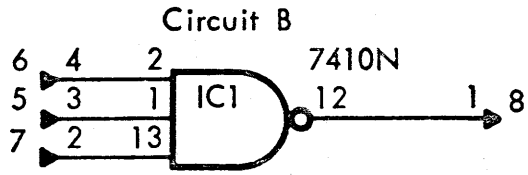
Input loading	1 unit load (each input)
Fan-out	10 unit loads

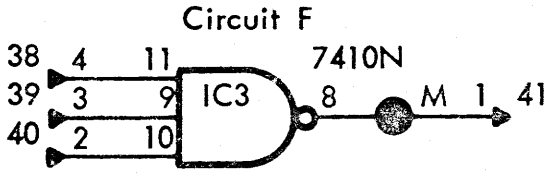
SWITCHING CHARACTERISTICS

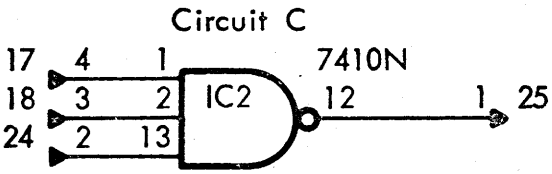
Propagation Time	td(1)	Typ. 18 ns; Max. 29 ns
	td(0)	Typ. 8 ns; Max. 15 ns

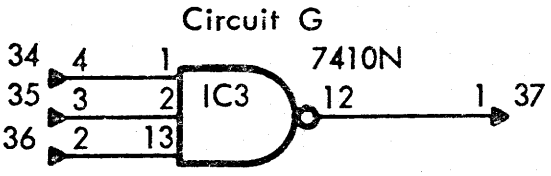


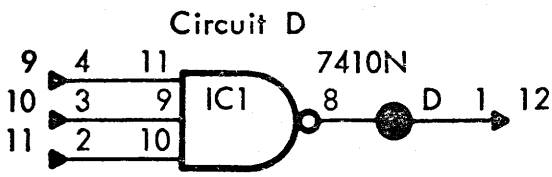


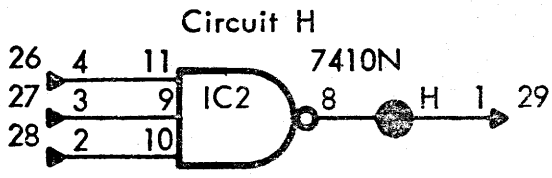


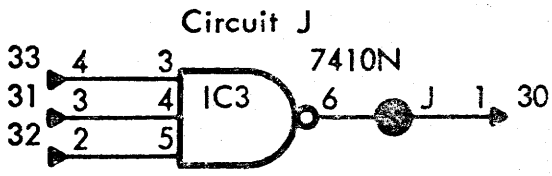


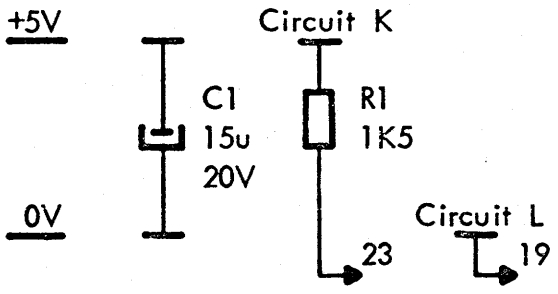




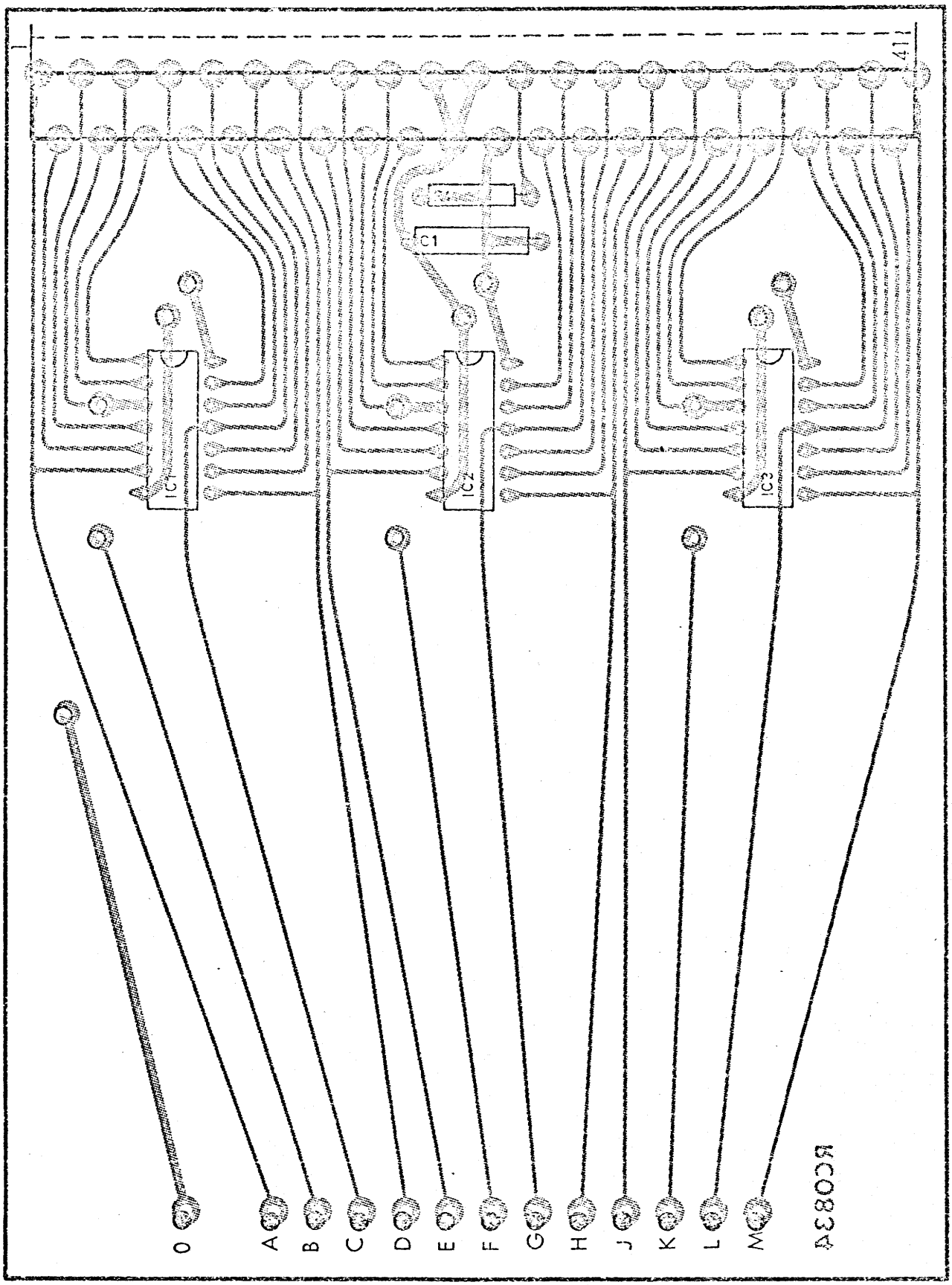






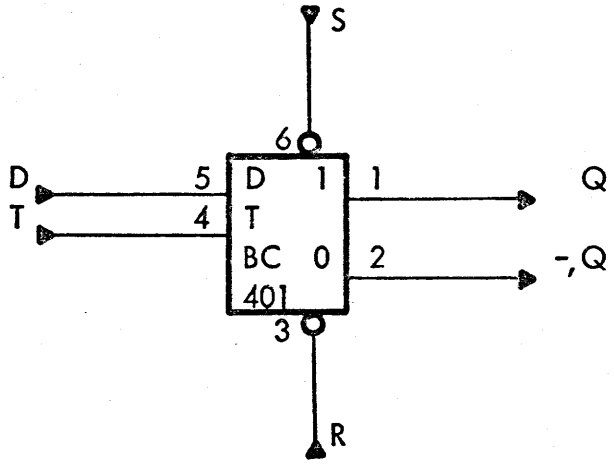


POWER REQUIREMENTS		
0V	pin 21	
+5V	pin 22	30 mA
Power Dissipation		166 mW



040269 BN 290869 KS 031169 JA 031169 PF

BC401



CIRCUIT DESCRIPTION

The BC401 is a bistable element of the D-type with a data-input, a trigger-input, a reset-input, and a set-input.

S- and R-inputs are superior to other inputs and control the outputs Q and -,Q as described below:

S	R	Q	-,Q
0	0	1	1
0	1	1	0
1	0	0	1
1	1	Not under control by S- and R-inputs.	

Any change of Q, when controlled by D- and T-inputs, is initiated at a voltage level of T, when T changes from logical 0 to logical 1, and is not related to the transition time.

The function is described below:

S	R	D	↑Q
1	1	0	0
1	1	1	1

↑Q is the output after the transition of T from 0 to 1

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

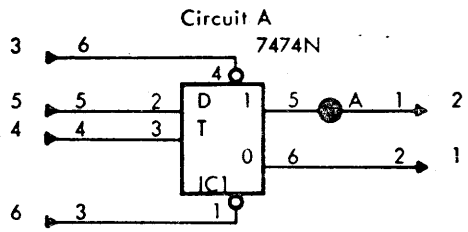
Input Loading	
D, S	1 unit load (each input)
T, R	2 unit loads (each input)
Fan-Out	10 unit loads (each output)

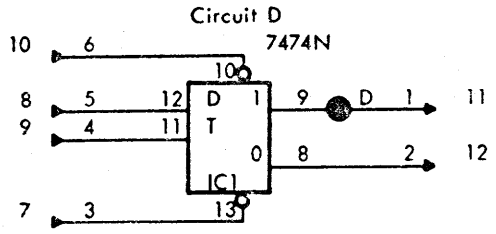
SWITCHING CHARACTERISTICS

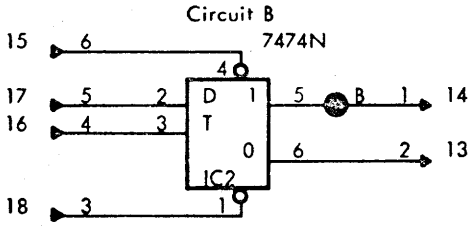
Min. Set-Time 1)		20 nS
Min. Hold-Time 2)		5 nS
Min. trigger pulse width		30 nS
Max. toggle frequency		15 MHz
Propagation Time.		
From trigger to output	td(1)	Min. 10 nS; Typ. 20 nS; Max. 35 nS
	td(0)	Min. 10 nS; Typ. 28 nS; Max. 50 nS
From S- and R-inputs		
to output	td(1)	Max. 25 nS
	td(0)	Max. 40 nS

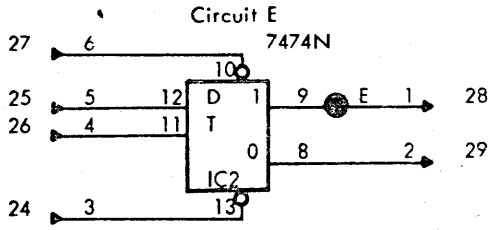
1) To ensure correct storage of data, D-input should be set up for a time $\geq$ Min. Set-Time. During this time D-input should remain stable.

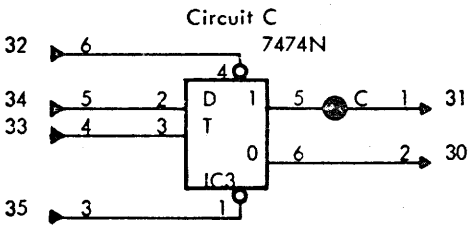
2) To ensure correct storage of data, D-input should remain stable for a time, $\geq$ Min. Hold-Time, after T has passed the threshold value as T changes from logical 0 to logical 1.

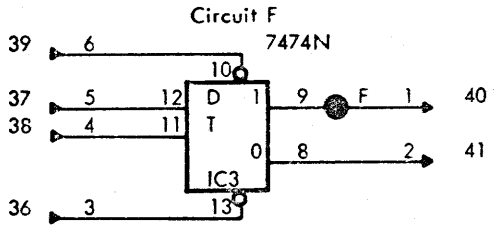


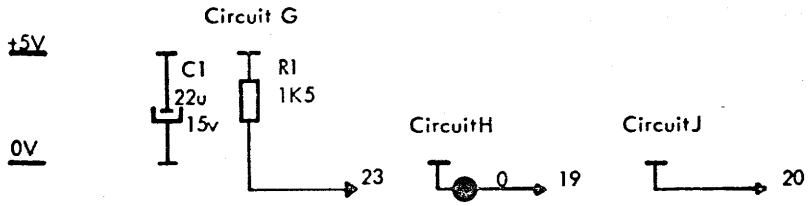






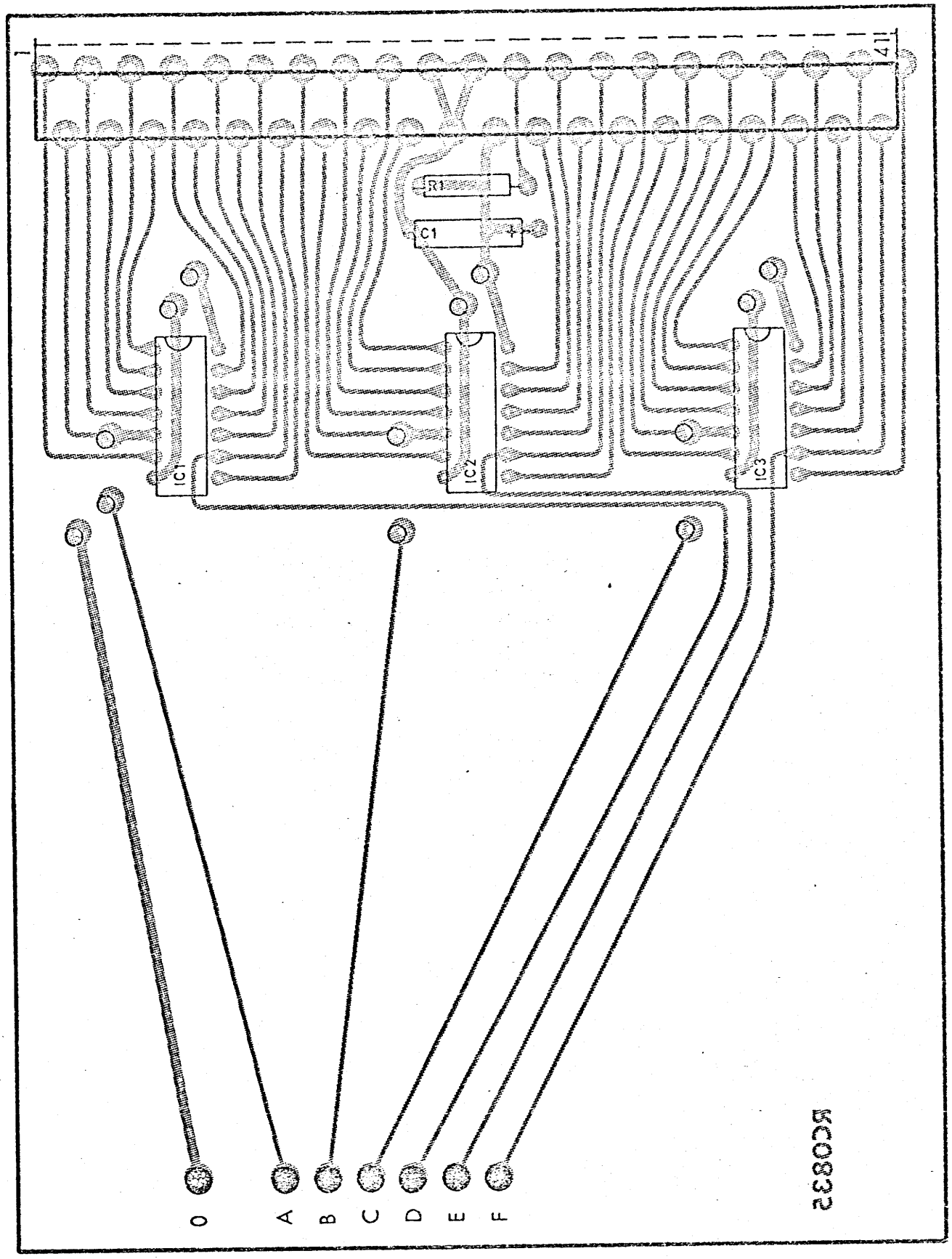






POWER REQUIREMENTS		
+5 V	PIN. 22	57 mA
0 V	PIN. 21	
POWER DISSIPATION: 295 mW		

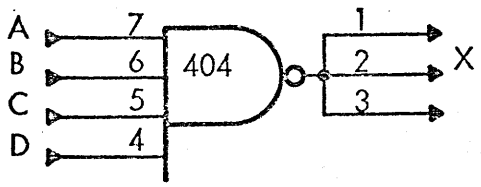
091167 HC 120869 CEM 120869 JA 120869 AAGR



RCLM400 6 BC401 RC0835-1

A20 417 PCB Assembly Drawing

AC404



CIRCUIT DESCRIPTION

The AC404 is a 4-input NAND power element. The element has 3 parallel coupled output terminals, and if possible, the load should be divided equally on the 3 output terminals. The logical operation of the element is:

$$X = -,(A \wedge B \wedge C \wedge D)$$

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

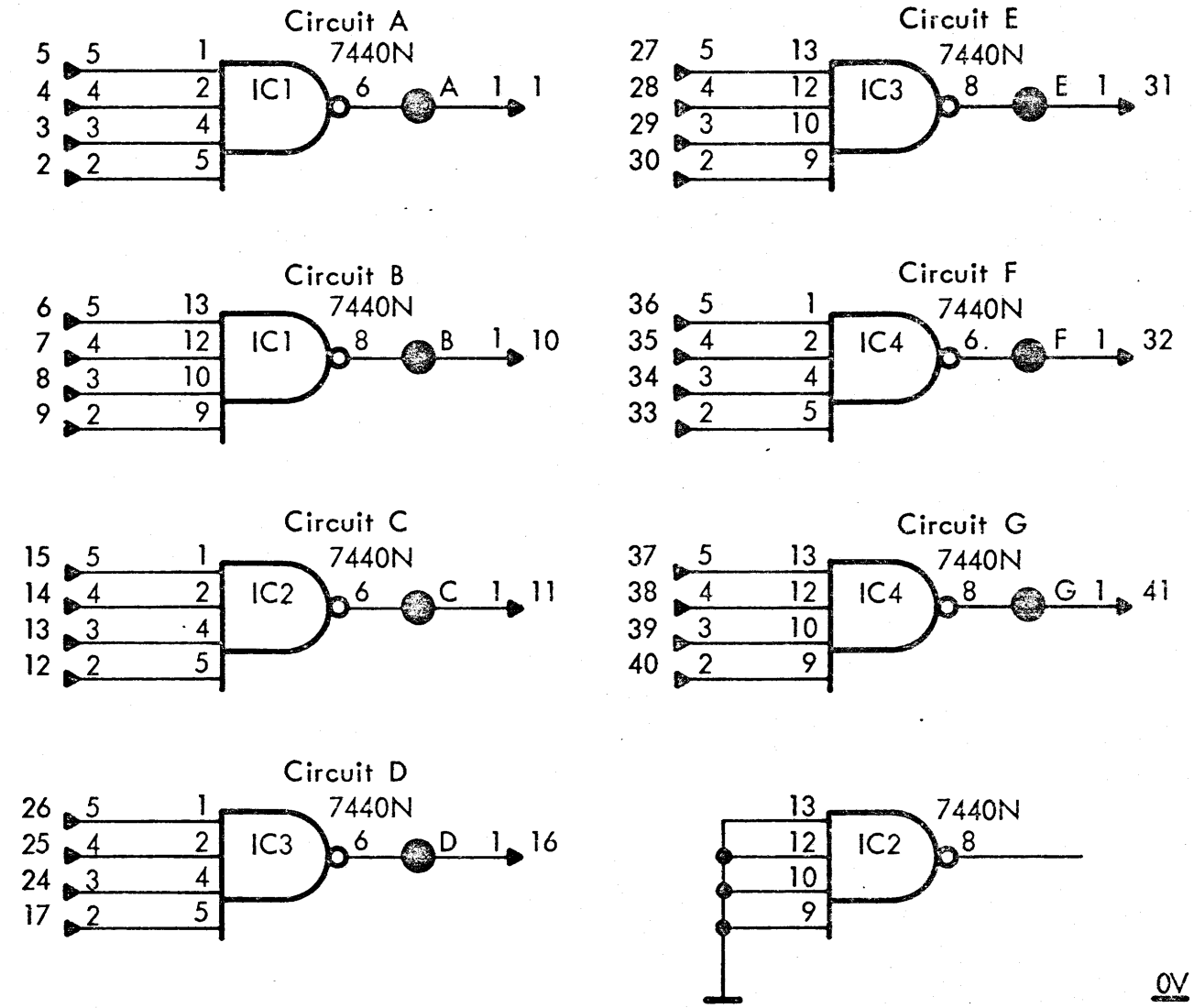
Input Loading	1 unit load (each input)
Fan-Out	30 unit loads

SWITCHING CHARACTERISTICS

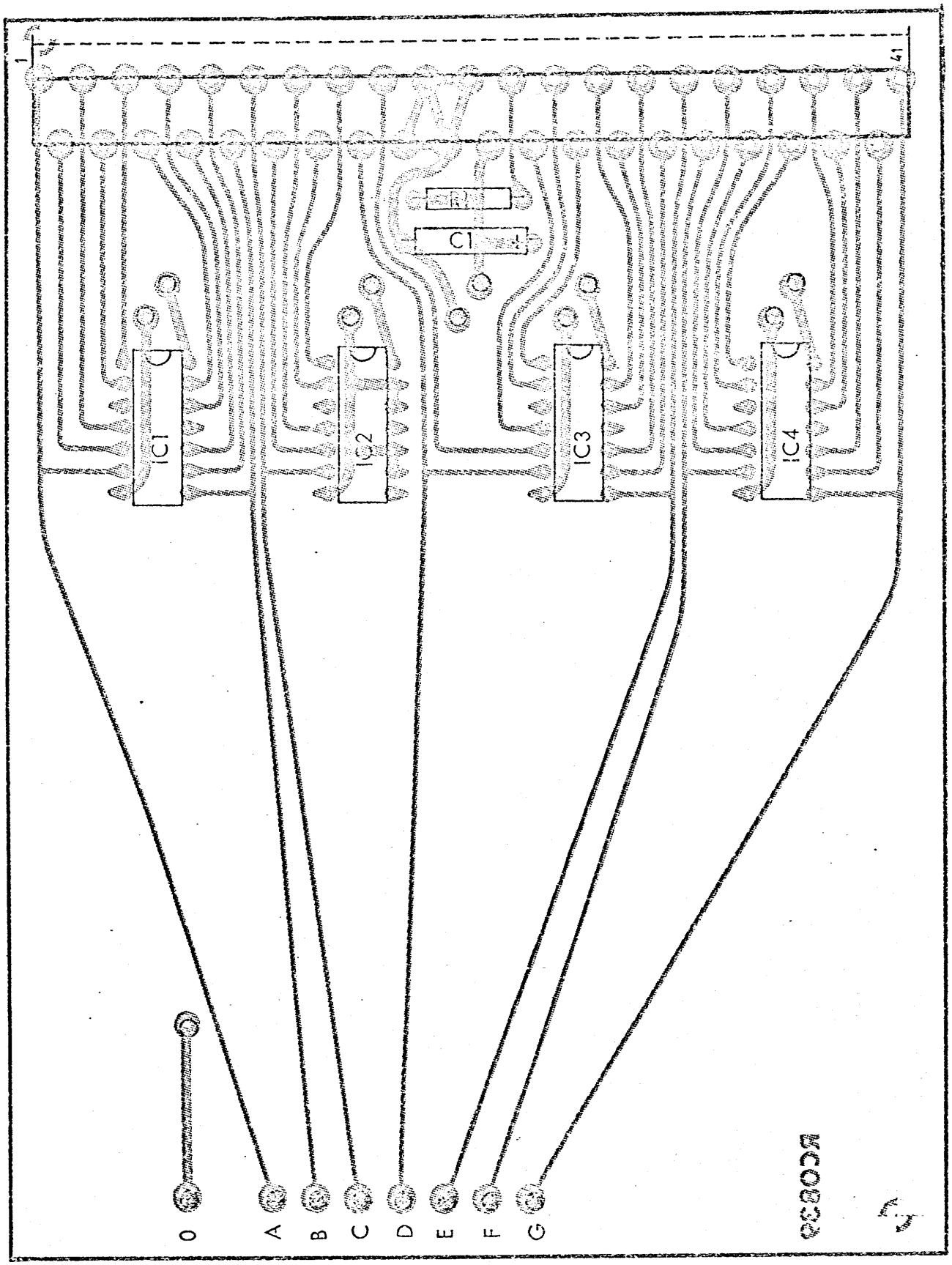
Propagation Delay:	td1	Min. 8 ns; Typ. 18 ns; Max. 29 ns 1)
	td0	Min. 4 ns; Typ. 8 ns; Max. 15 ns 1)

NOTE

1) The indicated values for minimum propagation delay are estimated values for which the manufacturer of the circuits does not guarantee.

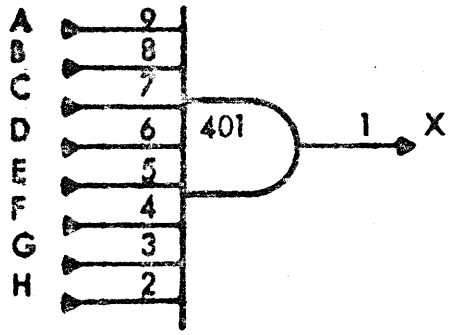


POWER REQUIREMENTS		
0V	pin 21	
+5V	pin 22	77mA
Power Dissipation :		390mW



220469 BN 240869 KS 071069 JA 090170BN

AA 401



CIRCUIT DESCRIPTION

The AA 401 is an 8-input AND element. The logical operation of the element is:

$$X = A\ B\ C\ D\ E\ F\ G\ H$$

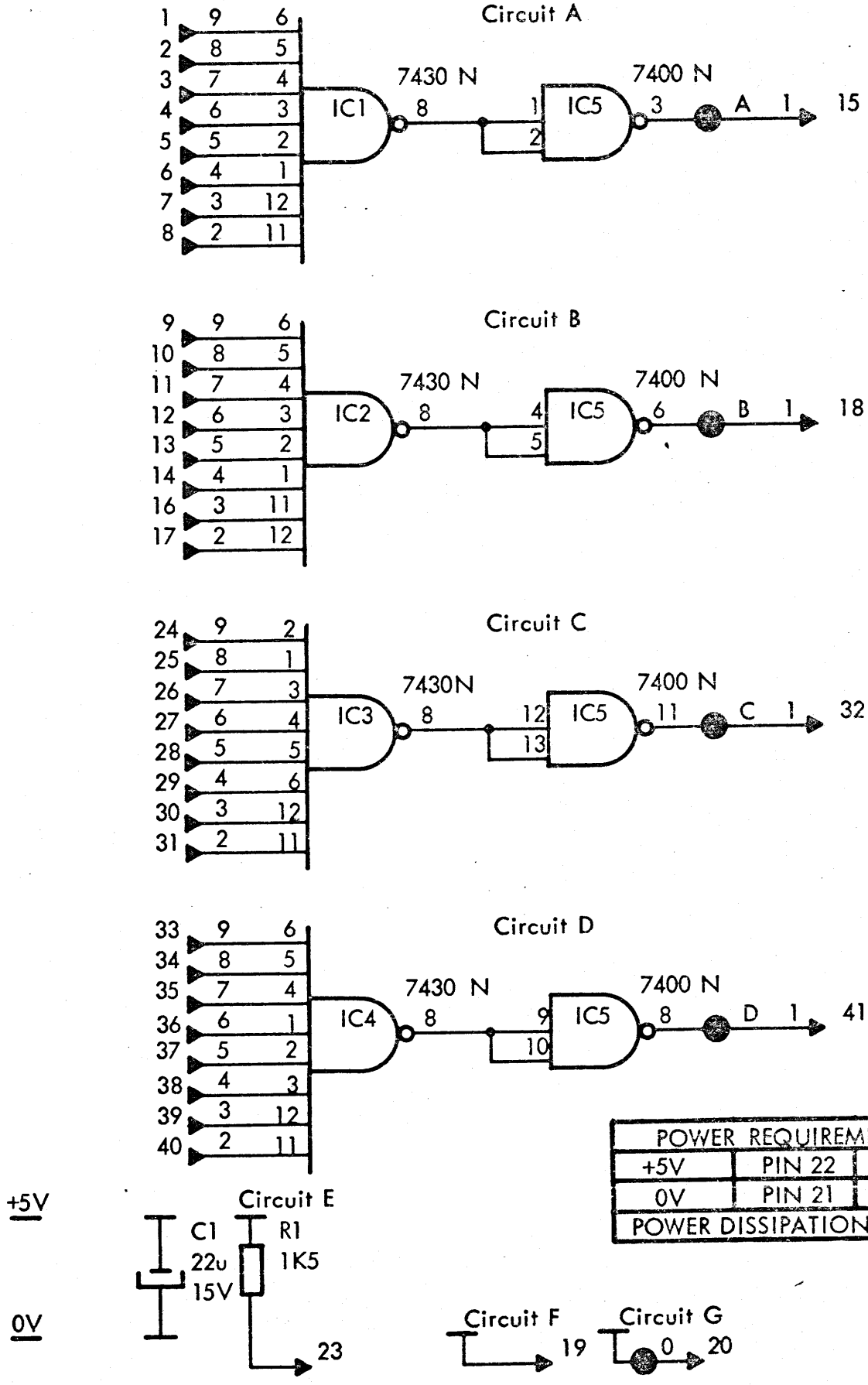
SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

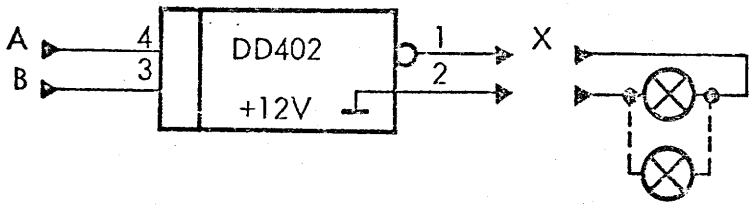
Input Loading	1 unit load (each input)
Fan - Out	10 unit loads

SWITCHING CHARACTERISTICS

Propagation Delay : td	Min. ns; Typ. 26 ns; Max. 44 ns.


Circuit A
1 9 6
2 8 5
3 7 4
4 6 3
5 5 2
6 4 1
7 3 12
8 2 11
IC1
7430 N
8
1
2
IC5
7400 N
3
A
1
15
Circuit B
9 9 6
10 8 5
11 7 4
12 6 3
13 5 2
14 4 1
16 3 11
17 2 12
IC2
7430 N
8
4
5
IC5
7400 N
6
B
1
18
Circuit C
24 9 2
25 8 1
26 7 3
27 6 4
28 5 5
29 4 6
30 3 12
31 2 11
IC3
7430N
8
12
13
IC5
7400 N
11
C
1
32
Circuit D
33 9 6
34 8 5
35 7 4
36 6 1
37 5 2
38 4 3
39 3 12
40 2 11
IC4
7430 N
8
9
10
IC5
7400 N
8
D
1
41
POWER REQUIREMENTS
+5V PIN 22 18mA
0V PIN 21
POWER DISSIPATION 95 mW
+5V
0V
Circuit E
C1
22u
15V
R1
1K5
23
Circuit F
19
Circuit G
0
20

DD402



CIRCUIT DESCRIPTION

The DD402 is a lamp driver for incandescent lamps, type CM330, 14 V, 80 mA or equivalent.

The logical operation of the circuit is: $X = -,(A \wedge B)$. I.e. the lamp will be lit when A and B are 1.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

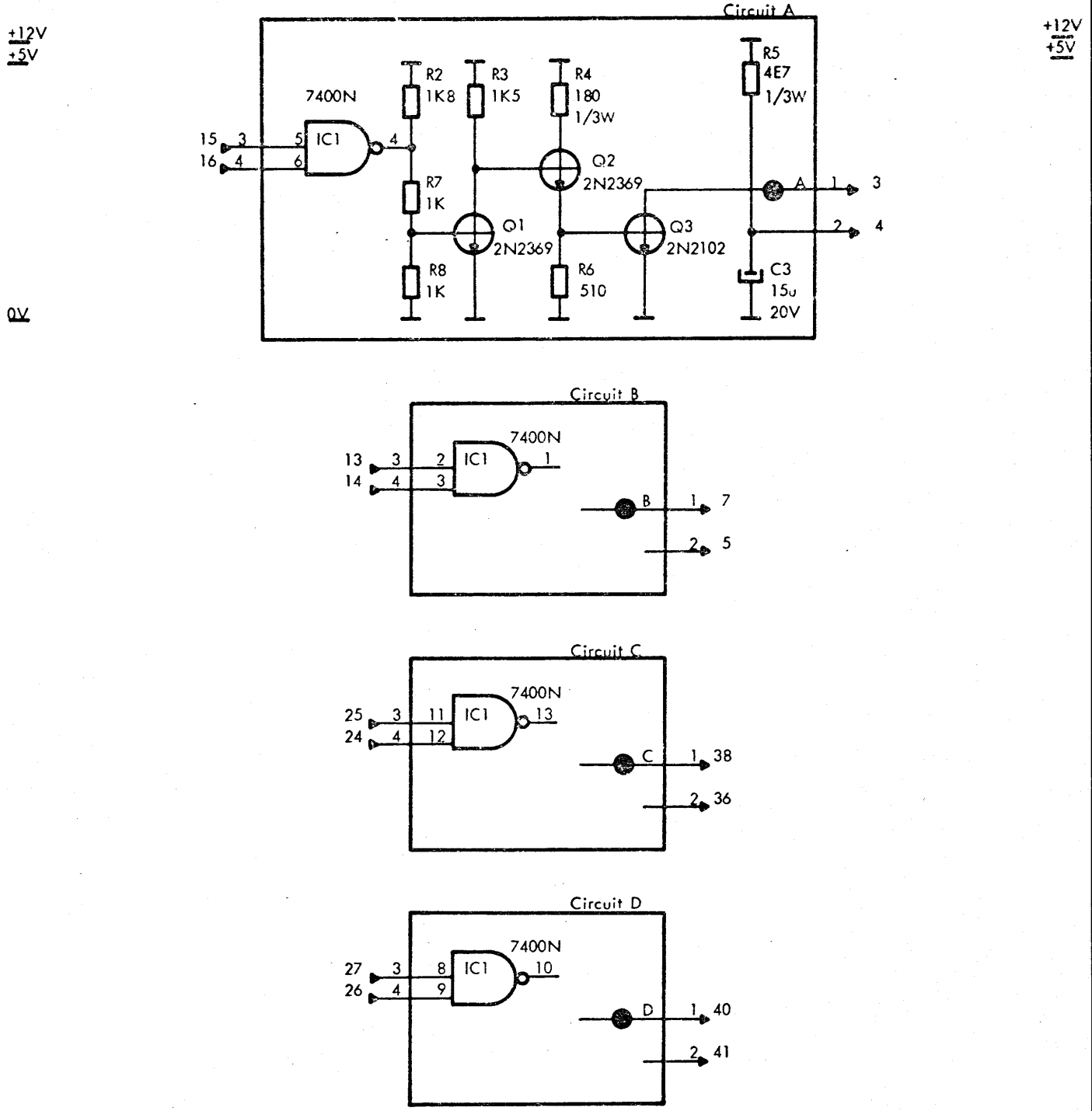
Input Loading	1 unit load
Output Drive Capability	Max. two CM330, 14 V, 80 mA or equivalent connected in parallel.
Max. Output Load Current	150 mA

SWITCHING CHARACTERISTICS

Min. Duration of On-Time	1)	10 us
Min. Duration of Off-Time		40 us

NOTE

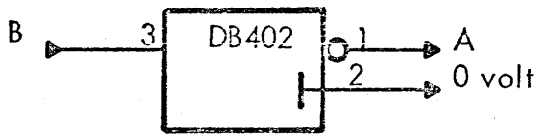
1) On-time is the time the output is 0.



POWER REQUIREMENTS		
+12V	PIN 1	65mA / LAMP
+ 5V	PIN 22	132mA
0V	PIN 21	
POWER DISSIPATION 695mW		

Lamp type: CM 330, 14V/80 mA or equivalent

DB402



The DB402 is a cable driver for up to 5 m cable with max. 1.25 ohms in the loop. The driver is equipped with two terminals for twisted pairs.
The operation is as follows:

$$A = -,B$$

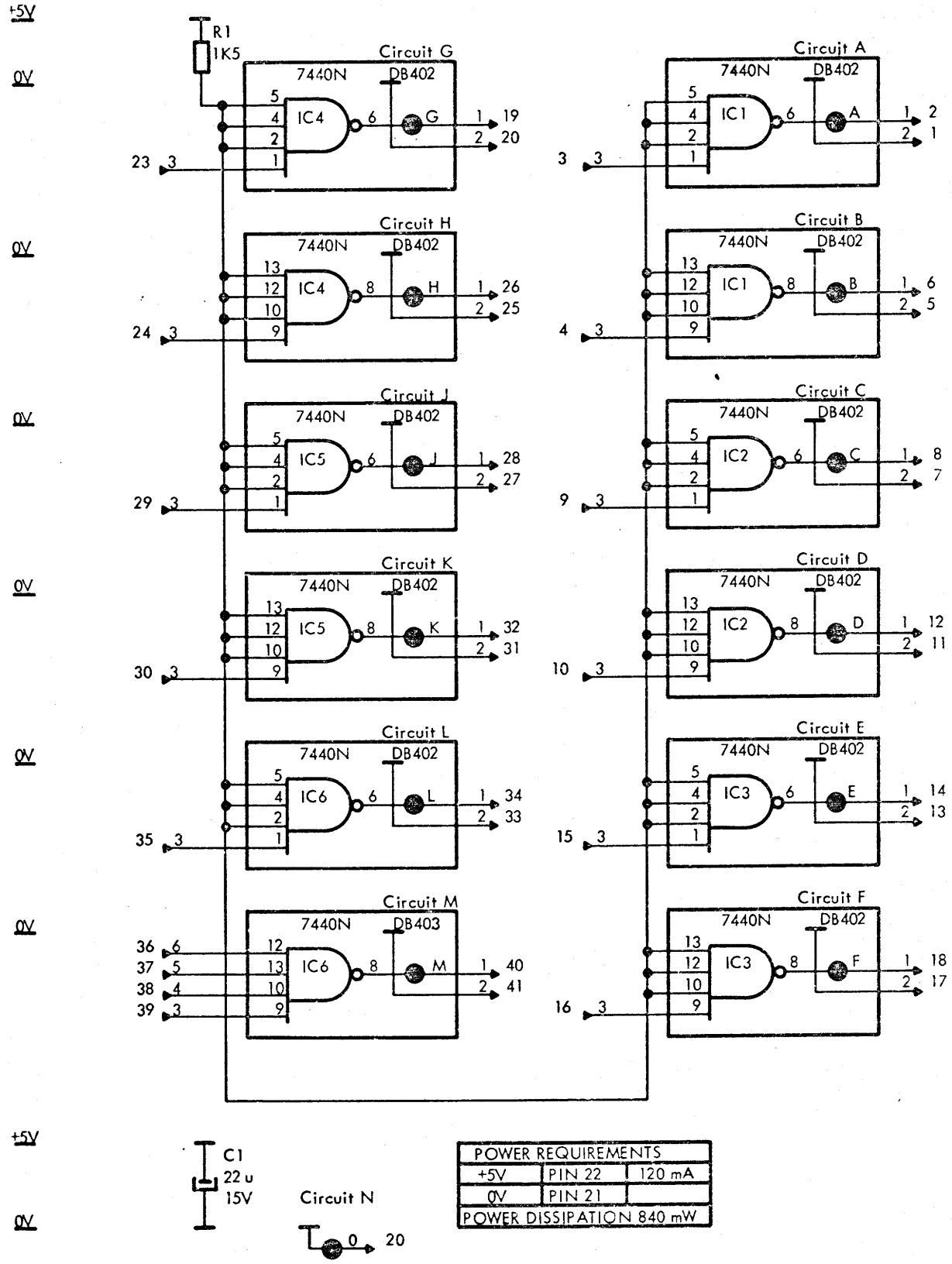
SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

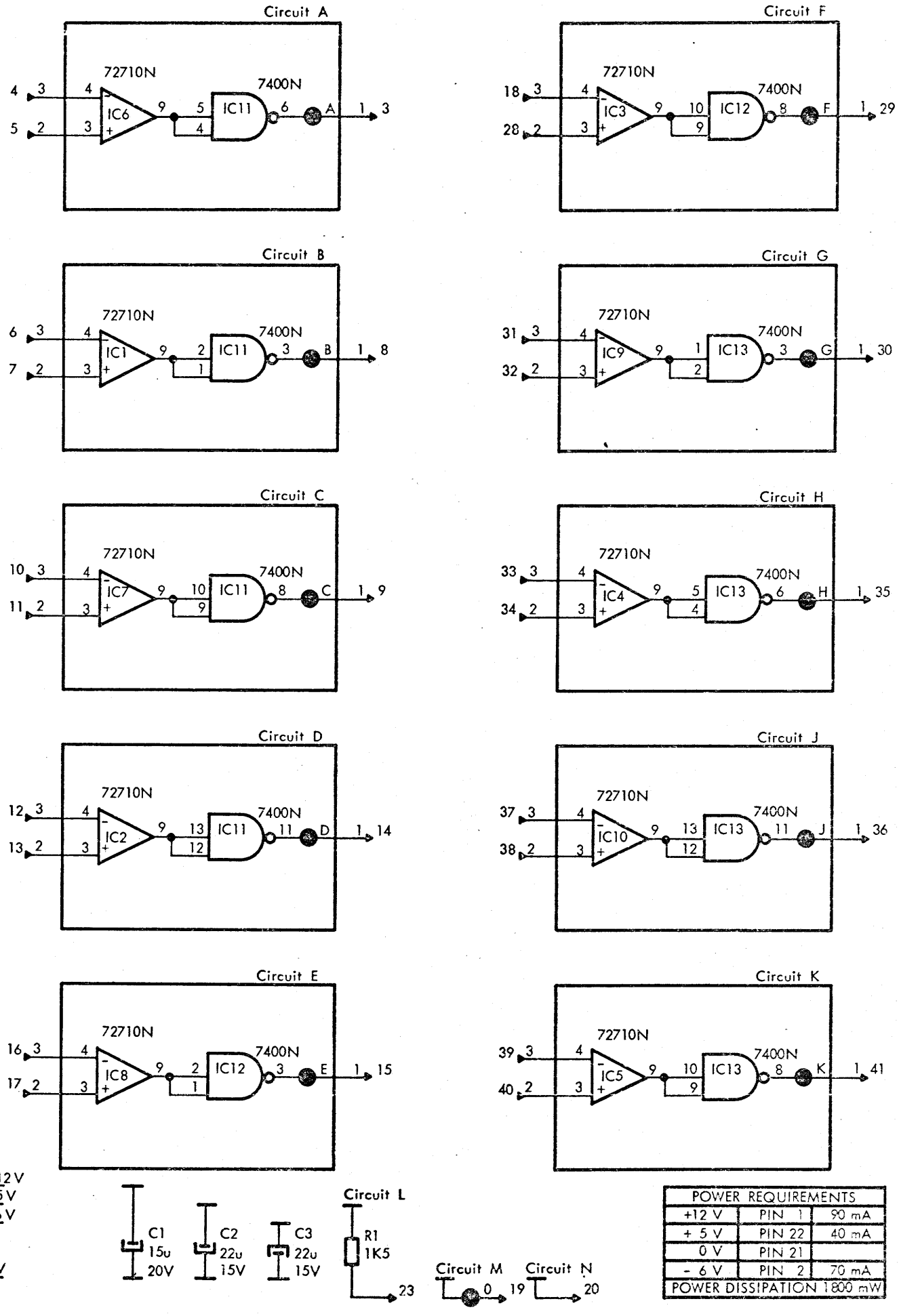
Input and output levels	RCLM400
Fan-In	1 unit load
Fan-Out	30 unit loads

SWITCHING CHARACTERISTICS

td1	Typ. 18 ns; Max. 29 ns
td0	Typ. 8 ns; Max. 15 ns



POWER REQUIREMENTS		
+5V	PIN 22	120 mA
0V	PIN 21	
POWER DISSIPATION 840 mW		



POWER REQUIREMENTS		
+12 V	PIN 1	90 mA
+ 5 V	PIN 22	40 mA
0 V	PIN 21	
- 6 V	PIN 2	70 mA
POWER DISSIPATION 1800 mW		

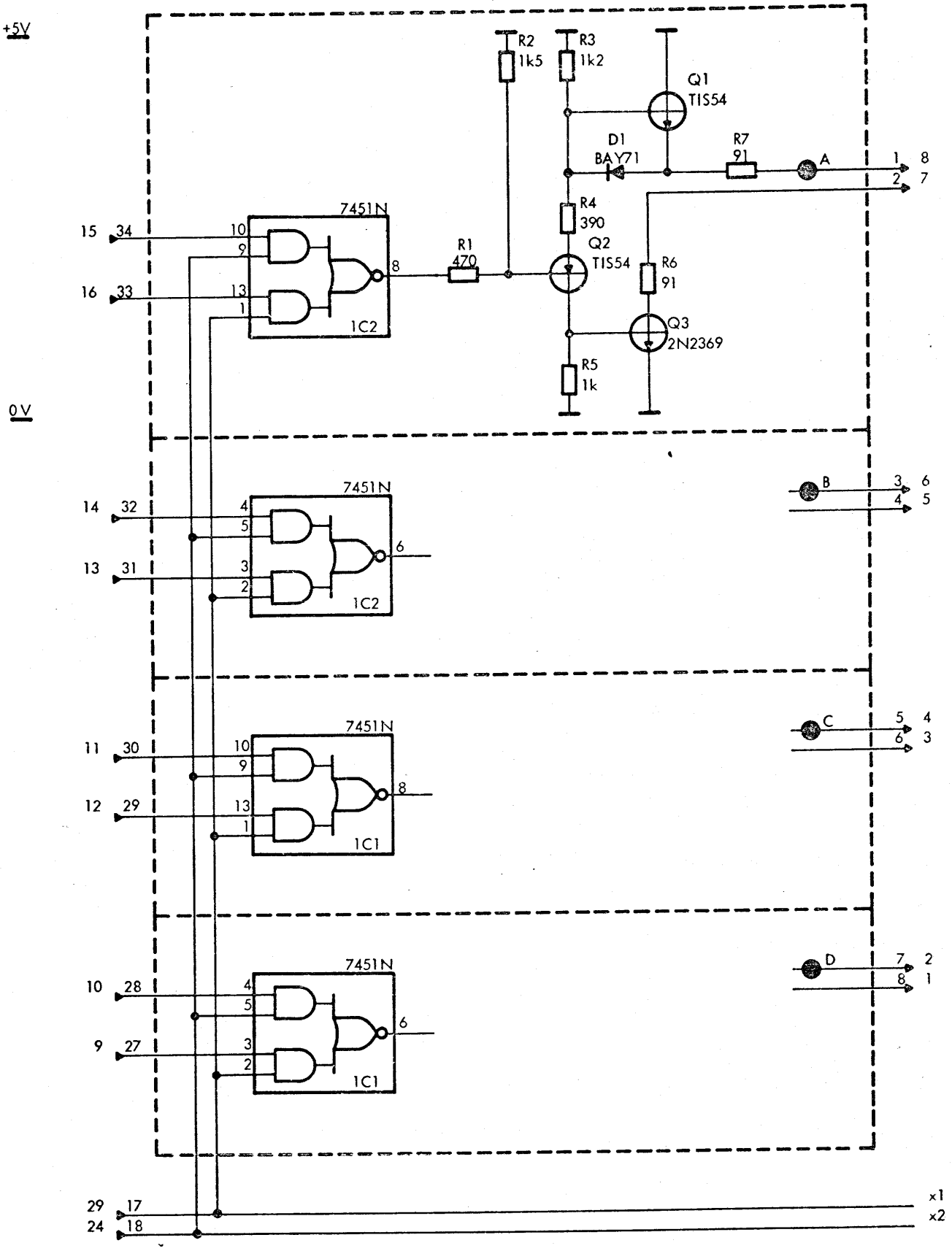
030568 PEP 260869 HA 250970 PE.P V12836

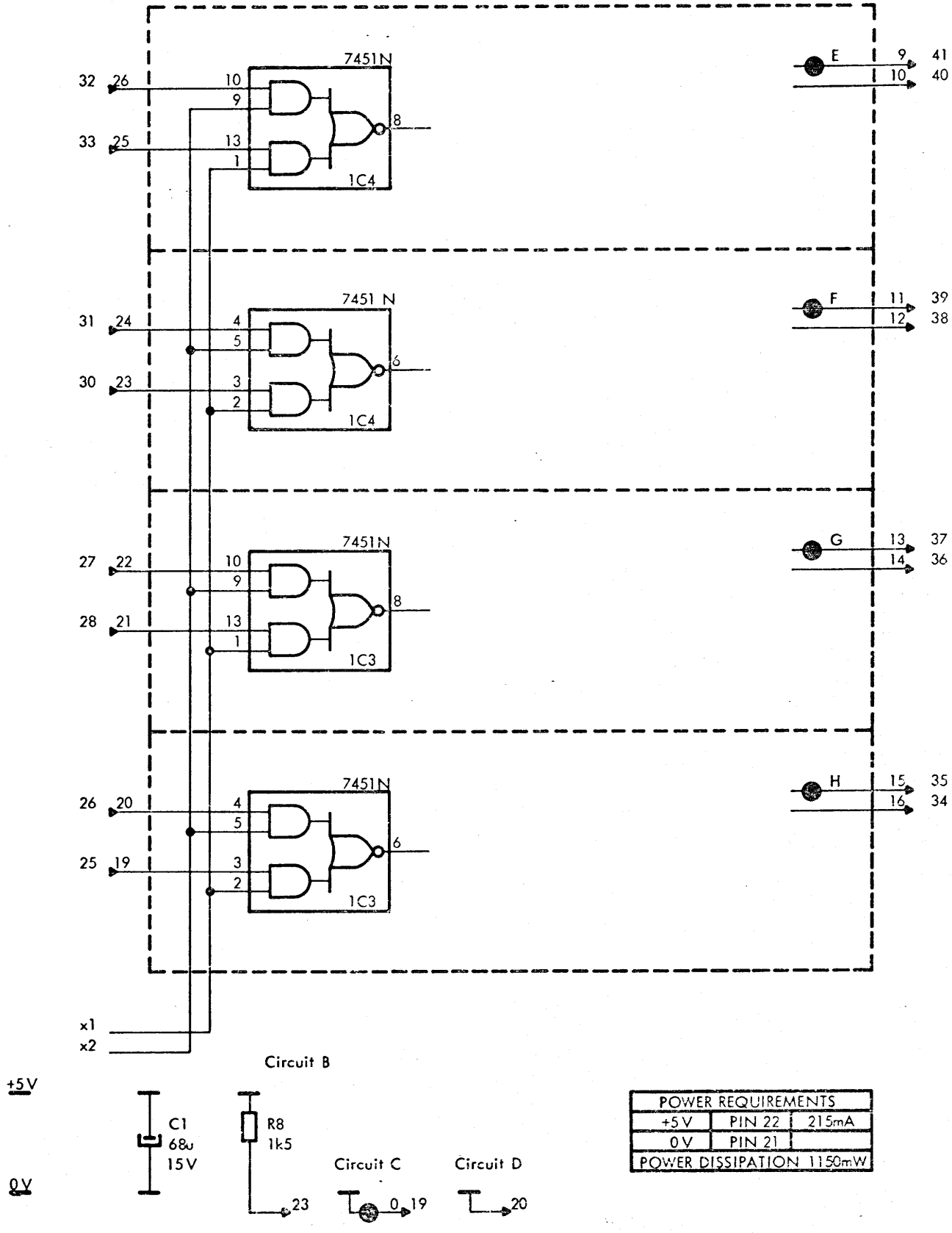
RCLM400 10 DC 405 RC0897-1

V13439

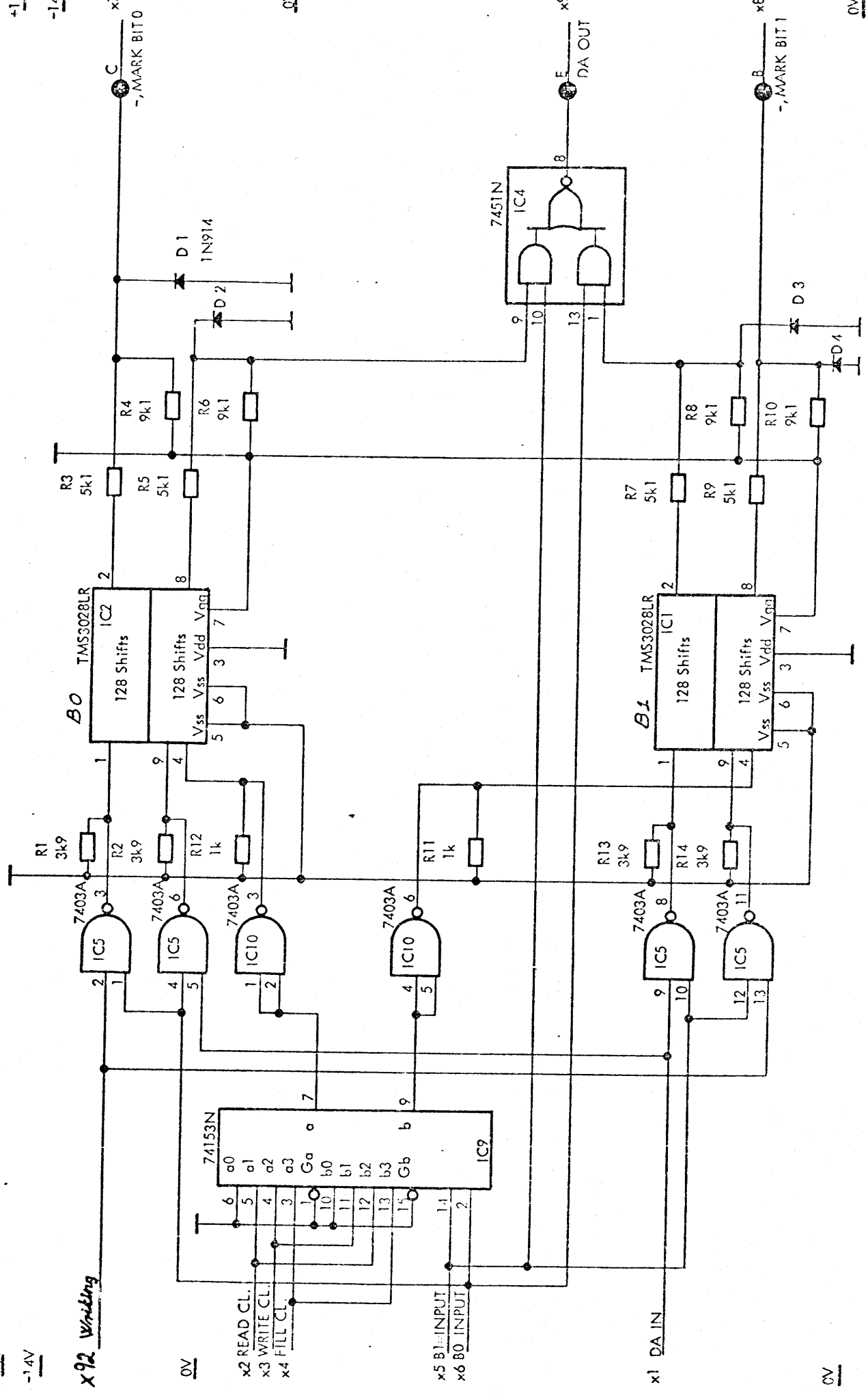
PCBA Circuit Diagram

Circuit A


+5V
0V
R2
1k5
R3
1k2
Q1
TIS54
D1
BAY71
R7
91
A
1
8
2
7
R4
390
Q2
TIS54
R6
91
Q3
2N2369
R5
1k
R1
470
7451N
15
34
16
33
10
9
13
1
8
1C2
14
32
13
31
4
5
3
2
6
1C2
B
3
6
4
5
11
30
12
29
10
9
13
1
8
1C1
C
5
4
6
3
10
28
9
27
4
5
3
2
6
1C1
D
7
2
8
1
29
24
17
18
x1
x2



POWER REQUIREMENTS		
+5 V	PIN 22	215mA
0 V	PIN 21	
POWER DISSIPATION 1150mW		



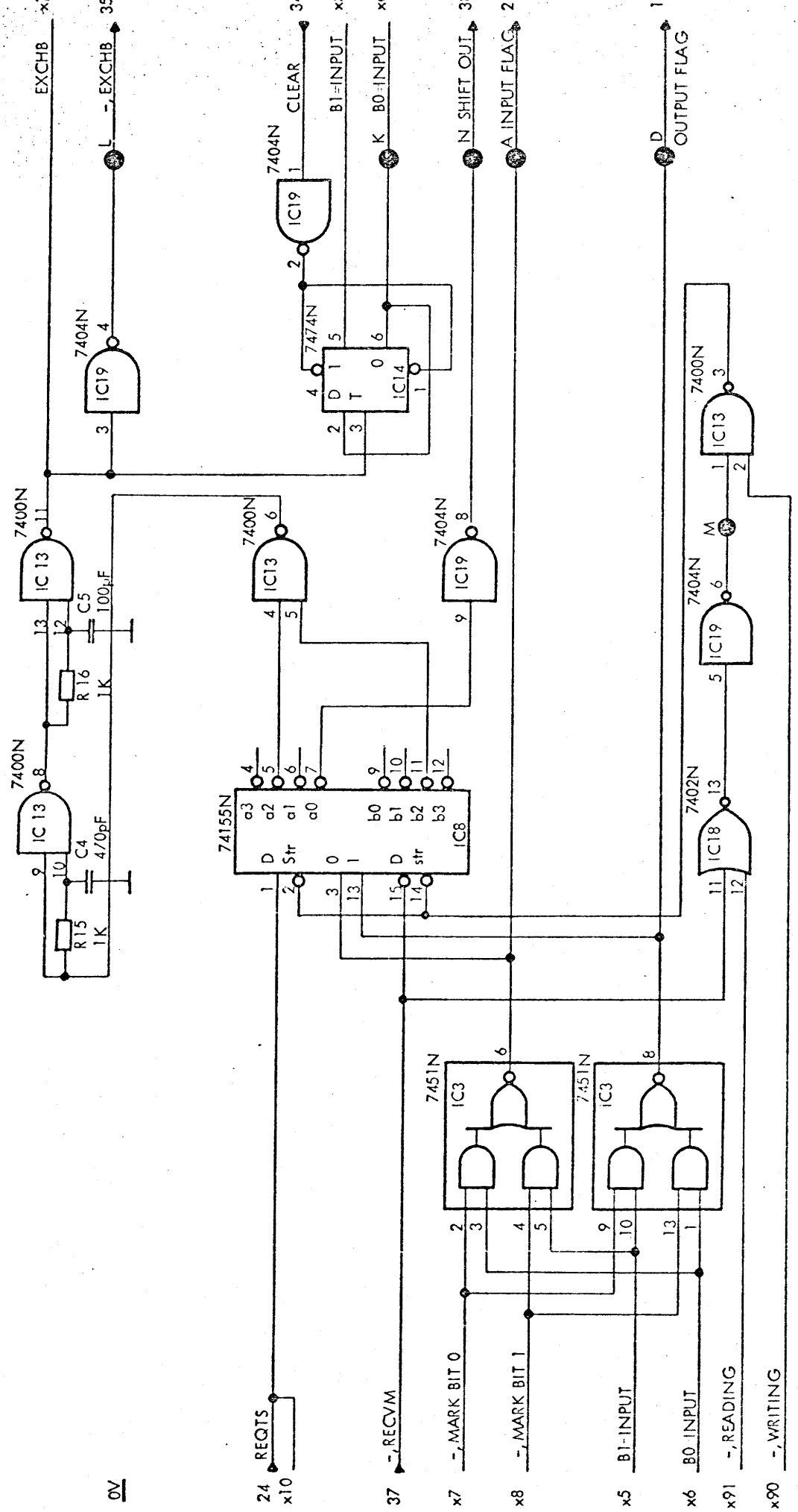
MSTC BUFFER CARD BUFFER

PCBA Circuit Diagram

V23432

RC 2064-1

p 1 of 4

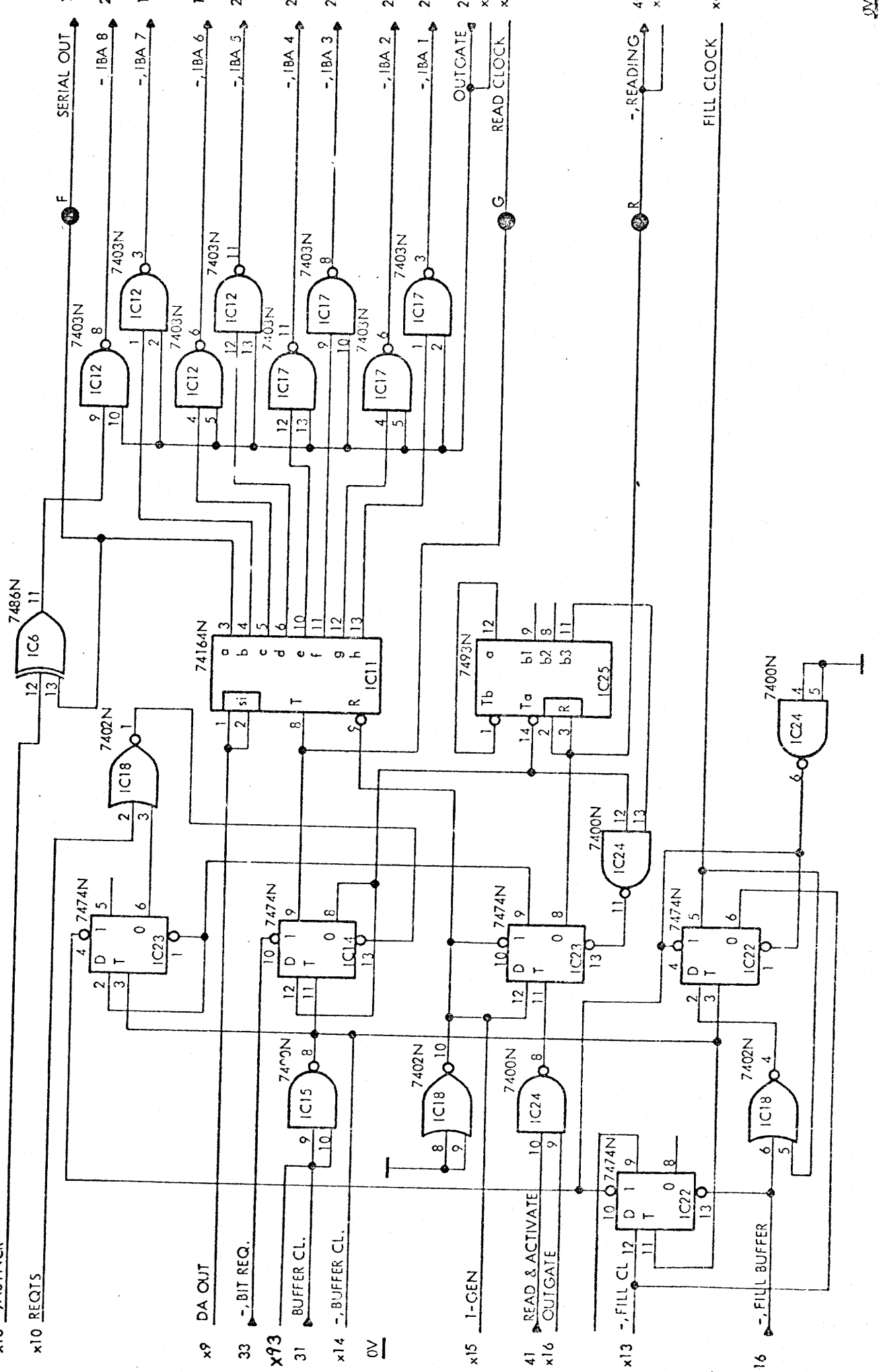


MSTC BUFFER CARD BUFFER EXCHANGE CONTROL

PCBA Circuit Diagram

V23433

RC.2064-1
p 2 of 4



MSTC BUFFER CARD OUTPUT CONTROL

PCBA Circuit Diagram

V23434

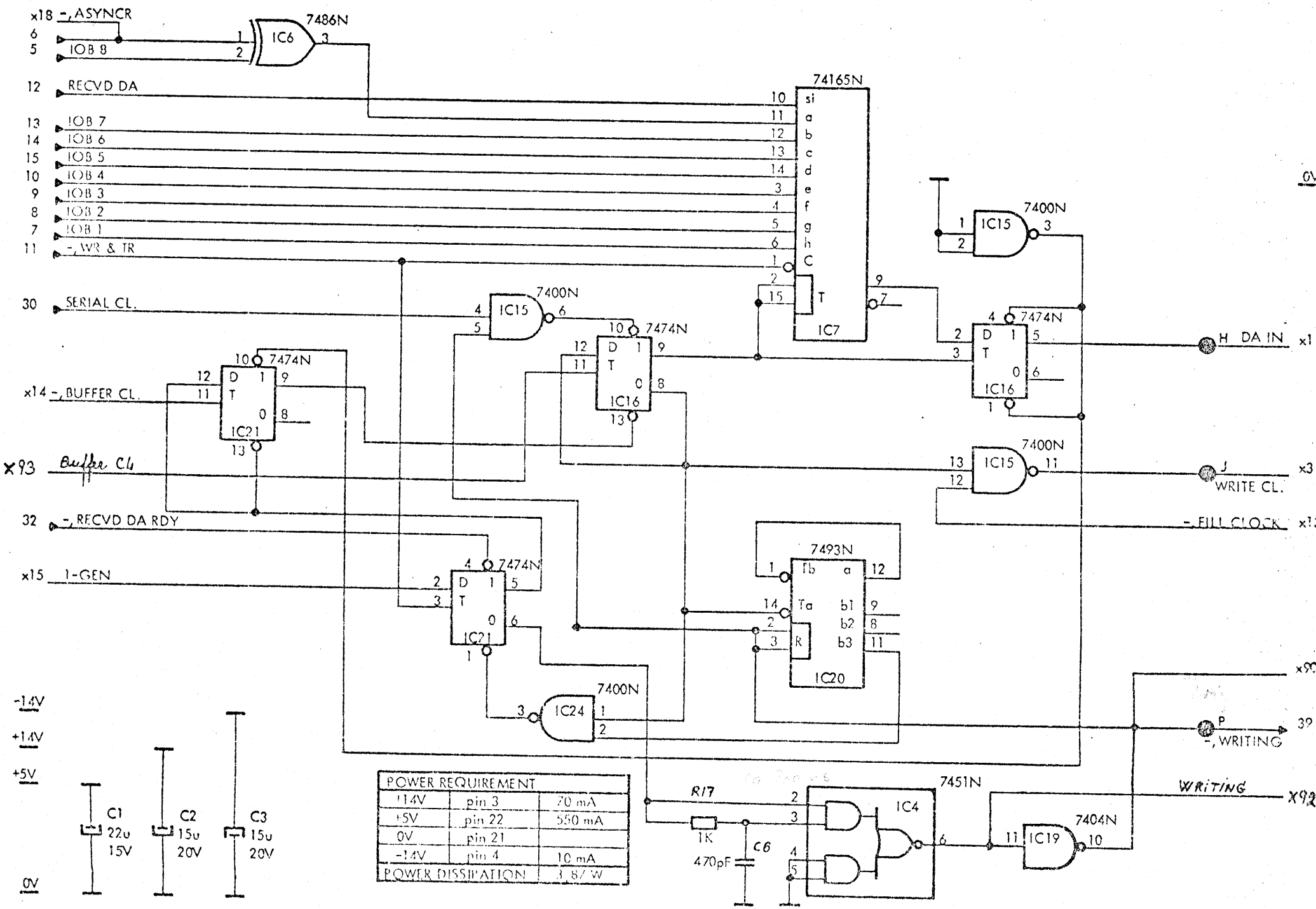
RC2064-1

p 3 of 4

V23435

MSTC BUFFER CARD INPUT CONTROL

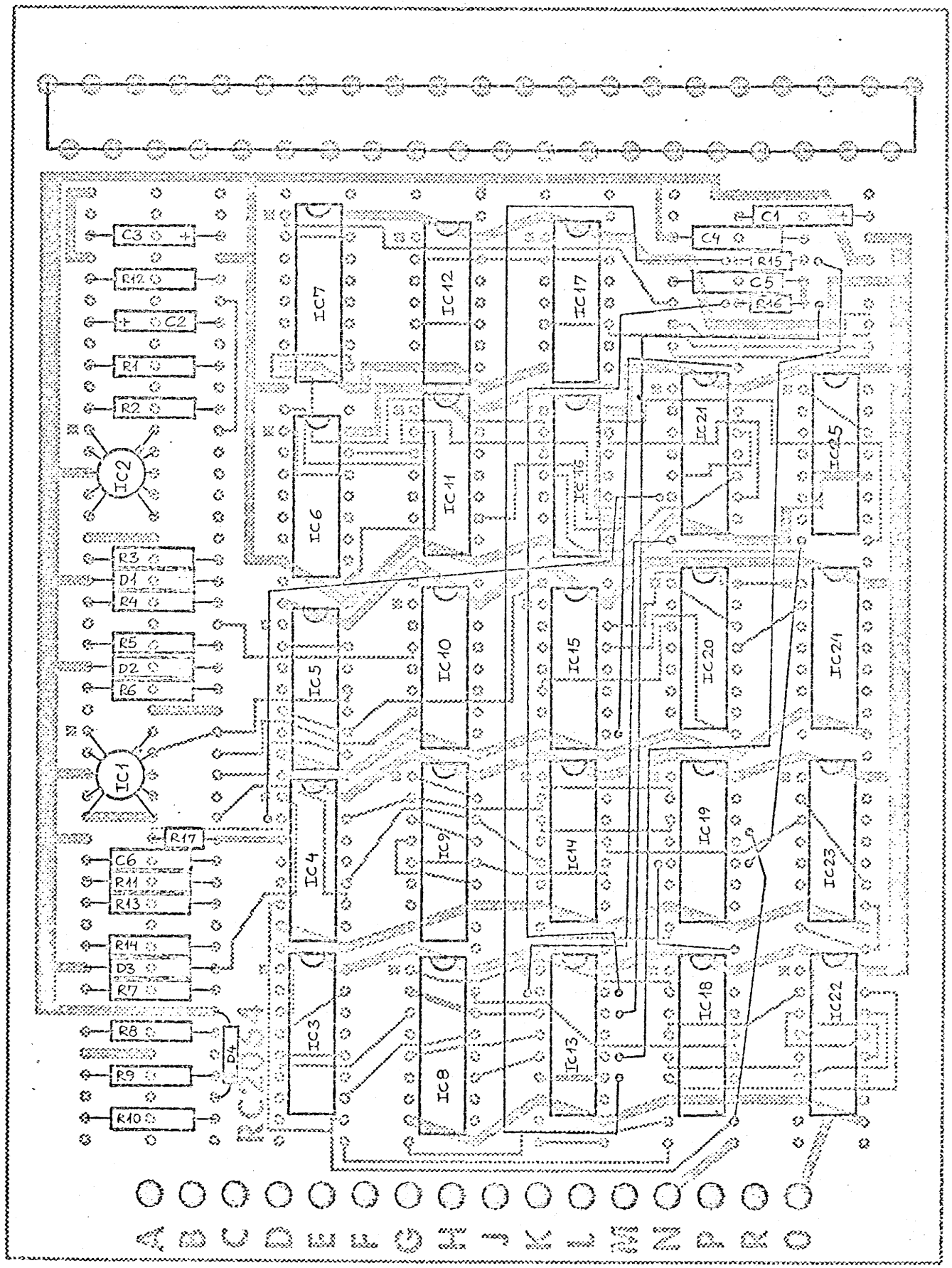
PCBA Circuit Diagram



POWER REQUIREMENT		
-14V	pin 3	70 mA
+5V	pin 22	550 mA
0V	pin 21	
+14V	pin 4	10 mA
POWER DISSIPATION		3.8 W

RC2064-1

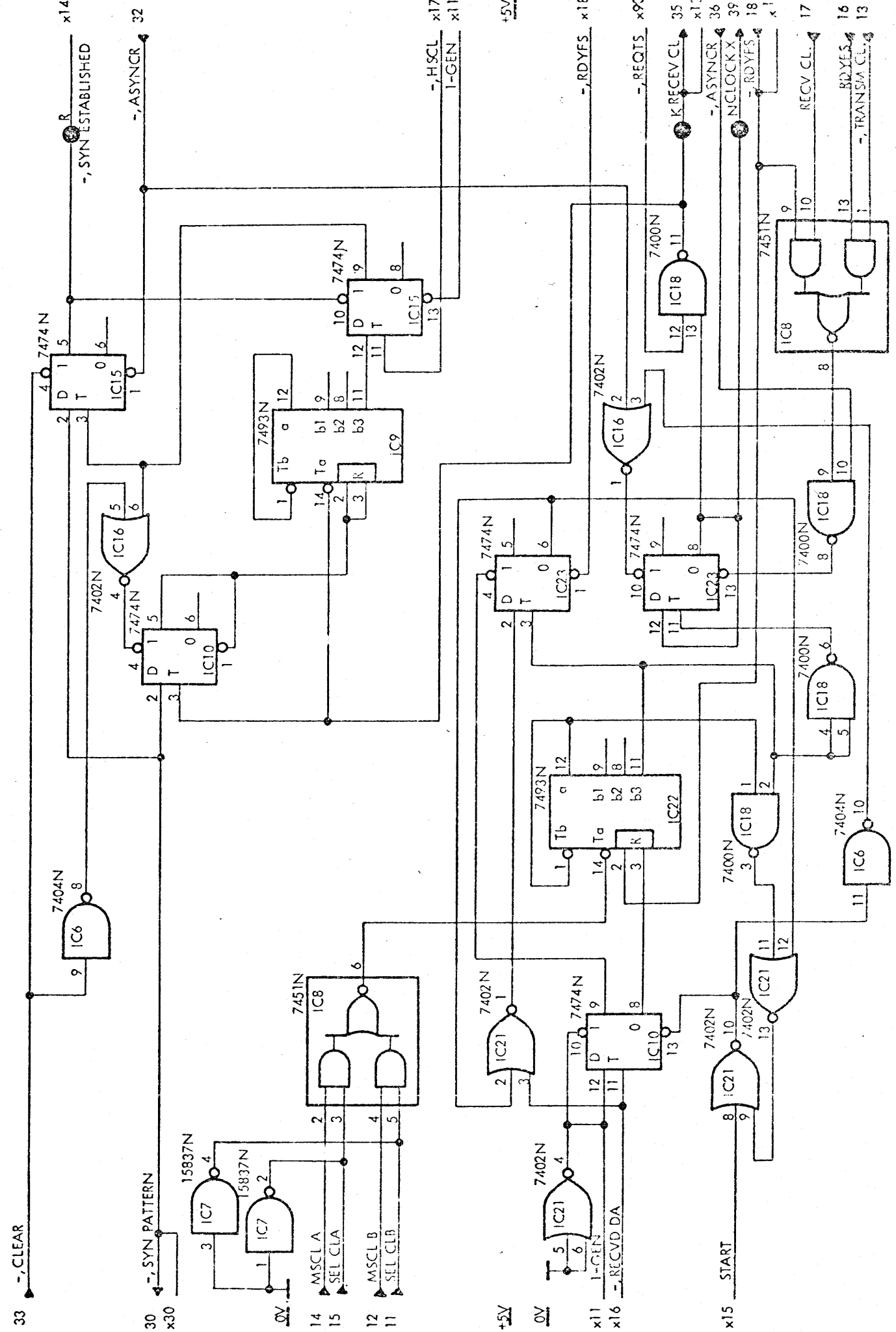
p 4 of 4



RC 2064 -1

V23383

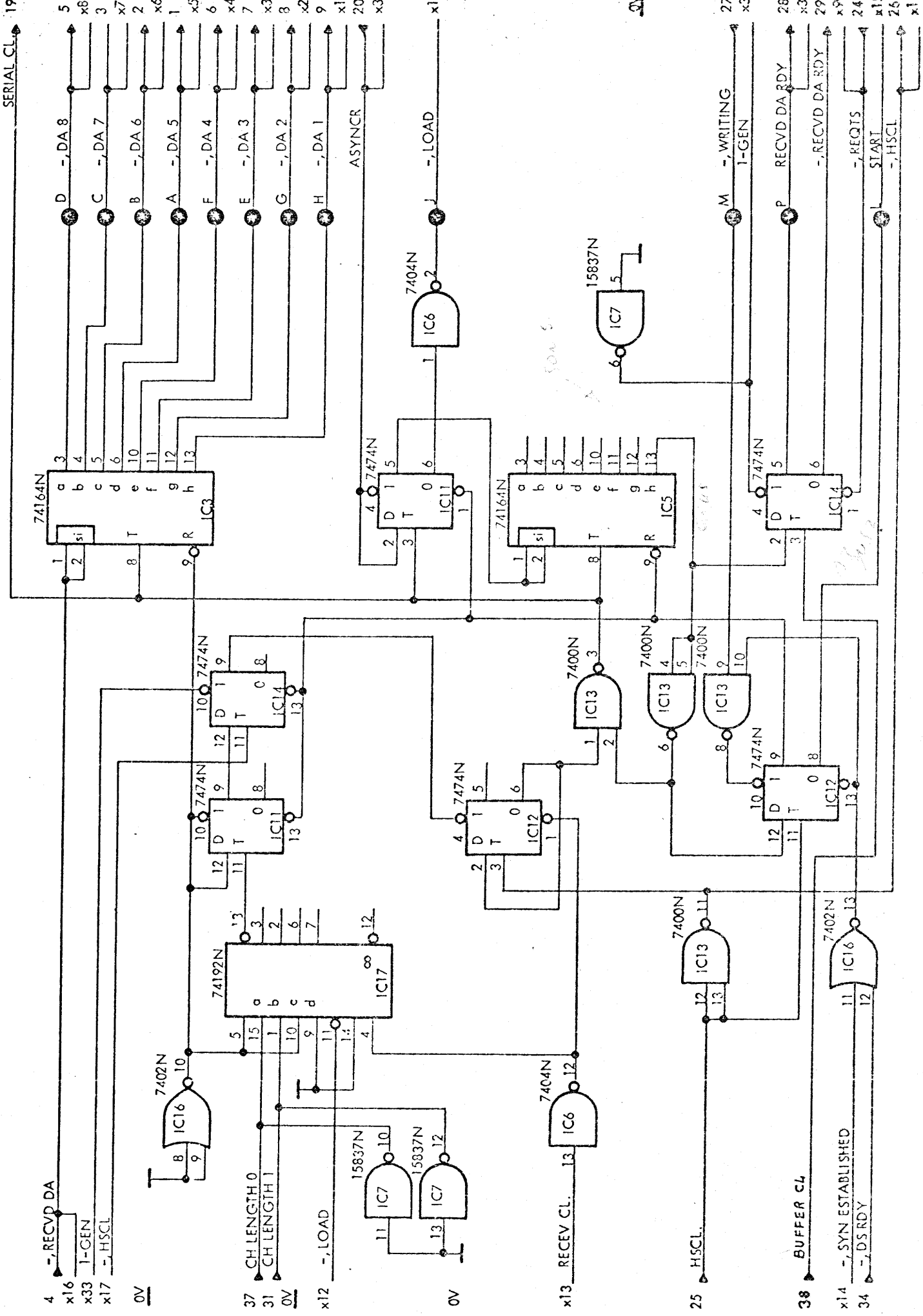
PCB Assembly Drawing



CIRCUITS FOR BIT SYNCRONIZATION AND CHARACTER SYNCRONIZATION
RECEIVER UNIT
PCBA Circuit Diagram

V23437

RC 2065-1
p 1 of 3



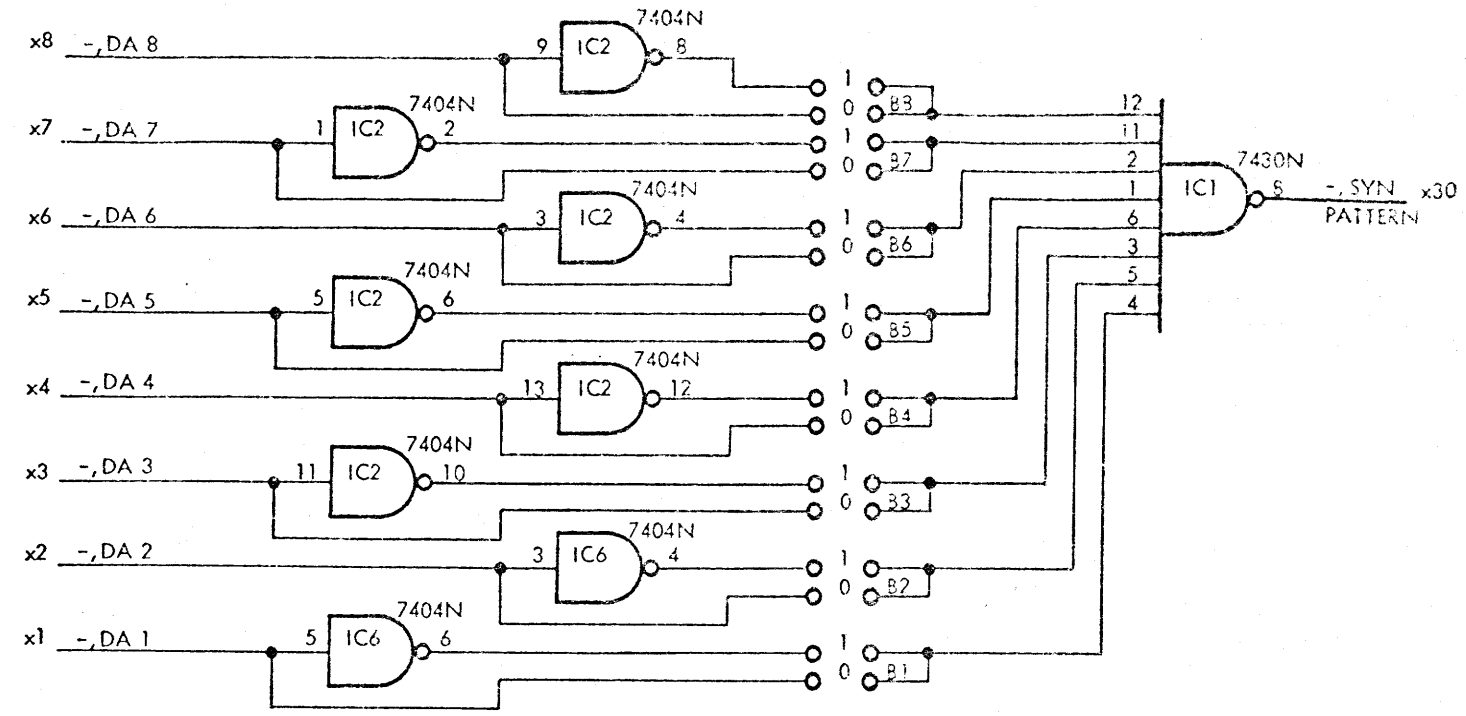
RECEIVER UNIT

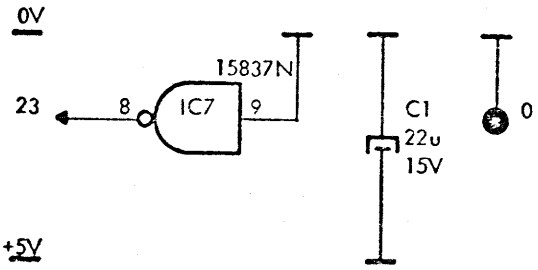
PCBA Circuit Diagram

V23438

RC 2065-1

p 2 of 3





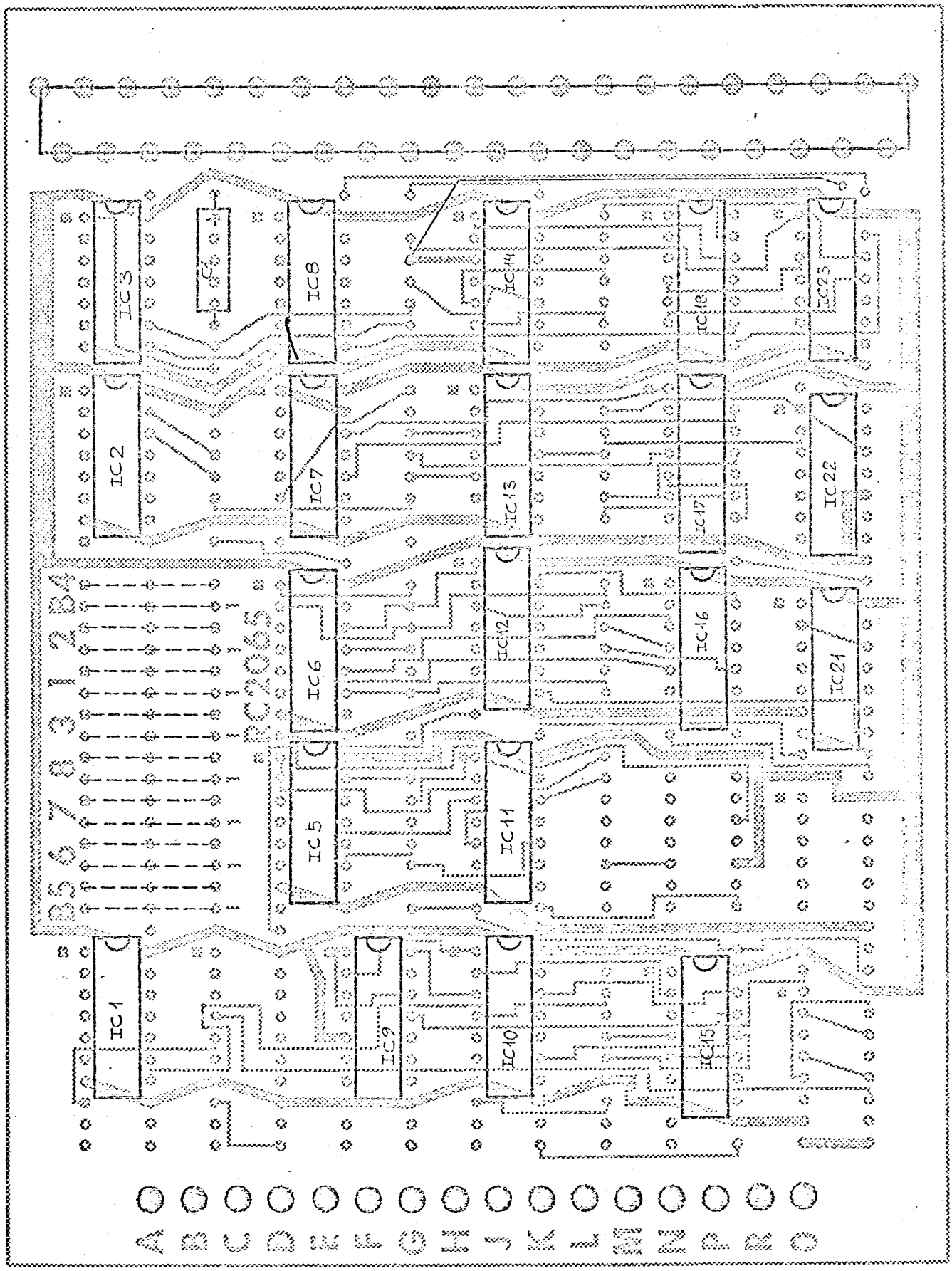
POWER REQUIREMENT		
+5V	pin 22	620 mA
0V	pin 21	
POWER DISSIPATION		3.10 W

RECEIVER UNIT

PCBA Circuit Diagram

V 23439

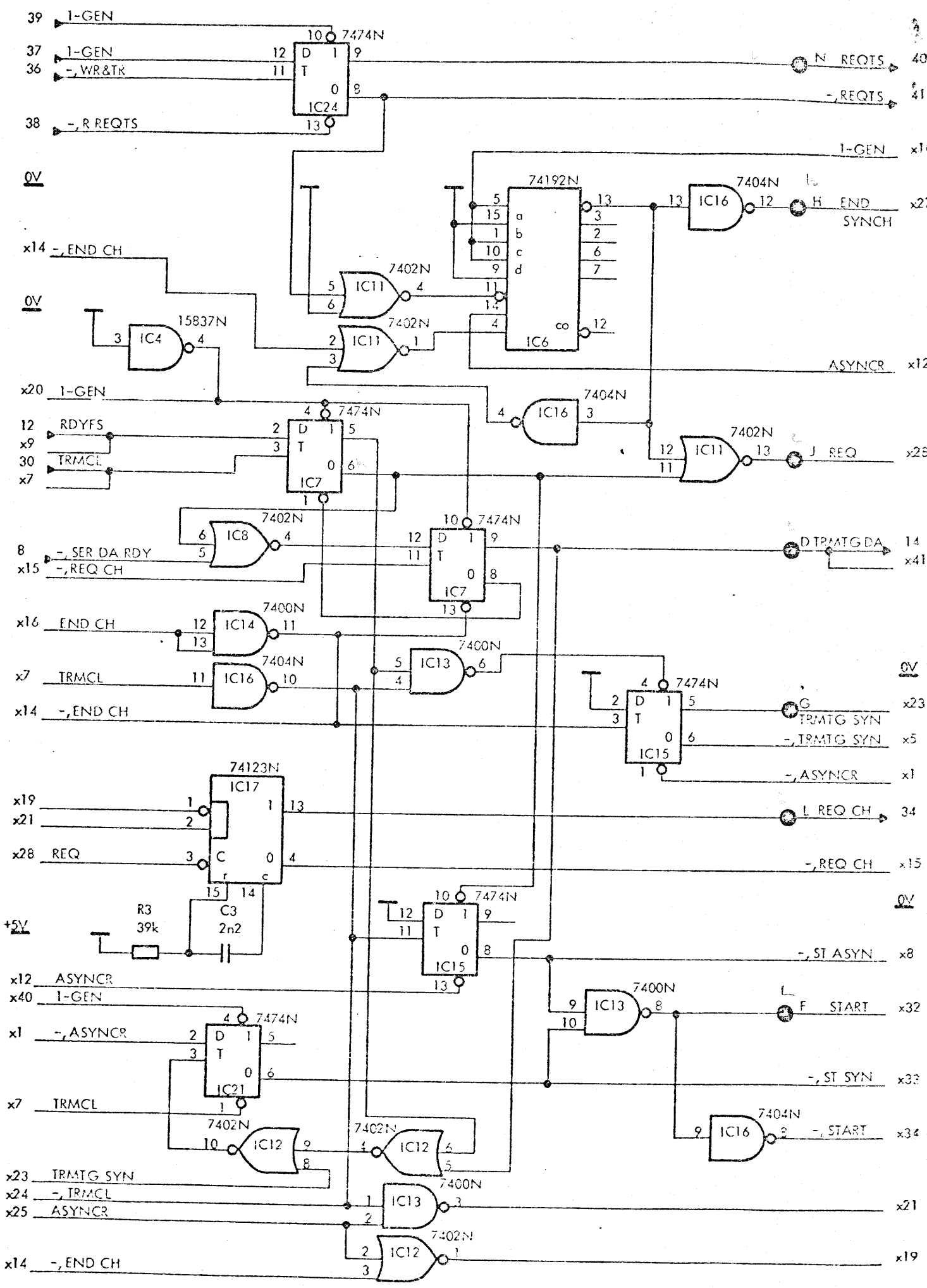
RC 2065-1
p 3 of 3



V23385

PC2065-1

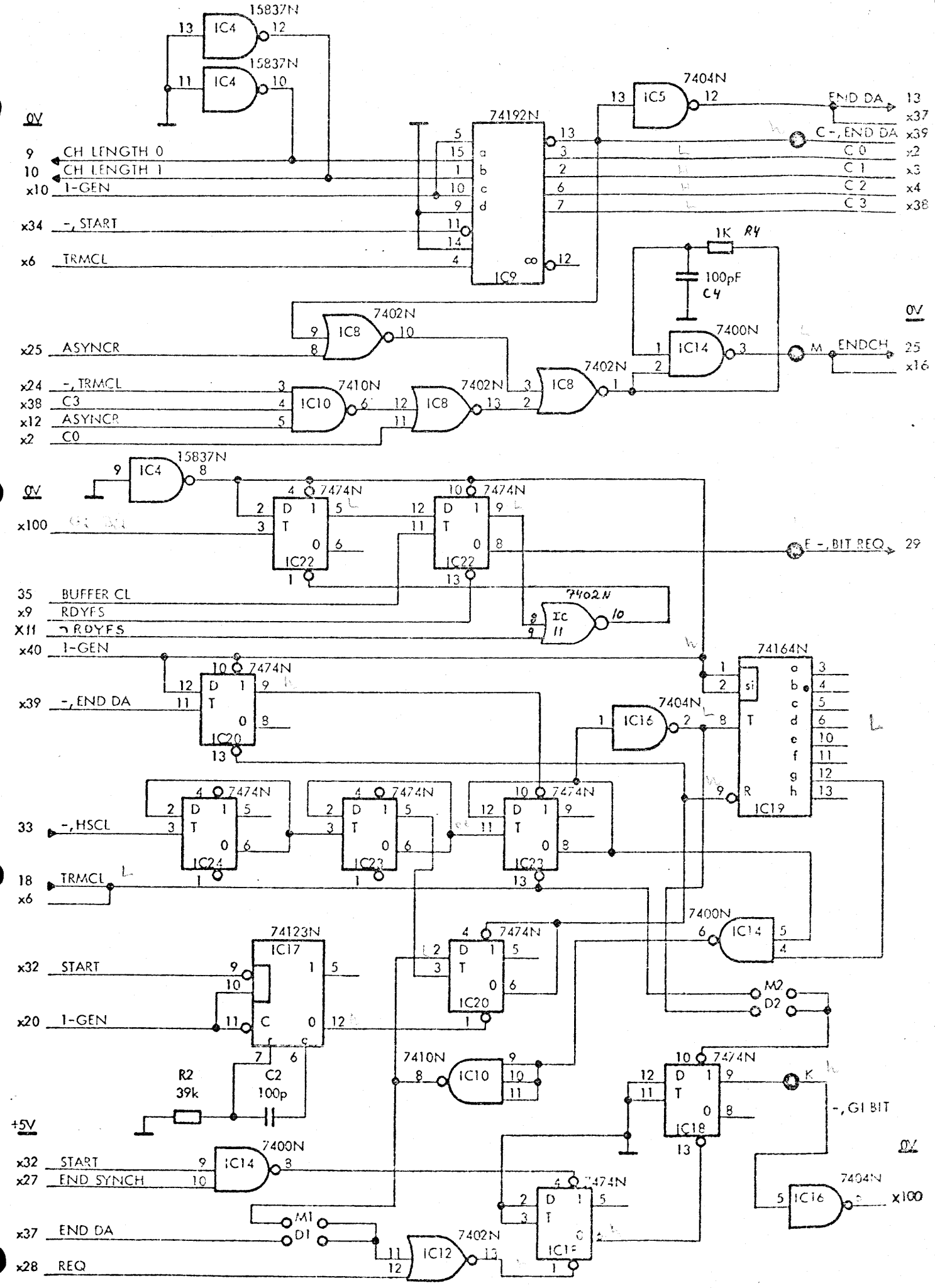
PCB Assembly Drawing



TRANSMITTER UNIT
PART 1
PCBA Circuit Diagram

V28441

RC2066-1
p1 of 3



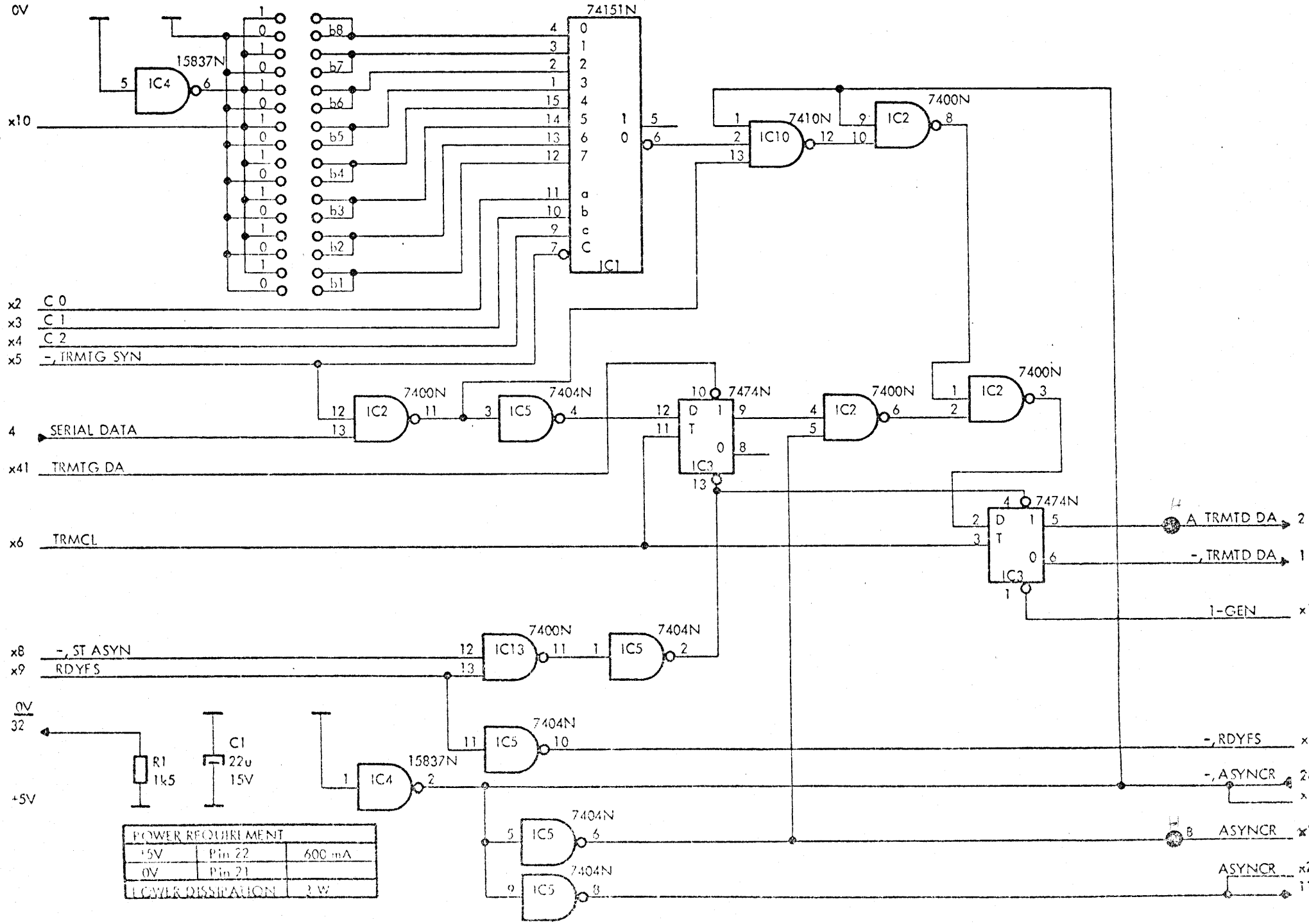
TRANSMITTER UNIT
PART 2
PCBA Circuit Diagram

RC2066-1
p 2 of 3

V23442

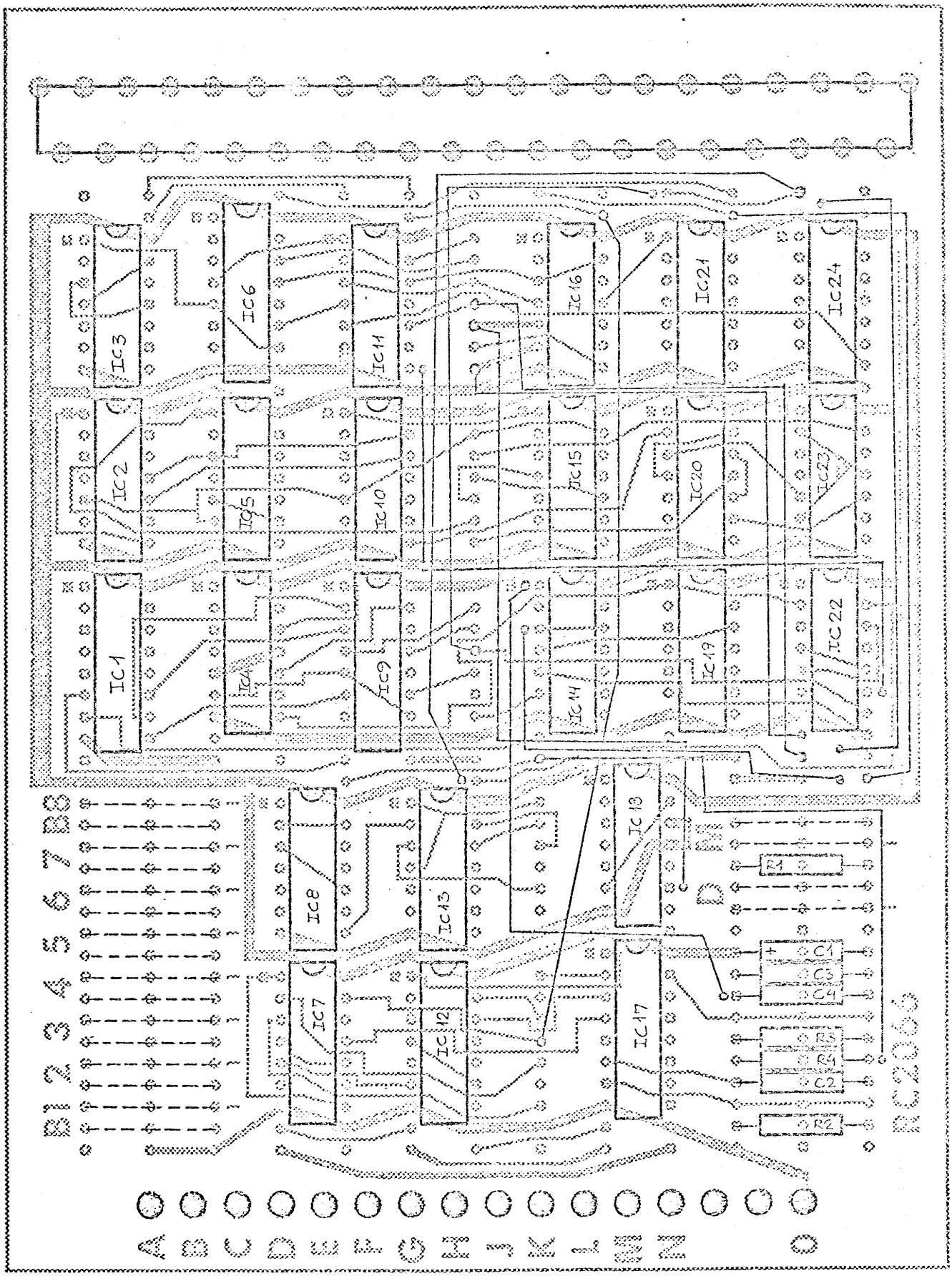
V23443

TRANSMITTER UNIT
PART 3
PCBA Circuit Diagram



POWER REQUIREMENT		
+5V	Pin 22	600 mA
0V	Pin 21	
POWER DISSIPATION		3 W

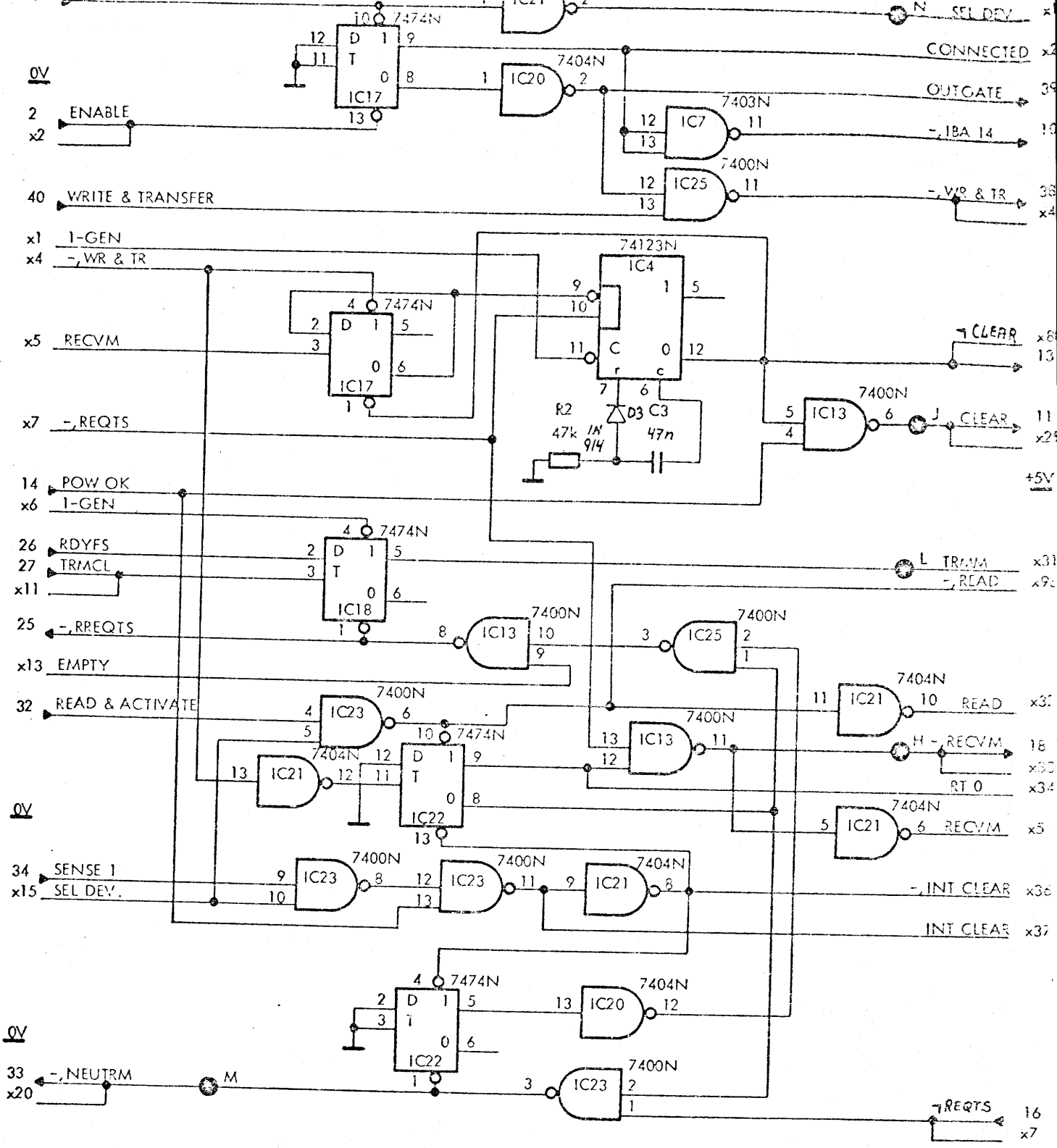
RC2066-1
P 3 of 3



RC2066-1

V23388

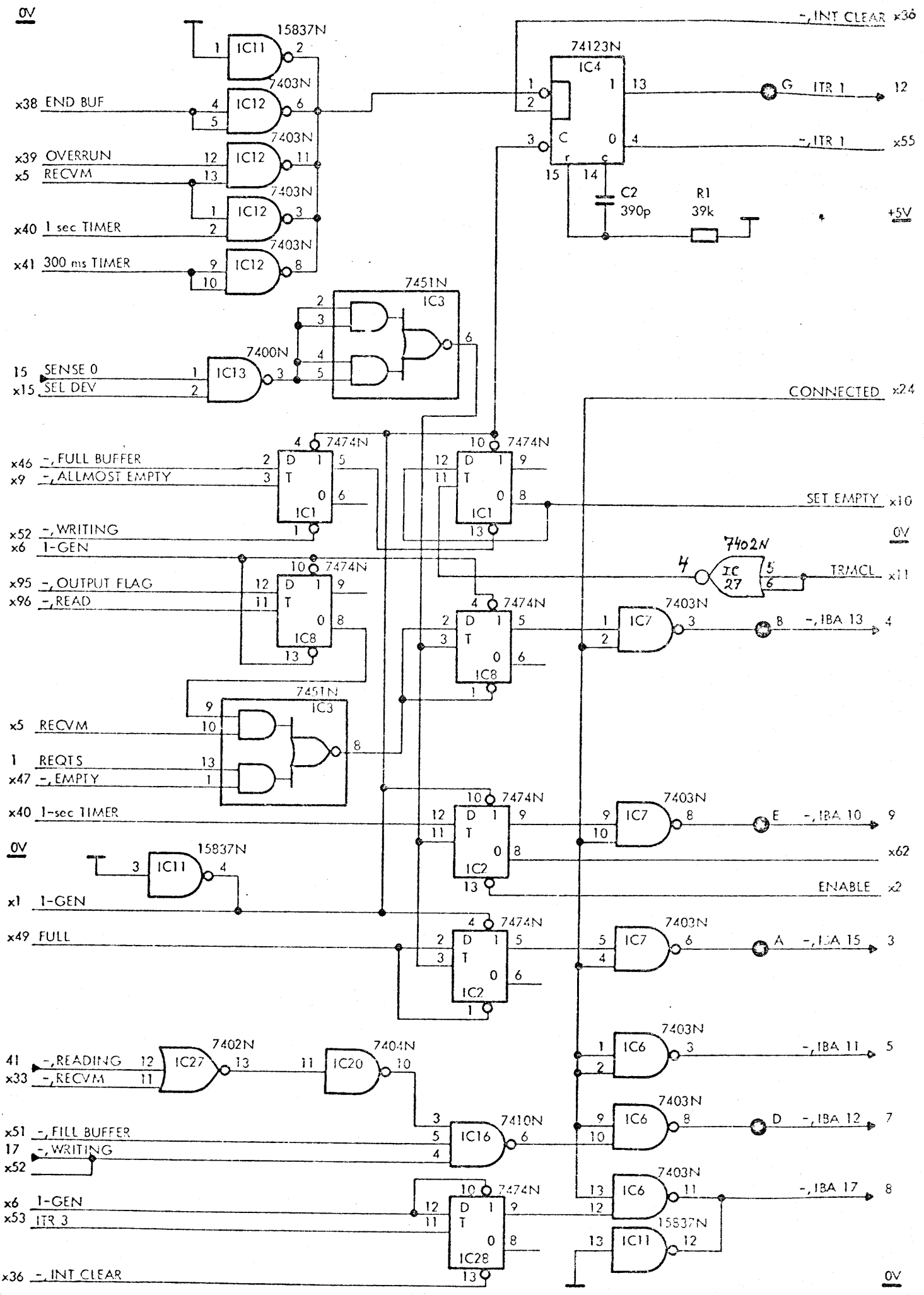
PCB Assembly Drawing



V23445

MSTC CONTROL CARD
MODE CONTROL
PCBA Circuit Diagram

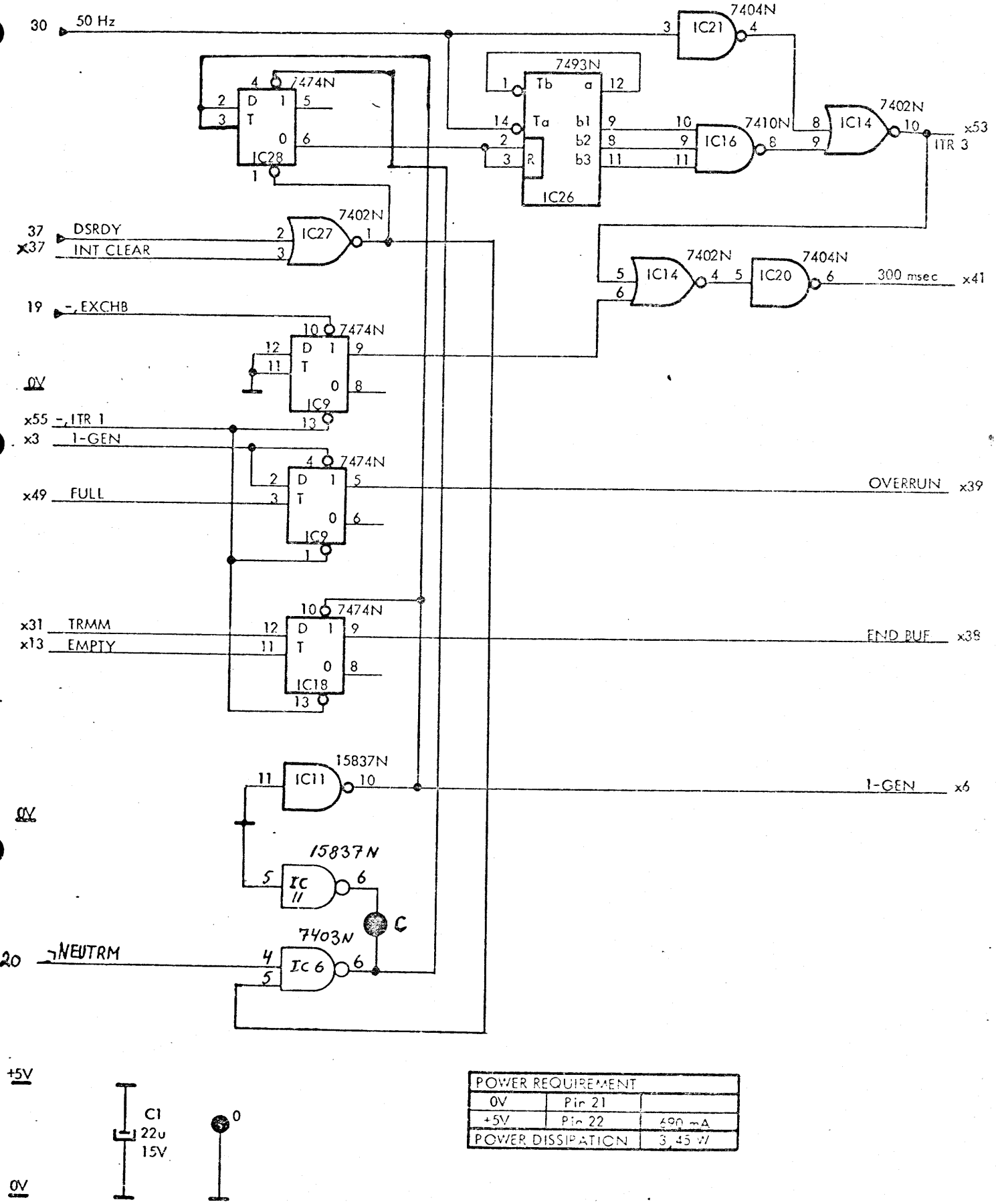
RC2067-1
p 1 of 4



MSTC CONTROL CARD
CHAR INTERRUPT AND STATUS REGISTER
PCBA Circuit Diagram

V23446

RC 2067-1
p 2 of 4

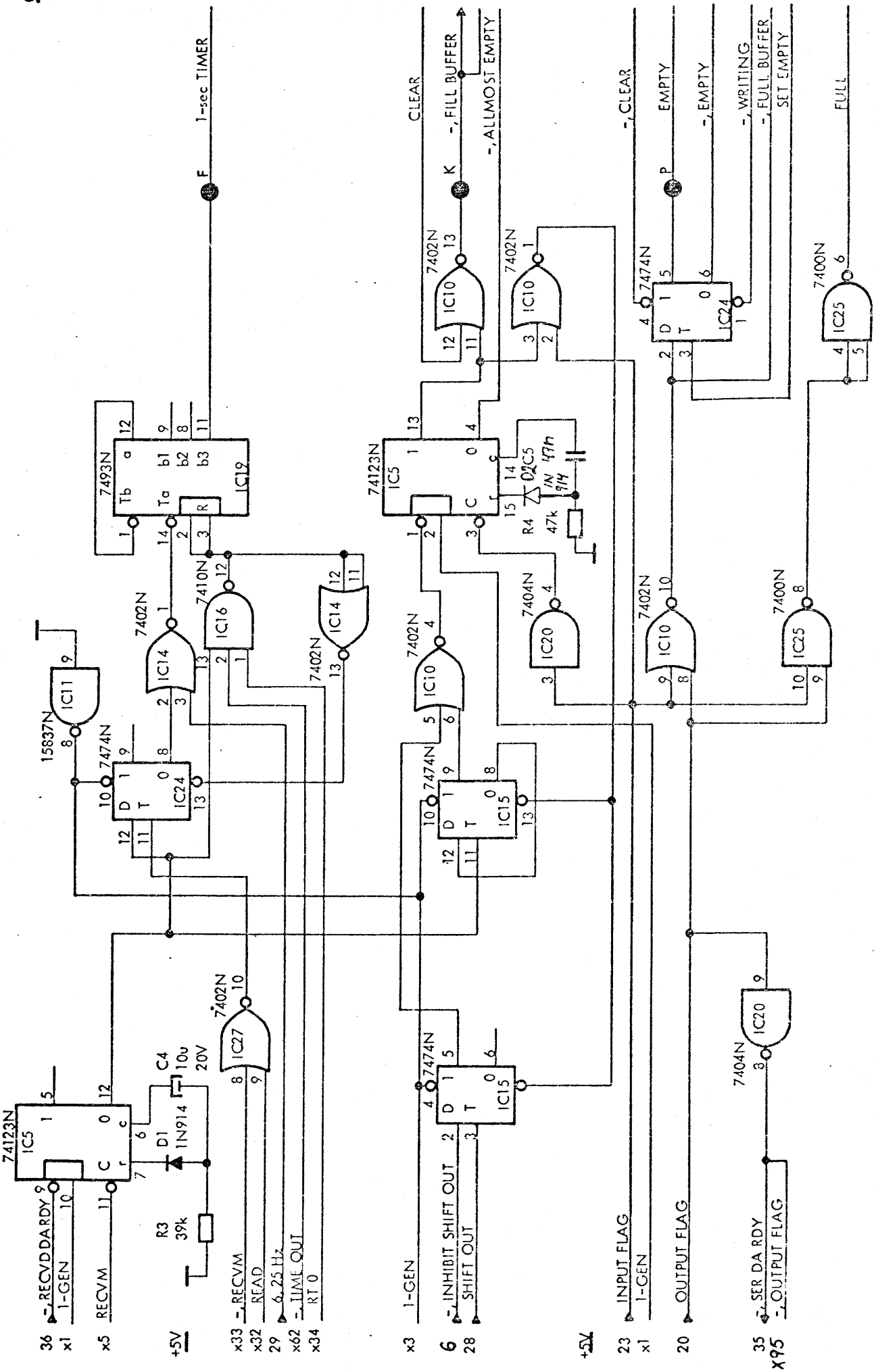


POWER REQUIREMENT		
0V	Pin 21	
+5V	Pin 22	690 mA
POWER DISSIPATION		3.45 W

V23447

MSTC CONTROL CARD
INTERRUPT LOGIC
PCBA Circuit Diagram

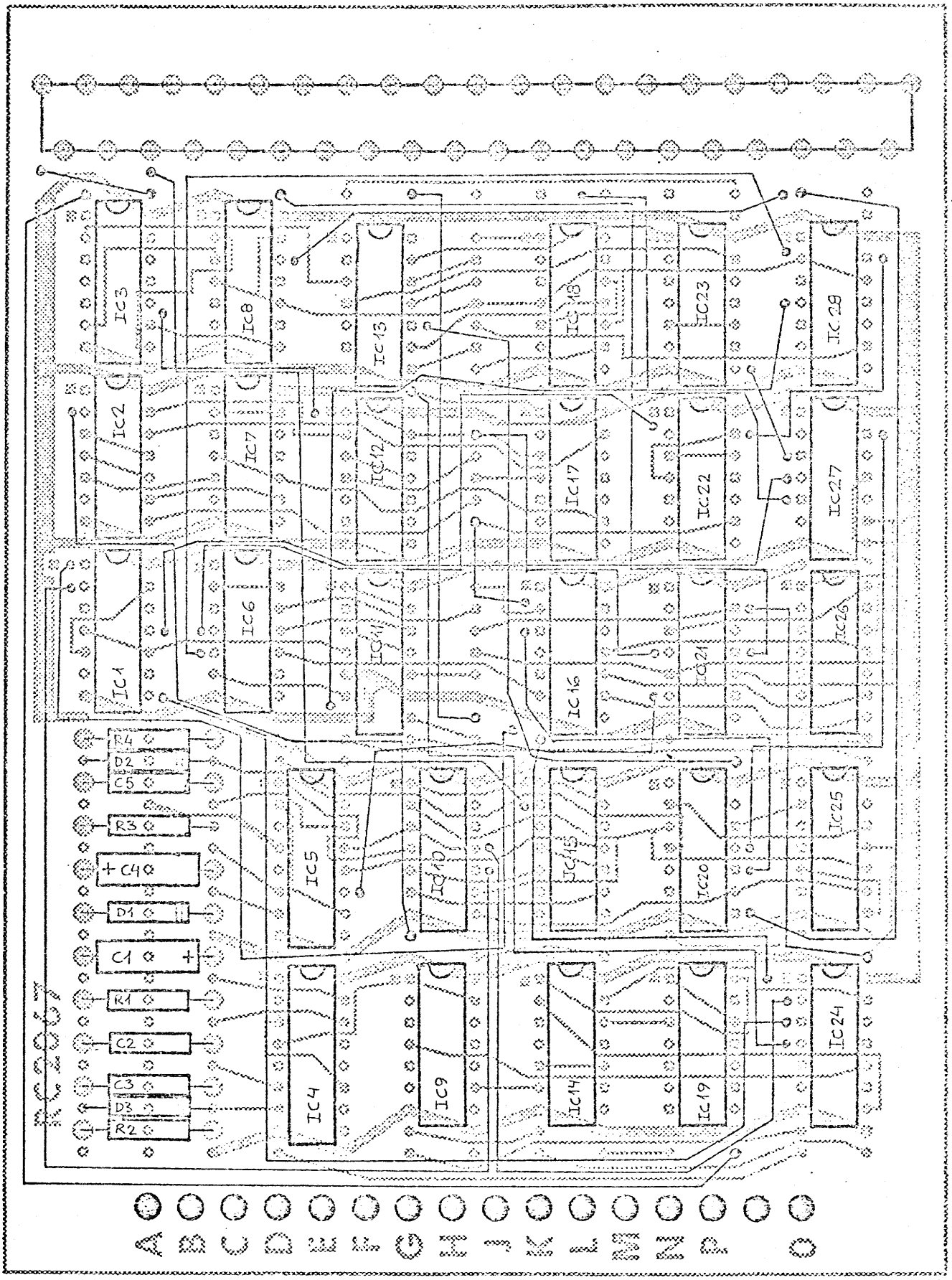
RC2067-1
p 3 of 4



MSTC CONTROL CARD
TIME OUTS
PCBA CircuitDiagram

V23448

RC2067-1
p 4 of 4



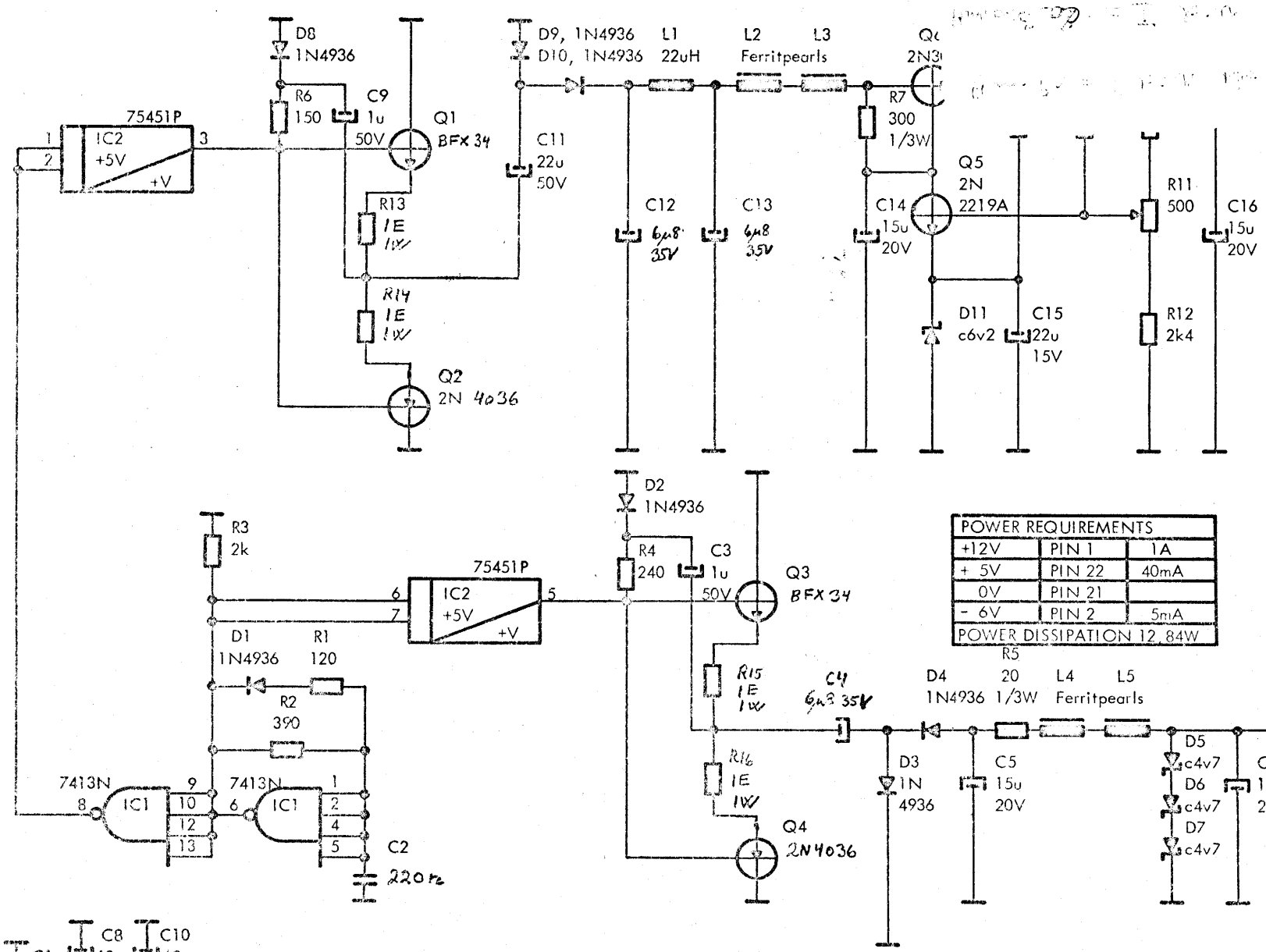
RC2067-1

V23391

PCB Assembly Drawing

16.3.73 KS 150972AL 150972BA 16.3.73 KS

Circuit A



POWER REQUIREMENTS		
+12V	PIN 1	1A
+ 5V	PIN 22	40mA
0V	PIN 21	
- 6V	PIN 2	5mA
POWER DISSIPATION 12.84W		

0V
+12V
+5V

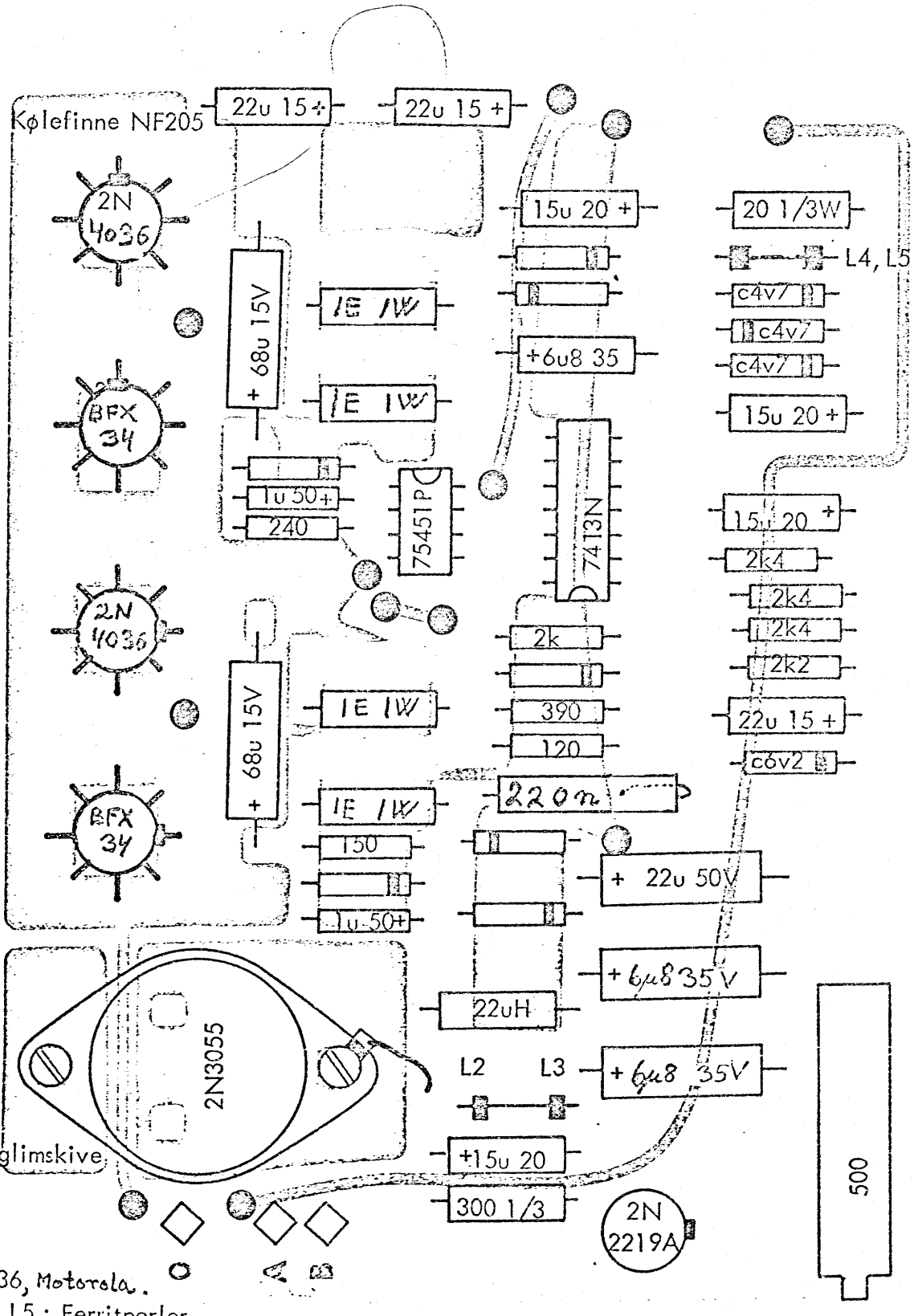
0V
-6V

+12V
+5V
0V
-6V

C1 22u 15V
C8 68u 15V
C10 68u 15V
C6 22u 15V

Circuit

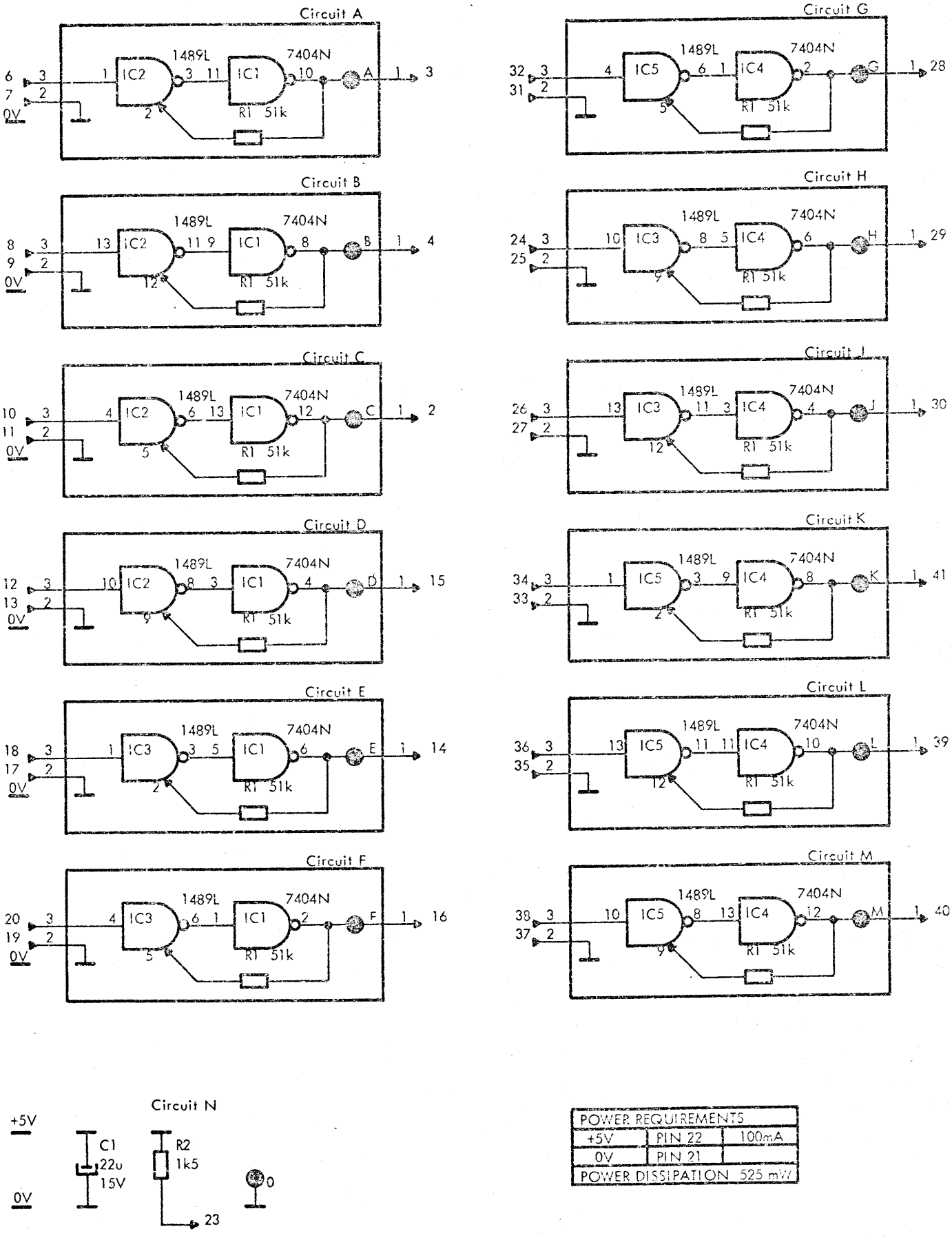
B C D E F G H J K L M N P R S T U V W X Y Z AA BB CC 0 2 38



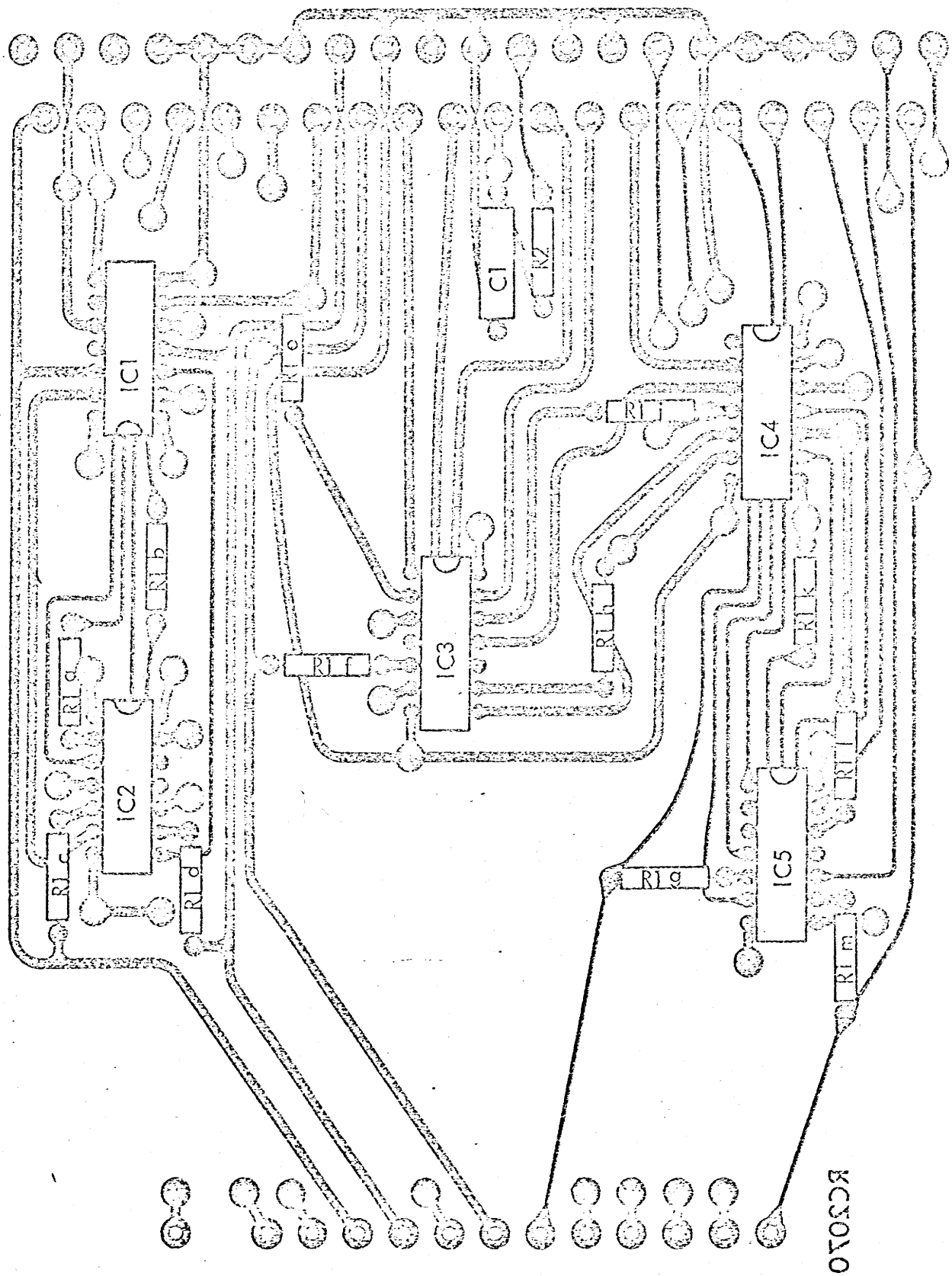
Monteres med glimskive.

Dioder: 1N4936, Motorola.
L2, L3, L4 og L5 : Ferritperler

Unit: RCLM400	Designed 15.3.78 k	MONTERINGSTEGNING	Drawing No V23312
A/S REGNE CENTRALEN	Approved	RC2069 - 1	Drawn by
	Checked		Checked
	Last Revision		Sheets / Sheet

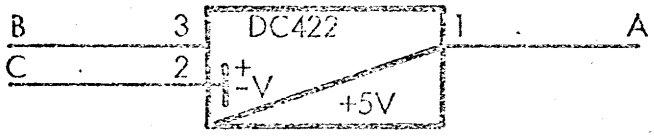


POWER REQUIREMENTS		
+5V	PIN 22	100mA
0V	PIN 21	
POWER DISSIPATION 525 mW		



Unit: RCLM400	Designed 270972BA	KOMPONENTPLACERING RC2070 - 1	Drawing no V23526
A/S REGNE CENTRALEN	Approved		Drawn by
	Checked		Checked
	Last Revision		Sheets / Sheet

DC 422



Circuit Description

The DC422 is a line receiver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of the CCITT standard V.24. Output is standard TTL level.
The operation of the circuit is described in the truth table below.

B	A
H	H
L	L

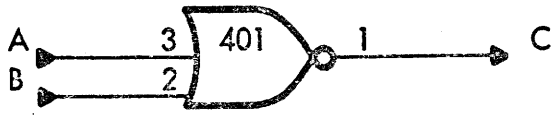
Input: H +3 V - +24 V
L -3 - -24 V.

Specifications

Input resistance: 3.0 k - 7.0 kohm
input signal range: ± 30 Volts.
Input threshold hysteresis: 400 mV.

Unit:	Designed		Drawing No
A/S REGNE CENTRALEN	Approved		Drawn by
	Checked		Checked
	Last Revision		Sheets / Sheet

AD401



CIRCUIT DESCRIPTION

The AD401 is a 2-input NORelement

C = -,(A!B)

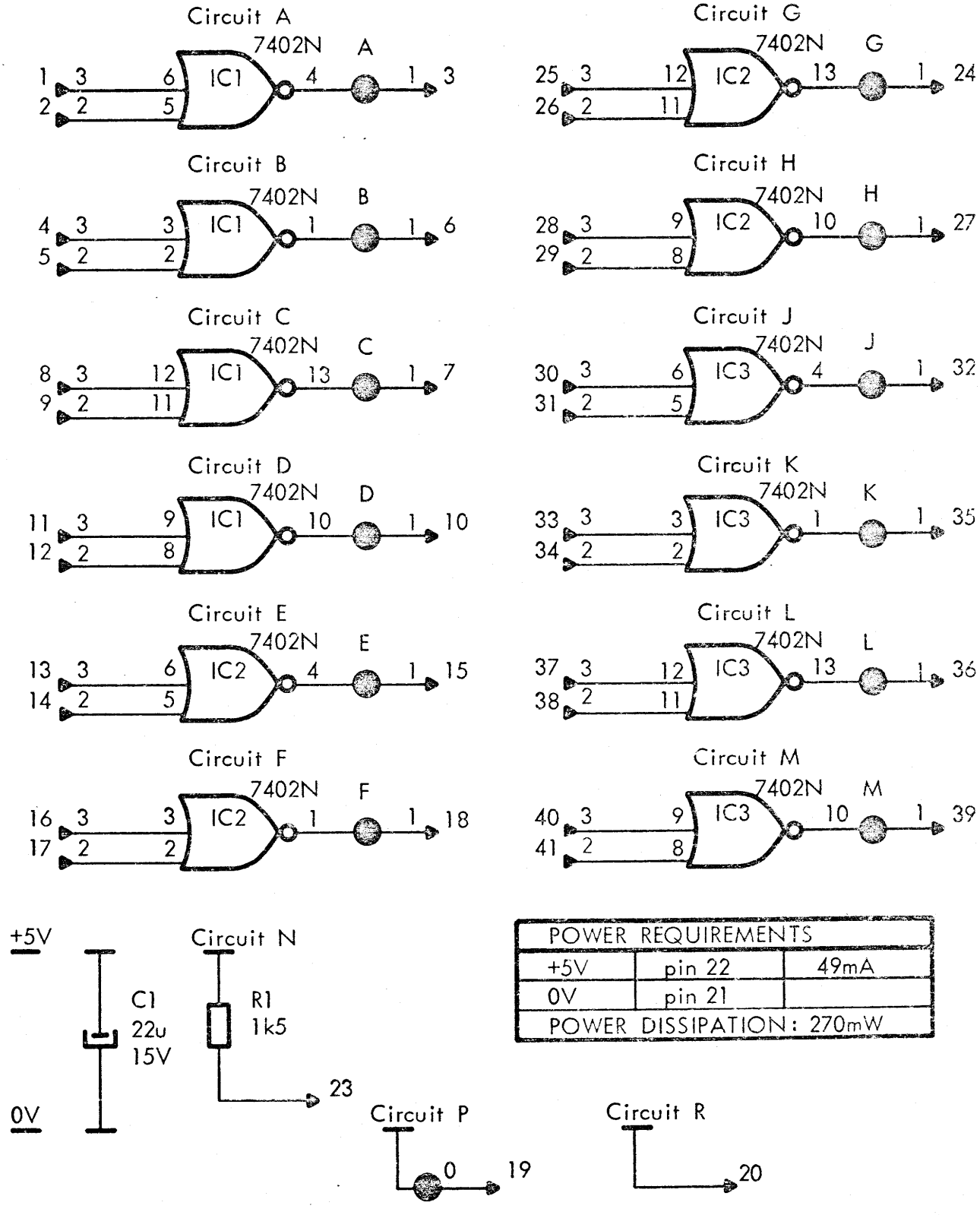
SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	1 unit load (each input)
Fan-Out	10 unit loads

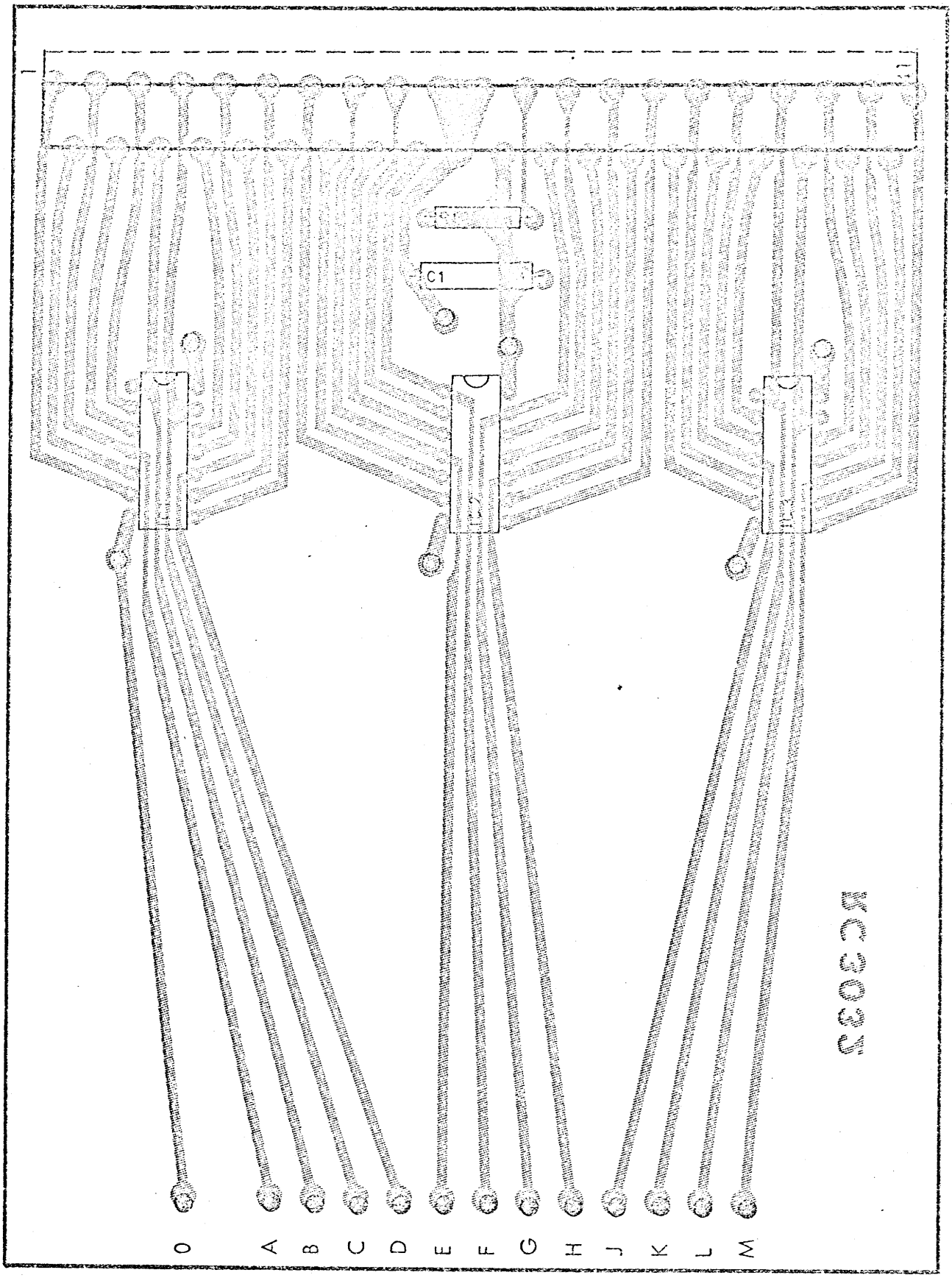
SWITCHING CHARACTERISTICS

Propagation Time	td(1)	Typ. 18 nS; Max. 29 nS
	td(0)	Typ. 8 nS; Max. 15 nS



POWER REQUIREMENTS		
+5V	pin 22	49mA
0V	pin 21	
POWER DISSIPATION: 270mW		

020469JCJ 110769CEM 290769JA 080769AAGR



RCLM400 12 AD401 RC3032-1

A20326 PCB Assembly Drawing

RCLM400

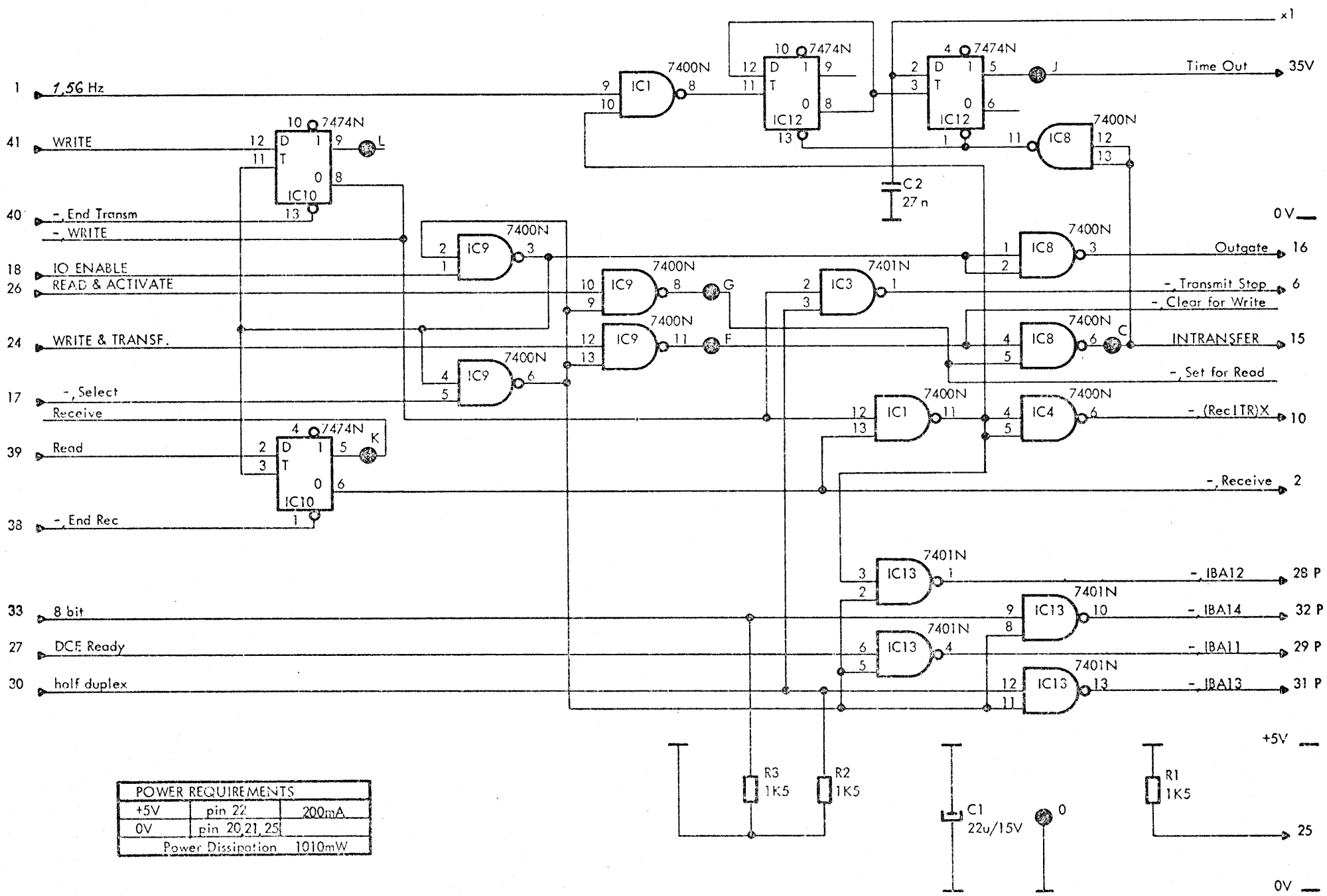
R16078

PCBA Circuit Diagram

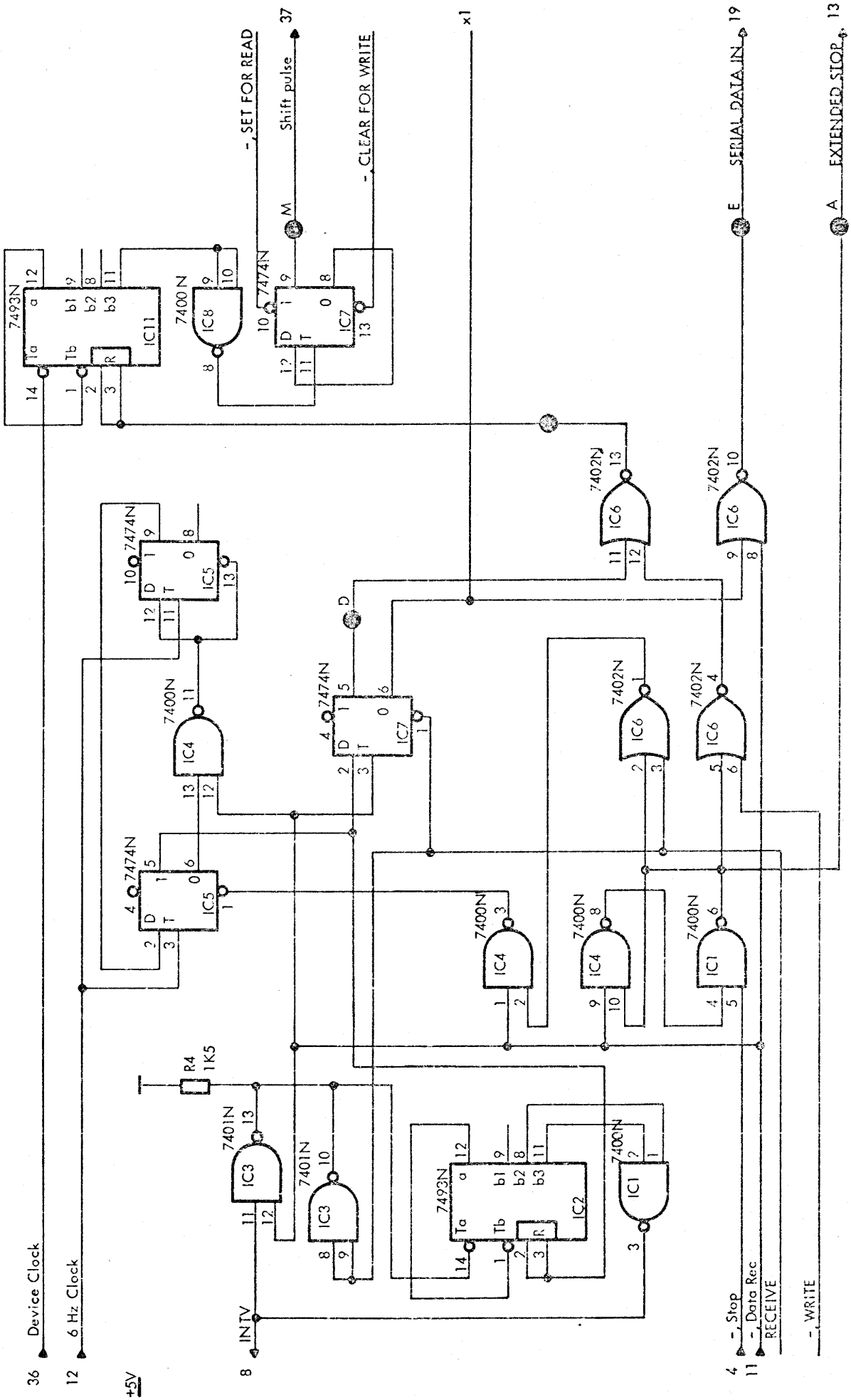
1 SA450

RC3041-1

P1 of 2



POWER REQUIREMENTS		
+5V	pin 22	200mA
0V	pin 20,21,25	
Power Dissipation 1010mW		



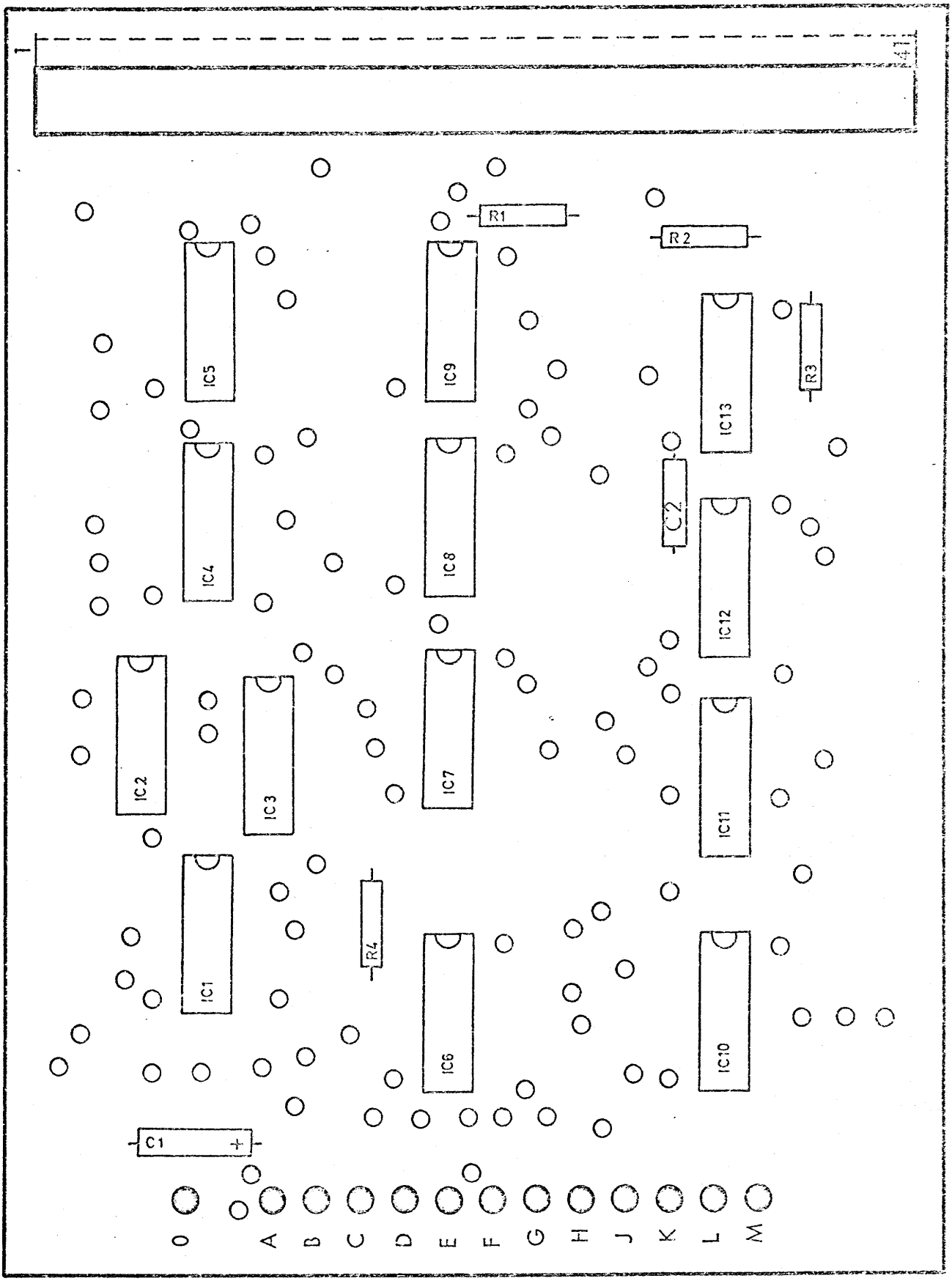
RCLM400

R10079

1 SA450

PCBA Circuit Diagram

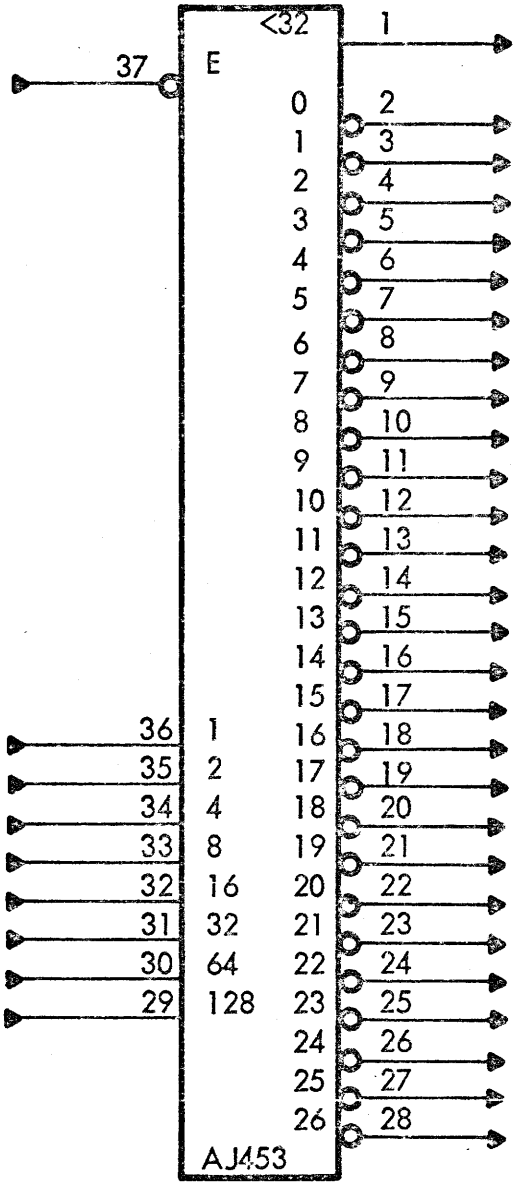
RC3041-1
P2 of 2



RCLM400 1 SA450 RC3041-1

R20066 PCB Assembly Drawing

AJ453


<32
E
AJ453
37
36
35
34
33
32
31
30
29
1
2
4
8
16
32
64
128
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
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24
25
26
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28

CIRCUIT DESCRIPTION

The AJ453 is a Subtraction circuit, which senses the difference between an 8 bit input byte, and a variable reference byte strapped on soldering terminals within the circuit.

The output is given modulo 32 as a one out of 32 decodings. However, only the values 0 to 26 are actually represented by an output pin. The output is low when true.

The output terminal < 32 is true if the true difference lies from 0 to 31.

A true input at E will enable the circuit. A false input will keep all outputs false.

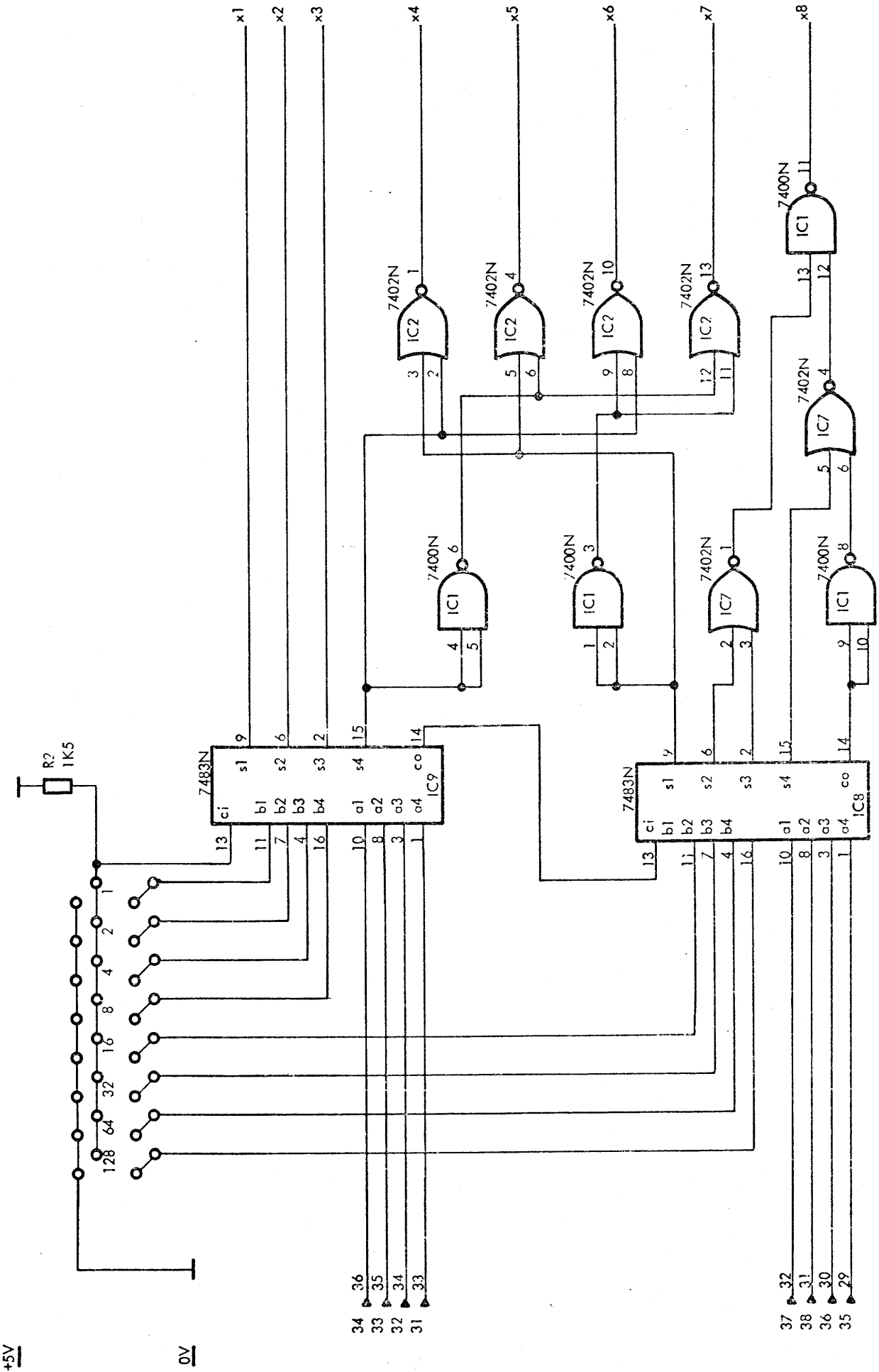
SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input levels	RCLM400 standard levels
Input Loads	
Input 2, 8, 32, 128	4 unit loads (each input)
Input 1, 4, 16, 64	1 unit load (each input)
Input E	2 unit loads
Fan Out	
Output 0-26	10 unit loads
Output < 32	16 unit loads

SWITCHING CHARACTERISTICS

Propagation delay	
from E input to logical 1 or 0 at	
output 0-26	max. 80 nS
from E input to logical 1 at	
output < 32	max. 29 nS
from E input to logical 0 at	
output < 32	max. 15 nS
from input 1-128 to logical 1 or at	
output < 32	max. 140 nS



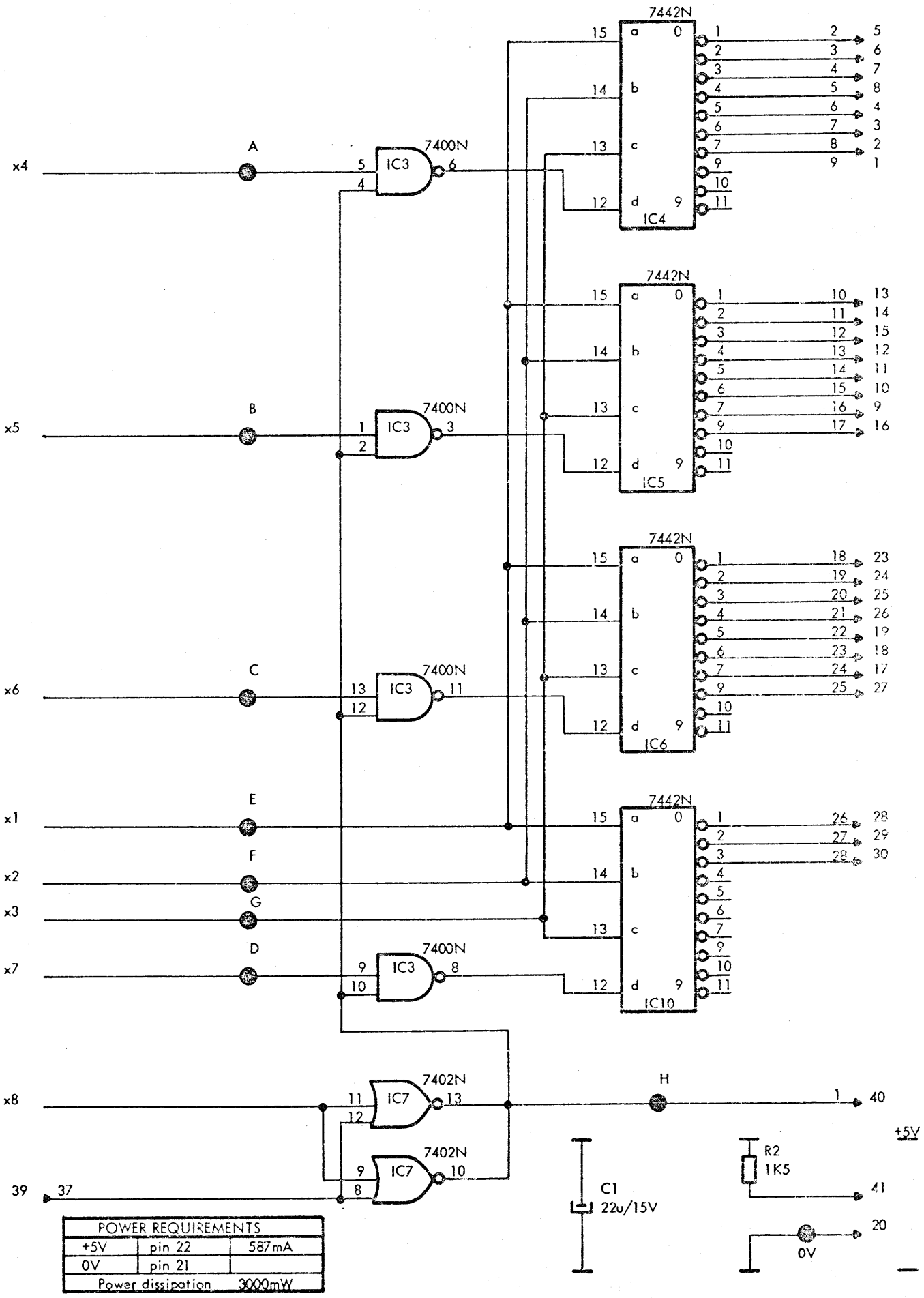
RCLM400

1 AJ453

RC3051-1
P1 of 2

A10266

PCBA Circuit Diagram



POWER REQUIREMENTS		
+5V	pin 22	587mA
0V	pin 21	
Power dissipation		3000mW

RCLM400

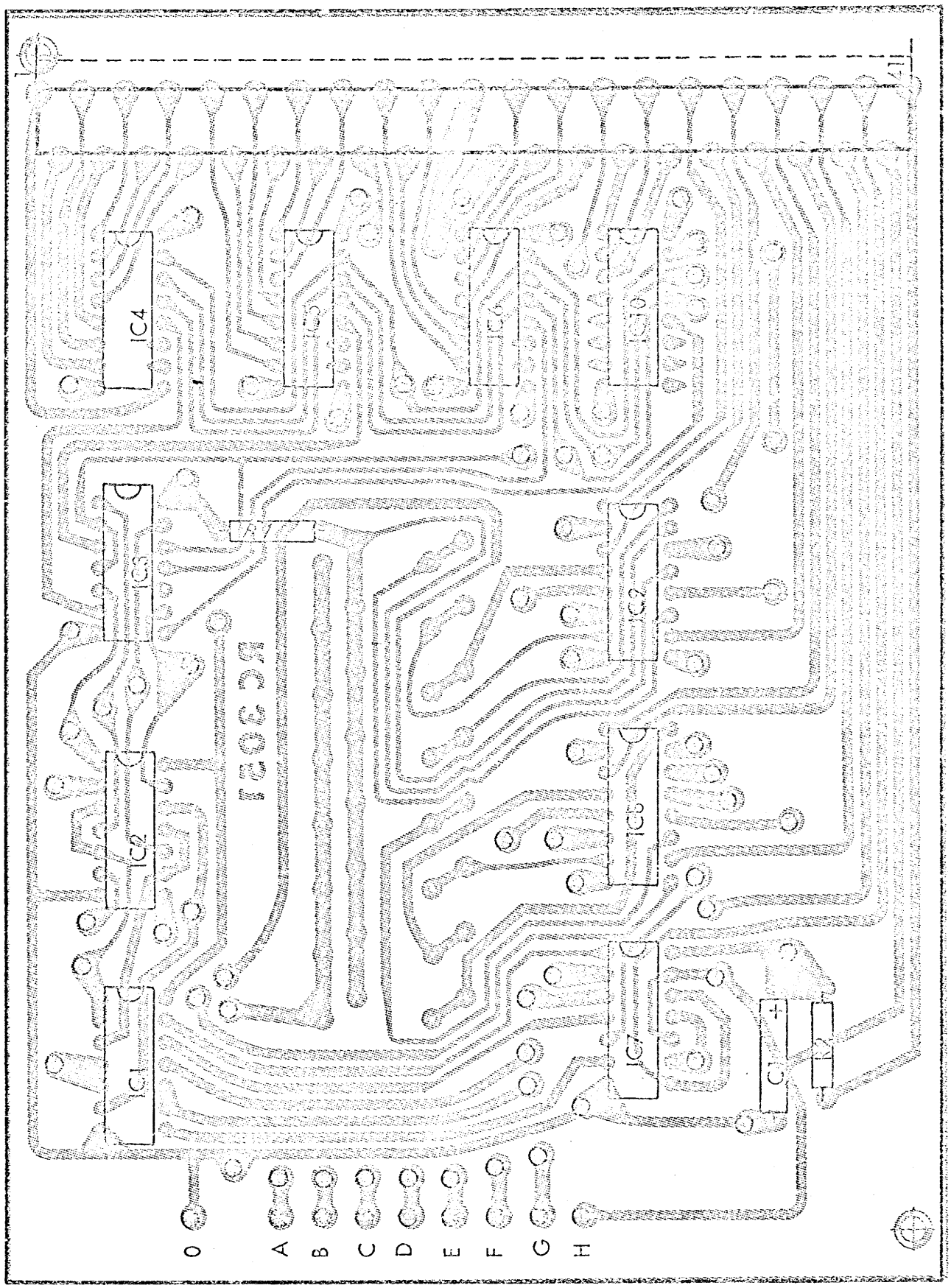
1 AJ453

RC3051-1
P2 of 2

A10267

PCBA Circuit Diagram

040269 BN 250869 KS 091069 LM 090170BN

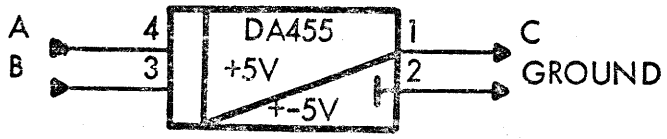


RCLM400 1 AJ453 RC3051-1

A20472 PCB Assembly Drawing

RCSL: 52-AA76
pp. 1:2
June 1969

DA455



CIRCUIT DESCRIPTION

The DA455 is a digital output level converter for coupling RCLM400 elements to systems utilizing logic signals (nominal +5V and -5V). The DA455 accepts RCLM400 standard signals at input A and B. The output terminal GROUND may e.g. be used for twisted pair wiring.

The logical operation of the circuit is described in the truth table below.

A	B	C
L	L	L
L	H	L
H	L	L
H	H	H

H denotes the most positive level and L the most negative level.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input levels, A and B	RCLM400 standard levels
Input Loading, A and B	1 unit load (each input)
Output levels	
Output high	+13V $\geq$ V out $\geq$ +5V
Output low	-5V $\geq$ V out $\geq$ -6V
Output Drive Capability	
Output high 1)	Max. -5 mA, V out = +5V
Output low 1)	Max. 15 mA, V out = -5V

SWITCHING CHARACTERISTICS

Delay from input to output	td+ 2)	Typ. 220 nS
	td- 2)	Typ. 220 nS

NOTES

1) The sign is positive when current flows towards the circuit.

2) td+ is the delay, when the output changes to a more positive level, and td- is the delay, when the output changes to a more negative level. Delays are measured with max. load on the output.

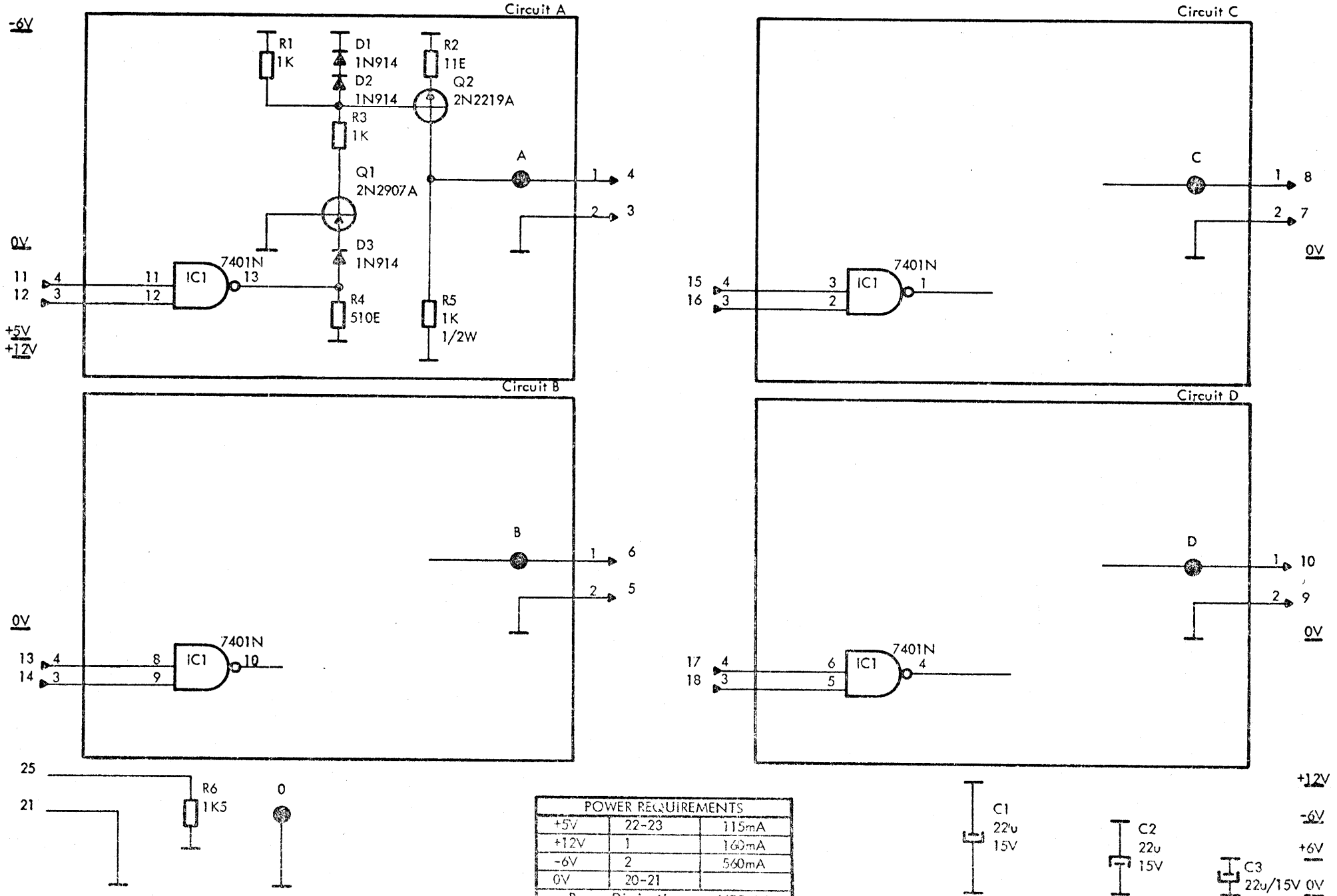
RCLM400

A10330

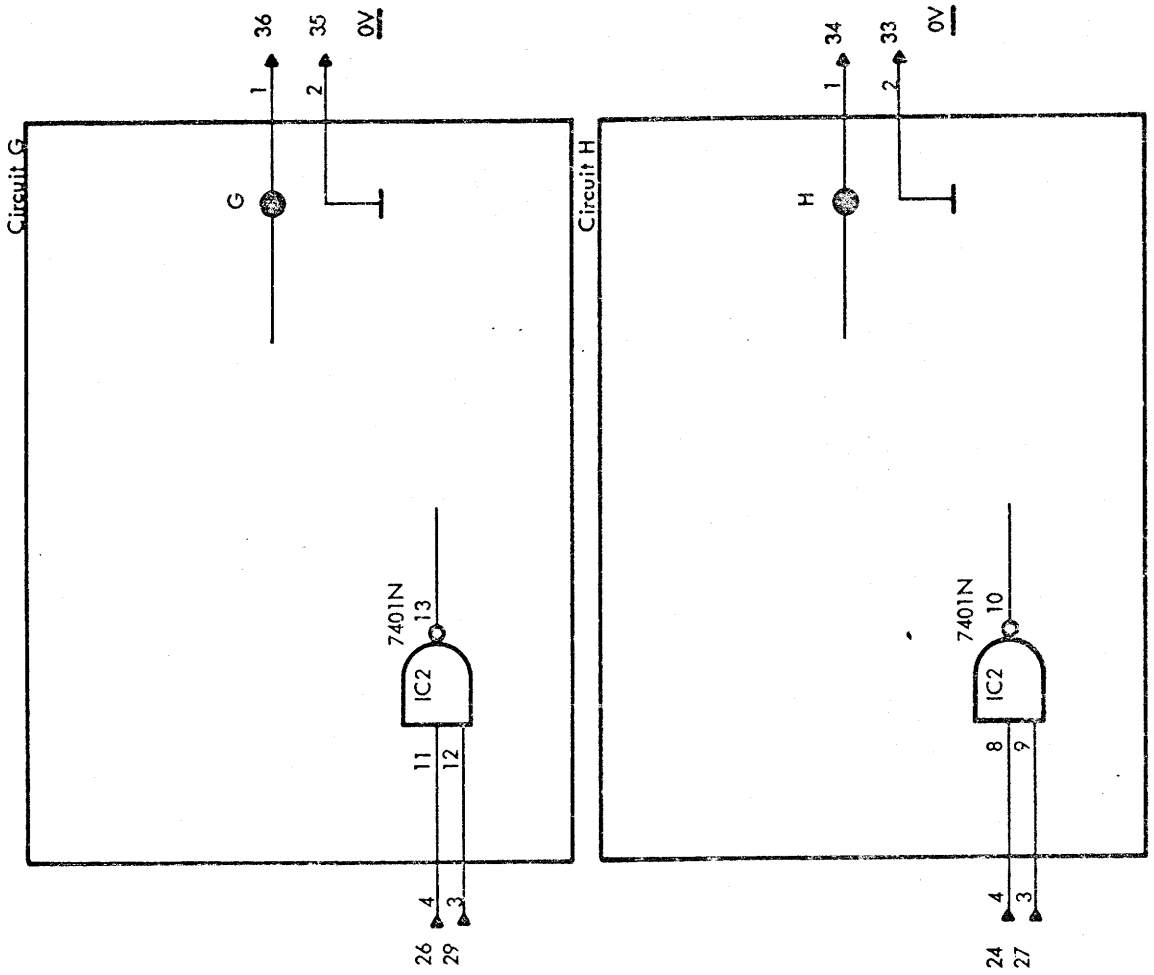
8 DA455

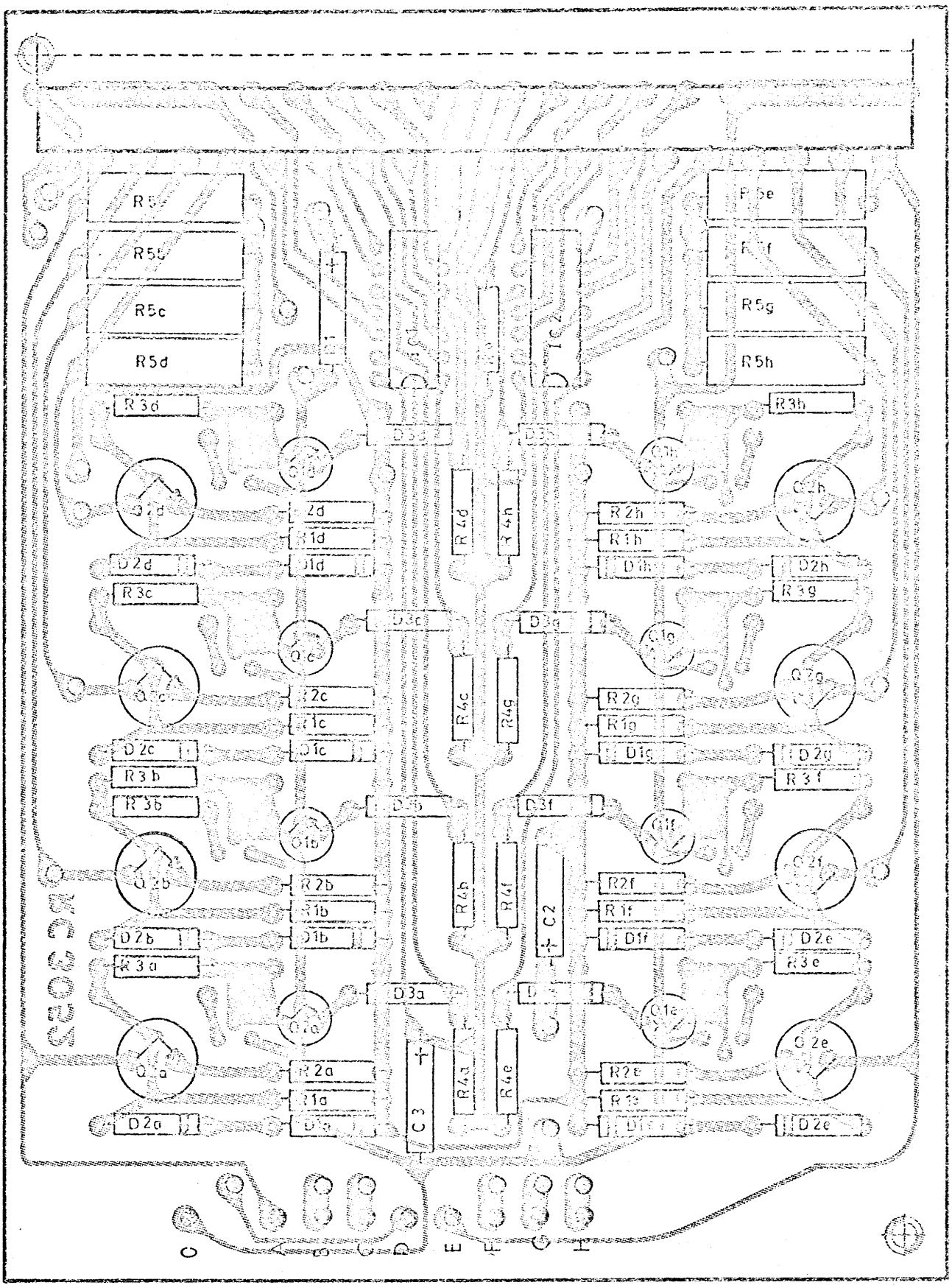
PCBA Circuit Diagram

RC3052-2
P1 of 2



POWER REQUIREMENTS		
+5V	22-23	115mA
+12V	1	160mA
-6V	2	560mA
0V	20-21	
Power Dissipation		4475mW


Circuit G
Circuit H
Circuit E
Circuit F
7401N
IC2
0V



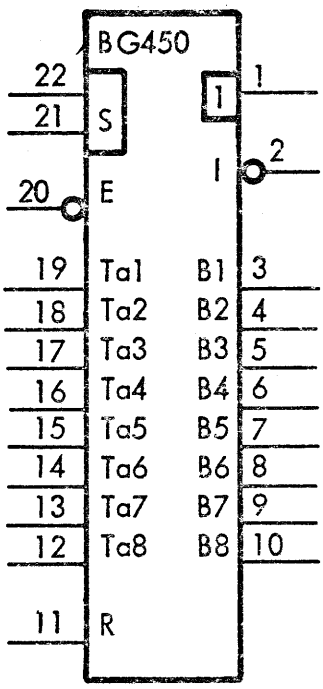
0910698n 091069SKS 091069JA 091070BN

RCLM400 8 DA455 RC3052-2

A20506 PCB Assembly Drawing

RCSL: 52-AA74
pp. 1:2
June 1969

BG450



CIRCUIT DESCRIPTION

The BG450 consists of two 8 bit registers A and B together with control logic connected to transform 8 interrupt signals into one single interrupt.
Each register is made by 8 D-type edge triggered flip-flops.

Transitions from 0 to 1 on the inputs Ta1-Ta8 will set flip-flops in the A register. The output of this register is connected to a wired or gate and will thus generate a common interrupt output.

The signal E will enable the B register to receive the information stored in reg. A. A parallel transfer is initiated when the two S inputs are both ones. Reg. B will hold the information till E again goes false.

If a flip-flop in the A register is transferring a one to reg. B, it will not react to transitions on the input until E has gone false.

A logical one at the Reset (R) input will set reg. B to one and reg. A to zero.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input loadings

S, E, R	1 unit load (each input)
Ta1 - Ta8	2 unit loads (each input)

Fan Out

B1 - B8	10 unit loads (each output)
I	wired or output
logical 1	I out max. - 2 mA
logical 0	I out max. - 16 mA

A logical 1 generator (1100 ohm) in each BG450 circuit will allow the I outputs from 1 to 3 circuits to be wire ored, to form a common output.

SWITCHING CHARACTERISTICS

Propagation delays (nS)

from input S to a logical 1 or 0	
at outputs B1 to B8	max. 160 nS
from input R to logical 1 or 0	
at outputs B1 to B8	max. 55 nS

RCLM400

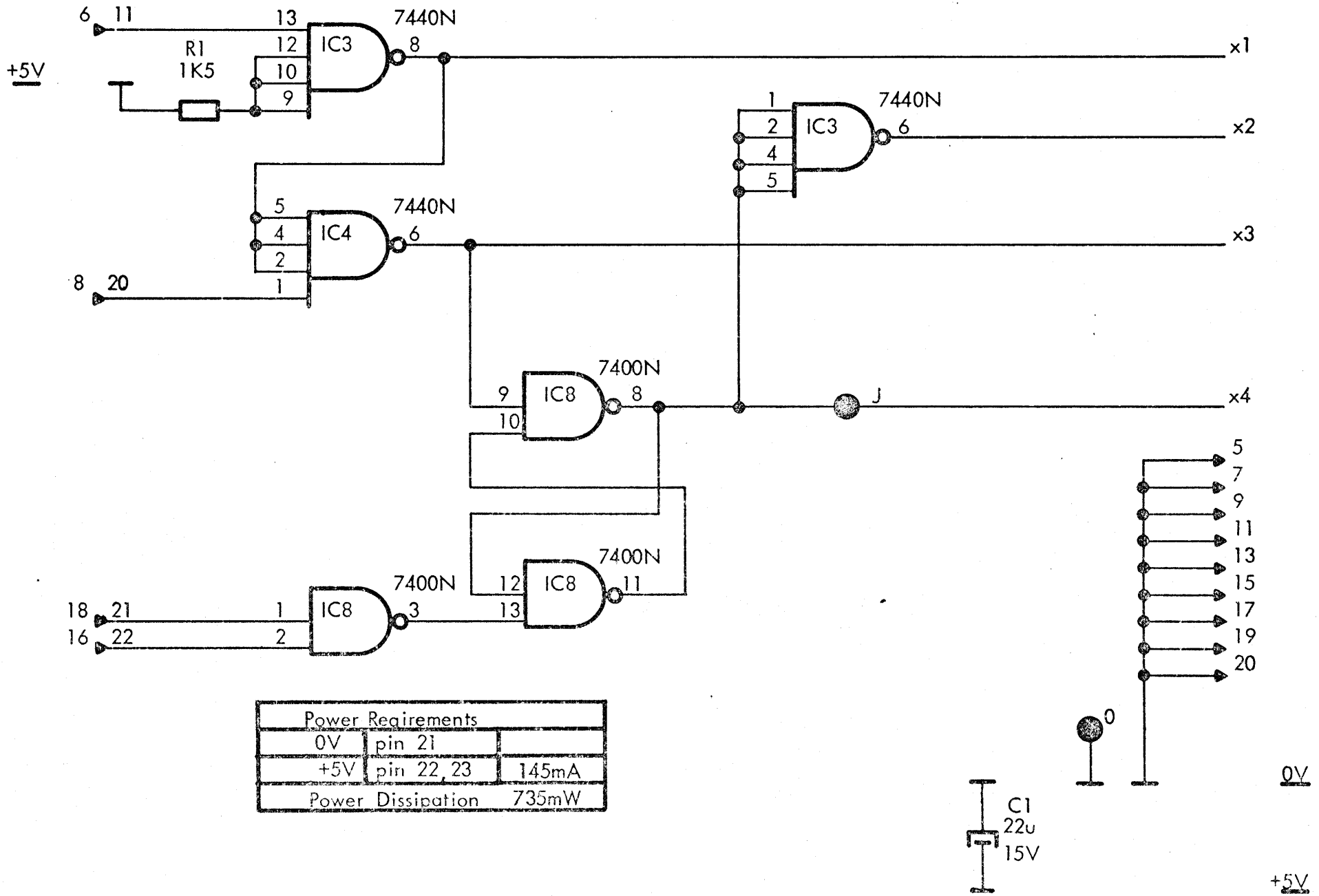
A20321

PCBA Circuit Diagram

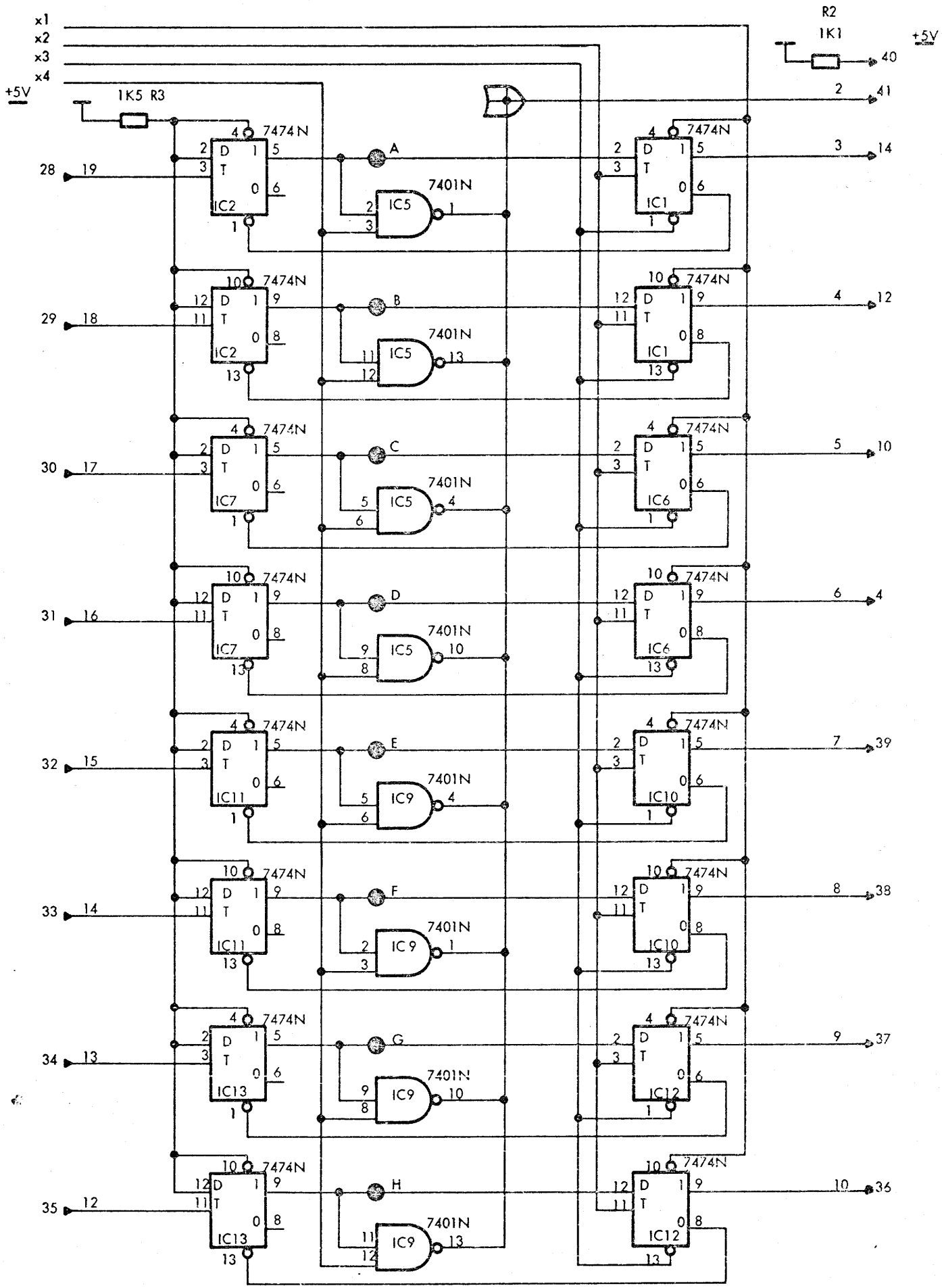
1 BG450

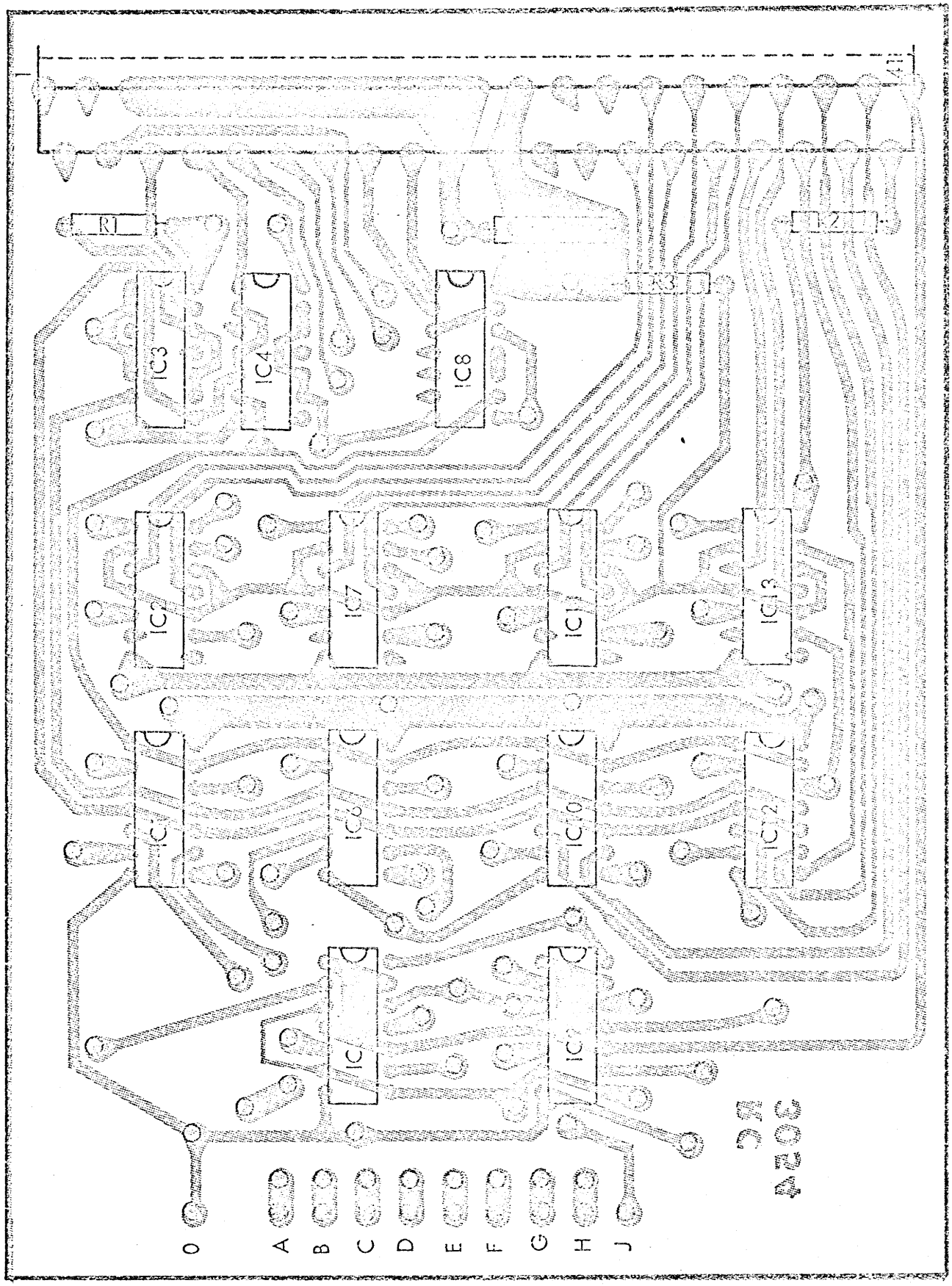
RC3054-1

p1 of 2



Power Regirements		
0V	pin 21	
+5V	pin 22, 23	145mA
Power Dissipation		735mW


x1
x2
x3
x4
+5V
1K5 R3
R2
1K1
+5V
40
2
41
3
14
4
12
5
10
6
4
7
39
8
38
9
37
10
36
28
19
29
18
30
17
31
16
32
15
33
14
34
13
35
12
7474N
7401N
IC2
IC1
IC7
IC6
IC11
IC10
IC13
IC12
IC5
IC9
A
B
C
D
E
F
G
H



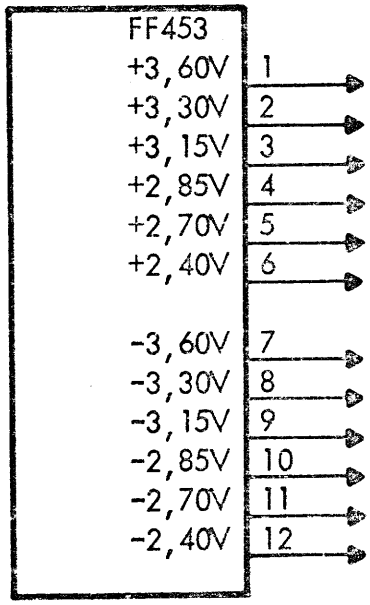
160669 BSP 260892 KS 091069 LLM 090170B

RCLM400 | BG450 | RC3054-1

A20476 PCB Assembly Drawing

RCSL: 52-AA79
pp. 1:2
Dec. 1969

FF453



CIRCUIT DESCRIPTION

The FF453 is a voltage generator producing 12 voltages with an accuracy better than 1 0/0.
The 12 voltages are intended to be used as reference levels for voltage supervision circuits.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Output impedance

Outputs: 1, 7	0 ohm
- 2, 8	9 ohm
- 3, 9	13 ohm
- 4, 10	20 ohm
- 5, 11	22,5 ohm
- 6, 12	27 ohm

Maximum permissible output currents

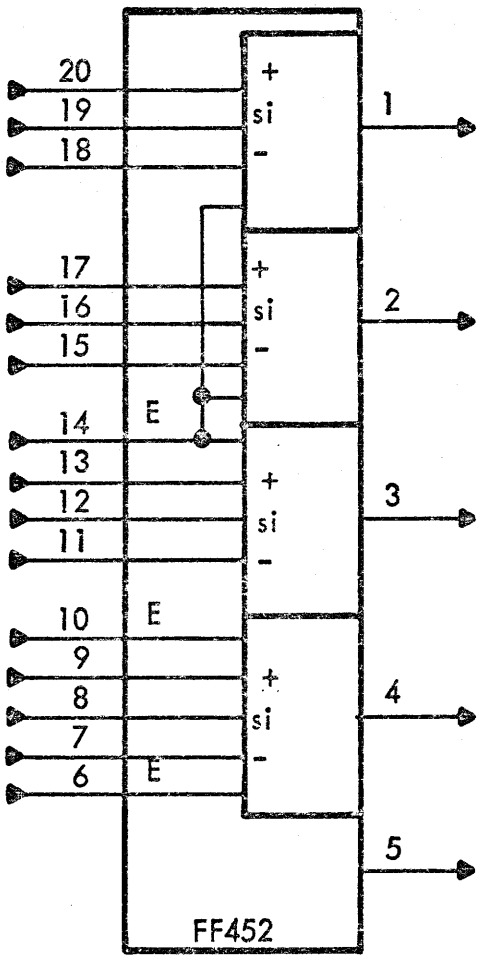
outputs 1 to 6	+ 5 mA > I out > -25 mA
outputs 7 to 12	+25 mA > I out > -50 mA

Adjustment:

The potentiometer shall be set so that the most negative reference output (7) is -3,60 Volts $\pm$ 0,01 Volt.

RCSL: 52-AA78
pp. 1:3
September 1969

FF452



CIRCUIT DESCRIPTION

The FF452 is 4 comparison circuits designed to work as a voltage supervision circuit able to check upper and lower limits for 4 voltages.

Each circuit has one or two of each of the following inputs:

Sense inputs (si) to which the supervised voltage shall be connected. An internal voltage divider will reduce a nominal input voltage to 3,00 V before it is compared with the reference voltages.

Reference inputs (+and-) which connected to the reference voltages will give the more positive (+) and the more negative (-) limit.
Supervising a negative voltage for an accuracy of ± 5 0/0 will then require -2,85 V at the (+) input and -3,15V at the (-) input.

Enable inputs (E). A logical 0 at one of these inputs will disable the supervision of either the upper or lower voltage limit in the circuits connected to it. This feature may be used where the circuit shall supervise one of the limits only, e.g. during the switch-on period of the supervised voltage.

The four outputs (1 to 4) will generate a logical one if the related circuit senses an error.
The common output (5) will generate a logical one if one or more of the circuits sense an error.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input loads	max. 4 mA
Reference inputs	max. 0,150 mA
Enable inputs 1) logical one	max. -0,95 mA
logical zero	max. -1,6 mA
Output 1 to 4 2)	
Logical 1 level	Min. 2,5V; typ. 4V; max. 5V
Logical 0 level	Min. -1V; typ. -0,5V; max. 0V
Sink current	Min. 0,5 mA; typ. 0,8 mA;
Output resistence	Typ. 200 ohm

Output 5 is the cathodes of 4 1N914 diodes connected to output 1 to 4.

SWITCHING CHARACTERISTICS

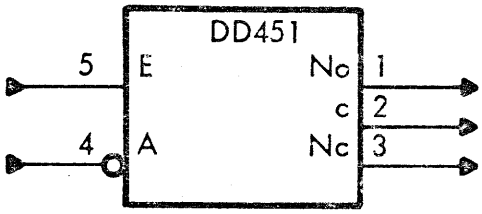
Response time (V in = 100 mV)	typ. 40 nS
Enable .elease time	typ. 12 nS

NOTES

1) Input 14 is connected to 3 circuits and will therefore take 3 times the specified load.

2) The values are valid only when output 5 is left floating.

DD451



CIRCUIT DESCRIPTION

The DD450 is a gated relay driver with relay.

The relay is activated when the E input is high and the A input has been low for more than app. 2 sec. The E input is disabled as soon as the relay is activated, and the realy is then solely controlled by the A input.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input levels		
E logical 1	open or $V \geq +4,3V$	Vmax.= +5,7V
logical 0	$V \leq 3,5V$	Vmin.= -10V
A logical 1	$V \leq +0,5V$	Vmin.= -4V
logical 0	$V \geq +1,6V$	Vmax.= 10V

Input loading	
E logical 1	max. -0,7 mA
logical 0	max. -5 mA
A logical 1	max. -30 uA
logcial 0	max. +10 mA

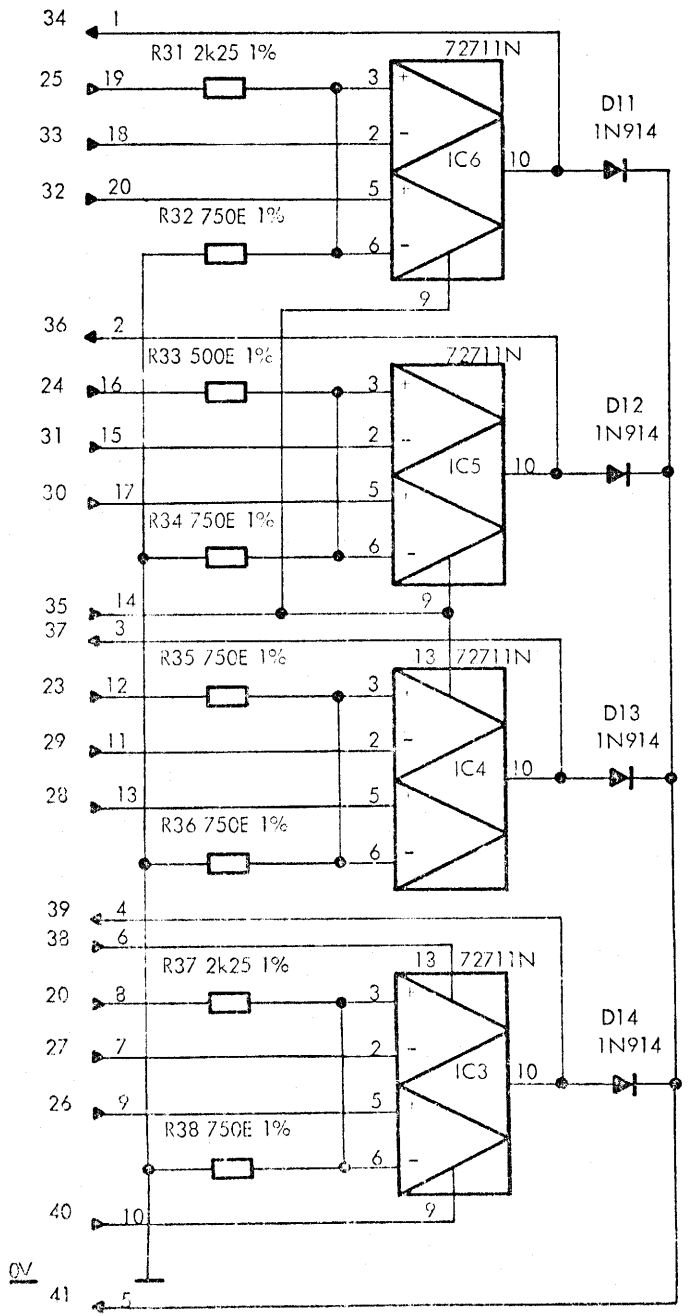
The sign is positive when current flows towards the circuit.

Output current	max. 2A at 30 VDC

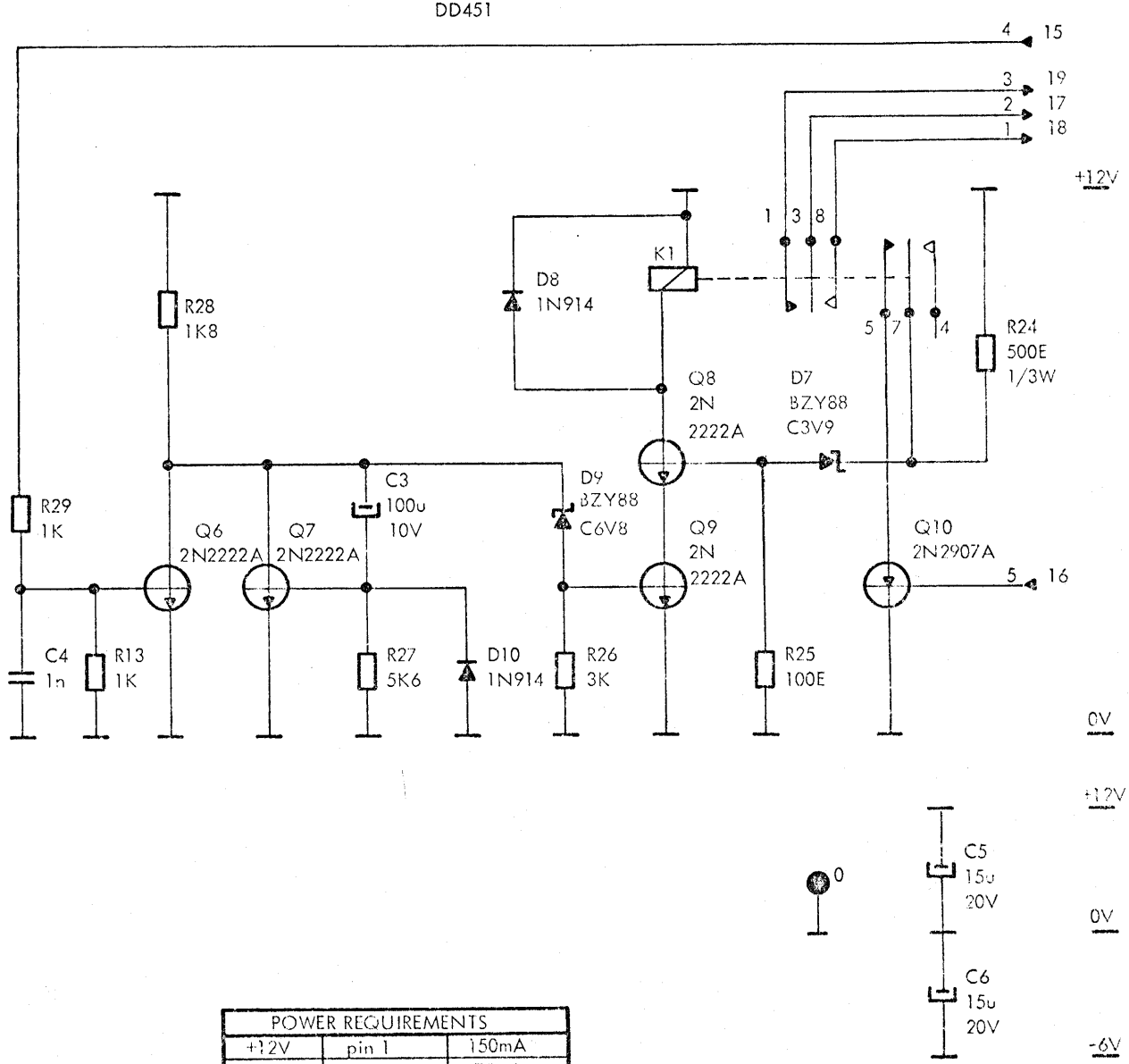
SWITCHING CHARACTERISTICS

Delay for operation	max. 5 mS
delay for release	max. 4 mS
Bounching	max. 2 mS

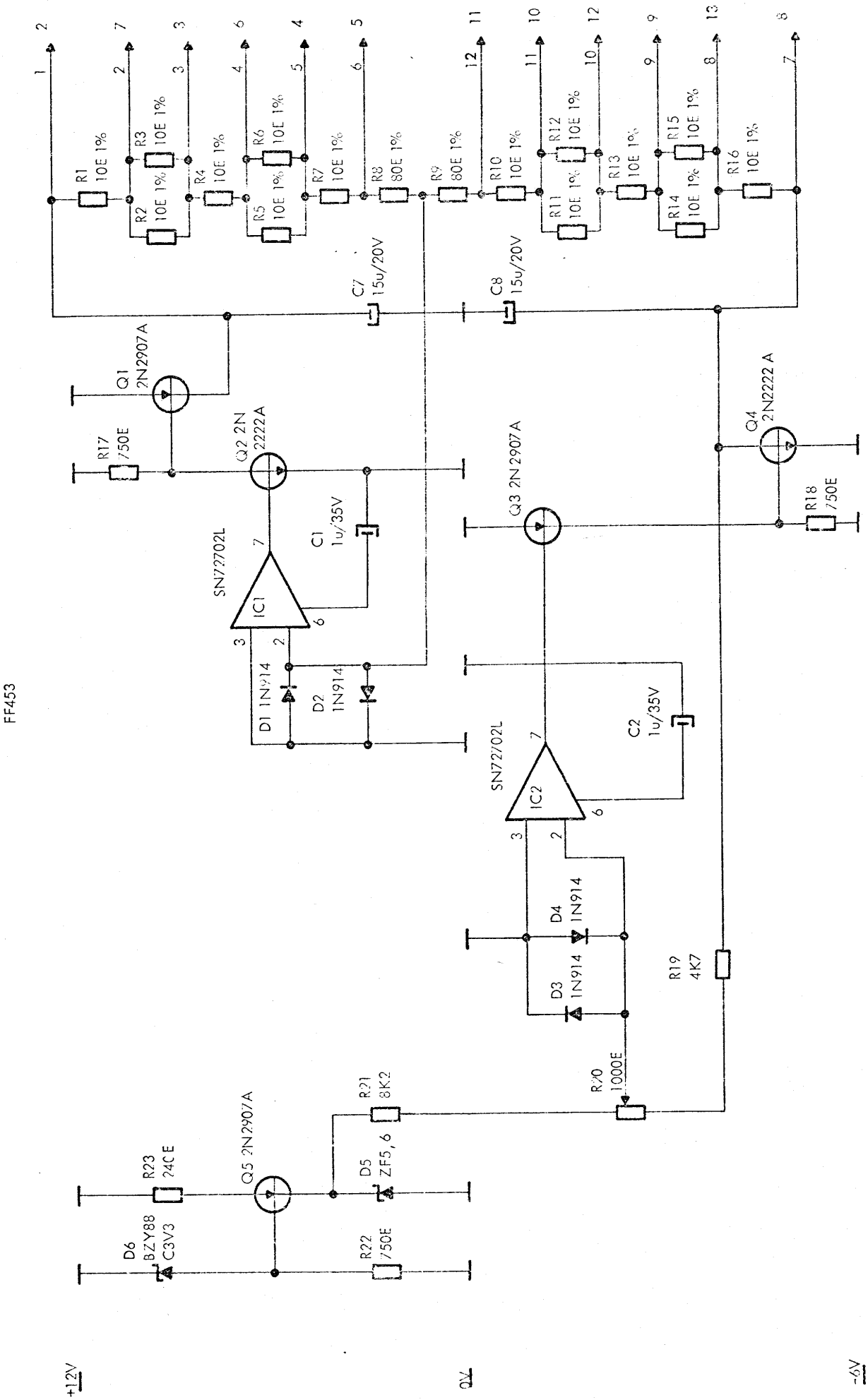
FF452

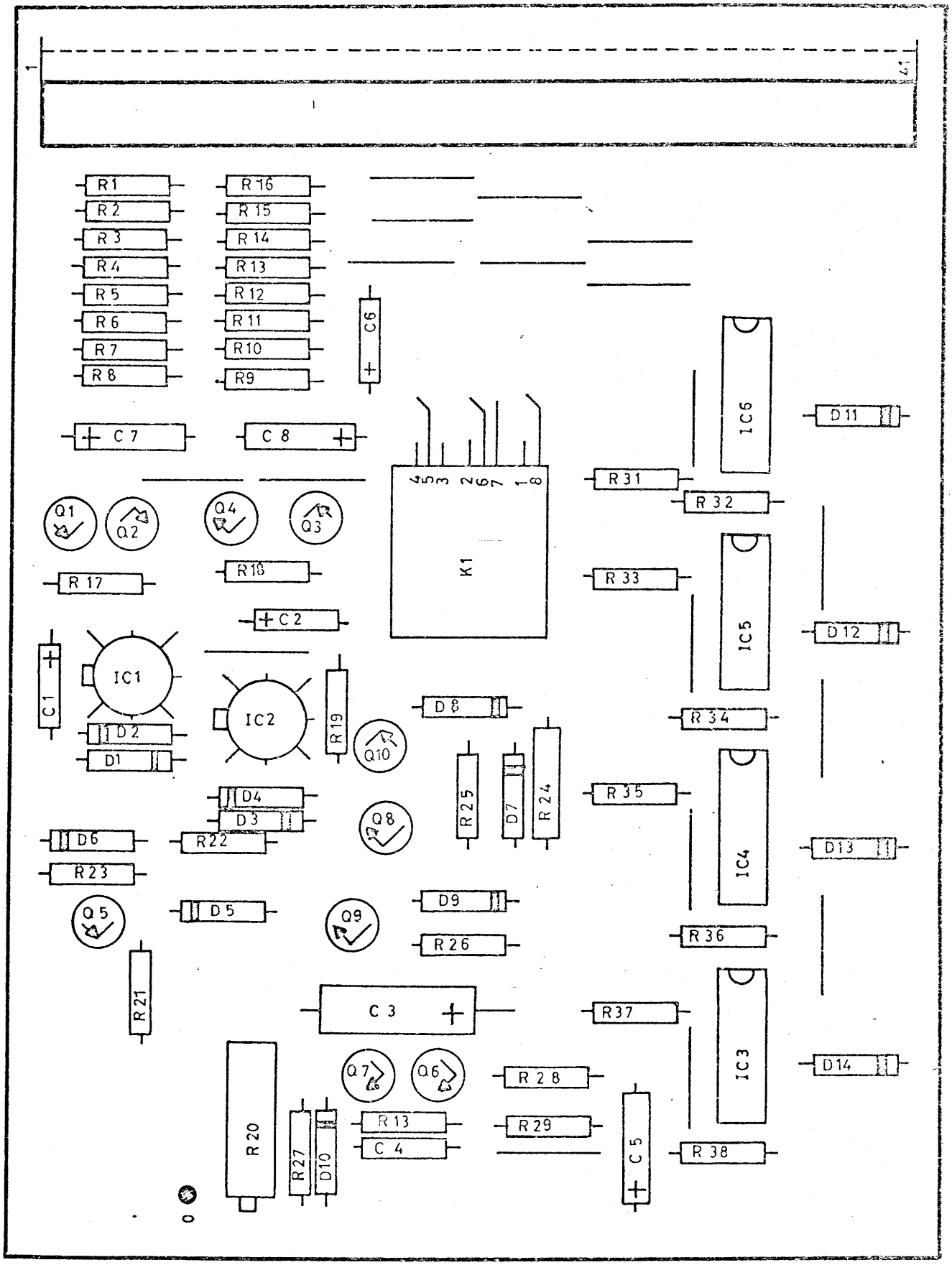


DD451



POWER REQUIREMENTS		
+12V	pin 1	150mA
-6V	pin 14	78mA
0V	pin 21	
Power Dissipation 2410mW		


FF453
R1 10E 1%
R2 10E 1%
R3 10E 1%
R4 10E 1%
R5 10E 1%
R6 10E 1%
R7 10E 1%
R8 80E 1%
R9 80E 1%
R10 10E 1%
R11 10E 1%
R12 10E 1%
R13 10E 1%
R14 10E 1%
R15 10E 1%
R16 10E 1%
C7 15u/20V
C8 15u/20V
Q1 2N2907A
Q2 2N 2222A
Q3 2N2907A
Q4 2N2222 A
R17 750E
R18 750E
SN72702L
IC1
C1 1u/35V
D1 1N914
D2 1N914
SN72702L
IC2
C2 1u/35V
D4 1N914
D3 1N914
R19 4K7
R20 1000E
R21 8K2
Q5 2N2907A
R23 24C E
D5 ZF5,6
D6 BZY88 C3V3
R22 750E
+12V
0V
-6V

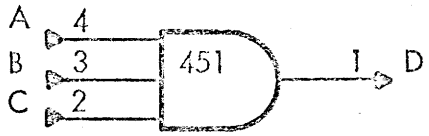


RCLM400 1 FF453, 1 FF452, 1 DD451 RC3066-6

R 20204 PCB Assembly Drawing

RCSL : 52-AA209
pp. 1 : 1
JULY 1970
Replaces 52-AA98

AA451



CIRCUIT DESCRIPTION

The AA451 is a 3-input AND-element the inputs of which are able to drive wired-OR-gates consisting of up to 8 inputs

D = A & B & C

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	4 unit Loads (each input)
Fan out	10 unit Loads

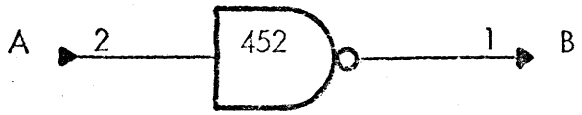
SWITCHING CHARACTERISTICS

Propagation Time

From A, B, or C to D	td(1)	Max. 60ns
	td(0)	Max. 44ns

RCSL : 52-AA173
pp. : 1 : 1
FEBR. 1970

AH452



CIRCUIT DESCRIPTION

The AH452 is a logic inverter.

$B = \overline{A}$

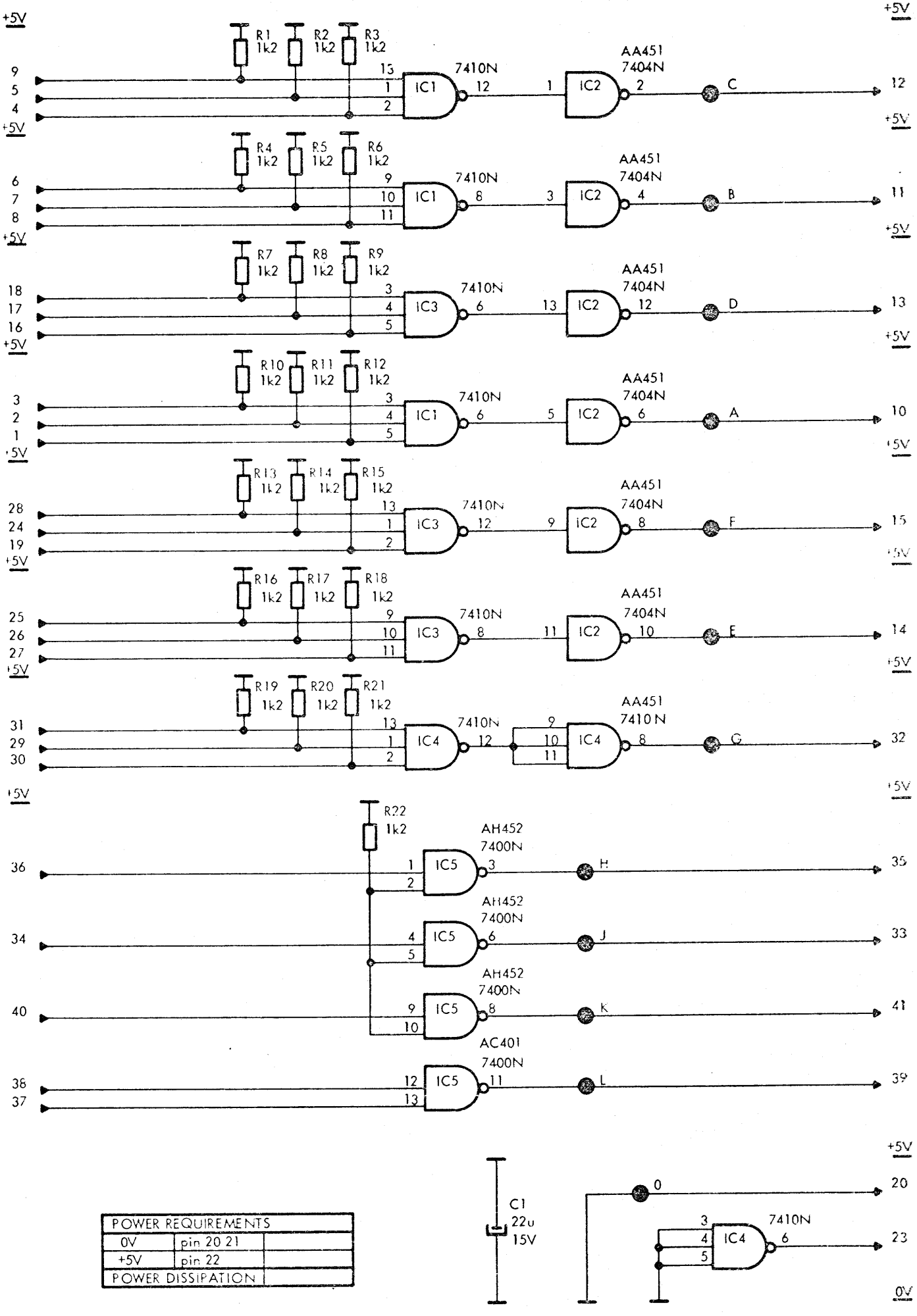
SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Input Loading	1 unit Load
Fan out	10 unit Loads

SWITCHING CHARACTERISTICS

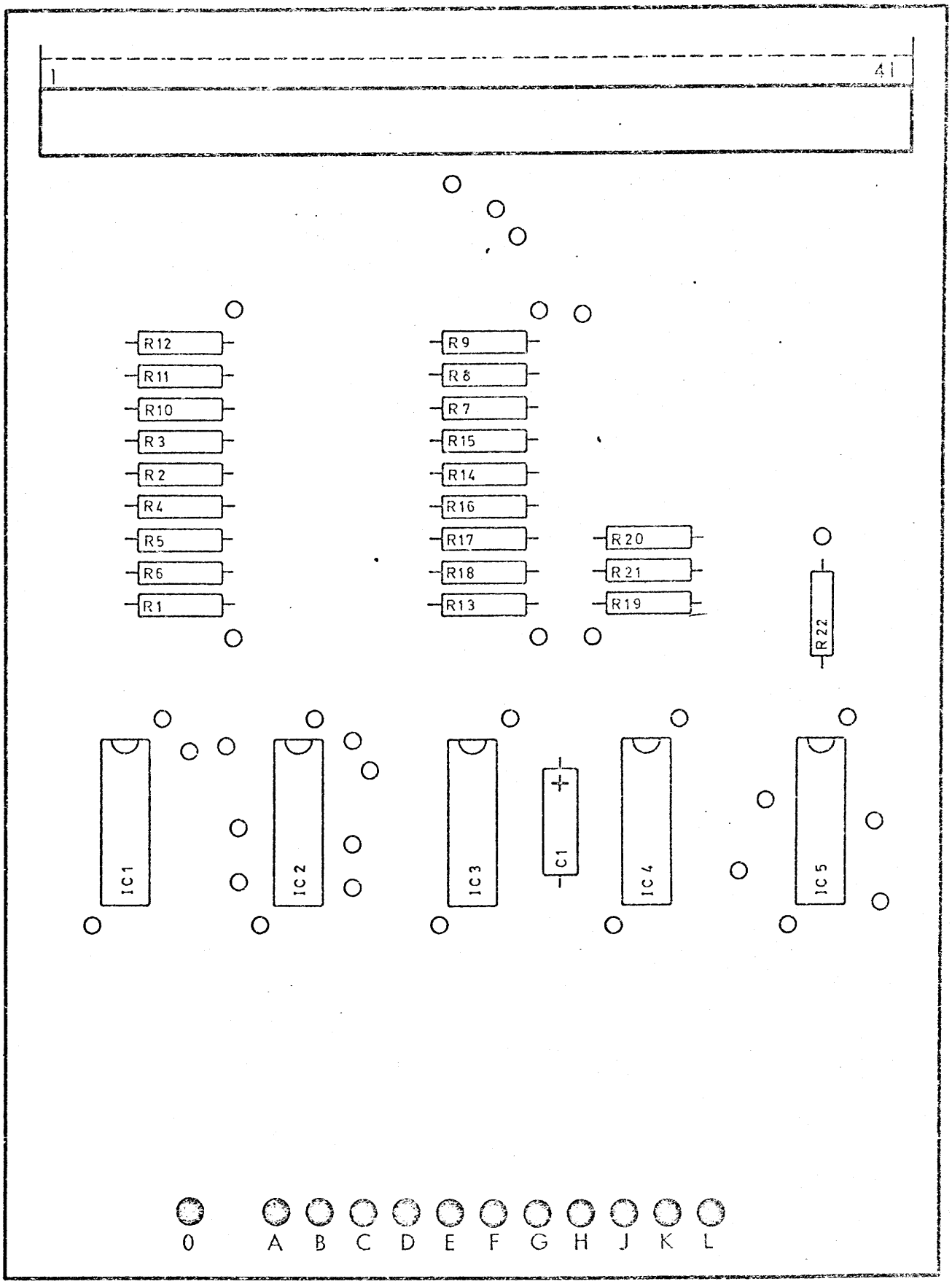
Propagation Time td(1) : Max. 15nS
td(0) : Max. 22nS



POWER REQUIREMENTS		
0V	pin 20 21	
+5V	pin 22	
POWER DISSIPATION		

RCLM400 — 7 AA451, 3 AH452, 1 AC401 — RC3125-1

R10095 — PCBA Circuit Diagram



RCLM400 7 AA451, 3 AH452, 1 AC401 RC3125-1

A21245 PCB Assembly Drawing

RCLM400

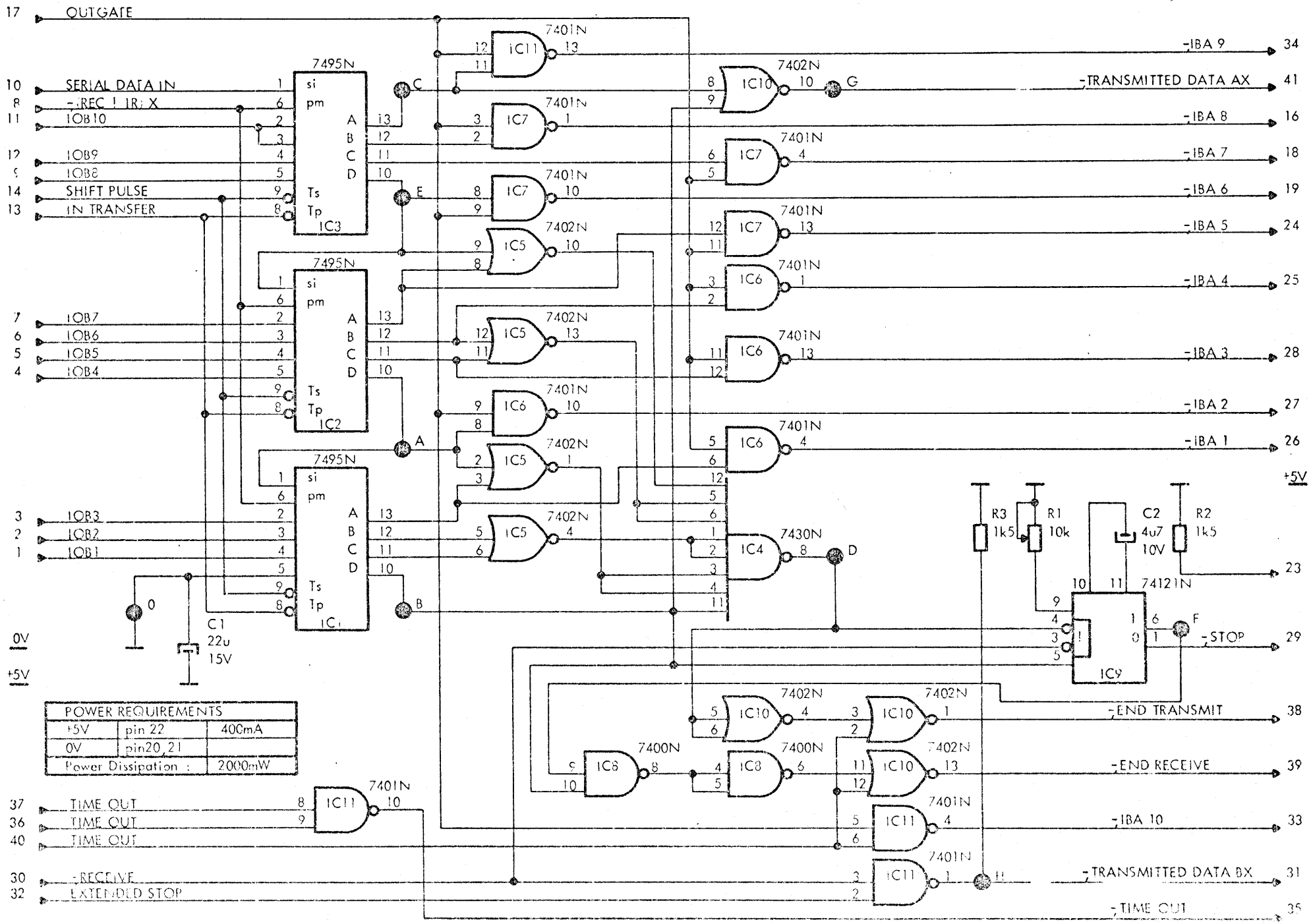
A10896

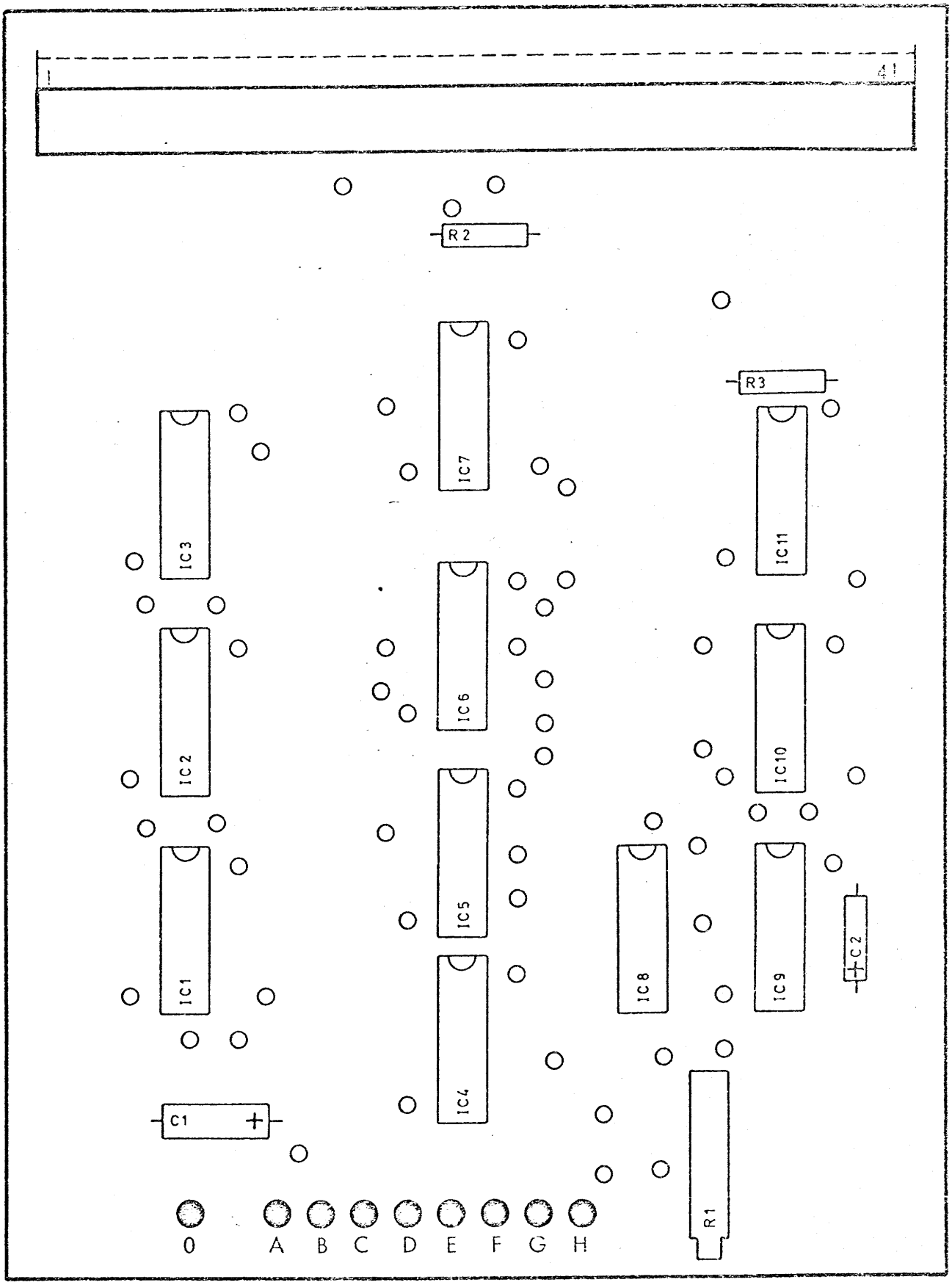
TELETYPE TRANSMIT RECEIVE REGISTER

1SA451

PCBA Circuit Diagram

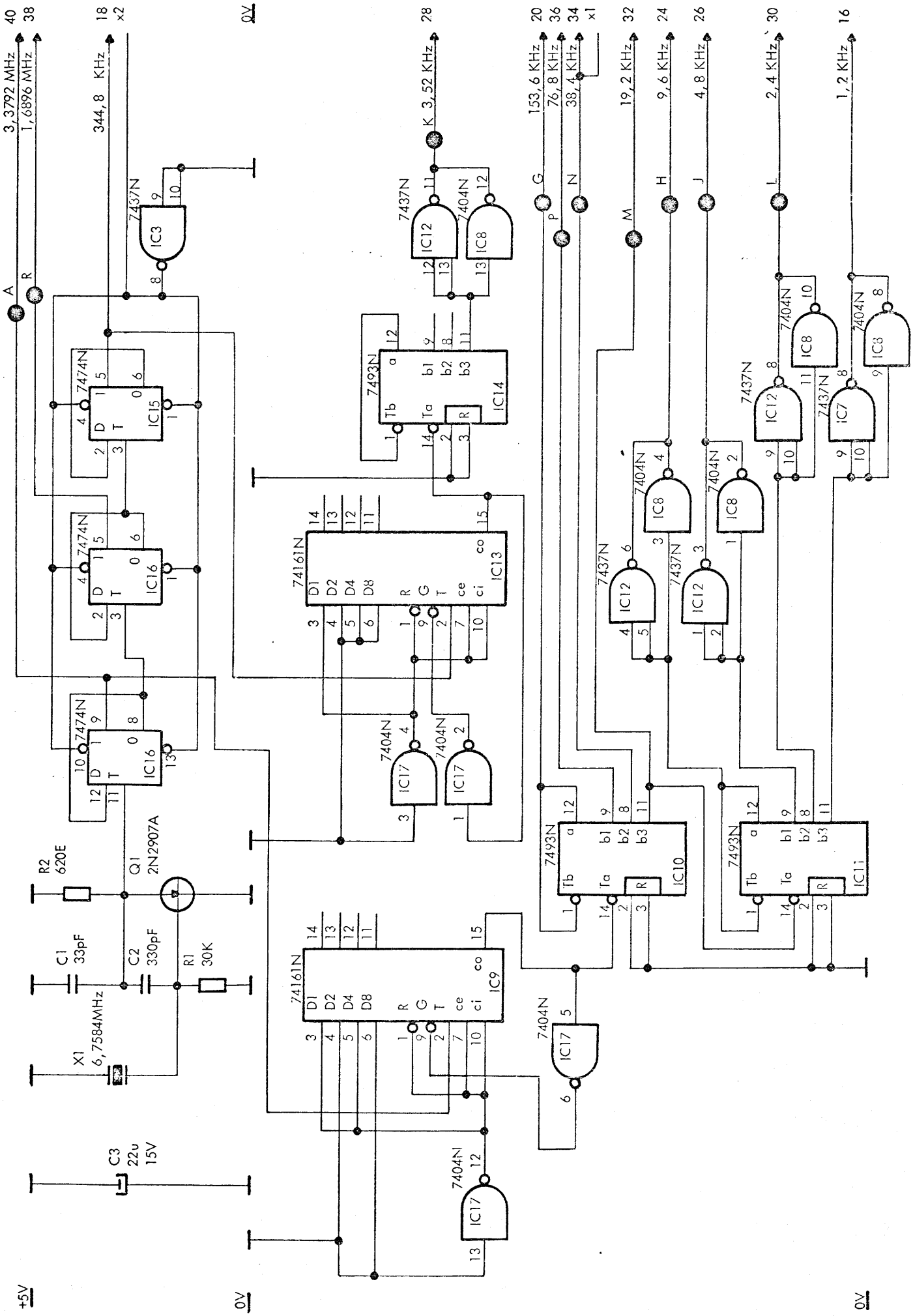
RC3123-1





RCLM400 1 SA451 RC3128-1

A21248 PCB Assembly Drawing

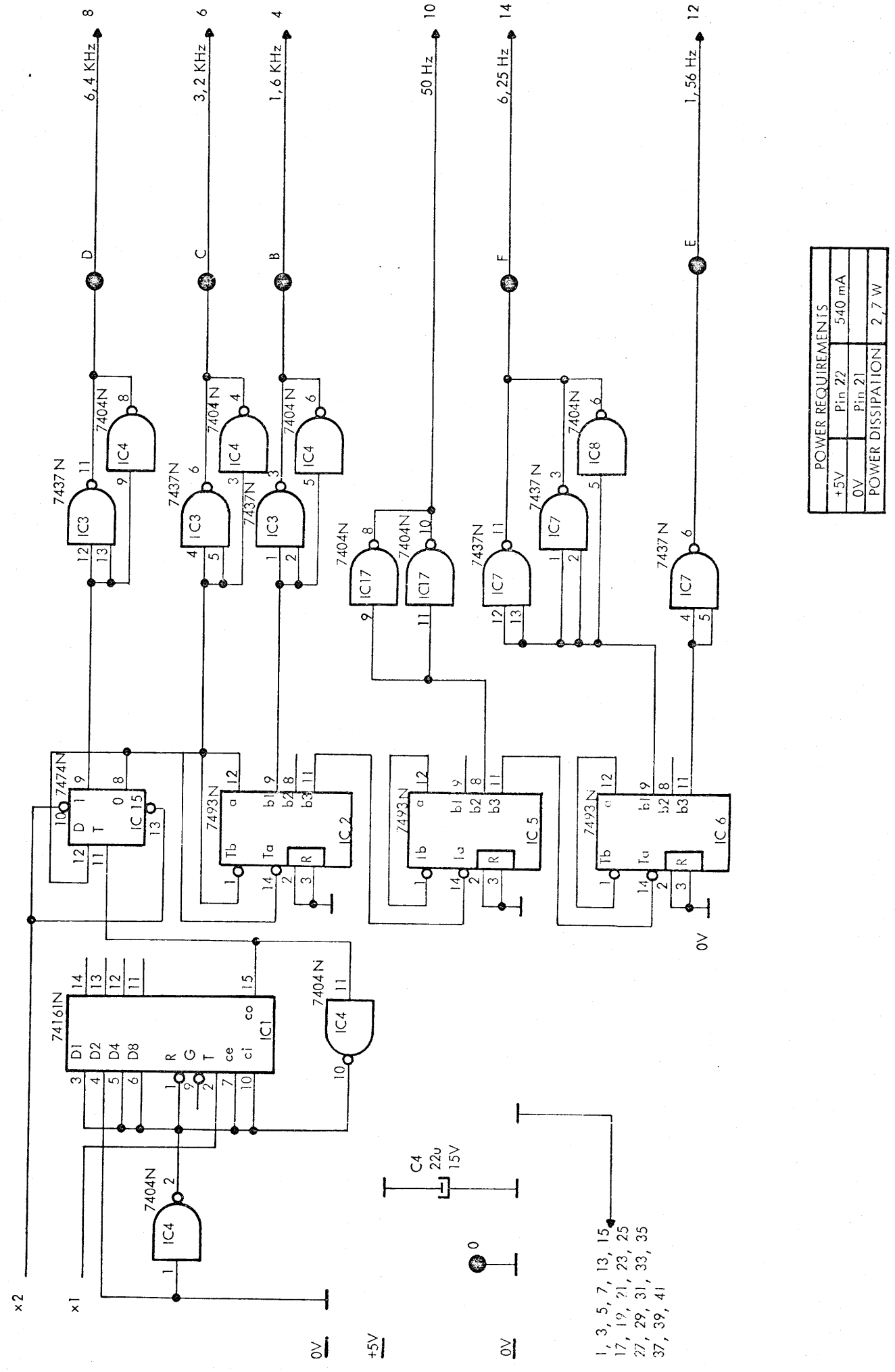


MTMX OSCILLATOR CARD OSCILLATOR AND FREQUENCY DIVIDERS

RC3140-1
pl of 2

A11007

PCBA Circuit Diagram



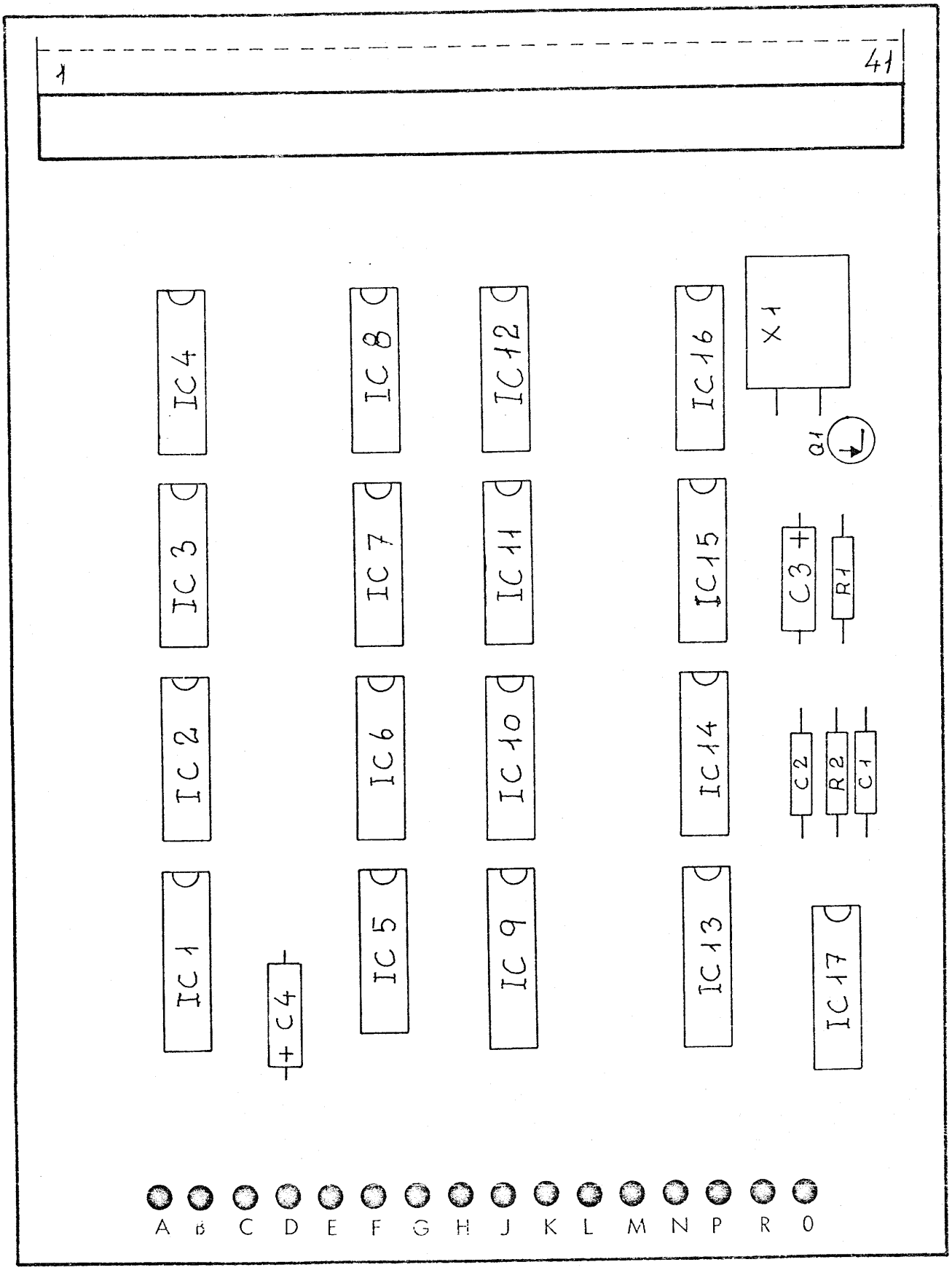
POWER REQUIREMENTS		
+5V	Pin 22	540 mA
0V	Pin 21	
POWER DISSIPATION		2,7 W

MTMX OSCILLATOR CARD FREQUENCY DIVIDERS

PCBA Circuit Diagram

A 11008

RC3140-1
p2 of 2

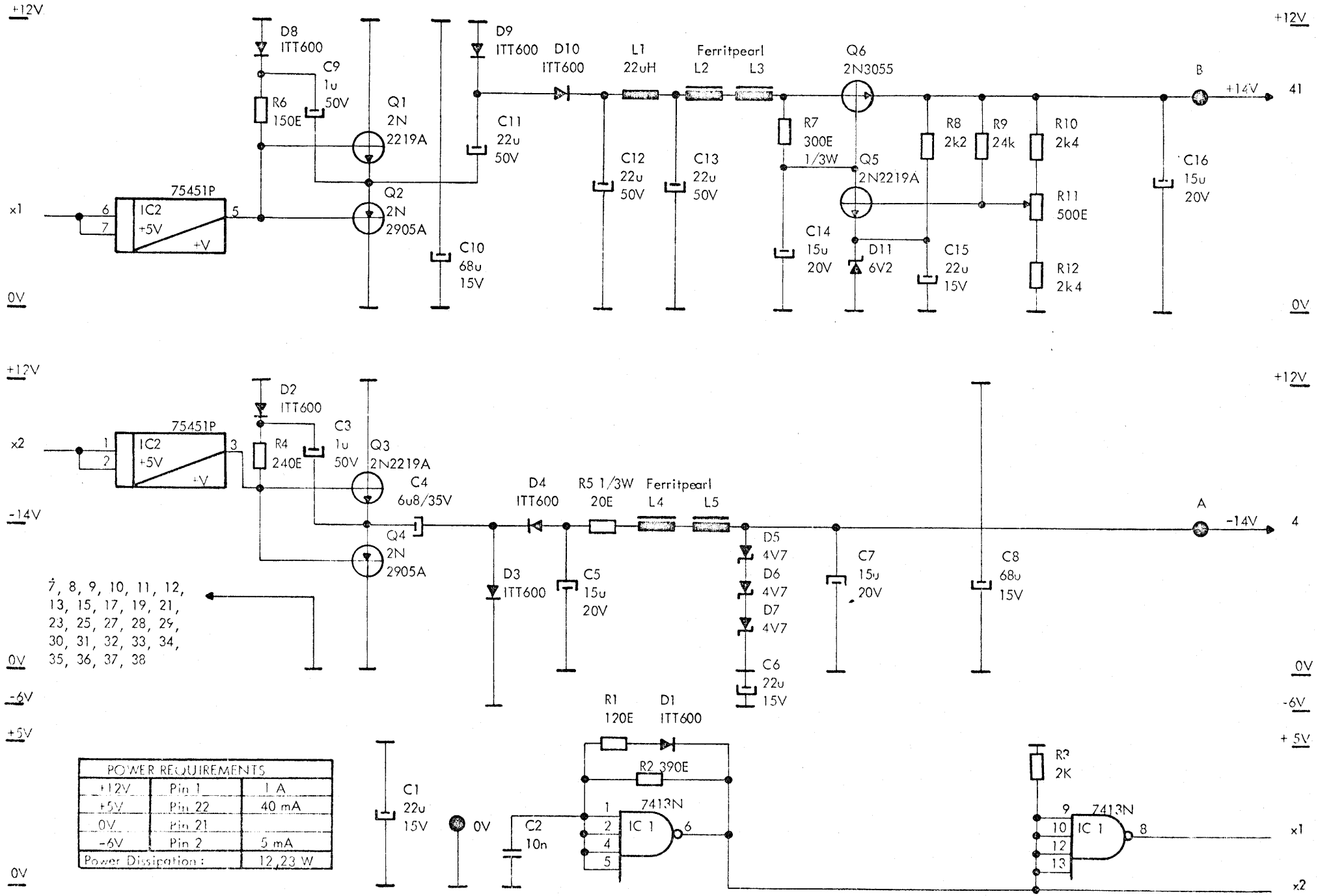

1
41
IC4
IC8
IC12
IC16
X1
Q1
IC3
IC7
IC11
IC15
C3
R1
IC2
IC6
IC10
IC14
C2
R2
C1
IC1
C4
IC5
IC9
IC13
IC17
A
B
C
D
E
F
G
H
J
K
L
M
N
P
R
0

RC3140-1

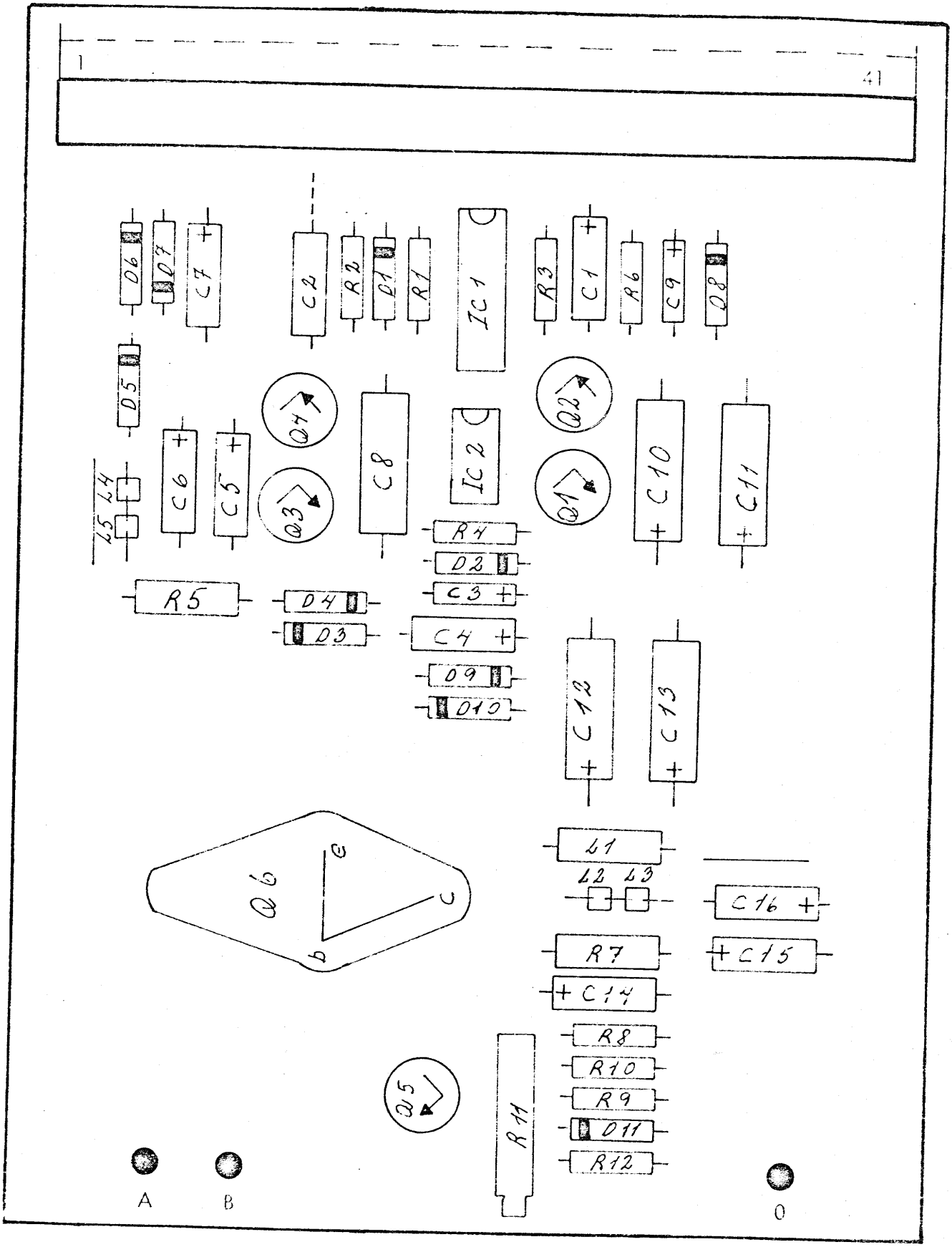
A11187

DC - DC CONVERTER
+12V/-6V, +14V/-14V
FCBA Circuit Diagram

RC3160-1



POWER REQUIREMENTS		
+12V	Pin 1	1 A
+5V	Pin 22	40 mA
0V	Pin 21	
-6V	Pin 2	5 mA
Power Dissipation :		12,23 W



RC3160-1

A21605

PCB Assembly Drawing

A/S REGNECENTRALEN

SCANDINAVIAN INFORMATION PROCESSING SYSTEMS

HEADQUARTERS: FALKONER ALLÉ 1 . DK-2000 COPENHAGEN F . DENMARK
TELEPHONE: (01) 105366 . TELEX: 6282 RCHQ DK . CABLES: REGNECENTRALEN