DATAMATICS

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RC 4320 MAGNETIC DRUM STORE CONTROLLER.

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RC 4320 MAGNETIC DRUM STORE

Technical Manual

for

Drum Controller, DRC 401

A/S REGNECENTRALEN
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CONTENTS:

1. SPECIFICATIONS.

Capacity	65,536 words expandable in modules of 65,536 words up to 524,288 words.
Transfer Rate	50,000 words/sec.
Word Size	24 bits
Segment Size	256 words
Block Size	Variable numbers of segments.
Mean Access Time	10.5 msec.
Transfer Time	5.2 msec./segment
Mean Time for Access and Transfer of a block containing n Segments	(10.5 + n×5.2)msec.
Reliability	Drum bearing life exceeds 100,000 hours of operation. Mean time between failures is 15,000 hours.
Power Supply	220 V ±10 per cent, 50 Hz ±4 per cent max. line current 6A operating current 1A
Power Dissipation	120 kcal/hour inside the drum can.
Temperature Range	10 degrees C to 50 degrees C surface temperature of can.
Drum Size	Width: 483 cm (19 inches) Depth: 580 cm Height: 650 cm
Controller Size	One 3-row unit mounted in the controller cabinet.

2. LOGICAL STRUCTURE.

This chapter describes the logical structure of RC 4320 Magnetic Drum Store used in connection with the RC 4000 Computer.

2.1. Main Characteristics.

The minimum drum capacity is 64K words of 24 bits each. The capacity can be extended in modules of 64K words up to a maximum of 512K words. The drum is divided into segments of 256 words each. It can transfer a data block consisting of a variable number of segments directly to or from the internal store. The average block transfer time in milliseconds is:

$$10.5 + 5.2 \times \text{number of segments}$$

The drum operates on the high-speed data channel, but uses the low-speed data channel to transfer commands and control parameters to or from the working registers. Protection keys are not stored in the drum.

2.2. Commands.

The drum controller accepts sense and control commands, the latter with four modifications.

In the input/output instruction specifying the sense command, the value of the modifier field, i.e. bits 18-21 in the effective address, is irrelevant.

The use of read commands, write commands, and other modifications of the control command than specified has no effect at all.

2.3. Control Commands.

The following control commands are available:

5	transfer first	<first segment>
9	transfer size	<number of segments>
13	input	<first storage address>
17	output	<first storage address>

The integers denote the values of bits 18-23 in the effective address of the input/output instruction. The parameters in the brackets AND denote the contents of the working register selected by the input/output instruction.

The parameters first segment, number of segments, and first storage address are interpreted modulo 2048, 512, and 262 144, respectively. The rightmost bit in the parameter, first storage address, is ignored. Thus it is irrelevant whether the parameter refers to the left or the right half of the storage word.

2.4. Input and Output.

The input or output of a block requires three control commands.

Two transfer commands are used to define the first segment and the number of segments on the drum.

One input or output command initiates the transfer defining the first address of the storage buffer.

After the initiation of input or output, the drum is busy until the operation is either completed successfully or terminated by an error condition. The drum delivers an interrupt signal when it becomes available.

2.5. Sense Command.

When the drum is available, a status word can be transferred to a working register by means of a sense command.

The status bits have the following meaning:

status bit 0:	(not used = 0)
status bit 1:	parity error
status bit 2:	synchronization error
status bit 3:	data overrun
status bit 4-23:	(not used = 0)

Parity error indicates a parity error in one or more data words during the transfer.

Synchronization error indicates a parity error on the block track of the drum. This is a serious hardware malfunction.

Data overrun indicates overloading of the high-speed data channel due to which the block transfer immediately has been stopped.

3. HARDWARE STRUCTURE.

This chapter describes the hardware structure of the RC 4320 Magnetic Drum Store consisting of the drum VRC 1016 and the controller DRC 401. See fig. 1.

3.1. Mechanical Construction.

The drum is a Vermont Research Corporation type 1016 rotating memory drum with flying heads. The recording heads are mounted in head pads, each pad containing 16 active data heads. At running speed, the head pads fly on a hydrodynamic air bearing formed by the laminar film of air close to the rotating drum surface. The head pads are supported in groups of four on the head bars. Thus a head bar contains 64 data heads. Up to eight head bars can be mounted on the drum giving a maximum of 512 heads. This is equivalent to 512 tracks each containing four segments of 256 data words of 24 bits.

Segment addressing (see DRC 023, 021, 007, 035, 036) is carried out in this way:

bit 13	specifies first second group selection circuits.
bit 14-15	specifies the selected head bar in the group.
bit 16-17	specifies the selected head pad in the head bar.
bit 18-21	specifies the selected data head in the head pad.
bit 22-23	specifies the selected sector on the track, and therefore they are not supplied to the drum.

The selection diodes, address lines and head pad selection circuits, are mechanical situated on the head bars inside the drum can, but the rest of selection as well as the reading and writing amplifiers are situated in an 11-position card frame with the drum base plate.

The drum and the drum controller are connected via one multicable (see DRC 006, 023, 004) containing all signals to and from the drum and also the d.c. supply voltages to the drum electronic. The 220V a.c. for the drum is supplied directly from POW406 via another cable, see fig. 1.

The Drum Controller DRC 401 is a 3-row sub-frame placed in the I/O controller cabinet, and connected to the low-speed bus and the high-speed bus.

3.2. Register Structure.

The drum controller registers can be divided into four groups, Data Registers, Drum Address Registers, Core Store Address Registers, and Control Registers. See fig. 2.

Data Registers:

WB(0:23) Word Buffer. Connected to the high-speed bus for parallel transport of 24-bit words between core store and register SP.

SP(0:23) Serial Parallel. Transfers the 24-bit words to serial during write operation, and converts the incomming data bits from serial to parallel during read operation.

PW(0:23) Parity Word. Twenty-four one-bit registers used to generate the parity word.

This data registers are implemented on 12 circuit cards, each containing 2 bits of the registers and two comparator circuits for comparing bit n and n+1 of WB and PW.

The data registers are shown on DRC 018, 019, 020 and the controlling and timing circuits on DRC 016, 017. The contents of the registers are given in the timing diagrams fig. 4 and 5.

Drum Address Registers:

DSA(12:23) Drum Store Address. When a block transport starts, it contains the address of the first segment that has to be transferred (see DRC 007, 035, 036). As long as NBS(15:23) is different from 0, the register is counted one up for each transferred segment.

DTA(0:8) Drum Track Address. This register controls directly the address lines to the drum, see DRC 021, 023). The contents is a copy of the contents of DSA(12:21) brought up to date in every sector gap.

Core Store Address Registers:

CSA(5:22) — Core Store Address. When a block transport starts, it contains the address of the first word that has to be transferred, see DRC 009, 010, 035, 036. The register is counted one up for each transferred word, see DRC 013.

Control Registers:

NBS(15:23) — Number of Segments. When a block transport starts, it contains the number of segments that has to be transferred in the block transport, see DRC 008, 035, 036. The register is counted one down for each transferred segment, see DRC 013.

Bit(0:4) — Bit Address Register. See DRC 015, 013, 012. A modulo 24 counter controlled by the clock pulse. It will shift every 800 nanoseconds.

Word(0:8) — Word Address Register. See DRC 014, 013, 012. A modulo 268 counter controlled by the clock pulse. It will shift every time Bit(0:4) goes from 23 to 0.

Sector(0:1) — Sector Address Register. See DRC 015, 013, 012. A modulo 4 counter controlled by the clock pulse. It will shift every time (Word(0:8), Bit(0:4)) goes from (257,3) to (257,4).

Time 000t150
Time 200t350
Time 400t550
Time 600t750

Timing Registers controlled by the clock pulse from the drum, see DRC 006. The Sector(0:1)conWord(0:8)conBit(0:4) register always indicates the rotational position of the drum. The register value is reset to (0,257,4) when the drum index pulse occurs, see fig. 3. When this has been done once, when the system was started, then this resetting should be unnessesary, because the 25728 clock pulses will automatically hold the register correctly synchronized with the drum. If this unnessesary synchronization occurs at array, other times than (3,257,3), or does not occur at all, this is detected as a synchronization error, see DRC 021.

Status(0:23) Status Register. See fig. 2. This register stores different types of errors that may occur from the moment a block transfer is initiated, see DRC 005. The status word can be transferred to the core store when the drum is ready by means of a sense command.
Status(1) indicates a parity error.
Status(2) indicates a synchronization error, or a too low drum speed, or prospectively an address error. (Address errors are only detected during input operations).
Status(3) indicates data overrun on the high-speed bus. (This may happen if so many high-speed devices operate simultaneously that a CYS Request from the drum is not answered within 18 microseconds. See fig. 6. Status(0) and Status(4:23) are 0.

3.3. Data Format.

On the drum the data are cyclically stored bit by bit, see fig. 4 and 5. The format of the data words is given in fig. 6. It is shown how half of the data bits are inverted during the transfer from high-speed bus to word buffer, WB(0:23), and how the same bits later on, when the recorded word has been read, are transferred from WB to the high-speed bus with their negated values. The reason for this is to increase the efficiency of the parity control system. On one track there are 4 sectors, each containing 256 data words and 12 other words giving a total of $4 \times 268 \times 24 = 25728$ bits. Identification of a certain bit is carried out by means of register Sector(0:1)conWord(0:8)conBit(0:4). If a track switching is nessesary for getting access to a segment, this track switching takes place between bit 3 and bit 4 in word 257. This is the beginning of the sector. Hereafter follows a Write/Read switching time equivalent to about four words. The following words are different from 0, and are used to synchronize the self-clocking peak detector. During reading operation, this preambler words which actually give the segment address are checked. Address checking takes place for word 267. The following words, numbered 0 to 255, contain the 256 data words, logically regarded as one segment. Hereafter follows word 256 containing the parity word. Then finally four bits of word 257 belong to the sector, but are not used for information.

3.4. Test Performance.

6 different types of functional controls and data checkings are carried out. The test results may be examined by means of a sense command, giving a 3-bit extract of the controller status. More detailed, the following are tested:

Speed Control (DRC 004) (Fig. 9,10)
The frequency of the main clock is detected, and, if it is above 95 per cent of normal frequency, the Drum Speed is OK. Otherwise, Status(2) will be set to logical 1. If an input/output operation is running, it will be stopped immediately.

Power Control (DRC 004)
All d.c. power supplies to the drum electronic as well as to the controller are controlled. If they are above approximately 90 per cent of nominal value, the DRC Power is OK. If not, no writing on the drum can be done, and the device will be disconnected.

When the two abovementioned signals are logically 1, a green lamp on the opertor control panel will switch on, indicating that device N (N is the wired-in device number of RC 4320) should be capable of handling data transports, see DRC 001.

Synchronization Control (DRC 021) (Fig. 3)
The controller counts the clock pulses from the drum. There must be exactly 25728 Read Strobes equally spread around the Clock Track. If not, Status(2) is set to logical 1.

Address Control (DRC 005) (Fig. 4)
In the head of every segment, the segment address is written. During Read operation, this number is compared with the address of the segment to be read. They must be equal, otherwise Status(2) is set to logical 1 and no data transport will be carried out.

Parity Control (DRC 005) (Fig. 5)

During writing a segment, a 24-bit parity word is generated. Bit n is the Boolean sum modulo 2 of all 1-bits in position n for the 256 data words and the segment address word. (Please notice that the data words are formed by the information on the high-speed bus by inverting some of the bits, see fig.6). The parity word is written immediately following the last data word. During reading, a parity word is generated in the same way, but now the data words are the readed words. Then this parity word is compared with the readed parity word. They have to be identical. Otherwise Status(1) is set to logical 1.

BUS Control (DRC 005) (Fig. 6)

Overloading of the high-speed bus will result in a too late response from the Core Store Controller upon Cycle Requests from the device. If this happens, Status(3) is set to logical 1, and further requests will not be sent. Drum Controller will give up and become ready, see DRC 001, 002.

3.5. High-Speed Bus.

Transports of data words via the high-speed data bus are initiated by a Cycle Stealing Request from the controller, see fig. 6. During writing, the CYS Request is sent one word time before the specified word location reaches the read/write head. During reading, the CYS Request is transmitted two-bit's time after the word has passed the head. In both cases, the central processor has to reply on the call, first by asking for the core store address and the direction of the data transfer, and then by sending a signal, HDCGiData, indicating the time interval in which data are to be gated on the high-speed bus, see DRC 030, 031. The whole procedure has to be terminated within 18 microseconds, otherwise it is too late. To prevent damage to the core store in case of bus overloading, the procedure is supervised, and, in case that the procedure is still in operation at the time it is too late for correct data handling, then the address and the data situation are frozen, the block transfer interrupted, no more CYS Requests transmitted, and Status(3) set to logical 1 indicating data overrun.

4. ADJUSTMENTS.

Two timing systems have to be adjusted in the DRC 401 controller: The basic clock pulse system which divides the bit time into four time intervals, and the speed control system which supervises the drum speed. Before any adjustments are carried out, the drum should have been running at least one hour to obtain thermal balance in the mechanical system so that the drum speed hereafter can be considered as constant.

4.1. Adjusting the Clock Pulses.

The Clock Pulses, Time 000t150, Time 200t350, Time 400t550, and Time 600t750 are to begin with adjusted so that their leading edges divide a bit time into 4 equal time intervals, see fig. 8 and DRC 006. Ta, Tb, and Tc are adjusted by means of potentiometers A, B, and C on the RC 0909-1M in position 5, and the trailing edge of the signal on testpoint D is adjusted with the potentiometer D. The adjustment tends to give Ta = Tb = Tc = Td = Tbit/4. When this has been done, the final adjustment is easiestly carried out while the RC 4000 is operating and the drum store frequently used in output operation.

Adjustment procedure:
Trig the oscilloscope with signal Time 000t150 (Pos. 5 Testpoint A) and observe signal WD and -,WD (Pos. 4 Testpoint B and C) in added mode. Adjust the timing by means of potentiometers A, B, C, and D on card position 5, so that Tm = Tn, Ta = Tb, Tc = Tbit/4, and Tg = 50 nanoseconds. Lock all four potentiometers.

4.2. Adjusting the Speed Control Circuit.

The Speed Control Circuit (See DRC 004) detects whether the clock frequency is higher than a certain minimum frequency fOK or not. If the frequency is higher than fOK, a short zero signal will set the drum speed OK flip-flop to 1, and if f is lower than fOK, another zero signal will reset the drum speed flip-flop to 0. Timing diagrams for their signals are given in fig. 10. For small variations, expressed in per cent, the length of the zero pulses is given by T = 38.4 × (fOK-f)/fOK microseconds. At normal speed, i.e. when the

drum has been running for at least one hour to stabilize the thermal conditions, the length of Th is adjusted to 38.4 × 0.05 = 1.92 microseconds. If the drum speed, hereafter, decreases below 0.95 × normal speed, the signal Drum Speed OK will go to 0. See fig. 11.

Adjustment procedure:
Adjust Te (pos. 5 Testpoint E) to 58 microseconds by means of potentiometer E on card position 5. Then adjust Th (pos. 30 testpoint H) to 1.92 microseconds by means of potentiometer F on card position 5. Lock both potentiometers.

4.3. Adjusting the Peak Detector.

The Peak Detector Circuit (see fig. 11) can be adjusted by means of the potentiometer on the circuit card in position 3 in the VRC electronic frame. Before any adjustments are carried out, one must be sure that the data on the tracks have been written correctly, i.e. the adjustment of the timing pulses has been done accurately.

The adjustment is carried out by reading random numbers from different segments, and by using an oscilloscope to observe the negative going signal on pin 16. By adjusting the potentiometer, or perhaps even by changing the values of capacitors C9 and C11, the length of the signal can be controlled. Find the minimum value, Tmin, and the maximum value, Tmax, for which readings are performed without parity errors, and then adjust the time to $T = Tmin + 0.4 \times (Tmax - Tmin)$. A powerful program tool for this operation is the testprogram, Read Check with Acoustics Alarm. Signal waveforms with time tolerances are given in fig. 7.

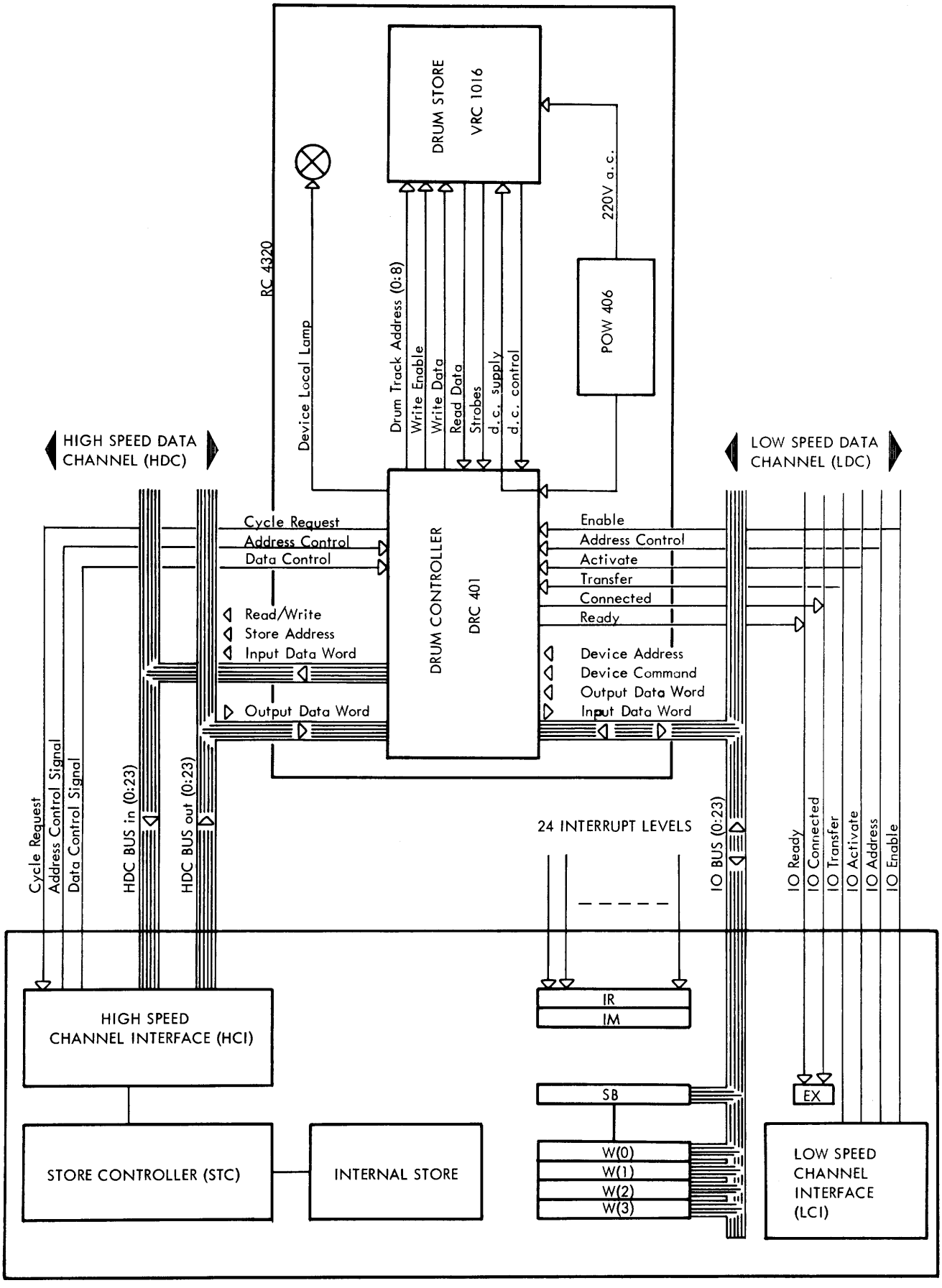


Fig. 1. Schematic diagram giving a functional description of the interconnections between the RC 4000 Computer, the Controller, and the Drum. It will be seen that RC 4320 is a standard High-Speed I/O Device controlled via the Low-Speed Channel and transferring data via the High-Speed Channel.

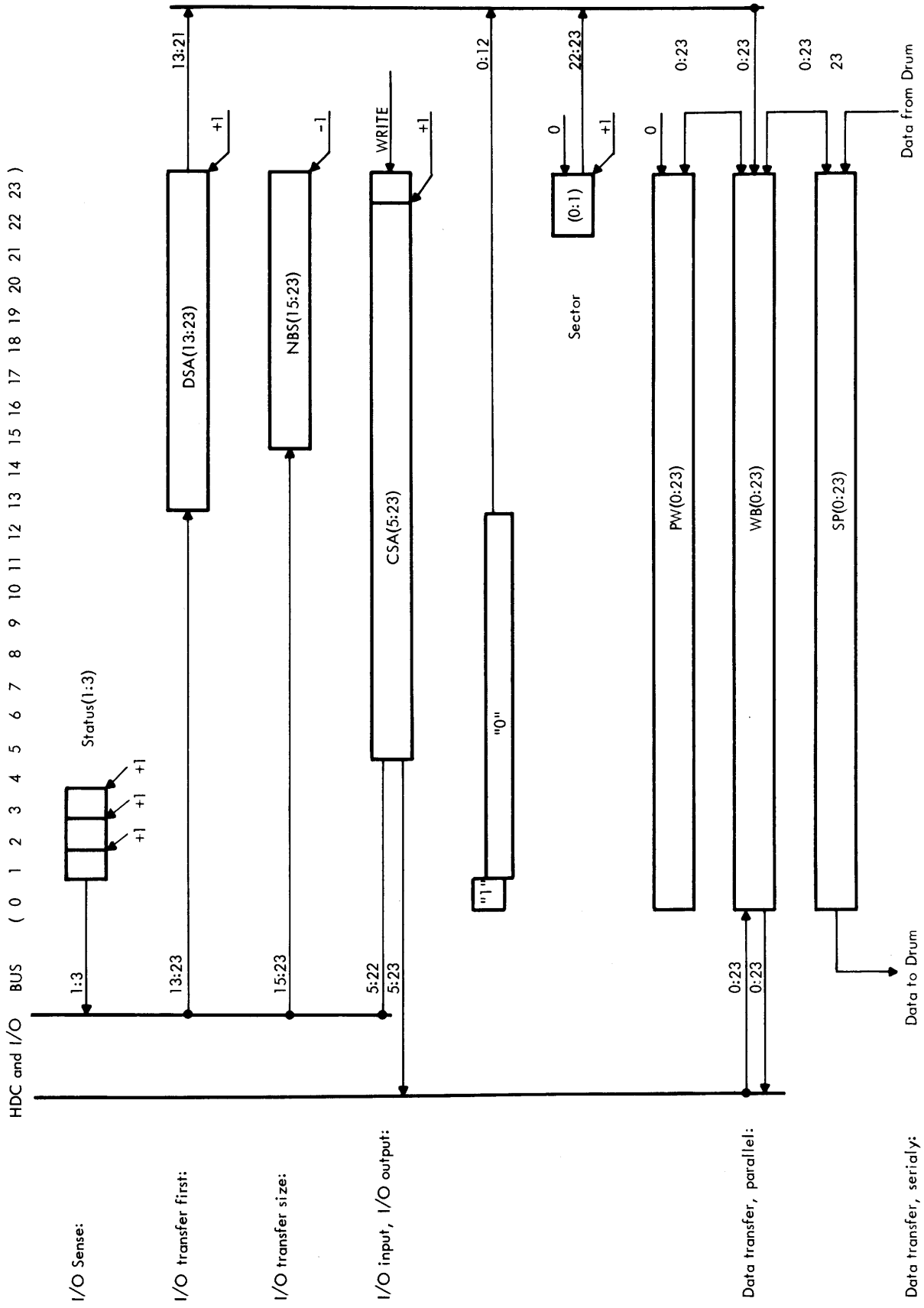


Fig. 2. Register structure for RC 4320. All registers having connections to or from Bus lines are shown as well as registers co-operating with the Word Buffer register. Other registers, such as word and bit counters or start stop logic elements, are not shown here.

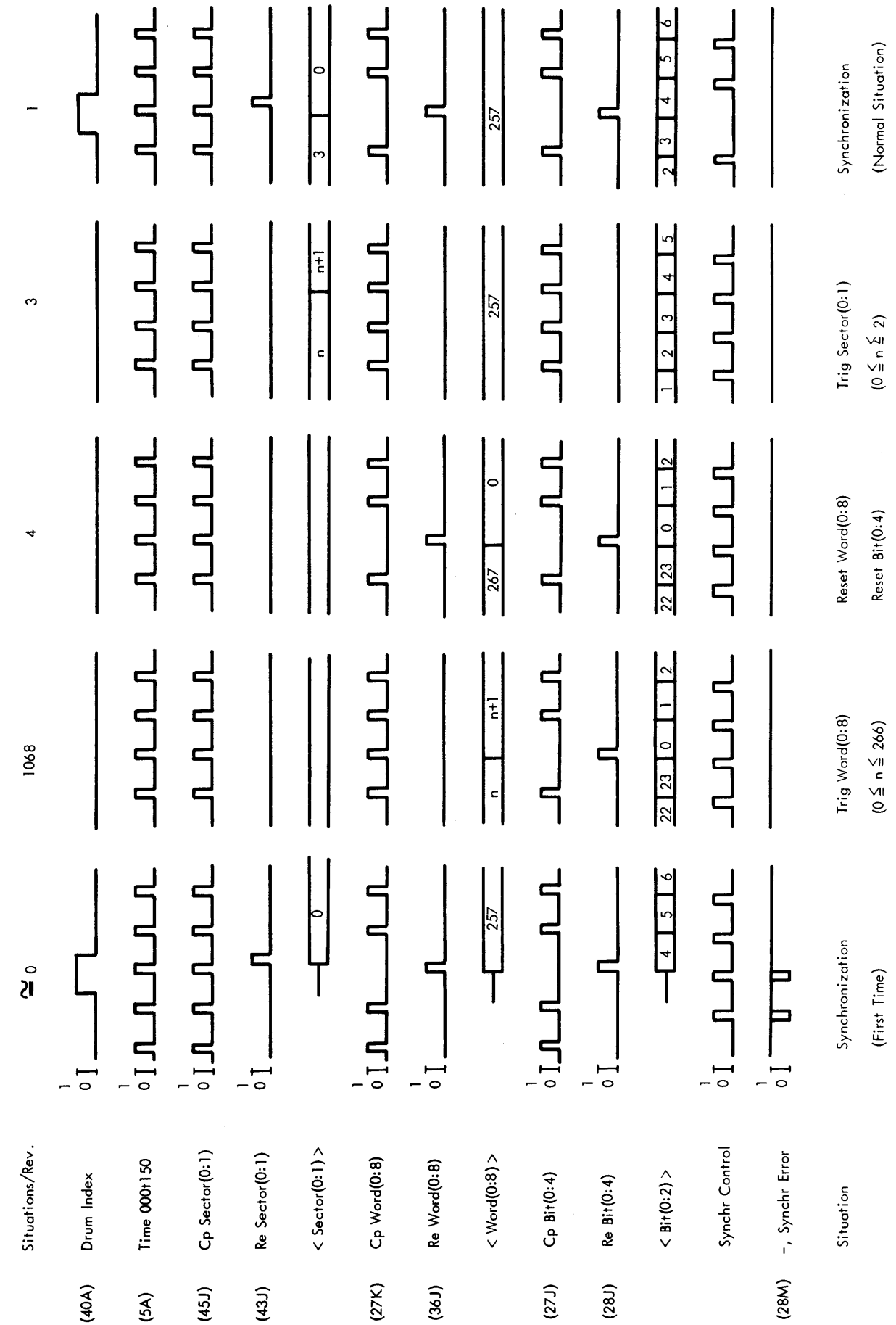
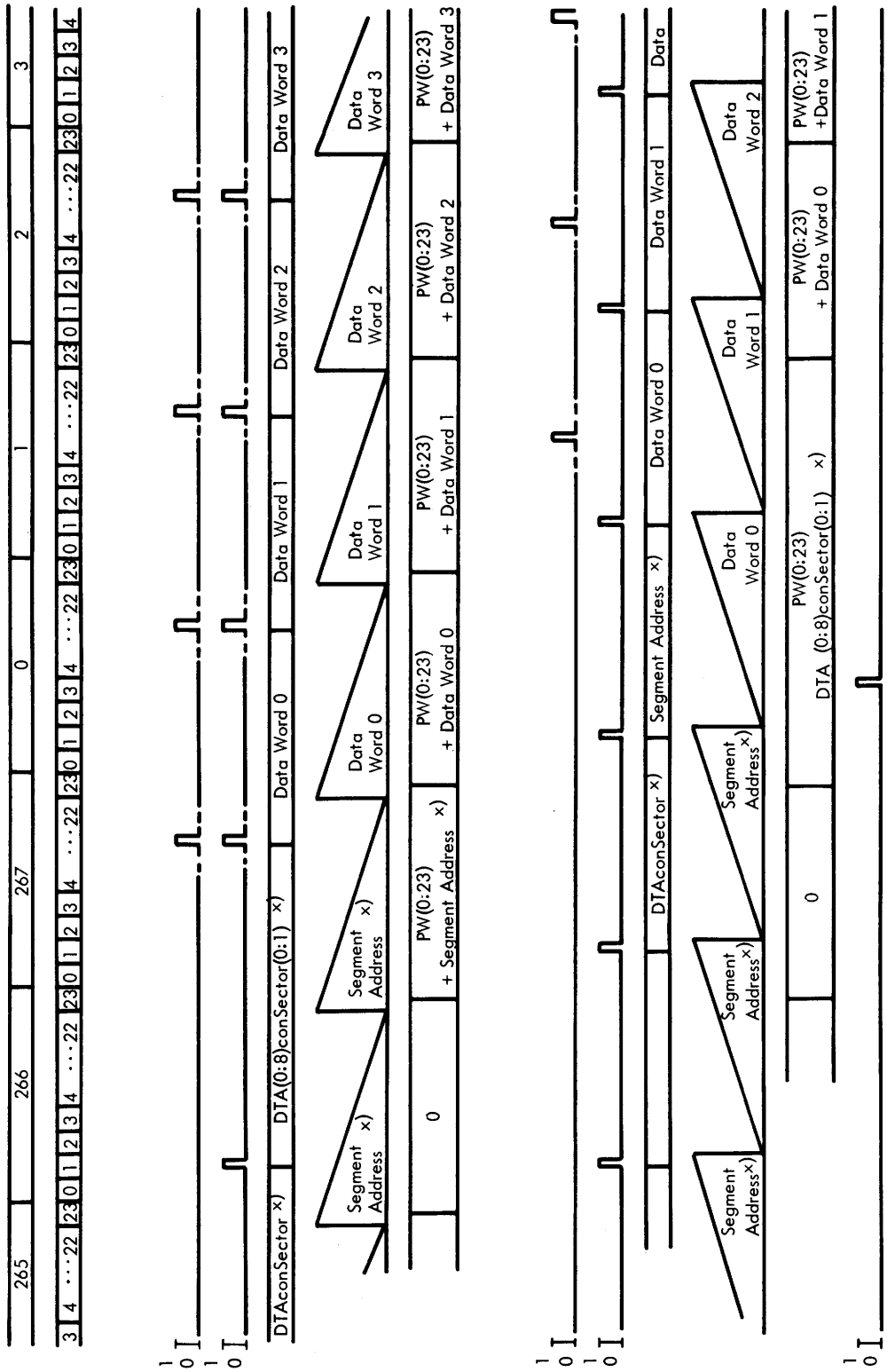


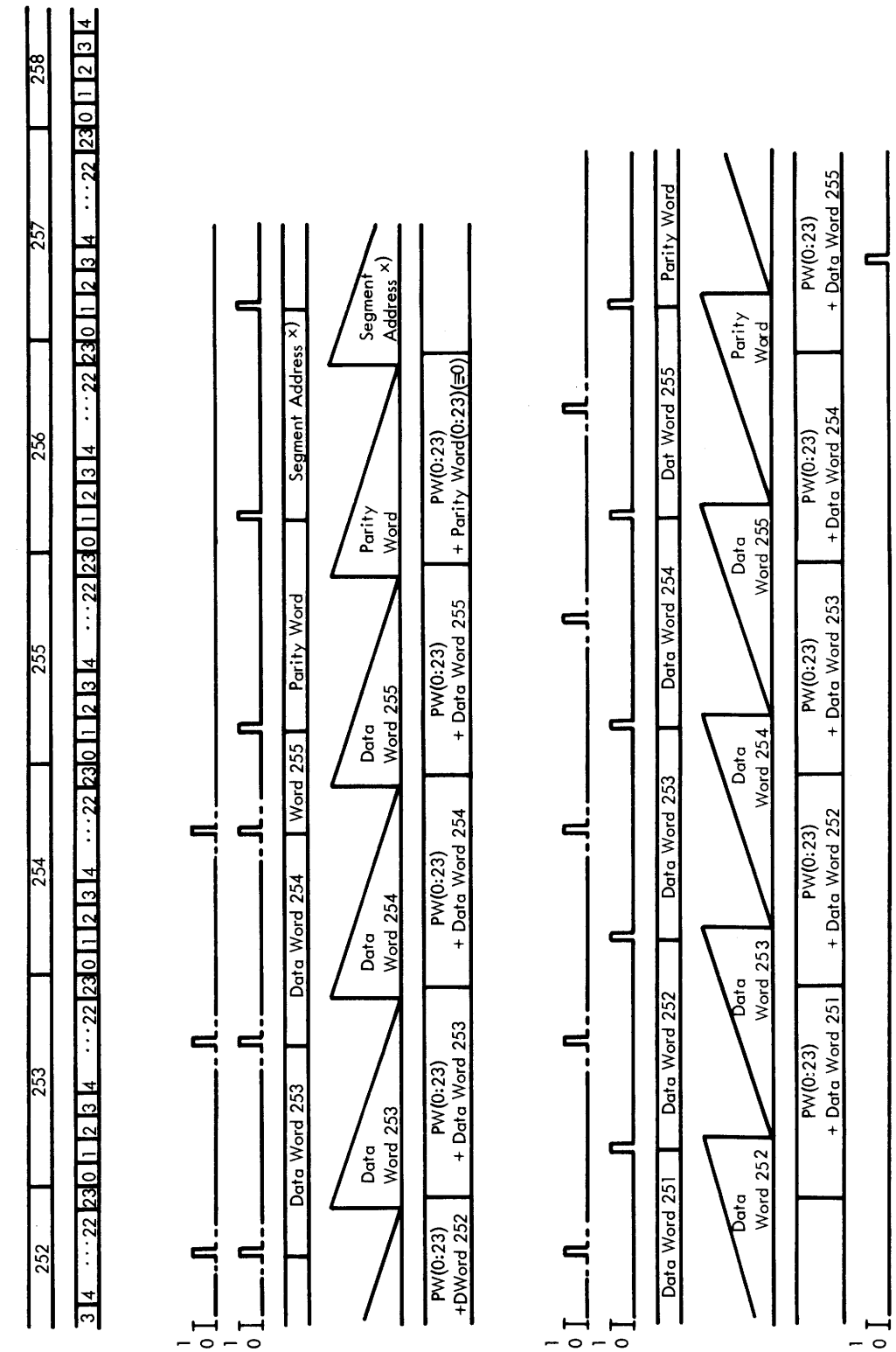
Fig. 3. Timing diagram for the Sector(0:1)conWord(0:8)conBit(0:4) register. The way it is synchronized from the drum index is indicated, and it is shown how the Sector register goes from 0 to 3, the Word register goes from 0 to 267, and the Bit register goes from 0 to 23.



x) And a "1" in position 0.

Timing Diagram for Data Transparts in the beginning of a Segment.

Fig. 4. Timing diagram for data transports in the beginning of segment transfer either to or from the drum. Register Word(0:8)conBit(0:4) acts as a time base. For the data registers, the contents, as well as shifting times, are indicated.



Timing Diagram for Data transparts in the end of a Segment

Fig. 5. Timing diagram for data transports in the end of a segment transfer either to or from the drum. Register Word(0:8)conBit(0:4) acts as a time base. For the data registers, the contents, as well as shifting times, are indicated.

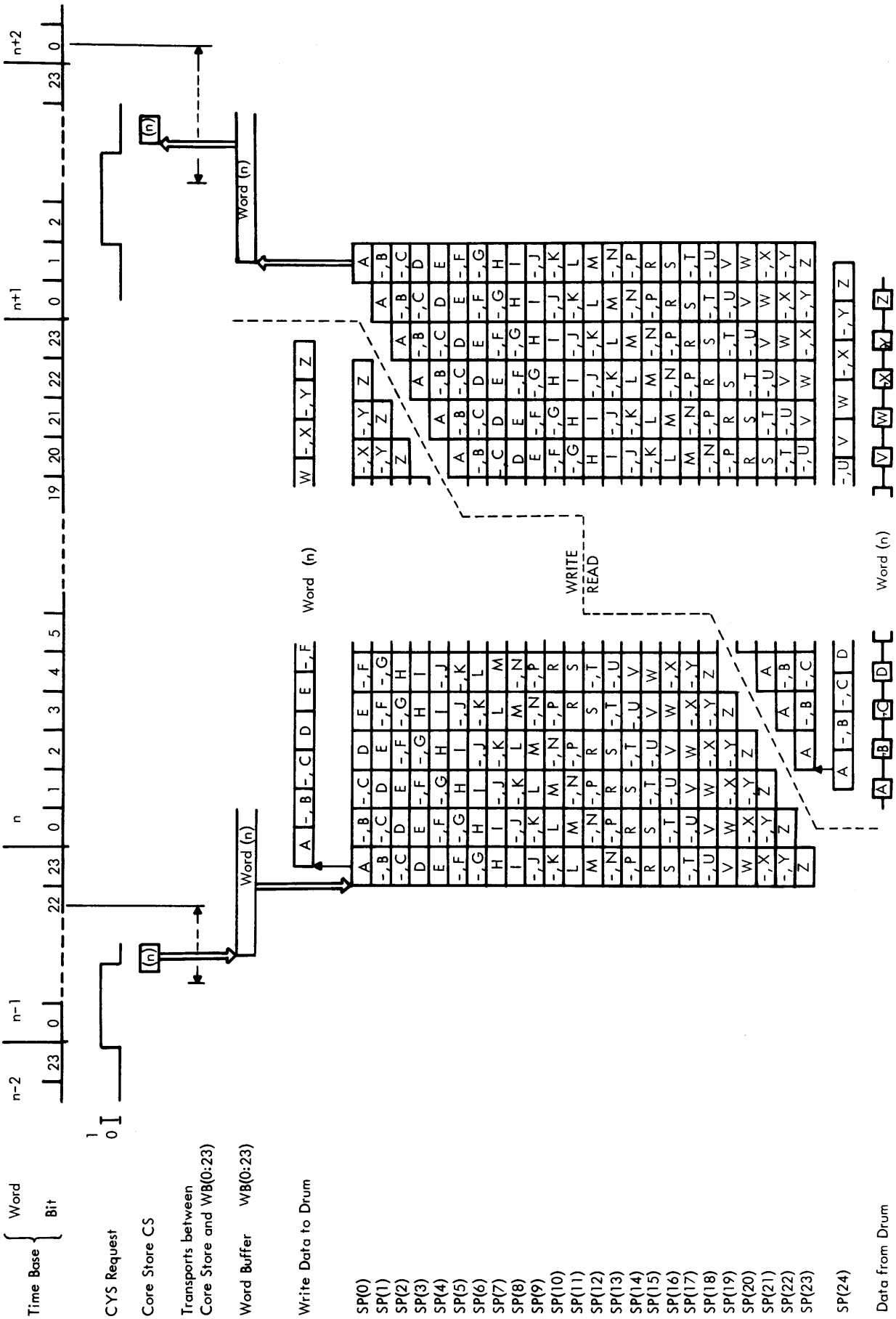


Fig. 6. Timing diagram for the data flow from Core Store via WB and SP to the drum track during writing operation, and from the track via SP and WB back to the Core Store during a reading operation.

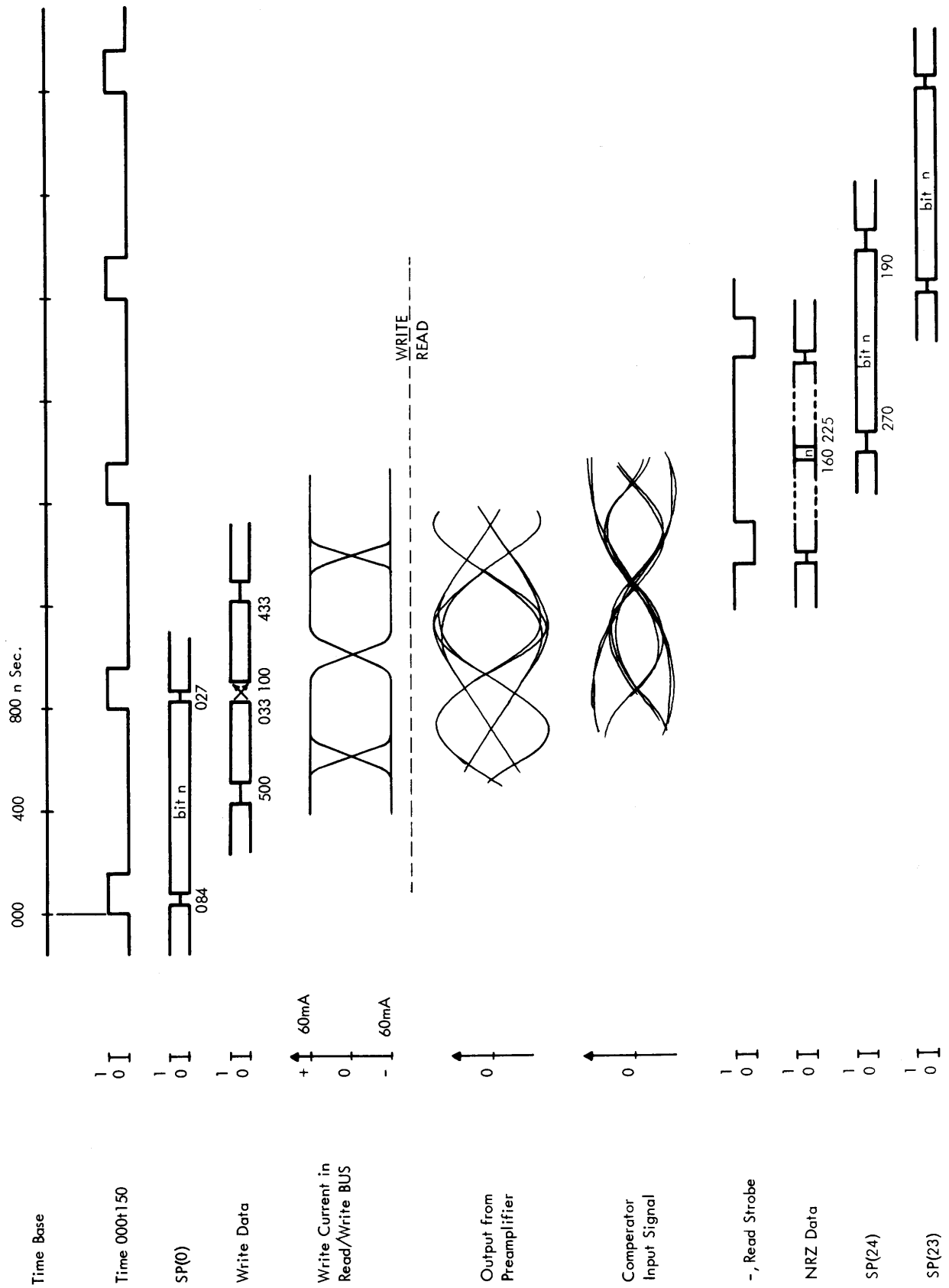


Fig. 7. Timing diagram showing the wave-forms of bit n from the time it leaves the serial register SP(0) and until it enters the register SP(23) after having been stored on a track. Calculated worst case shifting times for the signals are indicated.

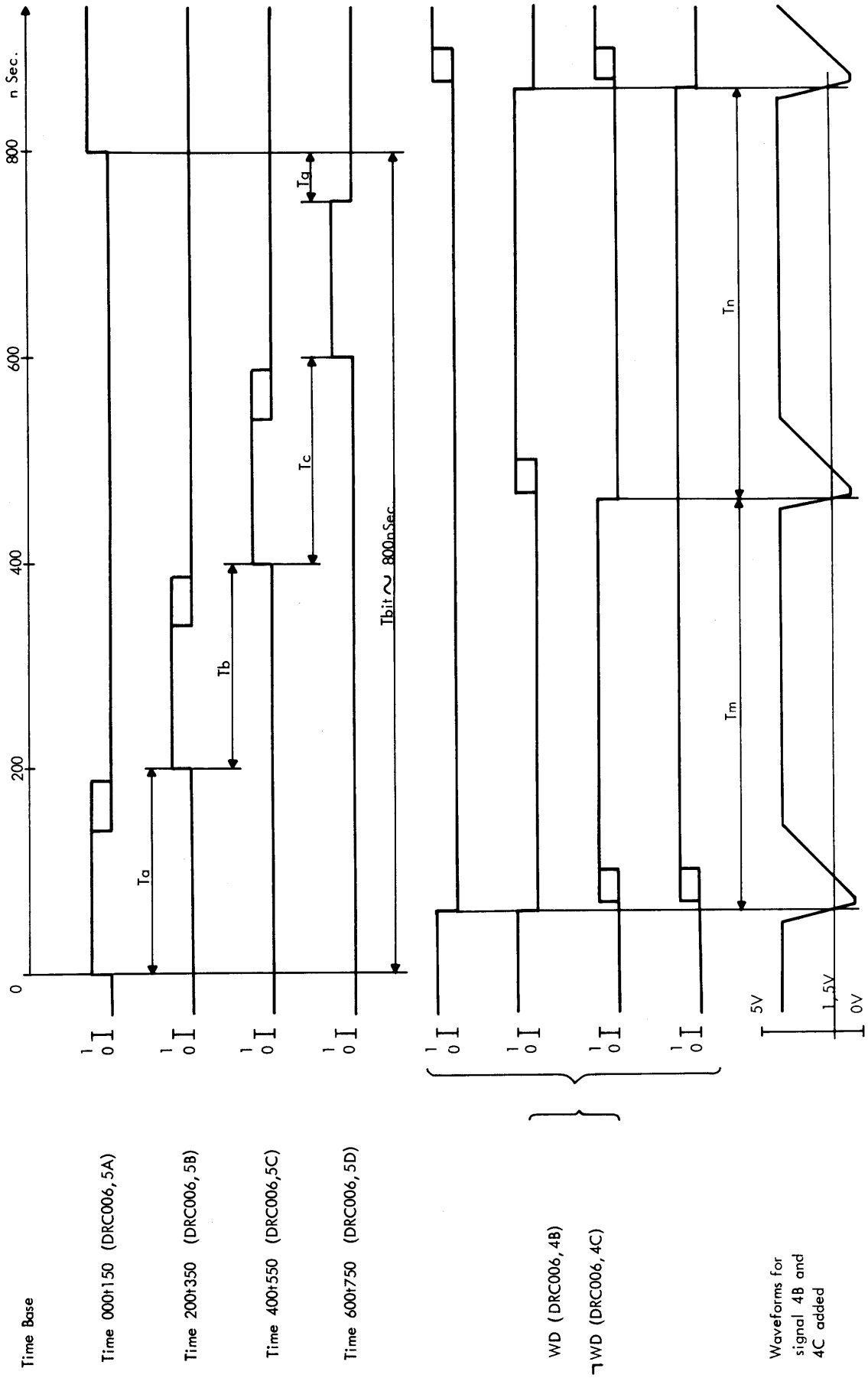


Fig. 8. Timing diagram for the clock pulse signals and the data signals to the drum. The clock pulses are always running, and their timings will correspond very nearly to the indicated values; but the exact timing adjustment depends on the waveforms of signal 4B and 4C added. Here Tm must be equal to Tn. The waveform can only be seen during writing on the drum.

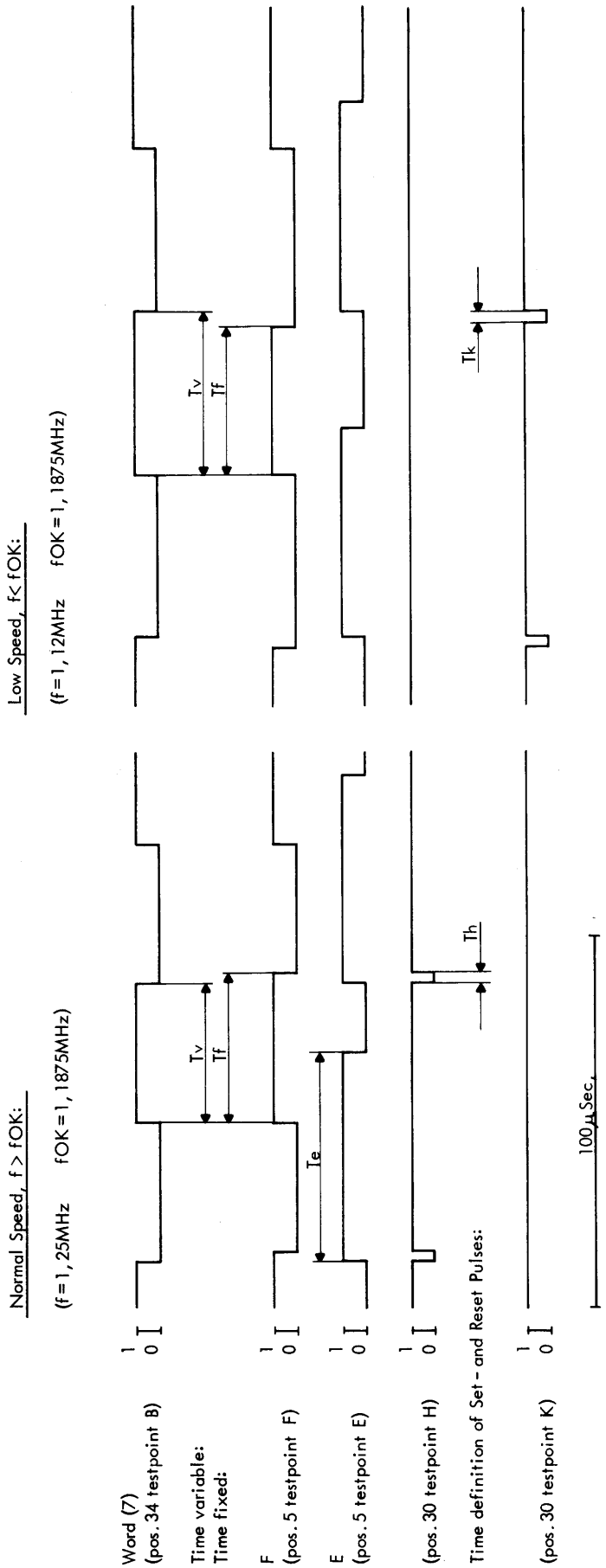


Fig. 9. Timing diagram showing the operation of the speed control circuit. Two situations are shown, one for the normal situation where the drum speed is 2880 RPM giving a clock frequency of 1,25 MHz, and one for the situation where drum speed is 10 per cent below normal.

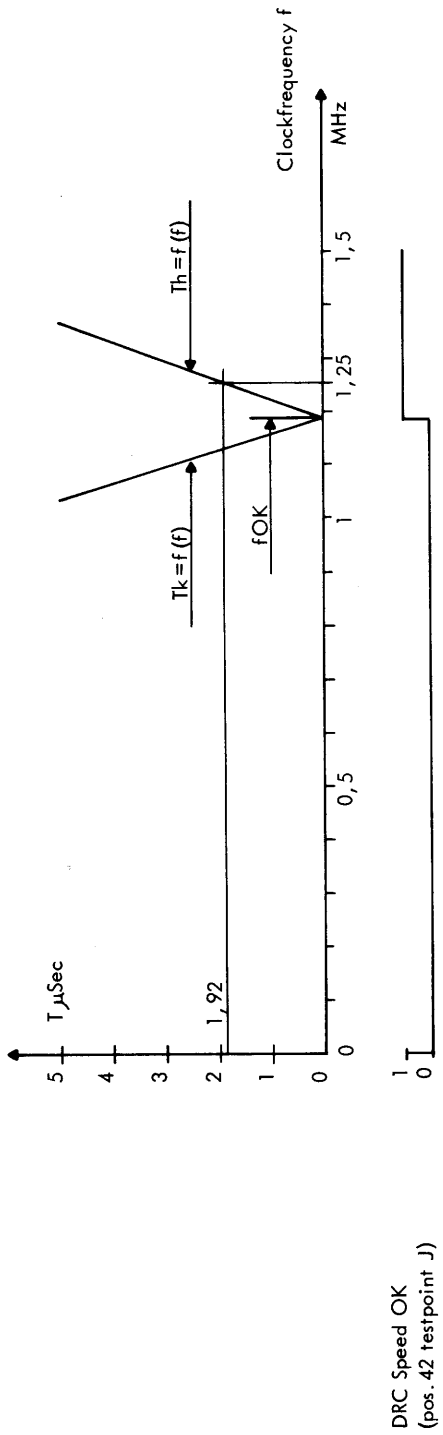


Fig. 10. The variation of the length Tn and Tk of the set and reset pulses is shown as functions of the clock frequency f. The final result from the speed control circuit is also given as a function of the frequency. It will be seen that, from not running to 95 per cent speed, the signal DRC Speed OK is logical 0, and from 95 per cent and up to 100 per cent (or more), the DRC Speed OK is logical one.

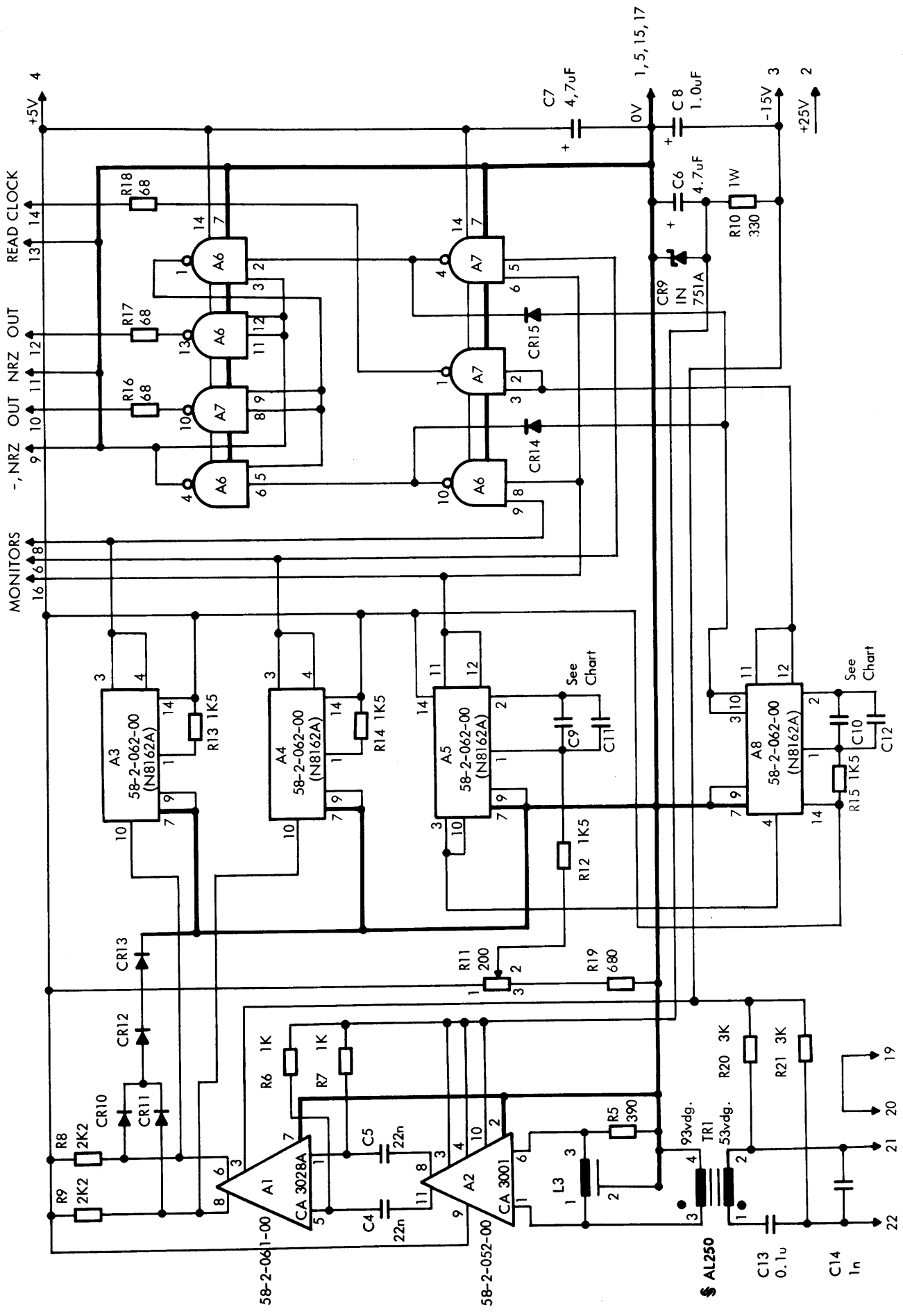


Fig. 11. Circuit diagram for the peak detector circuit card.

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MODIFICATION

OF

MODEL 1016 DRUM MEMORY

A/S REGNECENTRALEN
Falkoneralle 1
2000 COPENHAGEN F.

Temporary modification of VRC Drum type 1016 to obtain noise-free operation has been carried out by RC step-by-step as follows:

A. Taking Apart of the Electronic Card Chassis and Connector Panel

The electronic card chassis, control panel, tag board 3, and connector panel, including the multi-connectors J1, J2, J3, and J4, are taken from the rest of the drum system. These parts are sent to the assembling workshop where the following is carried out.

B. Clearing of Pin Positions

1. Remove all connection wiring from pins 13, 14, 15, and 16 on tag board 3.
2. Remove connection wiring from the electronic card chassis as follows:
   a. On card position 1 all wiring is disconnected
   b. On card position 2 all wiring is disconnected
   c. On card position 3 all wiring is disconnected
   d. On card position 4 all wiring is disconnected
   e. On card position 5 all wiring is disconnected
   f. On card position 6 all wiring to pins 1,2,3,4, and 29 is disconnected
   g. On card position 7 all wiring to pins 1,2,3,4, and 29 is disconnected
   h. On card position 8 all wiring to pins 1,2,3,4, and 29 is disconnected
   i. On card position 9 all wiring is disconnected except the wiring on pins 26, 27, and 28
   j. On card position 10 all wiring is disconnected except the wiring on pins 26, 27, and 28
   k. On card position 11 all wiring is disconnected except the wiring on pins 26, 27, and 28

Now the frame is ready for wiring.

C. Wiring of Inverters

The address X selection is changed somewhat by using some of the inverters on card position 8 to generate the necessary X selection signals in both representations. (see diagram pages 5,6 for new wiring)

D. Establishment of the 0 Volt System

The 0 volt system is constructed as two 0 volt systems connected together at one point (see diagram page 7). The one 0 system is a 0 system for all circuits having digital inputs and outputs. This system incorporates card positions 1,2,3, and 9,10,11.

The other 0 system is a 0 system for all circuits handling small level analog signals plus digital circuits which are not switched during reading of a track. This system incorporates card positions 4,5,6,7, and 8.

To obtain this separation, it is necessary to rearrange some of the cards:

1. Writer fo track 0 to 255
2. Writer for track 256 to 511
3. Peak Detector
4. Read Preamplifier for 0 to 255
5. Read Preamplifier for 256 to 511

6.-11. Unchanged

Furthermore, it is necessary to make small changes on the Read Preamplifier Cards and Peak Detector Circuit Cards (see diagram pages 8, 9, 10, 11).

E. Establishment of +25, -15, +5 Volt System

The DC power supply system is divided into two groups in the same way as the 0 volt system. The wiring of the DC supply system is shown on pages 12, 13.

F. Establishment of Digital Inputs and Outputs

Some minor changes in the wiring of the digital signals have been made (see diagram page 14).

G. BUS Wiring

Due to the rearrangement of the cards, the BUS wiring is changed a little (see diagram page 15).

H. Circuit Card Modifications

Four circuit cards (six, if drum has more than four head bar modules) have been modified as follows:

1. Read Preamplifier for data tracks has been modified by cutting two printed wires, drilling eight more holes, and inserting eight new components. The value of resistors R19 and R20 must be equal and is approximately 3000 ohms. The exact value depends on the amplitude of the AC output which must be adjusted to 2 volt peak to peak by inserting the expedient resistors. (see diagram page 11).
2. Read Preamplifier for clock track is modified in a simular way as H.1. (see diagram page 9).
3. Peak Detector card for data track is modified by cutting some of the printed wires, changing some of the components, and adding a few other components (see diagram page 12). Some of these components have been difficult to place in a proper way, so they are fixed to the circuit card. They are more or less self-supporting.
4. Peak Detector card for clock track is modified as in H.3. (see diagram page 10).

I. Reassembling

The modification in the assembling workshop is now

I. Reassembling (cont.)

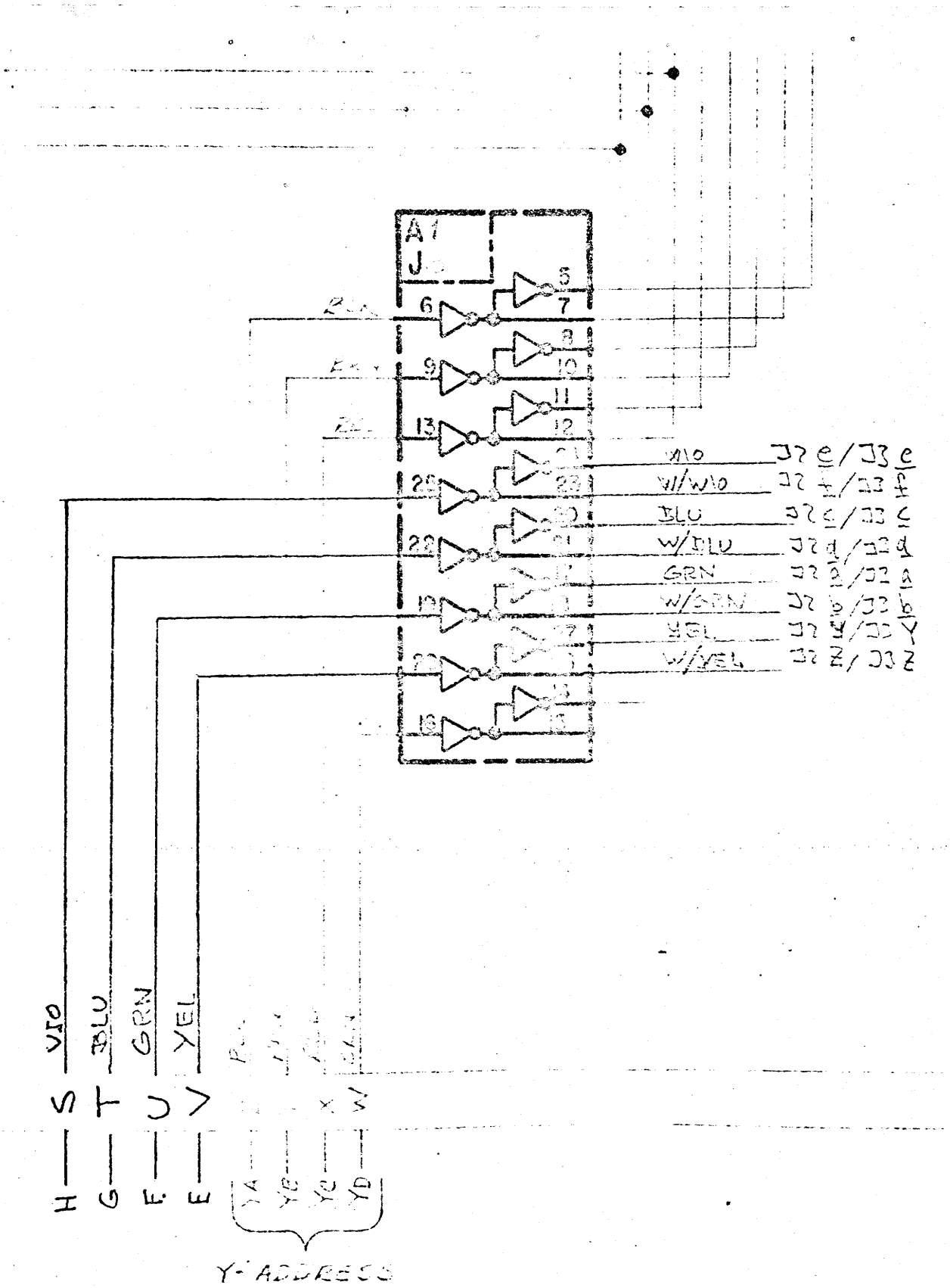
completed. The modified electronic chassis can now be reassembled with the drum plate.

J. Removal of 0 Volt to Chassis Connection

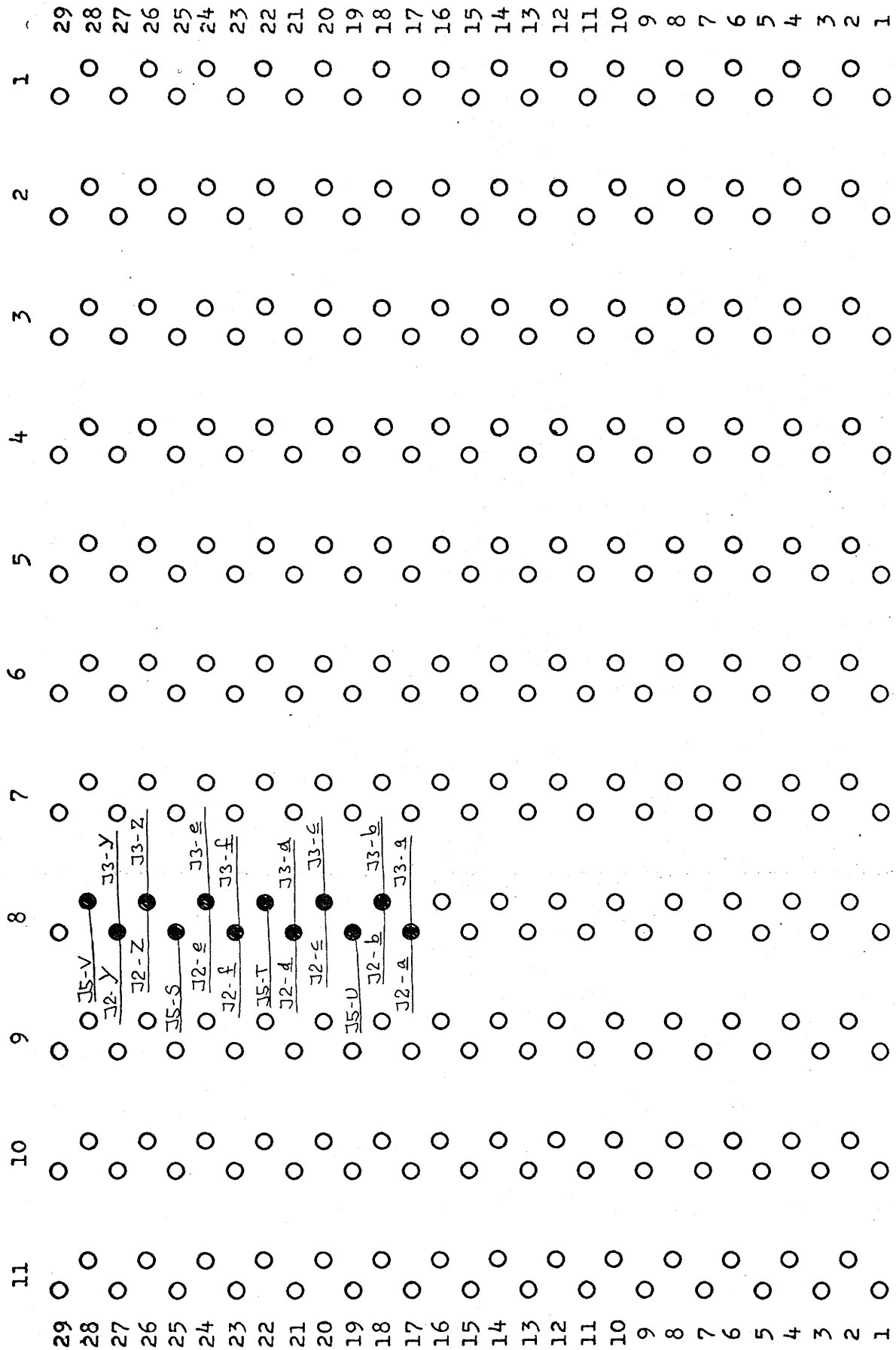
Inside the square can, the connection between chassis and 0 volt is removed by cutting away the black wire from chassis to 0 volt on the clock preamplifier circuit card.
Now there should be no connection between the electronic system and the drum chassis.

K. Interface Cable Connection

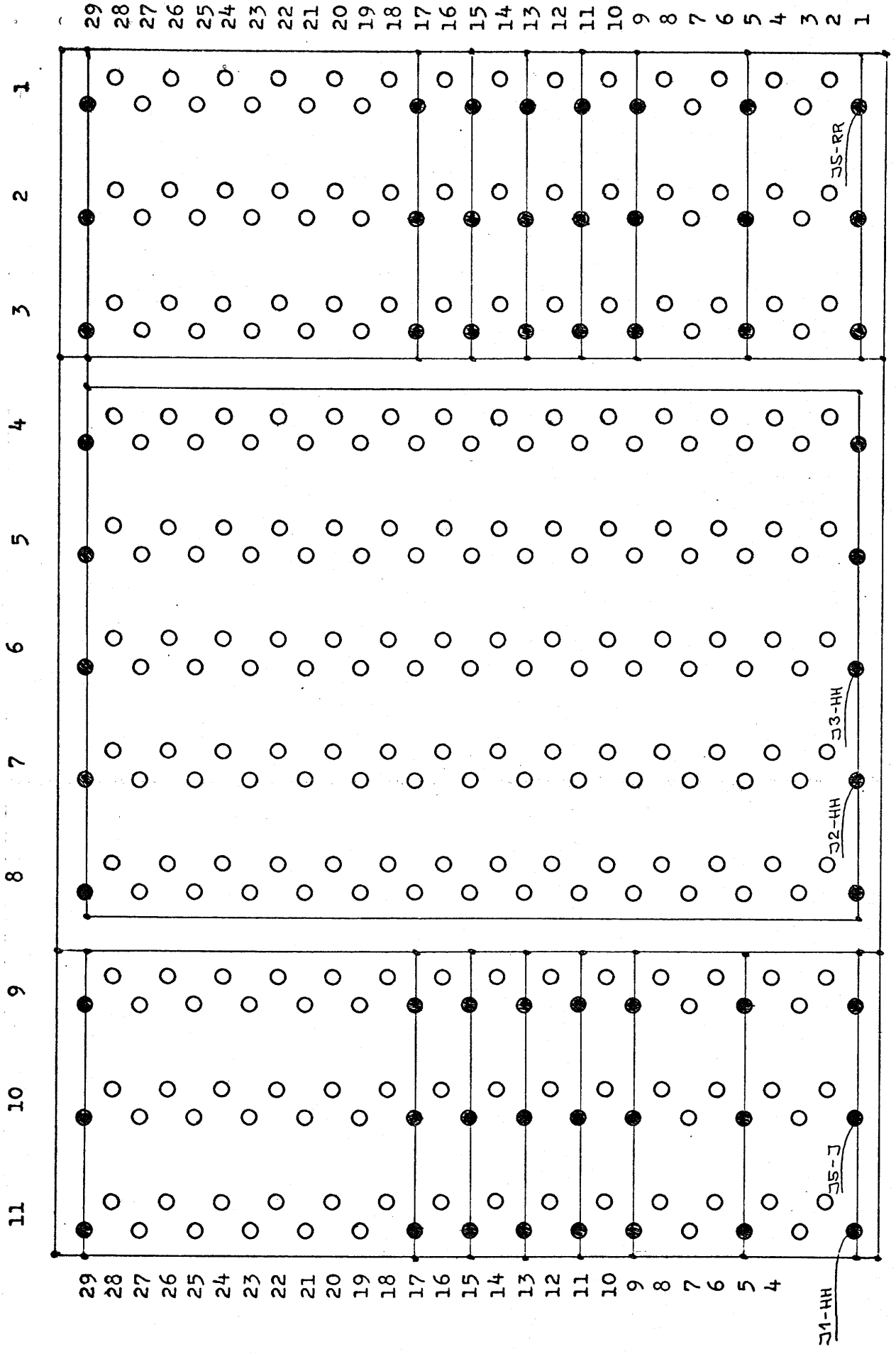
Some changes in the wiring of the interface connection have been made (see diagram page 16).



WIRING DEAGRAM FOR INVERTERS IN THE X SELECTION

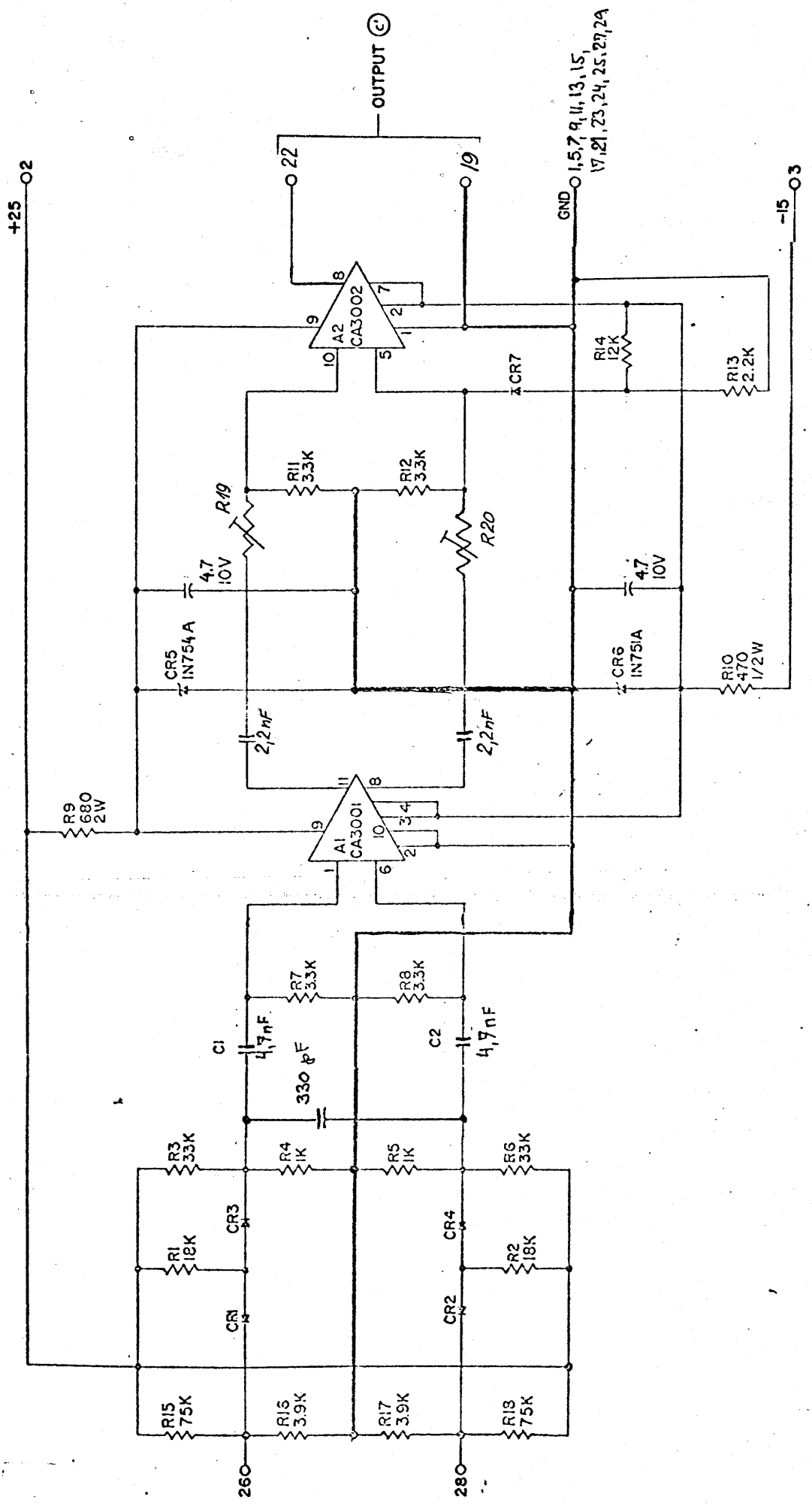


WIRING SCHEME FOR THE X SELECTION INVERTERS



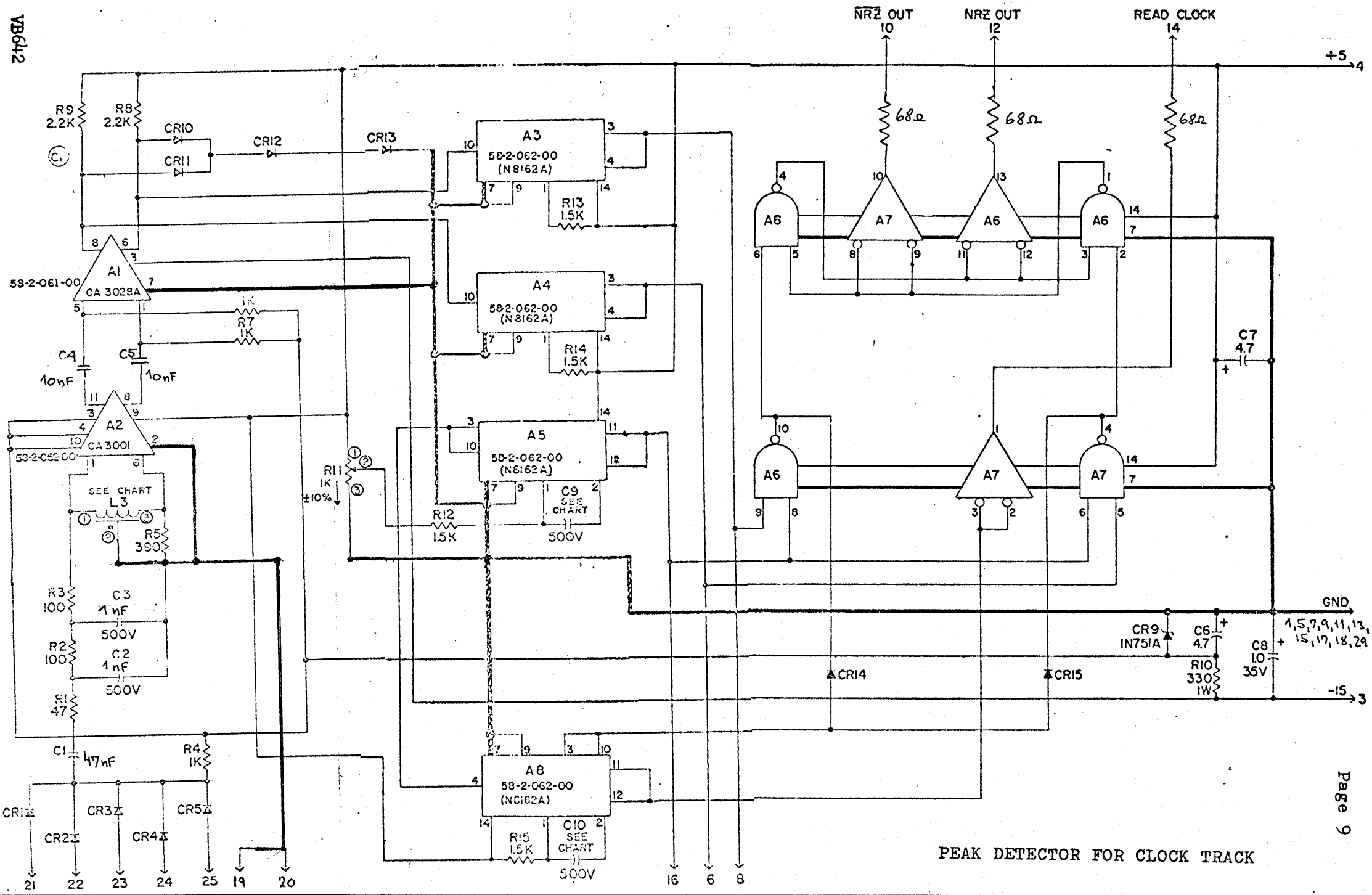
WIRING OF 0 VOLT

VB642

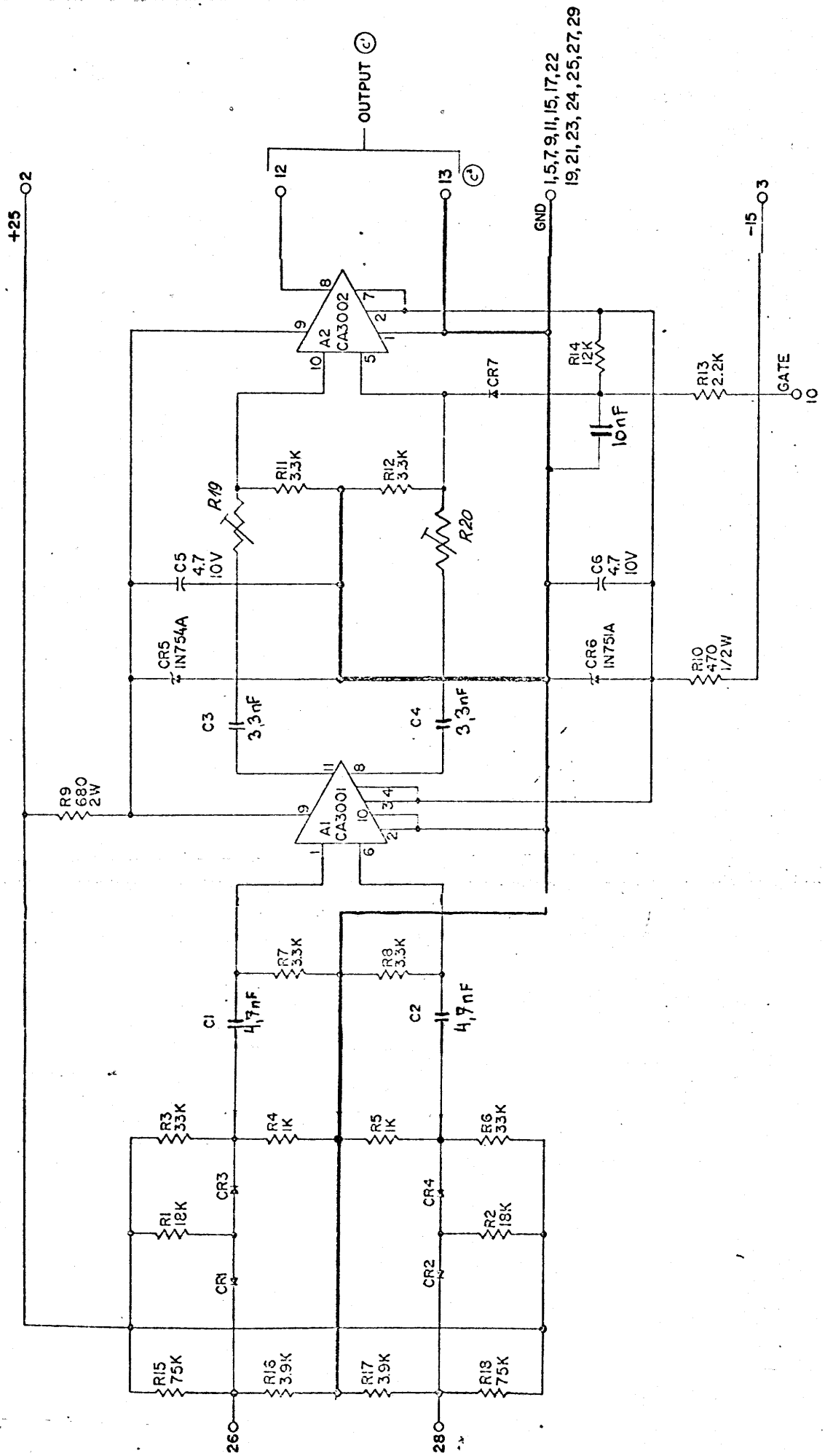


VB642

READ PREAMPLIFIER FOR CLOCK TRACK

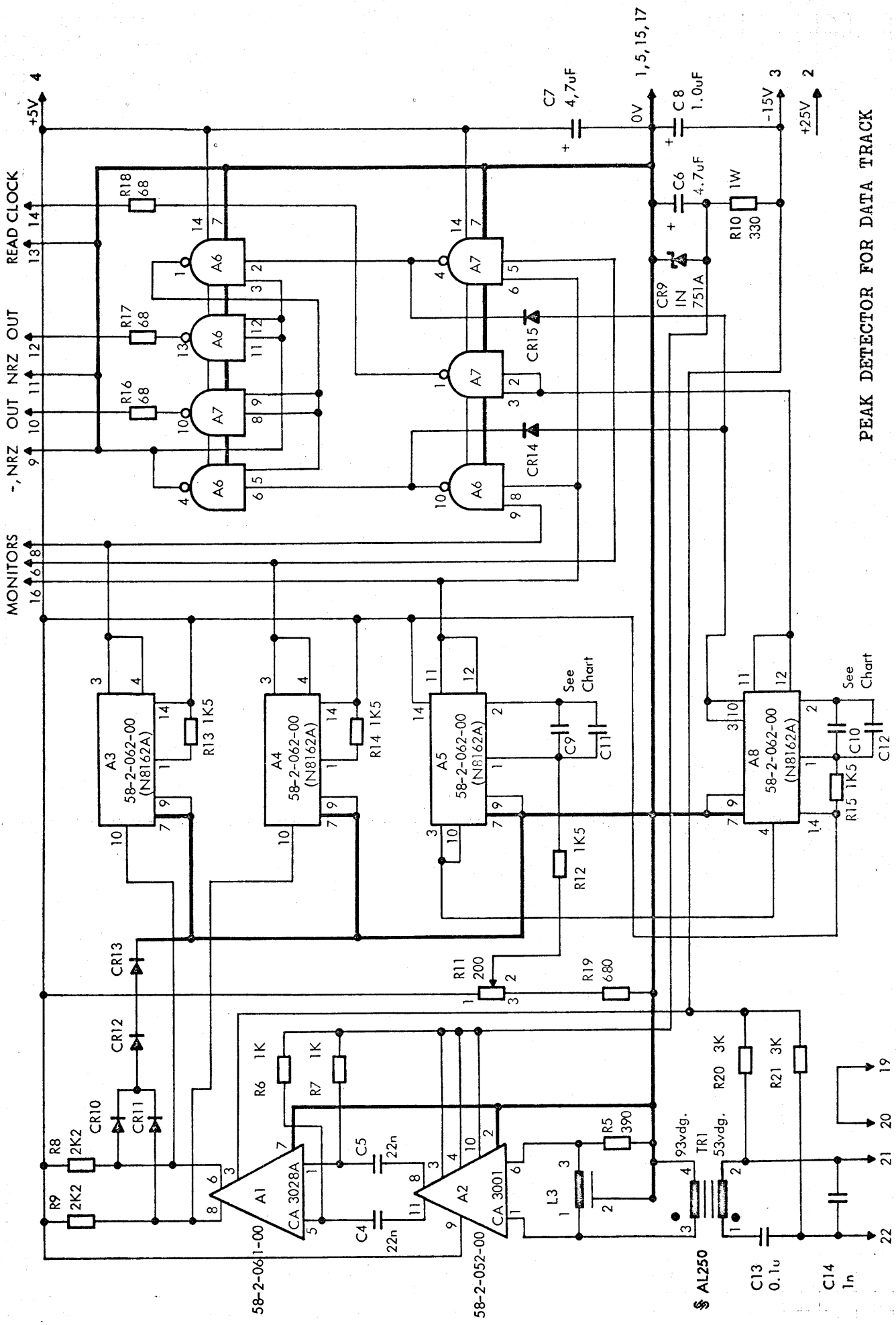


PEAK DETECTOR FOR CLOCK TRACK



VB642

READ PREAMPLIFIER FOR DATA TRACK



A/S REGNECENTRALEN 031169PEP 051169ML

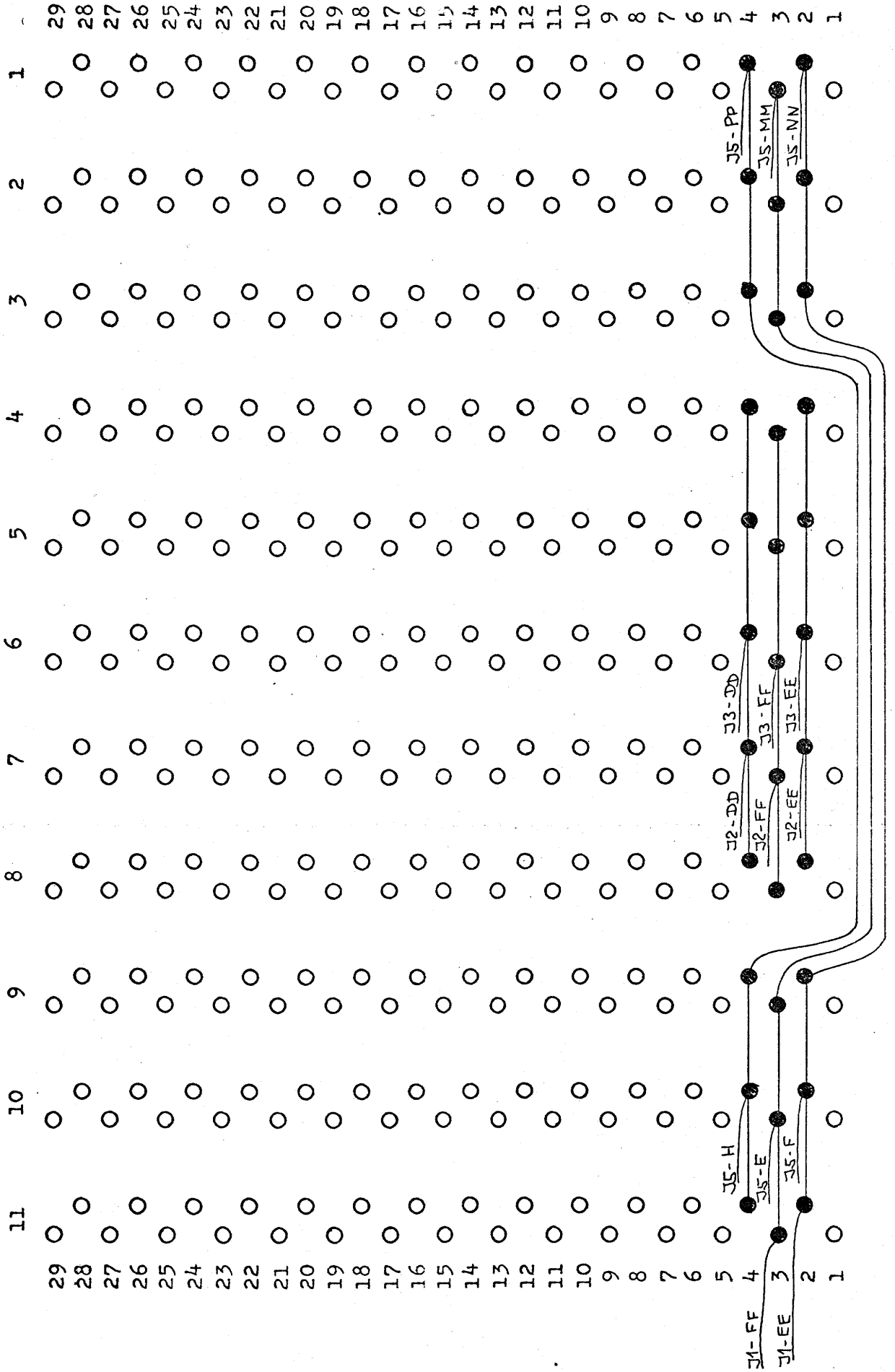
VRC 1016

V11620

PEAK DETECTOR

Logic Diagram

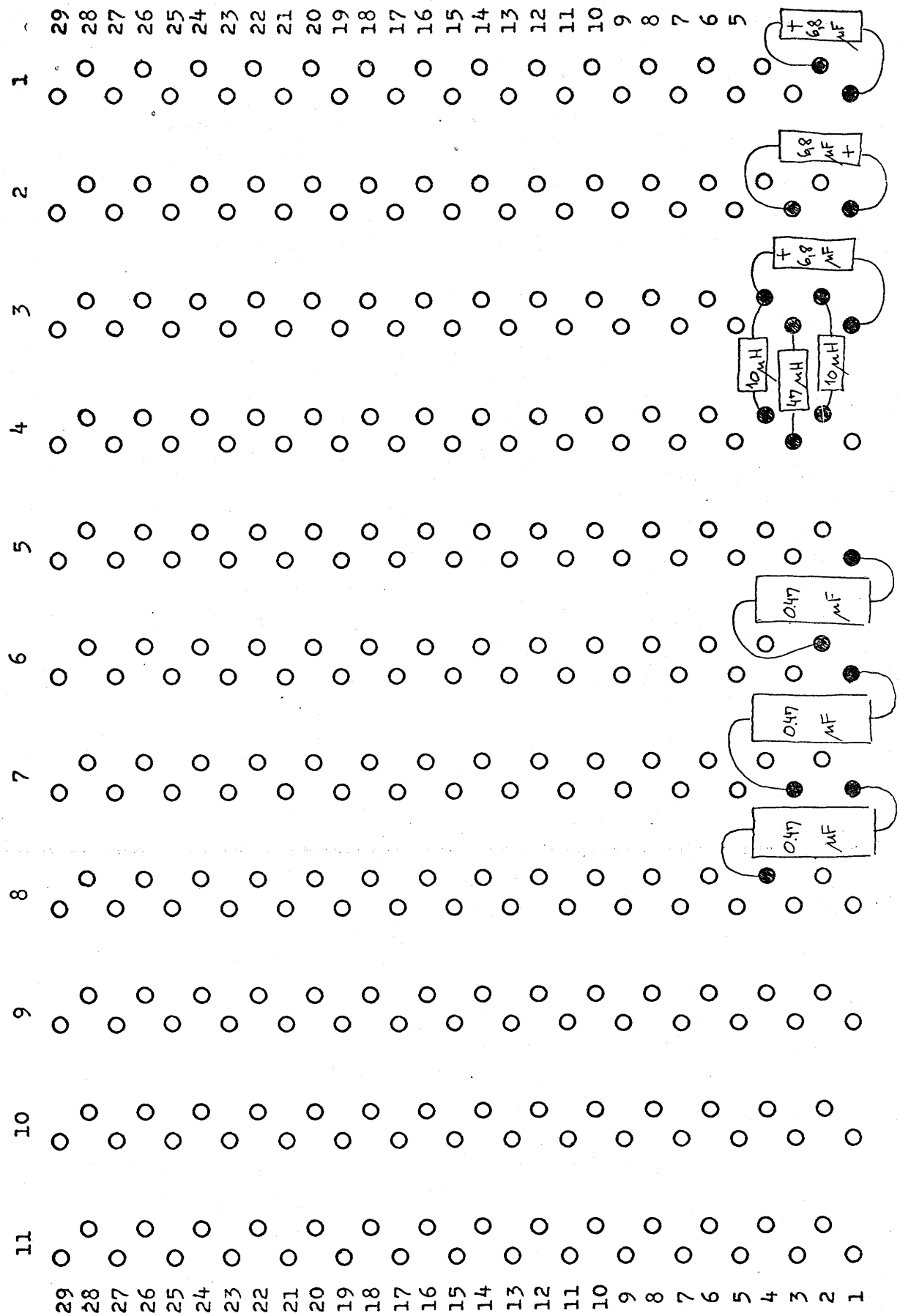
VB642



WIRING OF DC SUPPLY

VB642

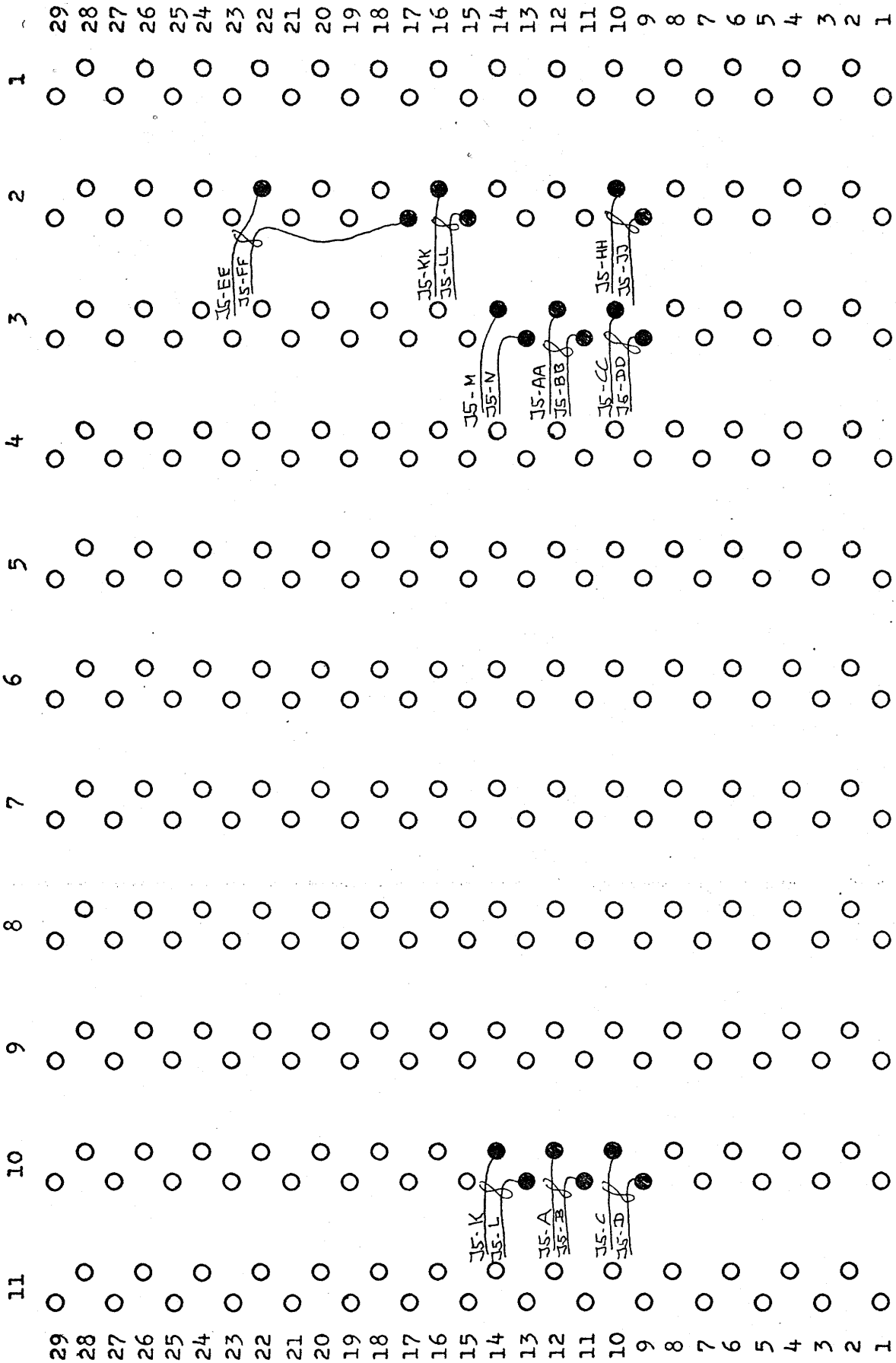
PEP Formular 220969



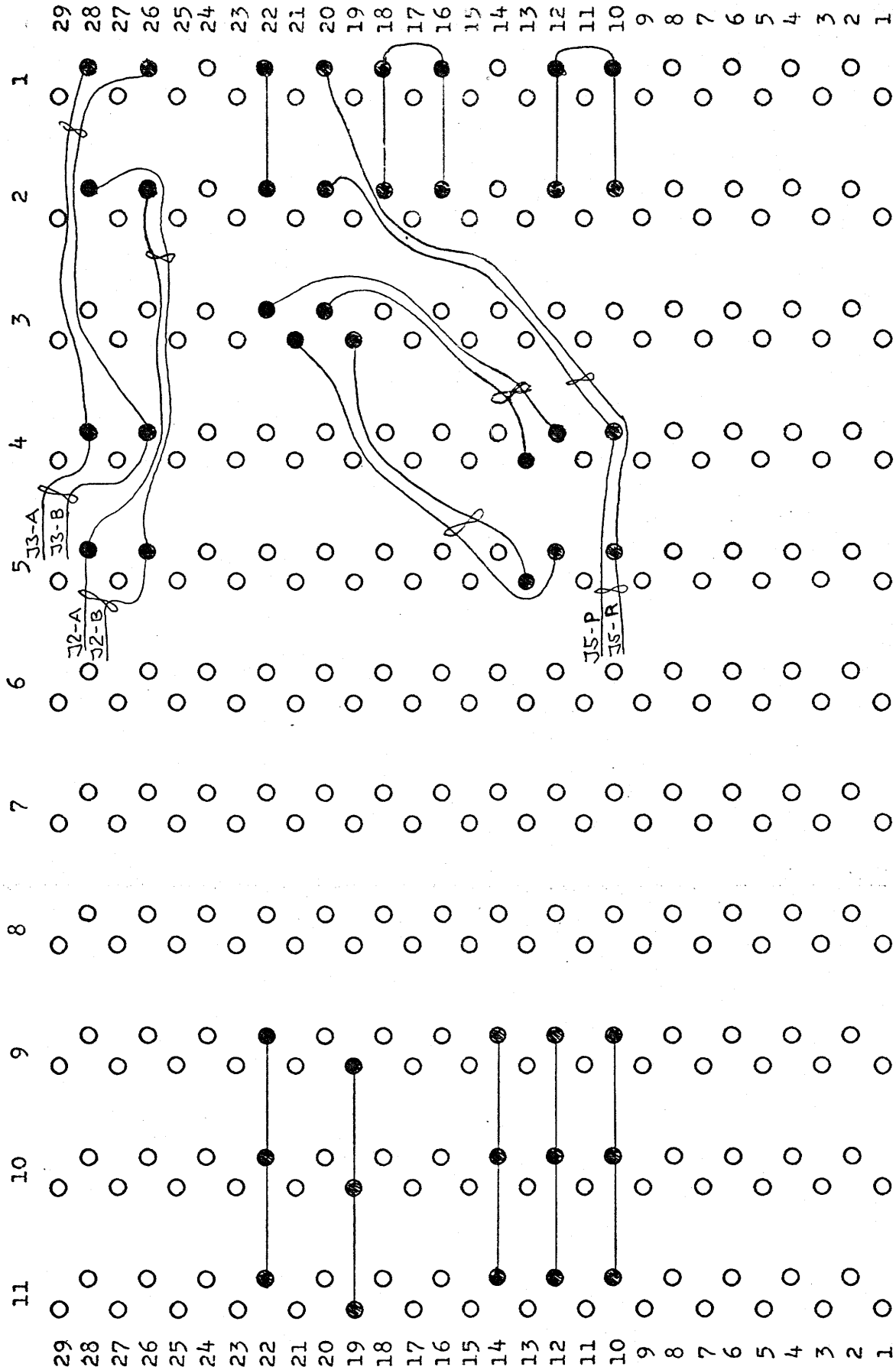
DECOUPLING COMPONENTS IN THE WIRING

VB642

PEP Formular 220969



WIRING OF INPUT - OUTPUT SIGNALS



BUS WIRINGS

CONNECTOR: 1307 UNIT : DRC401 NAME	COMMENTS	PIN	CONNECTOR: J5 NAME	COMMENTS
NRZ DATA	FROM CLOCK TRACK	A	NRZ DATA	FROM CLOCK TRACK
-Grd.-	-	B	-Grd.-	-
-,NRZ DATA	FROM CLOCK TRACK	C	-,NRZ DATA	FROM CLOCK TRACK
-Grd.-	-	D	-Grd.-	-
MINUS 15 VOLT	RETURN	E	-15	RETURN
PLUS 25 VOLT	RETURN	F	+25	RETURN
PLUS 5 VOLT	RETURN	H	+5	RETURN
NUL VOLT	RETURN	J	0	RETURN
READ STROBE	FROM CLOCK TRACK	K	READ STROBE	FROM CLOCK TRACK
-Grd.-	-	L	-Grd.-	-
READ STROBE	FROM DATA TRACK	M	READ STROBE	FROM DATA TRACK
-Grd.-	-	N	-Grd.-	-
DTA(0)	256	P	J	BAR:EFGH
-,DTA(0)	-,256	R	-,J	BAR:ABCD
DTA(1)	128	S	H	X8
DTA(2)	64	T	G	X4
DTA(3)	32	U	F	X2
DTA(4)	16	V	E	X1
DTA(5)	8	W	YD	Y8
DTA(6)	4	X	YC	Y4
DTA(7)	2	Y	YB	Y2
DTA(8)	1	Z	YA	Y1
NRZ DATA	FROM DATA TRACK	AA	NRZ DATA	FROM DATA TRACK
-Grd.-	-	BB	-Grd.-	-
-,NRZ DATA	FROM DATA TRACK	CC	-,NRZ DATA	FROM DATA TRACK
-Grd.-	-	DD	-Grd.-	-
WE	WRITE ENABLE	EE	WRITE ENABLE	WE
-Grd.-	-	FF	-Grd.-	-
WD	WRITE DATA	HH	WRITE DATA	WD
-Grd.-	-	JJ	-Grd.-	-
-,WD	-,WRITE DATA	KK	-,WRITE DATA	-,WD
-Grd.-	-	LL	-Grd.-	-
-15V	POWER F.POW406	MM	-15V	POWER
+25V	POWER F.POW406	NN	+25V	POWER
+5V	POWER F.POW406	PP	+5V	POWER
OV	POWER F.POW406	RR	OV	POWER
Chassis	SCREN	SS	CHASSIS	FRAME
Chassis	SCREN	TT	CHASSIS	FRAME

UNIT: RC4320 Designed:090969PEP CABLE CONNECTION BETWEEN DRC401 AND VRV1016

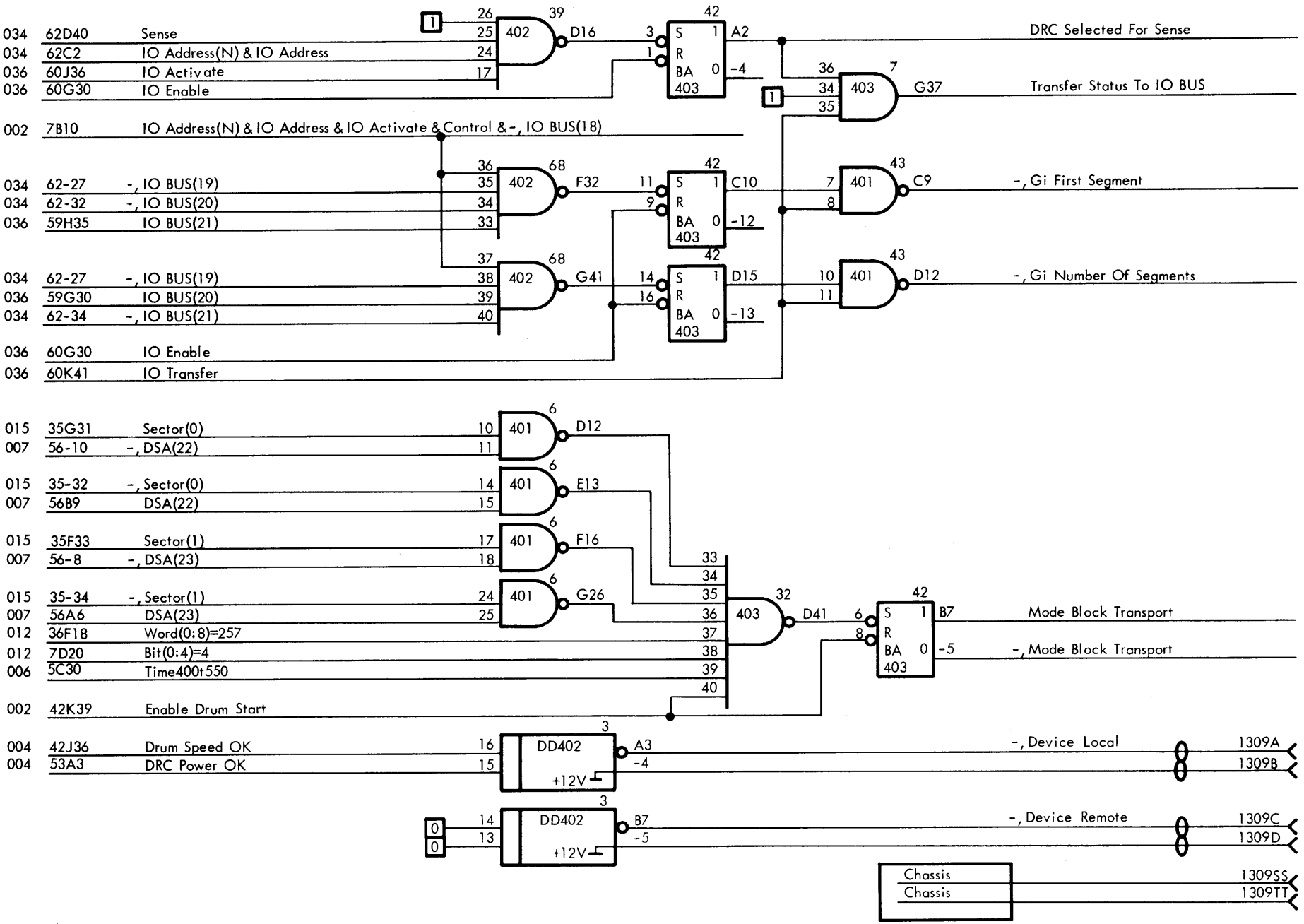
VB642

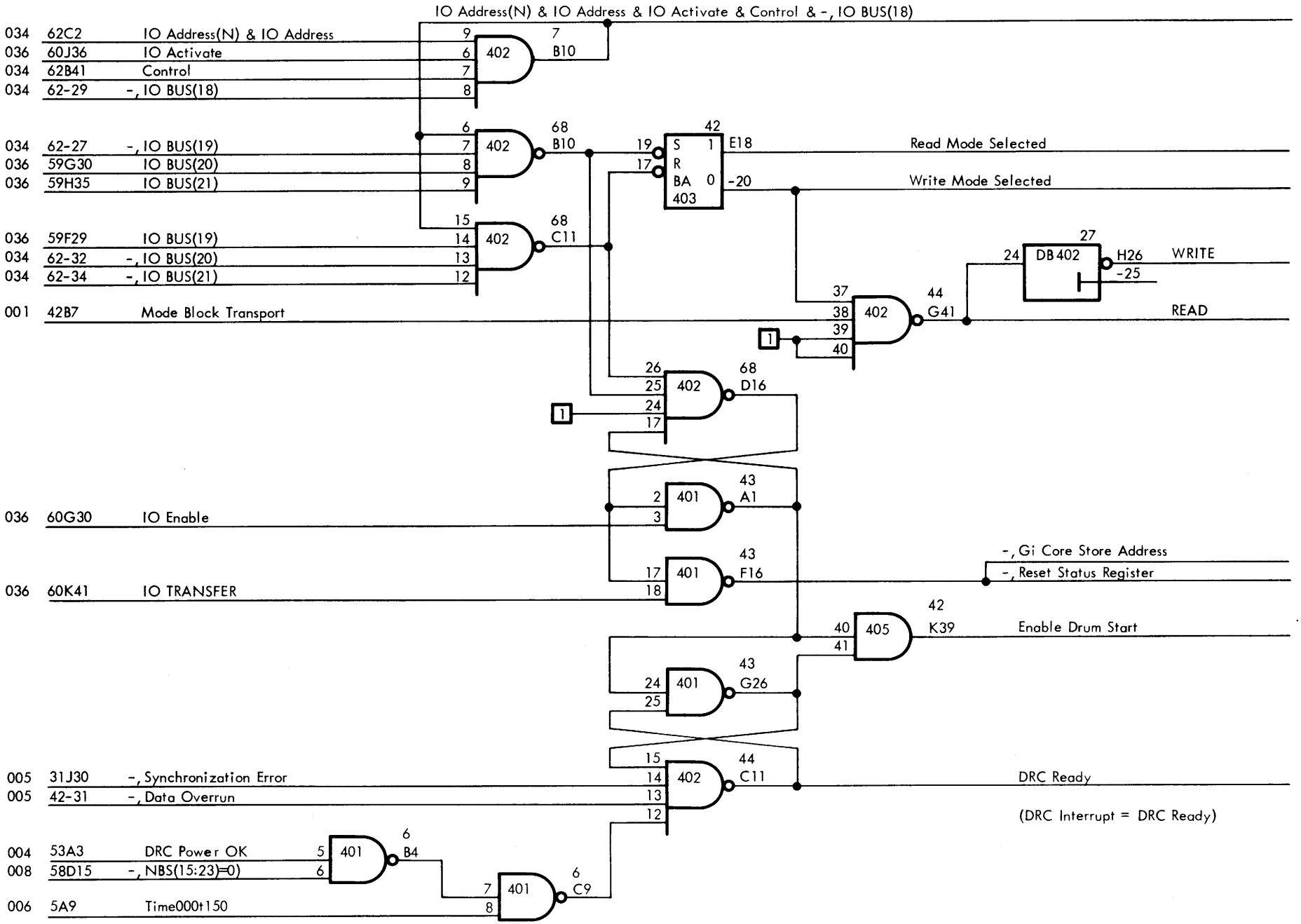
RC 4005 LOGIC DIAGRAMS

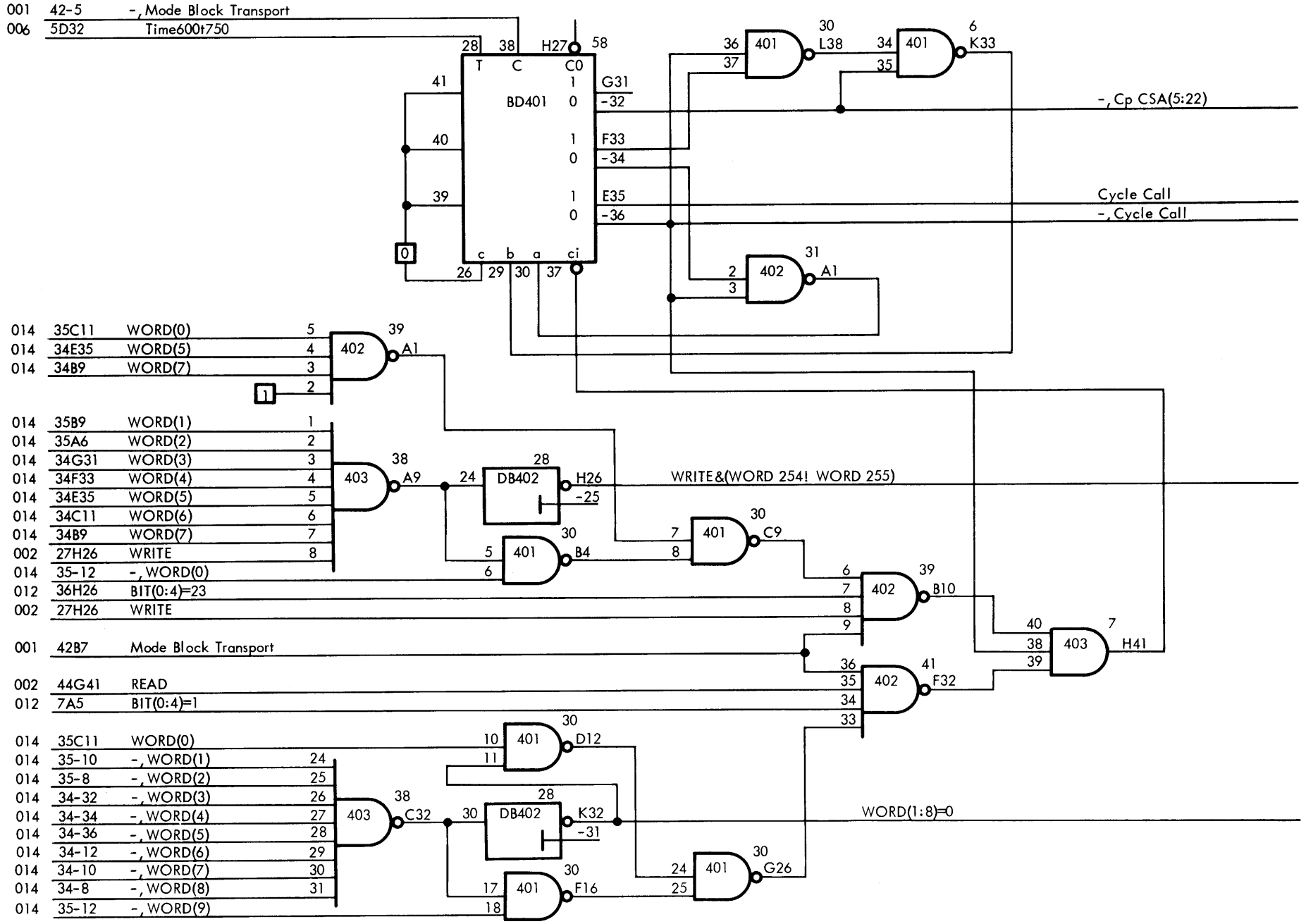
DRC401

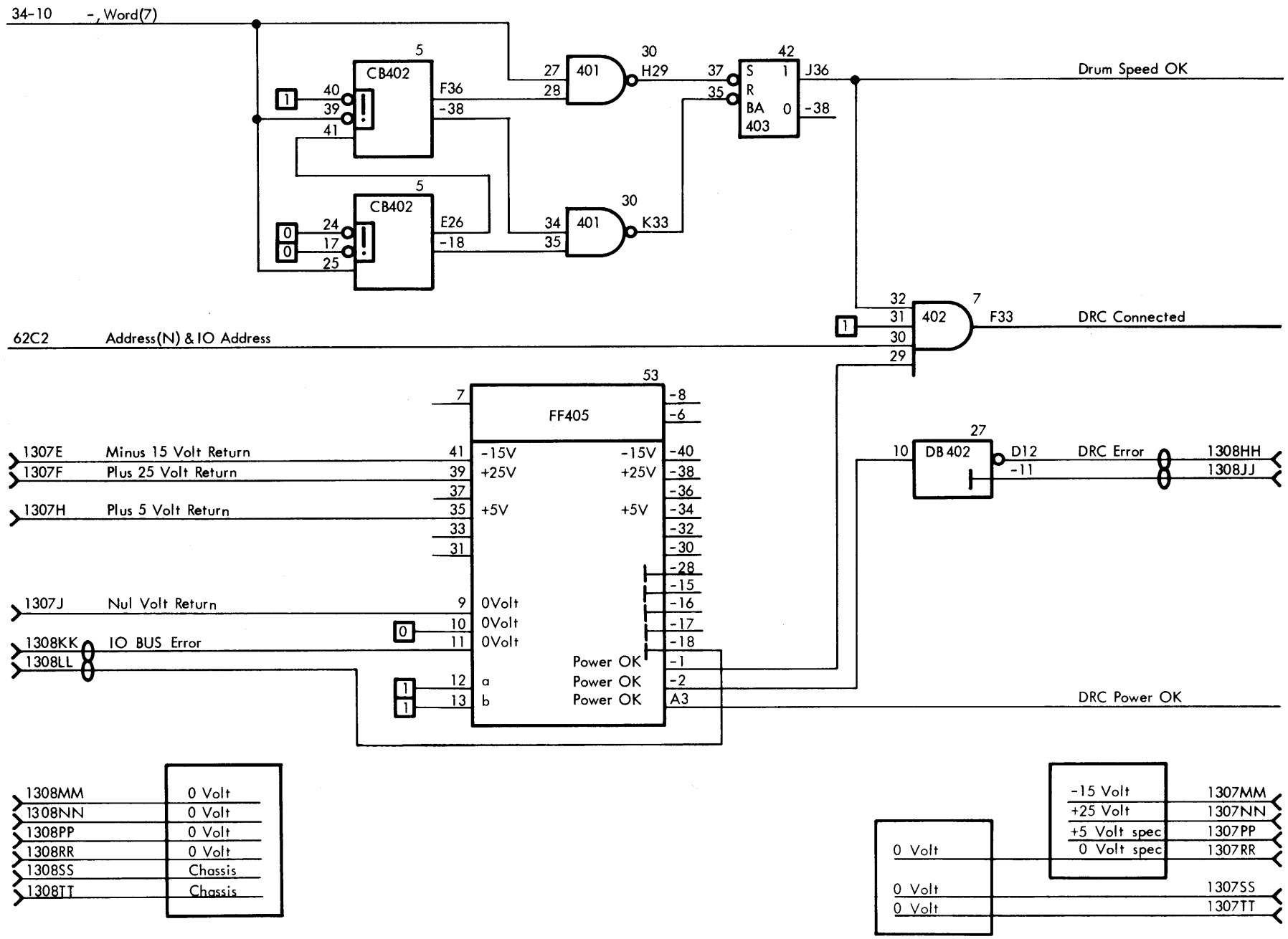
Drum Controller (DRC)		Dwg. No.
DRC001	IO COMMANDS AND MODE BLOCK TRANSPORT	V11456
002	READ/WRITE AND READY	V11457
003	CYCLE CALL	V11458
004	CONNECTED AND POWER OK	V11459
005	STATUS REGISTER	V11460
006	DRUM DATA SIGNALS	V11573
007	DRUM SEGMENT ADDRESS, DSA(12:23)	V11462
008	NUMBER OF SEGMENTS, NBS(15:23)	V11463
009	CORE STORE ADDRESS, CSA(5:10)	V11464
010	CORE STORE ADDRESS, CSA(11:23)	V11465
012	BIT AND WORD REGISTER DECODINGS	V11466
013	CONTROL SIGNALS FOR BIT, WORD, SECTOR, DSA, NBS, AND CSA	V11467
014	WORD(0:8)	V11468
015	BIT(0:4) AND SECTOR(0:1)	V11469
016	CONTROL SIGNALS FOR WORD BUFFER	V11470
017	CONTROL SIGNALS FOR PARITY WORD, AND SERIAL PARALLEL REGISTER	V11471
018	WORD BUFFER, WB(0:7)	V11472
019	WORD BUFFER, WB(8:15)	V11473
020	WORD BUFFER, WB(16:23)	V11474
021	DRUM TRACK ADDRESS, DTA(0:8), AND ENABLING OF CONTROLS	V11569
023	DRUM ADDRESS SIGNALS, DTA(0:8)	V11571
024	LOGICAL DIAGRAM	V11770
030	HDS BUSin(0:15)	V11477
031	HDC BUSin(16:23), AND HDC CONTROL	V11478

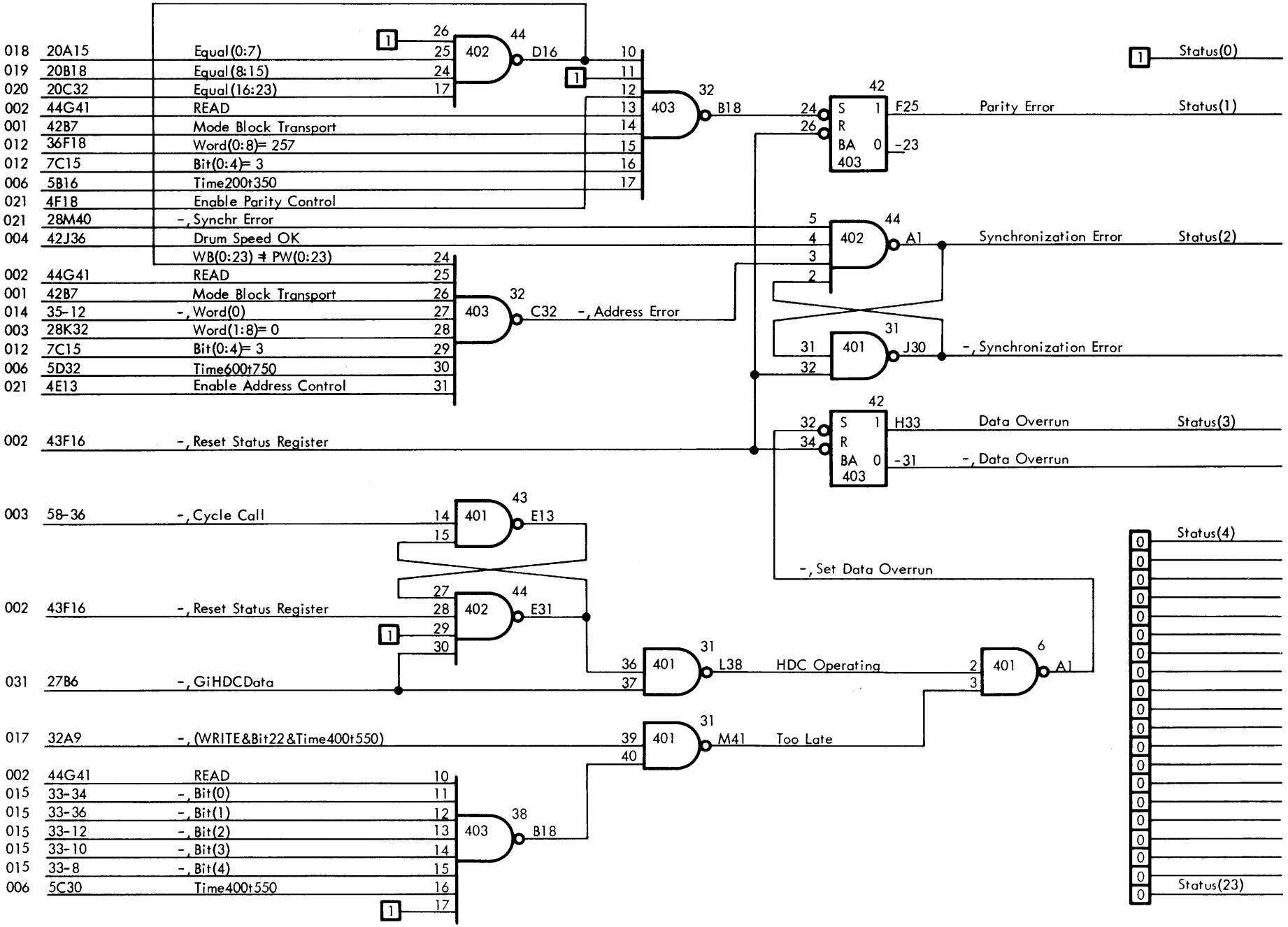
Drum Controller (DRC)		Dwg. No.
DRC032	HDC BUS(0:11)	V11479
033	HDC BUS(12:23)	V11480
034	DEVICE SELECTION, STATUS, CONNECTED, READY, AND INTERRUPT	V11481
035	IO BUS(5:16)	V11482
036	IO BUS(17:23), AND IO ENABLE, ADDRESS, ACTIVATE, AND TRANSFER	V11483
037	HDC CABLE CONNECTION	V10817
038	HDC AND LDC CABLE CONNECTIONS	V10818

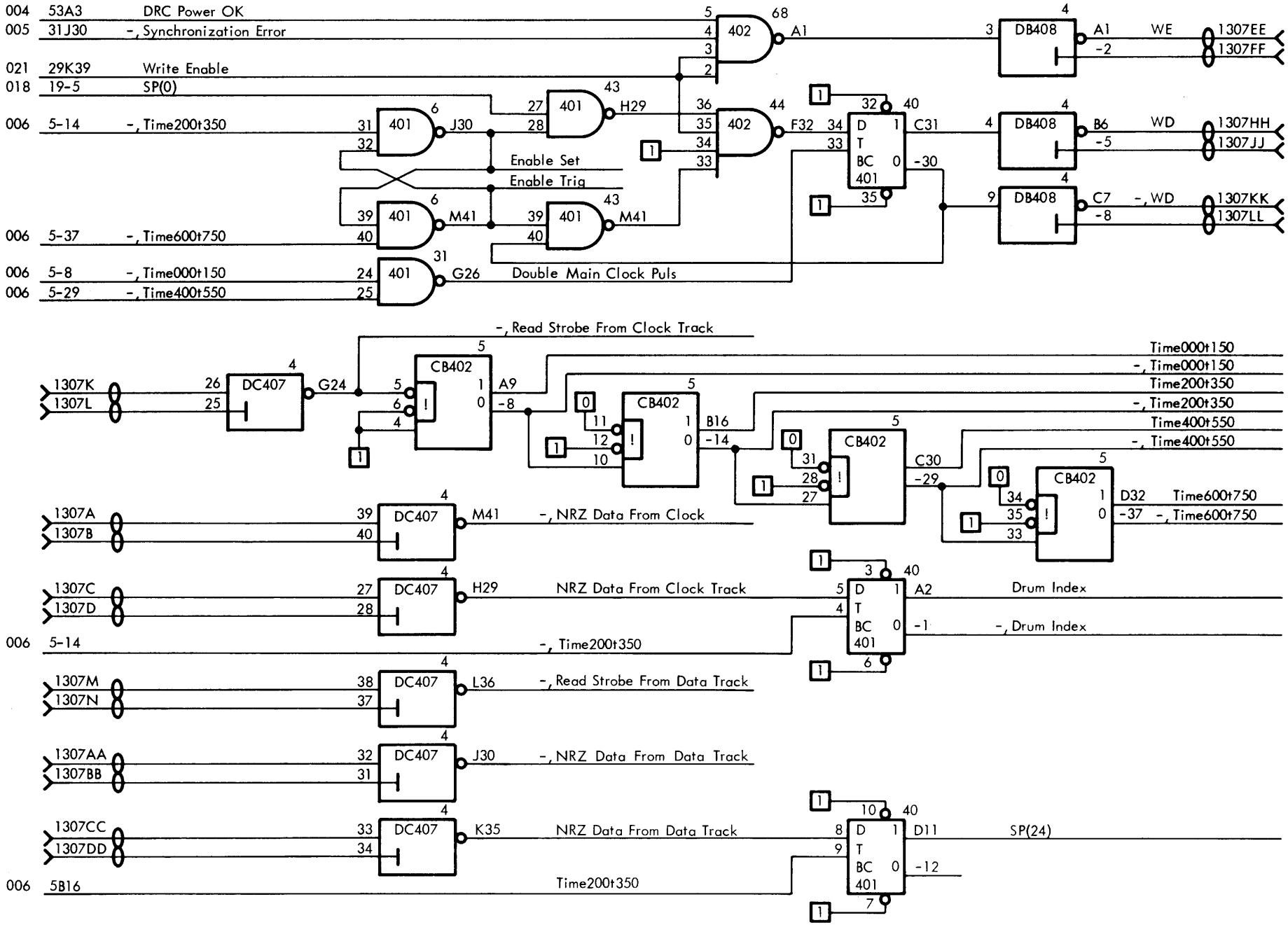

034 62D40 Sense
034 62C2 IO Address(N) & IO Address
036 60J36 IO Activate
036 60G30 IO Enable
002 7B10 IO Address(N) & IO Address & IO Activate & Control & -, IO BUS(18)
034 62-27 -, IO BUS(19)
034 62-32 -, IO BUS(20)
036 59H35 IO BUS(21)
034 62-27 -, IO BUS(19)
036 59G30 IO BUS(20)
034 62-34 -, IO BUS(21)
036 60G30 IO Enable
036 60K41 IO Transfer
015 35G31 Sector(0)
007 56-10 -, DSA(22)
015 35-32 -, Sector(0)
007 56B9 DSA(22)
015 35F33 Sector(1)
007 56-8 -, DSA(23)
015 35-34 -, Sector(1)
007 56A6 DSA(23)
012 36F18 Word(0:8)=257
012 7D20 Bit(0:4)=4
006 5C30 Time400t550
002 42K39 Enable Drum Start
004 42J36 Drum Speed OK
004 53A3 DRC Power OK
DRC Selected For Sense
Transfer Status To IO BUS
-, Gi First Segment
-, Gi Number Of Segments
Mode Block Transport
-, Mode Block Transport
-, Device Local
-, Device Remote
Chassis
Chassis
1309A
1309B
1309C
1309D
1309SS
1309TT
402
401
403
DD402
+12V

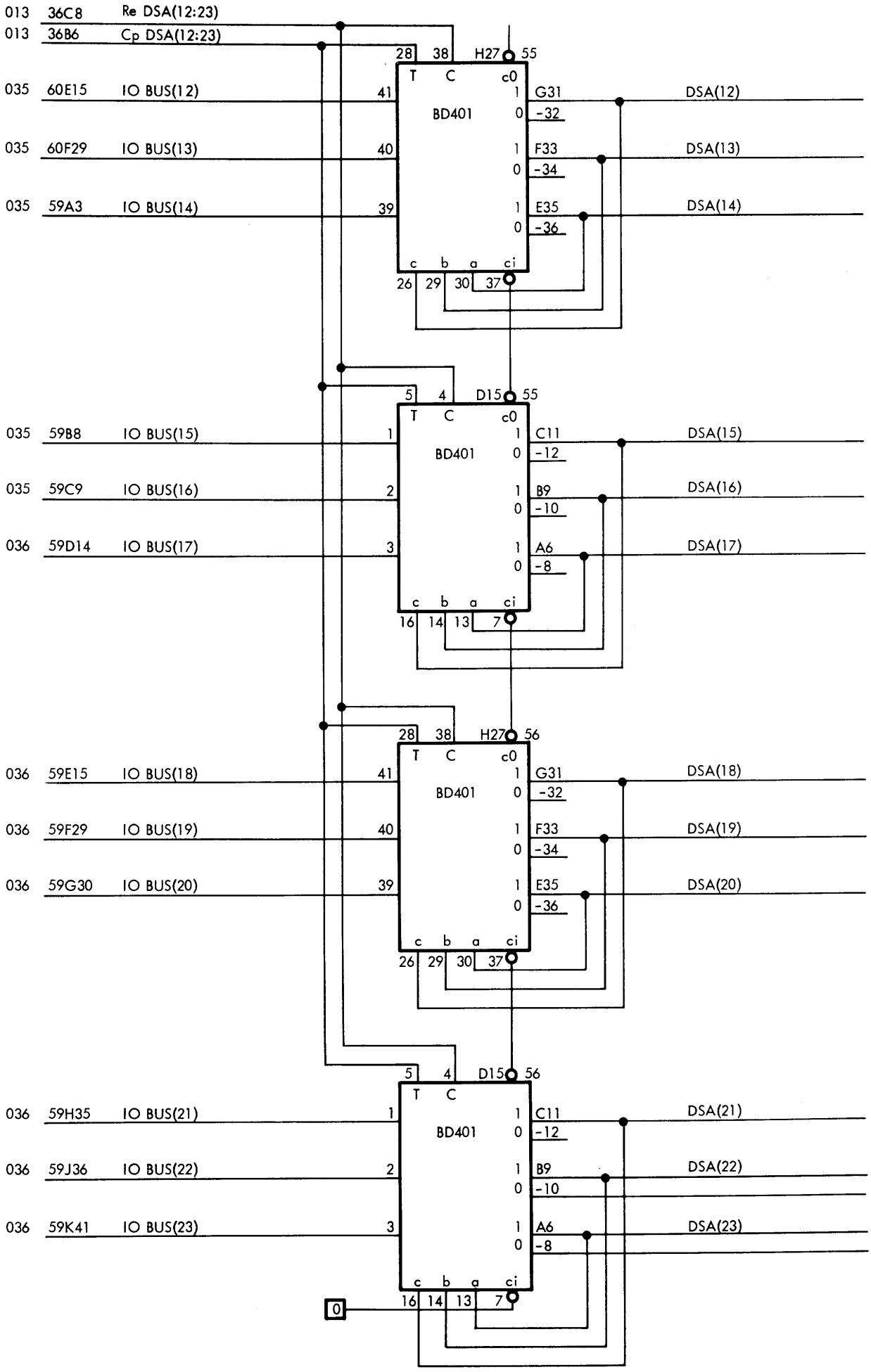

IO Address(N) & IO Address & IO Activate & Control & -, IO BUS(18)
034 62C2 IO Address(N) & IO Address
036 60J36 IO Activate
034 62B41 Control
034 62-29 -, IO BUS(18)
402 B10
034 62-27 -, IO BUS(19)
036 59G30 IO BUS(20)
036 59H35 IO BUS(21)
402 C11
036 59F29 IO BUS(19)
034 62-32 -, IO BUS(20)
034 62-34 -, IO BUS(21)
001 42B7 Mode Block Transport
403 E18
Read Mode Selected
-20
Write Mode Selected
DB 402 H26
WRITE
-25
402 G41
READ
402 D16
401 A1
036 60G30 IO Enable
401 F16
036 60K41 IO TRANSFER
-, Gi Core Store Address
-, Reset Status Register
405 K39
Enable Drum Start
401 G26
005 31J30 -, Synchronization Error
005 42-31 -, Data Overrun
402 C11
DRC Ready
(DRC Interrupt = DRC Ready)
004 53A3 DRC Power OK
008 58D15 -, NBS(15:23)=0
401 B4
006 5A9 Time000t150
401 C9


001 42-5 -, Mode Block Transport
006 5D32 Time600t750
BD401
T C C0
G31 -32
F33 -34
E35 -36
c b a ci
-, Cp CSA(5:22)
Cycle Call
-, Cycle Call
014 35C11 WORD(0)
014 34E35 WORD(5)
014 34B9 WORD(7)
014 35B9 WORD(1)
014 35A6 WORD(2)
014 34G31 WORD(3)
014 34F33 WORD(4)
014 34E35 WORD(5)
014 34C11 WORD(6)
014 34B9 WORD(7)
002 27H26 WRITE
014 35-12 -, WORD(0)
012 36H26 BIT(0:4)=23
002 27H26 WRITE
001 42B7 Mode Block Transport
002 44G41 READ
012 7A5 BIT(0:4)=1
DB402
H26 -25
K32 -31
WRITE&(WORD 254! WORD 255)
WORD(1:8)=0
014 35C11 WORD(0)
014 35-10 -, WORD(1)
014 35-8 -, WORD(2)
014 34-32 -, WORD(3)
014 34-34 -, WORD(4)
014 34-36 -, WORD(5)
014 34-12 -, WORD(6)
014 34-10 -, WORD(7)
014 34-8 -, WORD(8)
014 35-12 -, WORD(9)


014 34-10 -, Word(7)
CB402
F36
-38
E26
-18
401
H29
K33
S
R
BA
403
J36
Drum Speed OK
034 62C2 Address(N) & IO Address
402
F33
DRC Connected
FF405
1307E Minus 15 Volt Return
1307F Plus 25 Volt Return
1307H Plus 5 Volt Return
1307J Nul Volt Return
1308KK IO BUS Error
1308LL
-15V
+25V
+5V
0Volt
Power OK
DB402
D12
DRC Error
1308HH
1308JJ
DRC Power OK
1308MM 0 Volt
1308NN 0 Volt
1308PP 0 Volt
1308RR 0 Volt
1308SS Chassis
1308TT Chassis
-15 Volt 1307MM
+25 Volt 1307NN
+5 Volt spec 1307PP
0 Volt spec 1307RR
0 Volt
0 Volt 1307SS
0 Volt 1307TT

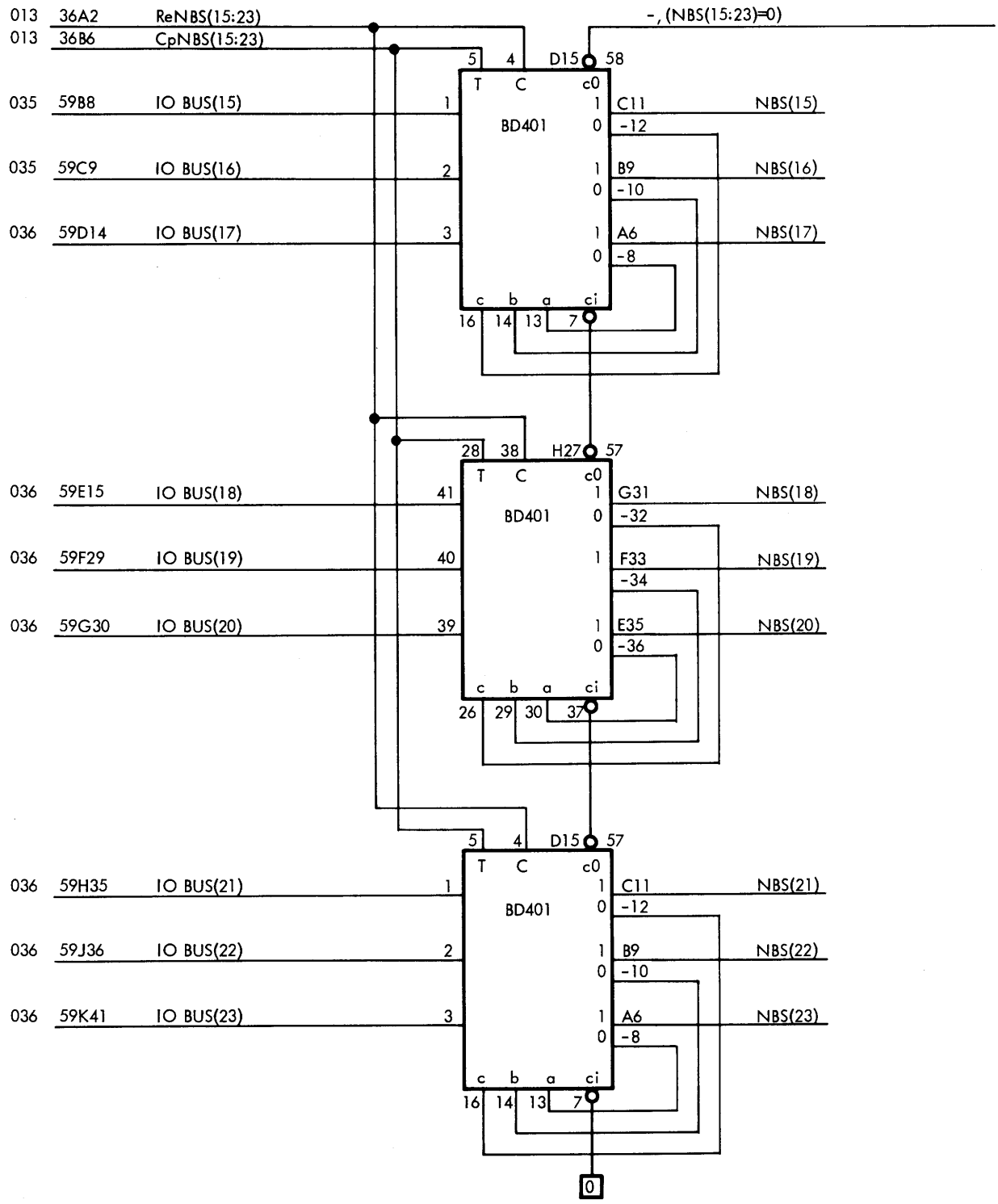

018 20A15 Equal(0:7)
019 20B18 Equal(8:15)
020 20C32 Equal(16:23)
002 44G41 READ
001 42B7 Mode Block Transport
012 36F18 Word(0:8)= 257
012 7C15 Bit(0:4)= 3
006 5B16 Time200t350
021 4F18 Enable Parity Control
021 28M40 -, Synchr Error
004 42J36 Drum Speed OK
WB(0:23) ≠ PW(0:23)
002 44G41 READ
001 42B7 Mode Block Transport
014 35-12 -, Word(0)
003 28K32 Word(1:8)= 0
012 7C15 Bit(0:4)= 3
006 5D32 Time600t750
021 4E13 Enable Address Control
002 43F16 -, Reset Status Register
003 58-36 -, Cycle Call
002 43F16 -, Reset Status Register
031 27B6 -, GiHDCData
017 32A9 -, (WRITE&Bit22&Time400t550)
002 44G41 READ
015 33-34 -, Bit(0)
015 33-36 -, Bit(1)
015 33-12 -, Bit(2)
015 33-10 -, Bit(3)
015 33-8 -, Bit(4)
006 5C30 Time400t550
402 D16
403 B18
403 C32
401 E13
402 E31
401 L38
401 M41
403 B18
S R BA 403 F25
S R BA 403 -23
402 A1
401 J30
S R BA 403 H33
S R BA 403 -31
401 A1
Parity Error
Synchronization Error
-, Synchronization Error
Data Overrun
-, Data Overrun
HDC Operating
Too Late
-, Address Error
-, Set Data Overrun
Status(0)
Status(1)
Status(2)
Status(3)
Status(4)
Status(23)

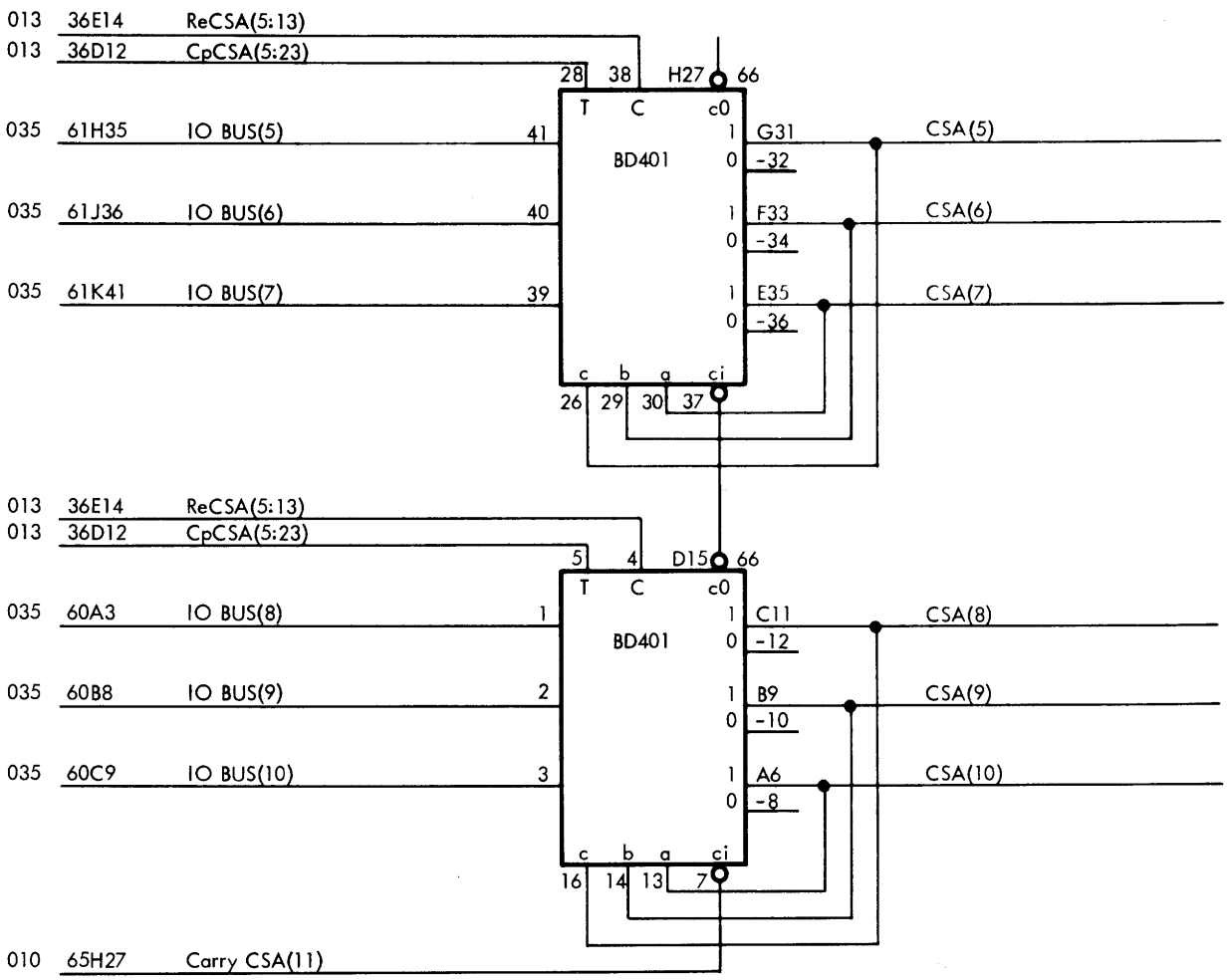

004 53A3 DRC Power OK
005 31J30 -, Synchronization Error
021 29K39 Write Enable
018 19-5 SP(0)
006 5-14 -, Time200t350
006 5-37 -, Time600t750
006 5-8 -, Time000t150
006 5-29 -, Time400t550
401
402
J30
M41
G26
H29
F32
A1
Enable Set
Enable Trig
Double Main Clock Puls
DB408
WE
WD
1307EE
1307FF
1307HH
1307JJ
1307KK
1307LL
C31
C7
-30
-, Read Strobe From Clock Track
1307K
1307L
DC407
G24
CB402
A9
-8
B16
-14
C30
-29
D32
-37
Time000t150
-, Time000t150
Time200t350
-, Time200t350
Time400t550
-, Time400t550
Time600t750
-, Time600t750
1307A
1307B
-, NRZ Data From Clock
1307C
1307D
NRZ Data From Clock Track
-, Time200t350
1307M
1307N
L36
-, Read Strobe From Data Track
1307AA
1307BB
-, NRZ Data From Data Track
1307CC
1307DD
NRZ Data From Data Track
5B16
Time200t350
A2
Drum Index
-1
-, Drum Index
D11
SP(24)
-12

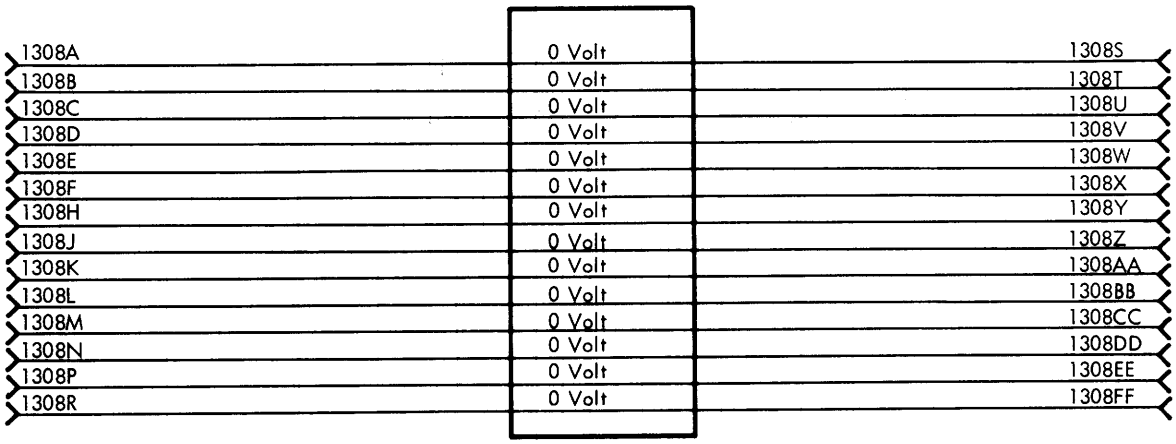


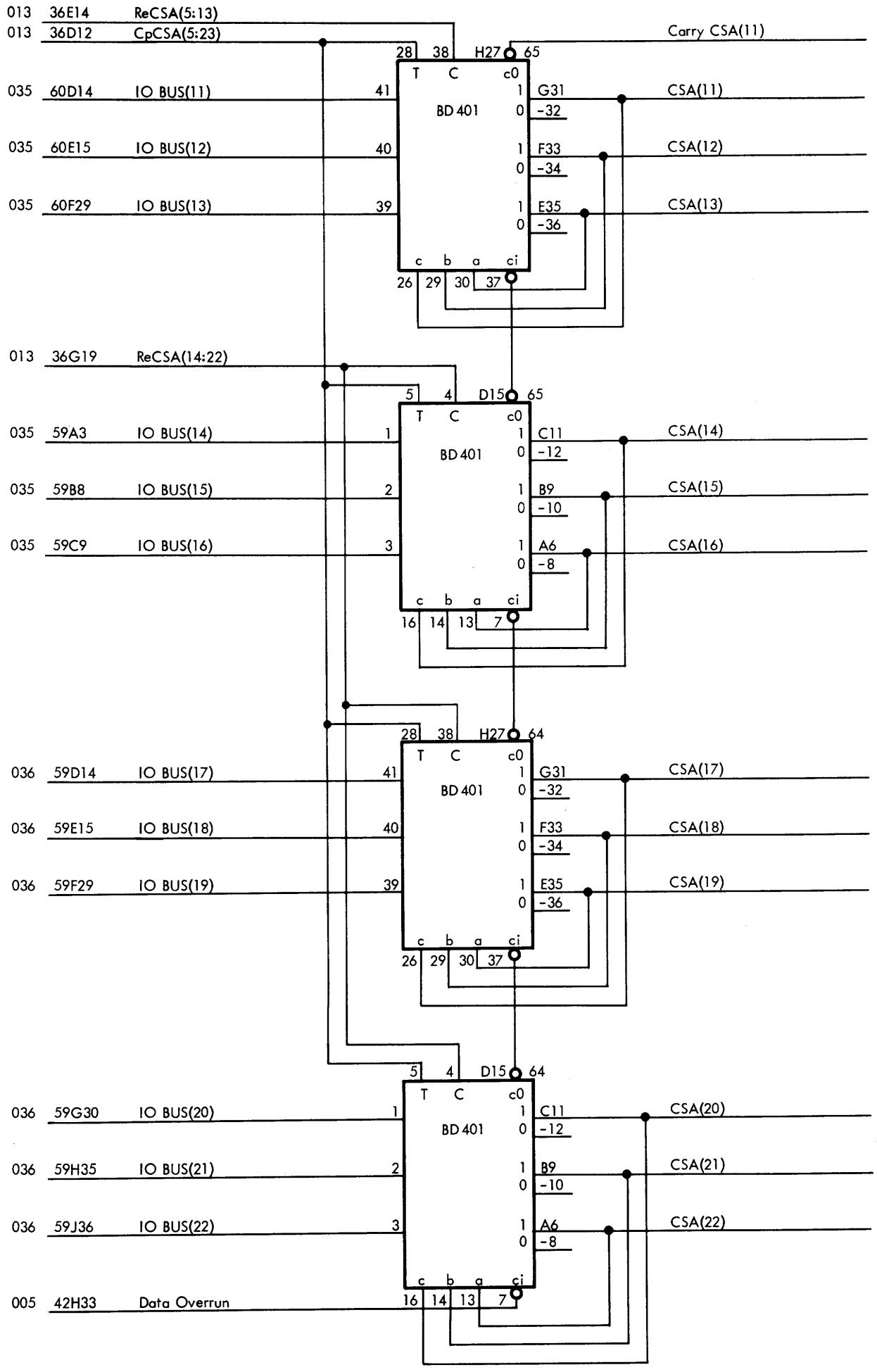
RC4000 DRUM SEGMENT ADDRESS, DSA(12:23) DRC007

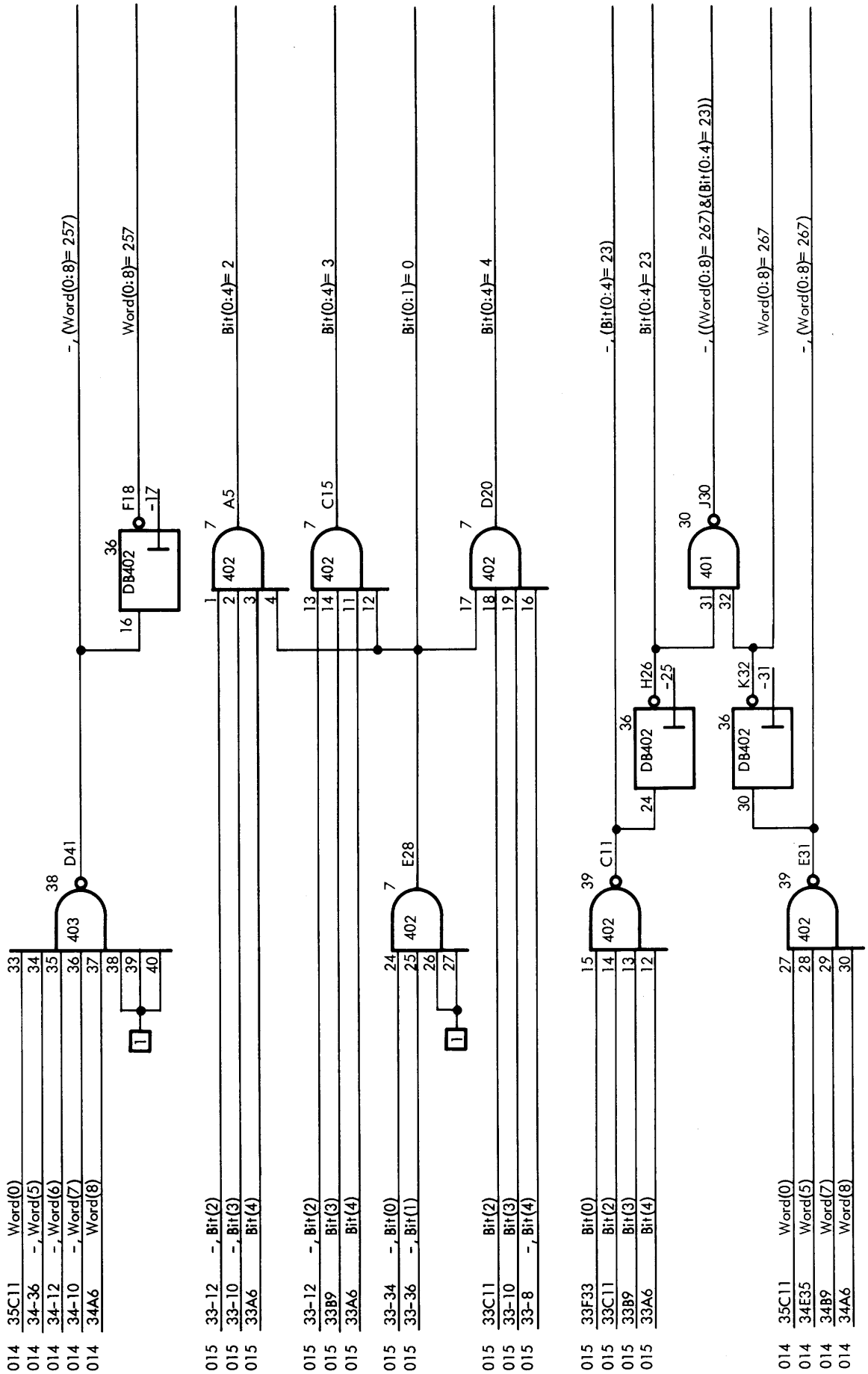
V11462 Logic Diagram


013 36A2 ReNBS(15:23)
013 36B6 CpNBS(15:23)
-, (NBS(15:23)=0)
BD401
035 59B8 IO BUS(15)
035 59C9 IO BUS(16)
036 59D14 IO BUS(17)
036 59E15 IO BUS(18)
036 59F29 IO BUS(19)
036 59G30 IO BUS(20)
036 59H35 IO BUS(21)
036 59J36 IO BUS(22)
036 59K41 IO BUS(23)
NBS(15)
NBS(16)
NBS(17)
NBS(18)
NBS(19)
NBS(20)
NBS(21)
NBS(22)
NBS(23)
C11
B9
A6
G31
F33
E35
-12
-10
-8
-32
-34
-36
D15
H27
T
C
c0
c
b
a
ci
0


013 36E14 ReCSA(5:13)
013 36D12 CpCSA(5:23)
28 38 H27 66
T C c0
035 61H35 IO BUS(5) 41
BD401
G31
-32
CSA(5)
035 61J36 IO BUS(6) 40
F33
-34
CSA(6)
035 61K41 IO BUS(7) 39
E35
-36
CSA(7)
c b a ci
26 29 30 37
013 36E14 ReCSA(5:13)
013 36D12 CpCSA(5:23)
5 4 D15 66
T C c0
035 60A3 IO BUS(8) 1
BD401
C11
-12
CSA(8)
035 60B8 IO BUS(9) 2
B9
-10
CSA(9)
035 60C9 IO BUS(10) 3
A6
-8
CSA(10)
c b a ci
16 14 13 7
010 65H27 Carry CSA(11)


1308A 0 Volt 1308S
1308B 0 Volt 1308T
1308C 0 Volt 1308U
1308D 0 Volt 1308V
1308E 0 Volt 1308W
1308F 0 Volt 1308X
1308H 0 Volt 1308Y
1308J 0 Volt 1308Z
1308K 0 Volt 1308AA
1308L 0 Volt 1308BB
1308M 0 Volt 1308CC
1308N 0 Volt 1308DD
1308P 0 Volt 1308EE
1308R 0 Volt 1308FF


013 36E14 ReCSA(5:13)
013 36D12 CpCSA(5:23)
Carry CSA(11)
28 38 H27 65
T C c0
035 60D14 IO BUS(11) 41 1 G31 CSA(11)
BD 401 0 -32
035 60E15 IO BUS(12) 40 1 F33 CSA(12)
0 -34
035 60F29 IO BUS(13) 39 1 E35 CSA(13)
0 -36
c b a ci
26 29 30 37
013 36G19 ReCSA(14:22)
5 4 D15 65
035 59A3 IO BUS(14) 1 C11 CSA(14)
035 59B8 IO BUS(15) 2 B9 CSA(15)
035 59C9 IO BUS(16) 3 A6 CSA(16)
16 14 13 7
28 38 H27 64
036 59D14 IO BUS(17) 41 G31 CSA(17)
036 59E15 IO BUS(18) 40 F33 CSA(18)
036 59F29 IO BUS(19) 39 E35 CSA(19)
26 29 30 37
5 4 D15 64
036 59G30 IO BUS(20) 1 C11 CSA(20)
036 59H35 IO BUS(21) 2 B9 CSA(21)
036 59J36 IO BUS(22) 3 A6 CSA(22)
005 42H33 Data Overrun 16 14 13 7



RC4000

BIT AND WORD REGISTER DECODINGS

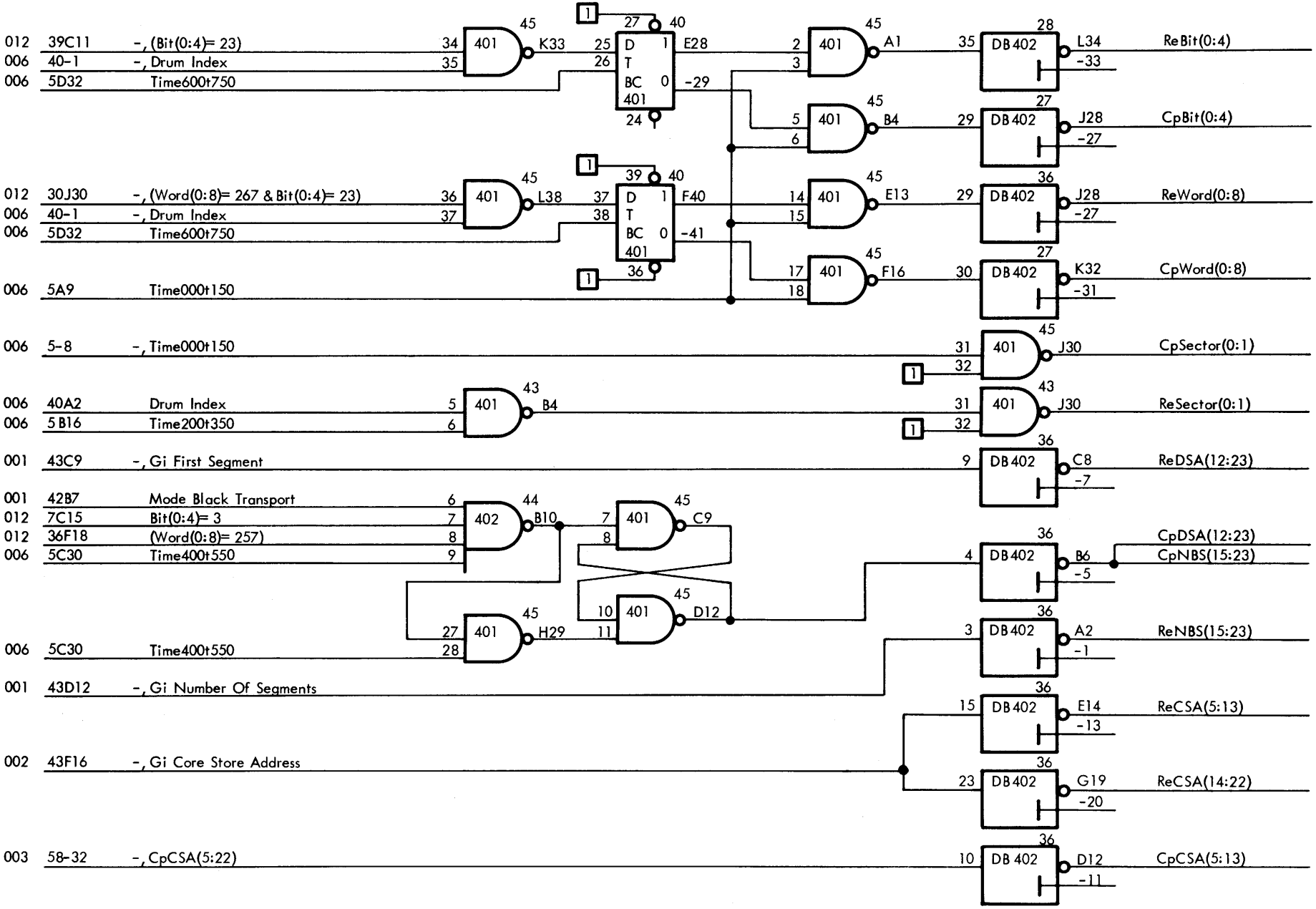
DRC012

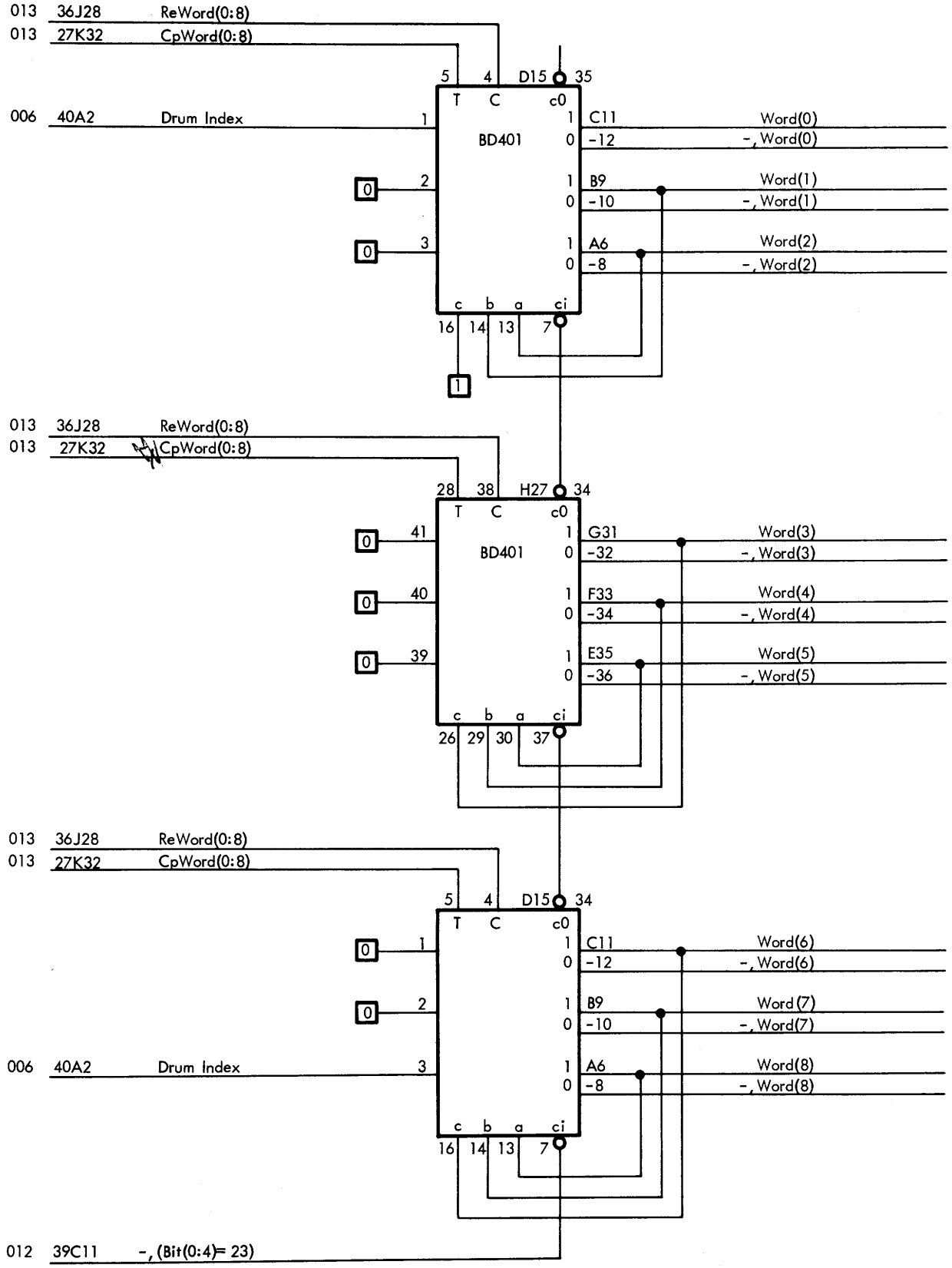
V11466

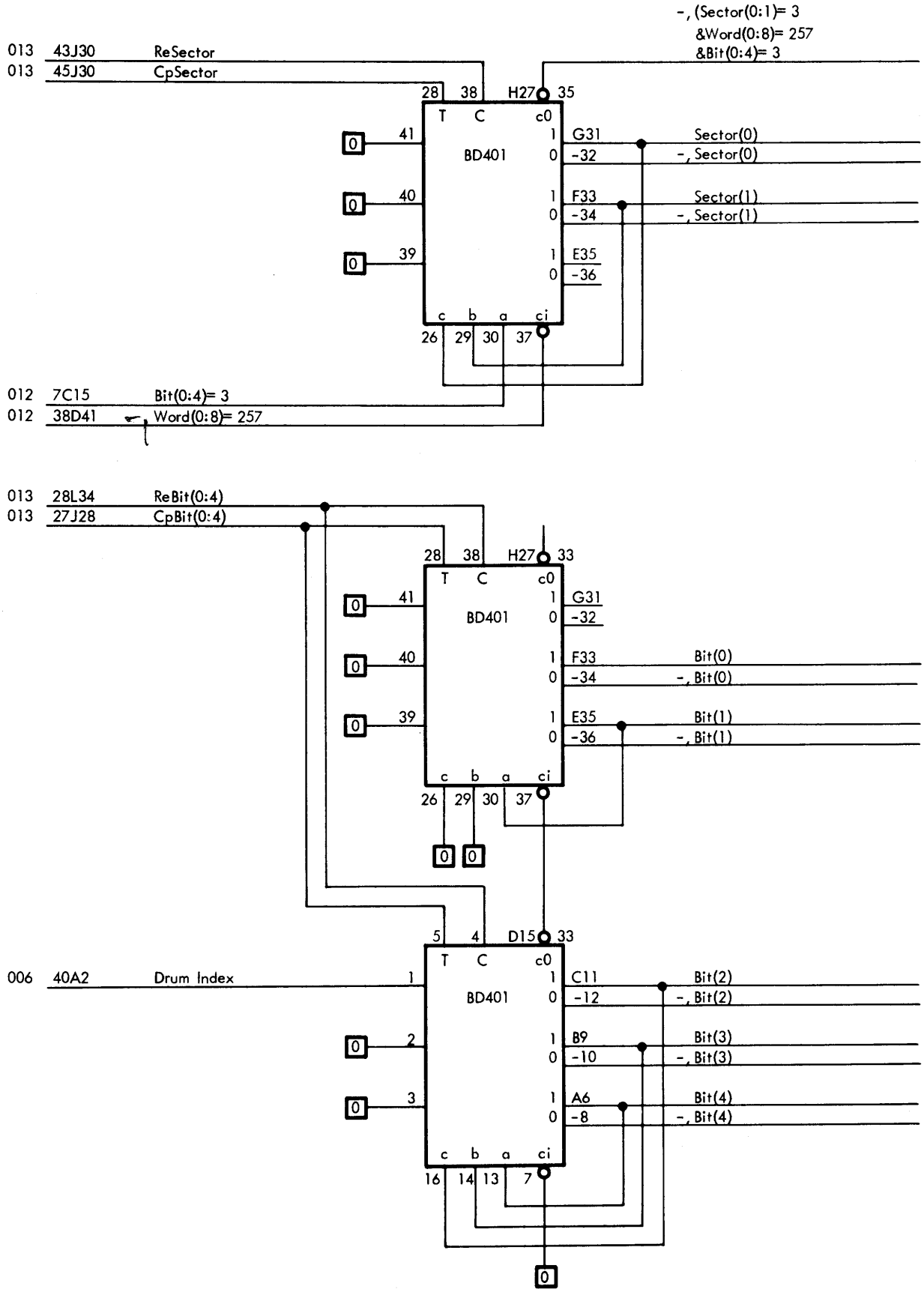
Logic Diagram

CONTROL SIGNALS FOR BIT, WORD, SECTOR, DSA, NBS, AND CSA

Logic Diagram

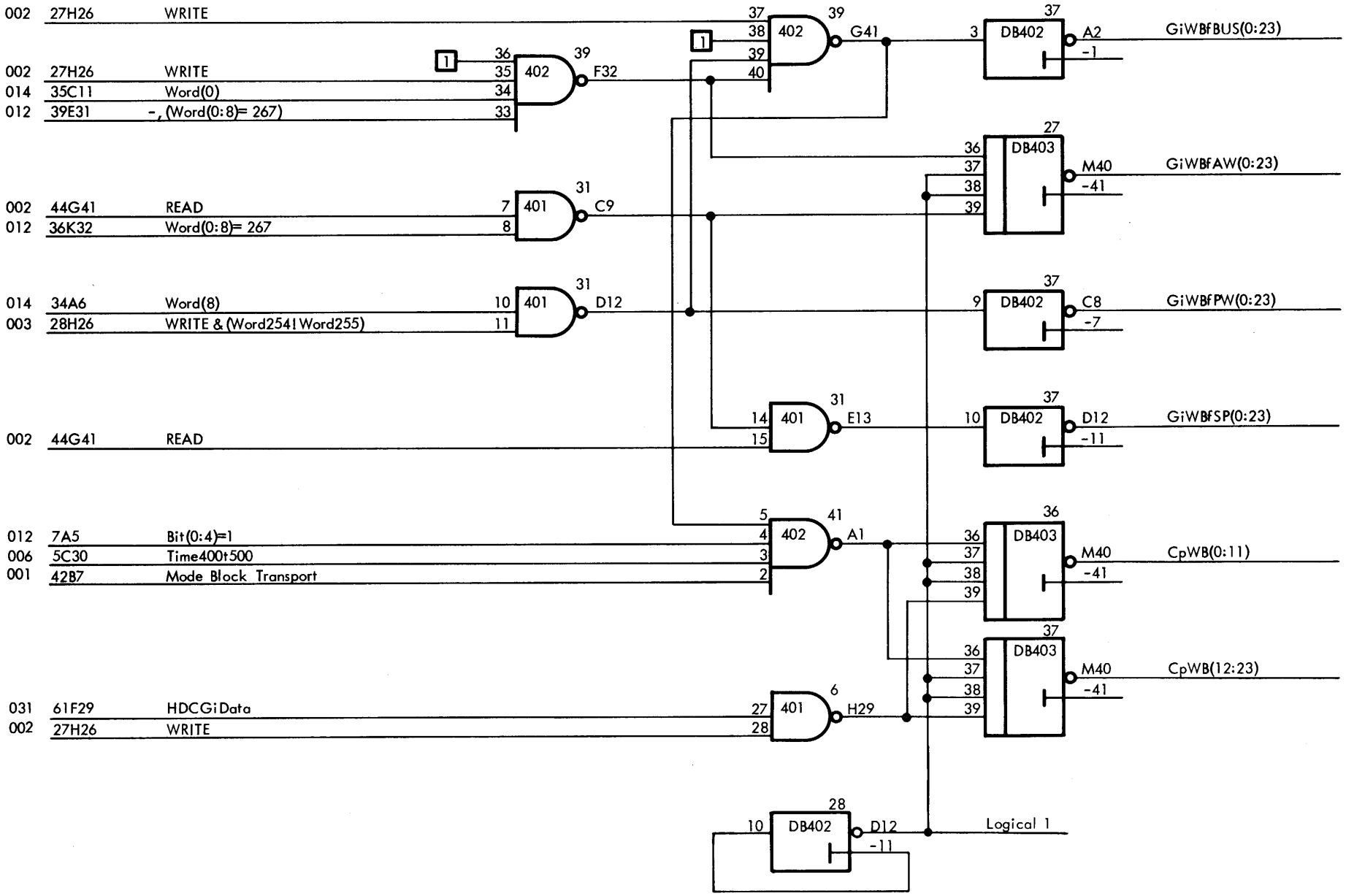


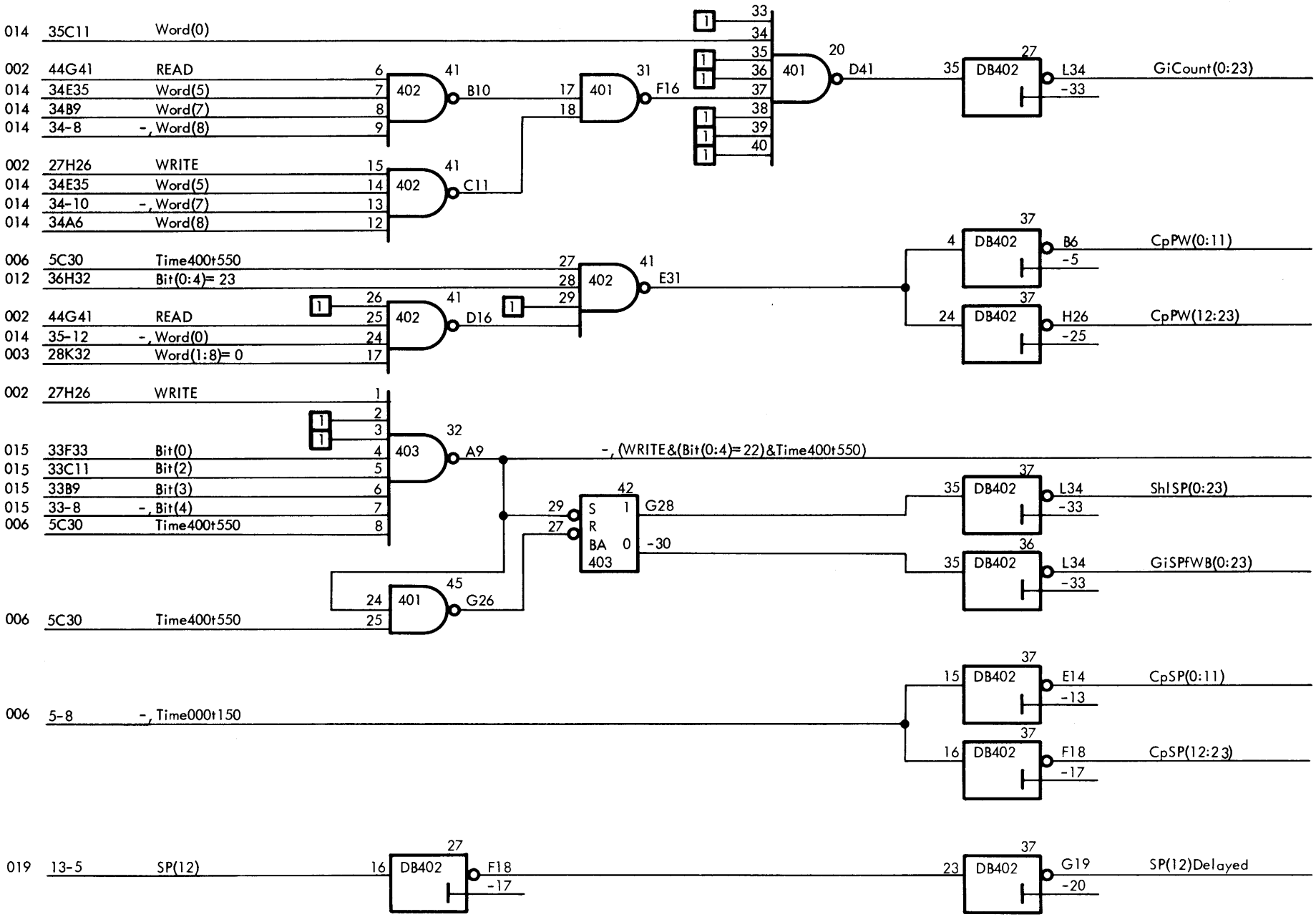

013 36J28 ReWord(0:8)
013 27K32 CpWord(0:8)
006 40A2 Drum Index
BD401
C11
B9
A6
-12
-10
-8
Word(0)
-, Word(0)
Word(1)
-, Word(1)
Word(2)
-, Word(2)
013 36J28 ReWord(0:8)
013 27K32 CpWord(0:8)
BD401
G31
F33
E35
-32
-34
-36
Word(3)
-, Word(3)
Word(4)
-, Word(4)
Word(5)
-, Word(5)
013 36J28 ReWord(0:8)
013 27K32 CpWord(0:8)
006 40A2 Drum Index
C11
B9
A6
-12
-10
-8
Word(6)
-, Word(6)
Word(7)
-, Word(7)
Word(8)
-, Word(8)
012 39C11 -, (Bit(0:4)= 23)

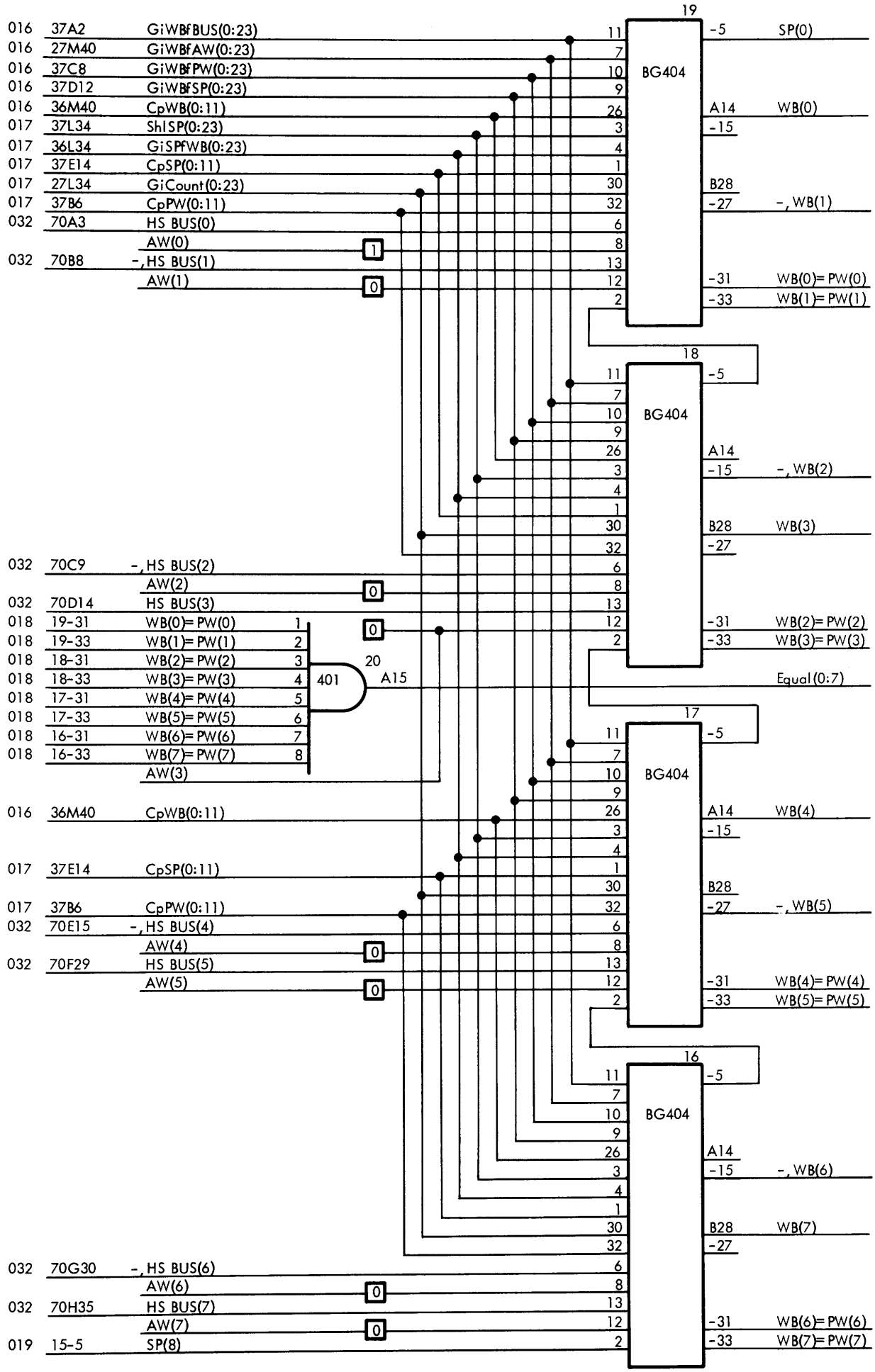

-, (Sector(0:1)= 3
&Word(0:8)= 257
&Bit(0:4)= 3
013 43J30 ReSector
013 45J30 CpSector
28 38 H27 35
T C c0
BD401
41 40 39
G31 -32 F33 -34 E35 -36
Sector(0) -, Sector(0) Sector(1) -, Sector(1)
c b a ci
26 29 30 37
012 7C15 Bit(0:4)= 3
012 38D41 Word(0:8)= 257
013 28L34 ReBit(0:4)
013 27J28 CpBit(0:4)
28 38 H27 33
41 40 39
G31 -32 F33 -34 E35 -36
Bit(0) -, Bit(0) Bit(1) -, Bit(1)
26 29 30 37
5 4 D15 33
006 40A2 Drum Index
1 2 3
C11 -12 B9 -10 A6 -8
Bit(2) -, Bit(2) Bit(3) -, Bit(3) Bit(4) -, Bit(4)
16 14 13 7

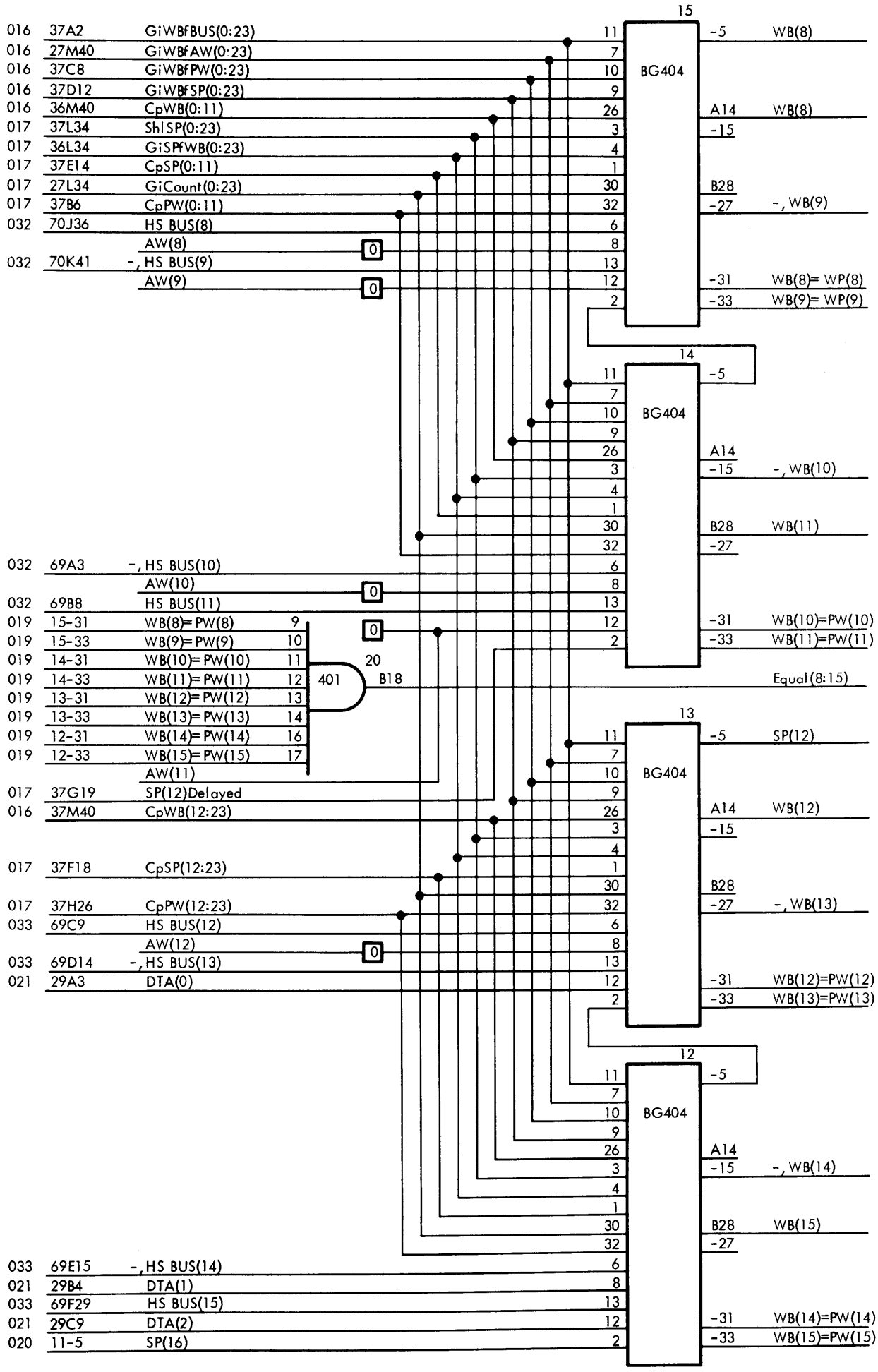
CONTROL SIGNALS FOR WORD BUFFER

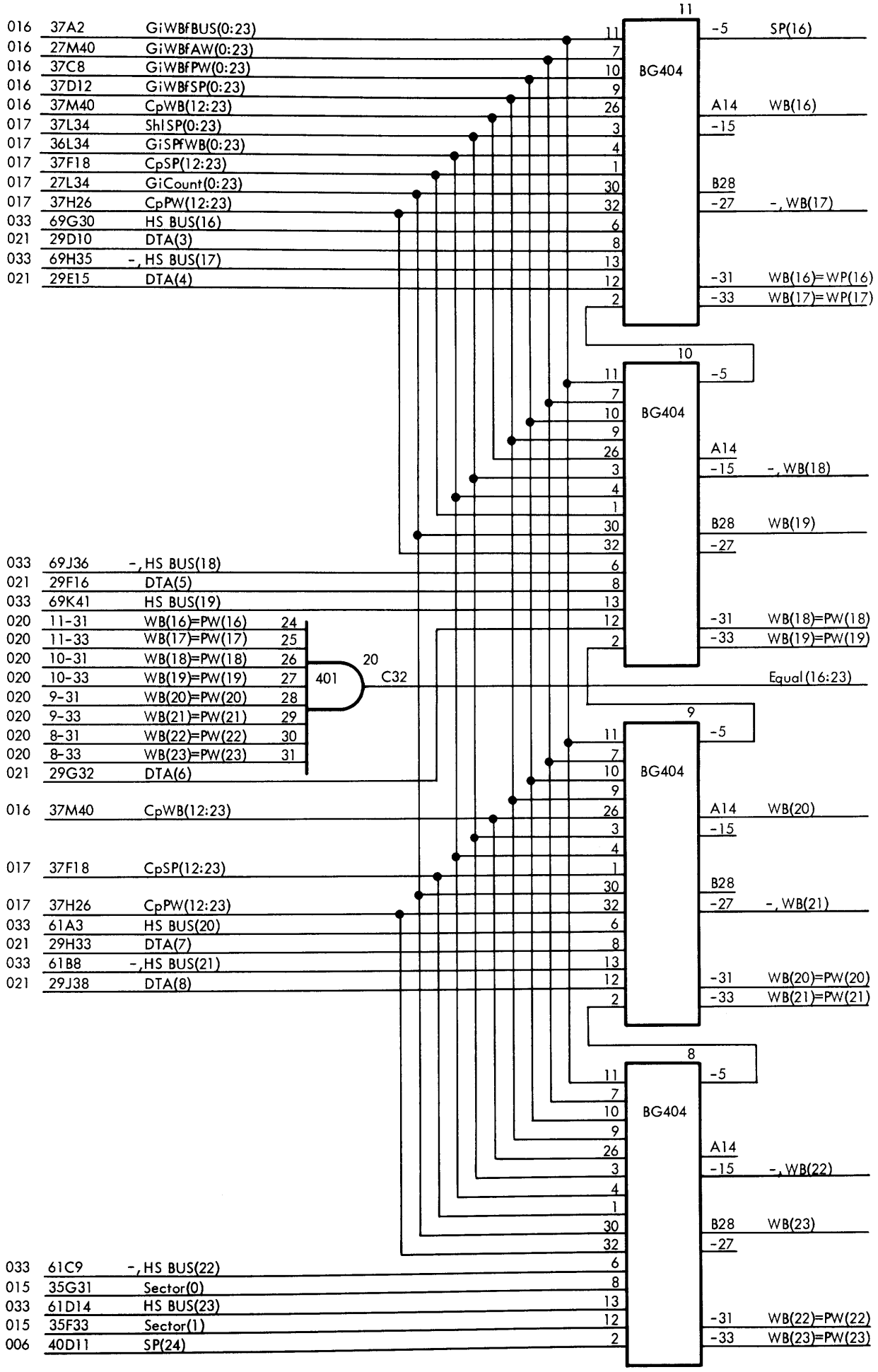
Logic Diagram




014 35C11 Word(0)
002 44G41 READ
014 34E35 Word(5)
014 34B9 Word(7)
014 34-8 -, Word(8)
402 B10
401 F16
401 D41
DB402 L34 -33
GiCount(0:23)
002 27H26 WRITE
014 34E35 Word(5)
014 34-10 -, Word(7)
014 34A6 Word(8)
402 C11
006 5C30 Time400t550
012 36H32 Bit(0:4)= 23
402 E31
002 44G41 READ
014 35-12 -, Word(0)
003 28K32 Word(1:8)= 0
402 D16
DB402 B6 -5
CpPW(0:11)
DB402 H26 -25
CpPW(12:23)
002 27H26 WRITE
015 33F33 Bit(0)
015 33C11 Bit(2)
015 33B9 Bit(3)
015 33-8 -, Bit(4)
006 5C30 Time400t550
403 A9
-, (WRITE&(Bit(0:4)=22)&Time400t550)
S R BA 403 G28 -30
DB402 L34 -33
ShISP(0:23)
DB402 L34 -33
GiSPfWB(0:23)
006 5C30 Time400t550
401 G26
006 5-8 -, Time000t150
DB402 E14 -13
CpSP(0:11)
DB402 F18 -17
CpSP(12:23)
019 13-5 SP(12)
DB402 F18 -17
DB402 G19 -20
SP(12)Delayed

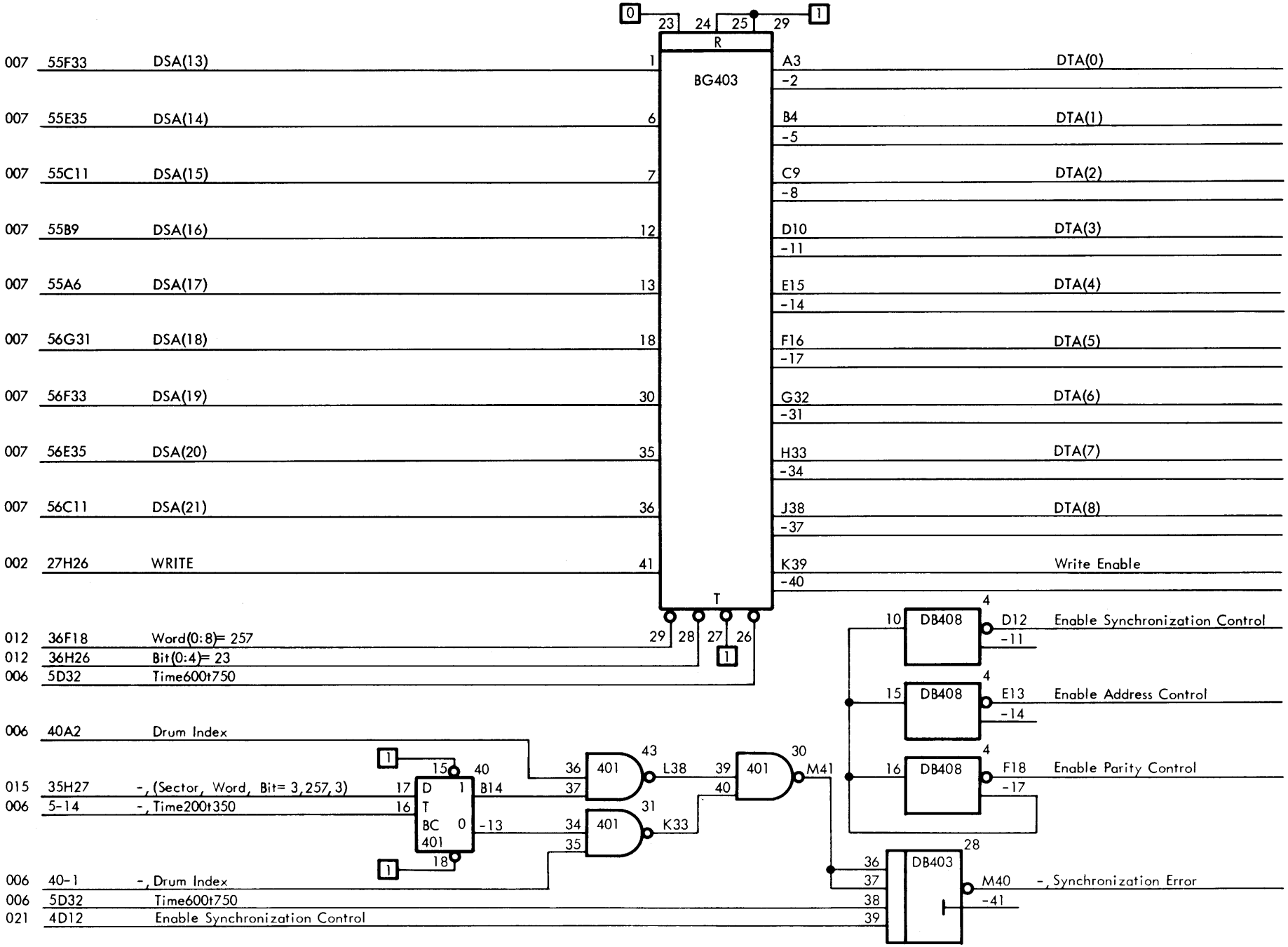

016 37A2 GiWBfBUS(0:23)
016 27M40 GiWBfAW(0:23)
016 37C8 GiWBfPW(0:23)
016 37D12 GiWBfSP(0:23)
016 36M40 CpWB(0:11)
017 37L34 ShISP(0:23)
017 36L34 GiSPfWB(0:23)
017 37E14 CpSP(0:11)
017 27L34 GiCount(0:23)
017 37B6 CpPW(0:11)
032 70A3 HS BUS(0)
AW(0)
032 70B8 -,HS BUS(1)
AW(1)
032 70C9 -,HS BUS(2)
AW(2)
032 70D14 HS BUS(3)
018 19-31 WB(0)= PW(0)
018 19-33 WB(1)= PW(1)
018 18-31 WB(2)= PW(2)
018 18-33 WB(3)= PW(3)
018 17-31 WB(4)= PW(4)
018 17-33 WB(5)= PW(5)
018 16-31 WB(6)= PW(6)
018 16-33 WB(7)= PW(7)
AW(3)
401
20
A15
016 36M40 CpWB(0:11)
017 37E14 CpSP(0:11)
017 37B6 CpPW(0:11)
032 70E15 -,HS BUS(4)
AW(4)
032 70F29 HS BUS(5)
AW(5)
032 70G30 -,HS BUS(6)
AW(6)
032 70H35 HS BUS(7)
AW(7)
019 15-5 SP(8)
19
BG404
-5 SP(0)
A14 WB(0)
-15
B28
-27 -,WB(1)
-31 WB(0)= PW(0)
-33 WB(1)= PW(1)
18
BG404
-5
A14
-15 -,WB(2)
B28 WB(3)
-27
-31 WB(2)= PW(2)
-33 WB(3)= PW(3)
Equal(0:7)
17
BG404
-5
A14 WB(4)
-15
B28
-27 -,WB(5)
-31 WB(4)= PW(4)
-33 WB(5)= PW(5)
16
BG404
-5
A14
-15 -,WB(6)
B28 WB(7)
-27
-31 WB(6)= PW(6)
-33 WB(7)= PW(7)

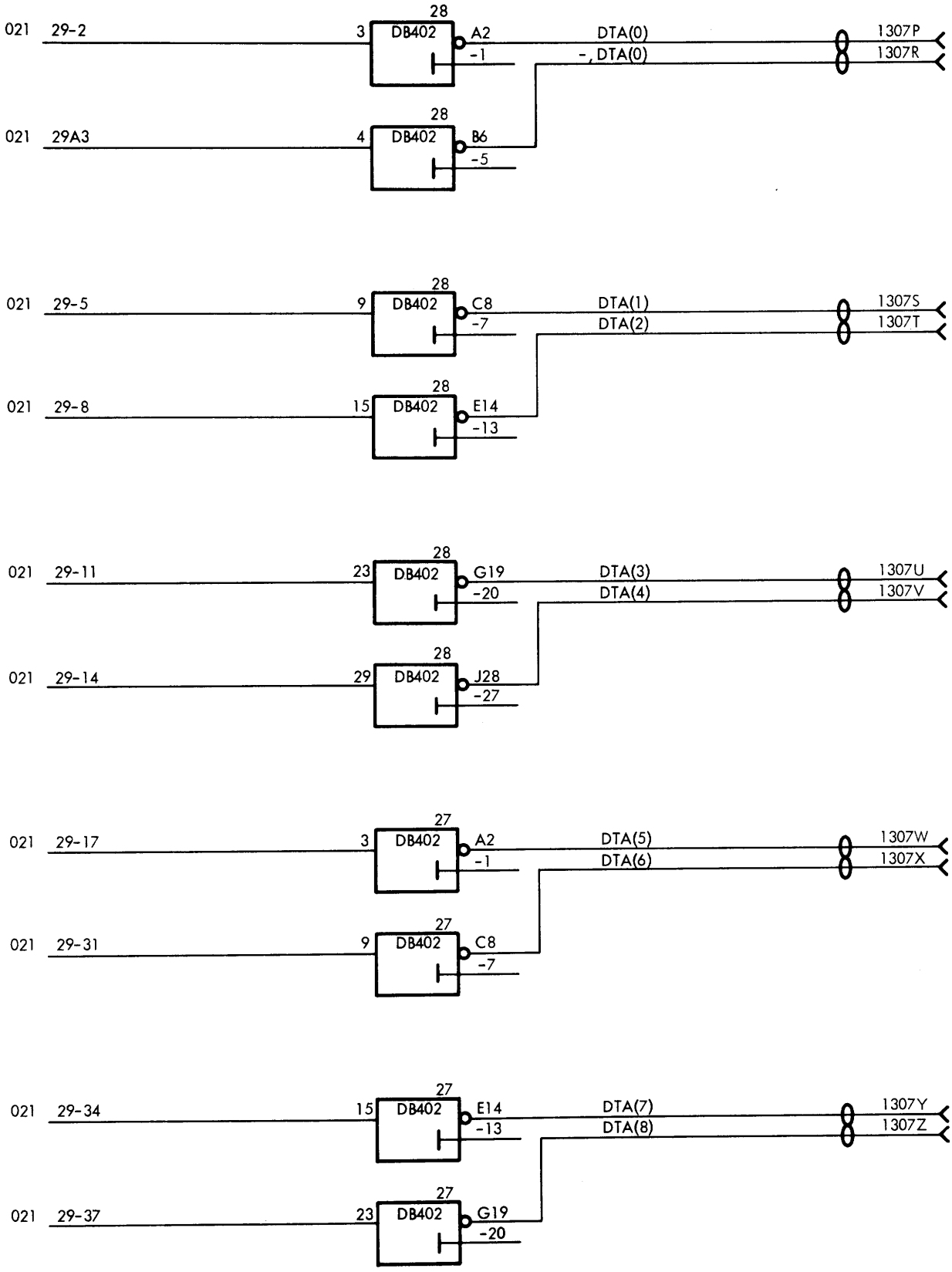

15
016 37A2 GiWBfBUS(0:23)
016 27M40 GiWBfAW(0:23)
016 37C8 GiWBfPW(0:23)
016 37D12 GiWBfSP(0:23)
016 36M40 CpWB(0:11)
017 37L34 ShlSP(0:23)
017 36L34 GiSPfWB(0:23)
017 37E14 CpSP(0:11)
017 27L34 GiCount(0:23)
017 37B6 CpPW(0:11)
032 70J36 HS BUS(8)
AW(8)
032 70K41 -, HS BUS(9)
AW(9)
BG404
-5 WB(8)
A14 WB(8)
-15
B28
-27 -, WB(9)
-31 WB(8)= WP(8)
-33 WB(9)= WP(9)
14
BG404
-5
A14
-15 -, WB(10)
B28 WB(11)
-27
-31 WB(10)=PW(10)
-33 WB(11)=PW(11)
032 69A3 -, HS BUS(10)
AW(10)
032 69B8 HS BUS(11)
019 15-31 WB(8)= PW(8) 9
019 15-33 WB(9)= PW(9) 10
019 14-31 WB(10)= PW(10) 11
019 14-33 WB(11)= PW(11) 12
019 13-31 WB(12)= PW(12) 13
019 13-33 WB(13)= PW(13) 14
019 12-31 WB(14)= PW(14) 16
019 12-33 WB(15)= PW(15) 17
AW(11)
20
401 B18
Equal(8:15)
13
BG404
-5 SP(12)
A14 WB(12)
-15
B28
-27 -, WB(13)
-31 WB(12)=PW(12)
-33 WB(13)=PW(13)
017 37G19 SP(12)Delayed
016 37M40 CpWB(12:23)
017 37F18 CpSP(12:23)
017 37H26 CpPW(12:23)
033 69C9 HS BUS(12)
AW(12)
033 69D14 -, HS BUS(13)
021 29A3 DTA(0)
12
BG404
-5
A14
-15 -, WB(14)
B28 WB(15)
-27
-31 WB(14)=PW(14)
-33 WB(15)=PW(15)
033 69E15 -, HS BUS(14)
021 29B4 DTA(1)
033 69F29 HS BUS(15)
021 29C9 DTA(2)
020 11-5 SP(16)

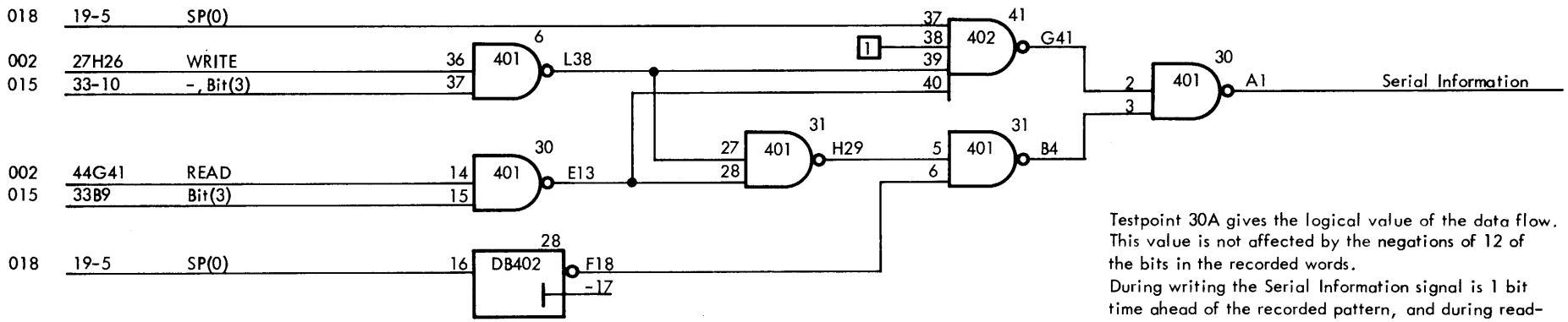

016 37A2 GiWBfBUS(0:23)
016 27M40 GiWBfAW(0:23)
016 37C8 GiWBfPW(0:23)
016 37D12 GiWBfSP(0:23)
016 37M40 CpWB(12:23)
017 37L34 ShlSP(0:23)
017 36L34 GiSPfWB(0:23)
017 37F18 CpSP(12:23)
017 27L34 GiCount(0:23)
017 37H26 CpPW(12:23)
033 69G30 HS BUS(16)
021 29D10 DTA(3)
033 69H35 -, HS BUS(17)
021 29E15 DTA(4)
033 69J36 -, HS BUS(18)
021 29F16 DTA(5)
033 69K41 HS BUS(19)
020 11-31 WB(16)=PW(16) 24
020 11-33 WB(17)=PW(17) 25
020 10-31 WB(18)=PW(18) 26
020 10-33 WB(19)=PW(19) 27
020 9-31 WB(20)=PW(20) 28
020 9-33 WB(21)=PW(21) 29
020 8-31 WB(22)=PW(22) 30
020 8-33 WB(23)=PW(23) 31
401
20
C32
021 29G32 DTA(6)
016 37M40 CpWB(12:23)
017 37F18 CpSP(12:23)
017 37H26 CpPW(12:23)
033 61A3 HS BUS(20)
021 29H33 DTA(7)
033 61B8 -, HS BUS(21)
021 29J38 DTA(8)
033 61C9 -, HS BUS(22)
015 35G31 Sector(0)
033 61D14 HS BUS(23)
015 35F33 Sector(1)
006 40D11 SP(24)
11
BG404
-5 SP(16)
A14 -15 WB(16)
B28 -27 -, WB(17)
-31 WB(16)=WP(16)
-33 WB(17)=WP(17)
10
BG404
-5
A14 -15 -, WB(18)
B28 -27 WB(19)
-31 WB(18)=PW(18)
-33 WB(19)=PW(19)
Equal(16:23)
9
BG404
-5
A14 -15 WB(20)
B28 -27 -, WB(21)
-31 WB(20)=PW(20)
-33 WB(21)=PW(21)
8
BG404
-5
A14 -15 -, WB(22)
B28 -27 WB(23)
-31 WB(22)=PW(22)
-33 WB(23)=PW(23)

DRUM TRACK ADDRESS, DTA(0:8), AND ENABLING OF CONTROLS

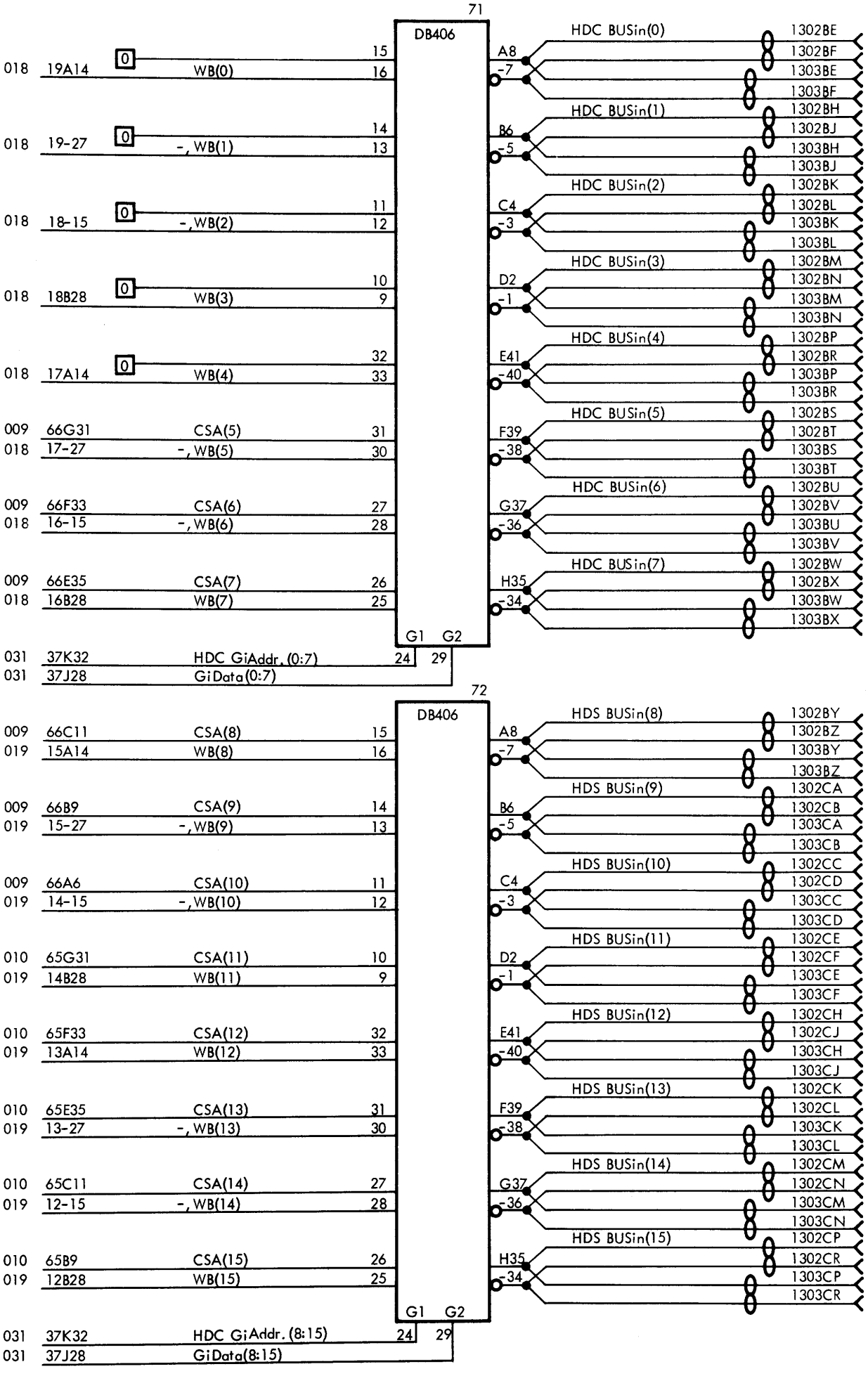
Logic Diagram

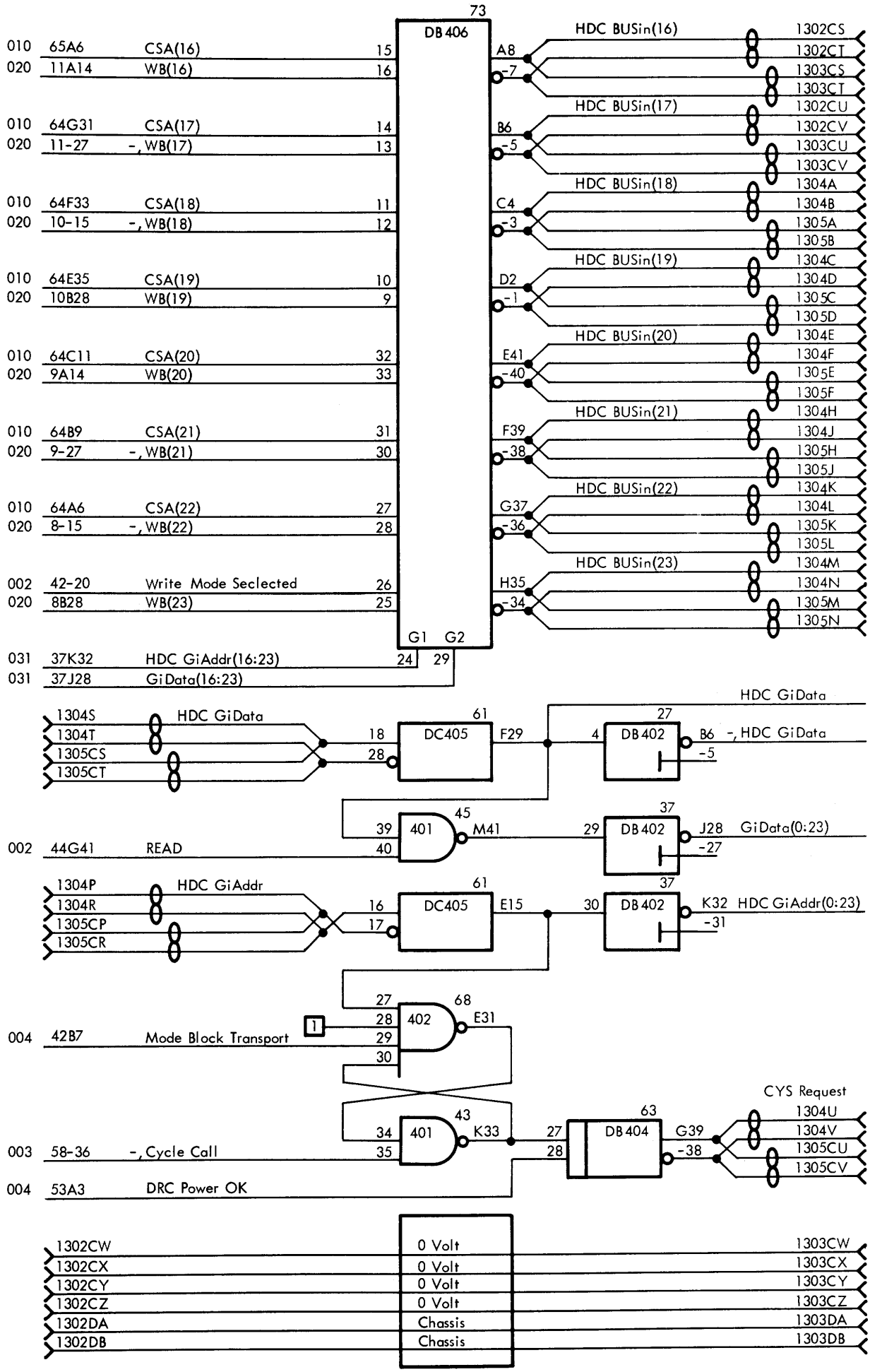


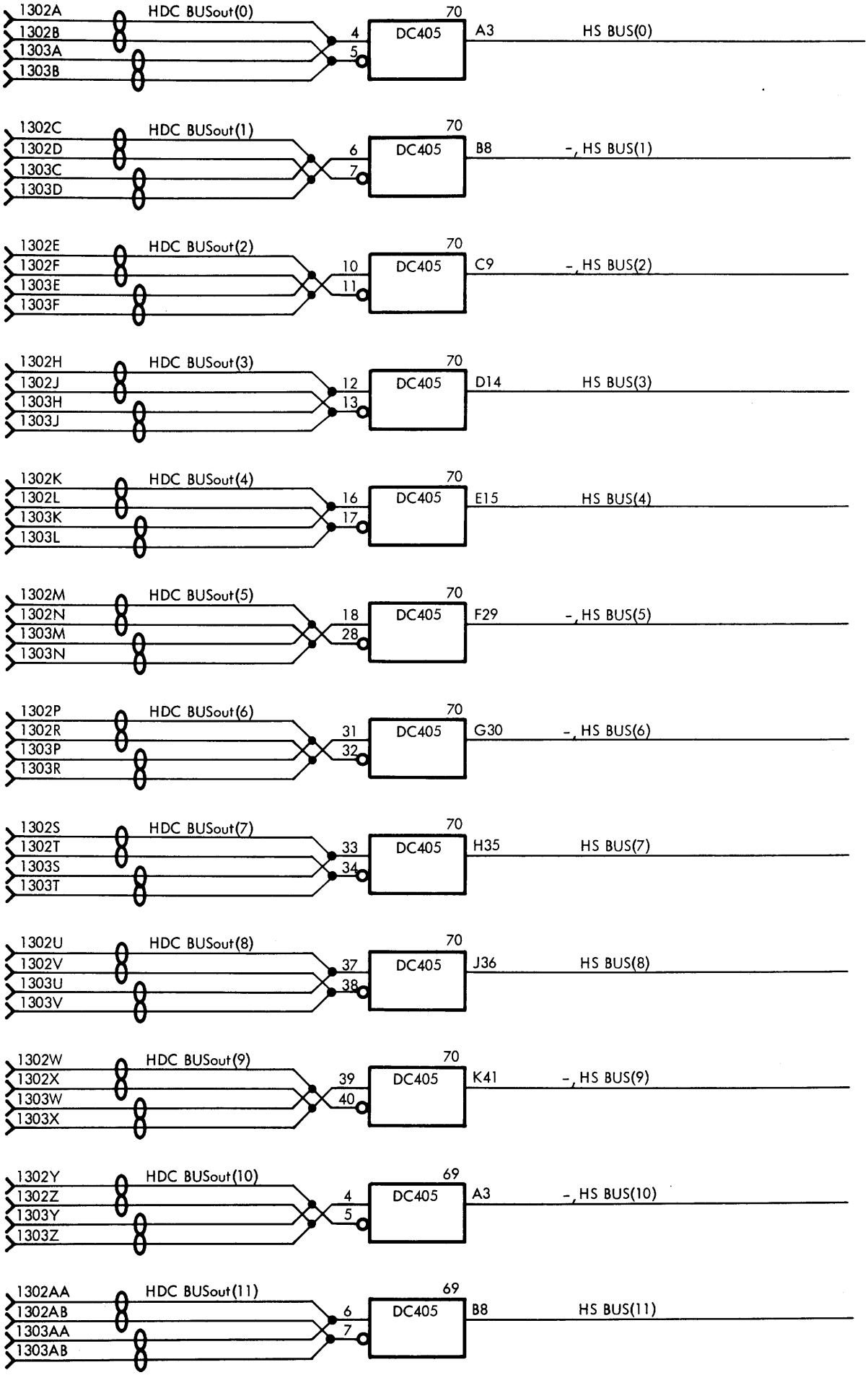

021 29-2
3
28
DB402
A2
-1
DTA(0)
-, DTA(0)
1307P
1307R
021 29A3
4
28
DB402
B6
-5
021 29-5
9
28
DB402
C8
-7
DTA(1)
DTA(2)
1307S
1307T
021 29-8
15
28
DB402
E14
-13
021 29-11
23
28
DB402
G19
-20
DTA(3)
DTA(4)
1307U
1307V
021 29-14
29
28
DB402
J28
-27
021 29-17
3
27
DB402
A2
-1
DTA(5)
DTA(6)
1307W
1307X
021 29-31
9
27
DB402
C8
-7
021 29-34
15
27
DB402
E14
-13
DTA(7)
DTA(8)
1307Y
1307Z
021 29-37
23
27
DB402
G19
-20

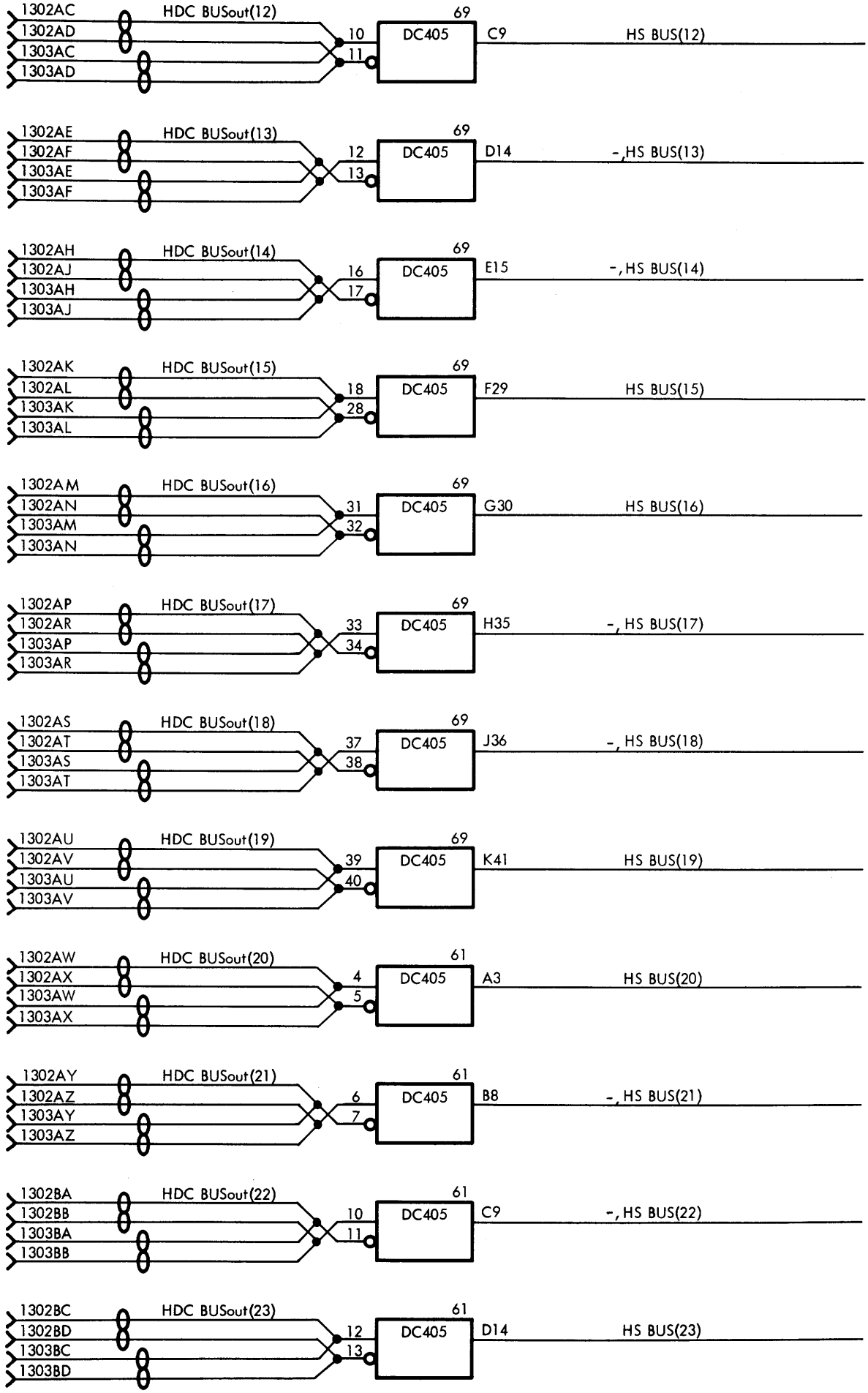


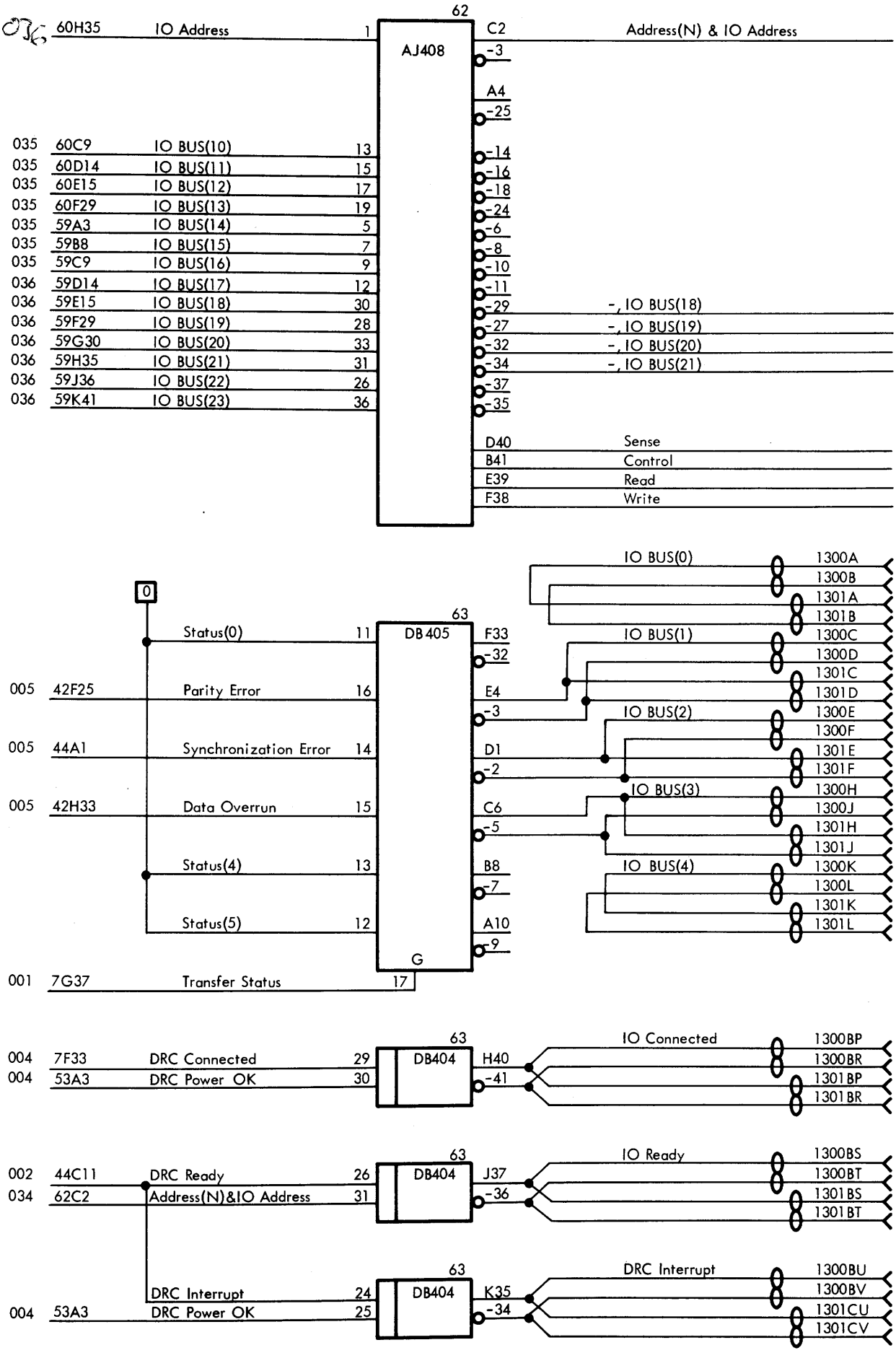
Testpoint 30A gives the logical value of the data flow. This value is not affected by the negations of 12 of the bits in the recorded words.
During writing the Serial Information signal is 1 bit time ahead of the recorded pattern, and during reading, the Serial Information signal is 1 Word time plus 1 bit time delayed in comparison with the recorded pattern.

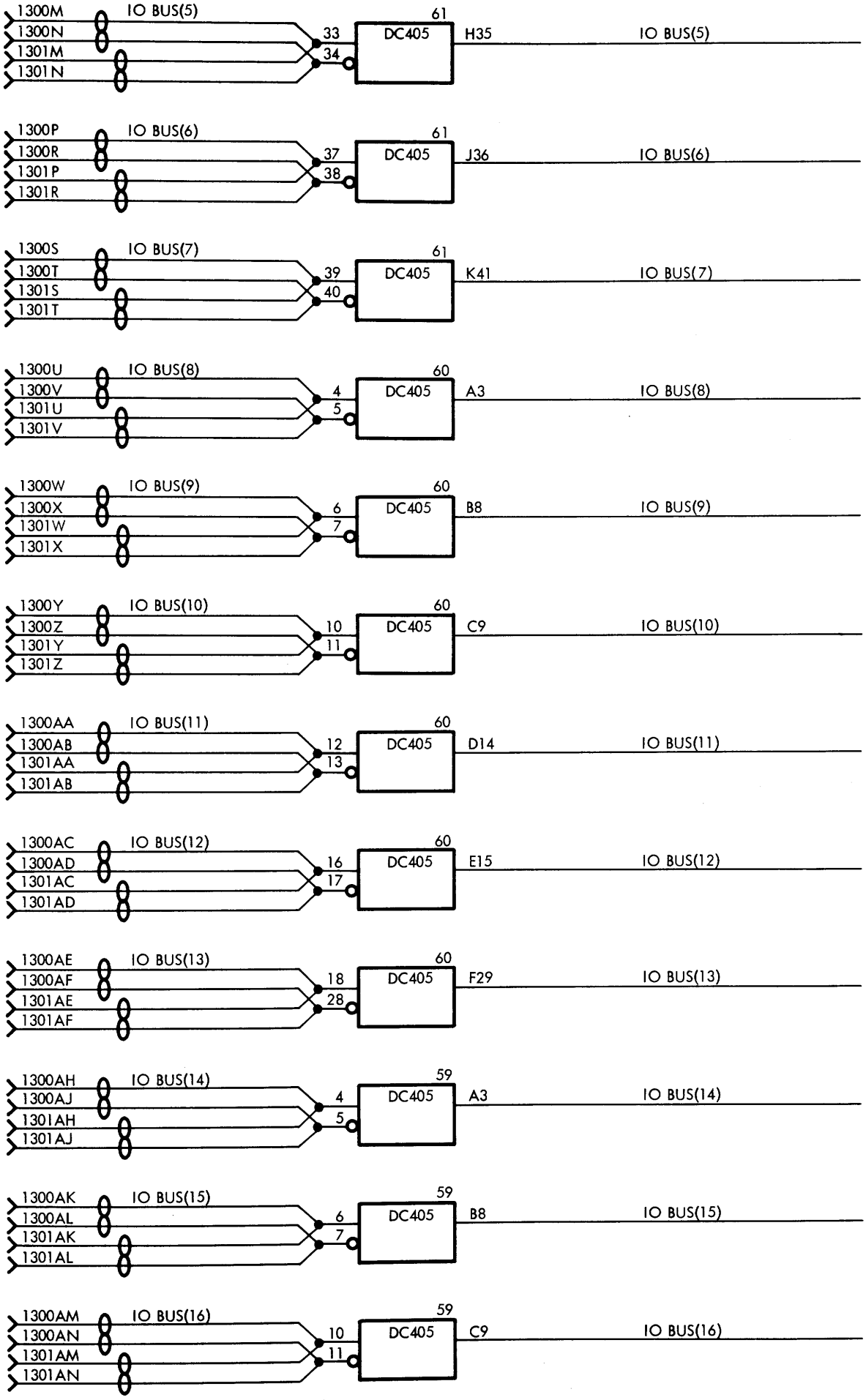

71
DB406
018 19A14 WB(0) 15 16
018 19-27 -,WB(1) 14 13
018 18-15 -,WB(2) 11 12
018 18B28 WB(3) 10 9
018 17A14 WB(4) 32 33
009 66G31 CSA(5) 31
018 17-27 -,WB(5) 30
009 66F33 CSA(6) 27
018 16-15 -,WB(6) 28
009 66E35 CSA(7) 26
018 16B28 WB(7) 25
G1 G2
031 37K32 HDC GiAddr.(0:7) 24 29
031 37J28 GiData(0:7)
A8 -7 HDC BUSin(0) 1302BE 1302BF 1303BE 1303BF
B6 -5 HDC BUSin(1) 1302BH 1302BJ 1303BH 1303BJ
C4 -3 HDC BUSin(2) 1302BK 1302BL 1303BK 1303BL
D2 -1 HDC BUSin(3) 1302BM 1302BN 1303BM 1303BN
E41 -40 HDC BUSin(4) 1302BP 1302BR 1303BP 1303BR
F39 -38 HDC BUSin(5) 1302BS 1302BT 1303BS 1303BT
G37 -36 HDC BUSin(6) 1302BU 1302BV 1303BU 1303BV
H35 -34 HDC BUSin(7) 1302BW 1302BX 1303BW 1303BX
72
DB406
009 66C11 CSA(8) 15
019 15A14 WB(8) 16
009 66B9 CSA(9) 14
019 15-27 -,WB(9) 13
009 66A6 CSA(10) 11
019 14-15 -,WB(10) 12
010 65G31 CSA(11) 10
019 14B28 WB(11) 9
010 65F33 CSA(12) 32
019 13A14 WB(12) 33
010 65E35 CSA(13) 31
019 13-27 -,WB(13) 30
010 65C11 CSA(14) 27
019 12-15 -,WB(14) 28
010 65B9 CSA(15) 26
019 12B28 WB(15) 25
G1 G2
031 37K32 HDC GiAddr.(8:15) 24 29
031 37J28 GiData(8:15)
A8 -7 HDS BUSin(8) 1302BY 1302BZ 1303BY 1303BZ
B6 -5 HDS BUSin(9) 1302CA 1302CB 1303CA 1303CB
C4 -3 HDS BUSin(10) 1302CC 1302CD 1303CC 1303CD
D2 -1 HDS BUSin(11) 1302CE 1302CF 1303CE 1303CF
E41 -40 HDS BUSin(12) 1302CH 1302CJ 1303CH 1303CJ
F39 -38 HDS BUSin(13) 1302CK 1302CL 1303CK 1303CL
G37 -36 HDS BUSin(14) 1302CM 1302CN 1303CM 1303CN
H35 -34 HDS BUSin(15) 1302CP 1302CR 1303CP 1303CR


73
DB406
010 65A6 CSA(16) 15
020 11A14 WB(16) 16
010 64G31 CSA(17) 14
020 11-27 -,WB(17) 13
010 64F33 CSA(18) 11
020 10-15 -,WB(18) 12
010 64E35 CSA(19) 10
020 10B28 WB(19) 9
010 64C11 CSA(20) 32
020 9A14 WB(20) 33
010 64B9 CSA(21) 31
020 9-27 -,WB(21) 30
010 64A6 CSA(22) 27
020 8-15 -,WB(22) 28
002 42-20 Write Mode Seclected 26
020 8B28 WB(23) 25
G1 G2
031 37K32 HDC GiAddr(16:23) 24 29
031 37J28 GiData(16:23)
A8 -7
B6 -5
C4 -3
D2 -1
E41 -40
F39 -38
G37 -36
H35 -34
HDC BUSin(16) 1302CS 1302CT 1303CS 1303CT
HDC BUSin(17) 1302CU 1302CV 1303CU 1303CV
HDC BUSin(18) 1304A 1304B 1305A 1305B
HDC BUSin(19) 1304C 1304D 1305C 1305D
HDC BUSin(20) 1304E 1304F 1305E 1305F
HDC BUSin(21) 1304H 1304J 1305H 1305J
HDC BUSin(22) 1304K 1304L 1305K 1305L
HDC BUSin(23) 1304M 1304N 1305M 1305N
HDC GiData
1304S 1304T 1305CS 1305CT HDC GiData
61 DC405 F29
18 28
27 DB402 4
B6 -5 -,HDC GiData
45 401 M41
39 40
37 DB402 29
J28 -27 GiData(0:23)
002 44G41 READ
1304P 1304R 1305CP 1305CR HDC GiAddr
61 DC405 E15
16 17
37 DB402 30
K32 -31 HDC GiAddr(0:23)
27 28 29 30
68 402 E31
1
004 42B7 Mode Block Transport
CYS Request
43 401 K33
34 35
63 DB404 27 28
G39 -38
1304U 1304V 1305CU 1305CV
003 58-36 -,Cycle Call
004 53A3 DRC Power OK
1302CW 0 Volt 1303CW
1302CX 0 Volt 1303CX
1302CY 0 Volt 1303CY
1302CZ 0 Volt 1303CZ
1302DA Chassis 1303DA
1302DB Chassis 1303DB


1302A
1302B
1303A
1303B
HDC BUSout(0)
4
5
70
DC405
A3
HS BUS(0)
1302C
1302D
1303C
1303D
HDC BUSout(1)
6
7
70
DC405
B8
-, HS BUS(1)
1302E
1302F
1303E
1303F
HDC BUSout(2)
10
11
70
DC405
C9
-, HS BUS(2)
1302H
1302J
1303H
1303J
HDC BUSout(3)
12
13
70
DC405
D14
HS BUS(3)
1302K
1302L
1303K
1303L
HDC BUSout(4)
16
17
70
DC405
E15
HS BUS(4)
1302M
1302N
1303M
1303N
HDC BUSout(5)
18
28
70
DC405
F29
-, HS BUS(5)
1302P
1302R
1303P
1303R
HDC BUSout(6)
31
32
70
DC405
G30
-, HS BUS(6)
1302S
1302T
1303S
1303T
HDC BUSout(7)
33
34
70
DC405
H35
HS BUS(7)
1302U
1302V
1303U
1303V
HDC BUSout(8)
37
38
70
DC405
J36
HS BUS(8)
1302W
1302X
1303W
1303X
HDC BUSout(9)
39
40
70
DC405
K41
-, HS BUS(9)
1302Y
1302Z
1303Y
1303Z
HDC BUSout(10)
4
5
69
DC405
A3
-, HS BUS(10)
1302AA
1302AB
1303AA
1303AB
HDC BUSout(11)
6
7
69
DC405
B8
HS BUS(11)


1302AC
1302AD
1303AC
1303AD
HDC BUSout(12)
10
11
69
DC405
C9
HS BUS(12)
1302AE
1302AF
1303AE
1303AF
HDC BUSout(13)
12
13
69
DC405
D14
-,HS BUS(13)
1302AH
1302AJ
1303AH
1303AJ
HDC BUSout(14)
16
17
69
DC405
E15
-,HS BUS(14)
1302AK
1302AL
1303AK
1303AL
HDC BUSout(15)
18
28
69
DC405
F29
HS BUS(15)
1302AM
1302AN
1303AM
1303AN
HDC BUSout(16)
31
32
69
DC405
G30
HS BUS(16)
1302AP
1302AR
1303AP
1303AR
HDC BUSout(17)
33
34
69
DC405
H35
-, HS BUS(17)
1302AS
1302AT
1303AS
1303AT
HDC BUSout(18)
37
38
69
DC405
J36
-, HS BUS(18)
1302AU
1302AV
1303AU
1303AV
HDC BUSout(19)
39
40
69
DC405
K41
HS BUS(19)
1302AW
1302AX
1303AW
1303AX
HDC BUSout(20)
4
5
61
DC405
A3
HS BUS(20)
1302AY
1302AZ
1303AY
1303AZ
HDC BUSout(21)
6
7
61
DC405
B8
-, HS BUS(21)
1302BA
1302BB
1303BA
1303BB
HDC BUSout(22)
10
11
61
DC405
C9
-, HS BUS(22)
1302BC
1302BD
1303BC
1303BD
HDC BUSout(23)
12
13
61
DC405
D14
HS BUS(23)


62
AJ408
60H35 IO Address 1
035 60C9 IO BUS(10) 13
035 60D14 IO BUS(11) 15
035 60E15 IO BUS(12) 17
035 60F29 IO BUS(13) 19
035 59A3 IO BUS(14) 5
035 59B8 IO BUS(15) 7
035 59C9 IO BUS(16) 9
036 59D14 IO BUS(17) 12
036 59E15 IO BUS(18) 30
036 59F29 IO BUS(19) 28
036 59G30 IO BUS(20) 33
036 59H35 IO BUS(21) 31
036 59J36 IO BUS(22) 26
036 59K41 IO BUS(23) 36
C2 Address(N) & IO Address
-3
A4
-25
-14
-16
-18
-24
-6
-8
-10
-11
-29 -, IO BUS(18)
-27 -, IO BUS(19)
-32 -, IO BUS(20)
-34 -, IO BUS(21)
-37
-35
D40 Sense
B41 Control
E39 Read
F38 Write
0
63
DB405
Status(0) 11
005 42F25 Parity Error 16
005 44A1 Synchronization Error 14
005 42H33 Data Overrun 15
Status(4) 13
Status(5) 12
001 7G37 Transfer Status 17
G
F33
-32
E4
-3
D1
-2
C6
-5
B8
-7
A10
-9
IO BUS(0)
IO BUS(1)
IO BUS(2)
IO BUS(3)
IO BUS(4)
1300A
1300B
1301A
1301B
1300C
1300D
1301C
1301D
1300E
1300F
1301E
1301F
1300H
1300J
1301H
1301J
1300K
1300L
1301K
1301L
63
DB404
004 7F33 DRC Connected 29
004 53A3 DRC Power OK 30
H40
-41
IO Connected
1300BP
1300BR
1301BP
1301BR
63
DB404
002 44C11 DRC Ready 26
034 62C2 Address(N)&IO Address 31
J37
-36
IO Ready
1300BS
1300BT
1301BS
1301BT
63
DB404
DRC Interrupt 24
004 53A3 DRC Power OK 25
K35
-34
DRC Interrupt
1300BU
1300BV
1301CU
1301CV


1300M
1300N
1301M
1301N
IO BUS(5)
33
34
61
DC405
H35
IO BUS(5)
1300P
1300R
1301P
1301R
IO BUS(6)
37
38
61
DC405
J36
IO BUS(6)
1300S
1300T
1301S
1301T
IO BUS(7)
39
40
61
DC405
K41
IO BUS(7)
1300U
1300V
1301U
1301V
IO BUS(8)
4
5
60
DC405
A3
IO BUS(8)
1300W
1300X
1301W
1301X
IO BUS(9)
6
7
60
DC405
B8
IO BUS(9)
1300Y
1300Z
1301Y
1301Z
IO BUS(10)
10
11
60
DC405
C9
IO BUS(10)
1300AA
1300AB
1301AA
1301AB
IO BUS(11)
12
13
60
DC405
D14
IO BUS(11)
1300AC
1300AD
1301AC
1301AD
IO BUS(12)
16
17
60
DC405
E15
IO BUS(12)
1300AE
1300AF
1301AE
1301AF
IO BUS(13)
18
28
60
DC405
F29
IO BUS(13)
1300AH
1300AJ
1301AH
1301AJ
IO BUS(14)
4
5
59
DC405
A3
IO BUS(14)
1300AK
1300AL
1301AK
1301AL
IO BUS(15)
6
7
59
DC405
B8
IO BUS(15)
1300AM
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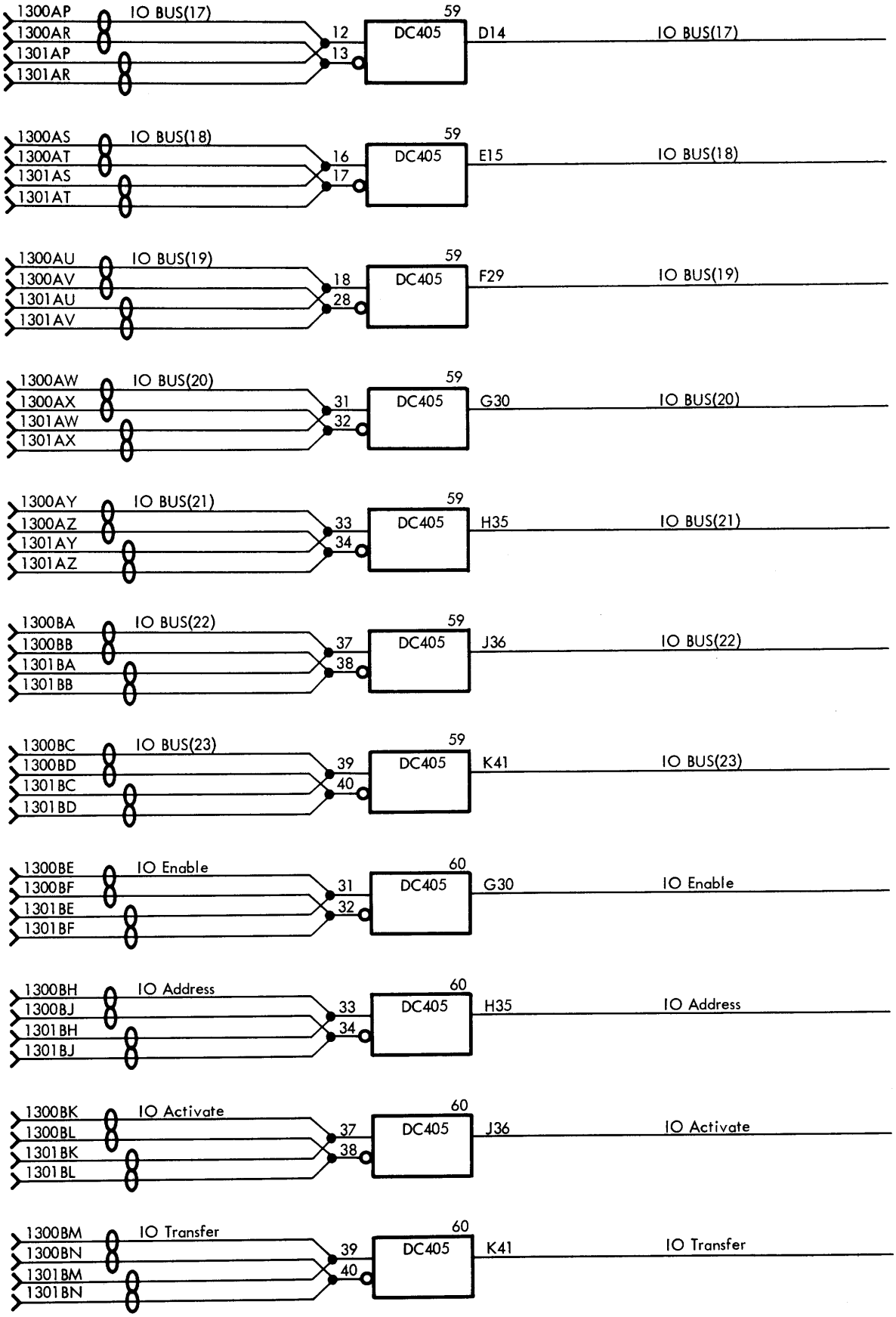
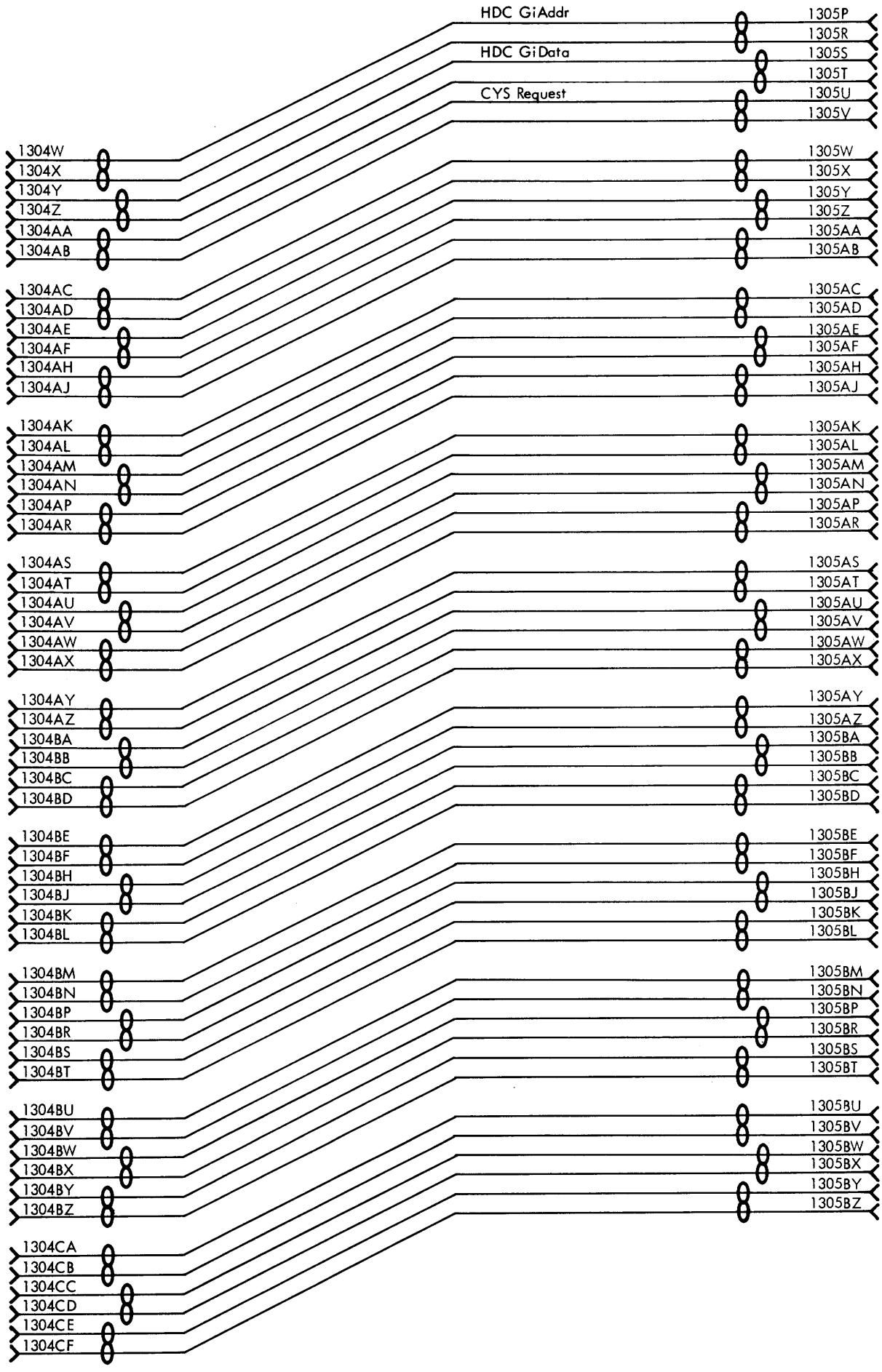
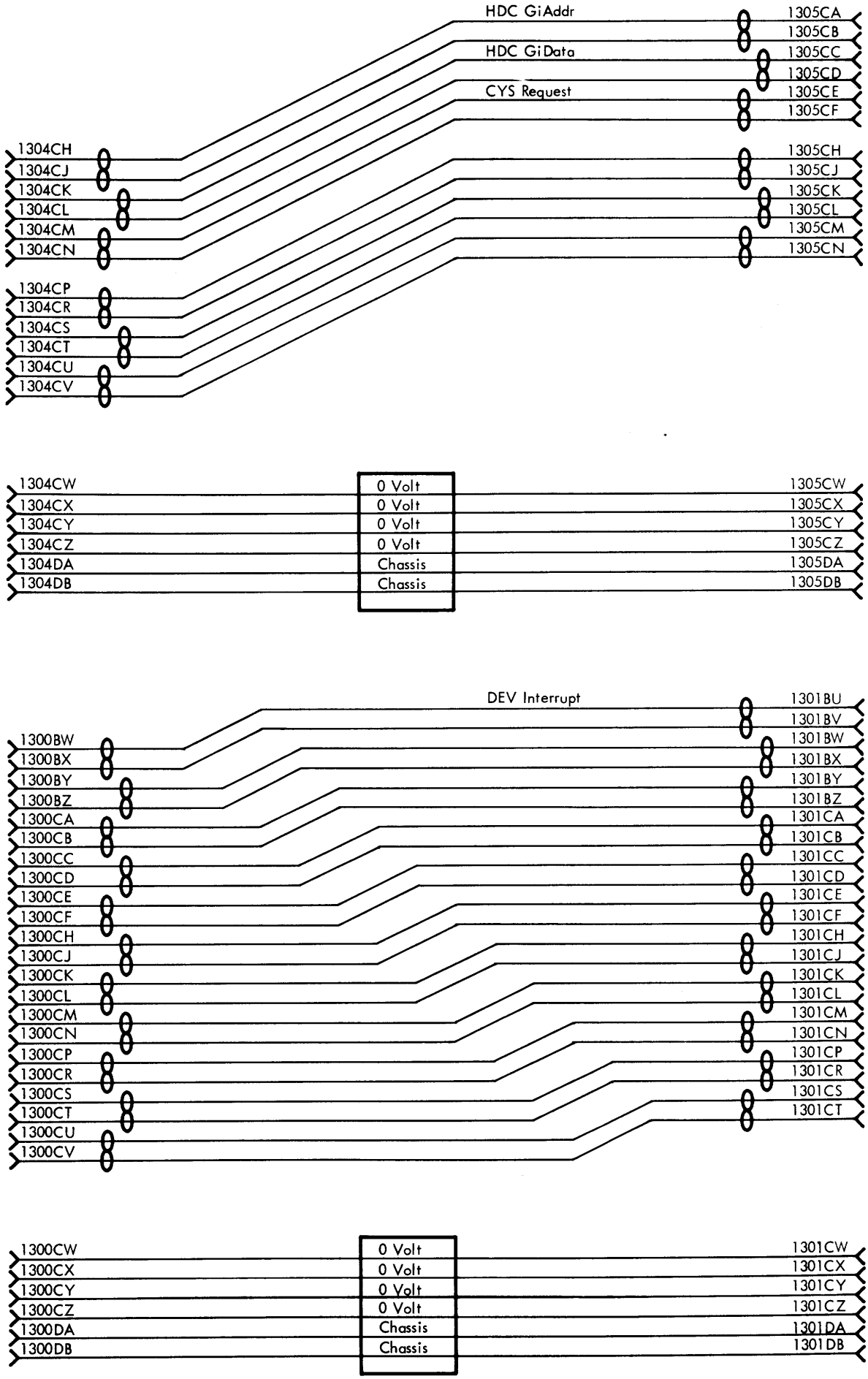
1301AM
1301AN
IO BUS(16)
10
11
59
DC405
C9
IO BUS(16)


1300AP
1300AR
1301AP
1301AR
IO BUS(17)
12
13
59
DC405
D14
IO BUS(17)
1300AS
1300AT
1301AS
1301AT
IO BUS(18)
16
17
59
DC405
E15
IO BUS(18)
1300AU
1300AV
1301AU
1301AV
IO BUS(19)
18
28
59
DC405
F29
IO BUS(19)
1300AW
1300AX
1301AW
1301AX
IO BUS(20)
31
32
59
DC405
G30
IO BUS(20)
1300AY
1300AZ
1301AY
1301AZ
IO BUS(21)
33
34
59
DC405
H35
IO BUS(21)
1300BA
1300BB
1301BA
1301BB
IO BUS(22)
37
38
59
DC405
J36
IO BUS(22)
1300BC
1300BD
1301BC
1301BD
IO BUS(23)
39
40
59
DC405
K41
IO BUS(23)
1300BE
1300BF
1301BE
1301BF
IO Enable
31
32
60
DC405
G30
IO Enable
1300BH
1300BJ
1301BH
1301BJ
IO Address
33
34
60
DC405
H35
IO Address
1300BK
1300BL
1301BK
1301BL
IO Activate
37
38
60
DC405
J36
IO Activate
1300BM
1300BN
1301BM
1301BN
IO Transfer
39
40
60
DC405
K41
IO Transfer



C4000 HDC CABLE CONNECTION DRC037

V10817 Logic Diagram



RC4000 HDC AND LDC CABLE CONNECTIONS DRC038

V10818 Logic Diagram

A/S REGNECENTRALEN

SCANDINAVIAN INFORMATION PROCESSING SYSTEMS

FALKONERALLE 1 · DK 2000 COPENHAGEN F
DENMARK – TELEPHONE: (01) 10 53 66
CABLES: REGNECENTRALEN · TELEX: 6282 RC HQ DK