

Date : September 1974

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TITLE : FIELD CHANGE ORDER No. 4032

APPLICABILITY : Disc File Controller type RC 4818 C, model DFC 403.
Field change must be executed on units with S/N below 98267.

CLASSIFICATION : Mandatory, warranty.

SCOPE : During write operations a data overrun situation may cause destruction of a word in the output area in the core store. This is due to the fact that data overrun terminates the operation resting bit 23 on the HDC at "zero". A pending cys call may now cause the fatal transport. The present modification will rest HDC 23 at "one" after termination.

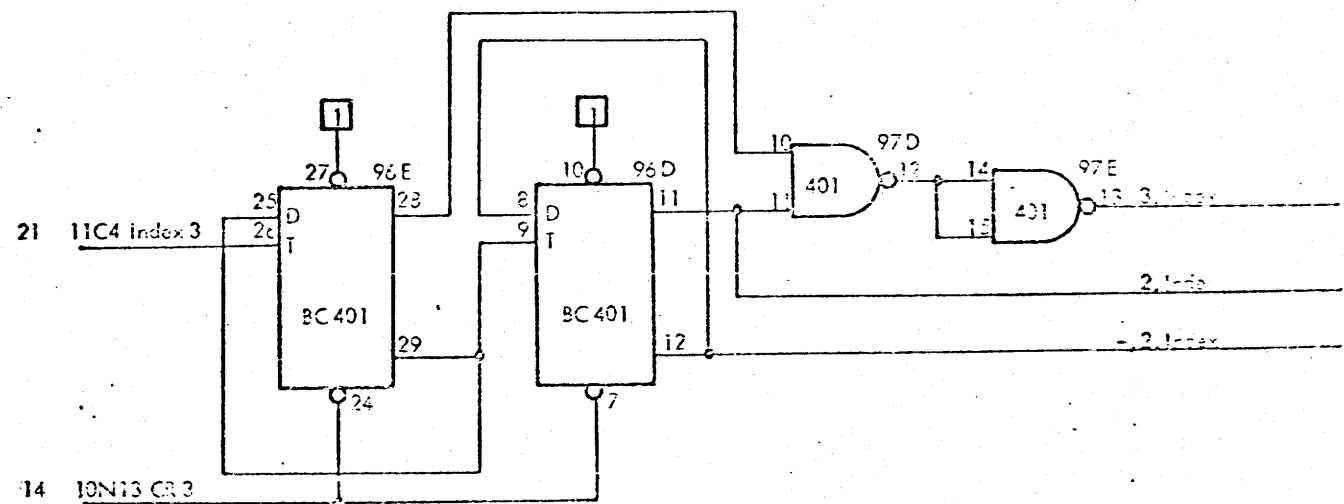
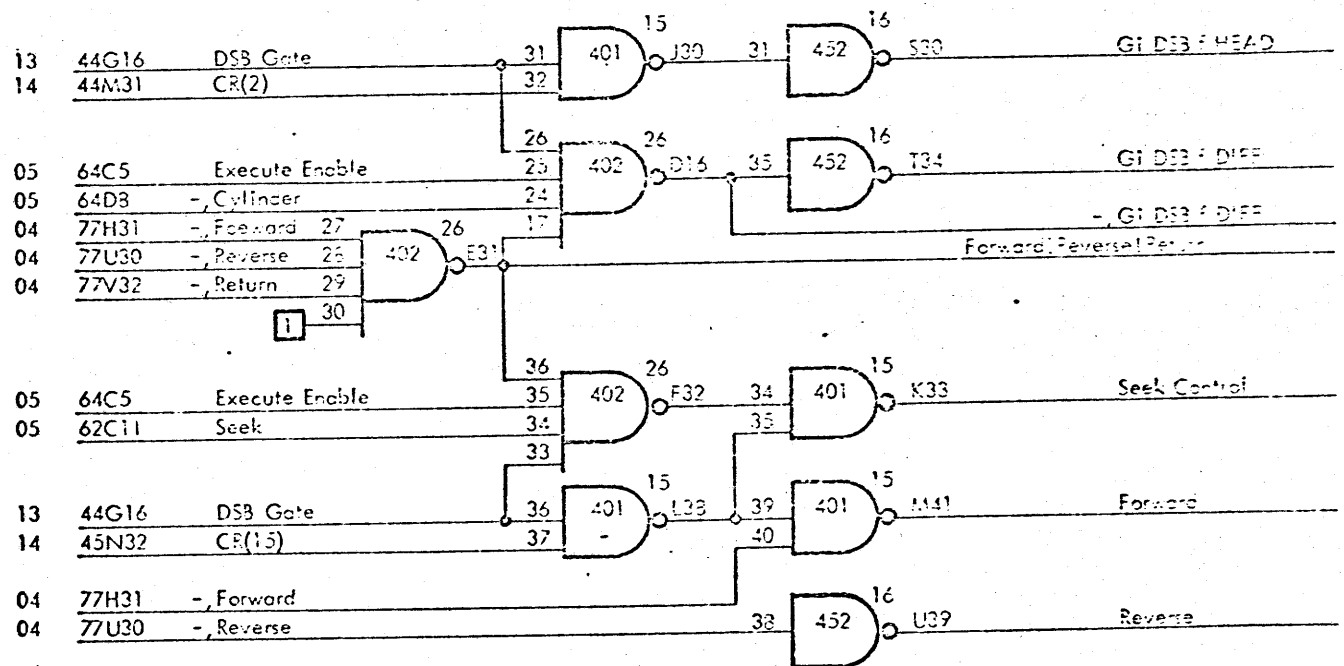
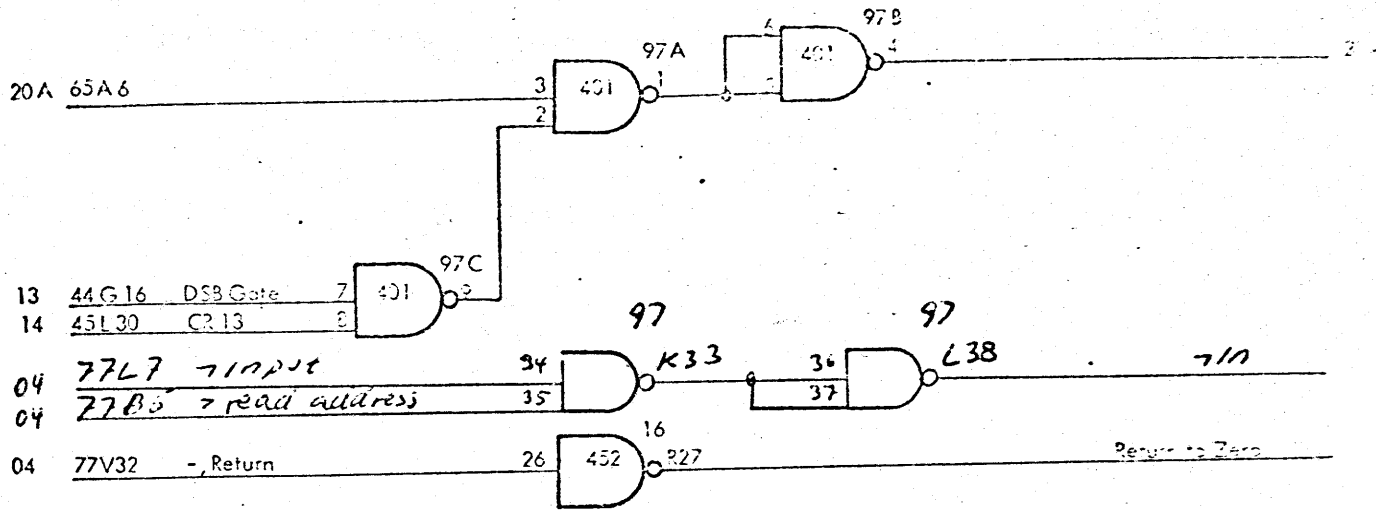
DOCUMENTATION ENCLOSED :
DFC 403 logic diagrams, revised page 20B and page 31.
List of wiring changes.

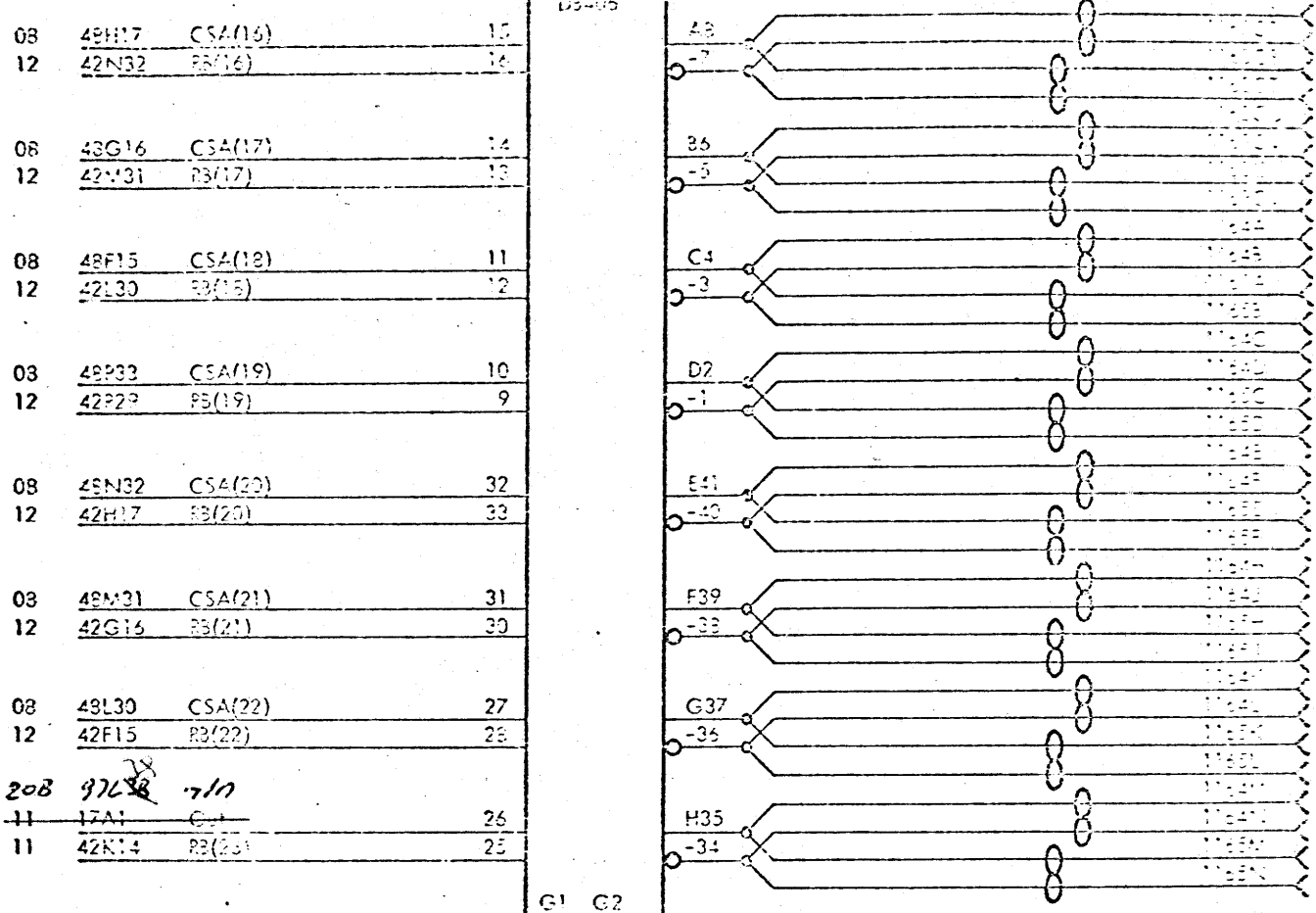
PARTS REQUIRED : 6 wrap pins,
3 m wrap wire.

FIELD INSTRUCTION : Normal testrun plus test of read and write address should be performed when the FCO has been made.

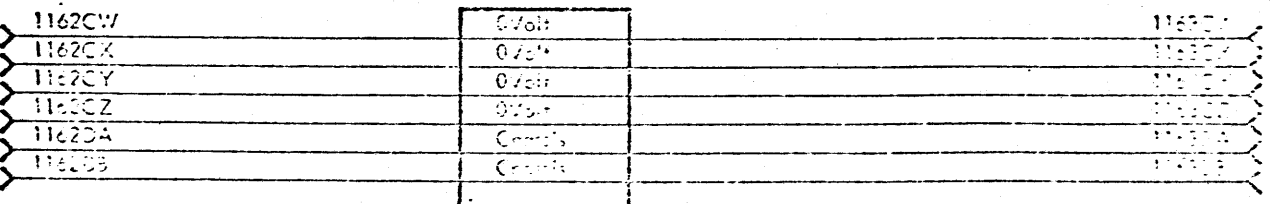
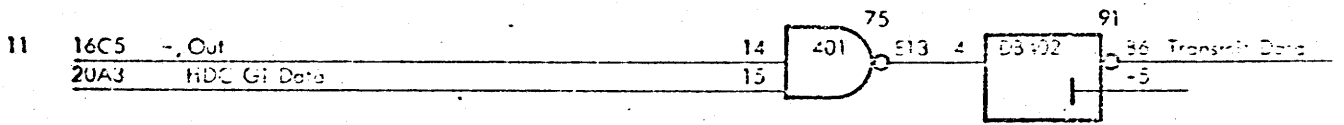
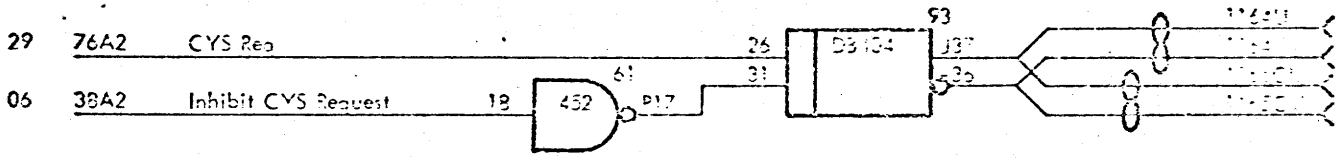
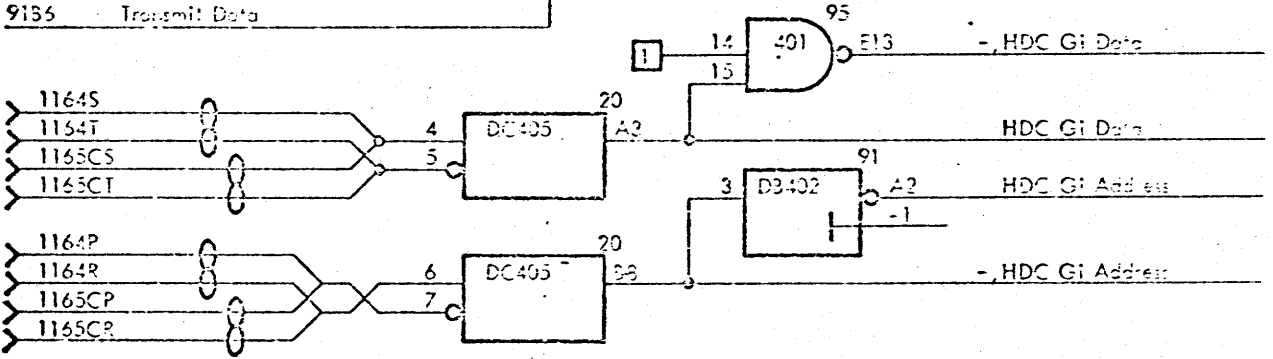
TIME REQUIRED : 1 hour.

A/S Regnecentralen
Per Hansen
Per Hansen





91A2 HDC Gi Address 74 29
 91B5 Transmit Data



RCSL: 44-RT635

Author: B. Kluge

Edited: May 1973

Technical Manual for
Disc File Controller
RC 4818C.

Keywords: RC4000, Peripheral Device/RC 4818C Disc File Controller/
Technical Manual.

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RCSL: 44 - RT 597
Authors: M. Strange and
F. Bækgaard
Edited: February 1973

RC 4818D/RC 4819D MAGNETIC DISC
and
RC 4818C DISC FILE CONTROLLER
REFERENCE MANUAL

Keywords : RC 4000, Peripheral Device, RC 4818, RC 4819 Disc Store,
Logical Structure, Reference Manual.

Abstract : This paper describes the logical structure of the RC 4818D and
RC 4819D magnetic disc and the RC 4818C disc file controller
(DFC 403) when used in connection with the RC 4000 computer.

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1. MAIN CHARACTERISTICS

The disc file controller DFC 403 is designed to control 1 to 8 disc stores of the type RC 4818D or RC 4819D.

RC 4818D and RC 4819D may be mixed at the same controller.

The RC 4818D disc has a capacity of 9.354.240 words each of 24 bits.

Physically the disc is organized as follows:

Segments :	36540 segments each of 256 words
Cylinders :	203 cylinders, i.e. possible head positions, each of 180 segments
Heads :	20 heads, each having access to one track with 9 segments

The RC 4819D disc has a capacity of 18.708.480 words each of 24 bits.

The total capacity per controller with 8 RC 4819D discs is therefore 149.667.840 words. Physically the disc is organized as follows:

Segments :	73080 segments each of 256 words
Cylinders :	406 cylinders, i.e. possible head positions, each of 180 segments
Heads :	20 heads, each having access to one track with 9 segments

A transfer of a data block to or from the disc is separated in two operations, - namely a cylinder selection followed by the actual data transfer.

The cylinder selection can be executed on several discs simultaneously. This is possible because the discs are connected to the controller via a party line system and because neither the controller nor the party line system is busy during the cylinder selection, only during the initiation.

The cylinder selection time varies from 7 to 70 milliseconds depending on the number of cylinder displacements. Nominal disc speed is 2400 revolutions per minute and nominal bit rate is 2.5 megabits per second.

The data transfer is done via the RC 4000 high-speed data channel, i.e. a data block is transferred directly to or from the internal store. The data block is composed of a variable number of consecutive segments.

The data transfer times are specified as follows:

1. Average transfer rate:
92000 words per second
2. Transfer rate within a segment:
104000 words per second
3. Average transfer time for transport inside a selected and positioned cylinder:
 $(13 + 2.8 * \text{number of segments})$ milliseconds
4. Average transfer time for transports including cylinder shifts:
 $(48 + 2.8 * \text{number of segments} + 8.3 * \text{number of cylinder shifts})$ milliseconds

The data transfer operation can only be executed on one disc at a time, and the controller will be busy in the transfer period. Therefore new cylinder selections cannot be initiated during the data transfer operation.

Two interrupt channels are associated with the disc controller; one indicates, that a data operation is completed, the other indicates, that at least one head movement is completed.

Cylinder selections and data transfers are initiated via the RC 4000 low-speed data channel by means of control commands as described in the following sections.

2. I/O COMMANDS

2.1 Control Commands

2.1.1 Control Command Modifications

The control commands are used to specify and initiate cylinder selections and data block transfers. The disc controller accepts 12 modifications of the control command:

5 transfer first	<cyl,head,sector>
9 transfer size	<number of segments>
13 input data	<first storage address>
17 output data	<first storage address>
21 input address	<first storage address>
25 output address	<first storage address>
29 select disc	<disc number>
33 return to zero	<irrelevant>
37 transfer forward	<abs (cylinder difference)>
41 transfer reverse	<abs (cylinder difference)>
45 set mode	<mode>
61 master clear	<irrelevant>

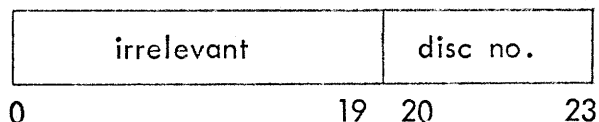
The integers denote the values of bits 18-23 in the effective address of the input/output instruction. The parameters in the brackets < and > denote the contents of the working register selected by the input/output instruction.

The parameters are interpreted as follows:

< disc number >	modulo 16
< abs (cylinder difference) >	modulo 512
< cylinder, head, sector >	modulo 512, 32, 16
< number of segments >	modulo 512
< first storage address >	modulo 262144
< mode >	modulo 16

2.1.2 Select Disc

While the disc controller is addressed by means of the device address of the input/output command, the disc itself must be selected by the control command select disc. The discs are numbered 0 to 7. In the disc select command a disc address word with the following format is transferred:



The effect of the select disc command is that all succeeding commands operate on the disc defined in the disc number word.

The disc and the controller are available immediately after the execution of the select disc command.

2.1.3 Return to Zero

The control command return to zero moves the read/write heads to cylinder 0. The command is normally used when the head position is unknown. This is the case after pack unsafe, intervention, synchronization error or data overrun. The reason for this is that the data operation is terminated as soon as the error is recognized, and that a possible cylinder shift may or may not have taken place.

The controller is busy approximately 10 μ s after the return to zero command is issued. Then the controller becomes available for operations on other units connected to the controller.

While the movement of the heads is in progress, bit 11 in the status 0 word (heads moving) is set, if the disc unit in question is selected.

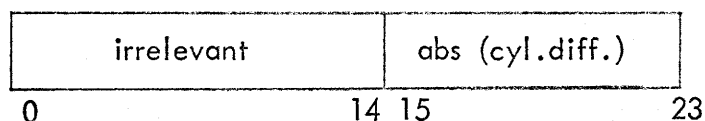
When the transfer of the heads to cylinder 0 has been completed (approx. xx to yy ms depending of initial distance from cylinder 0), the heads moving bit belonging to the disc unit in question will be cleared and a head interrupt will be generated. If an input/output address or data operation is in progress on another disc, when the head transfer is completed, the head interrupt will be delayed until the end of this operation.

Seen from the programmers point of view the data interrupt will then appear simultaneously with the head interrupt.

For this reason the head interrupt must be connected to an itr-channel with higher priority (lower number) than the itr-channel of the data transfer interrupt.

2.1.4 Transfer Forward and Transfer Reverse

These control commands initiate the cylinder selections, i.e. the positioning of read/write heads. In the transfer forward command the cylinder address is increased with abs (cylinder adifference) as specified in the transferred parameter word. The format of this is



In the transfer reverse command the cylinder address is decreased with abs (cylinder difference).

The controller is busy approximately 10 us after a transfer forward or a transfer reverse command is issued. Then the controller becomes available for operations on other units connected to the controller.

While the movement of the heads is in progress, bit 11 in the status 0 word (heads moving) is set, if the disc unit in question is selected. When the transfer of the heads has been completed (7 to 70 ms depending of the cylinder difference, average 35 ms), the heads moving status bit belonging to the disc unit in question will be cleared and a head interrupt generated. If an input/output address or data operation is in progress on another disc, when the head transfer is completed, the head interrupt will be delayed until the end of this operation.

It is possible to initiate a data transfer operation on a disc even if the cylinder selection has not been completed. In this case the controller will delay the data transfer until the heads are positioned. The head interrupt will then come at the end of the data operation and simultaneously with the interrupt from this.

The transfer forward/reverse command can be omitted if the segment address corresponds to the previous cylinder address.

A transfer first command (see 2.1.5) with the absolute value of the new cylinder address (bits 3:11) must be executed prior to the execution of the transfer forward/reverse command, because some of the bits in the absolute cylinder address are used in the disc unit for checking the head movement. The cylinder address is buffered in the selected disc drive during the head movement, so new transfer first commands may follow after the transfer forward/reverse command, with the purpose of specifying a head positioning on another disc drive or specifying a first segment address in a data transfer.

The transfer forward/reverse command must be executed before the transfer size command because the size register is used as a temporary buffer for the cylinder difference.

Positioning of heads to a non existing cylinder will be terminated with seek error and synchronization error status bits set.

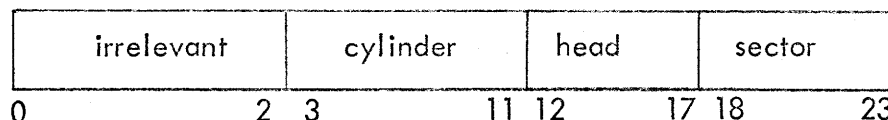
Cylinder shifts will take place automatically during a data transfer operation, if the specified data block is (or is to be) placed on more than one cylinder. This must be considered during the calculation of the next cylinder difference.

2.1.5 Transfer First and Transfer Size

A data transfer operation requires specification of a set of consecutive segments on the disc and a storage location. This specification must be presented for the disc controller in the mentioned order:

The control commands transfer first and transfer size are used to specify the set of consecutive segments. The first command transfers the address of the first segment and the second command the number of segments.

The segment address word is interpreted as follows:

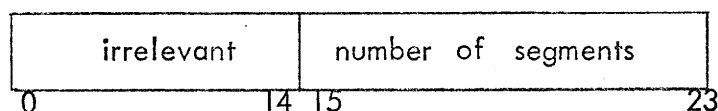


where $0 \leq \text{cylinder} \leq 405$, $0 \leq \text{head} \leq 19$, and $0 \leq \text{sector} \leq 8$.

The relation between a segment number and the segment address constituents is:

$$\text{segment number} = 180 * \text{cylinder} + 9 * \text{head} + \text{sector}$$

In the transfer size command the parameter word has the following format:

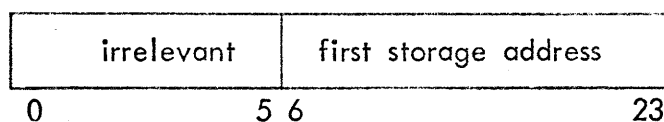


The contents of the size register is destroyed by the transfer forward/reverse commands.

The disc controller is available immediately after the execution of the transfer first and transfer size commands.

2.1.6 Input Data and Output Data

These control commands define a storage location and initiate a block transfer. The storage location is given by the first storage address word, transferred and interpreted as follows:



The data block will be transferred with the first word in the storage location specified by first storage address. The rightmost bit of this parameter (bit 23) is ignored. Thus it is irrelevant whether the parameter refers to the left or right half of the storage word.

The input data command initiates a transfer from disc to internal store. The output data command initiates a transfer from internal store to disc. After initiation of a data transfer, the disc controller is busy until the data operation is either completed successfully or terminated by an error condition. The disc delivers a data interrupt signal when it after a data transfer becomes available.

2.1.7 Input Address and Output Address

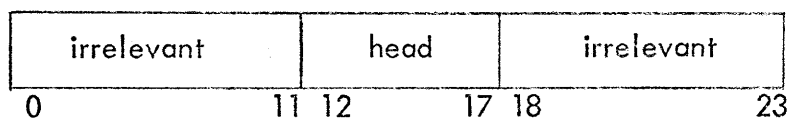
The disc surface is physically divided into sectors separated from each other by sector gaps. Each sector contains preamble bits (zeros), address marker word, address word, parity word for address (longitudinal odd parity), gap, preamble bits (zeros), marker bit (one), 256 data words, parity words for data (longitudinal odd parity), and tolerance gap. The address marker word is used to detect a sector start.

The segment address word identifies the segment. A new disc pack must be supplied with address marker words and segment addresses before use.

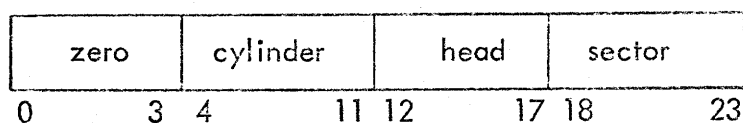
The segment addresses may afterwards be input for checking. The input and output of segment addresses follow a similar scheme as given for input data and output data.

In details, writing of segment addresses is done in 3 steps:

- 1) Positioning of heads to actual cylinder by means of the commands transfer first, return to zero, transfer forward, and transfer reverse.
- 2) Head selection by means of the transfer first command. The parameter word is interpreted as follows:



- 3) Writing of segment address words on the now selected track by means of output address. This command initiates writing of 9 segment address words in the sectors 0 to 8. The first storage address in the command refers to a buffer area of 9 words, the contents of which must be 9 consecutive segment address words. The format of each word should be:



The address marker words and parity words are generated automatically by the disc controller during the executing of the segment address writing.

The disc controller is busy during writing of segment addresses, and when it afterwards becomes available an interrupt signal is generated.

Use of the command transfer size is irrelevant (will be ignored) because the controller always writes 9 segment addresses per operation.

The sequence of the segment addresses should be shifted 3 per cylinder to enable cylinder shifts in 1/3 revolution (8.3 msec.).

All segment addresses must be written before checking is relevant. The checking is carried out in 3 steps:

- 1) Equivalent to step 1 of segment address writing.
- 2) Equivalent to step 2 of segment address writing.
- 3) Reading of segment addresses by means of input address.

This command initiates reading of 9 segment address words in the sectors 0 to 8. First storage address of the command refers to a buffer area to which the 9 segment address words are transferred.

The format of the segment address word for the commands input and output address are identical.

The disc controller is busy during reading of segment addresses, and when it afterwards becomes available an interrupt signal is generated.

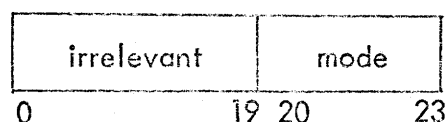
When the address markers have been written it is a good practice to initiate the data area by overwriting all segments with zeros. This will avoid status errors in case of superfluous reading later.

Notice, that this initiation always should be done. This means that if the address markers on an old diskette need a "shine up" the relevant data areas must be dumped at first.

2.1.8 Set Mode

This command is for diagnostic purposes only.

In the set mode command the parameter word has the following format:



The 4 bits in the mode register is thus under control of the set mode command. Each bit in the mode register has certain effects on the status generation when set, and may be used for checking the status generation. The meaning and effect of the mode register bits is as follows:

mode (20): Inhibit index. When set, the index pulse from the disc drive is removed. This causes input address or output address operations executed with mode (20) set, to be terminated with the timer status bit set. CR(3) in the sense 32 status word (see section 2.2.3) should be set.

The inhibit index will not have any effect on other operations.

mode (21): Inhibit CYS Requests. When set, cycle stealing requests to the RC 4000 core store are inhibited. This causes data or address transfer operations to be terminated with data overrun status bit set.

mode (22): Modify preamble. When set during an output address operation the address marker words will be slightly modified.

When the segments in question later are operated on with either input address, input data or output data, the operation will be terminated with status bits sync error and wrong 2nd index set.

mode (23): Inhibit parity. When set during write address operations, the address parity word will be written as zero.

When the segments in question later are operated on with input address, input data or output data the parity error status will be set. For input data and output data further more sync error and wrong 2nd index will be set. If mode (23) is set during write data operations, the data parity word will be written as zero.

When the segments in question later are operated on with read data operations, the parity error status bit will be set provided that the longitudinal parity of the written data is different from all ones (-1).

2.1.9 Master Clear

The control command master clear brings all important bistables in the disc file controller in a well defined initial state. The master clear signal may also be generated by the master clear switch at the controller or during a power up sequence.

The master clear command has no effect on the bistables in the disc drive (e.g. pack unsafe, pack change). The command has effect even when the controller is busy. The parameter word associated with the command is irrelevant.

2.2 Sense Commands

2.2.1 Sense Command Modifications

The sense commands are used to inform the programs about the state of the controller and the result of previous operations. The disc controller accepts 2 modifications of the sense command:

0 sense status 0	<status 0>
32 sense status 32	<status 32>

The leftmost integers denote the values of bits 18-23 in the effective address of the input/output instruction.

Bits 0-11 in status 0 word can be considered as the main status, which is required for normal operation in the RC 4000 system. Bits 12-23 in status 0 word and bits 0-23 in status 32 word are status bits, which are generated for technical diagnostic purposes only.

The status bits can be divided in two groups:

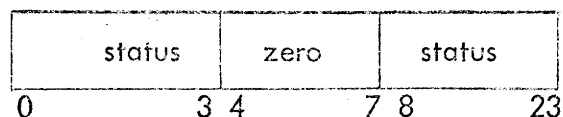
Type 1: Bits, which logically belong to the controller, and which are common to all disc units. They specify the result of the latest performed data or address operation and are independent of the contents of the unit register. They will normally be cleared by the next input/output data or input/output address operation.

Type 2: Bits, which logically belong to each disc unit, and which are selected by means of select disc command. They thus indicate the state of the currently selected disc unit. These bits are only affected by actions applied to a specific disc unit (manual or program).

The sense 0 command can only be executed when the controller is ready and connected, whereas the sense 32 command only requires the controller to be connected, because the controller always signals ready to the CPU, when this specific command is issued. The status 32 information is thus available even when the controller is busy.

2.2.2 Sense 0

When the disc controller is available, (i.e. ready and connected), a status 0 word can be transferred to a working register by means of a sense 0 command. The format of the status word is:



The status bits have the following meaning:

<u>Bit No.</u>	<u>Meaning</u>	<u>Type</u>
0	intervention	2
1	parity	1
2	timer	1
3	data overrun	1
8	disc in local	2
9	pack unsafe	2
10	synchronization error	1,2
11	heads moving	2
12:15	command register	1
16:23	unit selected	2

The synchronization error status bit represents error status bits both of type 1 and type 2.

2.2.2.1 Intervention

Intervention indicates that the selected disc is in local mode or has been in local mode since the most recent data transfer operation.

The intervention bit is set when the disc goes from remote to local state. The bit is reset by the first input/output data or input address command to the selected disc, but only if the disc is returned to remote state.

Setting of intervention implies a termination of a possible current operation on the disc.

The intervention bit will also be set when no disc is connected to the controller corresponding to the unit number selected.

2.2.2.2 Parity Error

This status bit indicates a parity error in one or more segments transferred in the most recent data input operation.

The parity error status is set when recognized by the controller. Recognition of the error will not terminate the operation. The status bit is reset by the first input/output data or input/output address command.

or data (see diagram) / H)

2.2.2.3 Timer

This status bit indicates, that the controller has been busy for longer than 3 seconds and has failed to complete the required operation.

Only operations, during which the controller is busy is supervised in this way.

Head movements are thus not supervised by the controller, but each disc has a local timer to supervise the head movements. Time out in this case indicated by seek error and synchronization error status bits.

Time is cleared by in/output data/address (see diagram) (FC28) / H)

2.2.2.4 Data Overrun

Data overrun indicates overloading of the high-speed data channel. Further data transfers are suppressed and the operation terminates. The status bit is reset by the first input/output address command.

2.2.2.5 Disc in Local

Disc in local indicates that the selected disc cannot be controlled by the disc controller due to one or more of the following situations:

- cable between controller and disc is removed.
- power to the disc electronics is switched off.
- disc motor not at the proper speed.
- disc number plug has been removed.
- operator has interfered by means of the maintenance panel switches.

The transition to local sets the status bit and terminates a possible current operation. When the disc returns to the remote state, the status bit disc in local is reset.

Operations initiated in local state are not buffered but terminated immediately.

2.2.2.6 Pack Unsafe

Pack unsafe may be set due to several hardware malfunctions or irregular control of the selected disc.

The setting of this status bit terminates any operation in progress immediately.

When it is set, the FAULT indicator on the disc unit in question is illuminated and any operations on this unit will be terminated immediately. The status bit can only be cleared by manually depressing the FAULT switch. (see section 5).

2.2.2.7 Synchronization Error

This status bit indicates one or more of the following errors:

- Wrong 2nd index (type 1),
- Address error (type 1),
- Drop out (type 1),
- Seek error on selected disc (type 2).

These error bits are described in detail in later sections.

All the above mentioned errors terminates the current operation immediately. The status bit is reset by the first input/output data or input/output address command if it is set due to one or more of the three first mentioned errors.

If the bit is one due to the last mentioned reason, the bit will be cleared by the first return to zero command to the selected disc or by selecting another disc number.

2.2.2.8 Heads Moving

Heads moving indicates that a head positioning on the selected disc takes place. The status bit is set by a transfer forward/reverse or return to zero command, and is reset when the head positioning has been completed.

2.2.2.9 Command Register

Status bits 12:15 contains the 4 modifier bits of the latest control command issued to the disc controller (i.e. bits 18:21 in the address part of the input/output instruction).

2.2.2.10 Unit Selected

These 8 status bits indicates the select status of the 8 possible discs, which can be connected to the controller, one bit for each disc. A one in a bit position indicates, that the disc connected to the B cable position associated with the bit position is selected. This means, that the disc in question has a logic number plug corresponding to the current contents of the unit register.

Not more than one bit in the unit selected register should be set at a time, i.e. not more than one disc should have a given unit number.

Note that there is no certain relation between bit positions in the unit selected register and unit number, because logic number plugs may be installed and interchanged independent of the physical installation of the cables.

2.2.3 Sense 32.

When the disc controller is connected, a status 32 word can be transferred to a working register by means of a sense 32 command. Note, that the transfer is independent of the ready/busy state. The controller simulates ready with regard to this command even when it is busy. The status bits have the following meaning:

<u>Bit No.</u>	<u>Meaning</u>	<u>Type</u>
0:14	CR(0:14), control register	1
15	Wrong 2nd index	1
16	Address error	1
17	Drop out	1
18	Seek error	2
19	Pack unsafe	2
20:23	Unit register	2

2.2.3.1 Control Register

The control register is a 16 bit register, which specifies the state of the controller when performing a data or address operation.

One and only one of the 16 bits should be set at a time. The position of the bit set in the register specifies the state. A short description of the operation performed in each state follows:

- CR(0): Ready state. No data operation in progress.
- CR(1): Waiting for head movements to be completed. If already completed, only 0.4 μ s in this state.
- CR(2): Transfer head address to head register in selected disc drive. Duration 3.2 μ s.

- CR(3): Input/output address operations: Wait for index pulse. Duration up to 25 ms.
- Input/output data operations: Decrement "number of segments" (size) counter. Duration 0.4 μ s.
- CR(4): Reset readdetector. Set word counter. Duration 0.4 μ s.
- CR(5): Output address operation: Dummy. Duration 0.4 μ s.
- Other operations: Unlock readdetector. Search for 8 consecutive zeroes to be sure, that the readdetector is synchronized to a zero pattern. Duration: min. 0.4 μ s, max. depending on track information.
- The state may be entered several times during the search for a proper segment address record.
- CR(6): Output address: Write a segment address record. Duration 285 words * 9.6 μ s = 2.73 ms.
- Input address: Lock readdetector to recorded pattern. Synchronize word frame on first coming 1. Check address marker word, transfer address word to core, and check parity word. In case of mismatch in address marker word go to CR(4).
- Input/output data: Lock readdetector to recorded pattern. Synchronize word frame on first coming 1. Check address marker word, check address word and check parity word. In case of any mismatch go to CR(4).
- CR(7): Output/input address: Decrement "segment counter". (Special 9 to 0 counter for address operations).
- Output/input data: Set wordcounter for 3 words delay. Duration 0.4 μ s.
- Last state in input address operations.

- CR(8): Output address operation: Check the correct timing of the 2nd index pulse following the end of the 9th segment address record. Duration: $77 \text{ words} * 9.6 \mu\text{s} = 739.2 \mu\text{s}$. The nominal position of the 2nd index pulse is in the middle of this period.
- Last state for output address operations.
- Input/output data operations: 2 word delay, duration $28.8 \mu\text{s}$. Reset readdetector.
- CR(9): Output data: Set wordcounter. Duration $0.4 \mu\text{s}$.
- Input data: Unlock readdetector and search for 8 consecutive zeros. Duration approximate $4 \mu\text{s}$.
- CR(10): Output data: Write data record. Duration: $261 \text{ words} * 9.6 \mu\text{s} = 2.51 \text{ ms}$.
- Input data: Lock readdetector. Synchronize word frame on the 1, which is recorded before the first data bit. Read and transfer the data record. Check parity. Duration $257 \text{ words} * 9.6 \mu\text{s} = 2.47 \text{ ms}$. + a short synchronize time.
- CR(11): If number of segments counter equals zero go to CR(0). Otherwise go to CR(12). Duration $0.4 \mu\text{s}$.
- CR(12): Increment the concatenated cylinder, head, and sector counters. In case of a count up in cylinder counter go to CR(13), else go to CR(2). Duration $0.4 \mu\text{s}$.
- CR(13): Transfer cylinder difference = 1 to selected disc drive. Duration $3.2 \mu\text{s}$.
- CR(14): Transfer absolute cylinder address to selected disc drive. Duration $3.2 \mu\text{s}$.
- CR(15): Transfer a forward move command to selected disc drive. Duration $3.2 \mu\text{s}$. Go to CR(2).

Only the first 15 bits of the control register (CR(0:14)) can be sensed by the sense 32 command.

To avoid false sense results due to changes in the control register during sense operation, the contents of the control register is transferred through a buffer, which contents is continuously updated with the 2.5 Mhz clock of the control register, except in the following two cases, where transfer is inhibited:

- 1) During the execution of the sense 32 command.
- 2) While the timer status bit is set (see 2.2.2.3).

The buffer will in this case store the contents of the control register at the time, where the timer run out.

2.2.3.2 Wrong 2nd Index

The meaning of this status bit depends of the type of operation.

Output address: The status bit is set, if the position of the 2nd index pulse was either too early or too late during the writing of a track. The required speed tolerance of the disc pack during the output address operation is tighter than normal, namely $\pm 1.5\%$. If there are no severe hardware error, this status bit indicates, that the speed tolerance was exceeded.

Input address: The status bit is set, if a 2nd index occurs before 9 segment address records are found after 1st index.

Input/output data: The status bit is set, if 2 index pulses occur before the segment address record matching the specified first segment address is found.

The status bit is cleared by the first coming input/output address or data operation.

The setting of this status bit implies, that the synchronization error also will be set. (See 2.2.2.7).

The wrong 2nd index status bit terminates the operation immediately.

2.2.3.3 Address Error

Can only be set during input or output data operations and when more than 1 segment is transferred from one cylinder.

The status bit is set, if the address word belonging to the first found address marker word following a just transferred segment on the same cylinder is not matching.

The status bit is cleared by the first coming input/output address or data operation.

The setting of this status bit implies, that the status bit sync error also will be set. (See 2.2.2.7).

The address error status bit terminates the operation immediately.

2.2.3.4 Drop Out

This status bit can be set during input address and input/output data operations.

It is set, if the readdetector, when supposed to be synchronized, detects that an expected flux change is missing.

The status bit is cleared by the first coming input/output address or data operation.

The setting of this status bit implies, that the status bit synchronization error also will be set. (See 2.2.2.7).

The drop out status bit terminates the operation immediately.

2.2.3.5 Seek Error

This status bit indicates when set, that the selected disc unit was unable to complete a head positioning initiated by a transfer forward/reverse command due to one of the following reasons:

1. The heads have gone beyond the outer limits of the recording area.
2. The selected disc unit was unable to complete the desired move in a predetermined time.

A return to zero command sent to the unit, that indicates a seek error, will clear the seek error status bit and return the heads to cylinder zero. A seek error status bit implies, that the heads moving status bit of the unit is cleared and synchronization error is set.

2.2.3.6 Pack Unsafe

Pack unsafe may be set due to several hardware malfunctions or irregular control of the selected disc.

The setting of this status bit terminates any operation in progress immediately.

When it is set, the FAULT indicator on the disc unit in question is illuminated, and any operations on this unit will be terminated immediately. The status bit can only be cleared by manually depressing the FAULT switch. (See section 5).

2.2.3.7 Unit Register

The unit register is a 4 bit register, which specifies the currently selected disc unit, i.e. the value modulo 16 of the parameter word in the latest executed select disc command. The unit register is cleared by the master clear command.

3. INTERRUPT

Two interrupt channels are associated with the disc controller, a data interrupt channel and a head interrupt channel.

3.1 Data Interrupt

When an input address, output address, input data, or output data control command is issued, the disc controller is busy until the operation is either completed successfully or terminated by an error condition. When it then becomes available, a data interrupt is delivered.

3.2 Head Interrupt

A head movement may be initiated by means of a return to zero, transfer forward or transfer reverse control command. The controller is busy in approx. 10 μ s after any of these 3 commands. However, no interrupt is generated when it becomes available again. When the controller is available, a head movement may be initiated on any disc unit, which not already has a head movement in progress.

In this way several head movements may take place simultaneously. When any head movement is completed a head interrupt is generated.

If two or more disc units completes their head movements simultaneously, only a single interrupt is generated.

If a head interrupt is generated before a previous interrupt has been serviced, only a single interrupt will be received. Head interrupts are not generated while the controller is busy; they are delayed until the controller becomes available. If two or more head movements are completed or terminated while the controller is busy, only a single head interrupt is generated, when the controller becomes available again.

In any case the unit or the units, which have caused the head interrupt, may be identified by selecting the disc units, from which head interrupts may be expected, one after another, and examining the heads moving status bit.

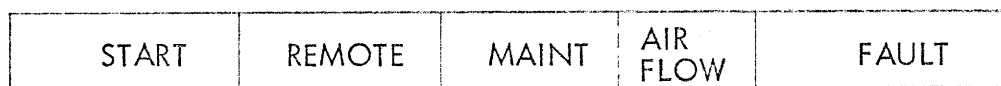
4. INDICATOR ON THE RC 4000 OPERATOR PANEL

Even if a disc controller can have up to 8 discs connected, there is just one indicator on the RC 4000 operator panel. This indicator is lit (green), when the disc controller itself is connected to RC 4000.

The status of the single disc must be observed by looking at the disc indicator panel or at the console messages.

5. DISC CONTROL SWITCHES AND INDICATORS

The disc is equipped with an operator control panel, which has the following switches and indicators:



Disc No.
plug

START is a combined switch and indicator. When the switch is depressed once, it will energize the spindle drive motor and begin the first seek sequence, provided the following conditions are satisfied:

- 1) The disc pack is in place
- 2) All covers are closed
- 3) Power and circuit breakers are on and maintenance control switches are in the right positions.

Depressing the START switch once more the spindle drive motor will be stopped again.

The START indicator illuminates when the START switch is in the on condition, even if a condition exists, which prevents the spindle drive motor to start.

REMOTE is an indicator illuminated when the disc can be controlled by the computer, i.e. when the local bit in the status word is zero.

MAINT is an indicator illuminated when the disc is in maintenance mode caused by use of different switches on the maintenance control panel.

AIR FLOW The AIR FLOW lamp, when illuminated, indicates proper air flow rate.

FAULT This is a combined switch and indicator. FAULT is illuminated in consequence of different hardware malfunctions or irregular control of the disc.

The FAULT switch, when depressed, clears the FAULT memory element and extinguishes the indicator if no errors are present.

Disc No.
plug:

This is an interchangeable plug with indicator.
The plug defines the disc address on the party line system.
The plug is equipped with a digit indicating the disc address
(0 to 7). The plug indicator is illuminated when the disc in
question has been selected by the select disc command.

6. LOAD METER

A load meter may be connected to the disc controller. This contains three 0 to 100% meters labelled HEAD ACCESS, ROTATIONAL ACCESS AND DATA TRANSFER.

6.1 Head Access

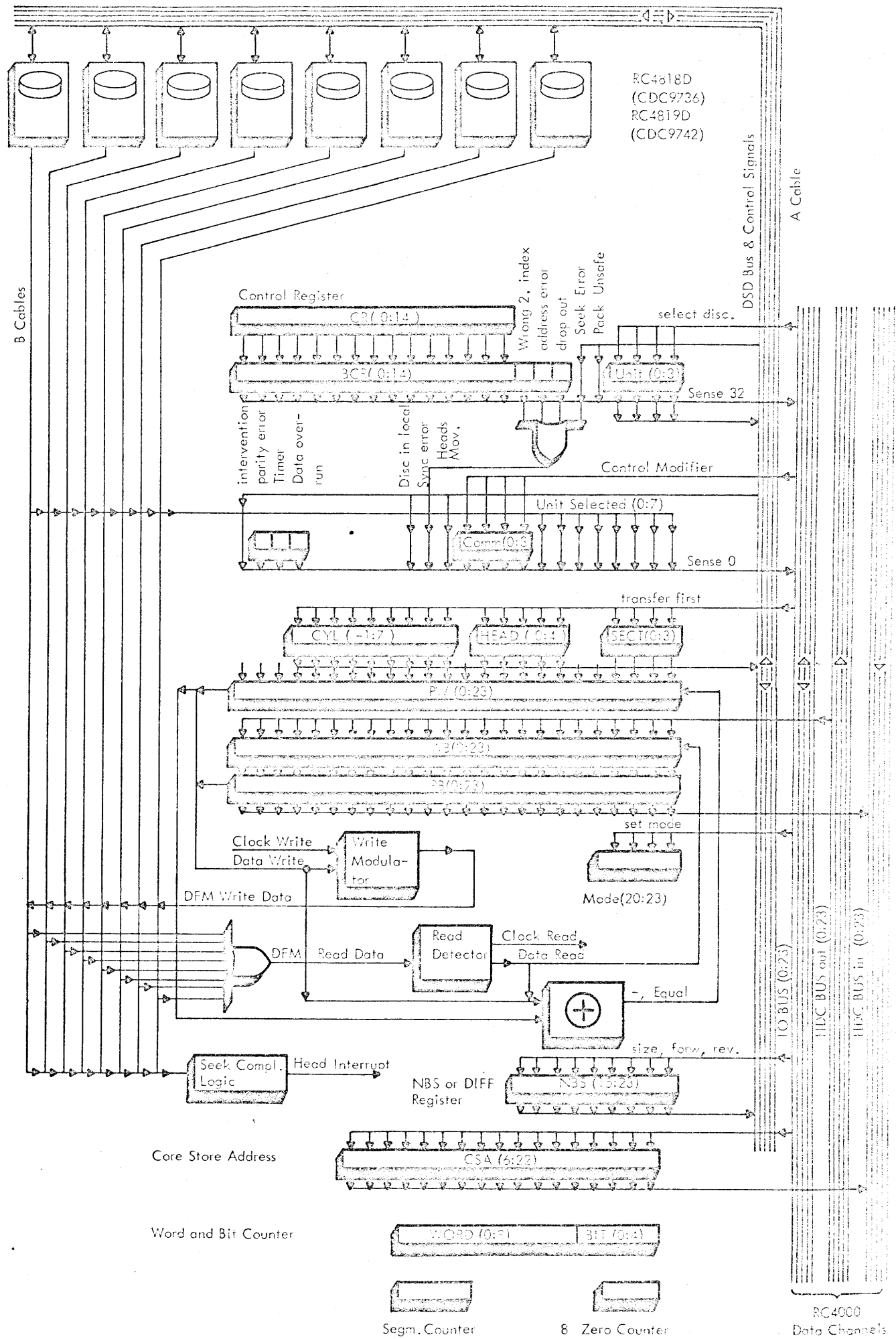
This meter indicates the relative amount of time in per cent, during which a selected disc has its heads moving.

6.2 Rotational Access

This meter indicates the relative amount of time in per cent, during which the controller is busy, has completed the head movement on the selected disc, and is waiting for the start of a segment.

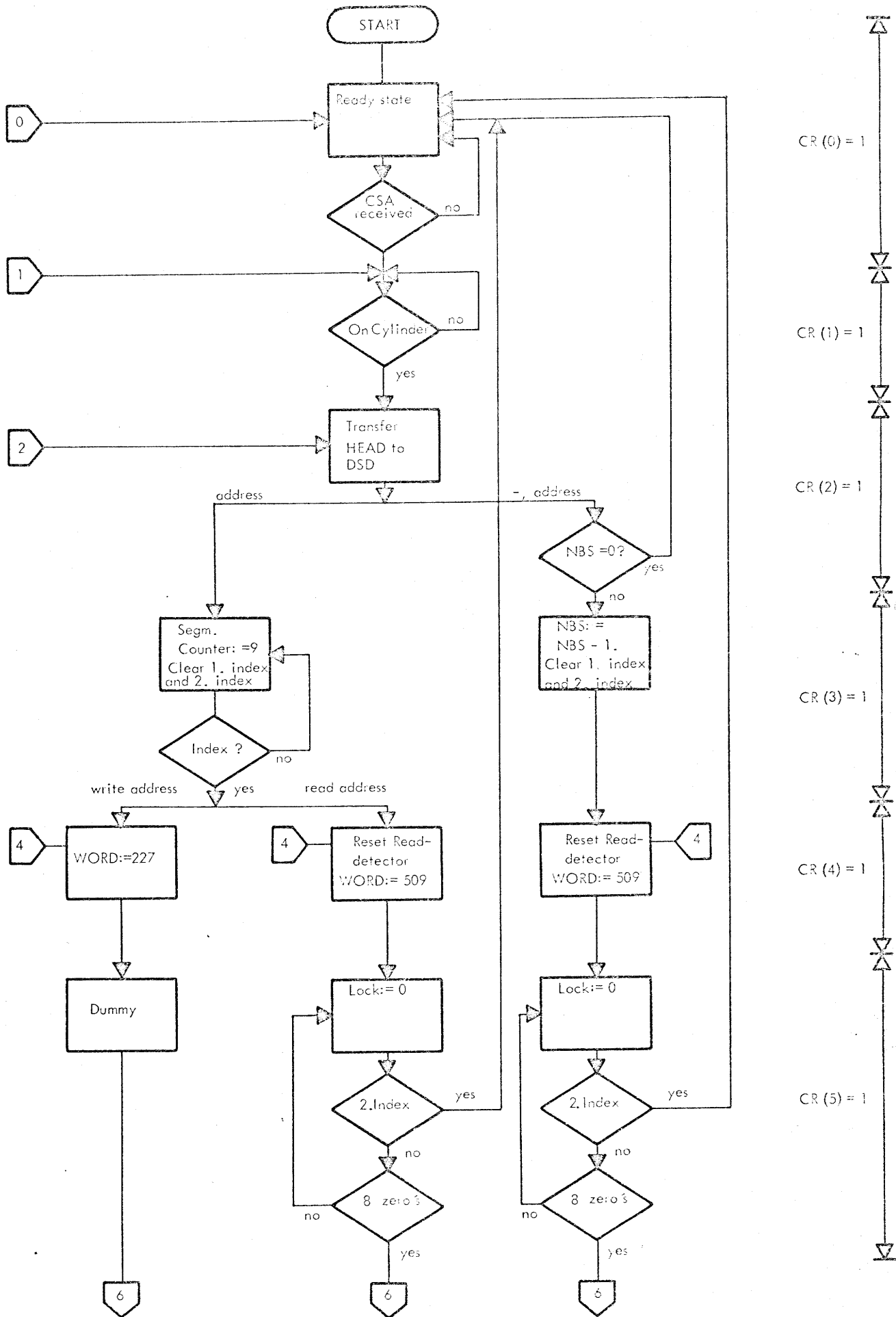
6.3 Data Transfer

This meter indicates the relative amount of time in per cent, during which the controller is transferring data with the full rate of 104 kword per second.



DISC FILE CONTROLLER DFC403
Register Structure

DFC403



CR (0) = 1

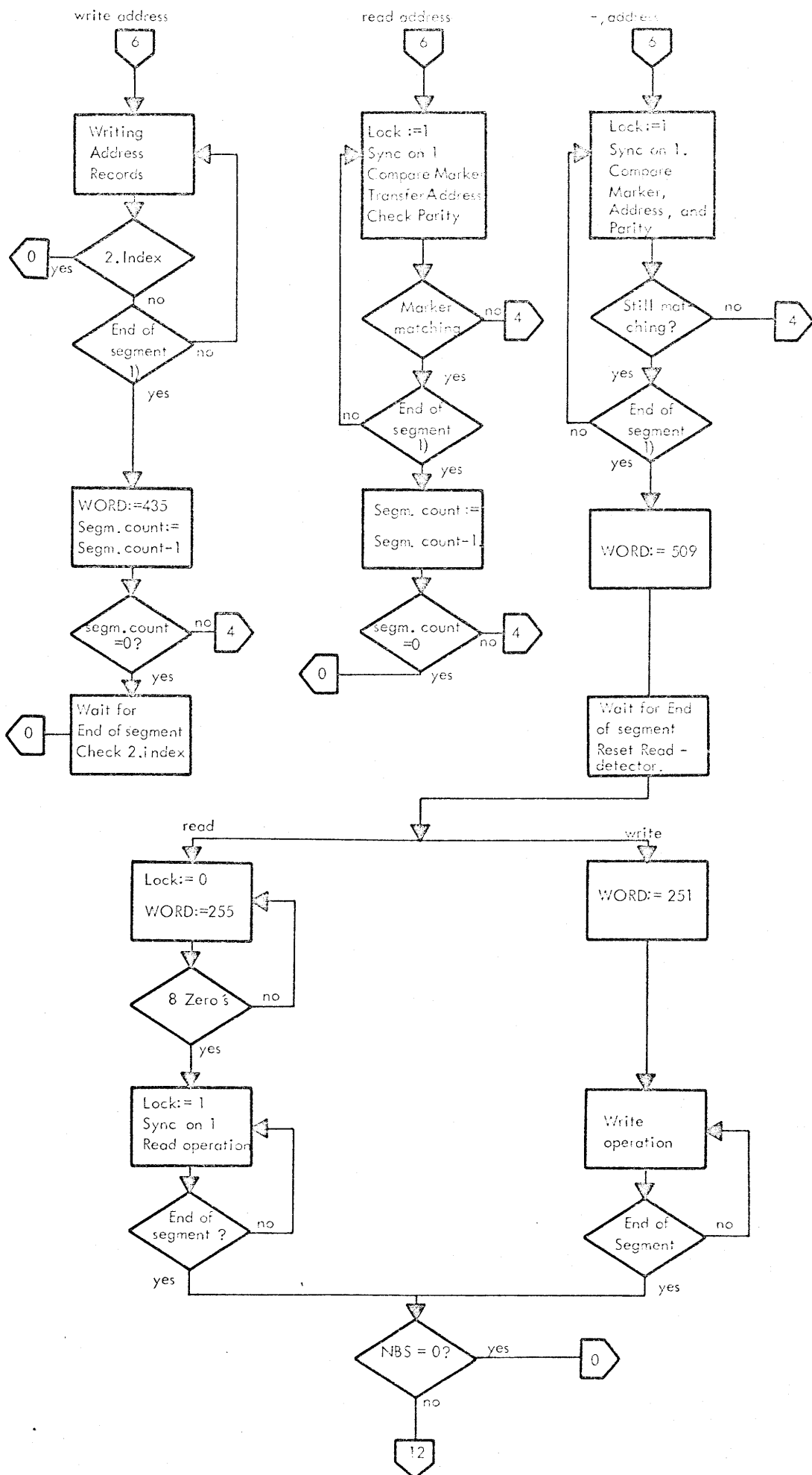
CR (1) = 1

CR (2) = 1

CR (3) = 1

CR (4) = 1

CR (5) = 1



CR (6) = 1

CR (7) = 1

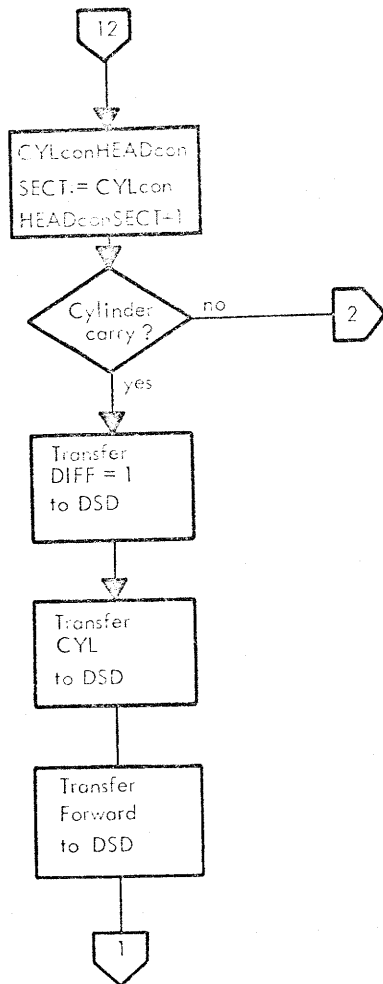
CR (8) = 1

CR (9) = 1

CR (10) = 1

CR (11) = 1

1) End of segment = WORD = 511 & BIT = 23



CR (12) = 1

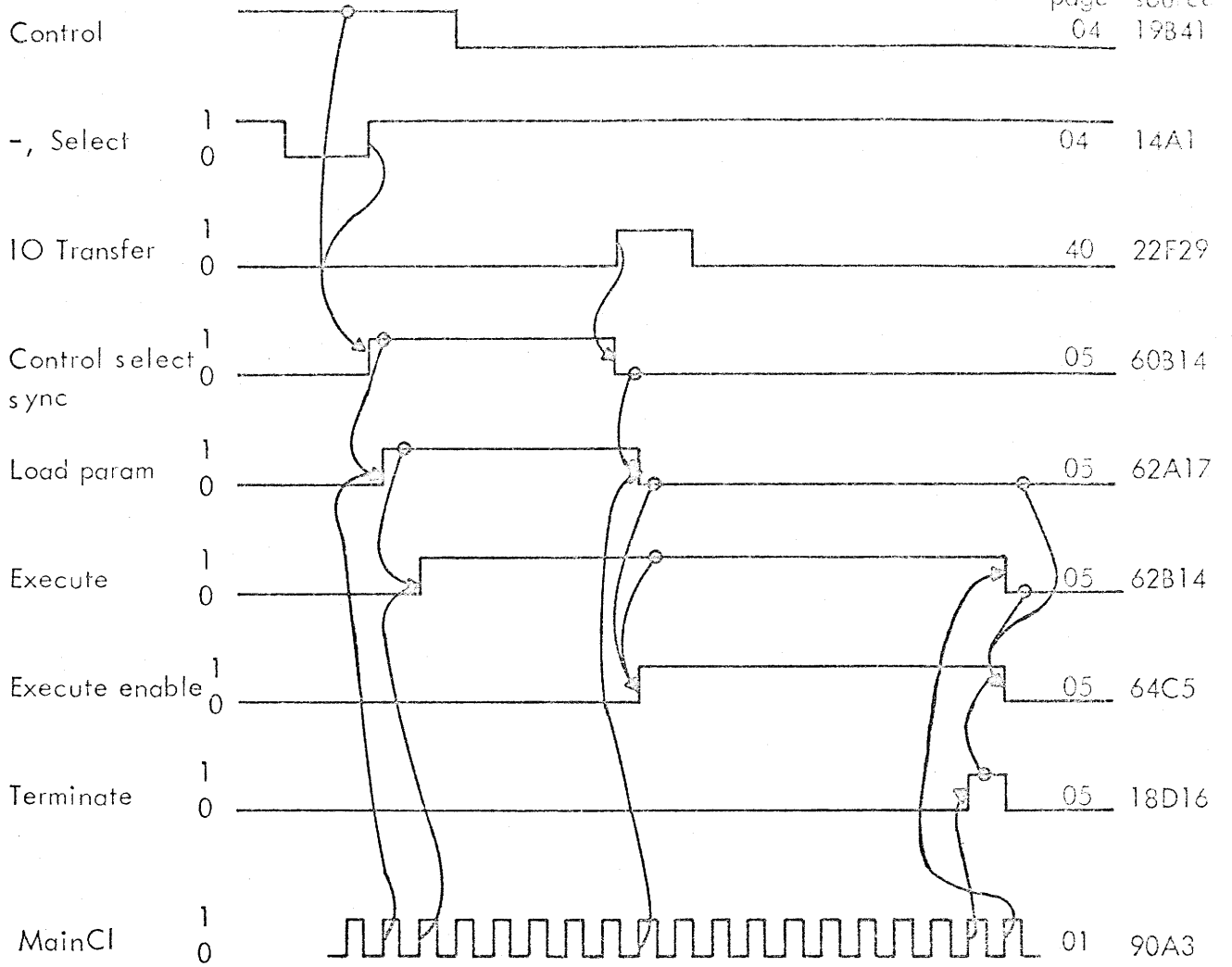
CR (13) = 1

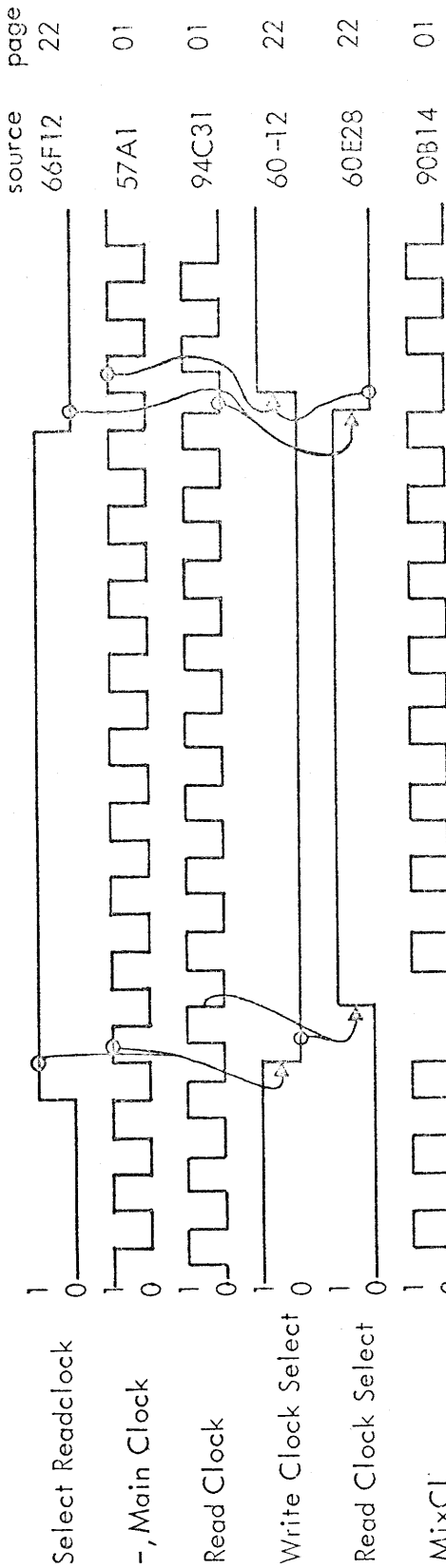
CR (14) = 1

CR (15) = 1



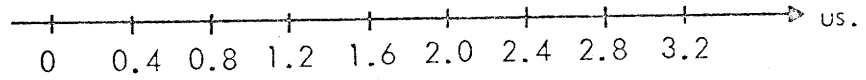
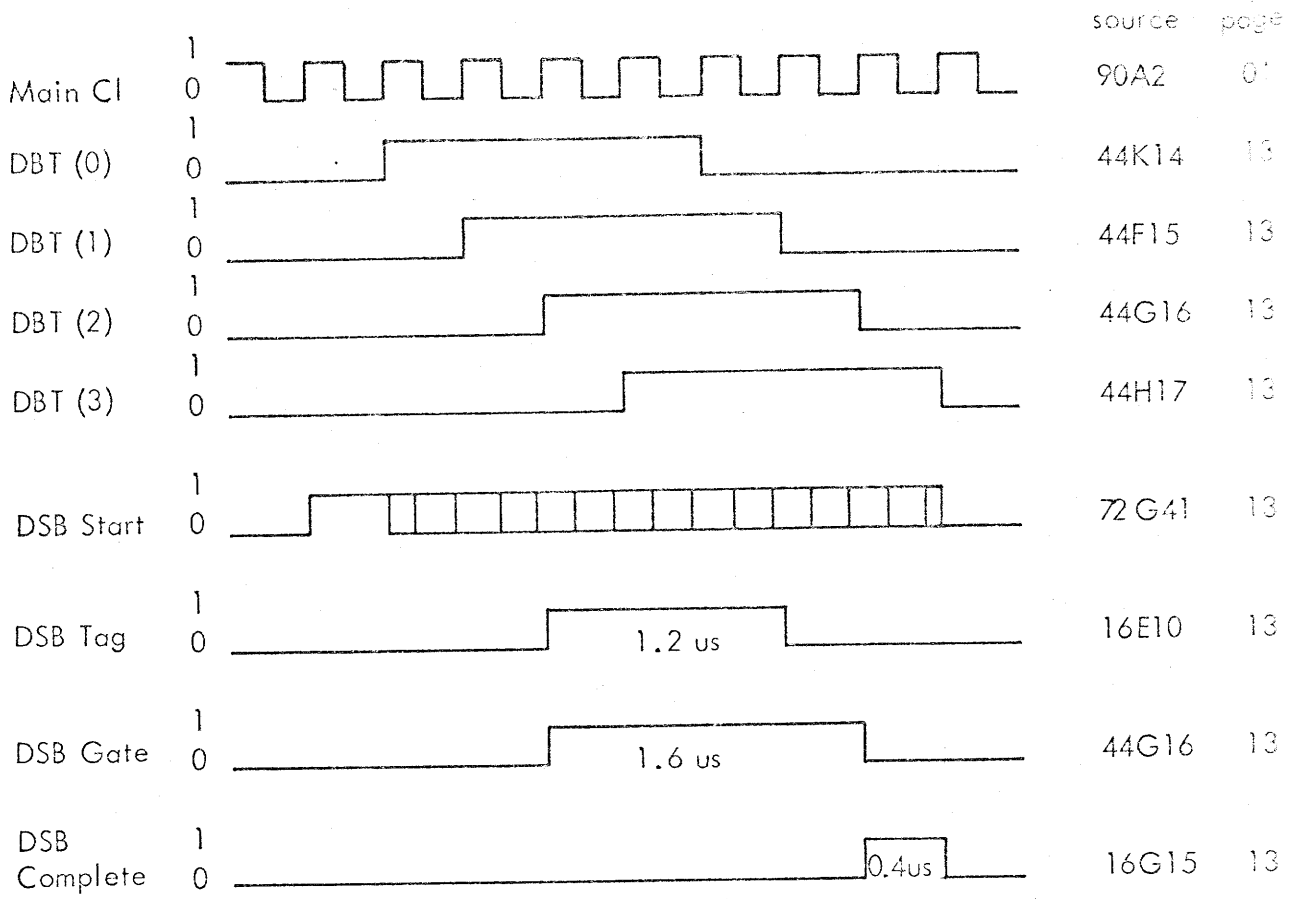
In all states: If-, Unit Ready! Seek Error! Data overrun! Pack Unsafe then go to Ready state
 In reading state: If drop out then go to Ready state.

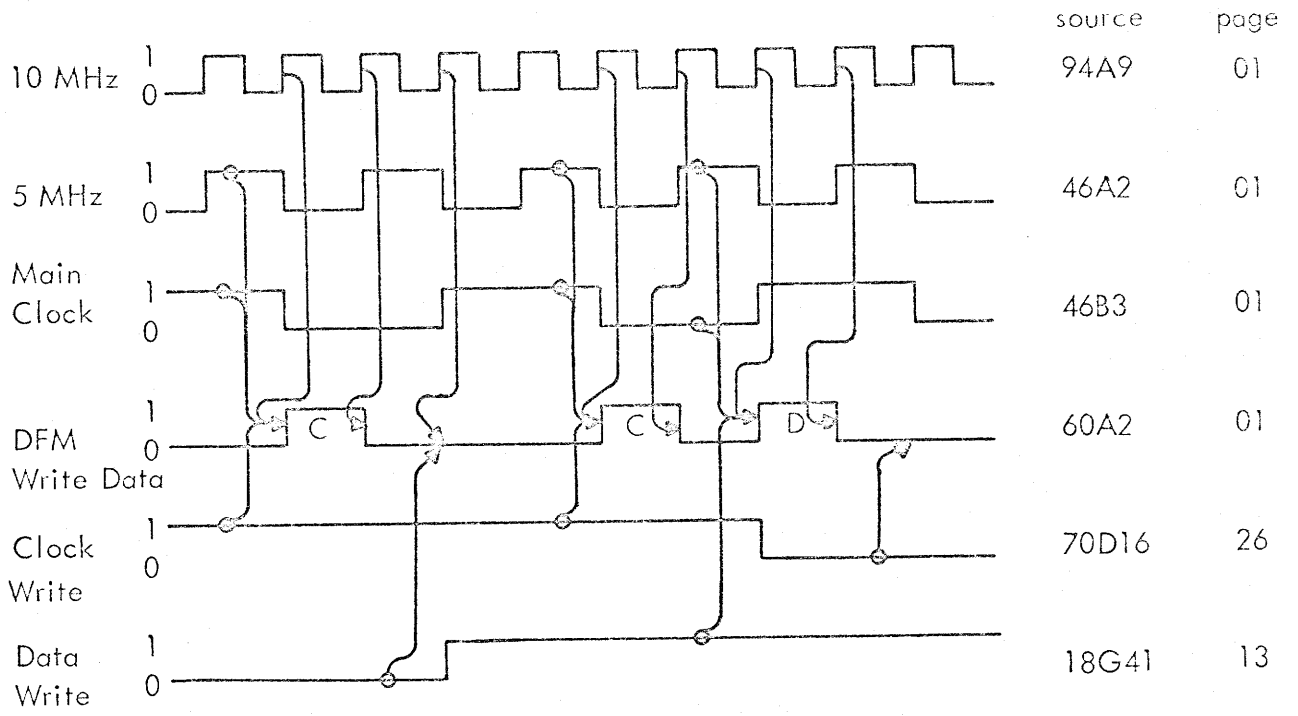
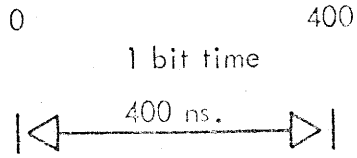


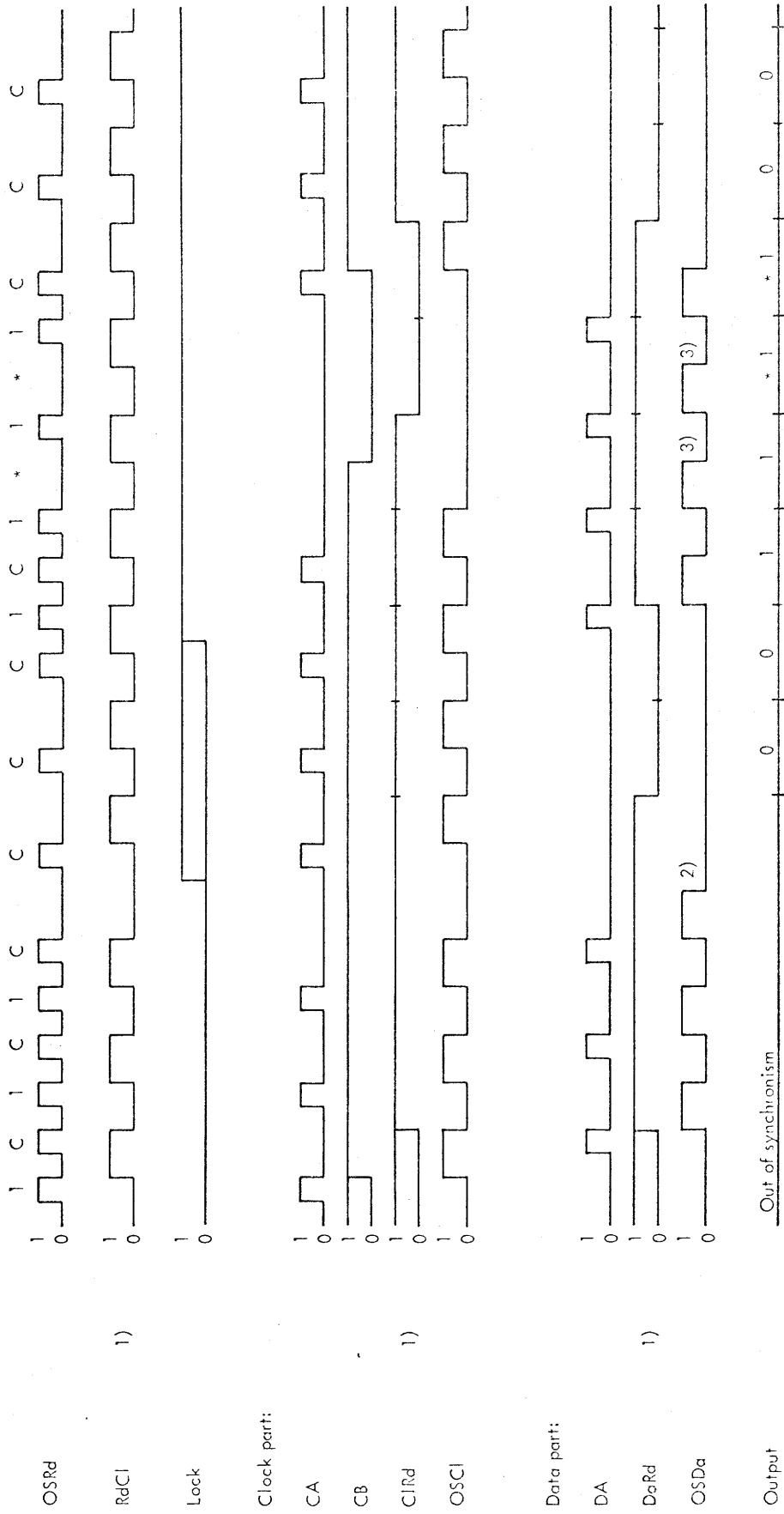


-, Read Clock Select & -, Main Clock
 -, Select Read Clock & -, Read Clock

-, Write Clock Select & Read Clock trailing
 Select Read Clock & -, Main Clock





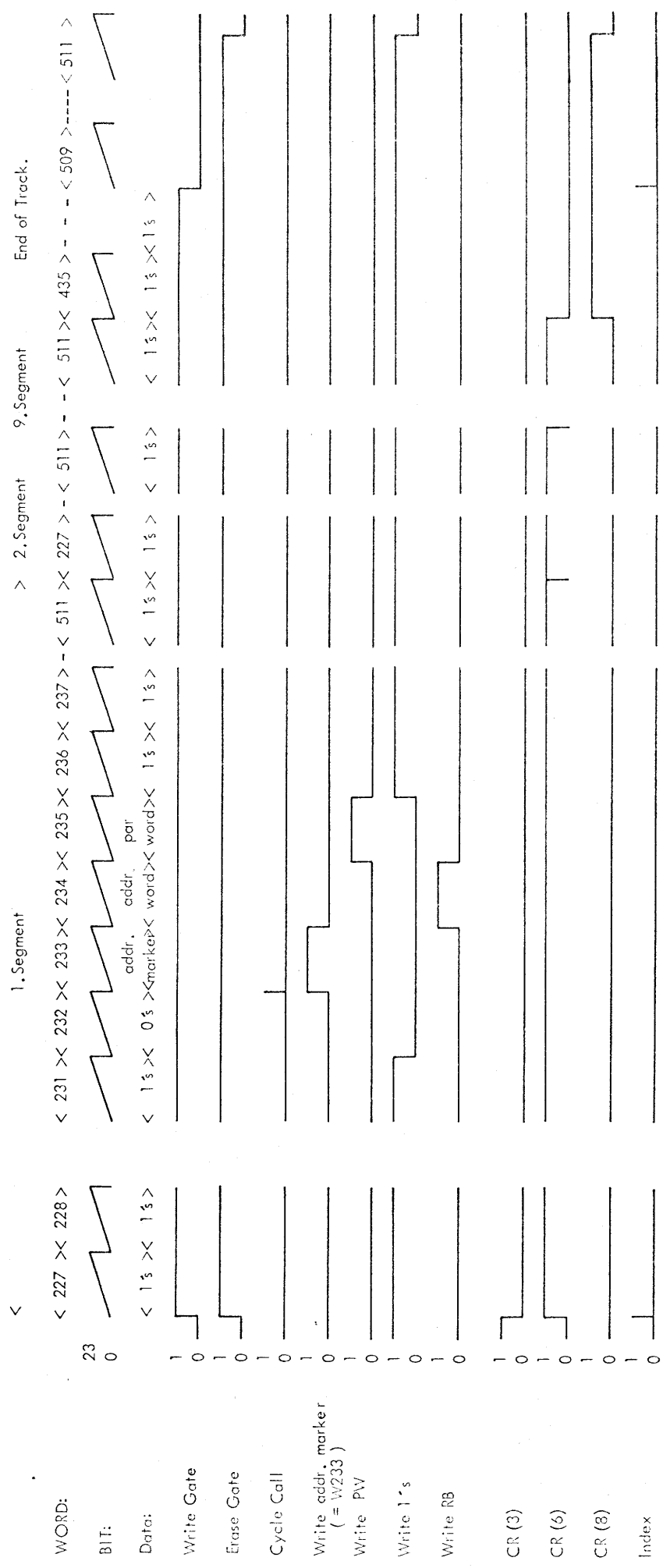


1) RdCl, ClRd, DaRd are output of the Readdetector

2) This trailing edge of OSDa does not set RdCl FF due to Lock = 0

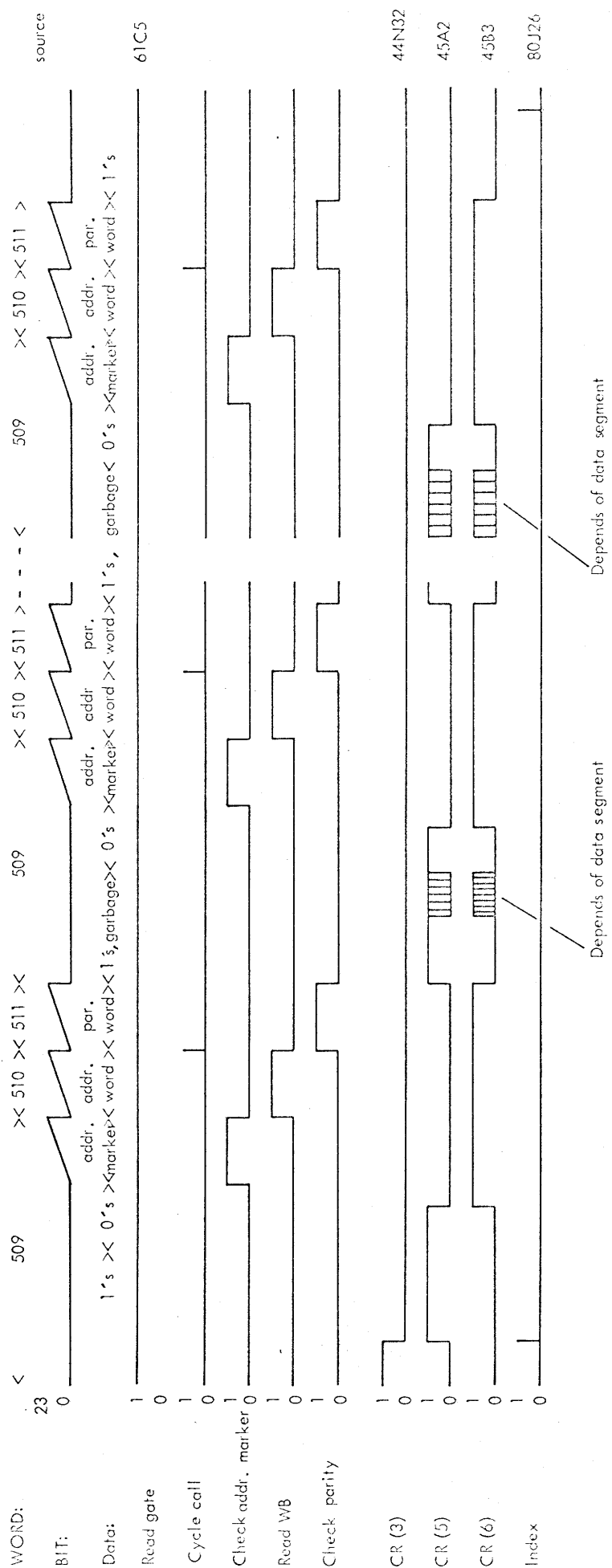
3) - - - sets RdCl FF due to Lock = 1.

1. Write Segment Addresses.

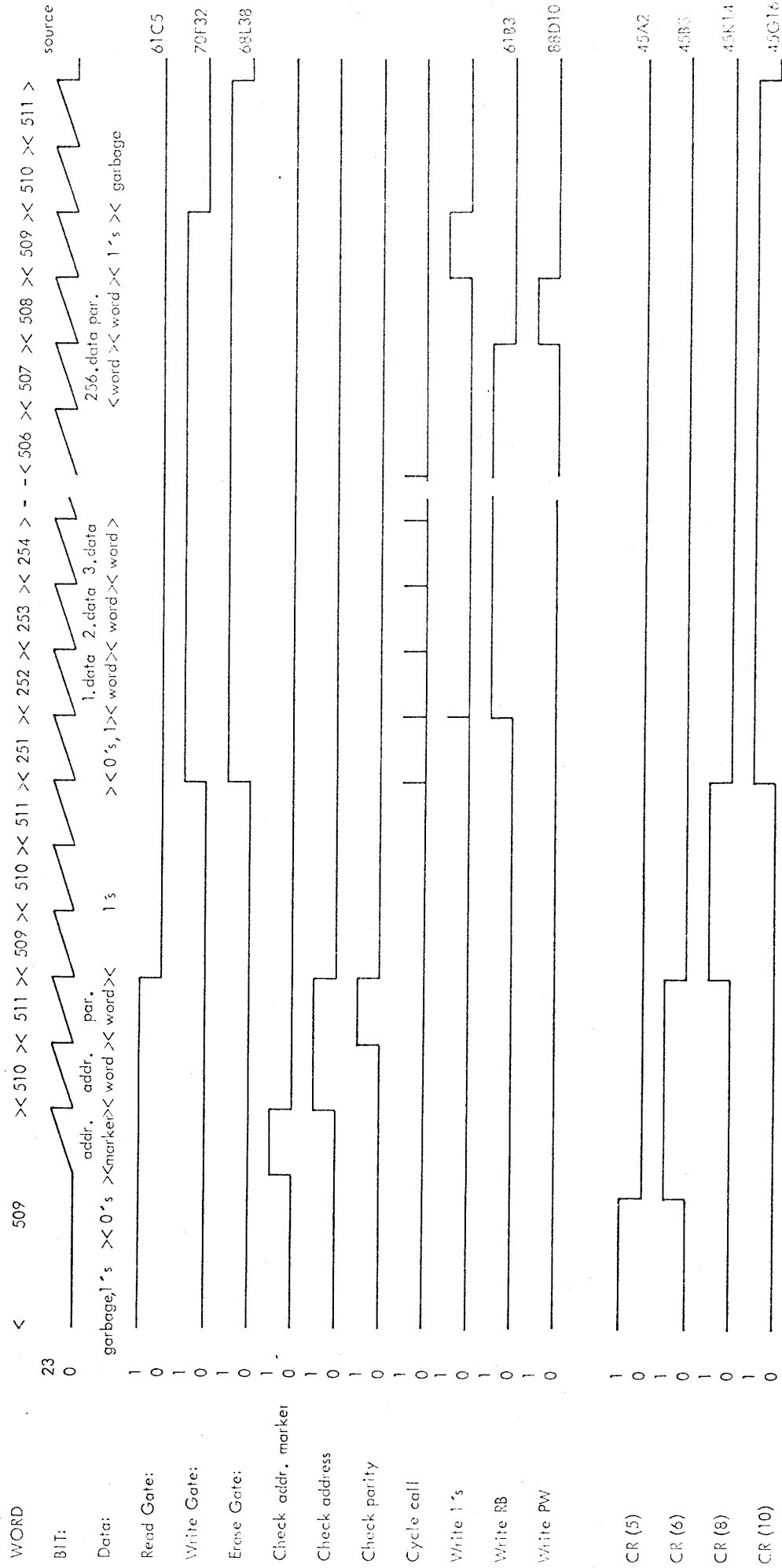


1 word time = 9.6 us

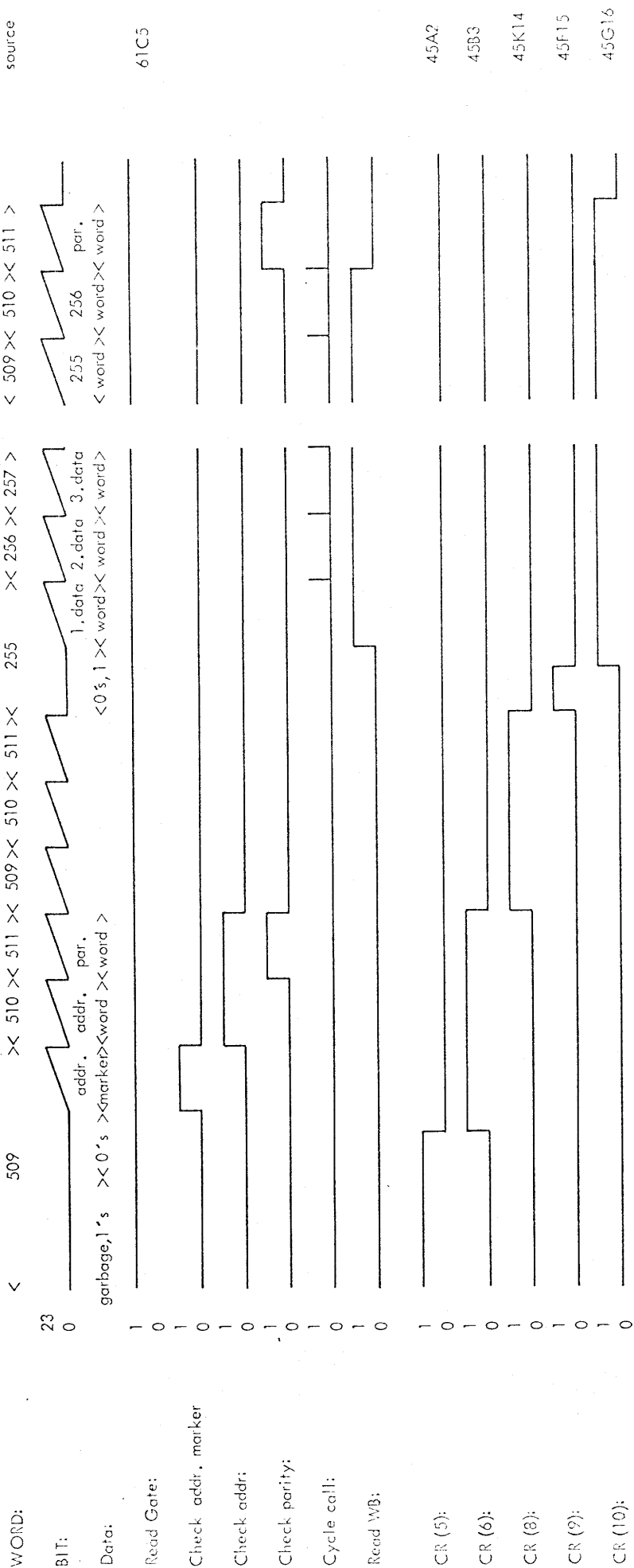
2. Read Segment Addresses.



3. Write data



4. Read data



DFC403

PCBA Positionlist

Position	PCBA
DFC005	RC2059-1
DFC010	RC0956-1
DFC011	RC0935-3
DFC012	RC0935-3
DFC013	RC3032-1
DFC014	RC0834-1
DFC015	RC0834-1
DFC016	RC0956-1
DFC017	RC0834-1
DFC018	RC0839-1
DFC019	RC0901-1
DFC020	RC0897-1
DFC021	RC0897-1
DFC022	RC0897-1
DFC023	RC0897-1
DFC024	RC0897-1
DFC025	RC3032-1
DFC026	RC0839-1
DFC027	RC0838-1
DFC028	RC0847-1
DFC029	RC0839-1
DFC030	RC0935-3
DFC031	RC0935-3
DFC032	RC0898-1
DFC033	RC0898-1
DFC034	RC0898-1
DFC035	RC0898-1
DFC036	RC0898-1
DFC037	RC0898-1
DFC038	RC0935-3
DFC039	RC0935-3
DFC040	RC0935-3
DFC041	RC0935-3
DFC042	RC0935-3
DFC043	RC0935-3
DFC044	RC0935-3
DFC045	RC0935-3
DFC046	RC0935-1

V23293

150373 Ment 1080972MOGK

V23294

150173 Rev-7 080972MOGK

Position	PCBA
DFC047	RC0935-1
DFC048	RC0935-1
DFC049	RC0935-1
DFC050	RC0935-1
DFC051	RC0935-1
DFC052	RC0935-1
DFC053	RC0839-1
DFC054	RC0839-1
DFC055	RC0834-1
DFC056	RC0956-1
DFC057	RC0834-1
DFC058	RC0838-1
DFC059	RC2060-1
DFC060	RC0835-1
DFC061	RC0956-1
DFC062	RC2060-1
DFC063	RC0847-1
DFC064	RC0956-1
DFC065	RC0858-1
DFC066	RC0956-1
DFC067	RC0834-1
DFC068	RC0834-1
DFC069	RC2060-1
DFC070	RC0839-1
DFC071	RC0956-1
DFC072	RC0839-1
DFC073	RC3032-1
DFC074	RC3032-1
DFC075	RC0834-1
DFC076	RC0835-1
DFC077	RC0957-1
DFC078	RC0995-1
DFC079	RC2056-1
DFC080	RC2056-1
DFC081	RC2056-1
DFC082	RC2057-1
DFC083	RC2057-1
DFC084	RC2057-1
DFC087	RC0888-1/1
DFC088	RC3032-1
DFC089	RC0847-1
DFC090	RC0836-1

V23421

040573 MOJ 080972MOGK

Position

PCBA

DFC091	RC0890-1
DFC092	RC2060-1
DFC093	RC0894-1
DFC094	RC2074-1
DFC095	RC0834-1
DFC096	RCC835-1
DFC097	RC0834-1
DFC099	RC0957-1
DFC100	RC0858-1

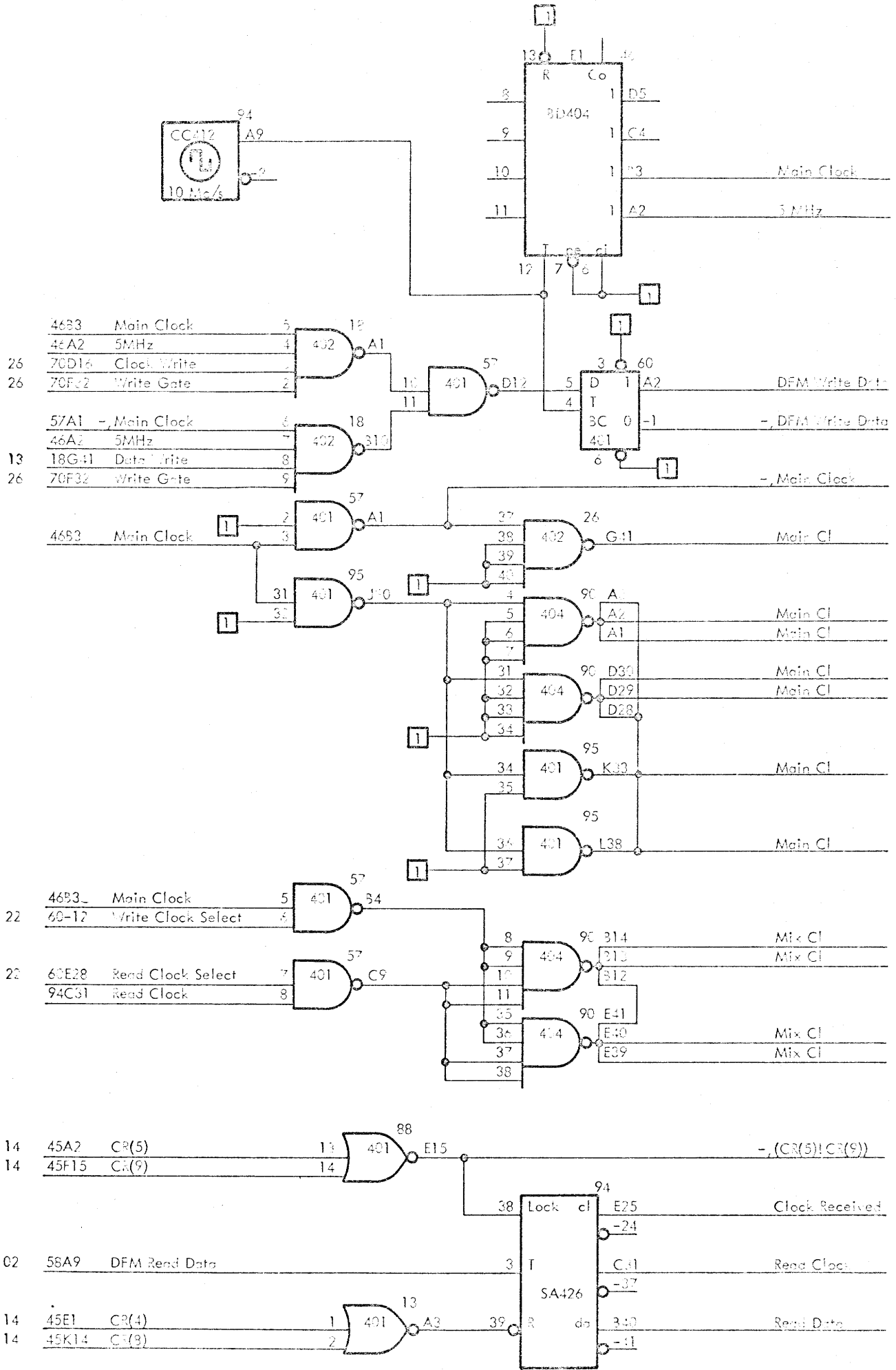
RC4000

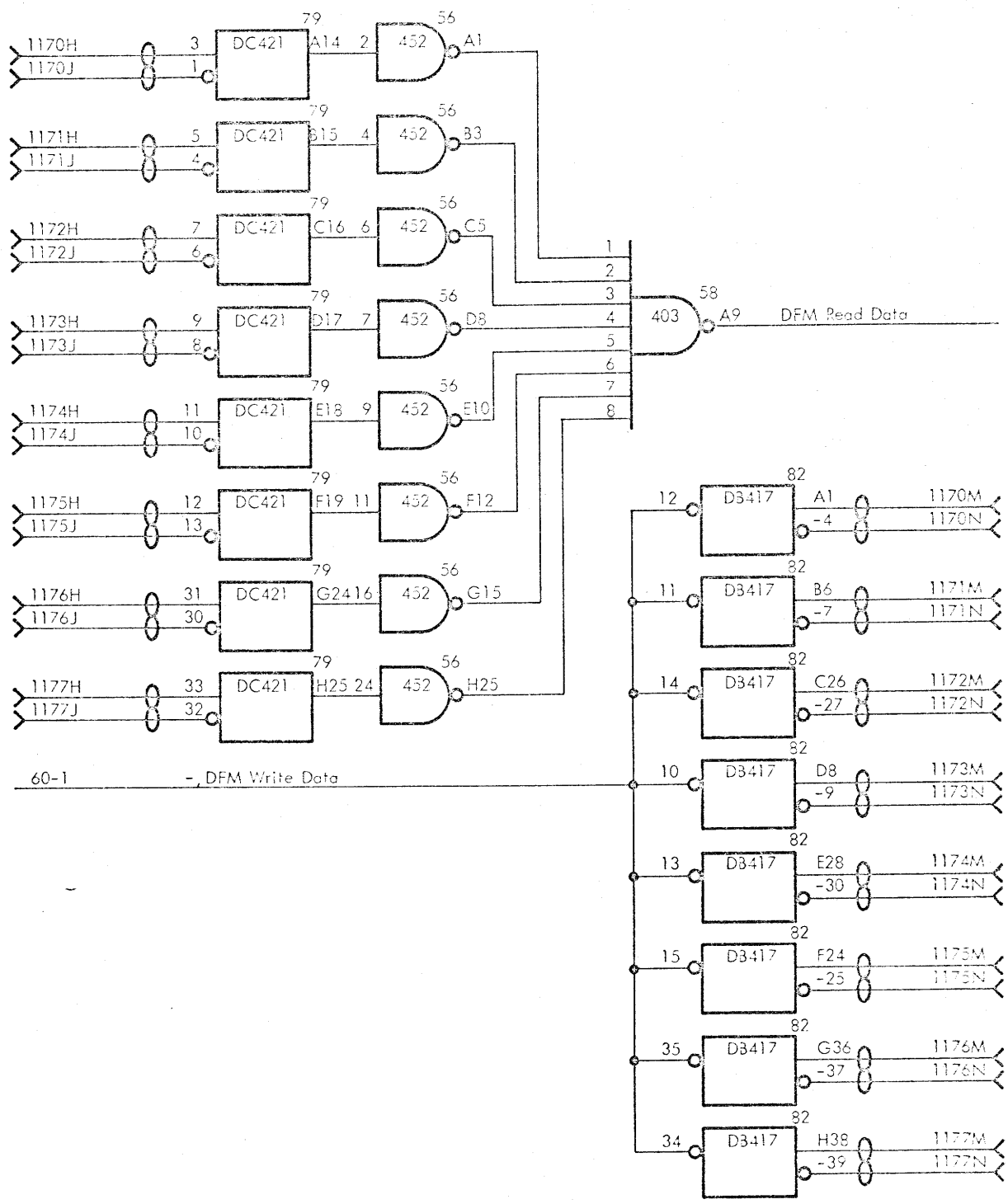
PCBA Positionlist

DFC403

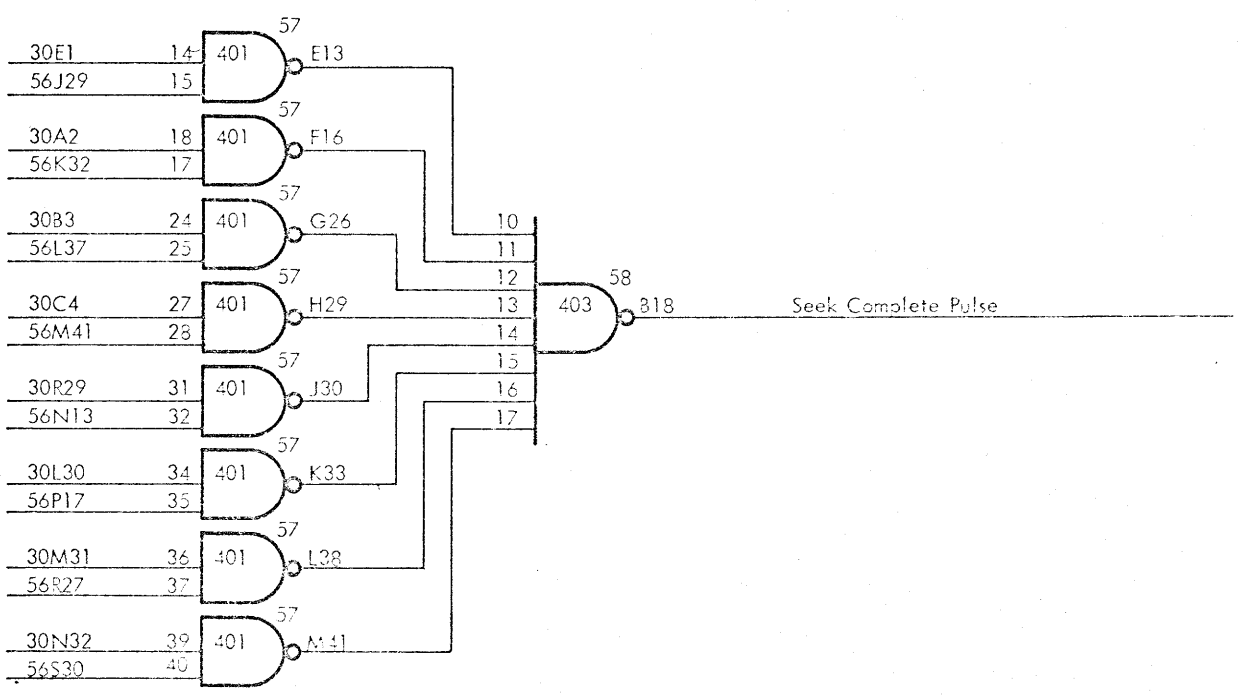
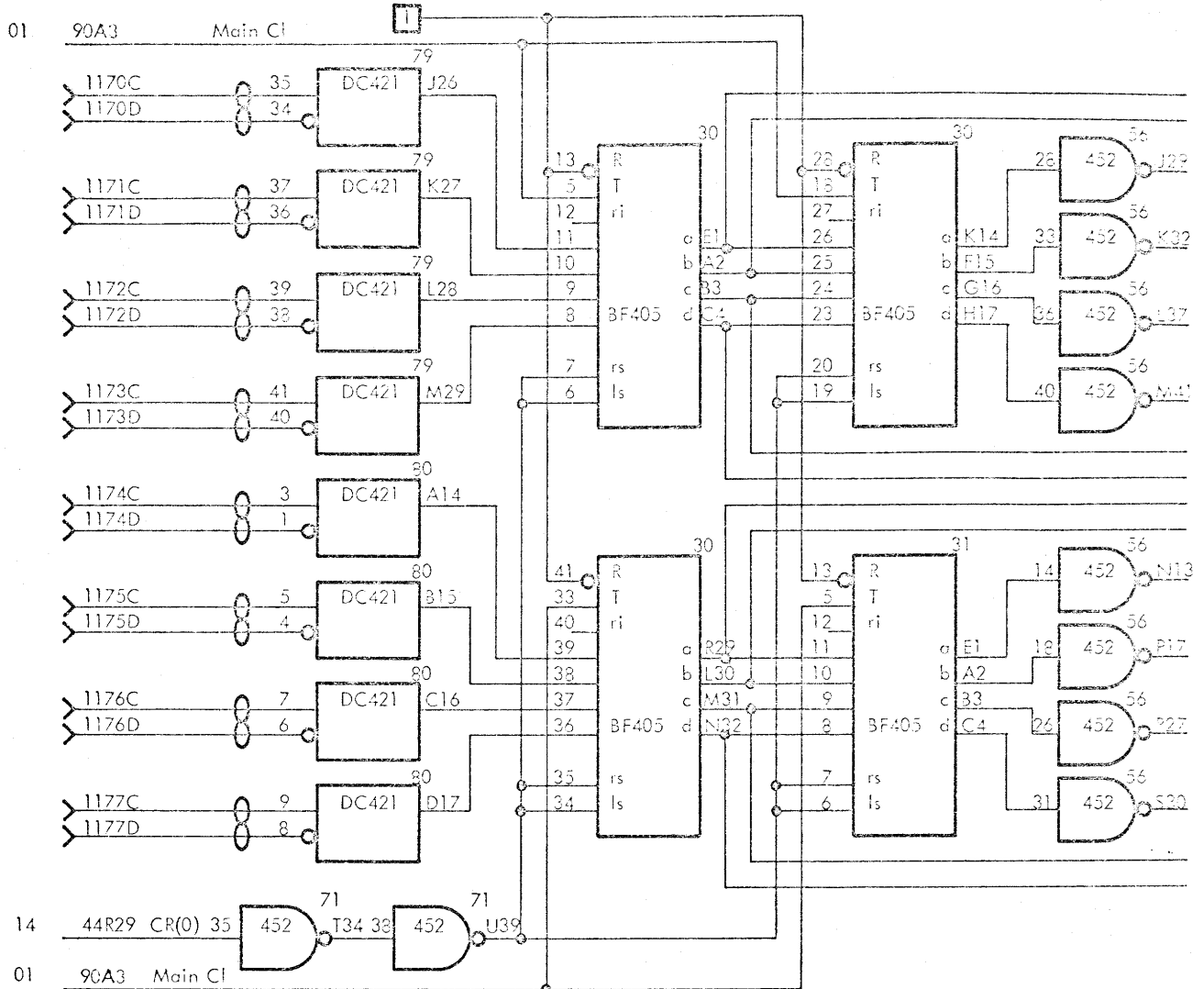
V23457

p. 3 of 3





01 60-1 - DFM Write Data



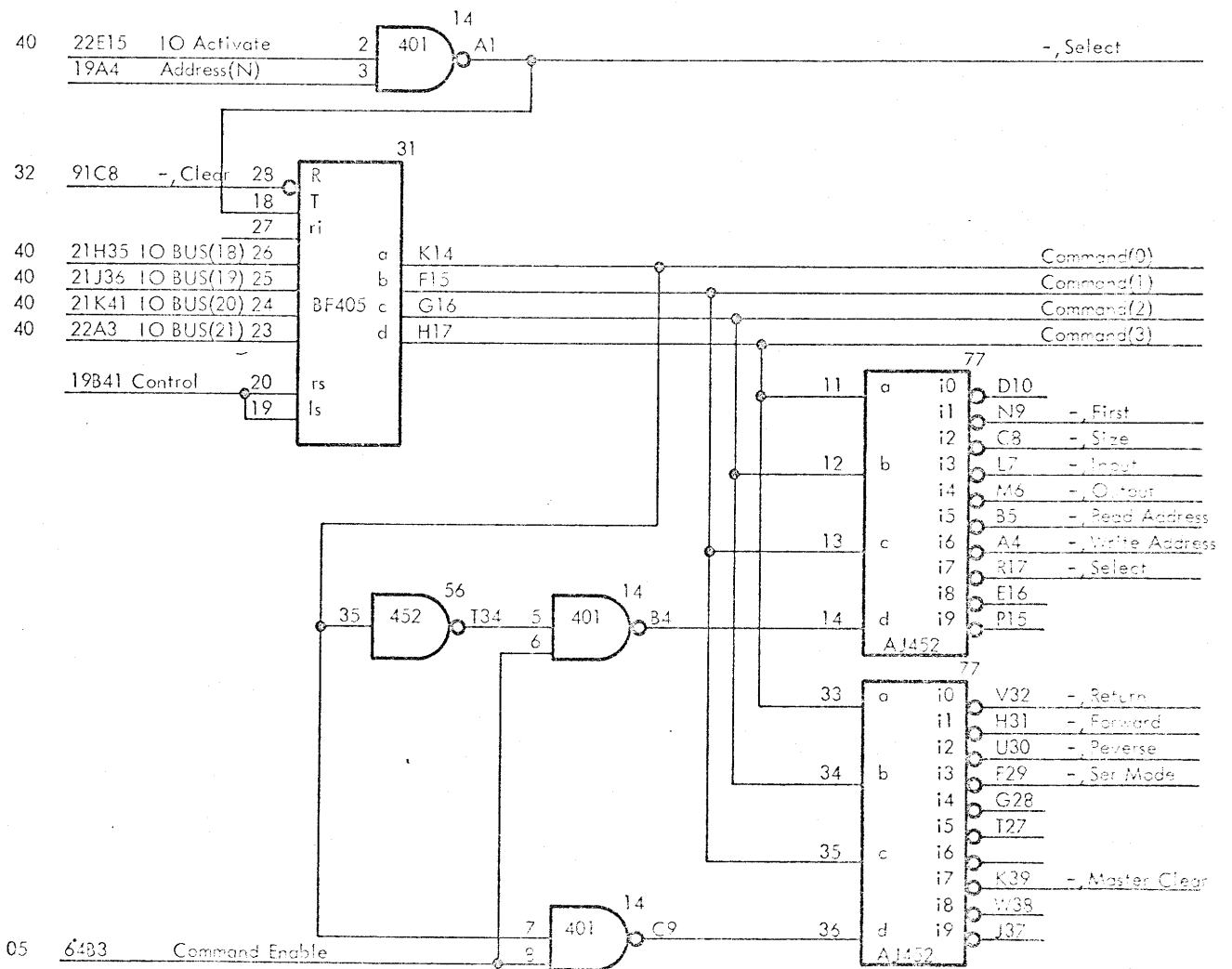
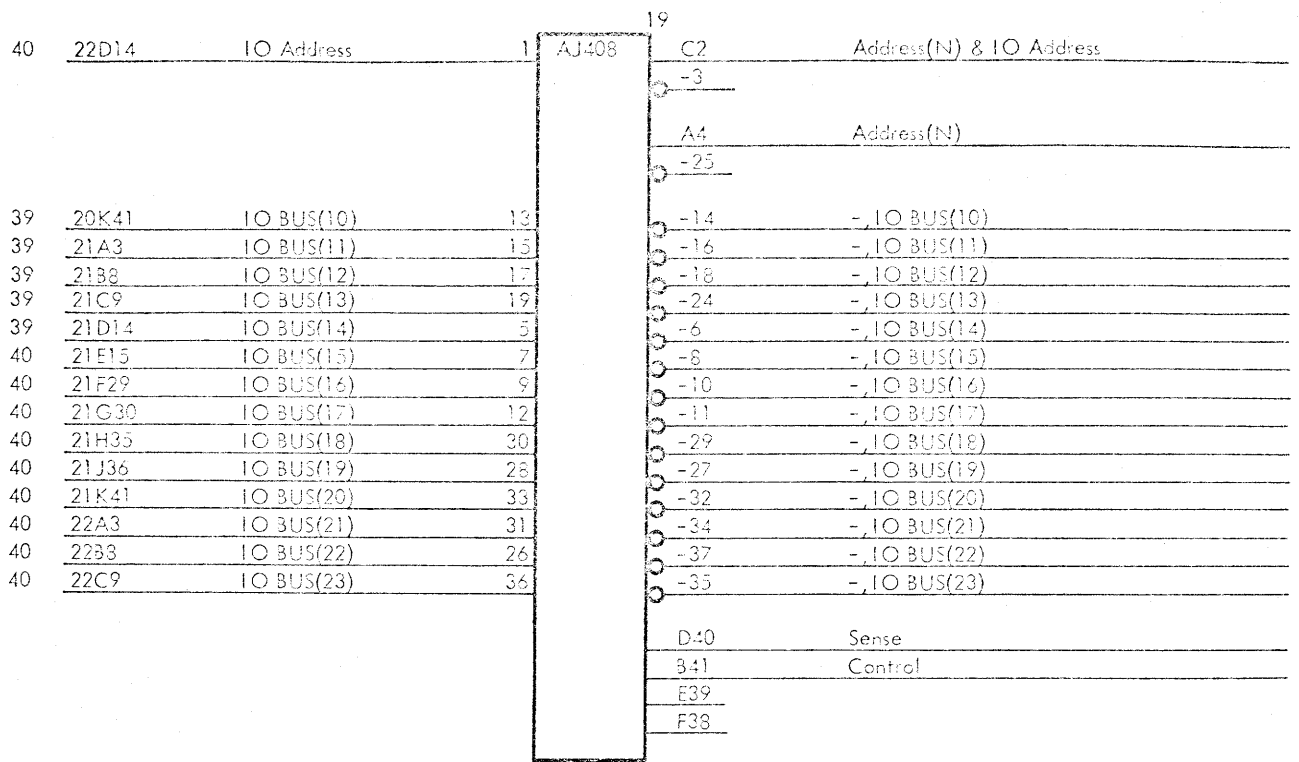
DFC 403
RC4000

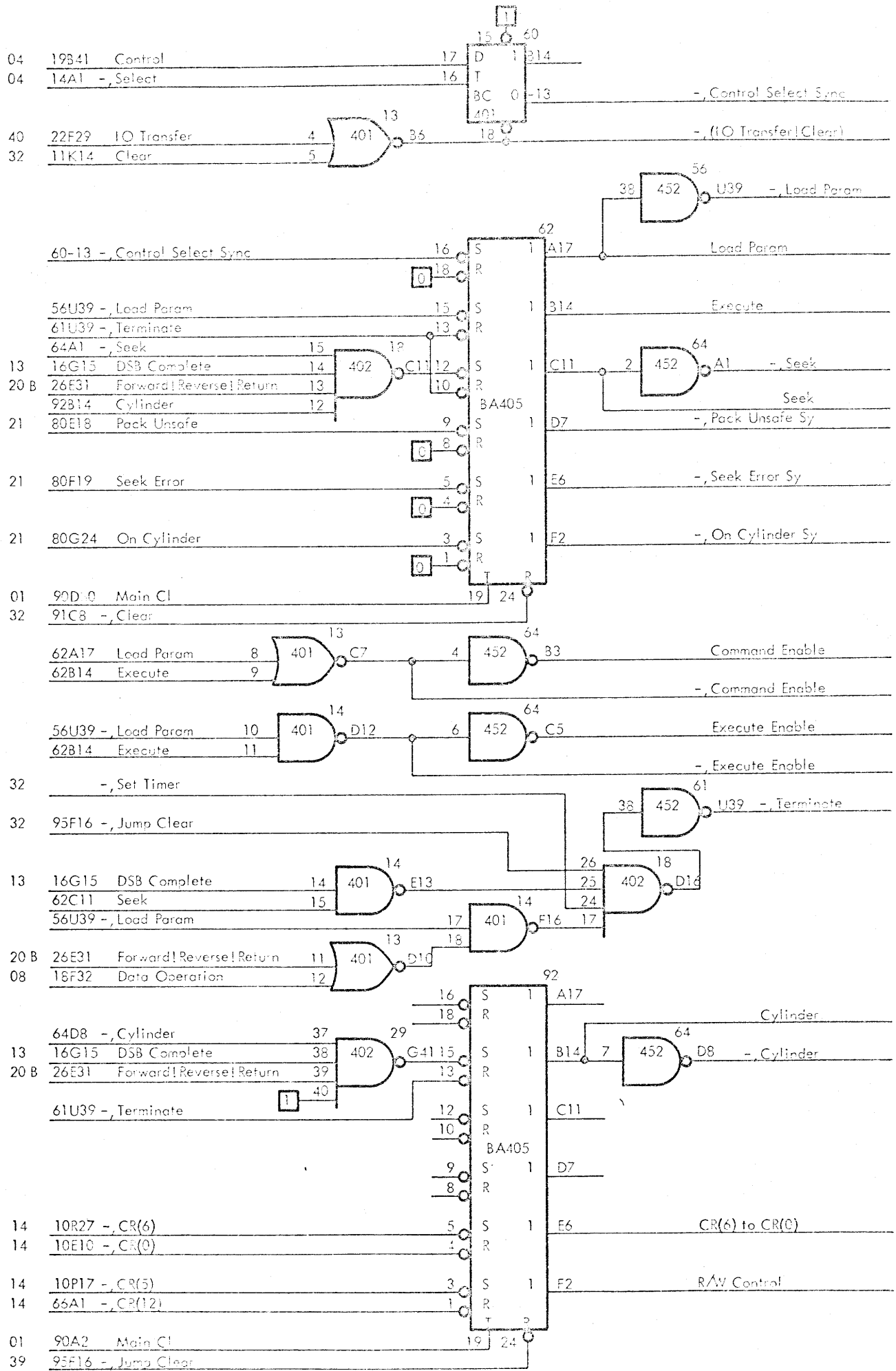
SEEK COMPLETE LOGIC

DFC03

R 10531

Logic Diagram

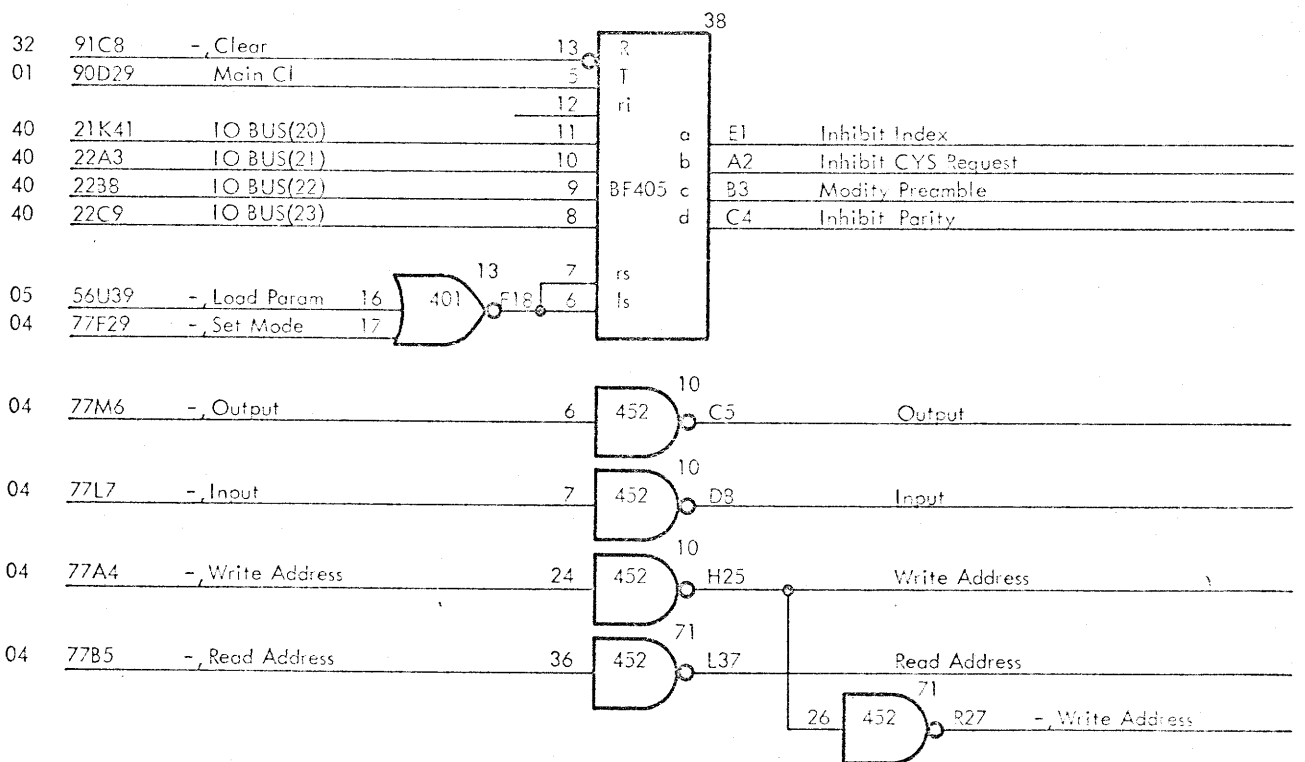
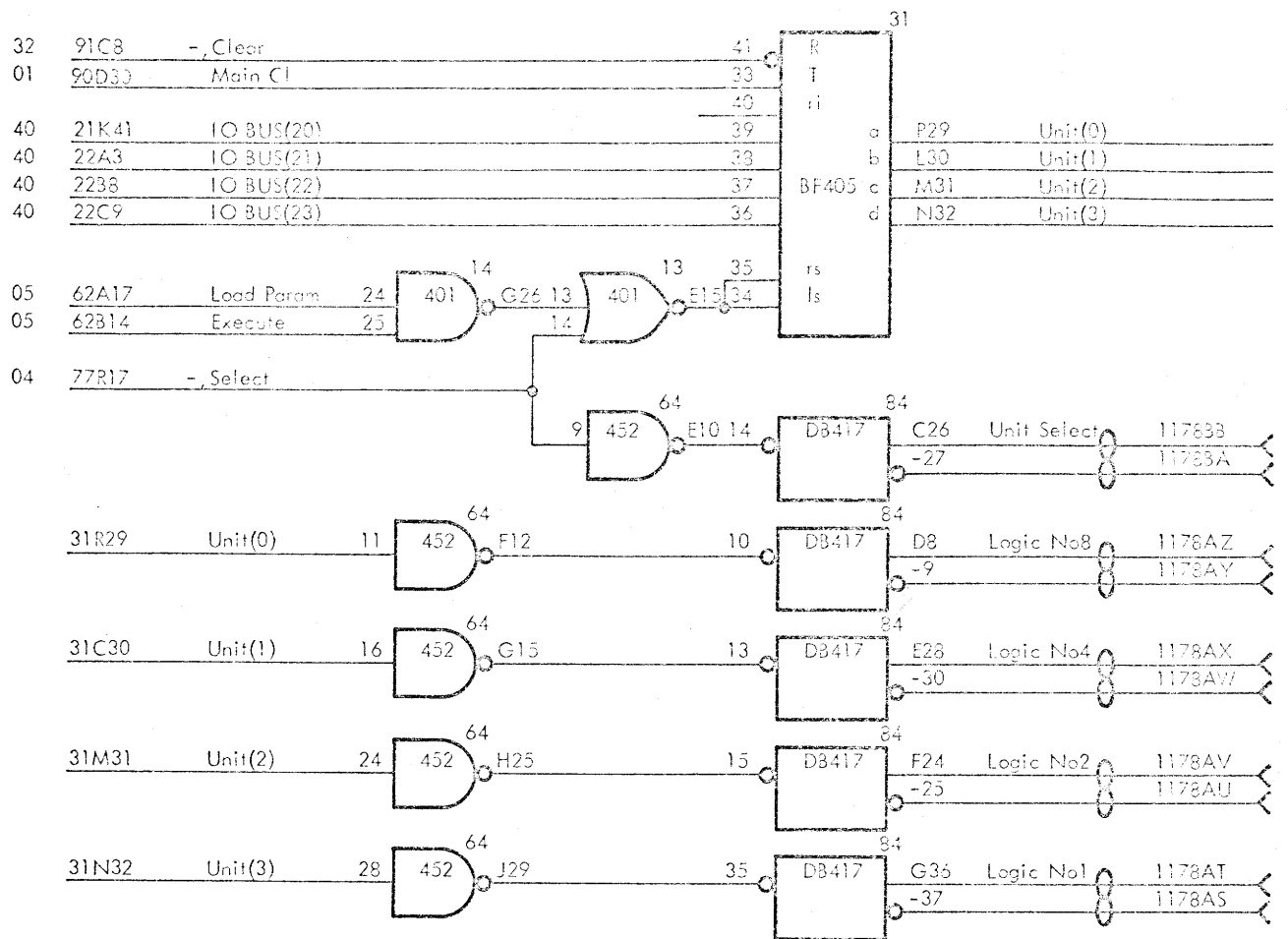


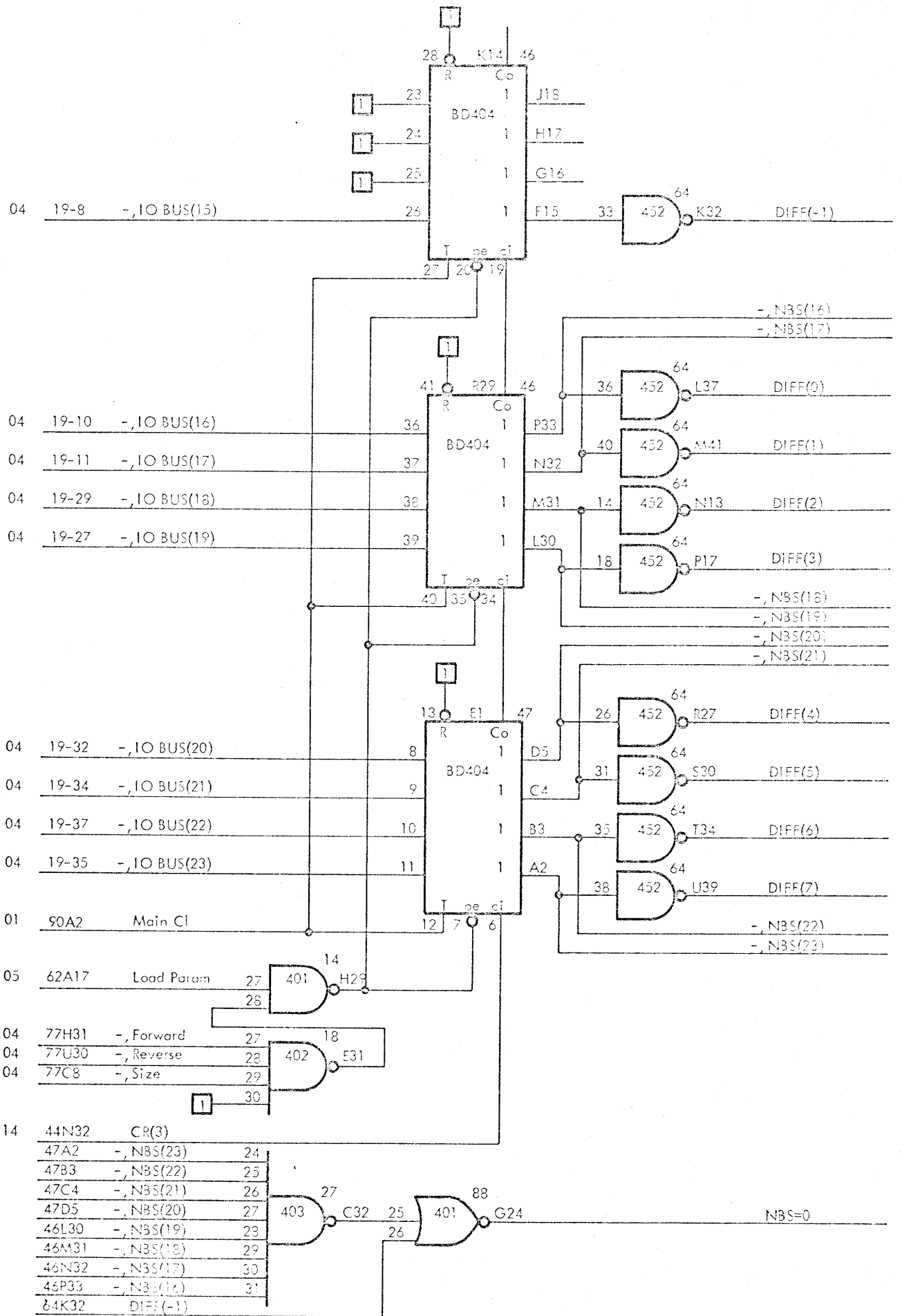


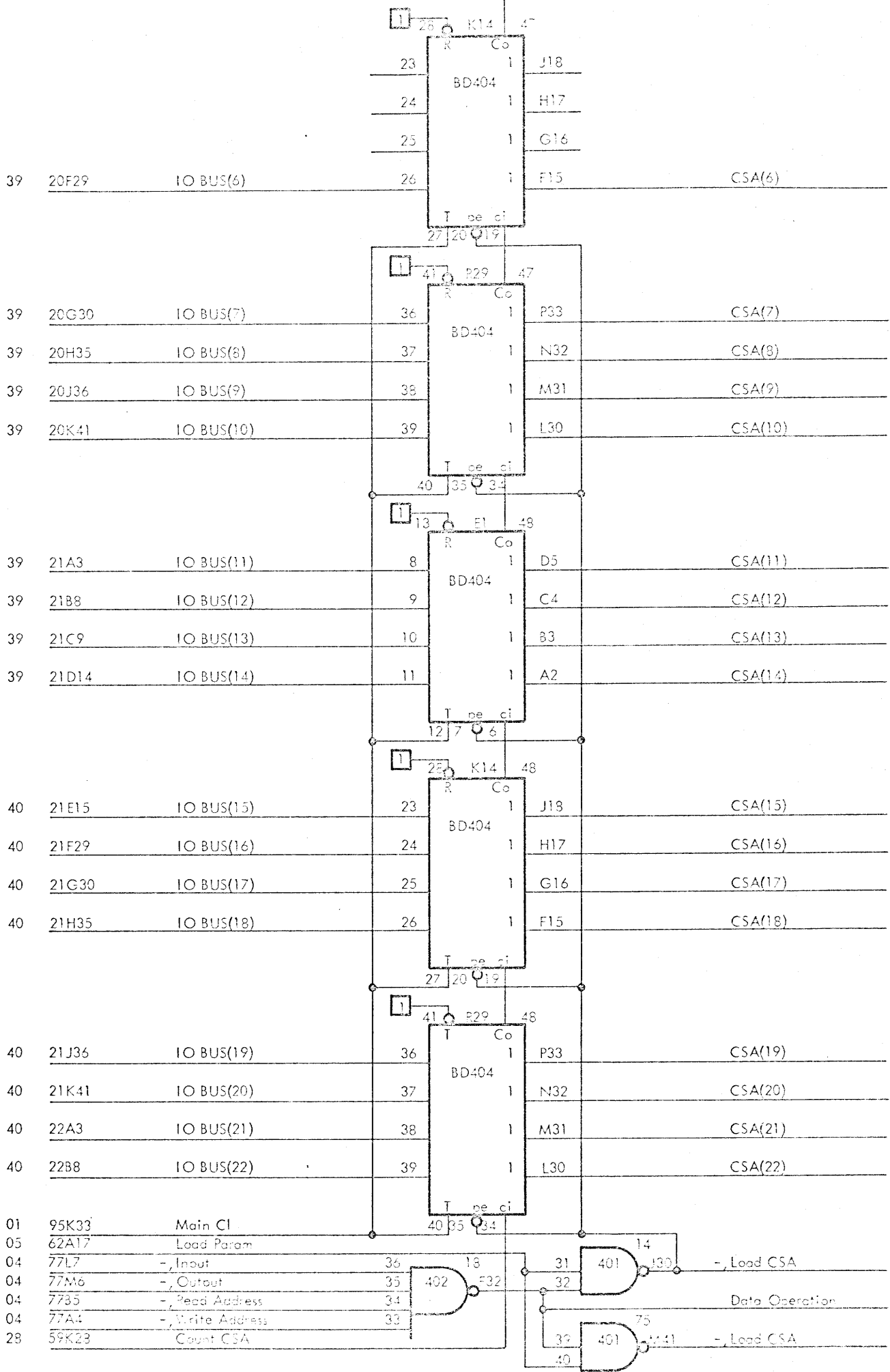
DFC 403
RC4000

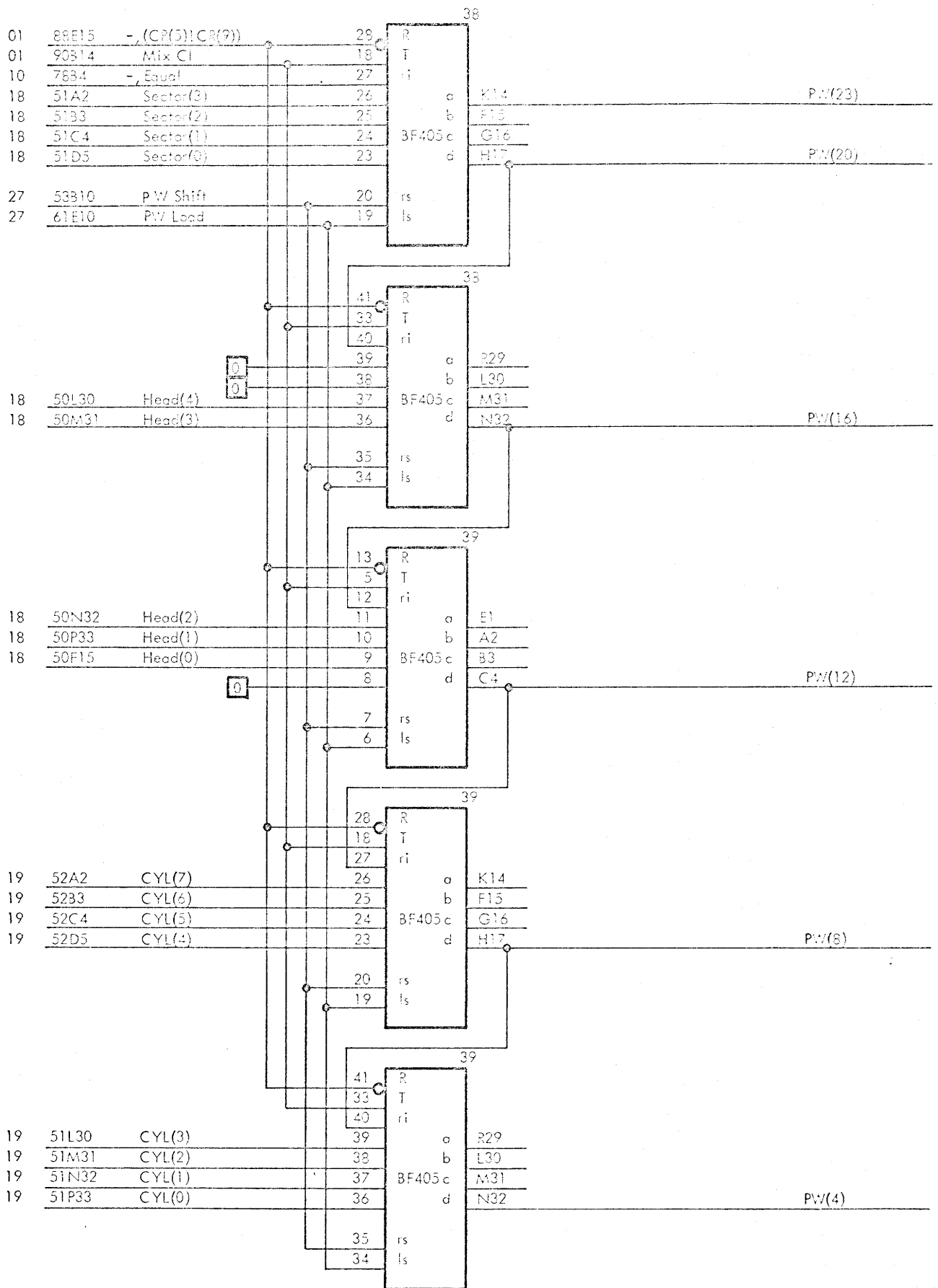
LOAD AND EXECUTE CONTROL

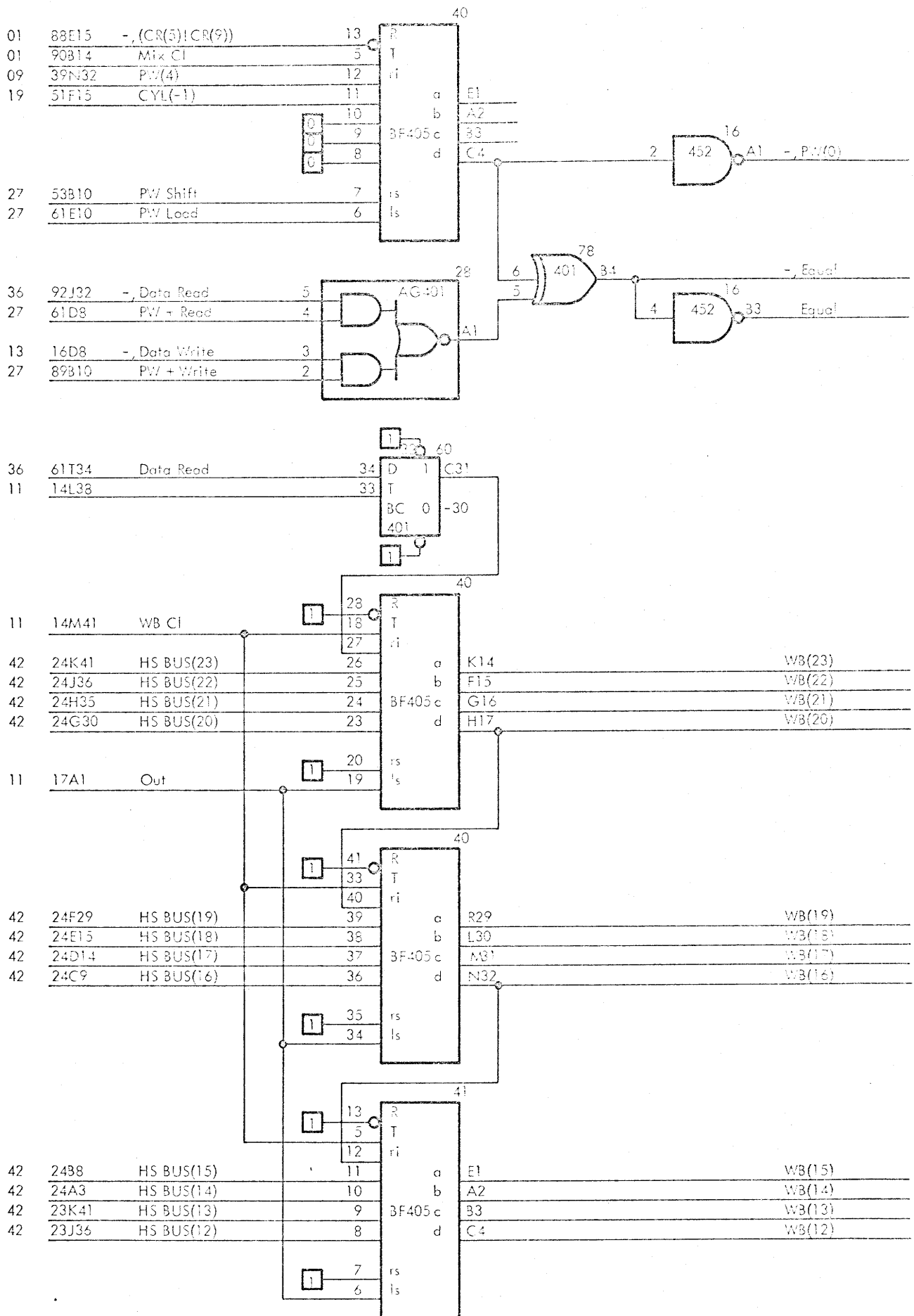
DFC05

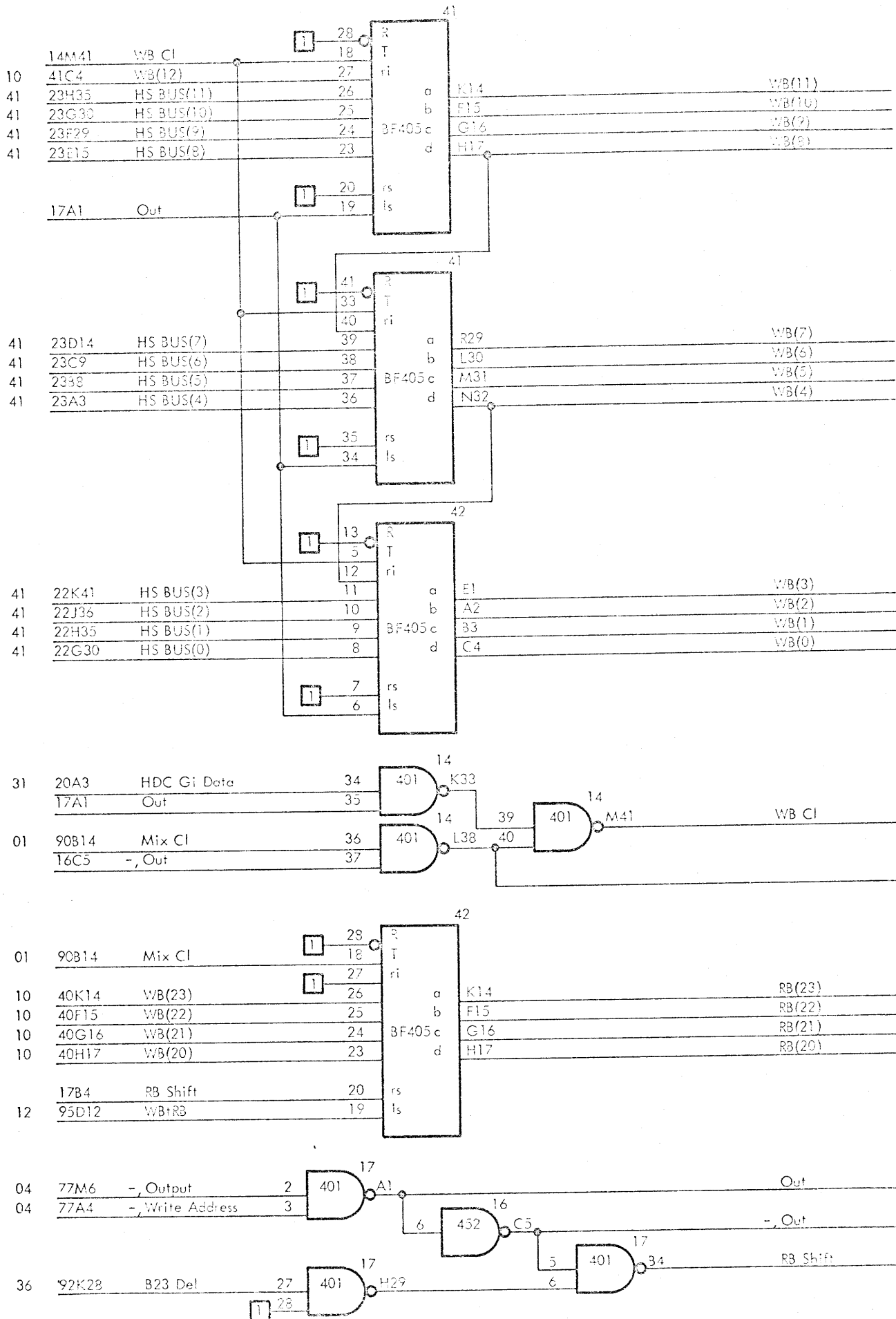








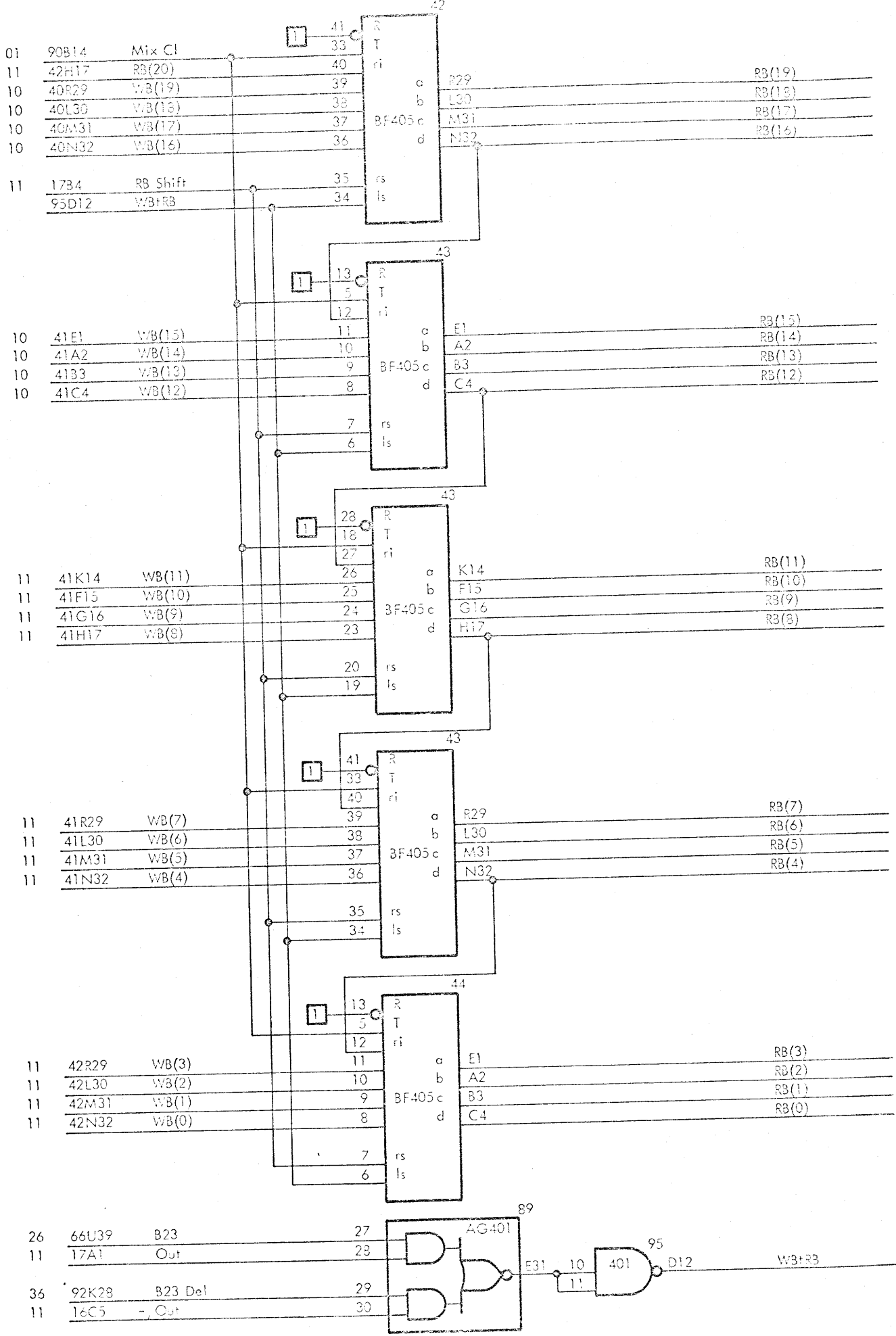




DFC 403
RC4000

WRITE BUFFER, WB(0:11), READ BUFFER, RB(20:23)

DFC11



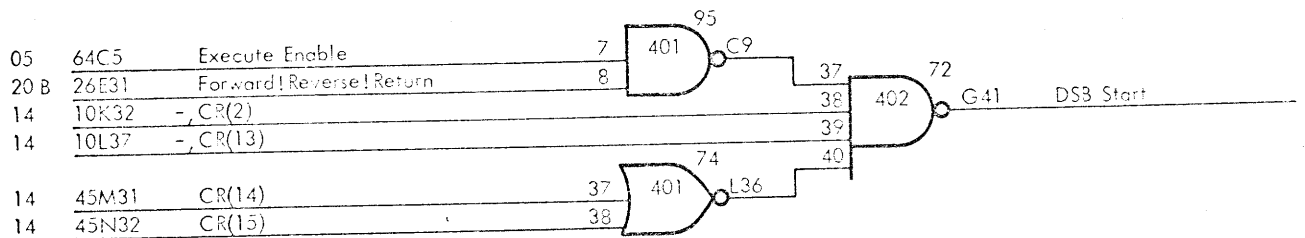
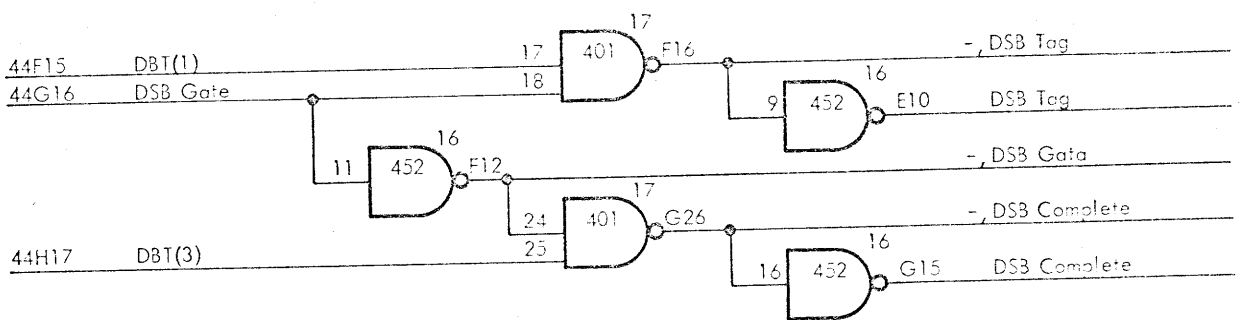
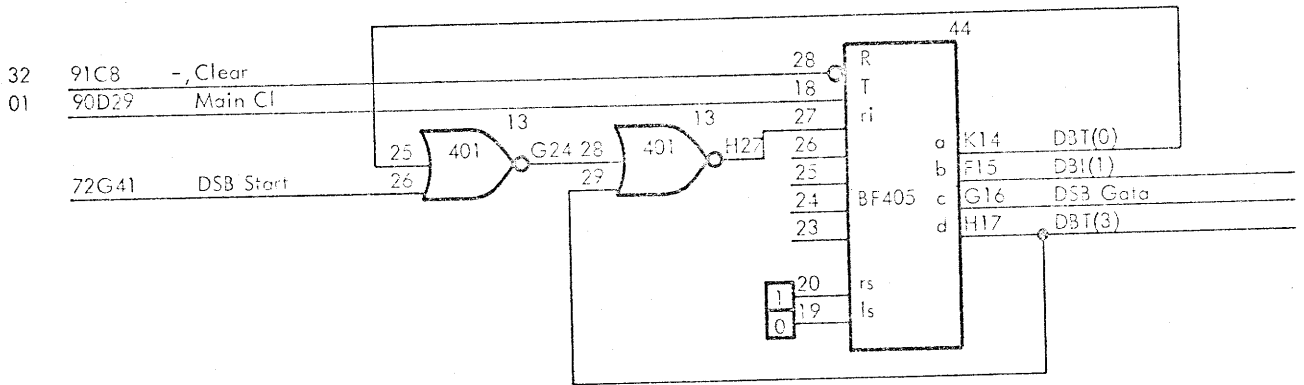
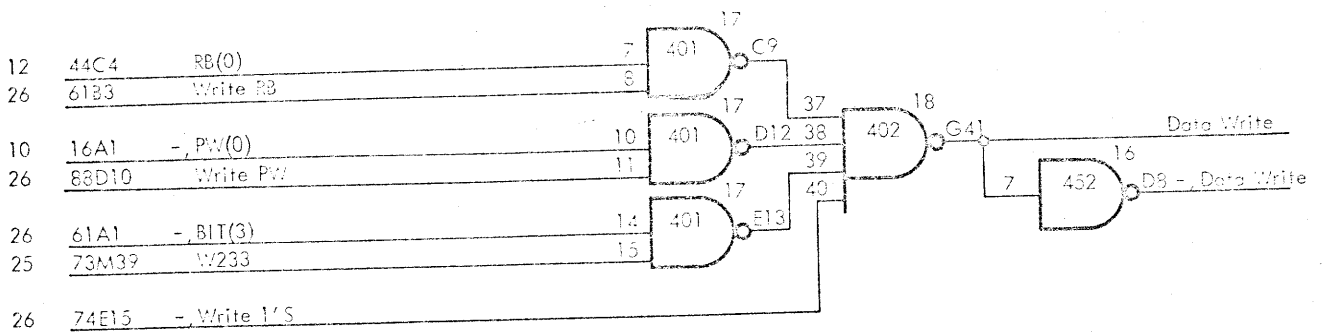
DFC 403
RC4000

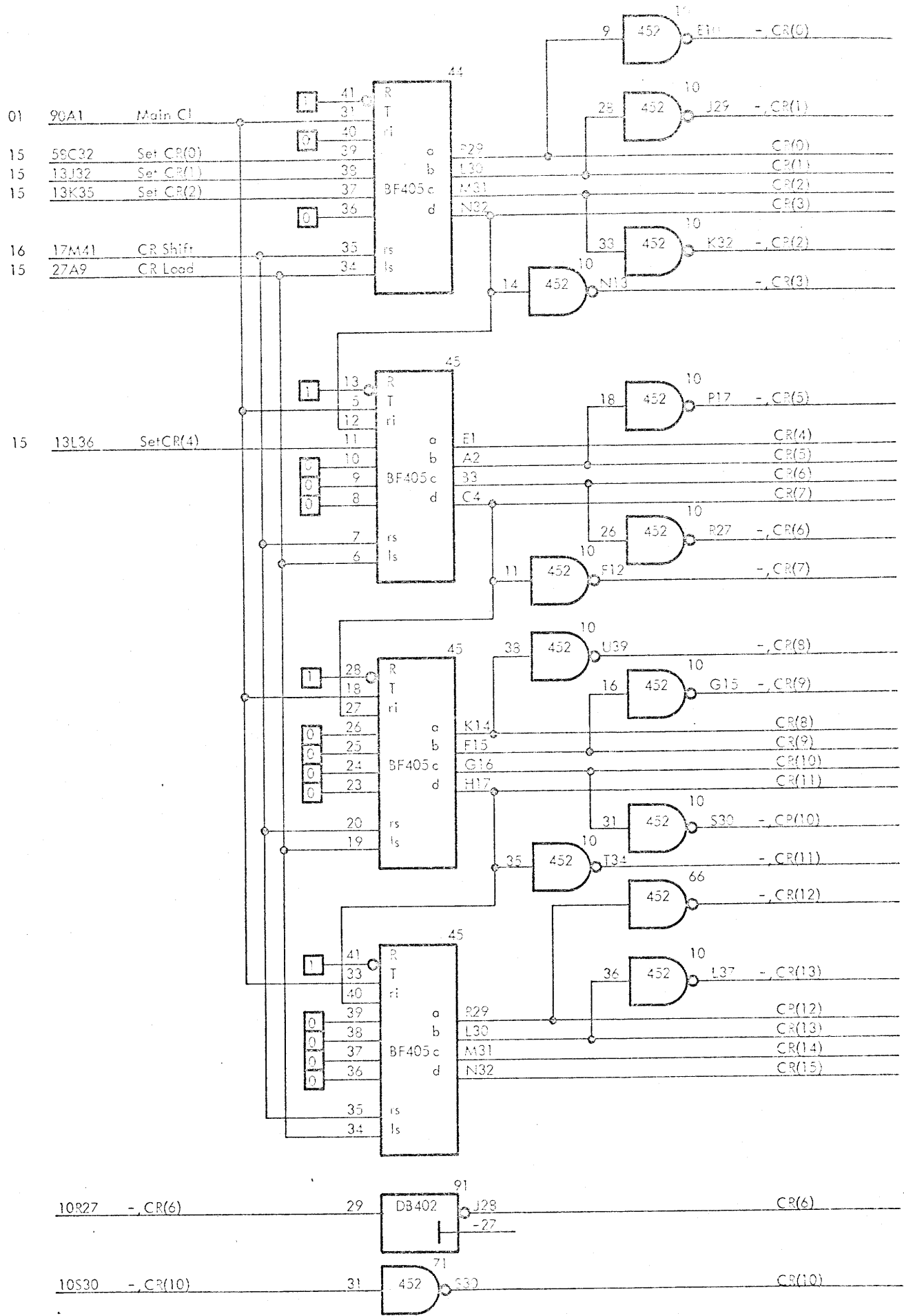
READ BUFFER, RB(0:19)

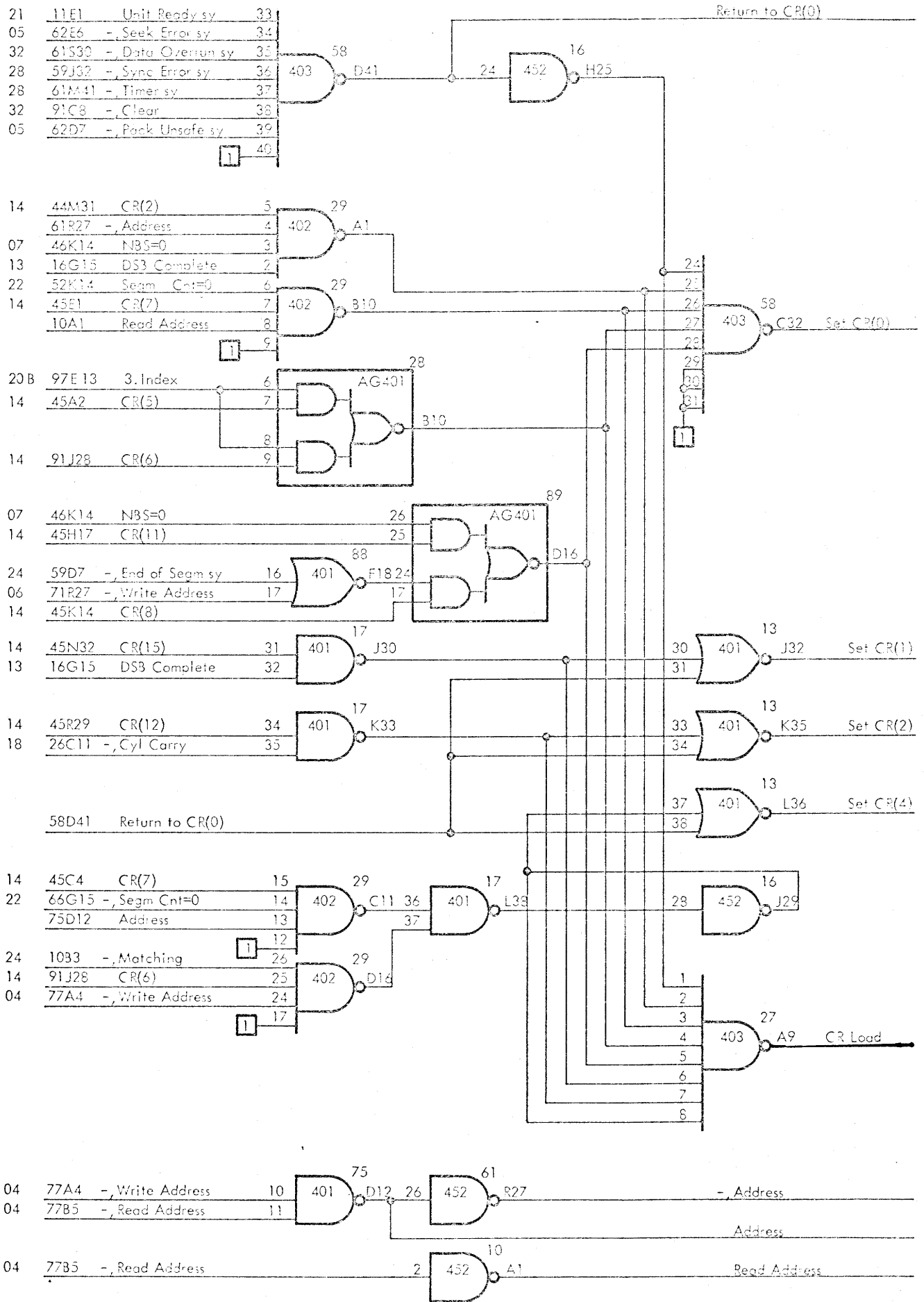
DFC12

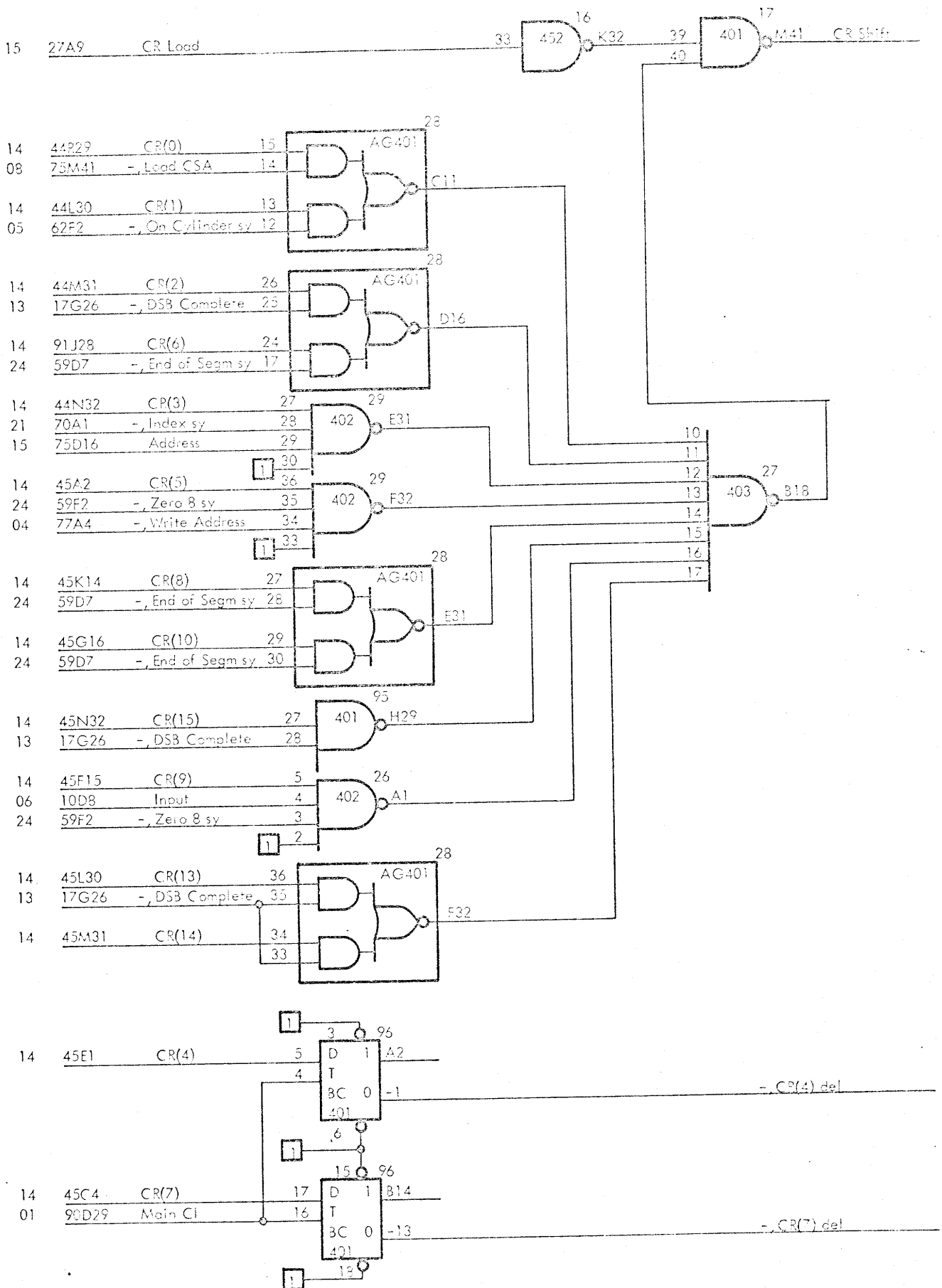
Logic Diagram

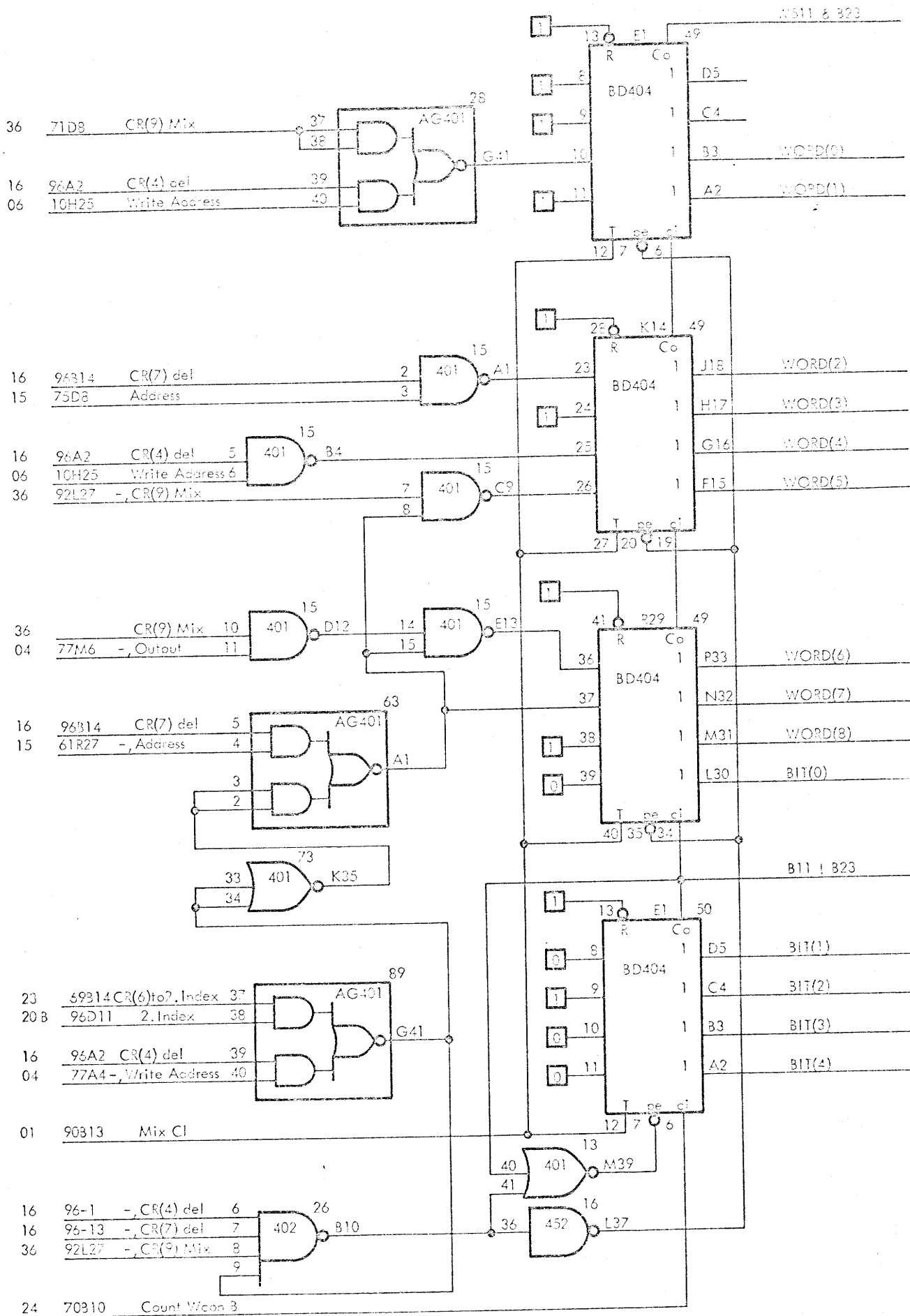
R 10540

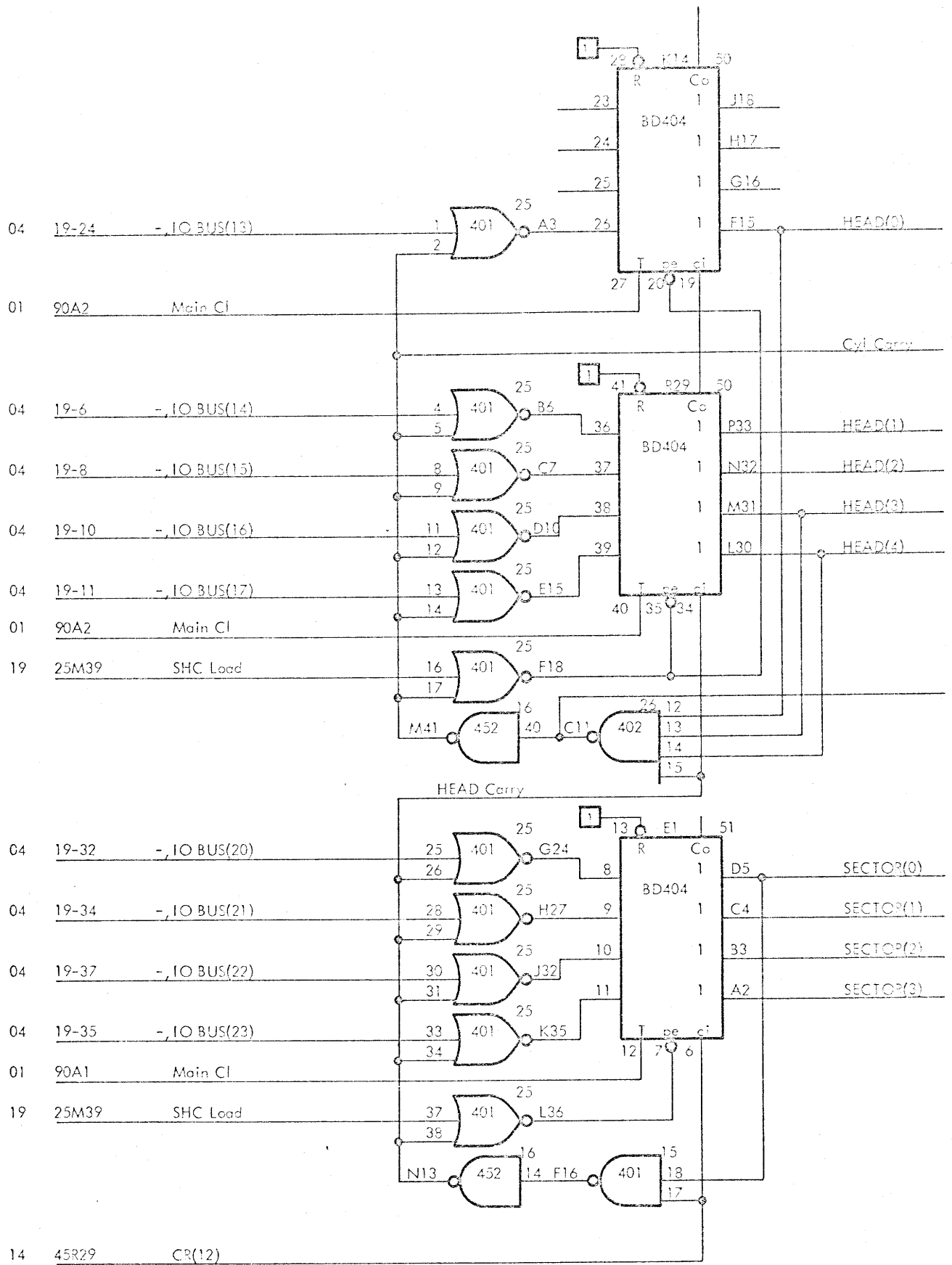


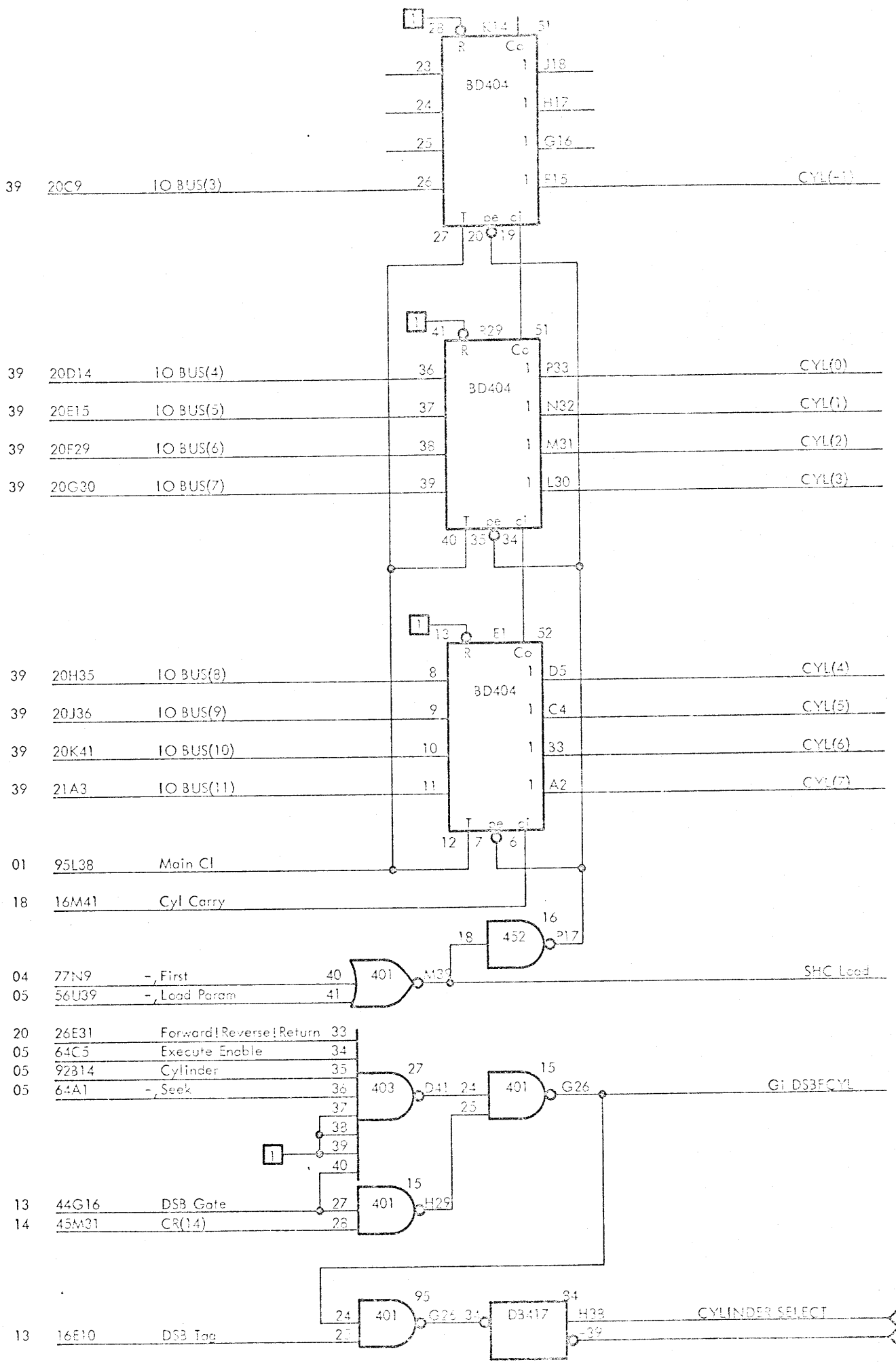








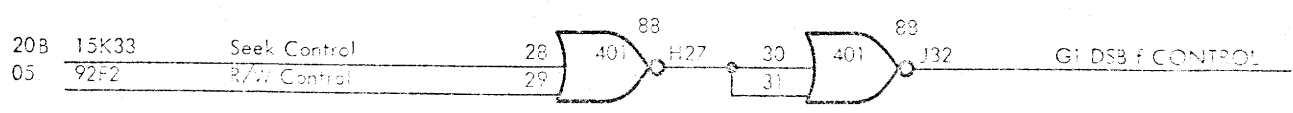
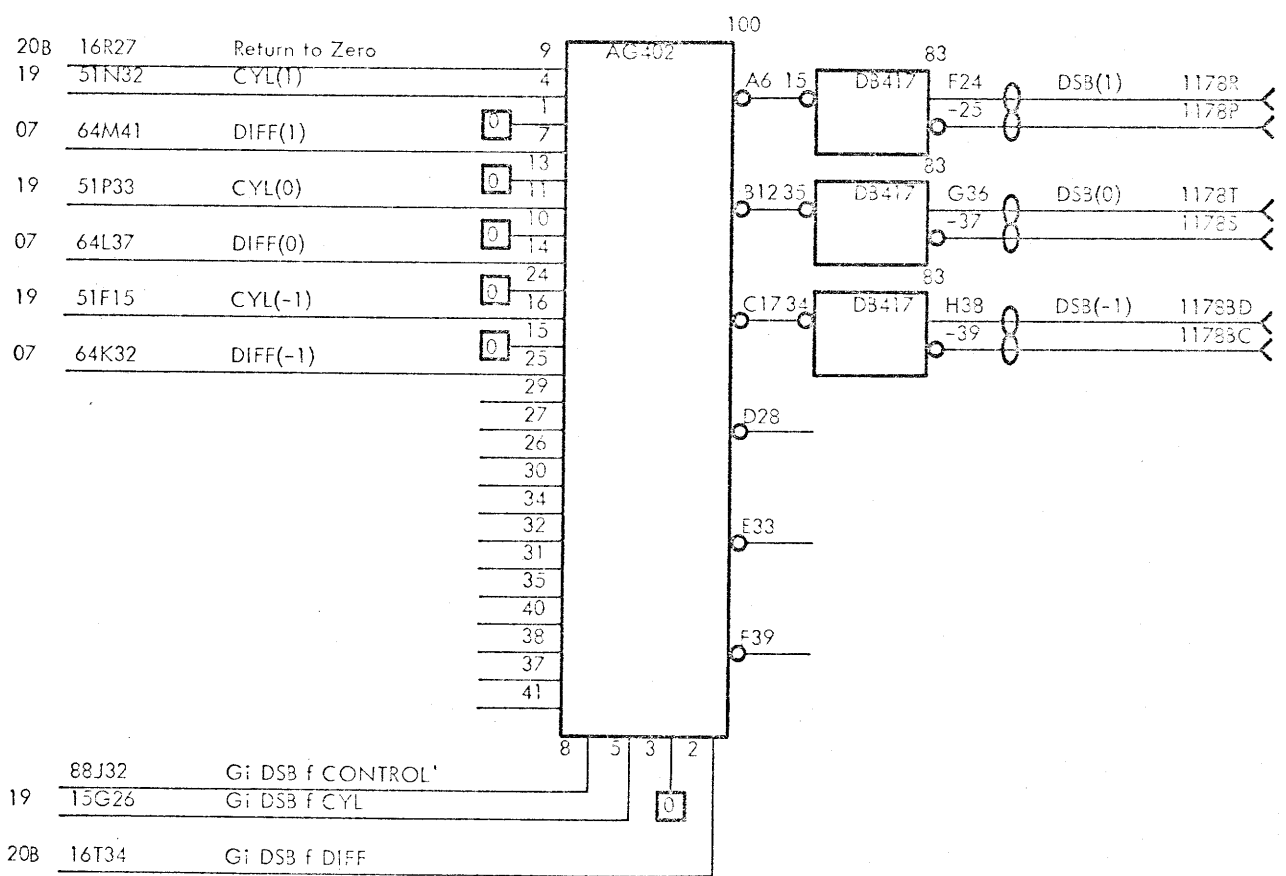
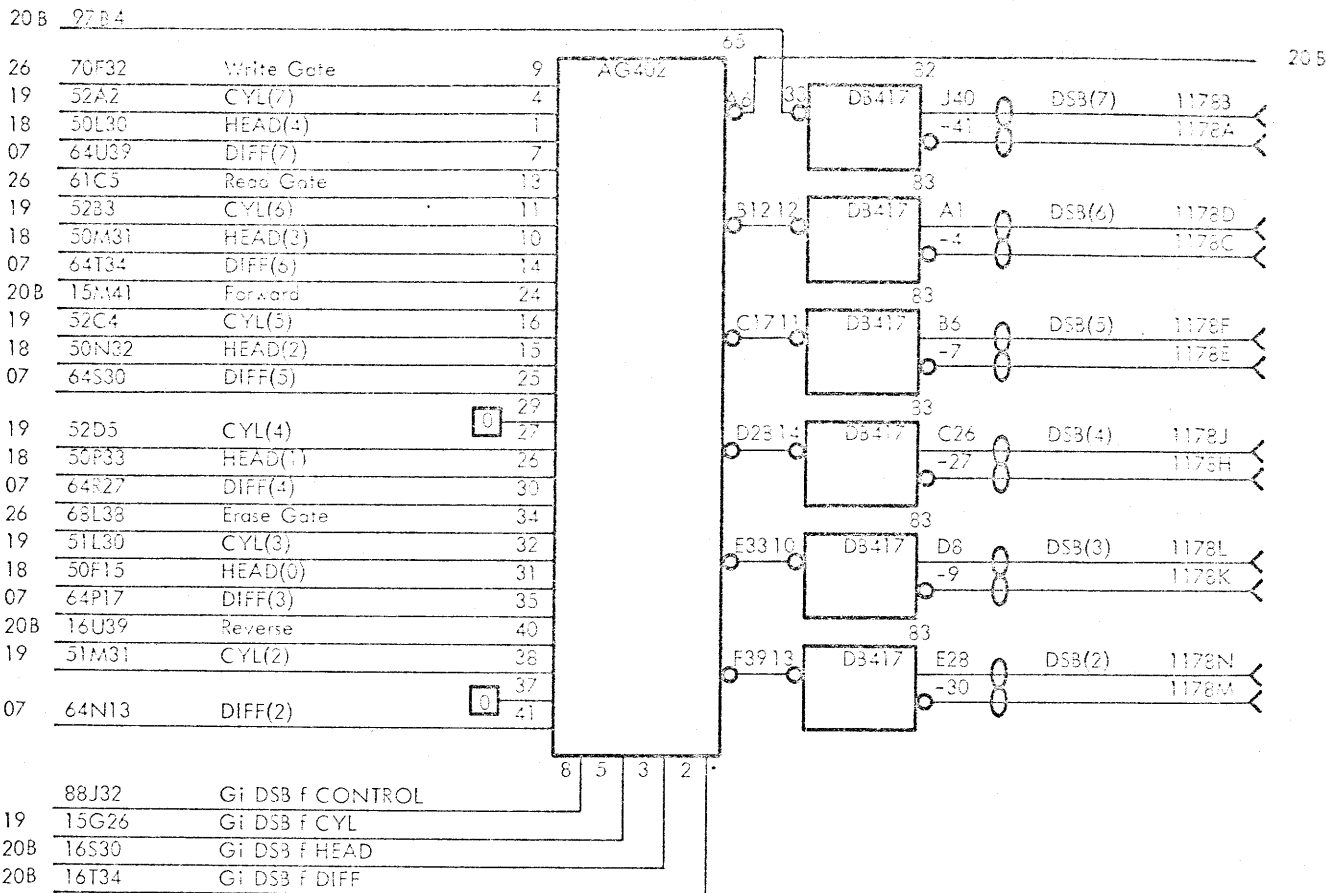


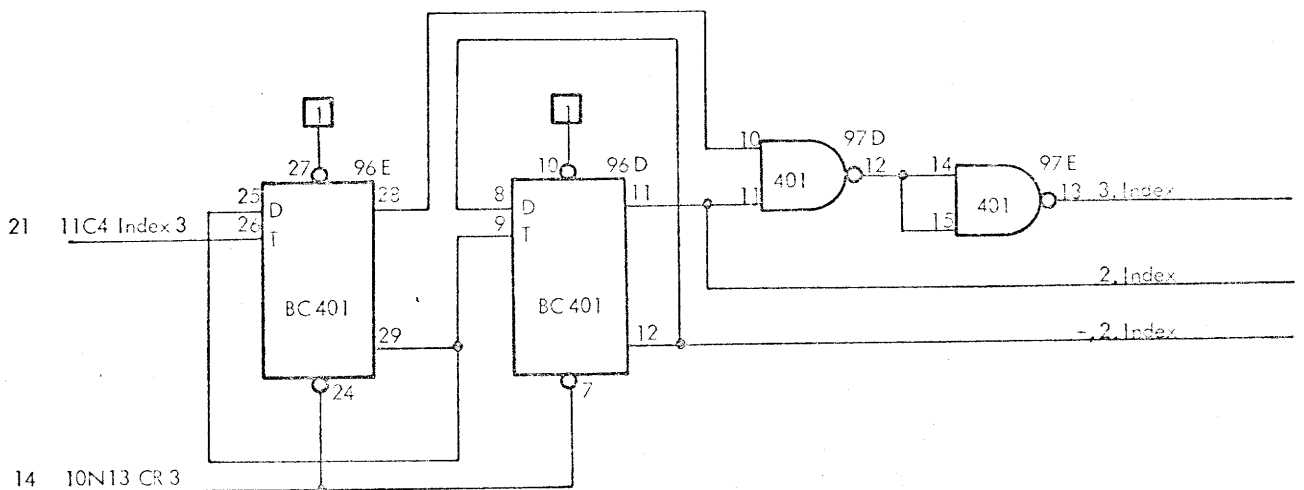
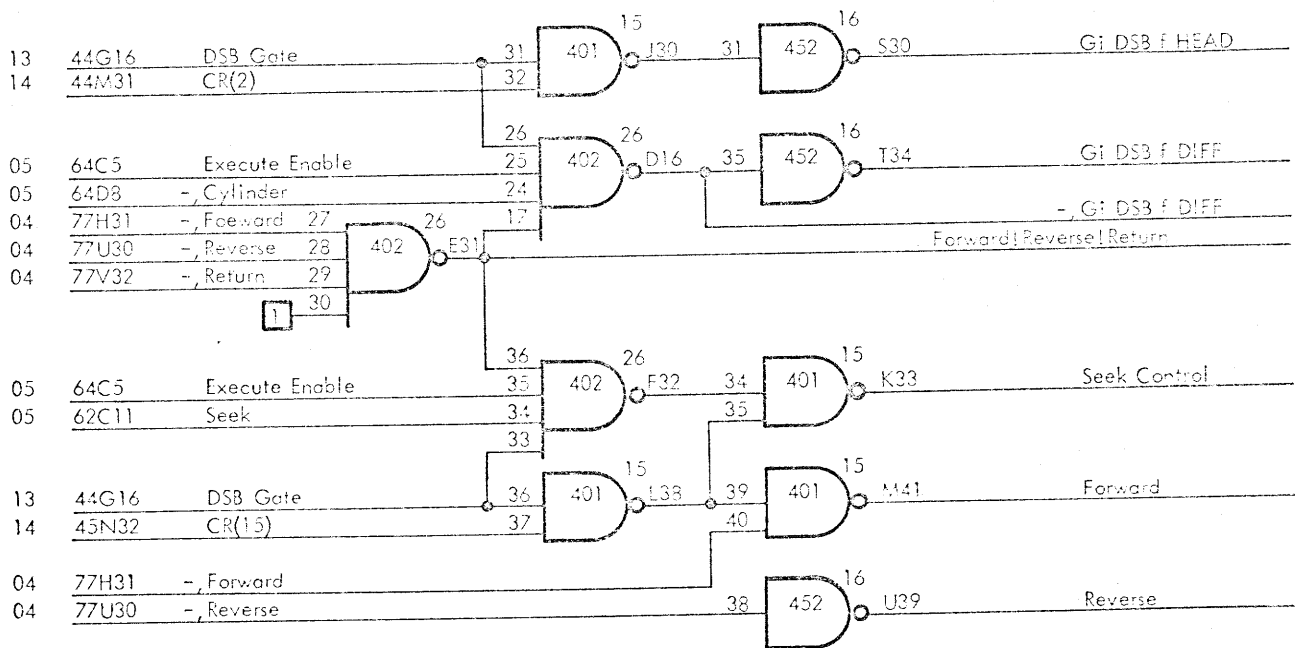
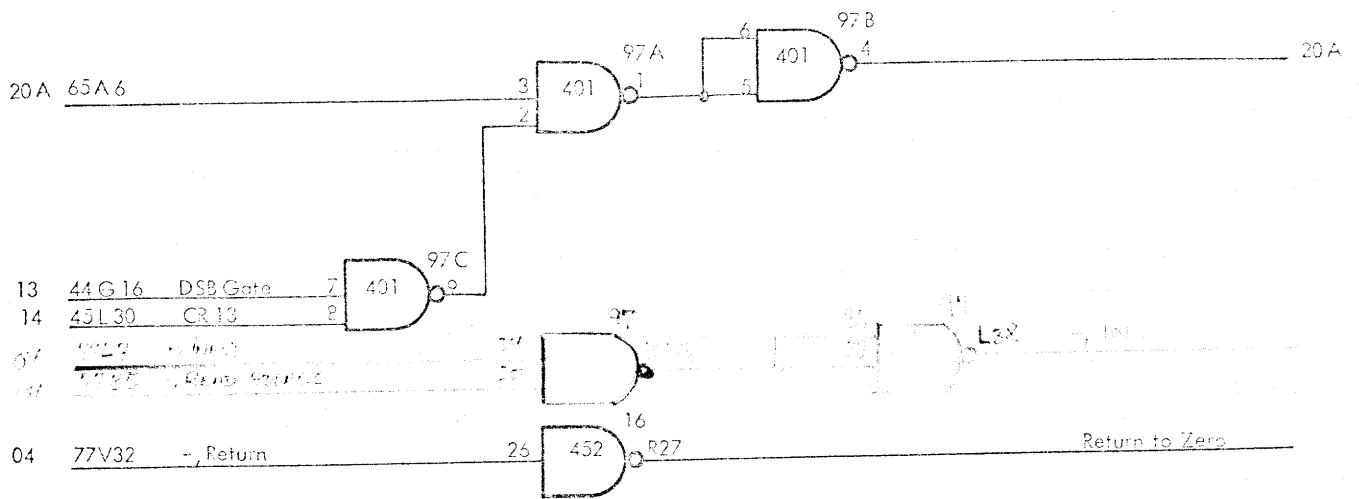


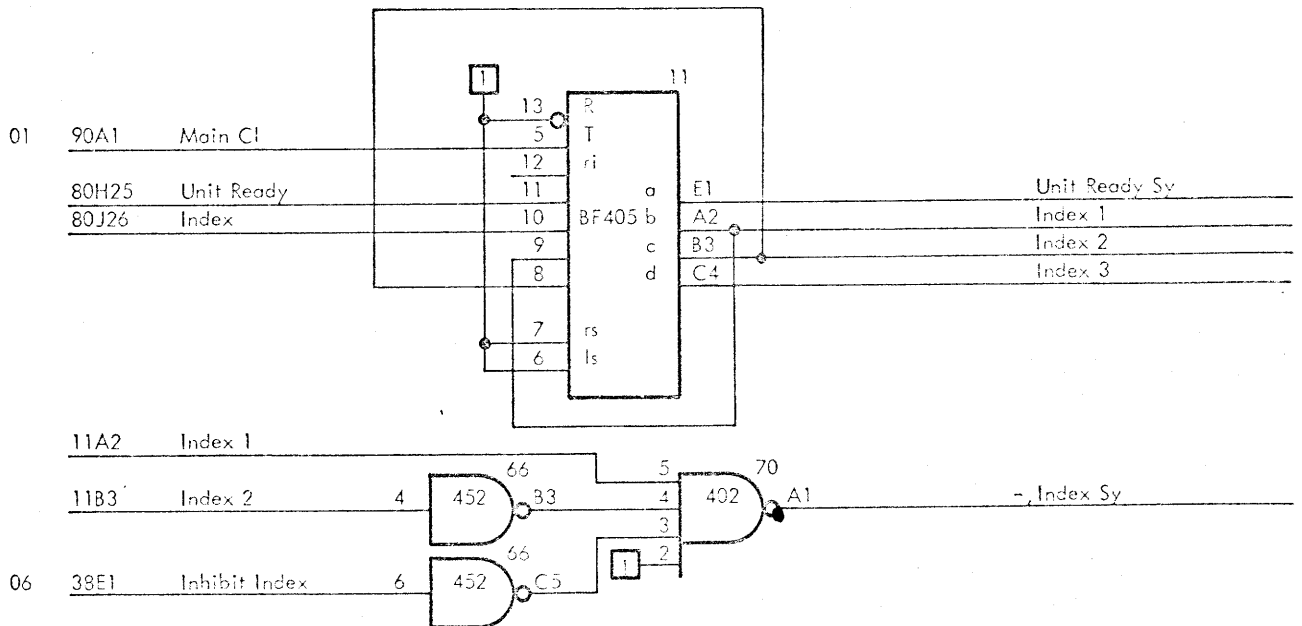
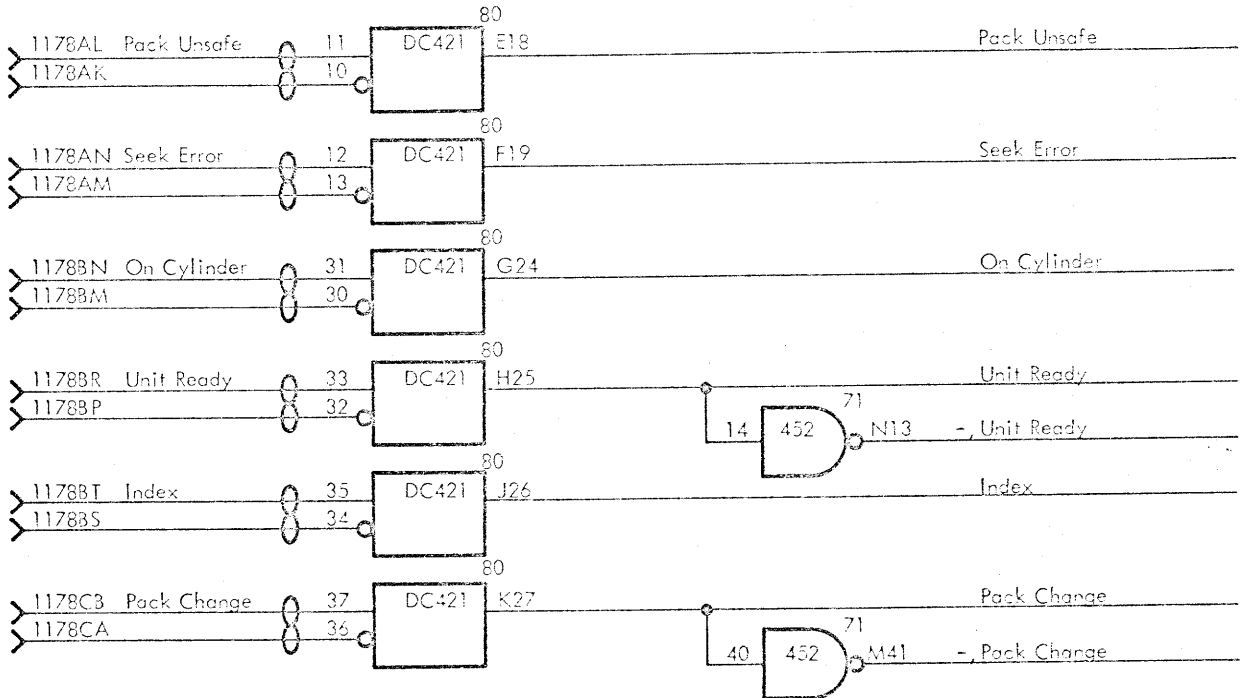
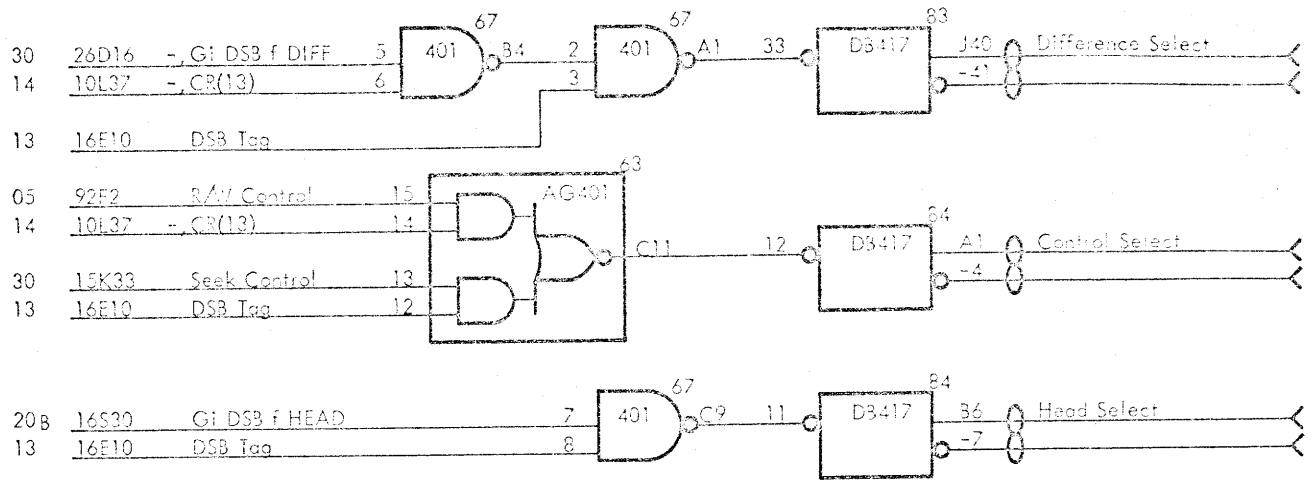
DFC 403
RC4000

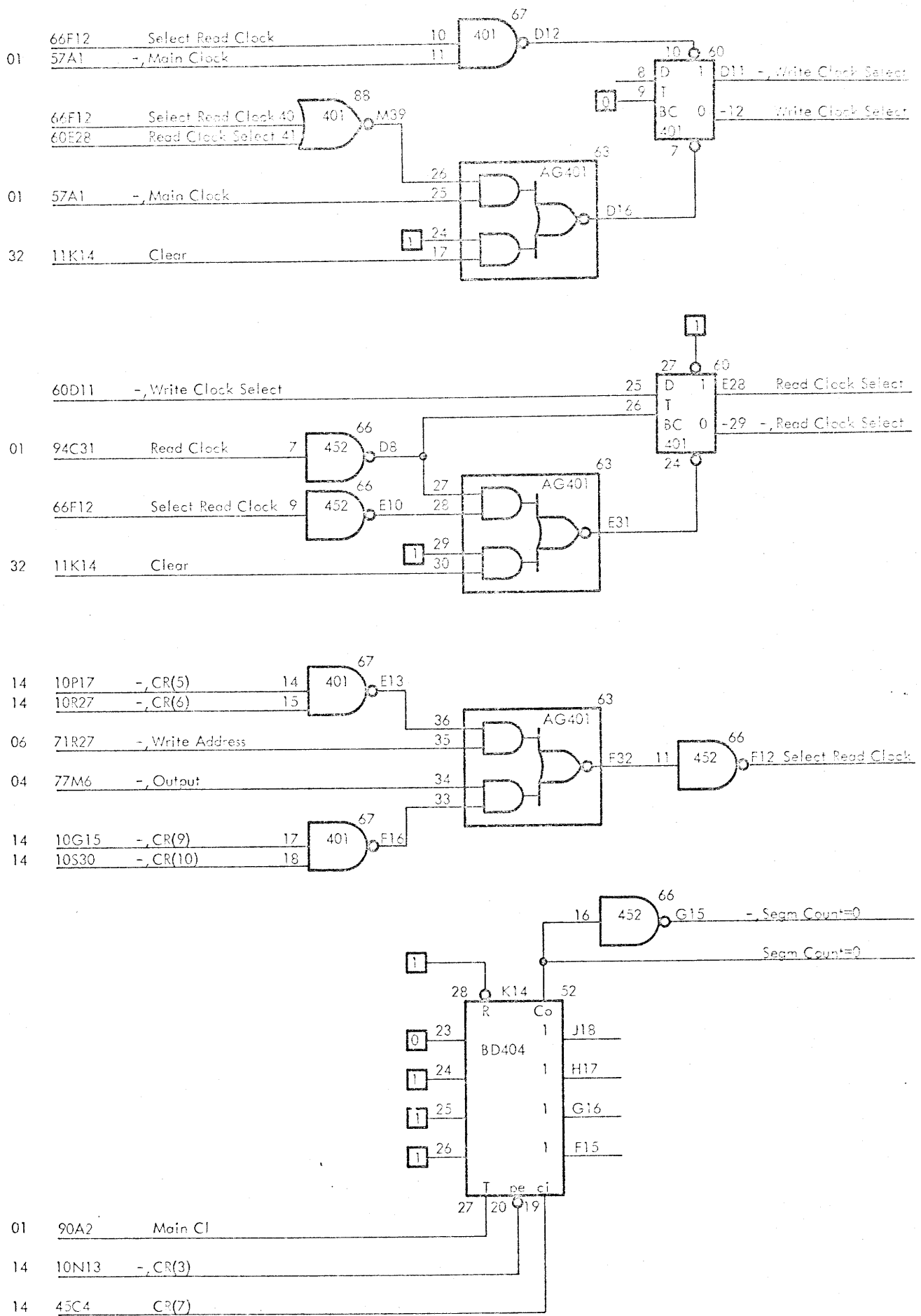
CYLINDER COUNTER, CYL(-1:7)

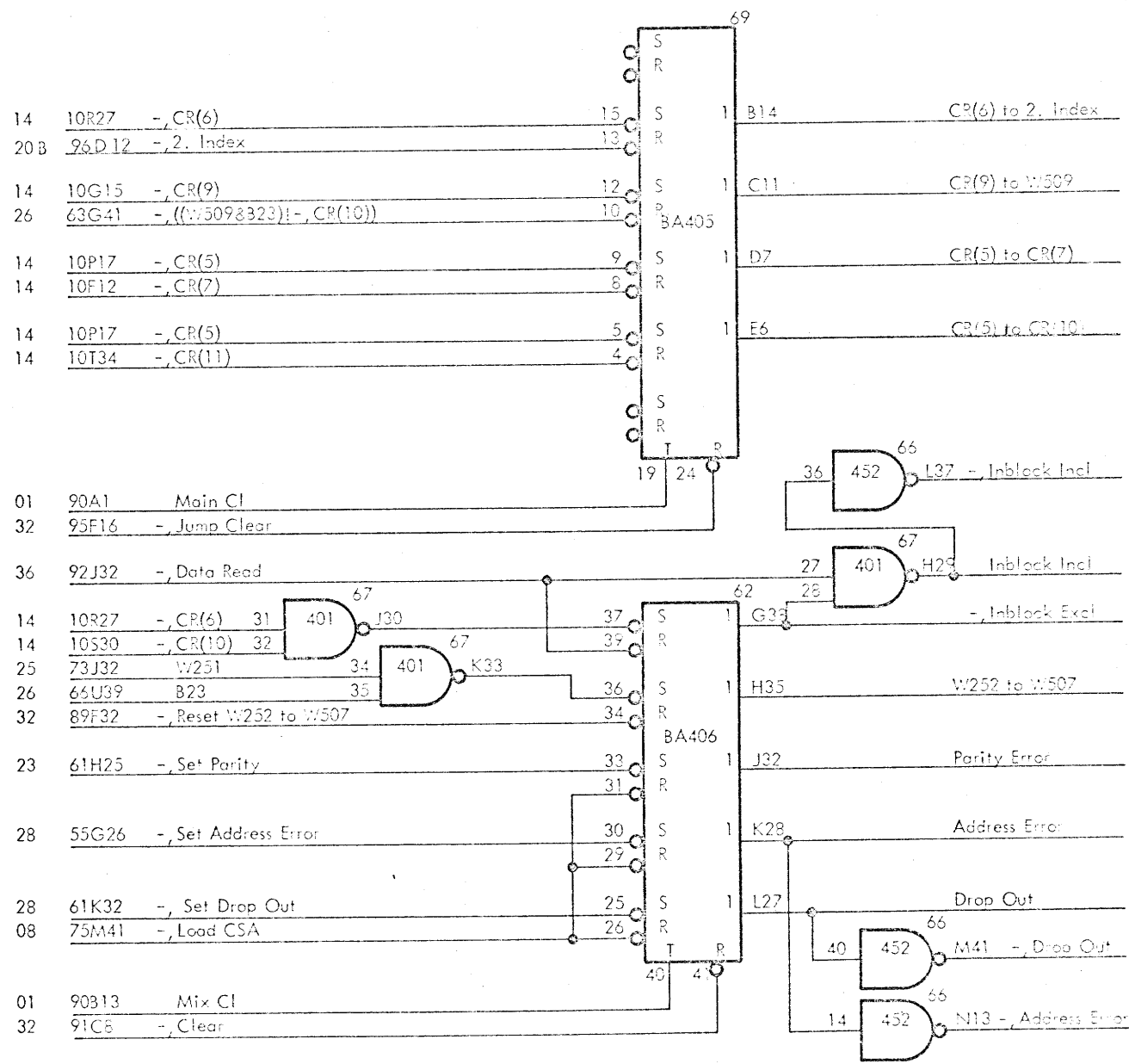
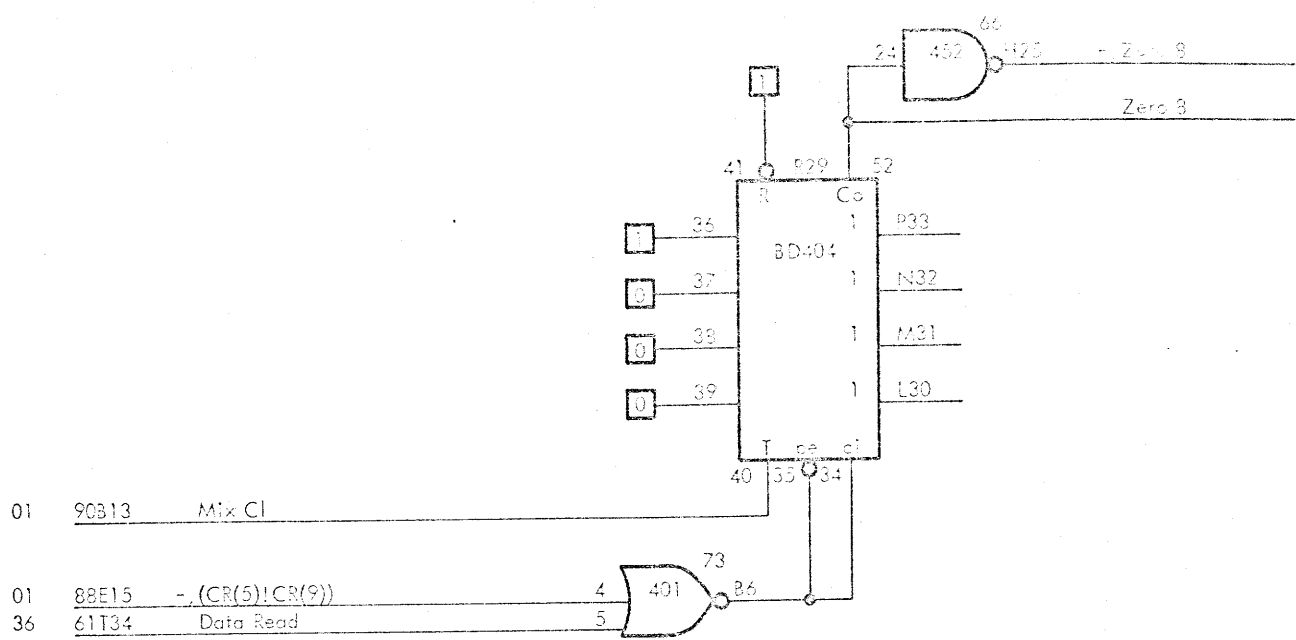
DFC19

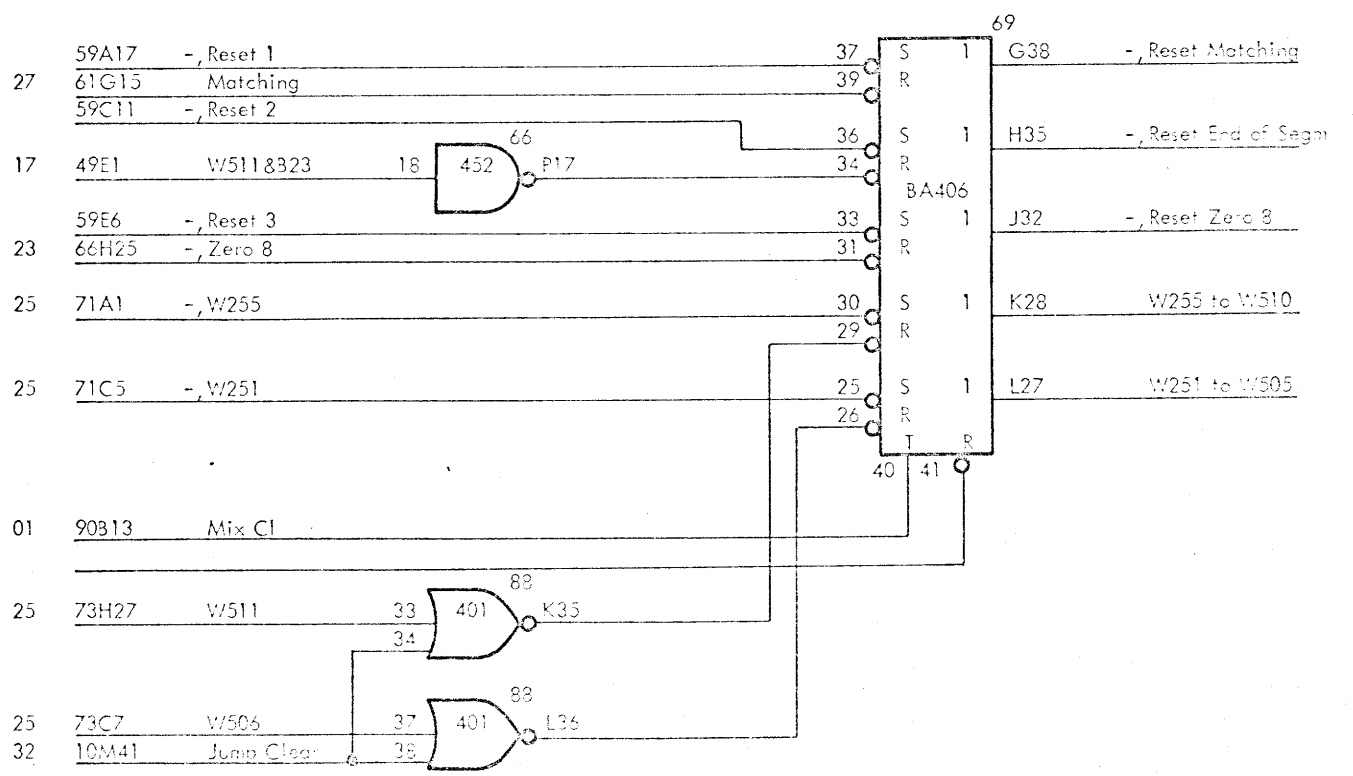
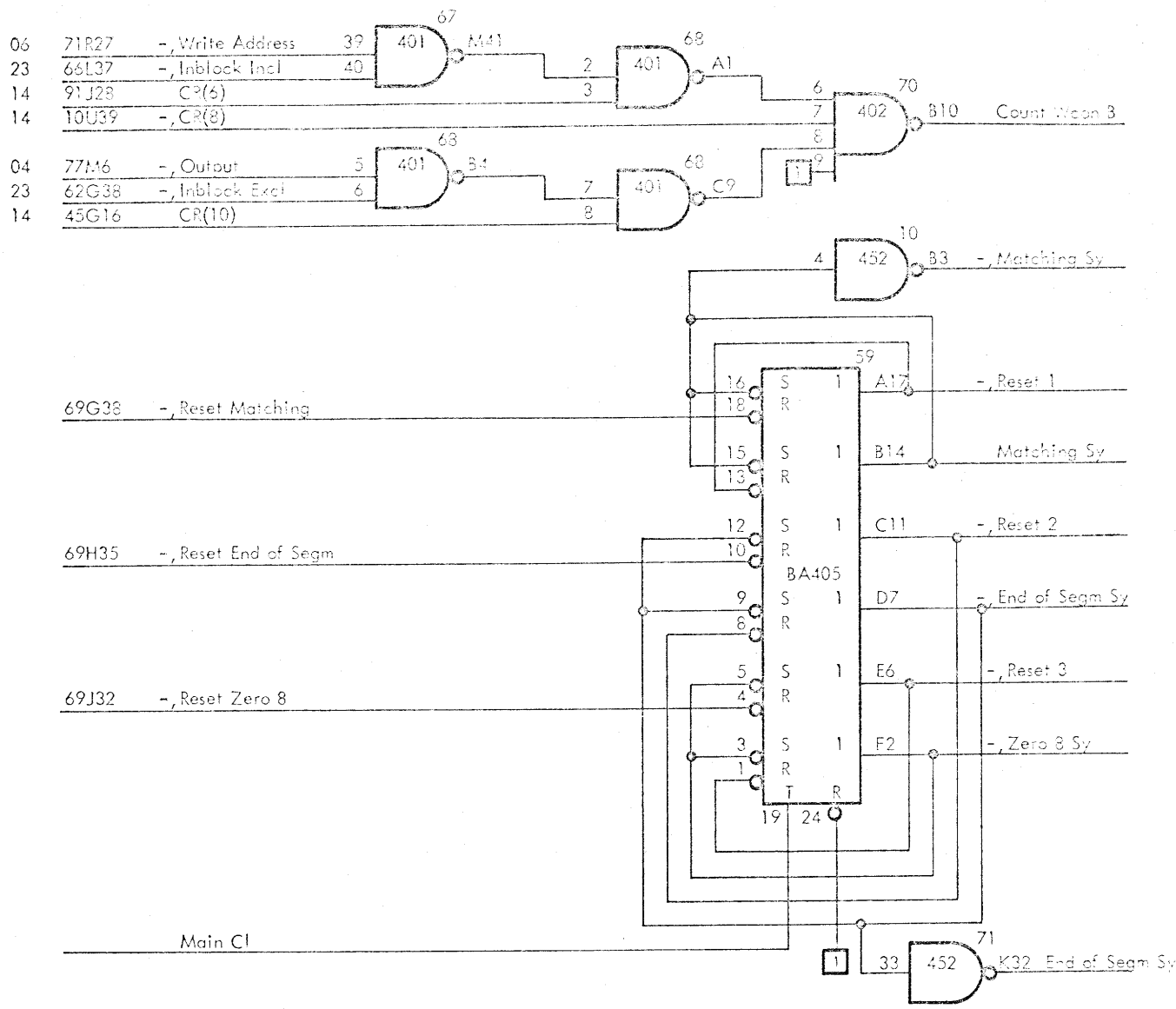










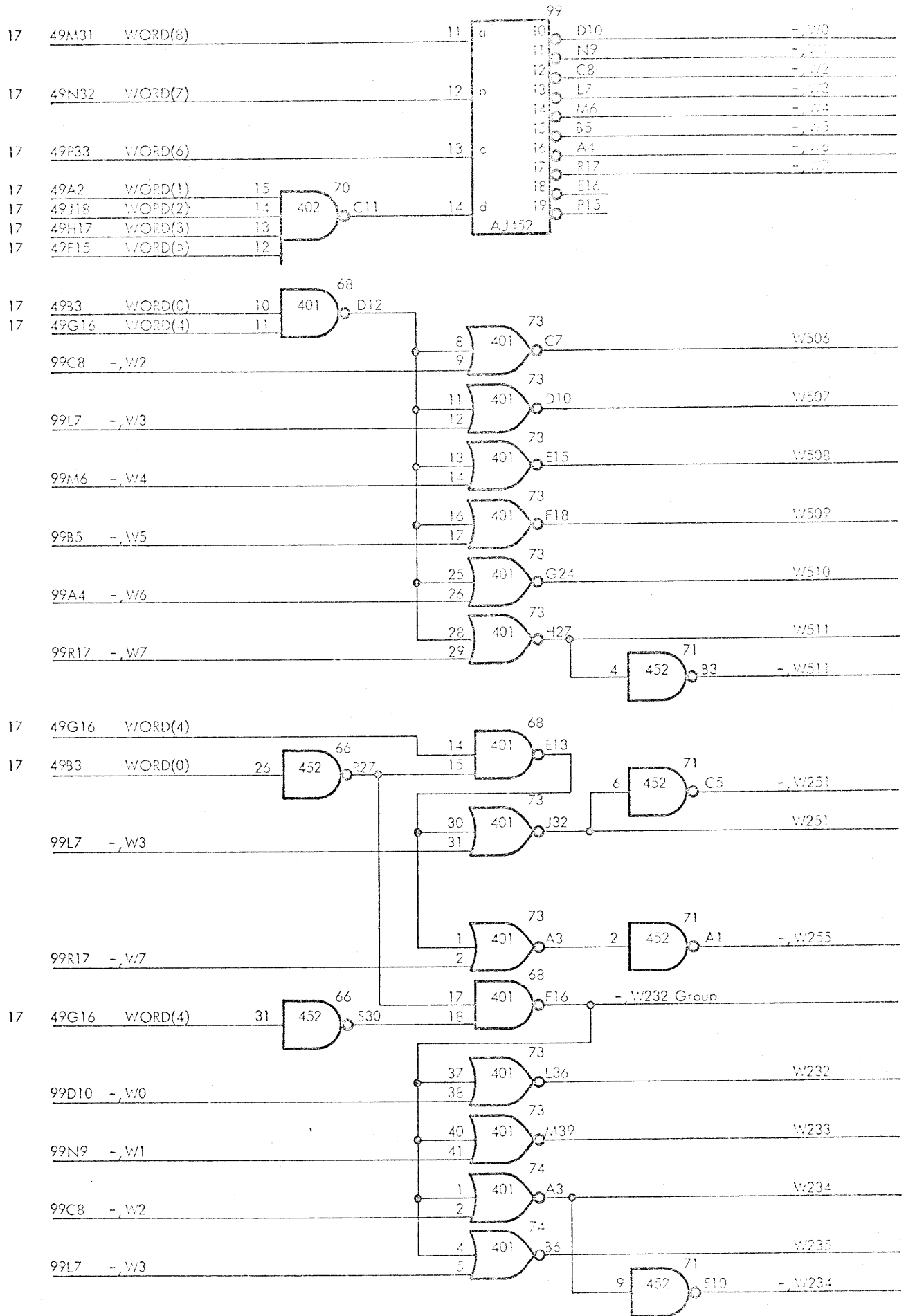


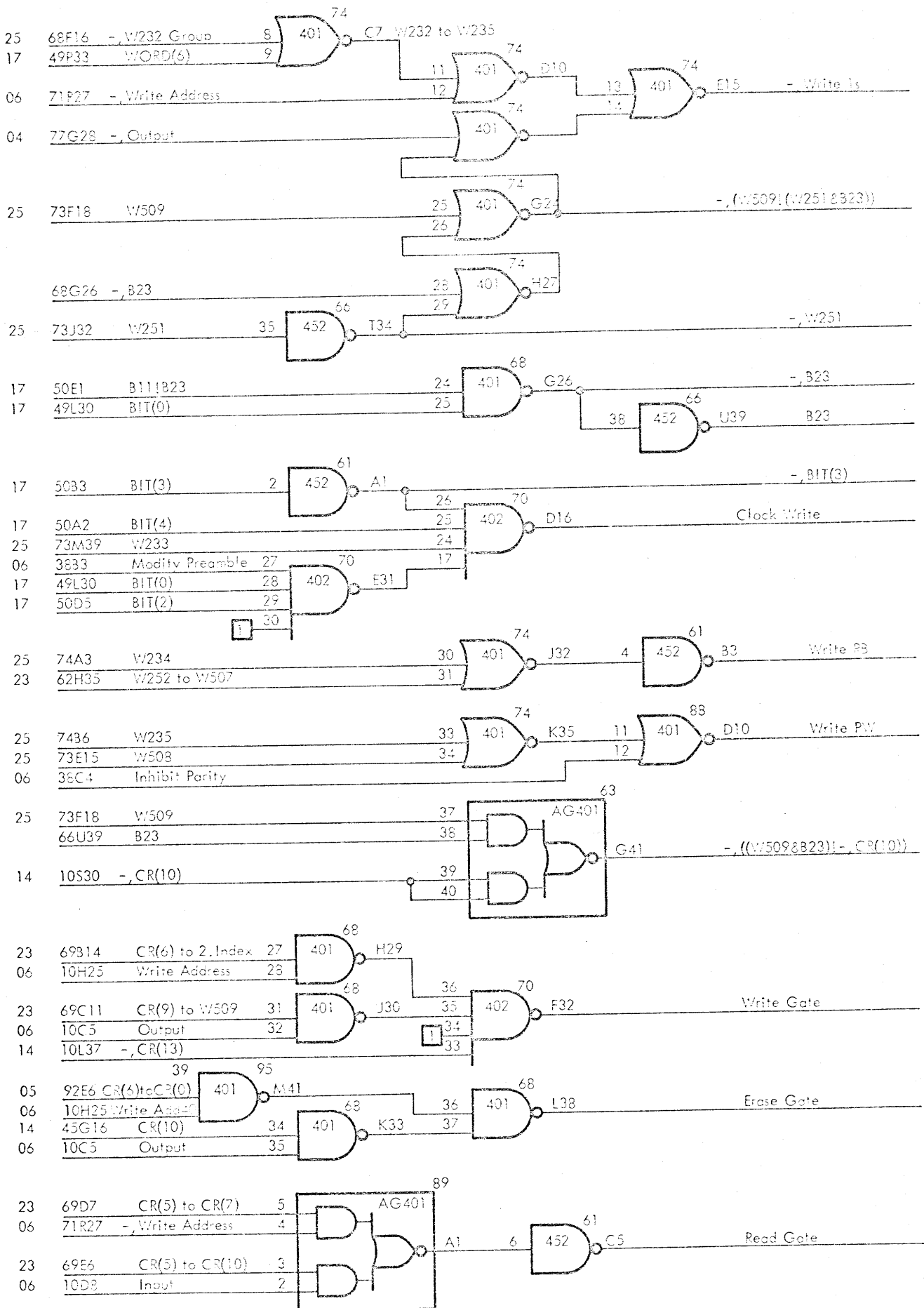
DFC 403
RC 4000
R 10553

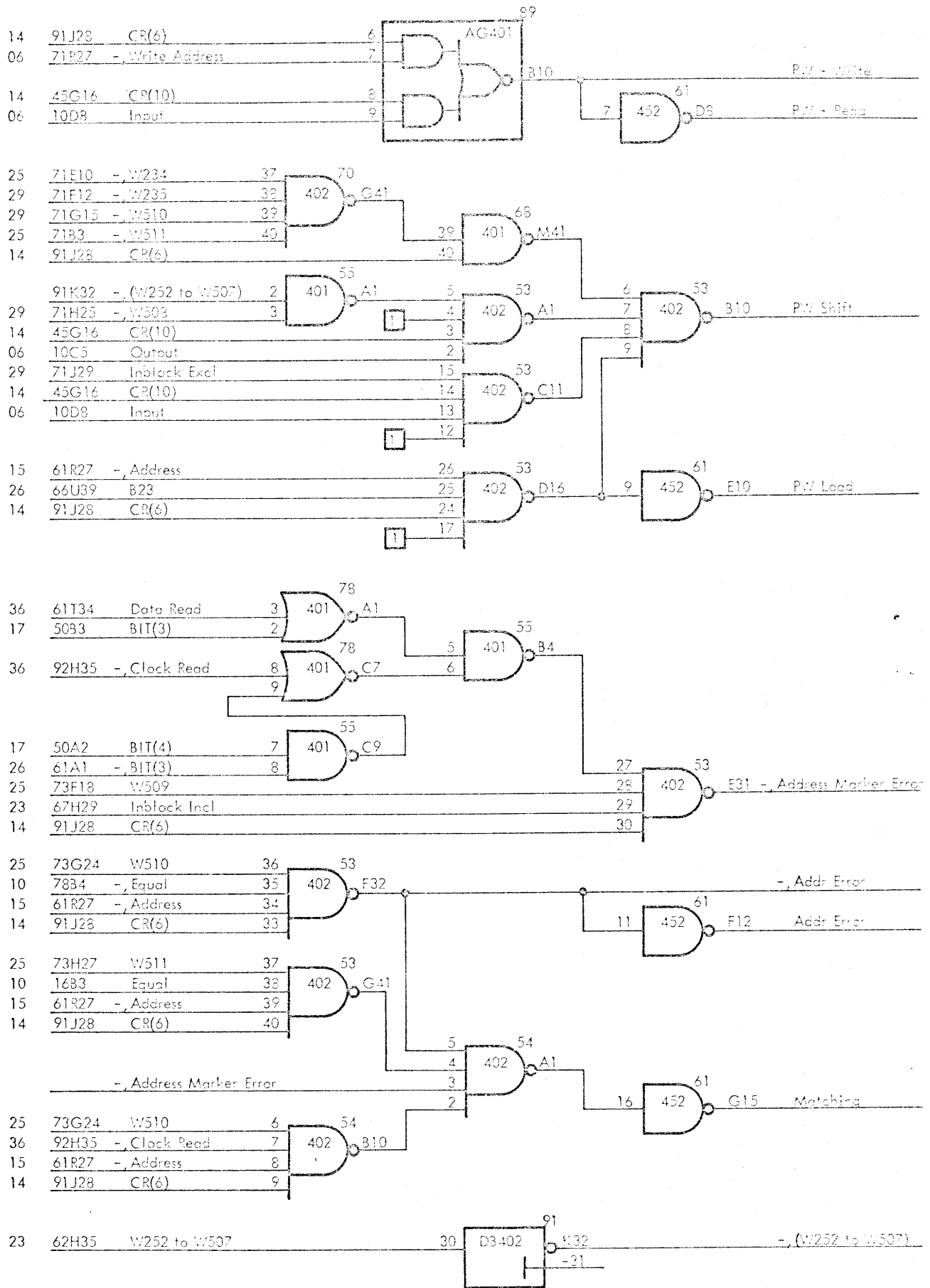
MIX CL TO MAIN CL SYNCHRONISING CIRCUIT

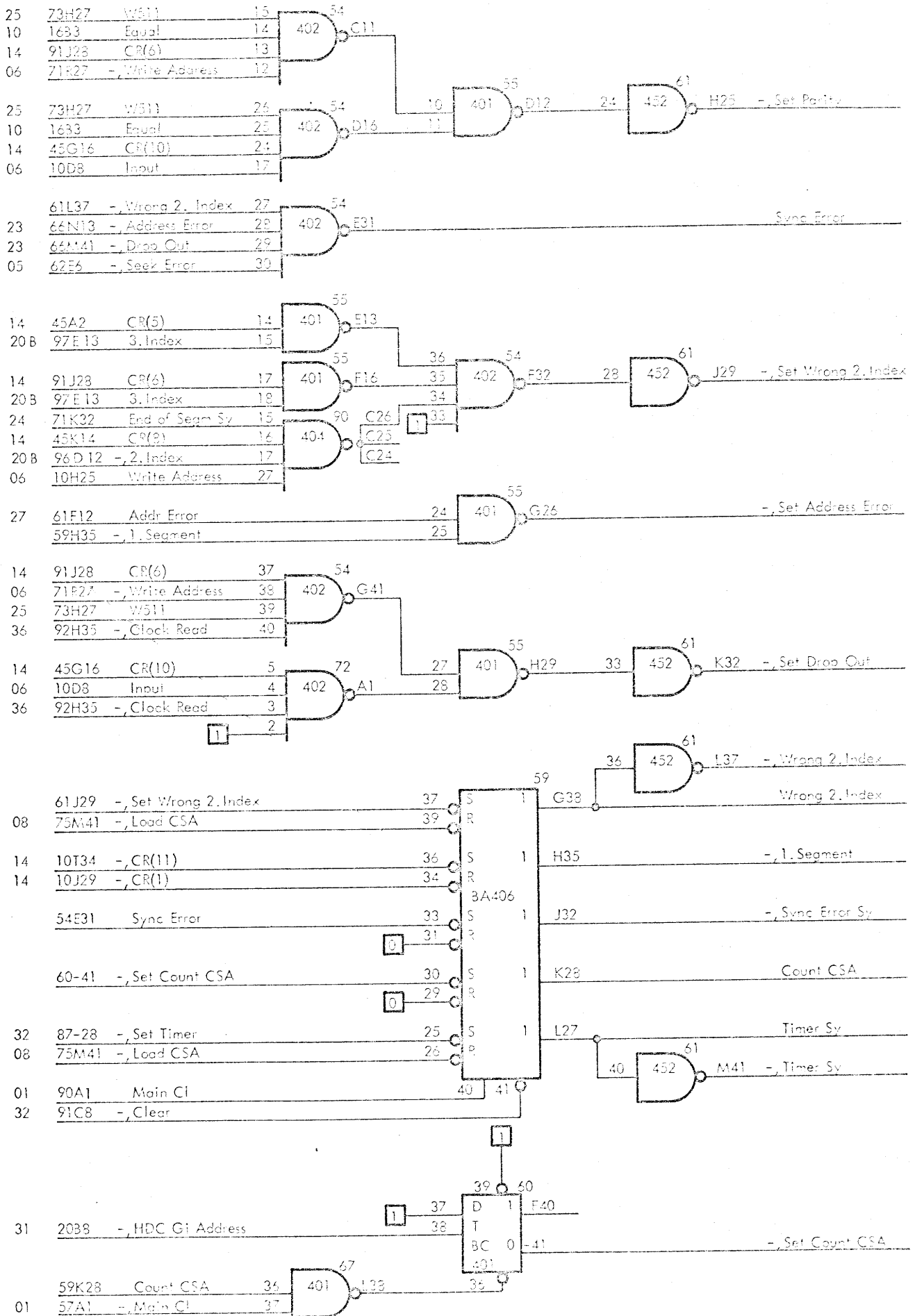
DFC 24

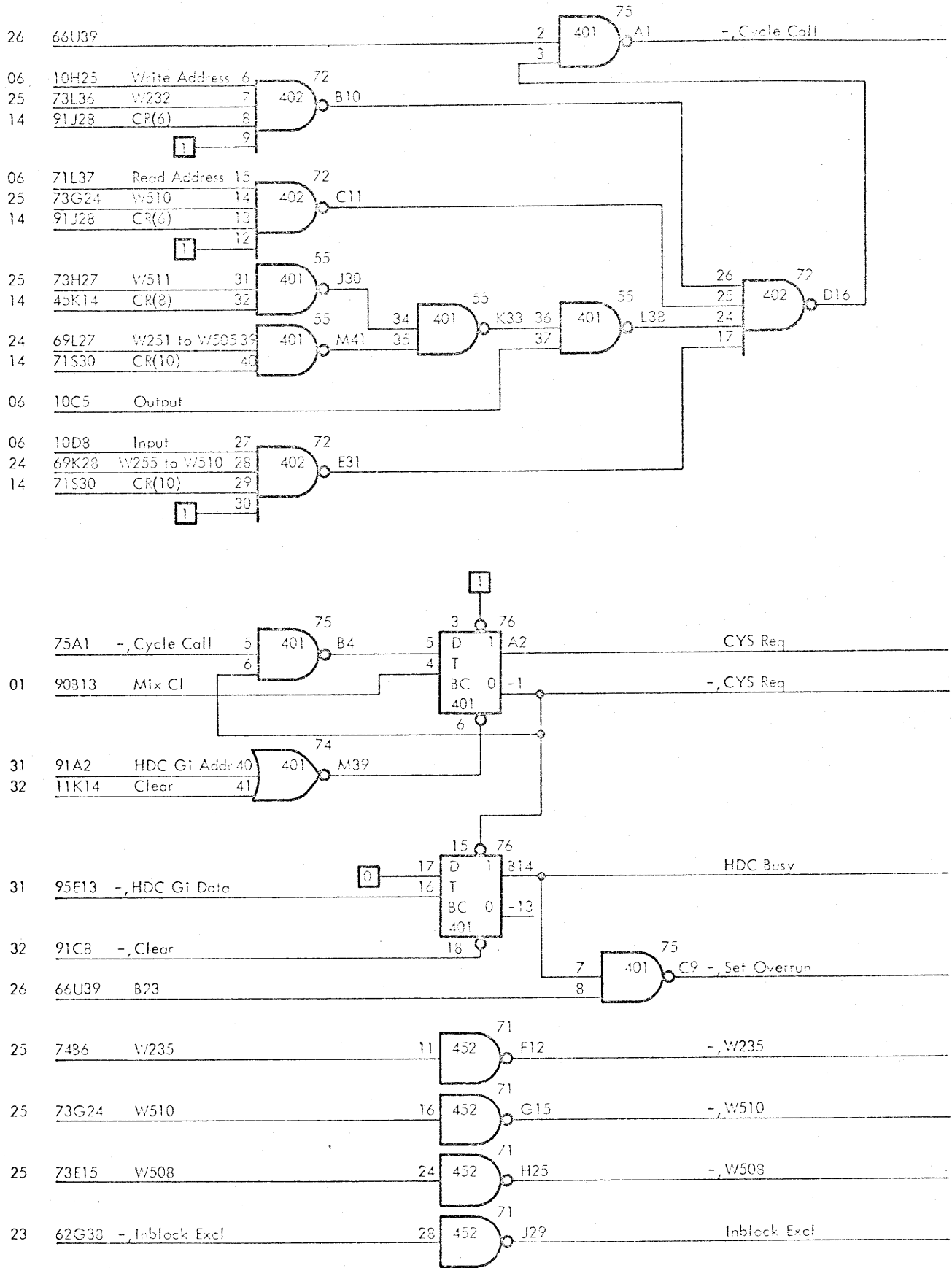
Logic Diagram

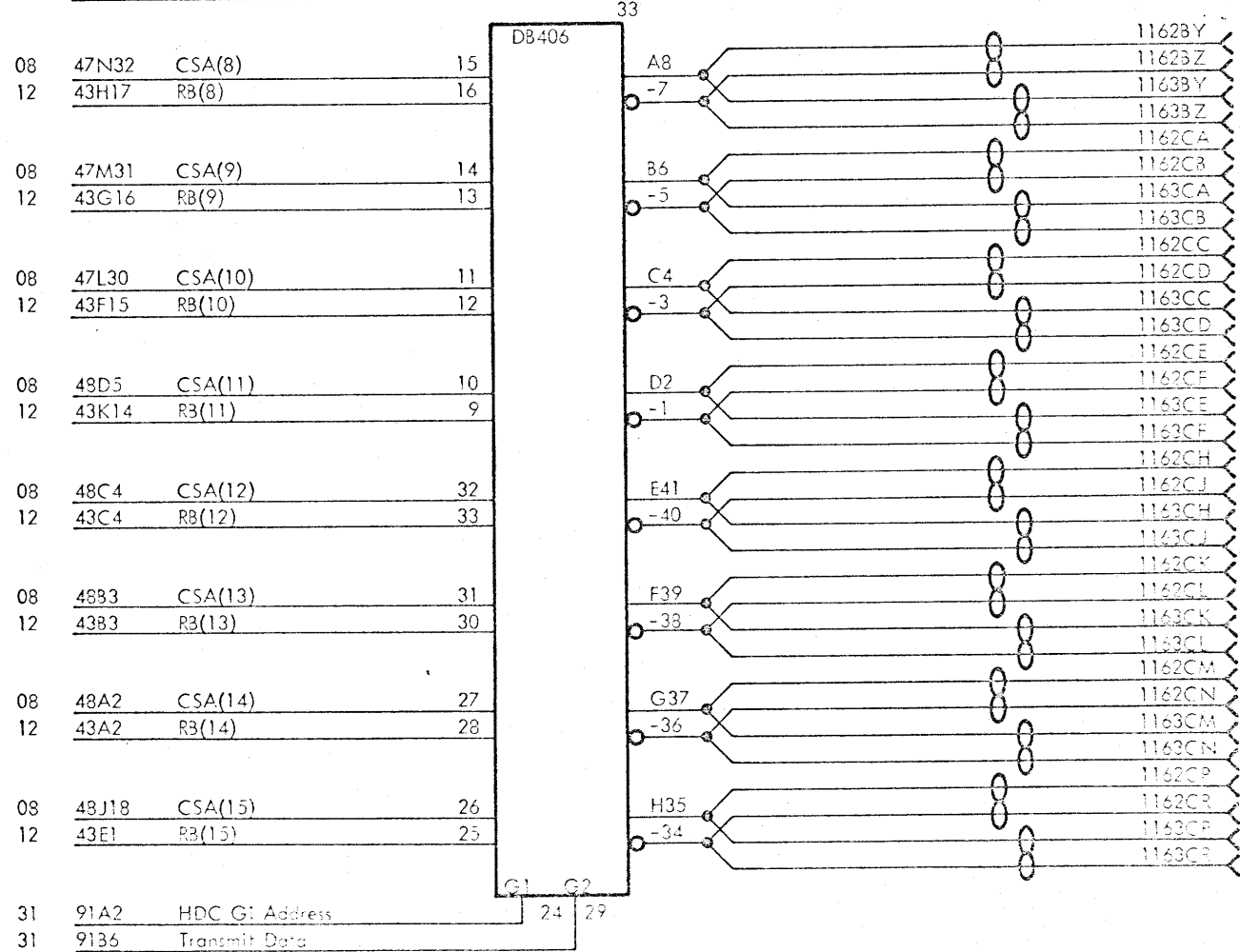
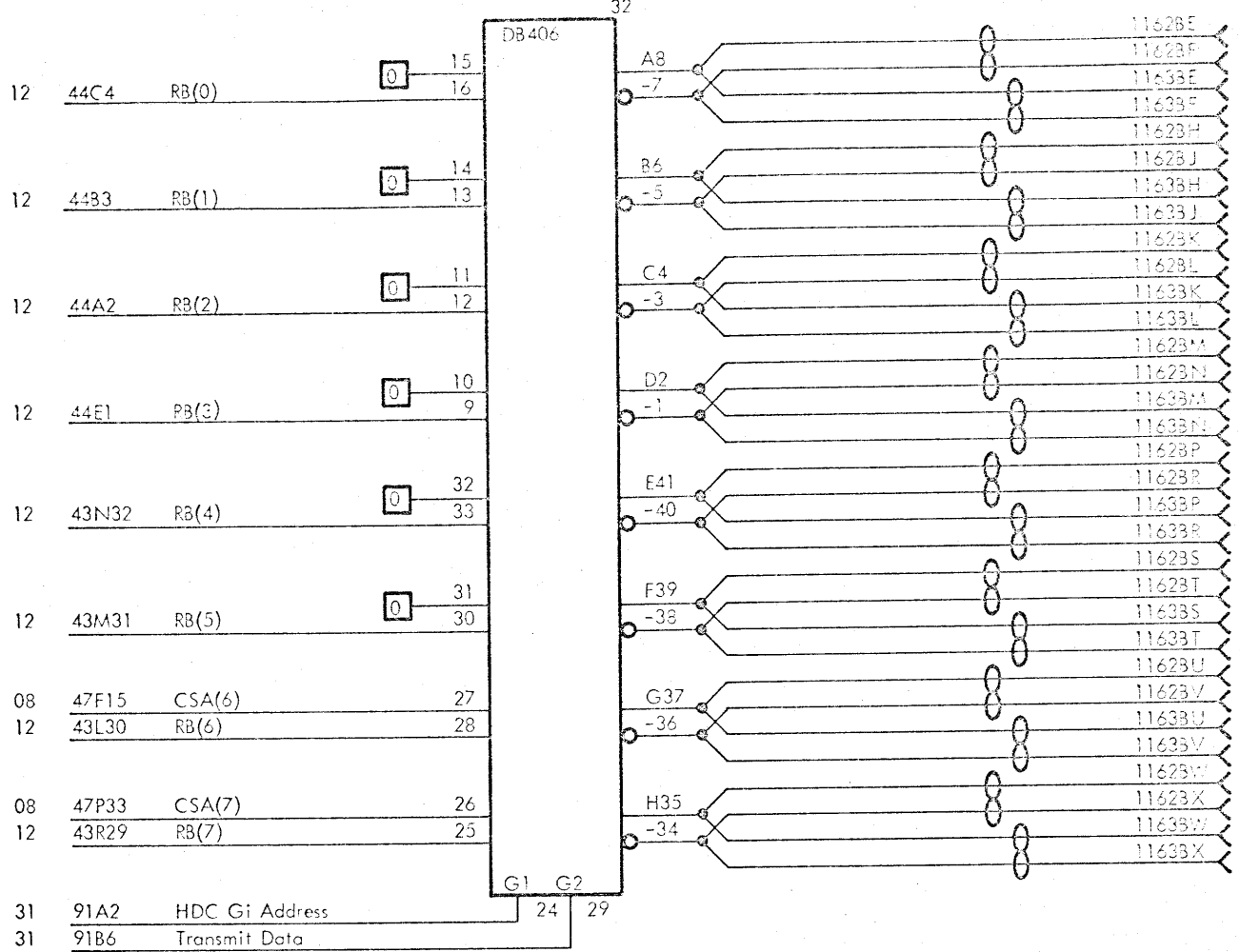


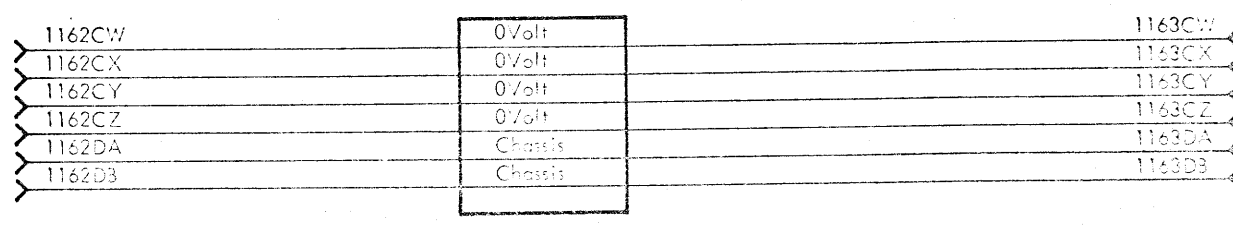
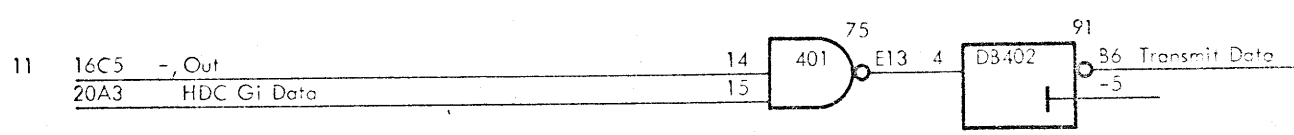
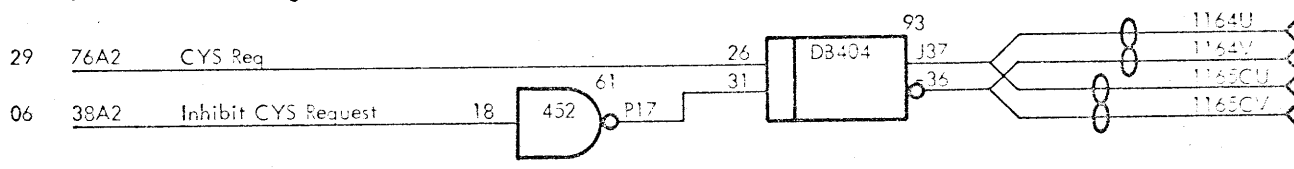
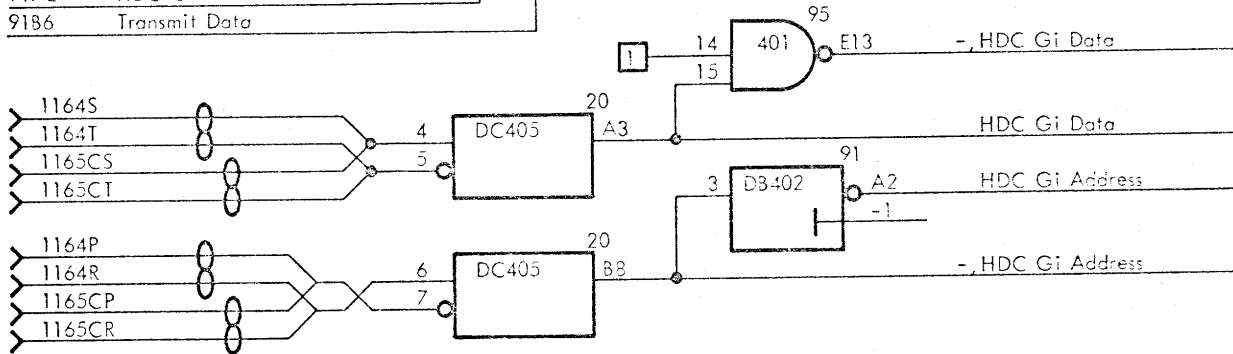
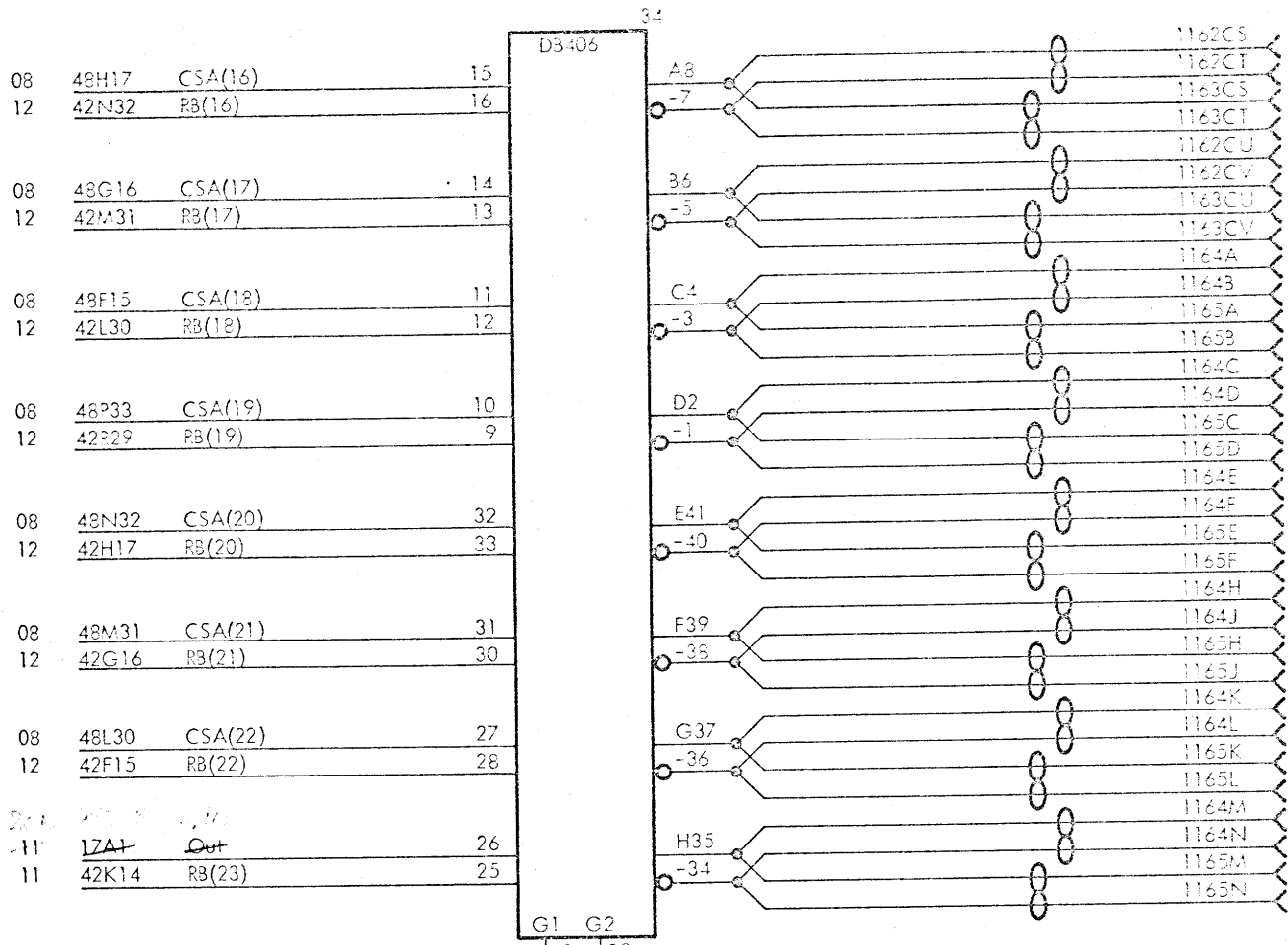


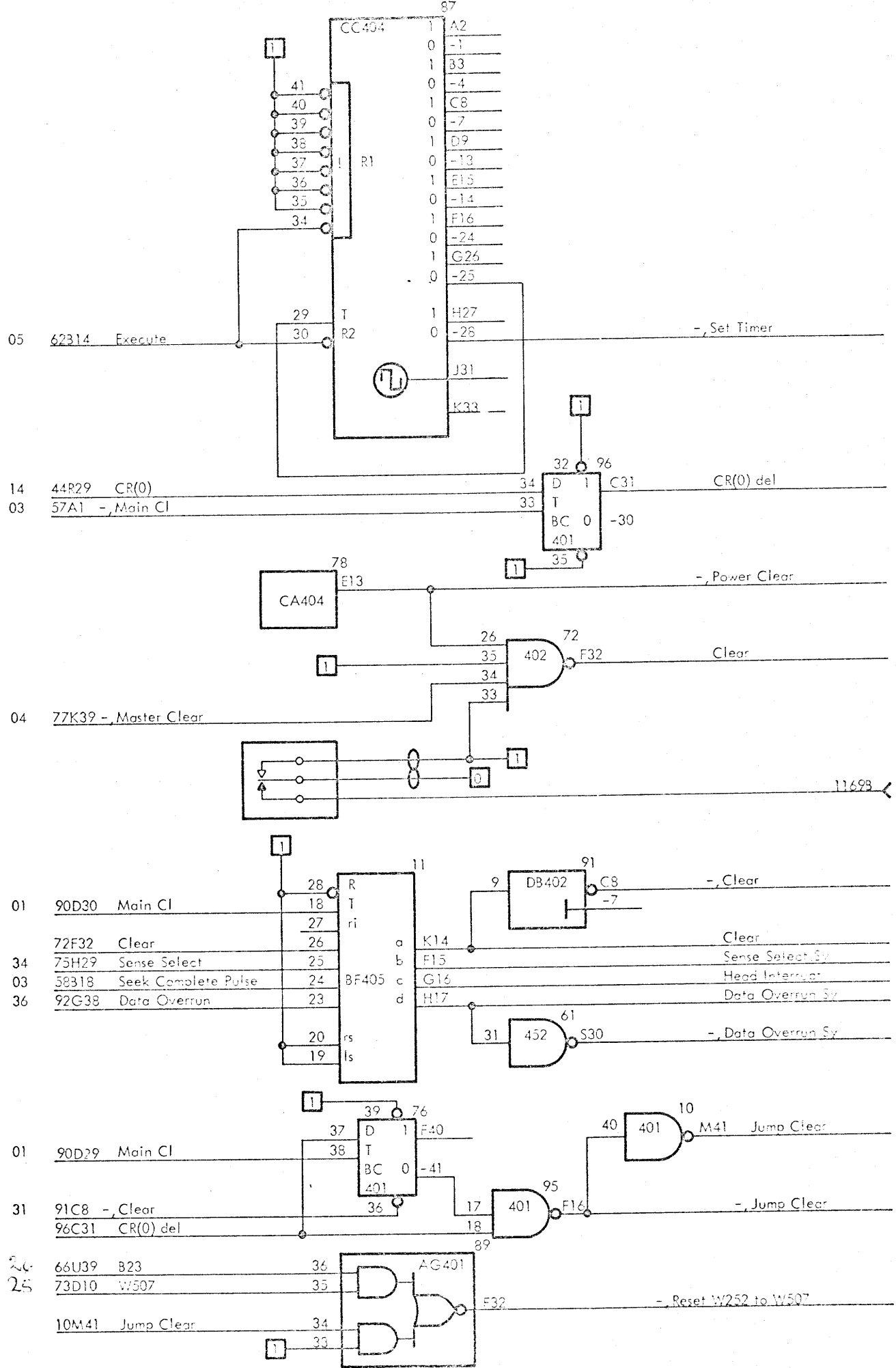


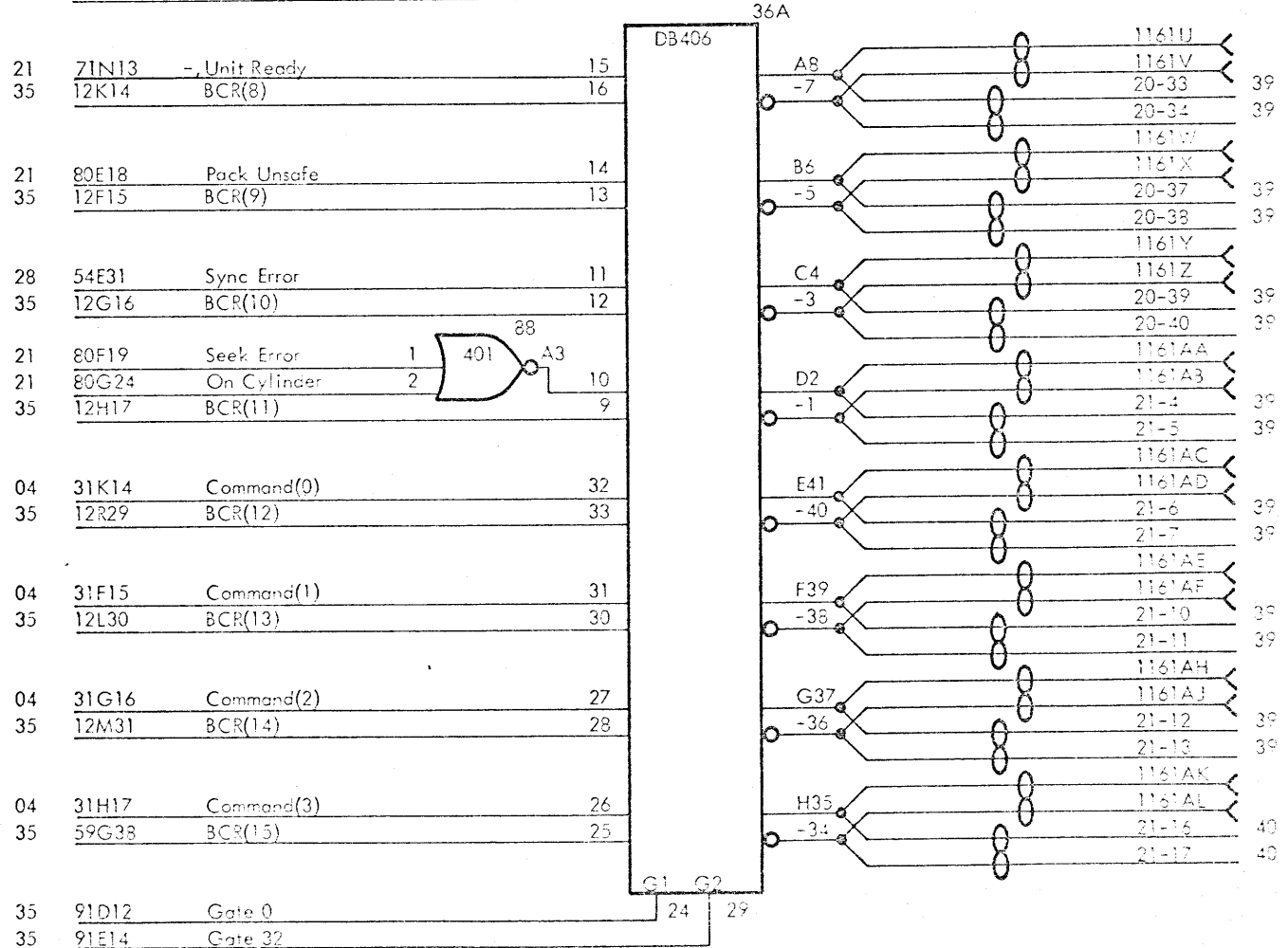
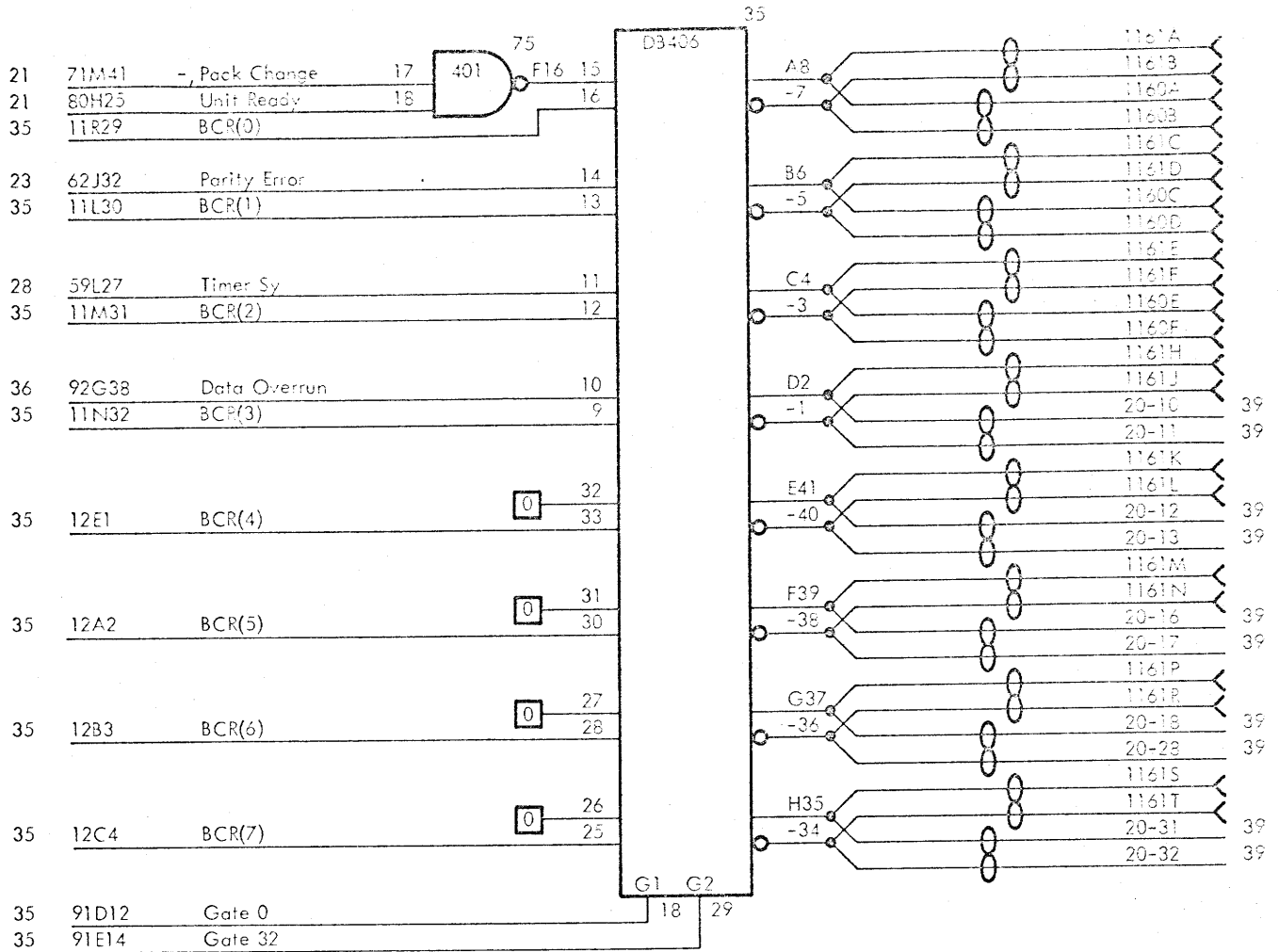


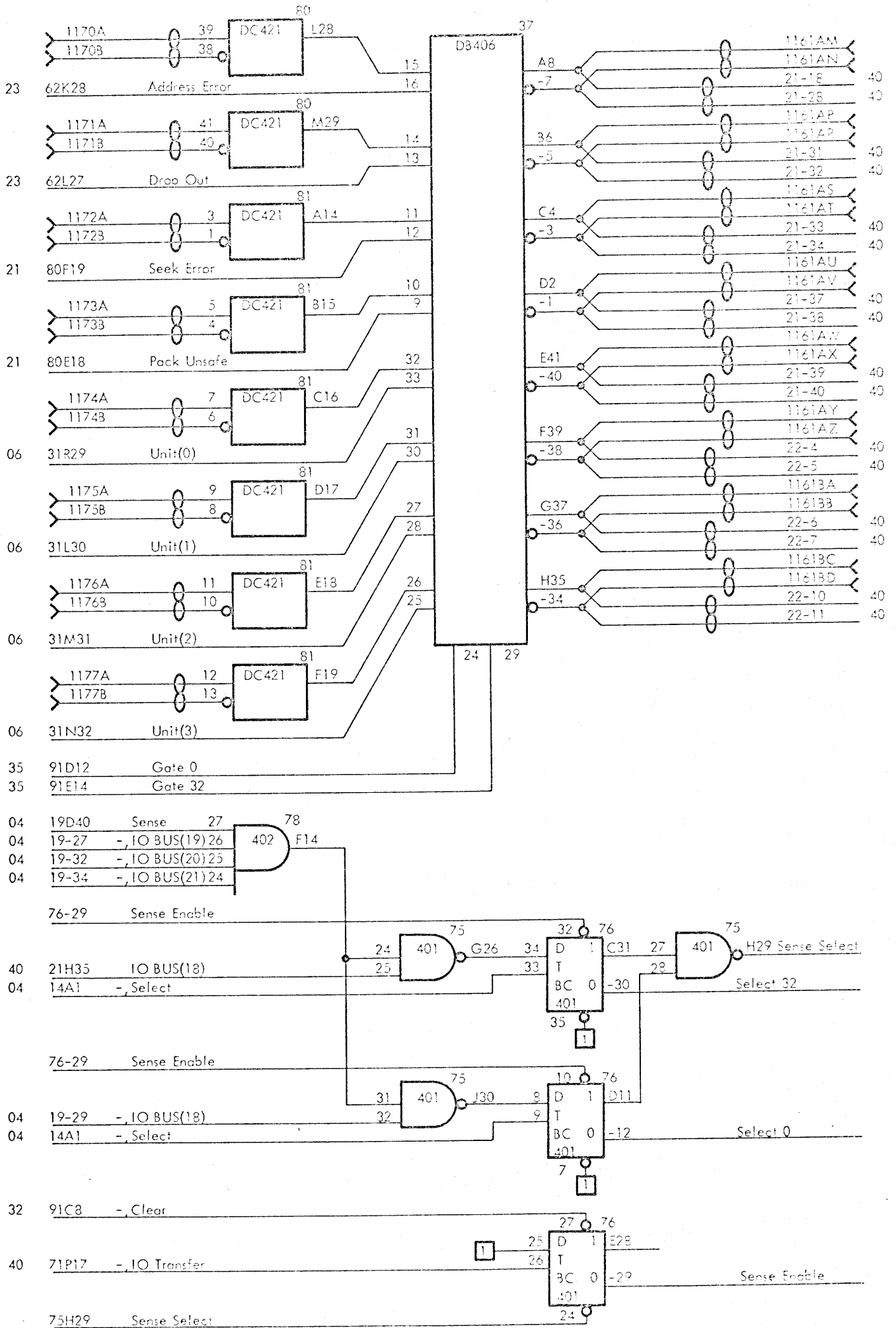


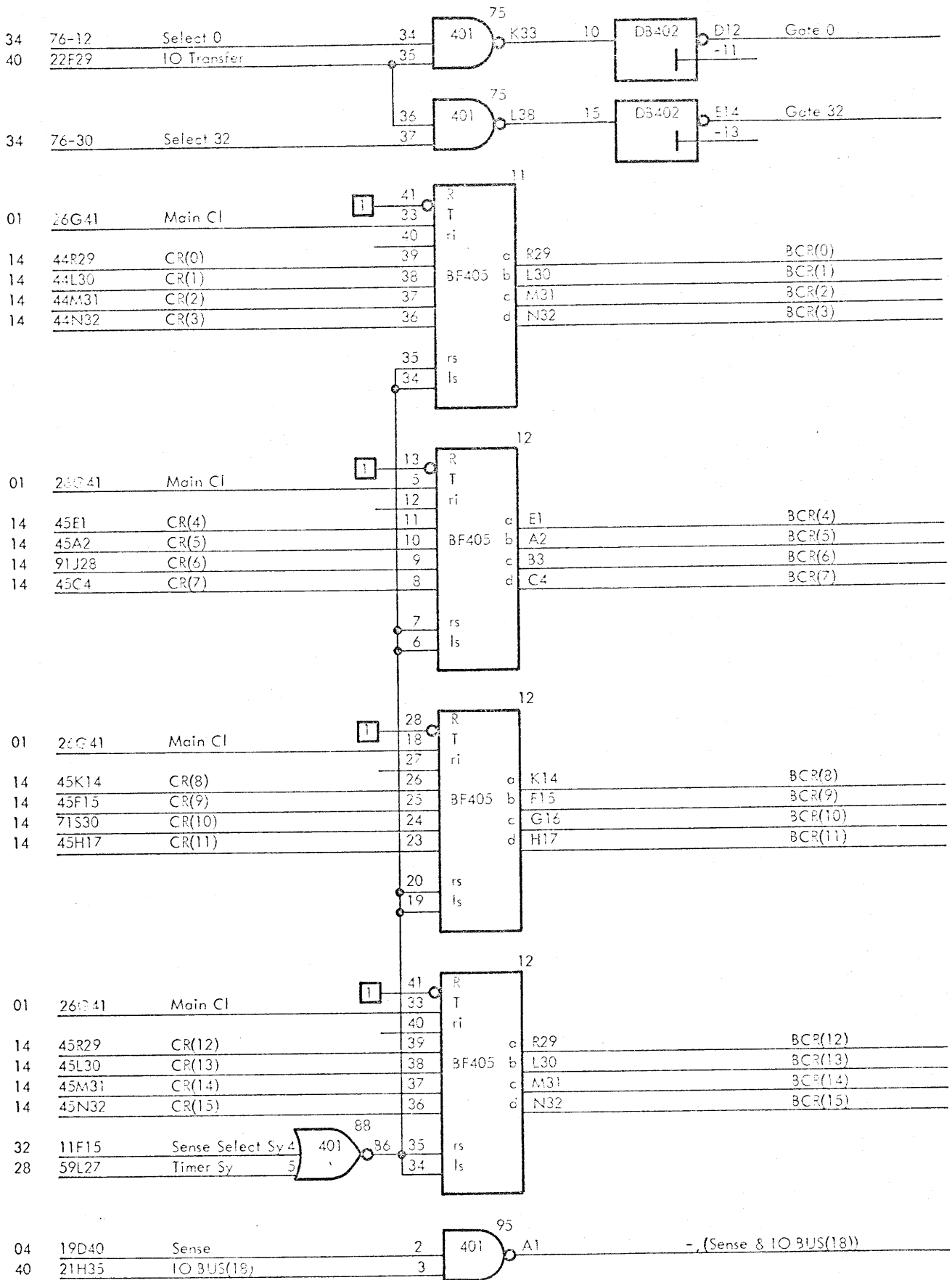


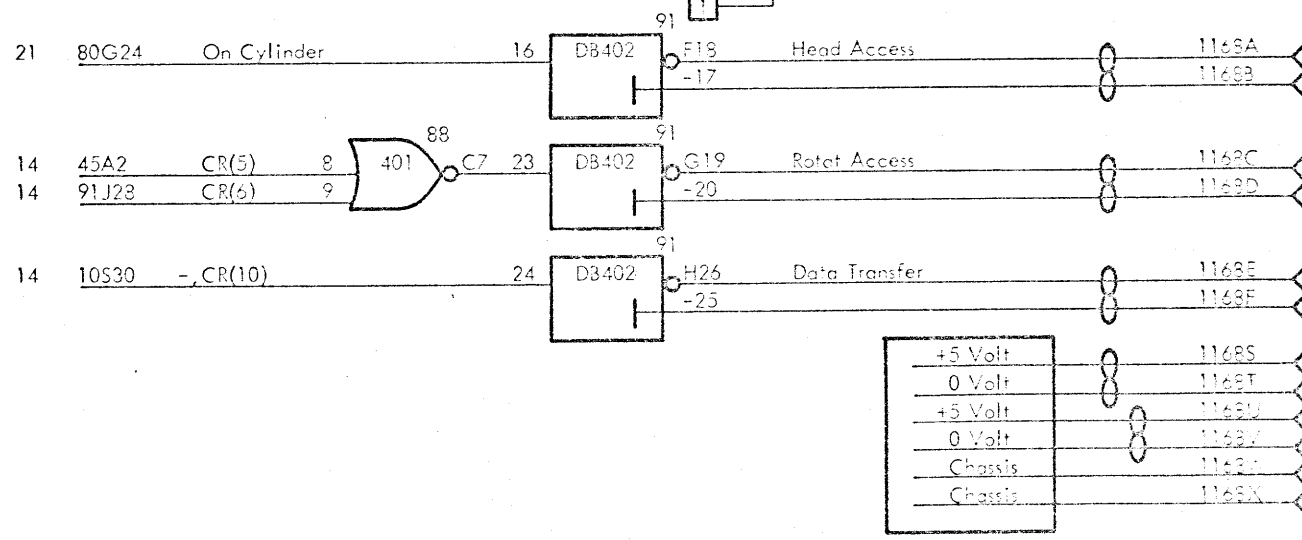
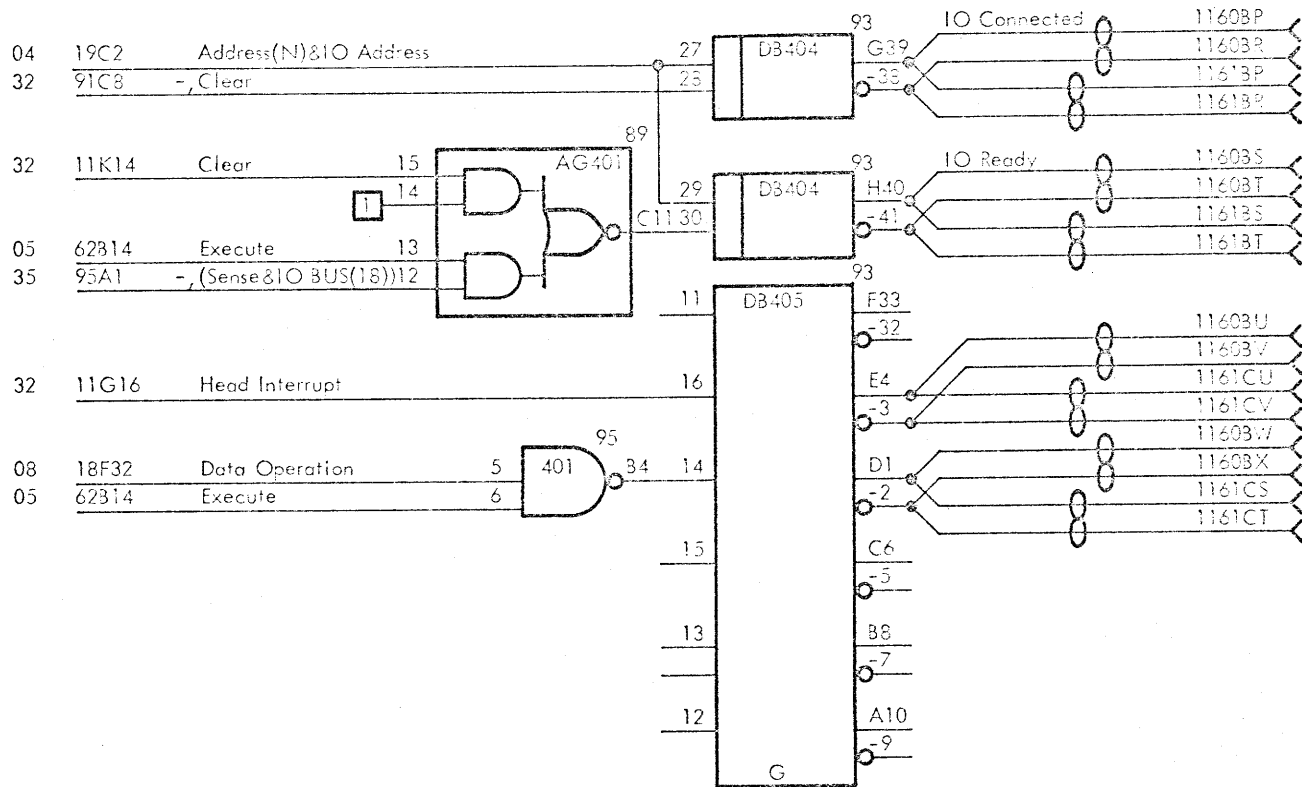
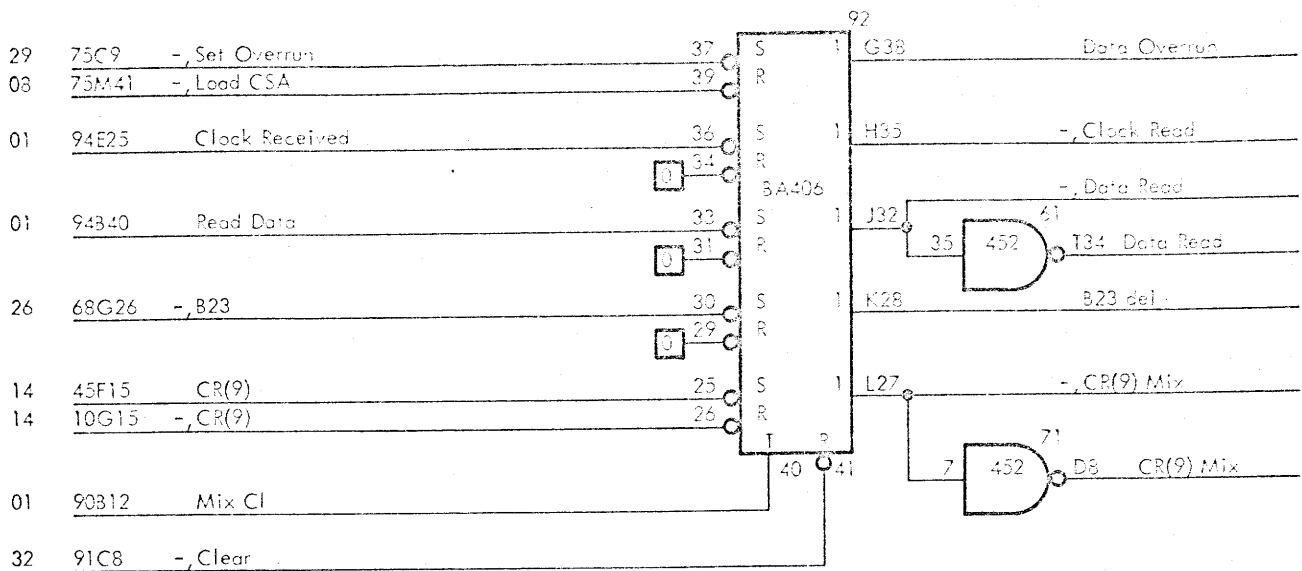


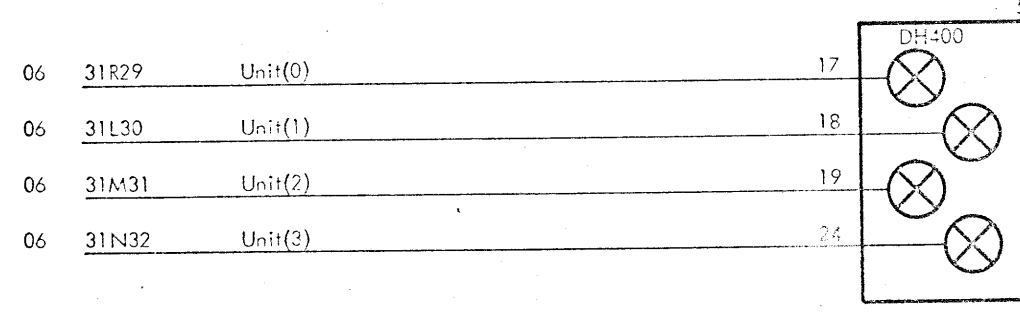
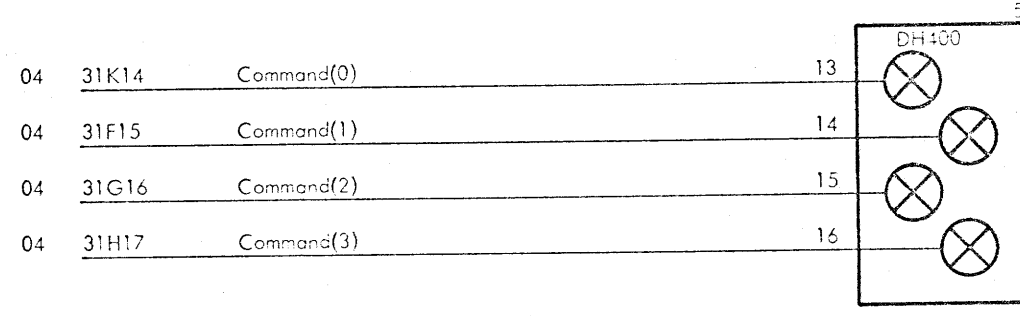
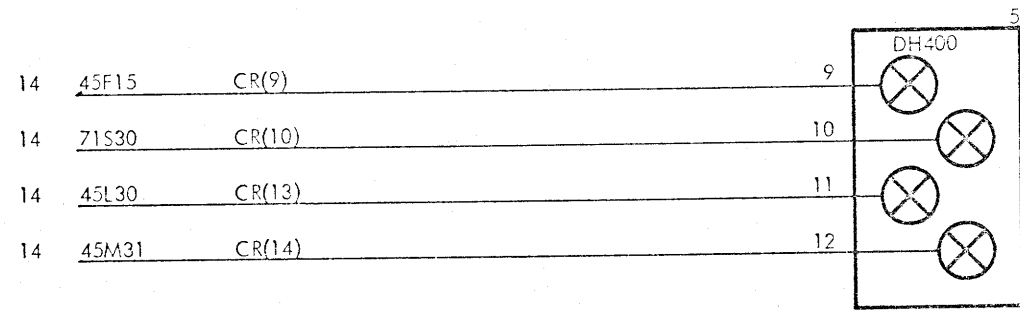
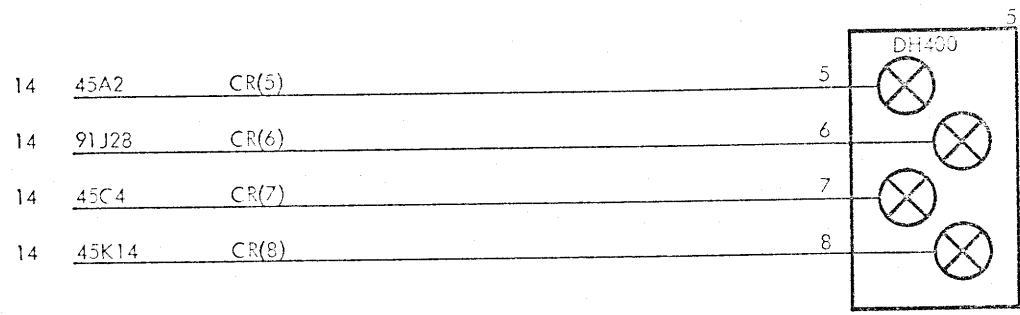
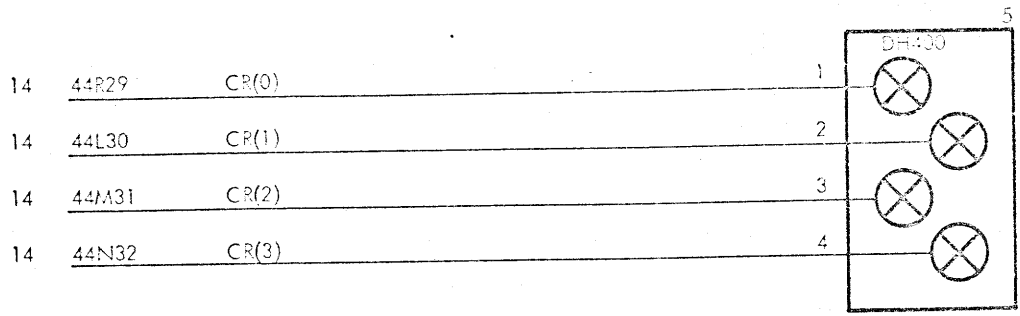


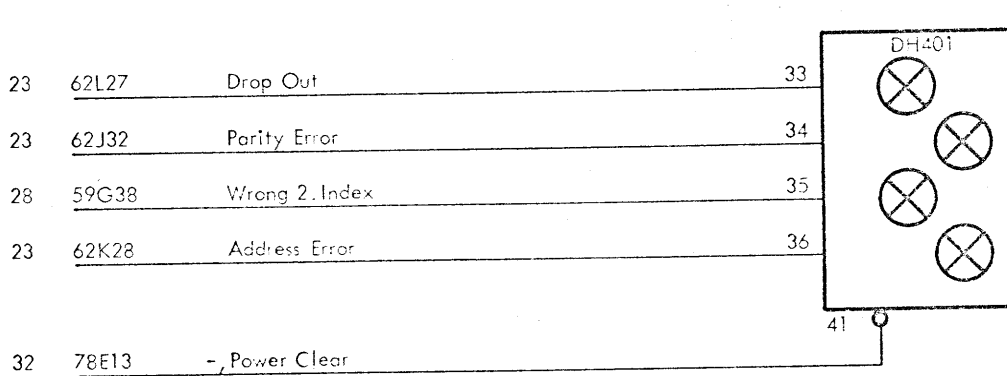
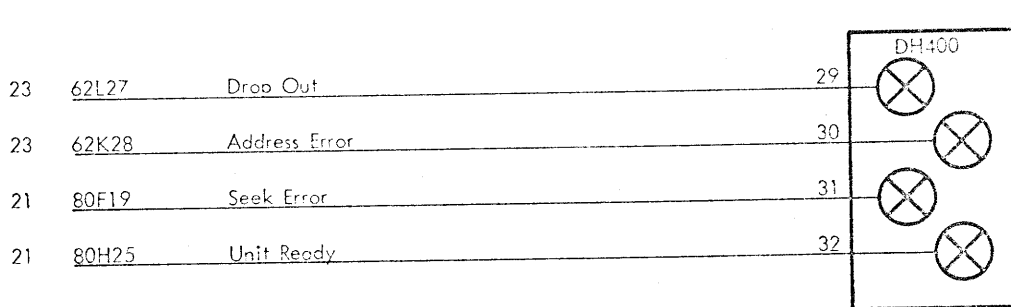
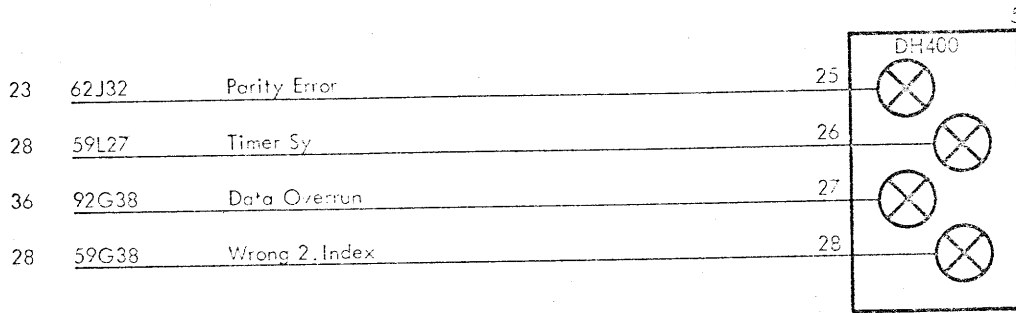


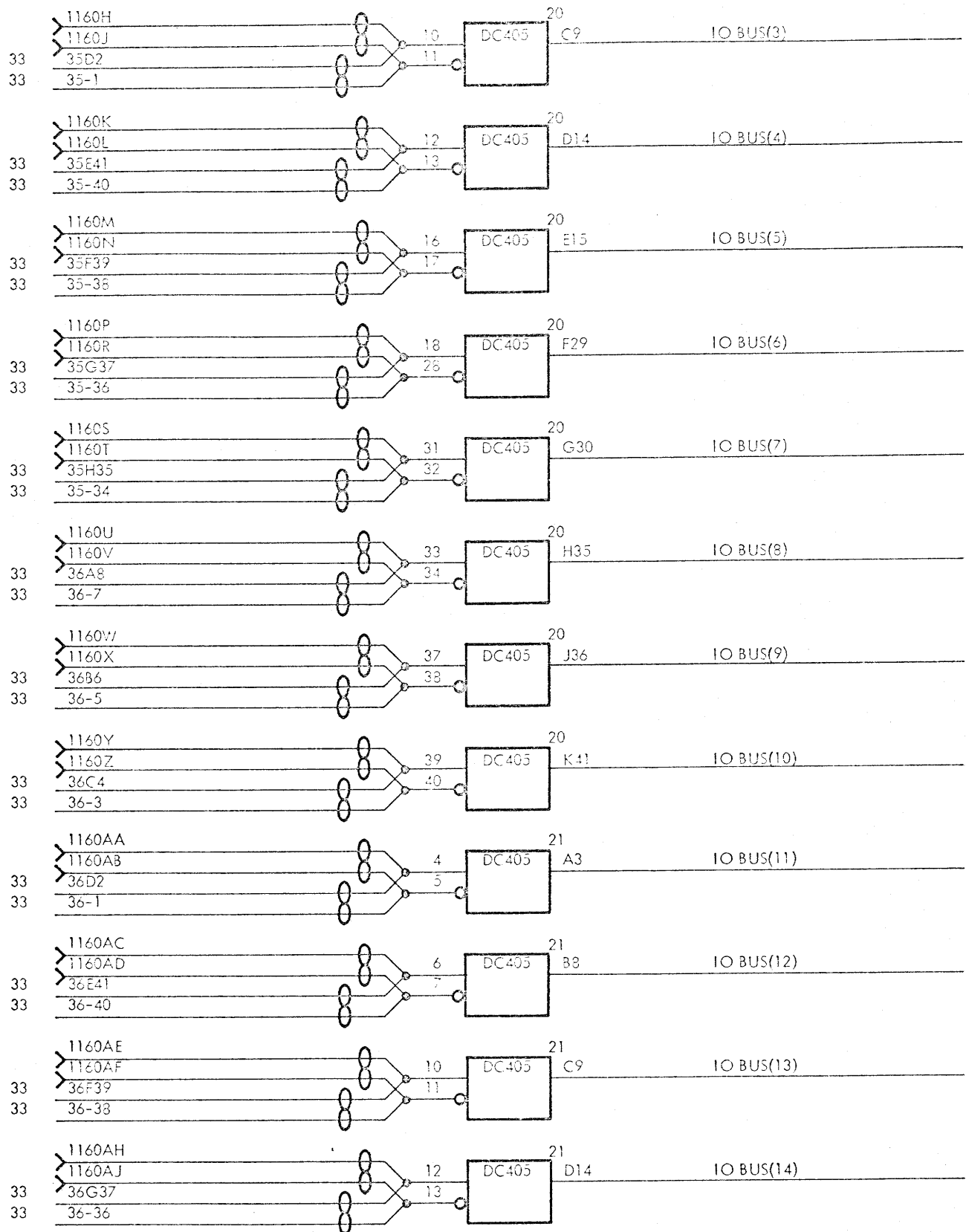








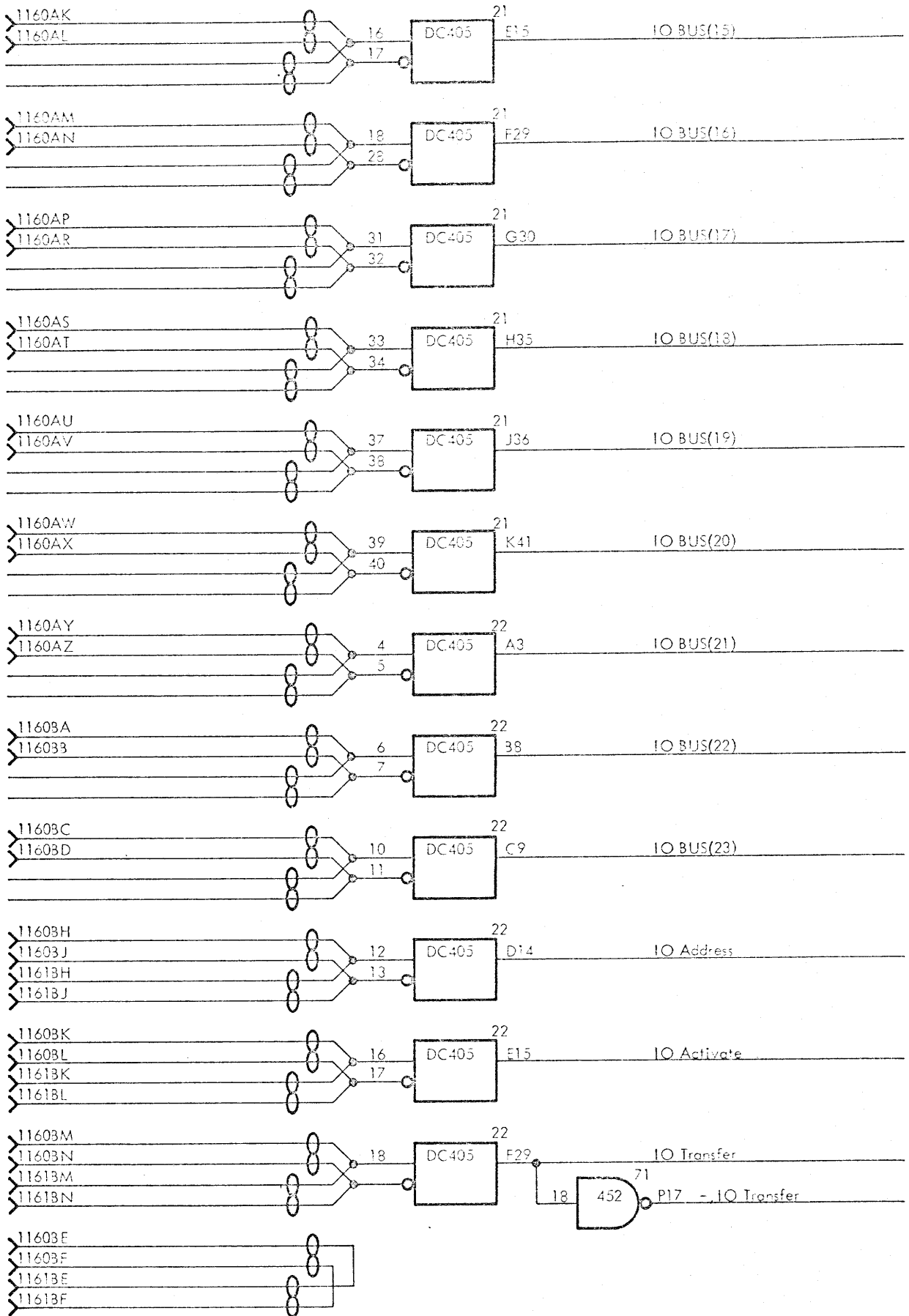


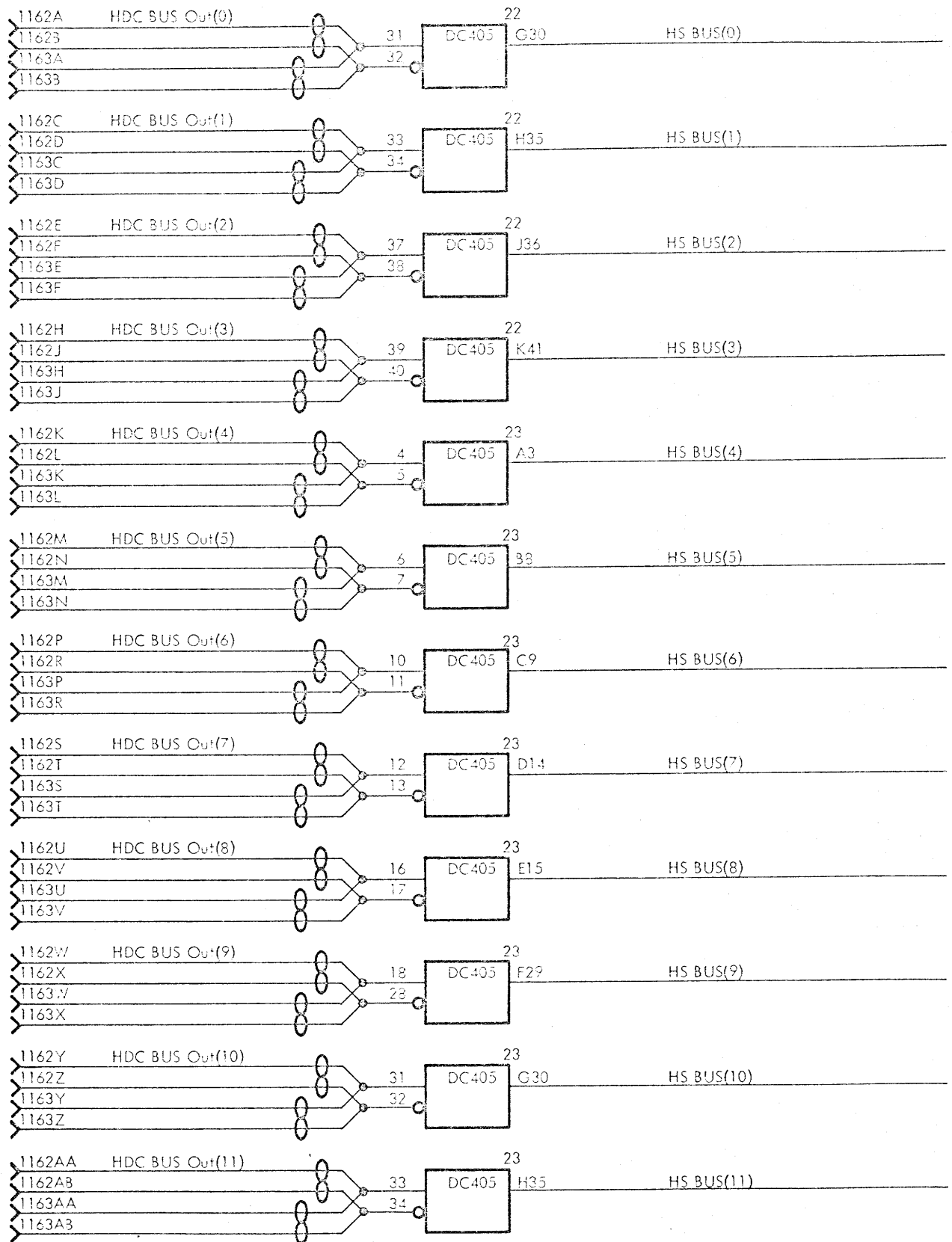


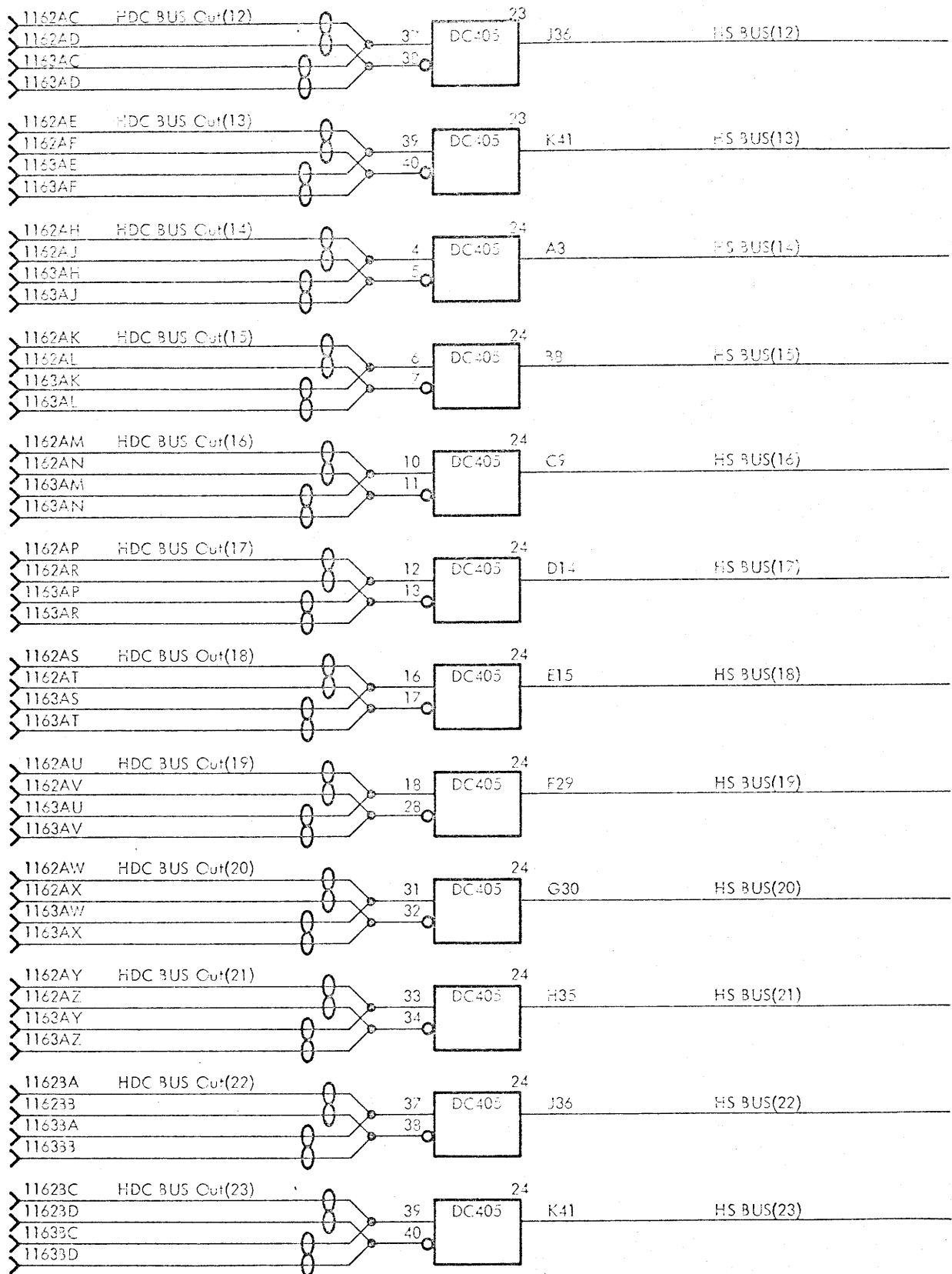
DFC 403
RC4000

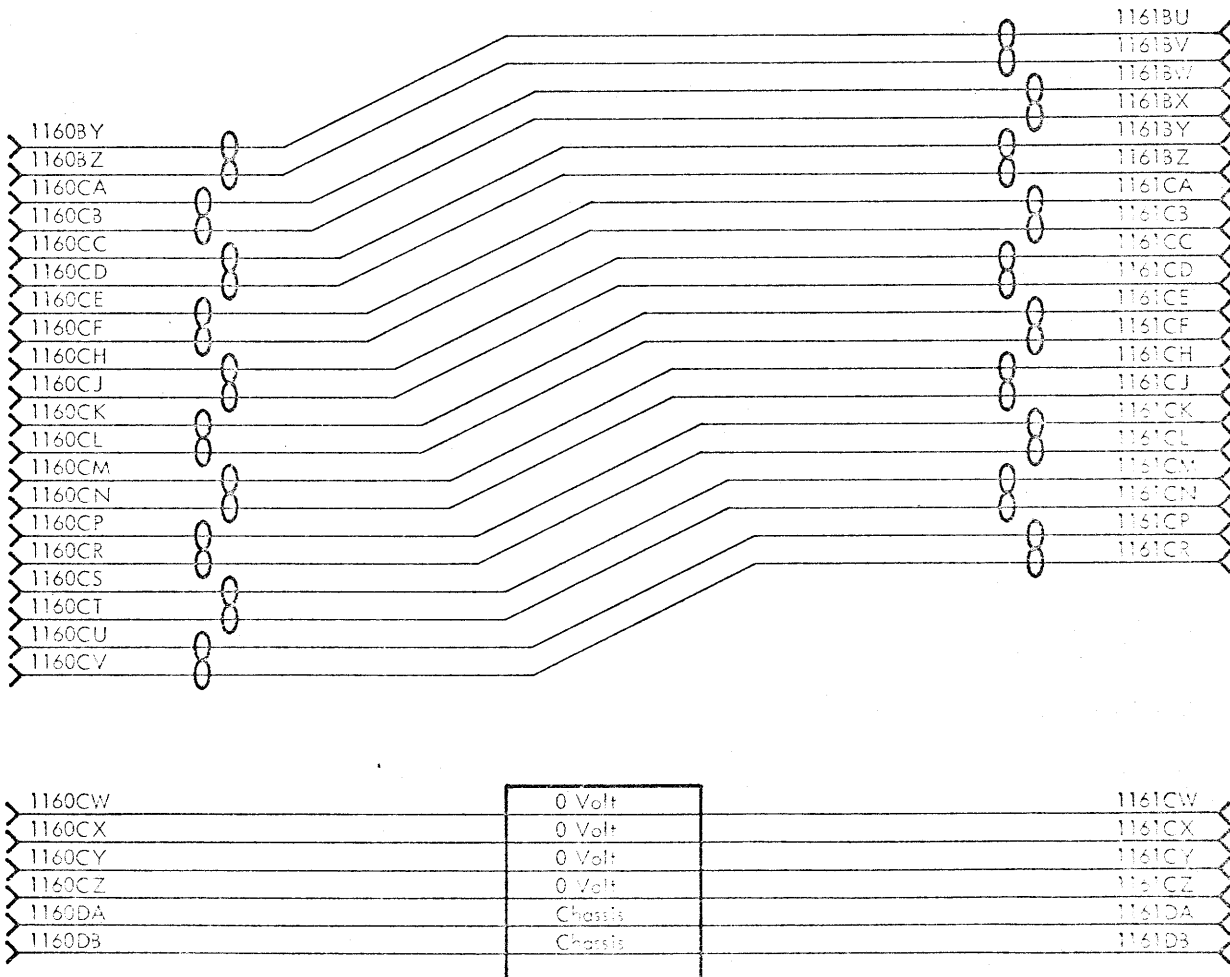
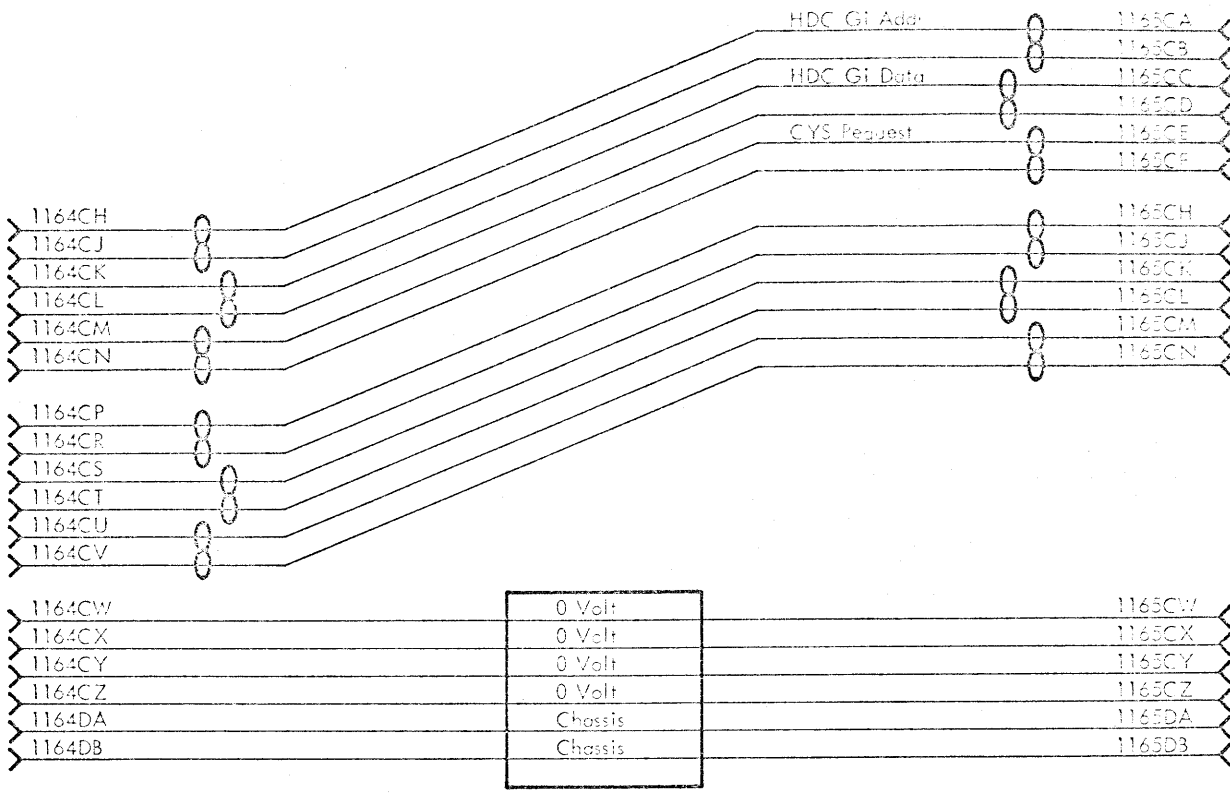
IO BUS(3:14)

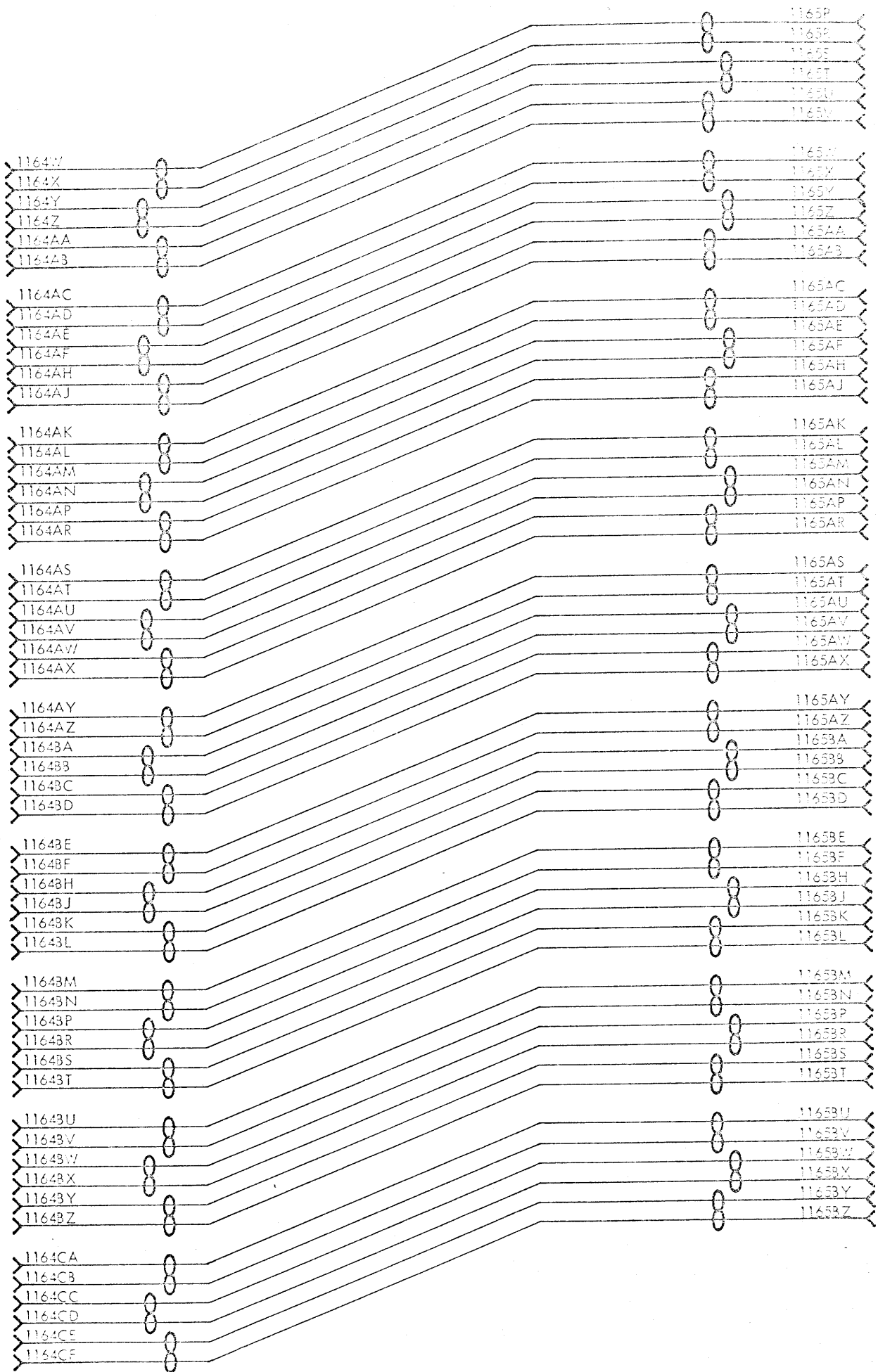
D: C3

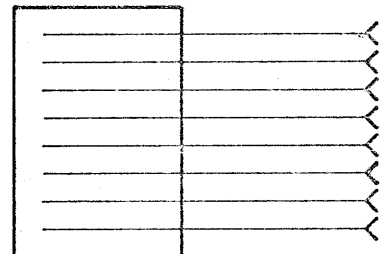
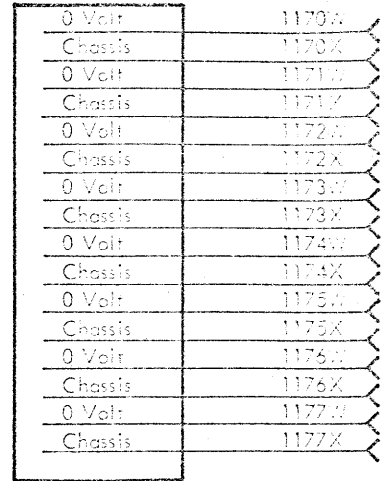
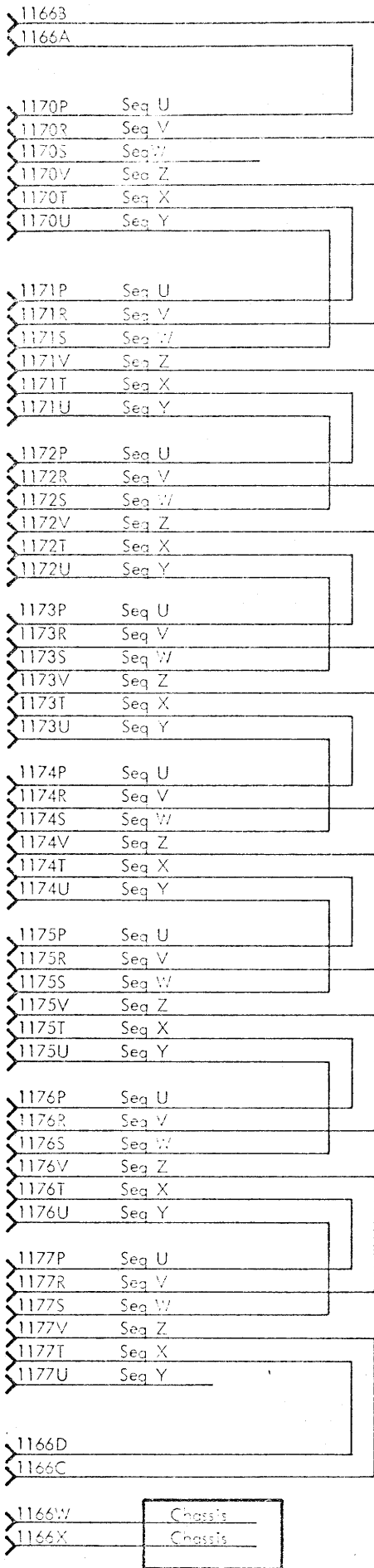




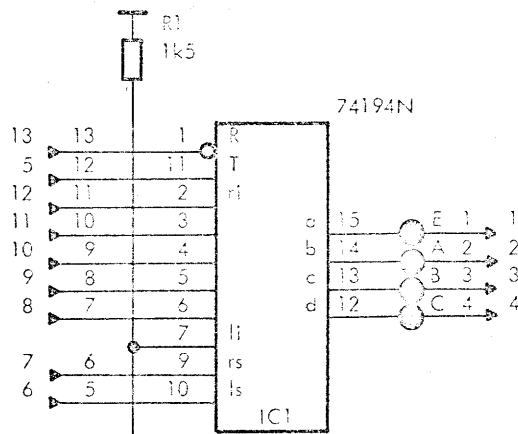




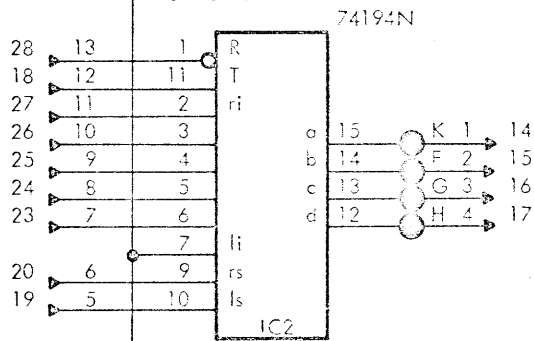




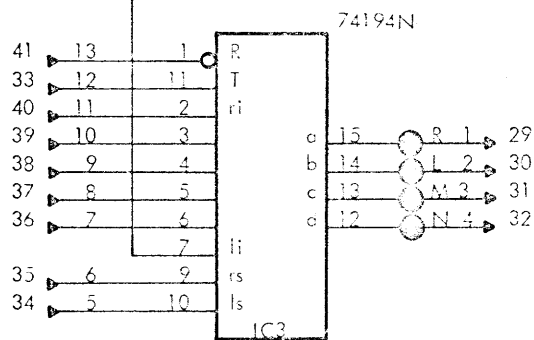
Circuit A



Circuit B

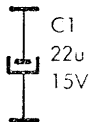


Circuit C

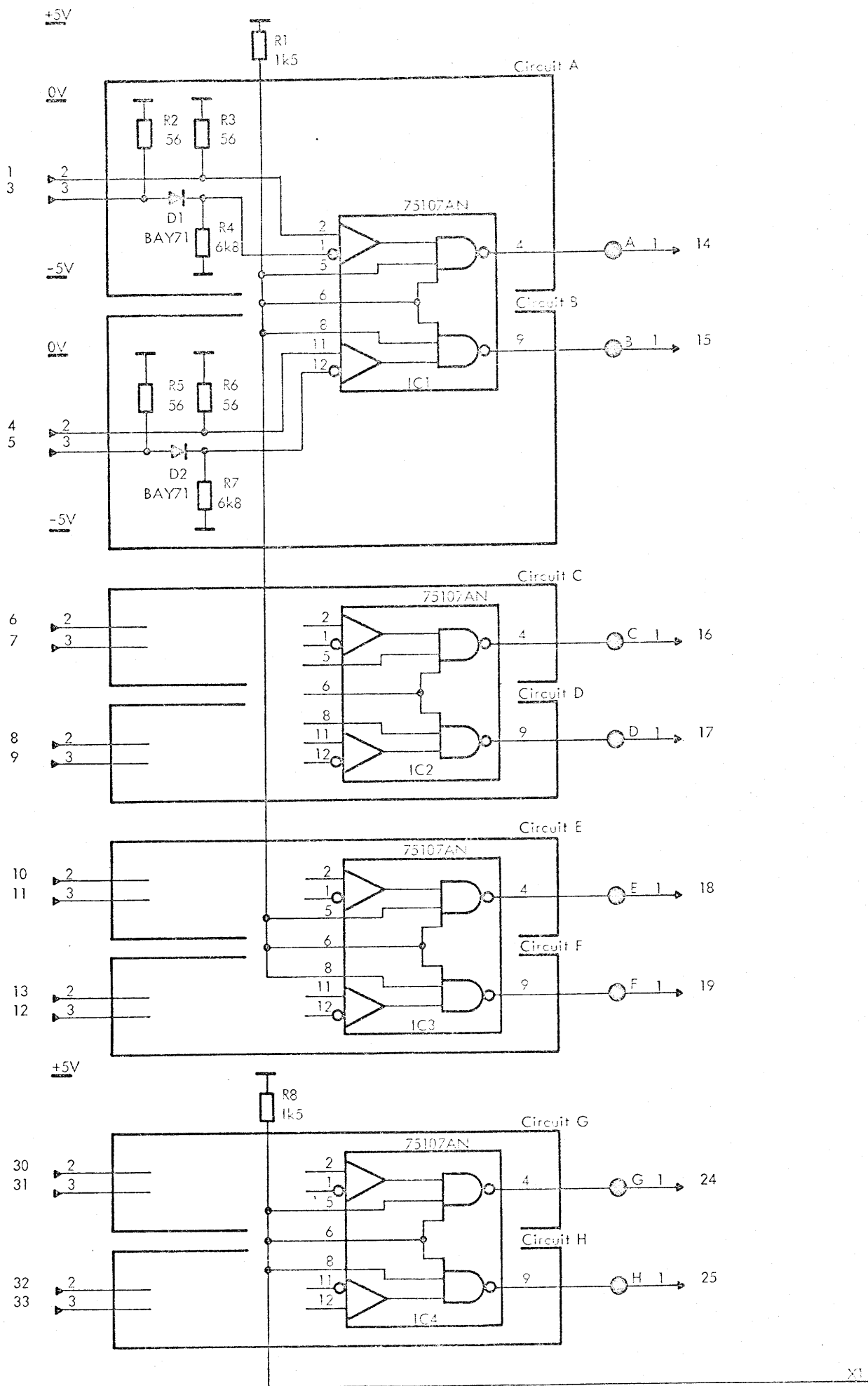


+5V

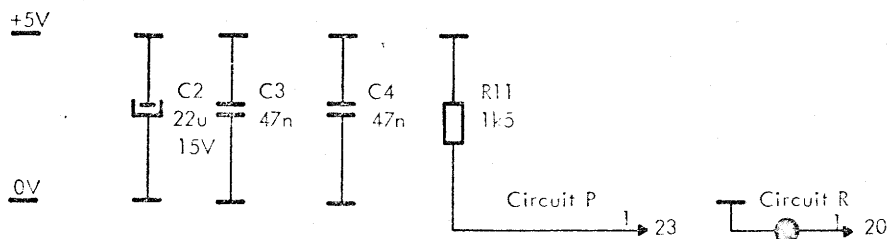
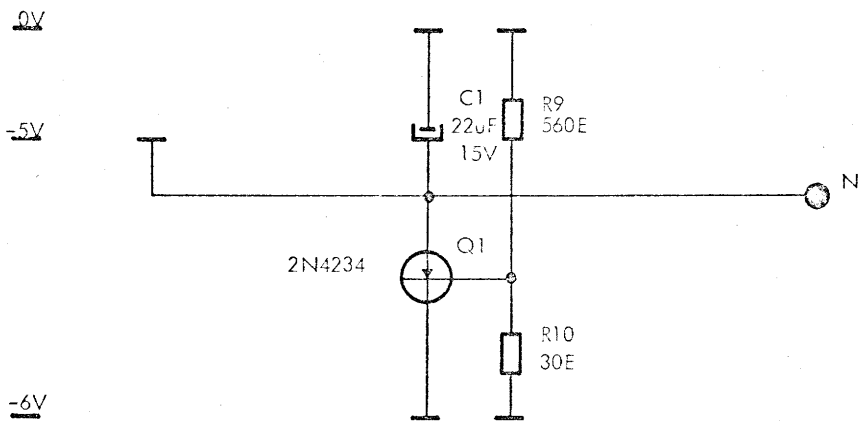
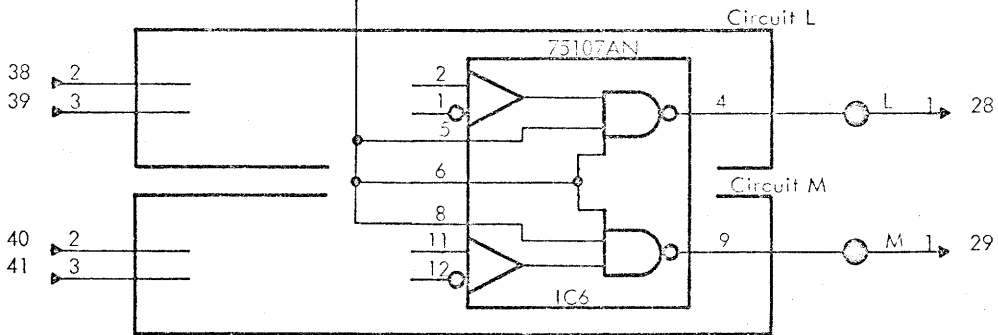
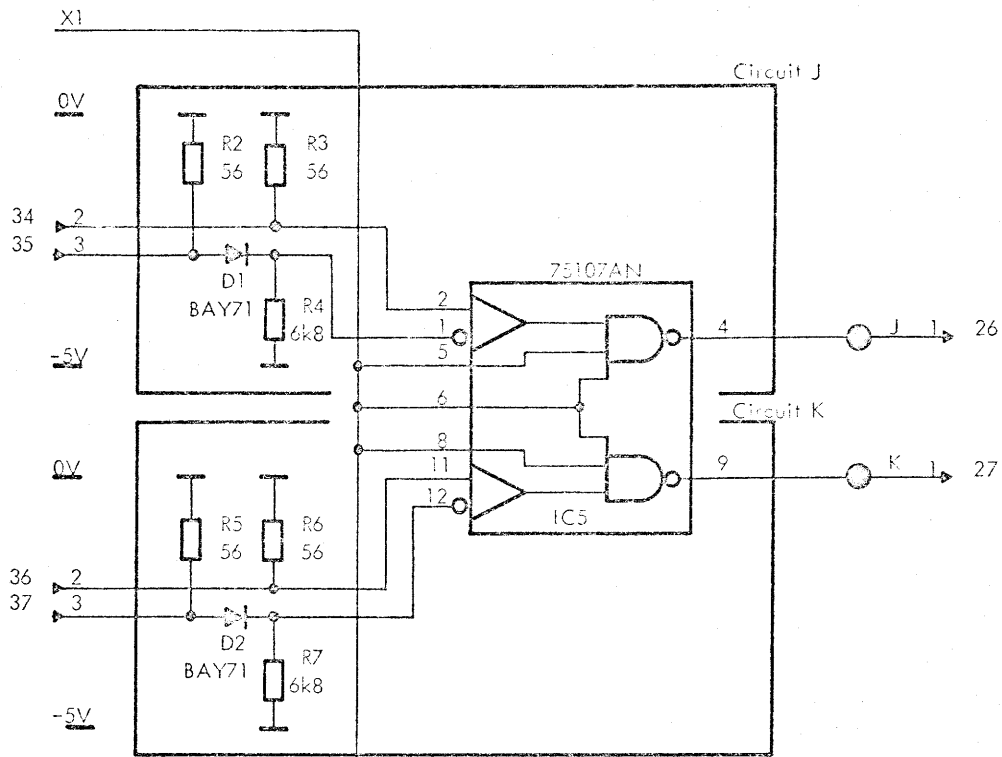
0V



POWER REQUIREMENTS		
+5V	PIN 22	100 mA
0V	PIN 21	
POWER DISSIPATION: 1000 mW		



X1

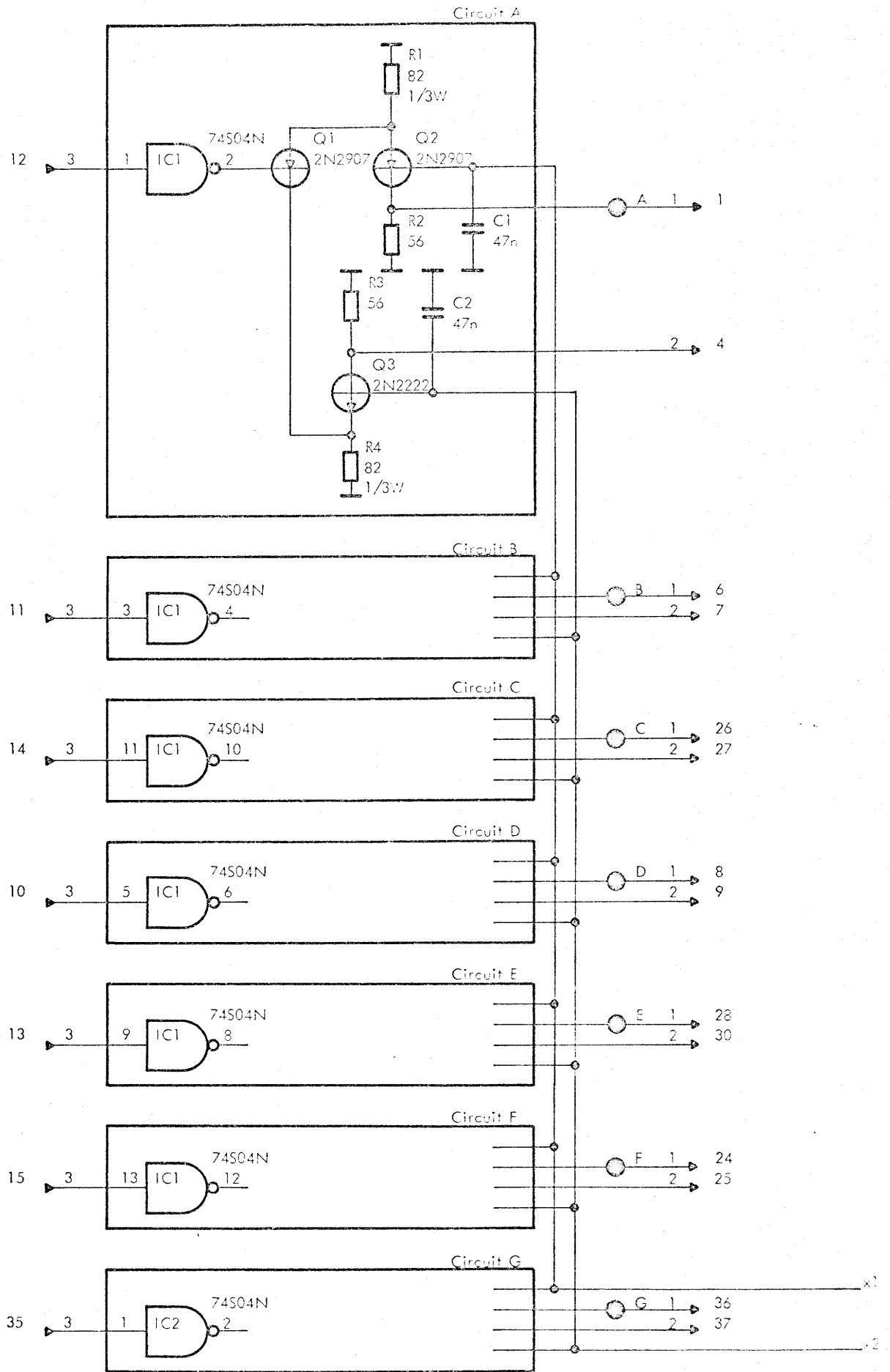


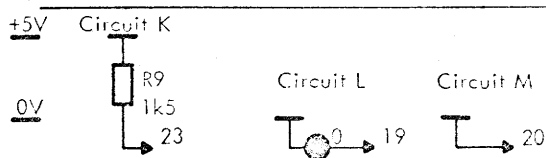
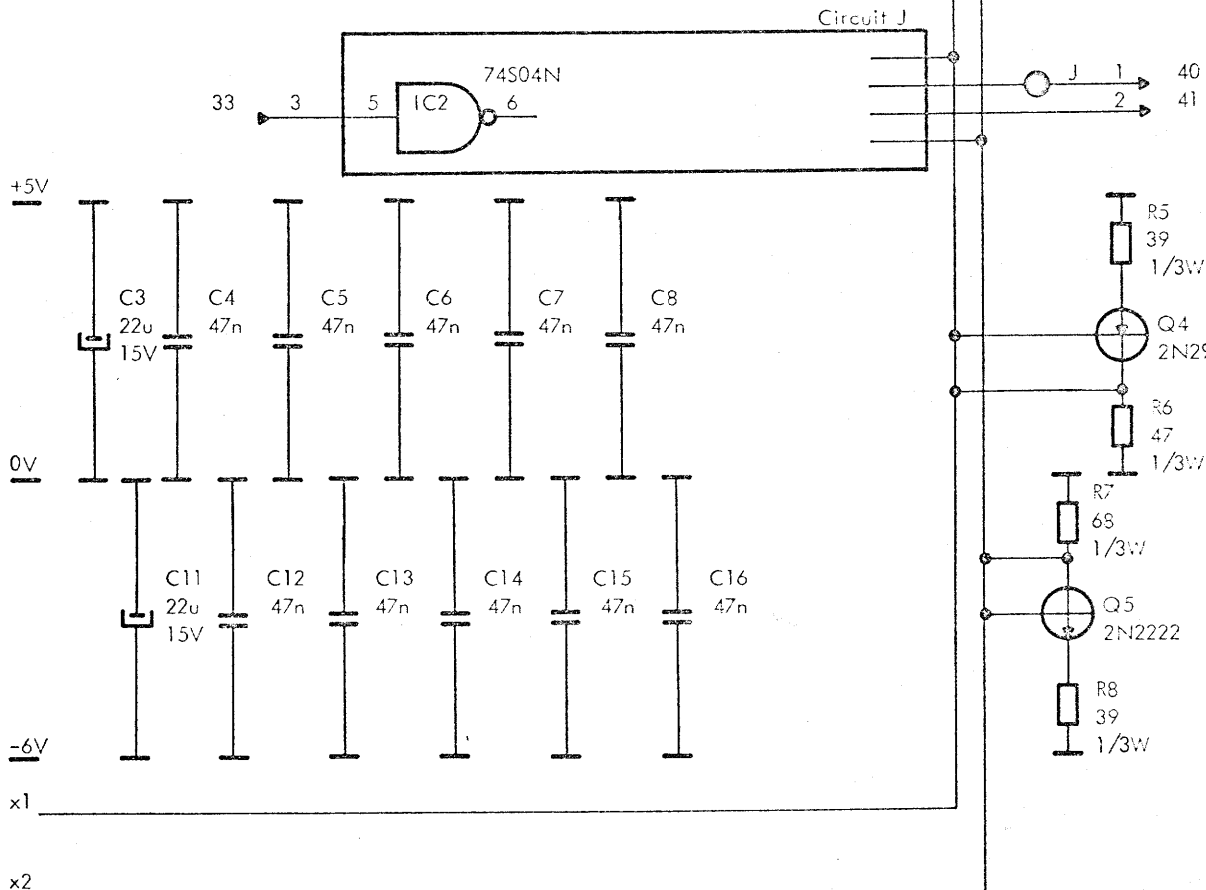
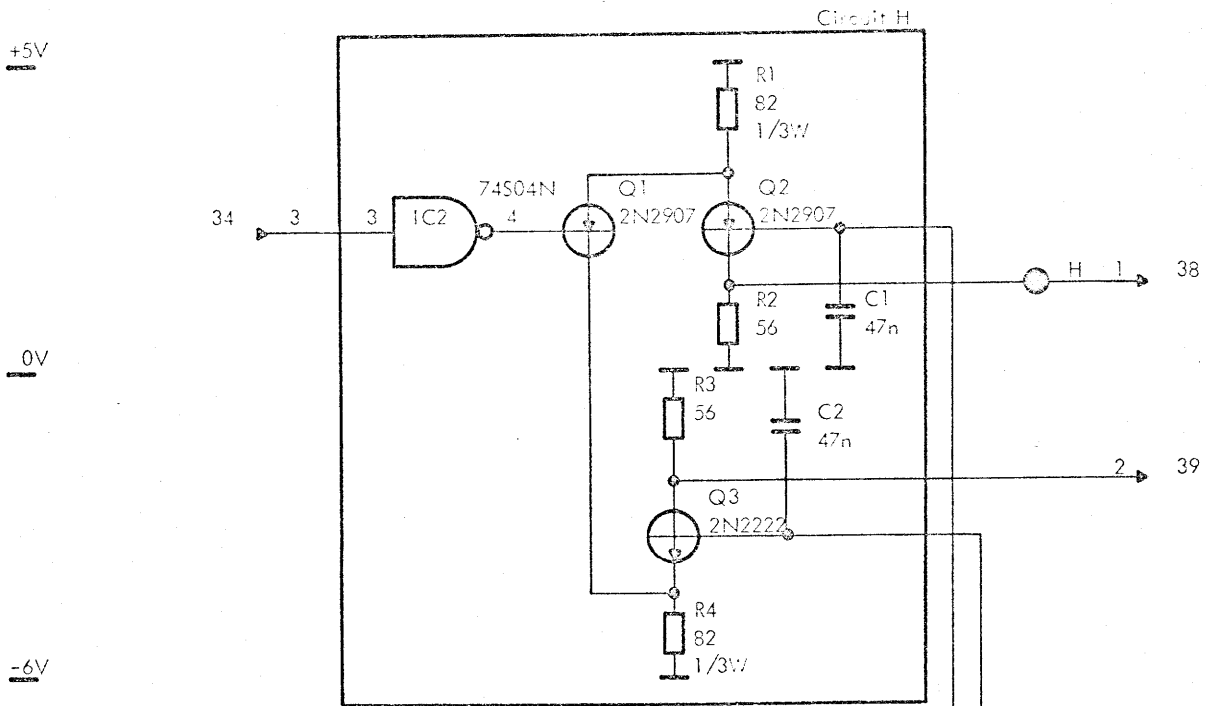
POWER REQUIREMENTS		
+5V	PIN 22	130mA
0V	PIN 27	
-6V	PIN 2	95mA
POWER DISSIP		1500mW

+5V

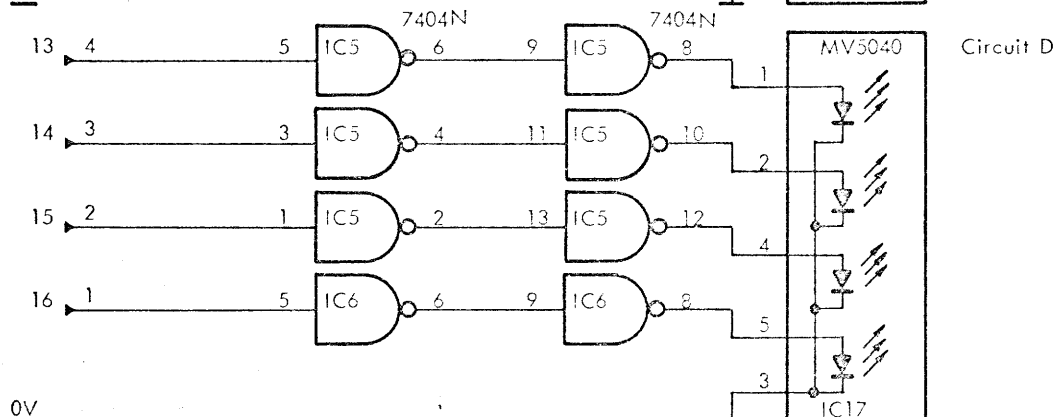
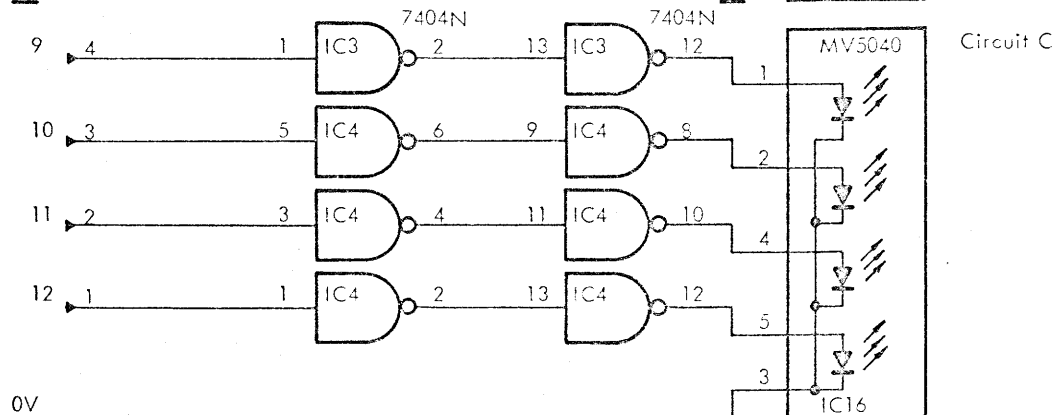
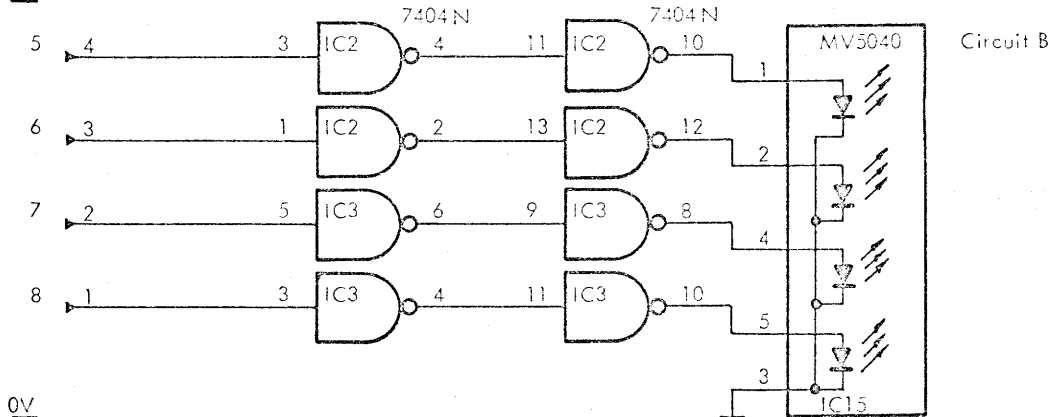
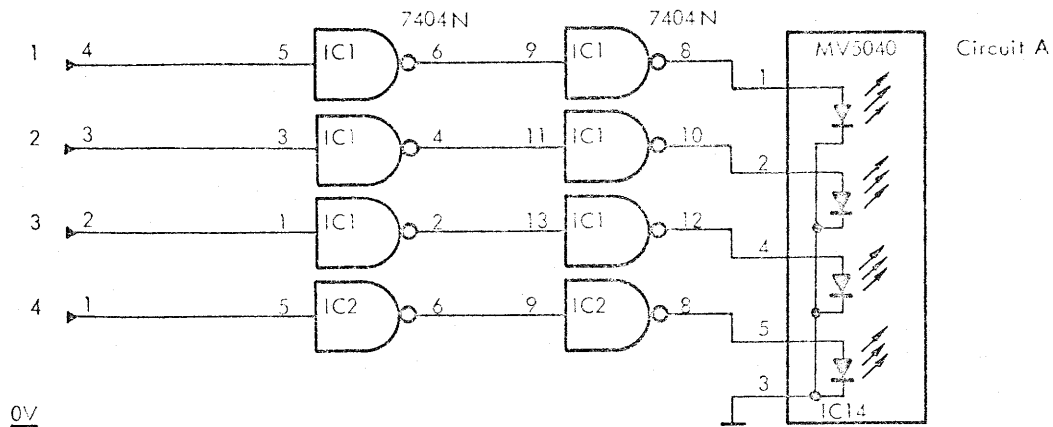
0V

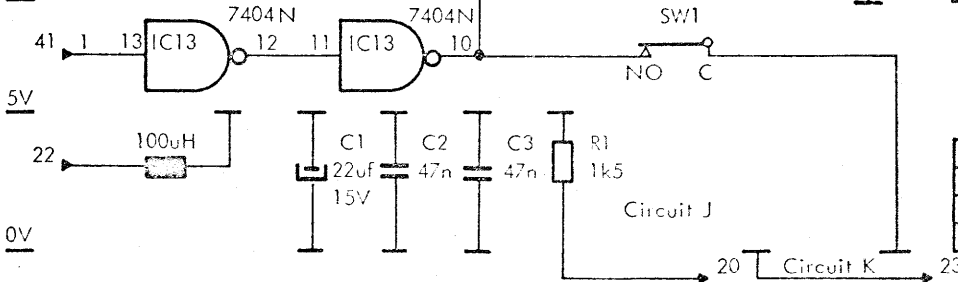
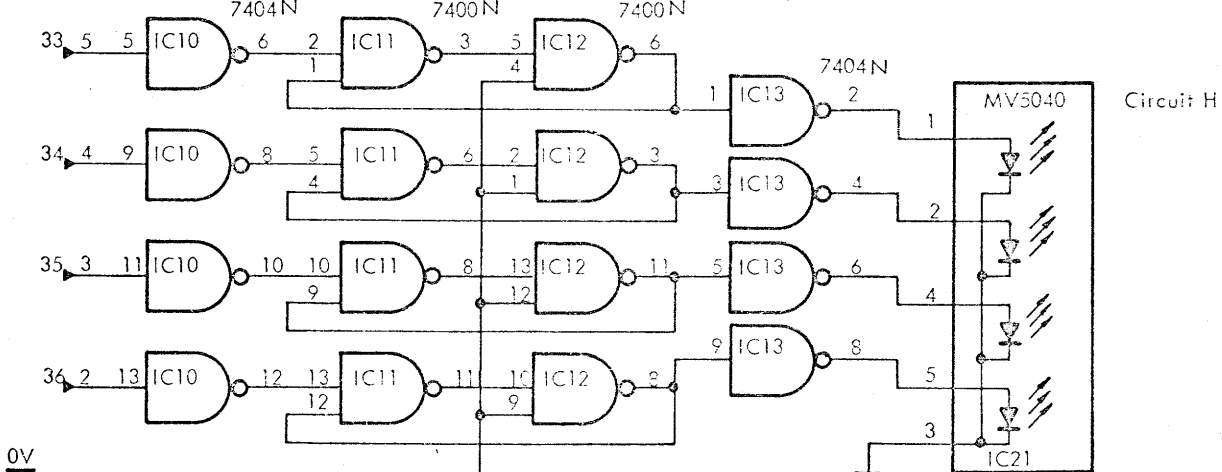
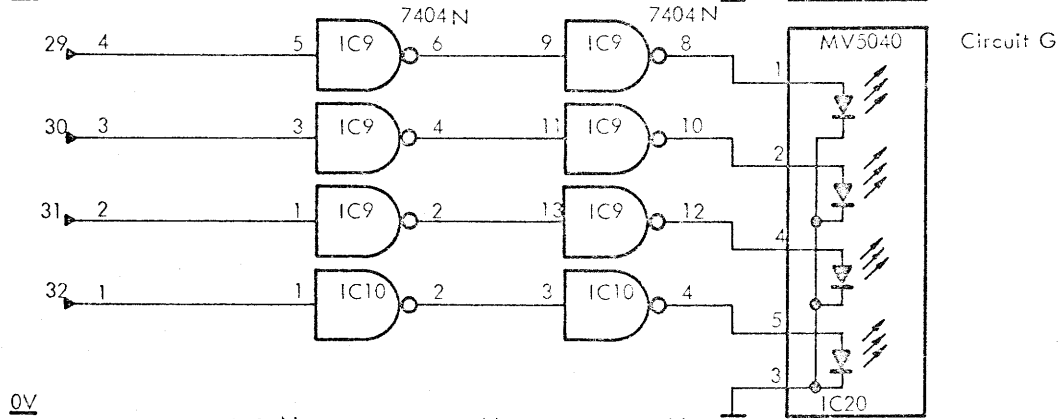
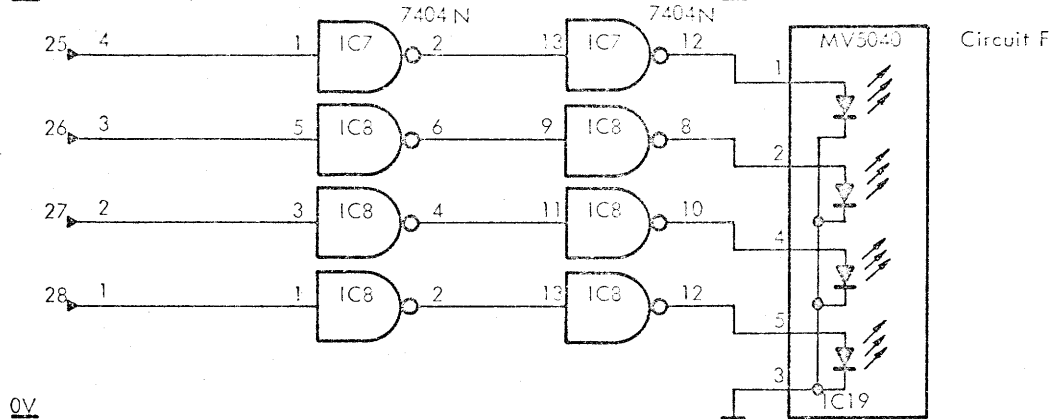
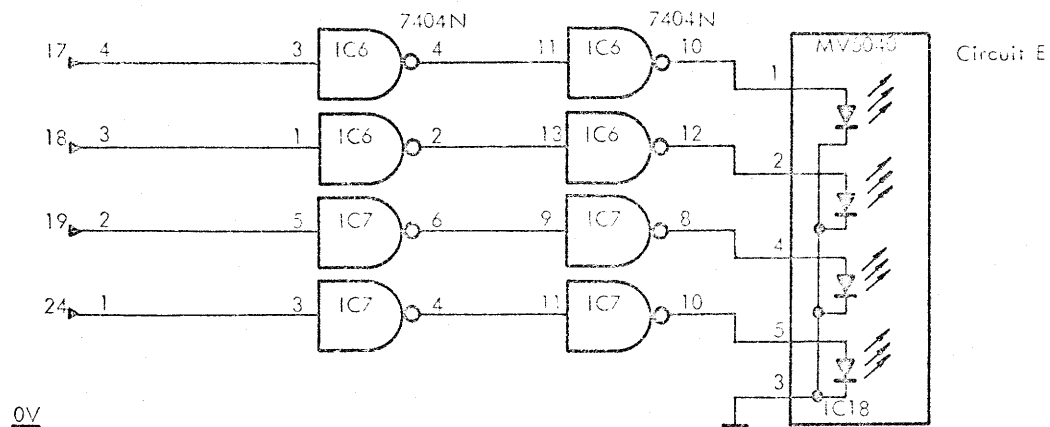
-6V



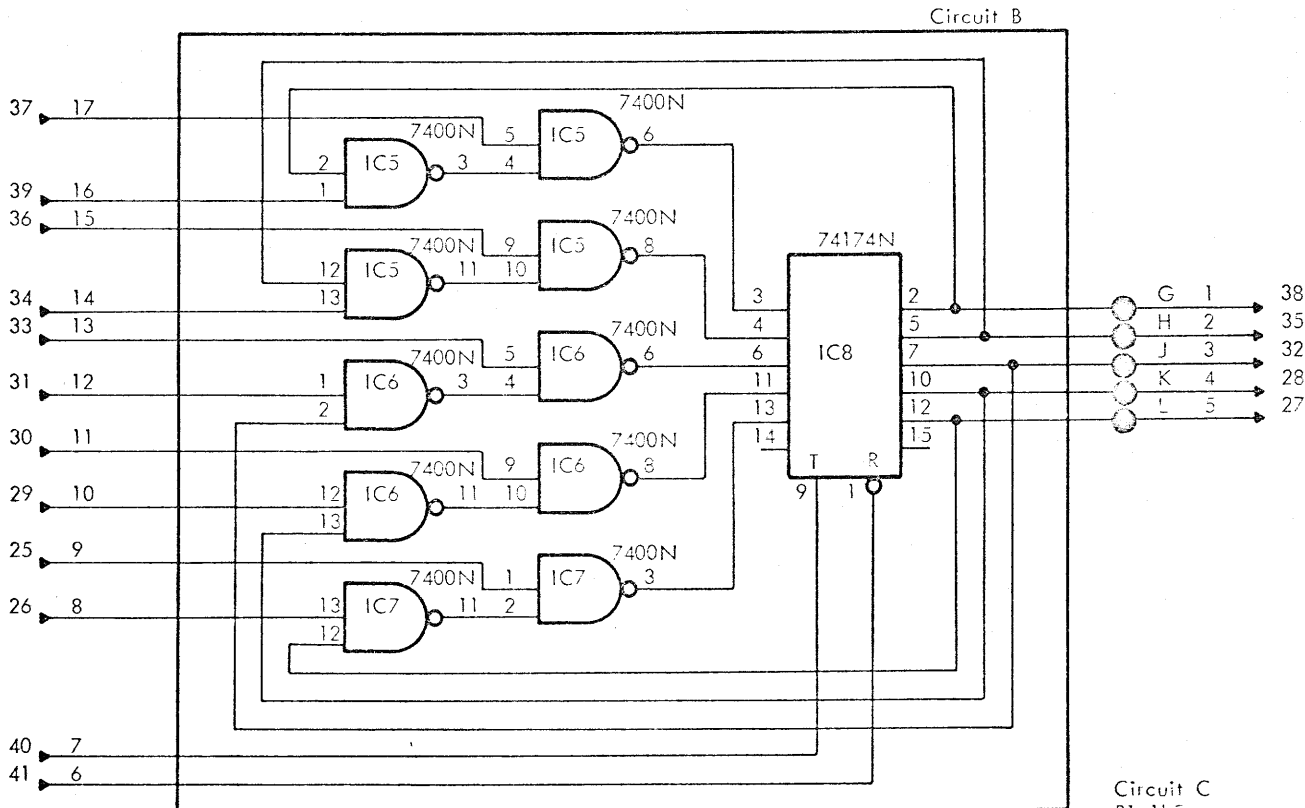
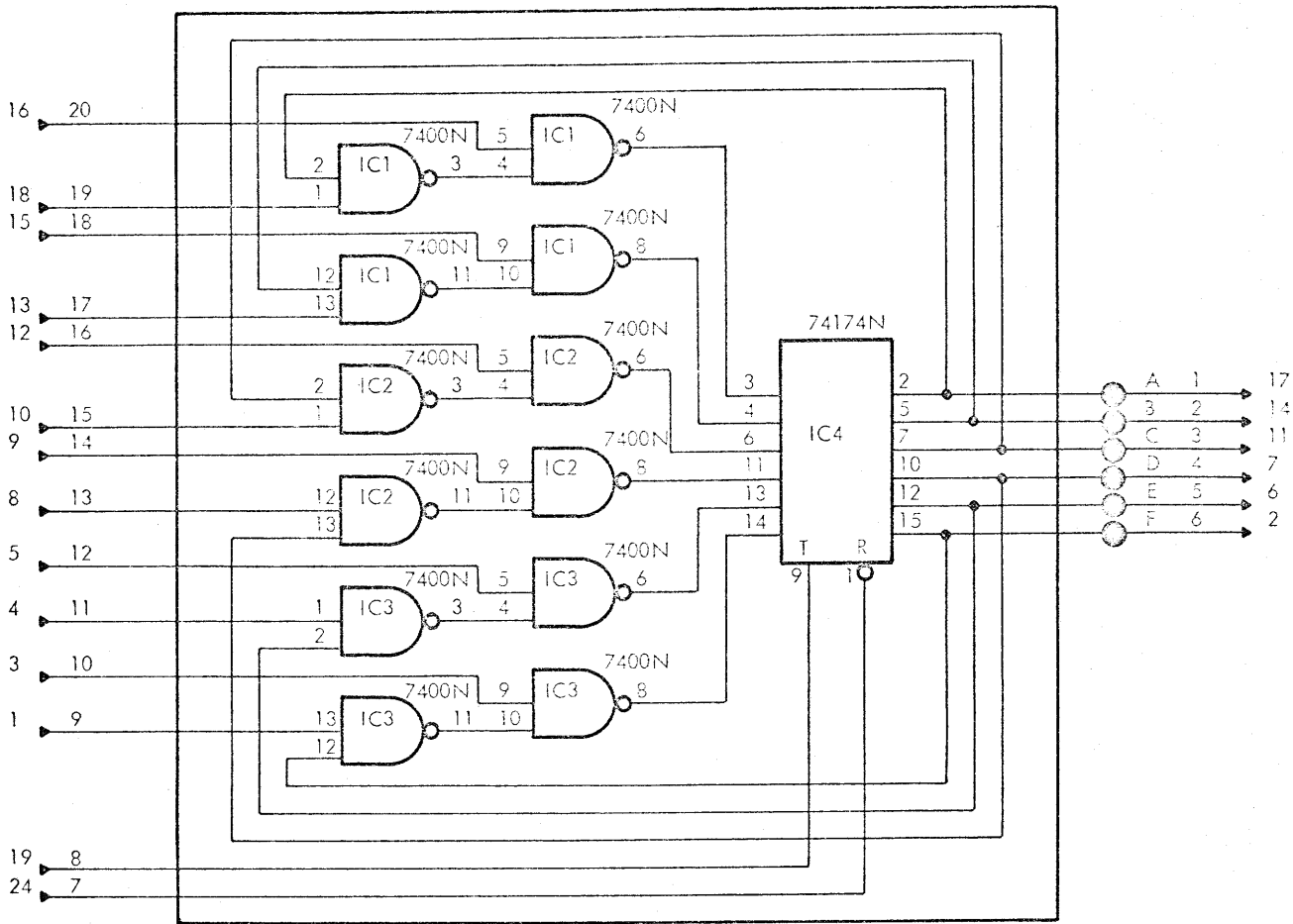


POWER REQUIREMENTS		
+5V	PIN 22	850mA
0V	PIN 2	
-6V	PIN 2	750mA
POWER DISSIPATION: 920mW		





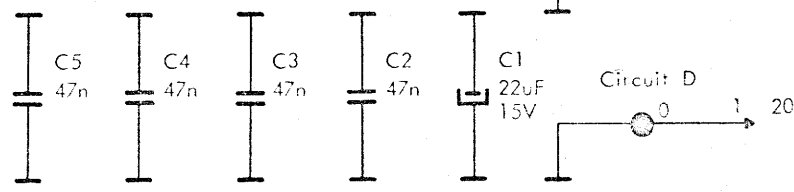
POWER REQUIREMENTS		
+5V	Pin 22	900 mA
0V	Pin 21	
POWER DISSIPATION:		4700 mW



+5V

POWER REQUIREMENTS		
+5V	PIN 22	245mA
0V	PIN 21	
POWER DISSIPATION 1230mW		

0V



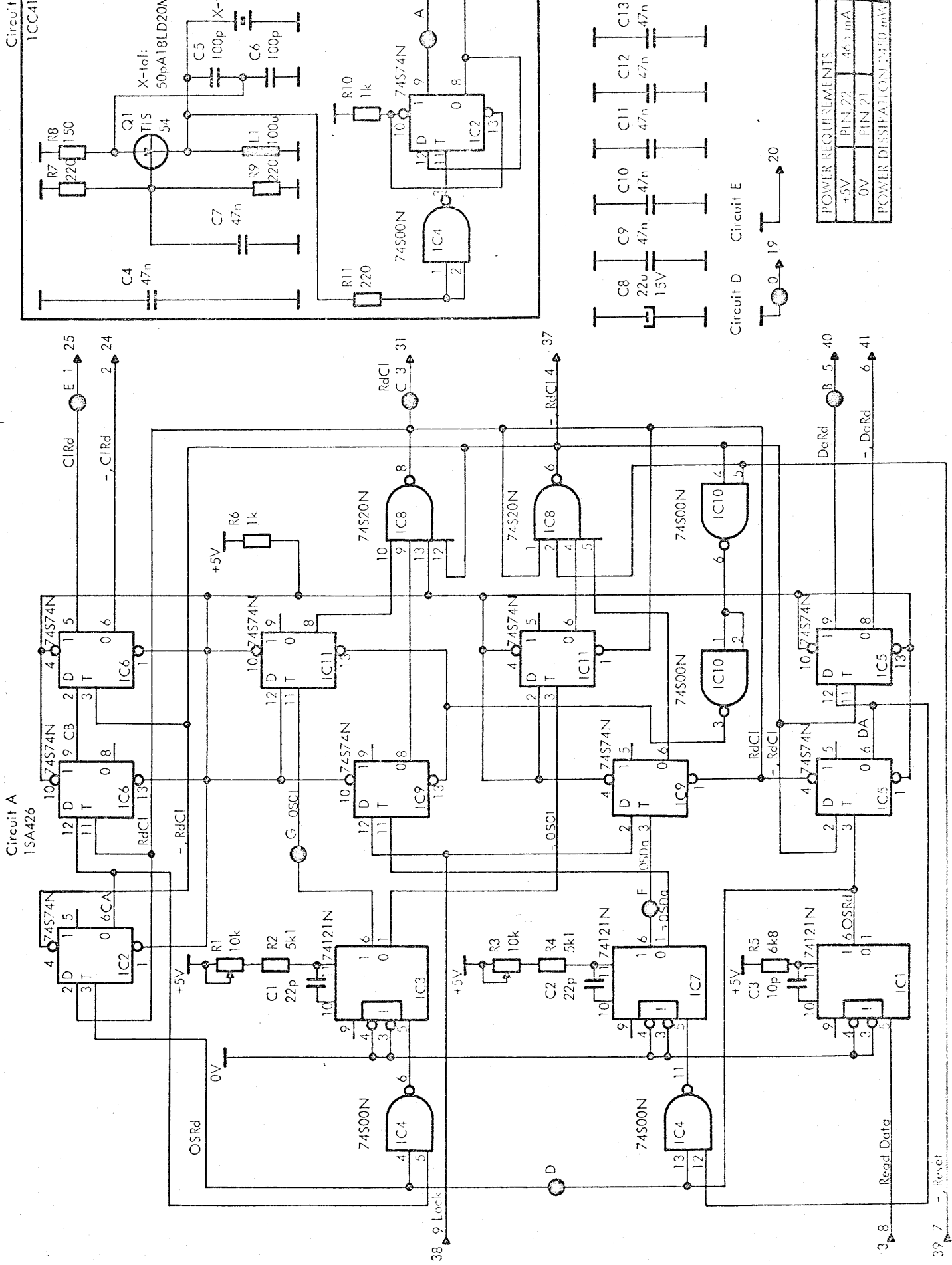
RCLM400

1BA405, 1BA406

RC2060-1

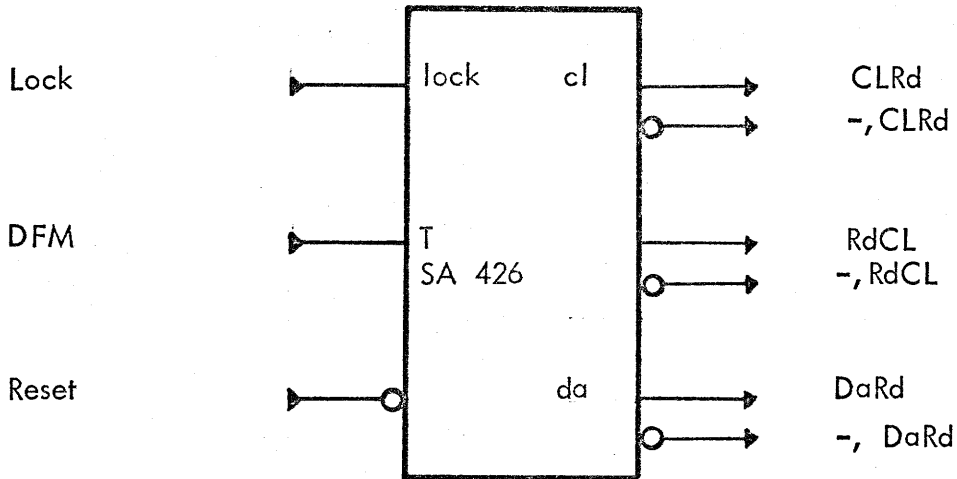
V13410

PCBA Circuit Diagram



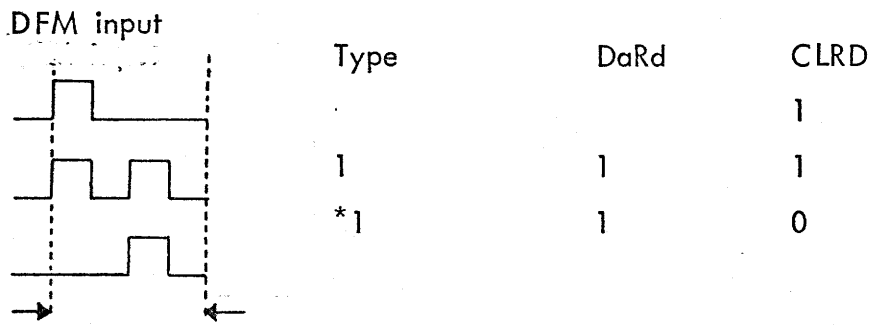
RCLM 400 DATA SHEET

SA 426



CIRCUIT DESCRIPTION

The SA 426 is a 2.5 Mbit/sec readdetector for double frequency modulated pulse trains. It is capable of detecting three types of "bits", 0's, 1's, and * 1's. Their relation to the input pulse train is as follows :

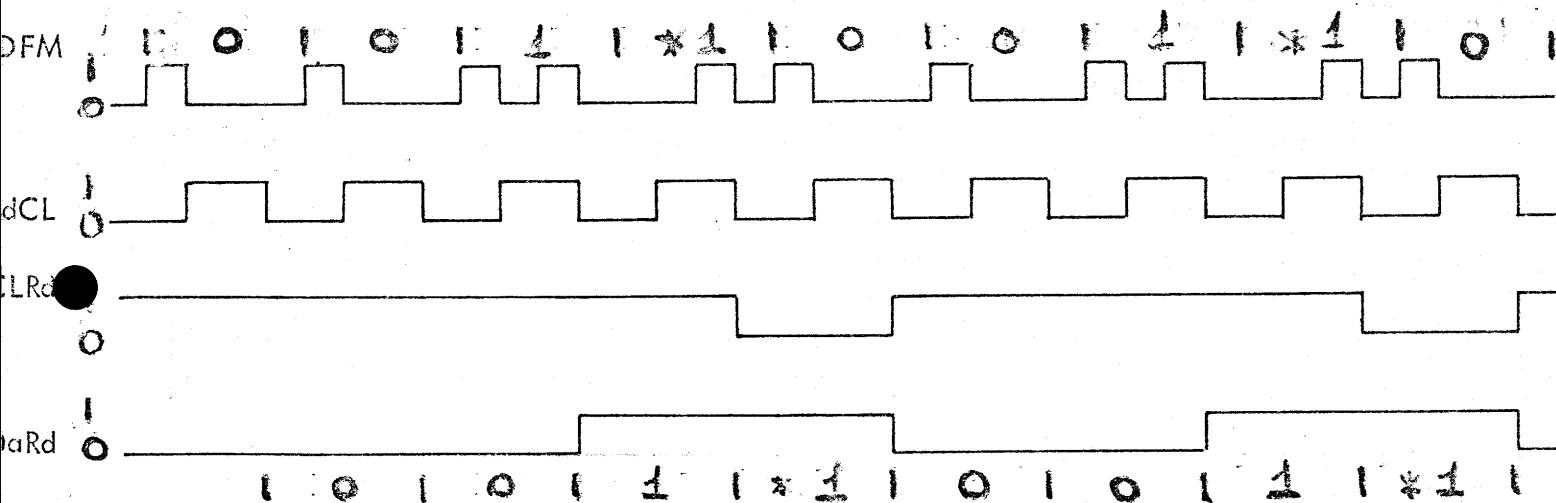


bit period = 400ns

The input pulse train is applied to the DFM input .

The readdetector generates a 2.5 MHz , 50% duty cycle bitperiod clock. (RdCL) .Within each bitperiod, the CLRd and DaRd output defines the type of bit according to the above shown table. The CLRd and DaRd outputs are defined from shortly after the trailing edge of RdCL to the next trailing edge of RdCL.

The output bit period is delayed approximately 300 ns in relation to the input bit period. A typical sequence may be as follows:



The input Reset clears when low asynchronous the RdCL bistable (RdCL =0) and brings the edgetriggering inputs to this bistable in a well defined initial state. The input is used to establish a bit period synchronization to a 0's pattern when low. When high, the readdetector keeps synchronization if no pulse- pulse time exceeds 400 ns nominal. In order to keep in synchronization when Lock= 1, a 0- * 1 sequence must be avoided.

The internal working principle of the readdetector is as follows. (Conf. Circuit Diagram V 13589 and Timing Diagram V 13472).

A nominal 100 ns monostable OSRd is triggered at each leading edge of the DFM input.

The state of the RdCL bistable at the raising edge of OSRd determines the classification of the pulse.

If RdCL= 0 at the OSRd raising edge , the pulse is registered as a "clock" pulse by setting CA= 1.

If RdCL= 1 at the OSRd raising edge , the pulse is registered as a " data " pulse by setting DA = 1.

At the trailing edge of OSRd, one of two nominal 200 ns monostables are triggered (OSCI and OSDa).

If the pulse was registered as a " clock " pulse (CA= 1) , OSCI is triggered.

If the pulse was registered as a " data " pulse (DA = 1), OSDa is triggered.

OSCI and OSDa control together the state of the RdCL bistable.

The RdCL bistable has two edge triggered set inputs and two edge triggered clear inputs.

RdCL is set by the earliest of leading edge OSCI and trailing edge OSDa.

RdCL is cleared by the earliest of trailing edge OSCI and leading edge OSDa.

When lock= 0 the set - clear inputs from OSDa are inhibited. RdCL is then only controlled by OSCI.

The RdCL and -, RdCL is furthermore used for clocking the CA and DA information into buffers (CB, CLRd and DaRd).

ADJUSTMENT PROCEDURE .

The readdetector may be adjusted off-line as follows.

A 5 MHz clock is applied to the DFM input. Lock= 1 .

The readdetector is reset by shortly applying a 0 to the Reset input. The monostables OSC1 (test point G) and OSDa (test point F) is first adjusted to approximate 250 ns.

RdCL (test point C) is monitored on the scope and the OSC1 time (test point G) is decreased until it just begins to move the trailing edge of RdCL.

In the same way the OSDa time (test point F) is decreased until it just begins to move the leading edge of RdCL.

Finally check , that OSRd leading edge (test pnt. D) fall approximately in the middle of each RdCL half period. To obtain this, the OSRd should be approximately 60 ns wide.