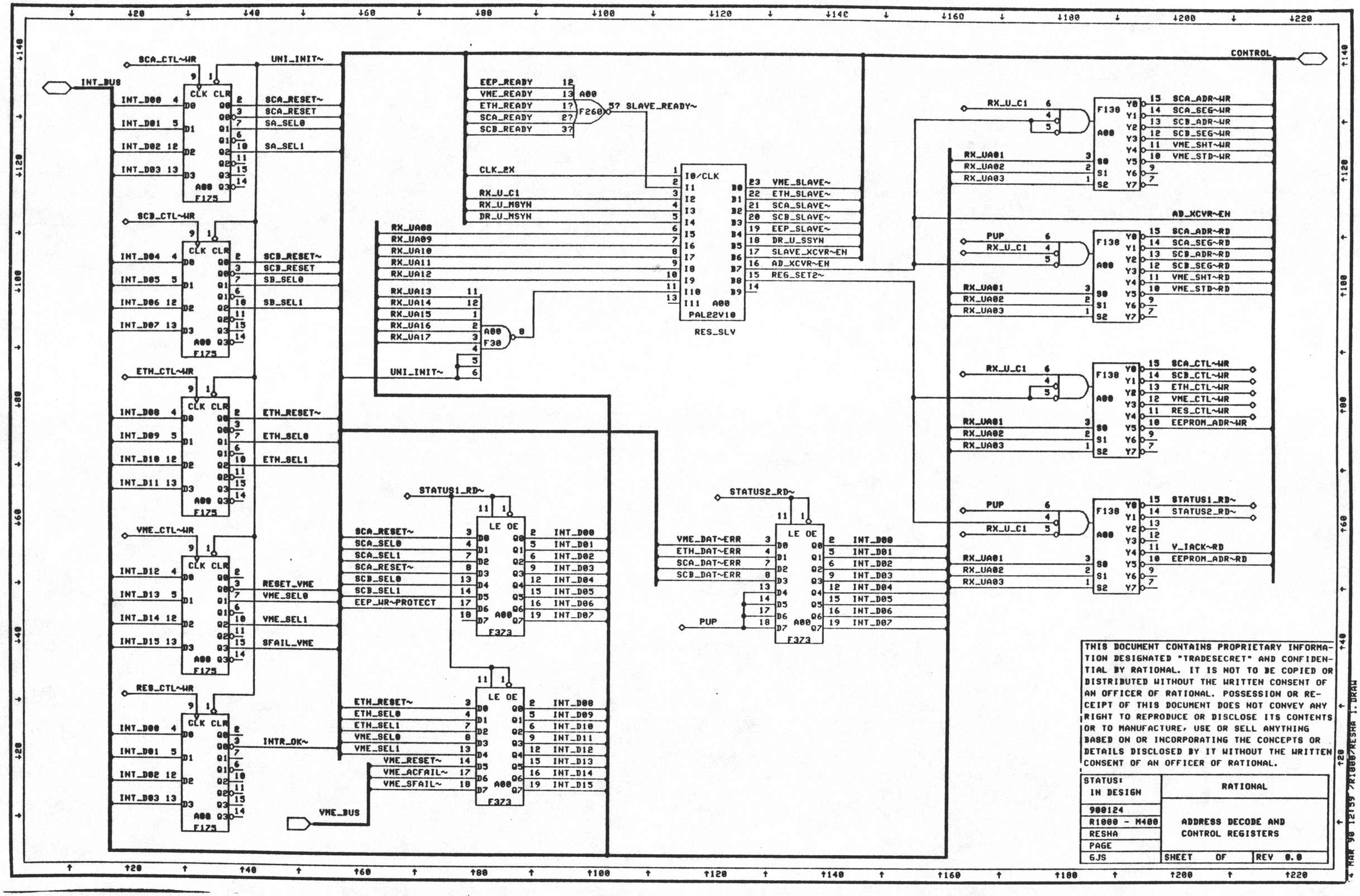
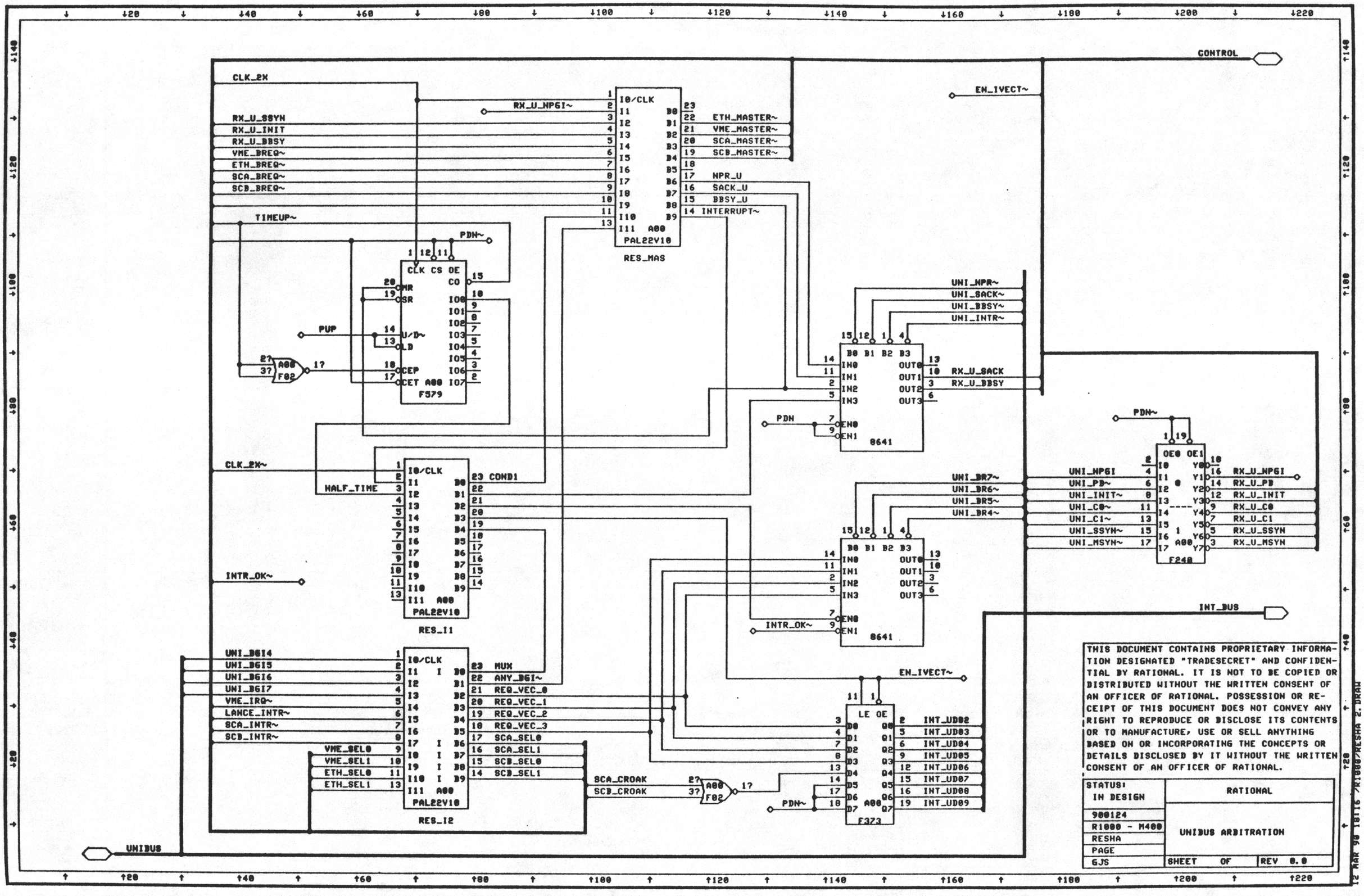
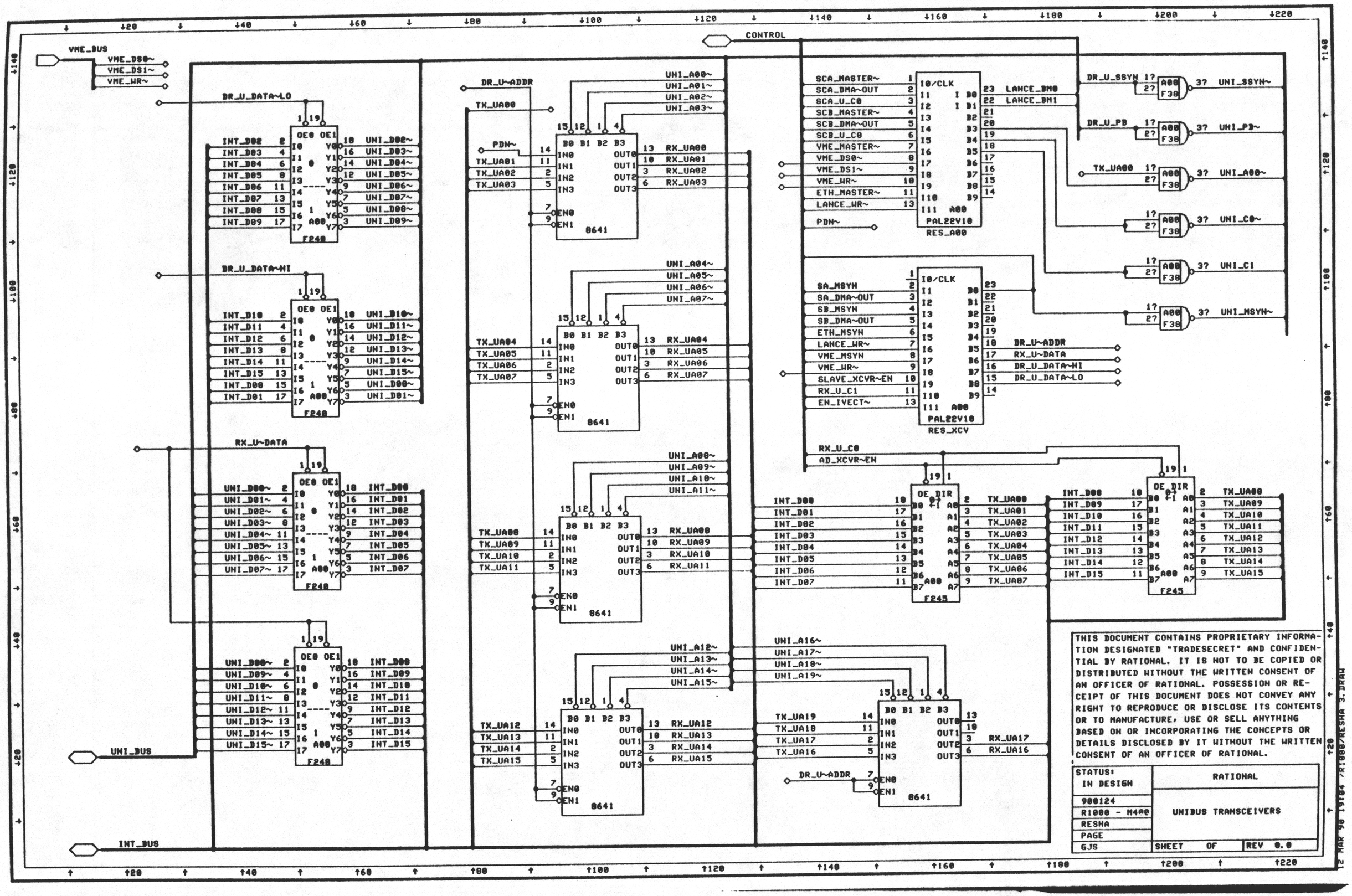


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STATUS: IN DESIGN	RATIONAL	
900124	ADDRESS DECODE AND CONTROL REGISTERS	
R1000 - M400		
RESHA		
PAGE		
GJS	SHEET OF	REV 0.0

MAR 30 12:59 '88 1000/RESHA 1.DRAW

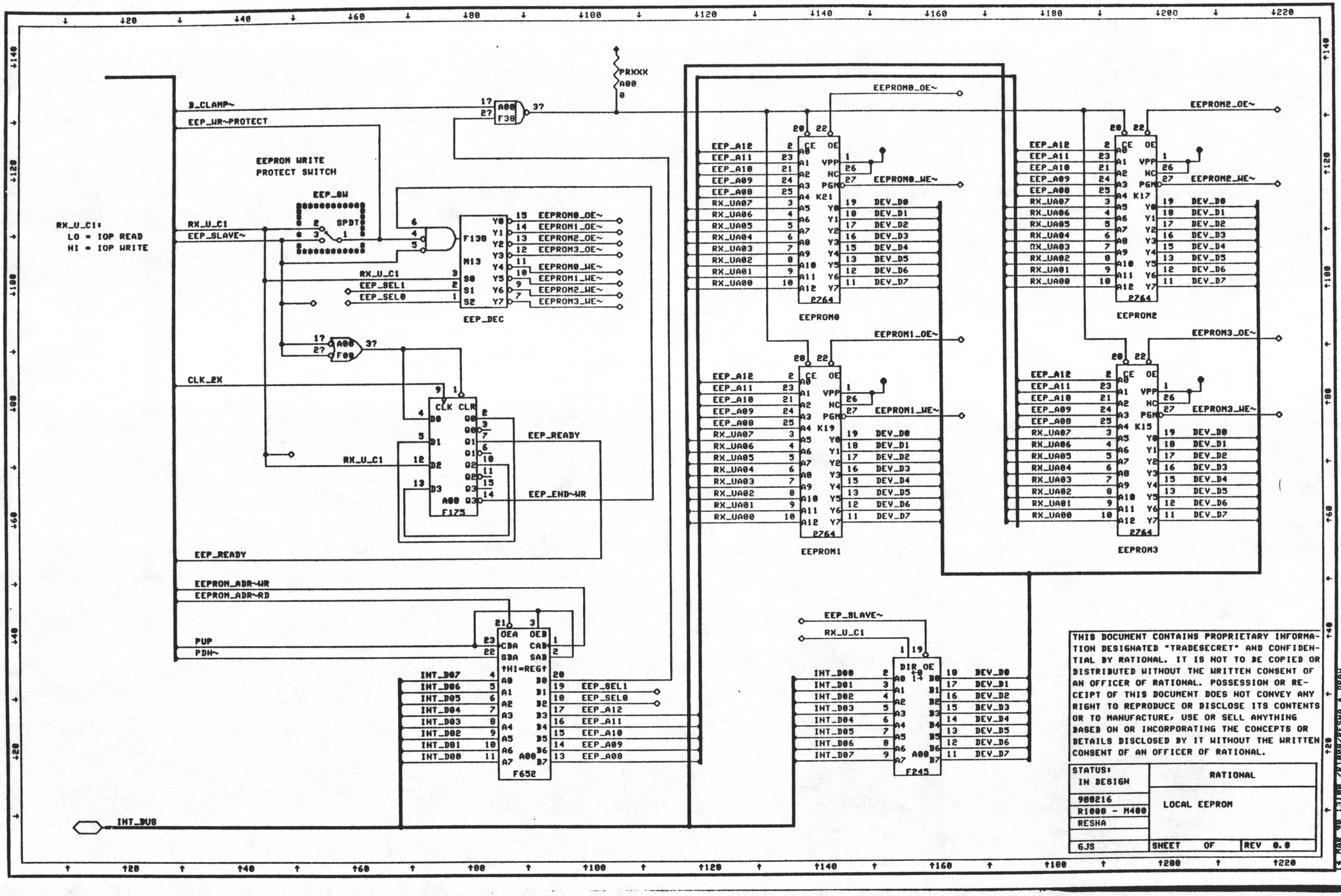

CONTROL
CLK_2X
RX_U_SSYN
RX_U_INIT
RX_U_BBSY
VME_BREQ~
ETH_BREQ~
SCA_BREQ~
SCB_BREQ~
TIMEUP~
PDN~
RX_U_NPGI~
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
A00
B0
B1
B2
B3
B4
B5
B6
B7
B8
B9
ETH_MASTER~
VME_MASTER~
SCA_MASTER~
SCB_MASTER~
NPR_U
SACK_U
BBSY_U
INTERRUPT~
PAL22V10
RES_MAS
EN_IVECT~
UNI_NPR~
UNI_SACK~
UNI_BBSY~
UNI_INTR~
B0 B1 B2 B3
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
RX_U_SACK
RX_U_BBSY
EN0
EN1
8641
CLK CS OE
CO
MR
SR
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
PUP
U/D~
LD
CEP
CET A00
F579
A00
F02
CLK_2K~
HALF_TIME
COND1
INTR_OK~
RES_I1
UNI_BG14
UNI_BG15
UNI_BG16
UNI_BG17
VME_IRQ~
LANCE_INTR~
SCA_INTR~
SCB_INTR~
VME_SEL0
VME_SEL1
ETH_SEL0
ETH_SEL1
MUX
ANY_BGI~
REQ_VEC_0
REQ_VEC_1
REQ_VEC_2
REQ_VEC_3
SCA_SEL0
SCA_SEL1
SCB_SEL0
SCB_SEL1
RES_I2
SCA_CROAK
SCB_CROAK
UNI_BR7~
UNI_BR6~
UNI_BR5~
UNI_BR4~
LE OE
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
INT_UD02
INT_UD03
INT_UD04
INT_UD05
INT_UD06
INT_UD07
INT_UD08
INT_UD09
F373
OE0 OE1
UNI_NPGI
UNI_PB~
UNI_INIT~
UNI_C0~
UNI_C1~
UNI_SSYN~
UNI_MSYN~
RX_U_NPGI
RX_U_PB
RX_U_INIT
RX_U_C0
RX_U_C1
RX_U_SSYN
RX_U_MSYN
F240
INT_BUS
UNIBUS
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STATUS: IN DESIGN
RATIONAL
900124
R1000 - M400
RESHA
PAGE
GJS
UNIBUS ARBITRATION
SHEET OF
REV 0.0
12 MAR 90 10:16 /R1000/RESHA 2.DRAW

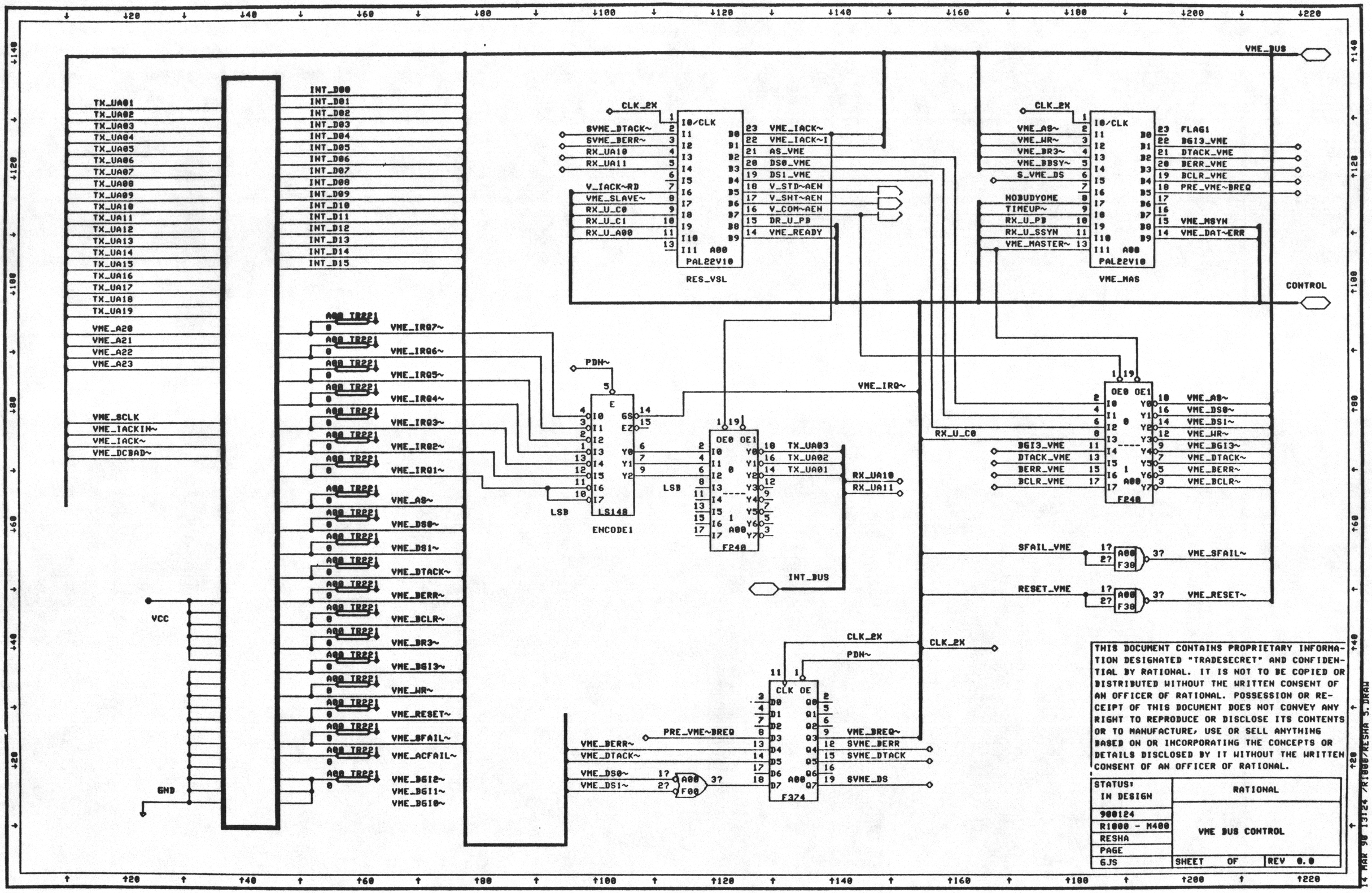


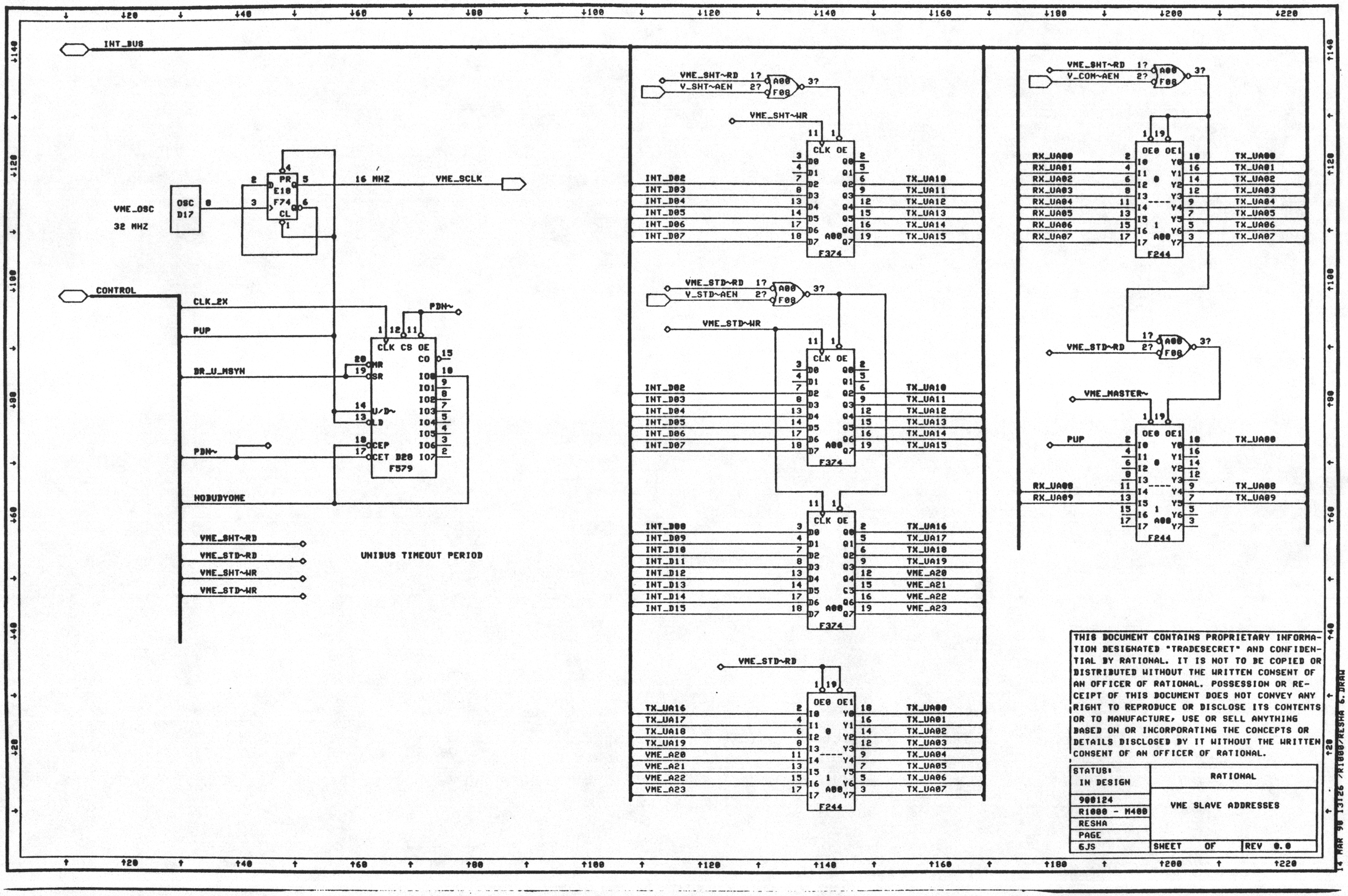
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STATUS: IN DESIGN	RATIONAL
900124	UNIBUS TRANSCEIVERS
R1000 - M400	
RESHA	
PAGE	
GJS	SHEET OF REV 0.0

12 MAR 90 19:04 /R1000/RESHA 3.DRAW


RX_U_C1:
LO = IOP READ
HI = IOP WRITE
B_CLAMP~
EEP_WR~PROTECT
EEPROM WRITE
PROTECT SWITCH
EEP_SW
SPDT
RX_U_C1
EEP_SLAVE~
EEP_SEL1
EEP_SEL0
F138
EEP_DEC
EEPROM0_OE~
EEPROM1_OE~
EEPROM2_OE~
EEPROM3_OE~
EEPROM0_WE~
EEPROM1_WE~
EEPROM2_WE~
EEPROM3_WE~
F08
CLK_2X
F175
EEP_READY
EEP_END~WR
EEPROM_ADR~WR
EEPROM_ADR~RD
PUP
PDN~
F652
INT_BUS
PRXXX
A00
0
EEP_A12
EEP_A11
EEP_A10
EEP_A09
EEP_A08
RX_UA07
RX_UA06
RX_UA05
RX_UA04
RX_UA03
RX_UA02
RX_UA01
RX_UA00
2764
EEPROM0
EEPROM1
EEPROM2
EEPROM3
DEV_D0
DEV_D1
DEV_D2
DEV_D3
DEV_D4
DEV_D5
DEV_D6
DEV_D7
F245
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STATUS: IN DESIGN
RATIONAL
980216
R1000 - M400
RESHA
LOCAL EEPROM
6JS
SHEET OF
REV 0.0
14 MAR 98 13:08 /R1000/RESHA 4.DRAW

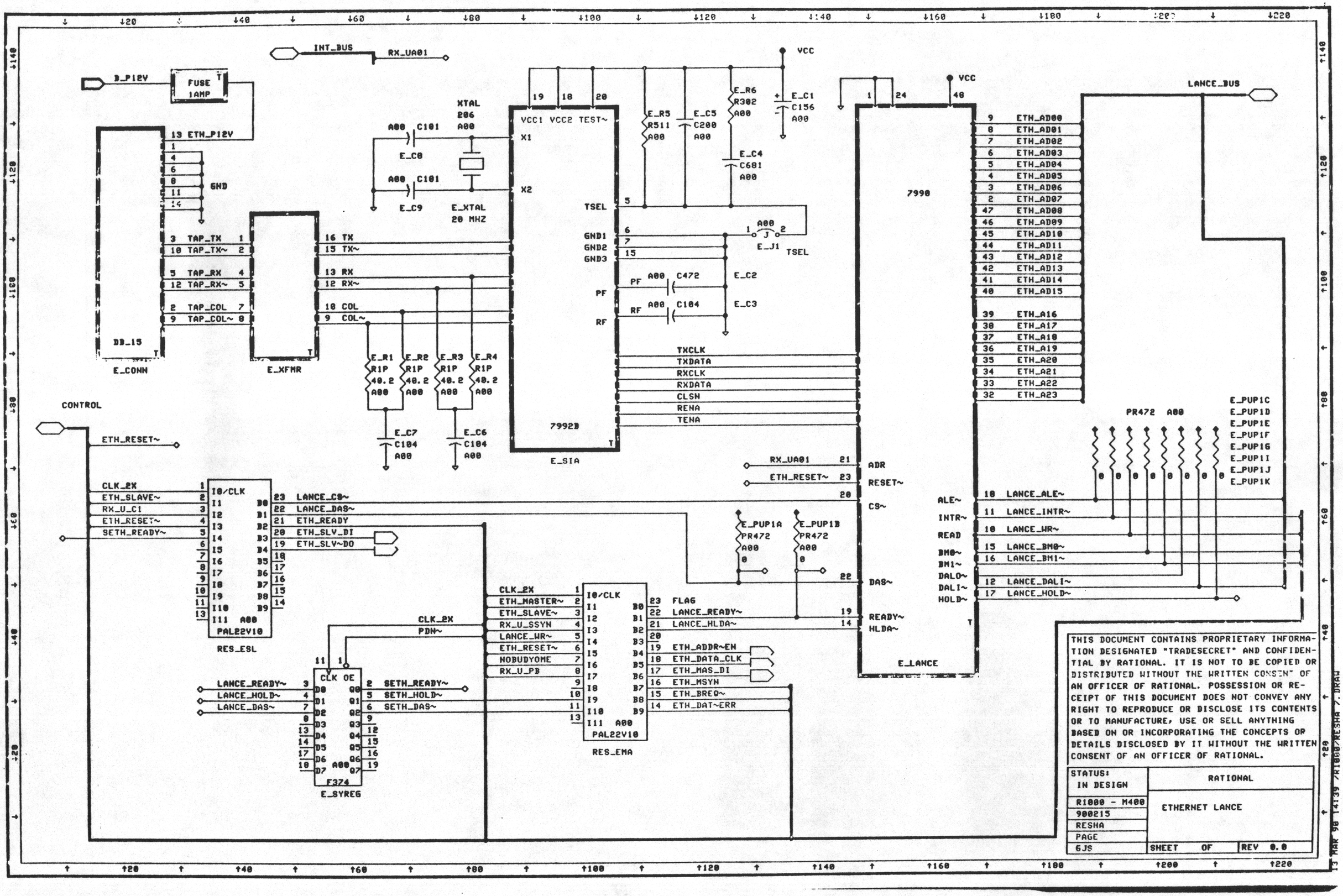

VME_BUS
CONTROL
TX_UA01
TX_UA02
TX_UA03
TX_UA04
TX_UA05
TX_UA06
TX_UA07
TX_UA08
TX_UA09
TX_UA10
TX_UA11
TX_UA12
TX_UA13
TX_UA14
TX_UA15
TX_UA16
TX_UA17
TX_UA18
TX_UA19
INT_D00
INT_D01
INT_D02
INT_D03
INT_D04
INT_D05
INT_D06
INT_D07
INT_D08
INT_D09
INT_D10
INT_D11
INT_D12
INT_D13
INT_D14
INT_D15
VME_A20
VME_A21
VME_A22
VME_A23
VME_SCLK
VME_IACKIN~
VME_IACK~
VME_DCBAD~
VCC
GND
CLK_2X
SVME_DTACK~
SVME_BERR~
RX_UA10
RX_UA11
V_IACK~RD
VME_SLAVE~
RX_U_C0
RX_U_C1
RX_U_A00
I0/CLK
PAL22V10
RES_VSL
VME_IACK~
VME_IACK~I
AS_VME
DS0_VME
DS1_VME
V_STD~AEN
V_SHT~AEN
V_COM~AEN
DR_U_PB
VME_READY
VME_AS~
VME_WR~
VME_BR3~
VME_BBSY~
S_VME_DS
NOBUDYOME
TIMEUP~
RX_U_PB
RX_U_SSYN
VME_MASTER~
VME_MAS
FLAG1
BG13_VME
DTACK_VME
BERR_VME
BCLR_VME
PRE_VME~BREQ
VME_MSYN
VME_DAT~ERR
VME_IRQ~
PDN~
ENCODE1
LS148
LSB
FP40
TX_UA03
TX_UA02
TX_UA01
RX_UA10
RX_UA11
INT_BUS
VME_IRQ7~
VME_IRQ6~
VME_IRQ5~
VME_IRQ4~
VME_IRQ3~
VME_IRQ2~
VME_IRQ1~
VME_AS~
VME_DS0~
VME_DS1~
VME_DTACK~
VME_BERR~
VME_BCLR~
VME_BR3~
VME_BG13~
VME_WR~
VME_RESET~
VME_SFAIL~
VME_ACFAIL~
VME_BG12~
VME_BG11~
VME_BG10~
SFAIL_VME
RESET_VME
F30
F00
F374
PRE_VME~BREQ
VME_BERR~
VME_DTACK~
VME_DS0~
VME_DS1~
SVME_BERR
SVME_DTACK
SVME_DS
VME_BREQ~
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STATUS: IN DESIGN
RATIONAL
900124
R1000 - M400
RESHA
PAGE
GJS
VME BUS CONTROL
SHEET OF
REV 0.0
14 MAR 90 13:24 /R1000/RESHA 5.DRAW



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STATUS: IN DESIGN	RATIONAL
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R1000 - M400	
RESHA	
PAGE 6JS	SHEET OF REV 0.0

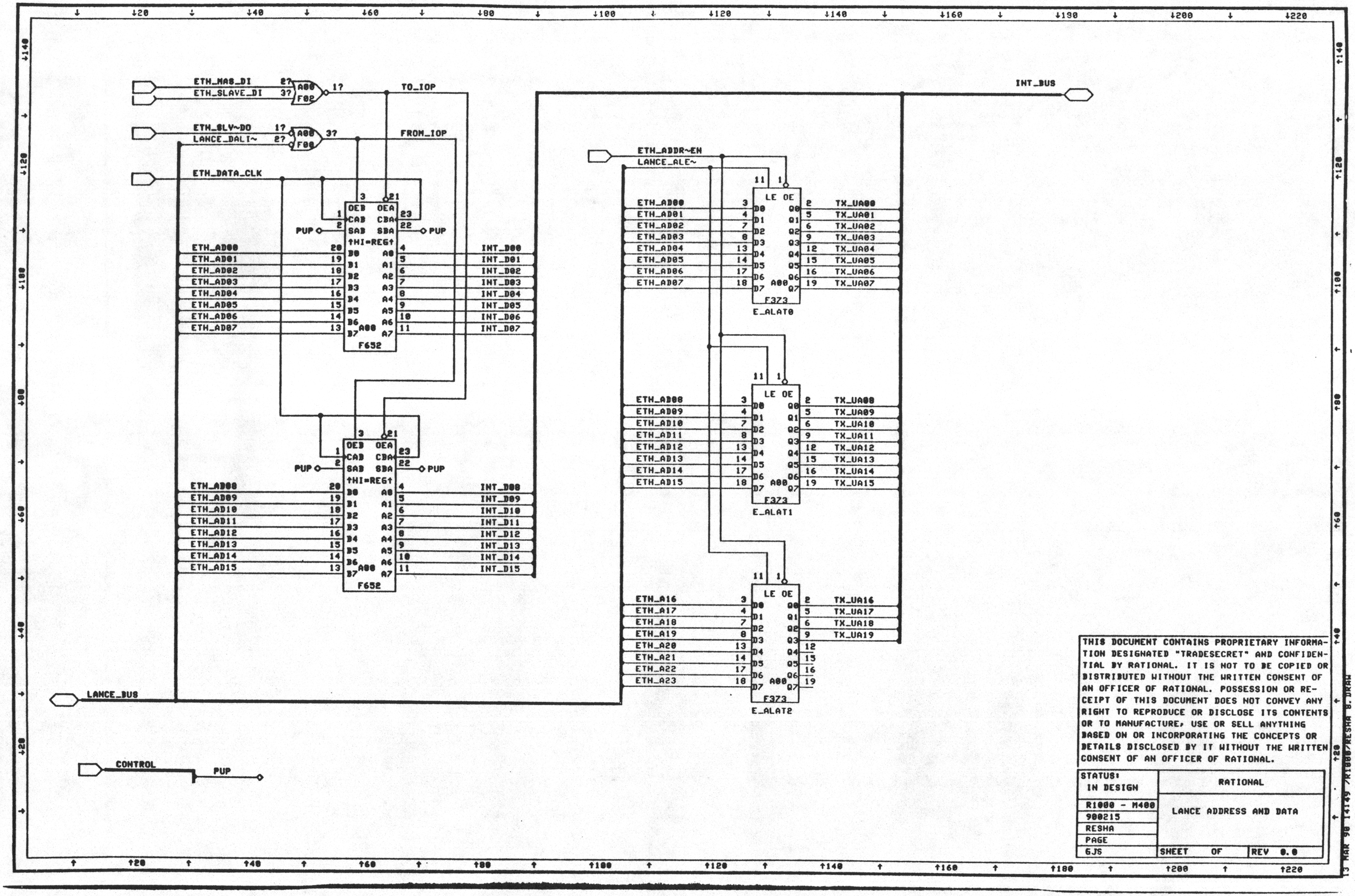
14 MAR 90 13:26 /R1000/RESHA/VME_SLAVE_ADDRESSES.DRAW



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STATUS: IN DESIGN	RATIONAL
R1000 - M400	ETHERNET LANCE
900215	
RESHA	
PAGE	
GJS	SHEET OF REV 0.0

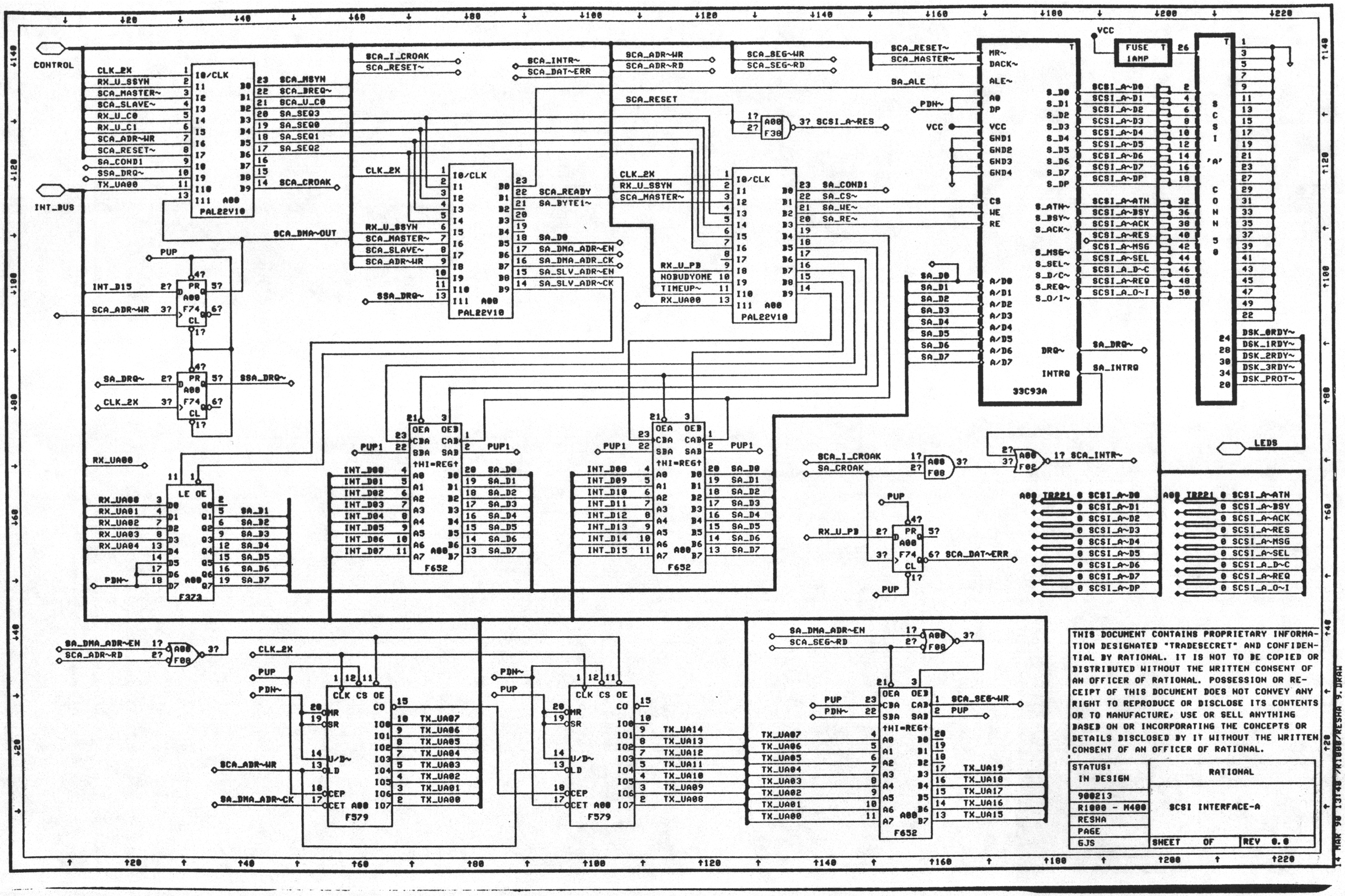
15 MAR 90 14:39 /R1000/RESHA/7.DRAW



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STATUS: IN DESIGN	RATIONAL	
R1000 - M400	LANCE ADDRESS AND DATA	
900215		
RESHA		
PAGE		
6JS	SHEET OF	REV 0.0

13 MAR 90 14:49 /R1000/RESHA B.DRAW


CONTROL
INT_BUS
PAL22V10
SCA_MSYN
SCA_BREQ~
SCA_U_C0
SA_SEQ3
SA_SEQ0
SA_SEQ1
SA_SEQ2
SCA_CROAK
SCA_DMA~OUT
SCA_I_CROAK
SCA_RESET~
SCA_INTR~
SCA_DAT~ERR
SCA_ADR~WR
SCA_ADR~RD
SCA_SEG~WR
SCA_SEG~RD
SCA_RESET~
SCA_MASTER~
SA_ALE
SCA_RESET
PDN~
VCC
SCSI_A~RES
SA_COND1
SA_CS~
SA_WE~
SA_RE~
SA_READY
SA_BYTE1~
SA_D0
SA_DMA_ADR~EN
SA_DMA_ADR_CK
SA_SLV_ADR~EN
SA_SLV_ADR~CK
SSA_DRQ~
RX_U_PB
NOBUDYOME
TIMEUP~
RX_UA00
INT_D15
PUP
PR
CL
F74
A00
SA_DRQ~
CLK_2X
SSA_DRQ~
RX_UA00
LE OE
F373
PUP1
INT_D00
INT_D01
INT_D02
INT_D03
INT_D04
INT_D05
INT_D06
INT_D07
INT_D08
INT_D09
INT_D10
INT_D11
INT_D12
INT_D13
INT_D14
F652
SA_D0
SA_D1
SA_D2
SA_D3
SA_D4
SA_D5
SA_D6
SA_D7
SA_DP
SA_ATN~
SA_BSY~
SA_ACK~
SA_RES
SA_MSG~
SA_SEL~
SA_D/C~
SA_REQ~
SA_I/O~
SA_INTRQ
33C93A
FUSE 1AMP
SCSI_A~D0
SCSI_A~D1
SCSI_A~D2
SCSI_A~D3
SCSI_A~D4
SCSI_A~D5
SCSI_A~D6
SCSI_A~D7
SCSI_A~DP
SCSI_A~ATN
SCSI_A~BSY
SCSI_A~ACK
SCSI_A~RES
SCSI_A~MSG
SCSI_A~SEL
SCSI_A_D~C
SCSI_A~REQ
SCSI_A_O~I
SCSI 'A' CONN 50
DSK_0RDY~
DSK_1RDY~
DSK_2RDY~
DSK_3RDY~
DSK_PROT~
LEDS
TR221
TX_UA00
TX_UA01
TX_UA02
TX_UA03
TX_UA04
TX_UA05
TX_UA06
TX_UA07
TX_UA08
TX_UA09
TX_UA10
TX_UA11
TX_UA12
TX_UA13
TX_UA14
TX_UA15
TX_UA16
TX_UA17
TX_UA18
TX_UA19
CLK CS OE
F579
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STATUS: IN DESIGN
900213
R1000 - M400
RESHA
PAGE
GJS
RATIONAL
SCSI INTERFACE-A
SHEET OF
REV 0.0
14 MAR 90 13:48 /R1000/RESHA/SCSI_A.DRAW

UNI_BUS

UNI_D15~ UNI_D14~ UNI_D13~ UNI_D12~ UNI_D11~ UNI_D10~ UNI_D09~ UNI_D08~ UNI_D07~ UNI_D06~ UNI_D05~ UNI_D04~ UNI_D03~ UNI_D02~ UNI_D01~ UNI_D00~

UNI_A19~ UNI_A18~ UNI_A17~ UNI_A16~ UNI_A15~ UNI_A14~ UNI_A13~ UNI_A12~ UNI_A11~ UNI_A10~ UNI_A09~ UNI_A08~ UNI_A07~ UNI_A06~ UNI_A05~ UNI_A04~ UNI_A03~ UNI_A02~ UNI_A01~ UNI_A00~

UNI_NPR~ UNI_NPGI

UNI_BR7~ UNI_BR6~ UNI_BR5~ UNI_BR4~ UNI_BGI7 UNI_BGI6 UNI_BGI5 UNI_BGI4

UNI_SACK~ UNI_BBSY~ UNI_MSYN~ UNI_INTR~ UNI_SSYN~ UNI_C1~ UNI_C0~ UNI_PA~ UNI_PB~

UNI_INIT~ UNI_ACLO~ UNI_DCLO~

B_P12V B_M12V

GND

VCC

TC A00 CT1 TC A00 CT2 TC A00 CT3 TC A00 CT4

TC A00 TC A00 TC A00 TC A00

SERCOM_BUS

B_CONS_DCD B_CONS_DSR B_CONS_CTS B_CONS_RXD B_CONS_TXD_TTL B_CONS_RTS_TTL B_CONS_DTR_TTL B_MODEM_DCD B_MODEM_DSR B_MODEM_CTS B_MODEM_RXD B_MODEM_TXD_TTL B_MODEM_RTS_TTL B_MODEM_DTR_TTL

BYTE_BUS

B_EXT_D0 B_EXT_D1 B_EXT_D2 B_EXT_D3 B_EXT_D4 B_EXT_D5 B_EXT_D6 B_EXT_D7

B_EXT~WR B_EXT~RD

B_EXT~CS B_EXT_A11 B_EXT_A10 B_EXT_A09 B_EXT~LEVEL1 B_EXT~LEVEL6 B_EXT_ID0 B_EXT_ID1 B_EXT_ID2

CONTROL

B_CLAMP~ B_RESET~ B_RESET B_PS0_ENABLE B_PS0_ADJUST B_PS0~ACFAIL B_PWR_MARGIN B_MARGIN_HI B_MARGIN_LO B_IOP_EPO B_CLK_MARGIN B_FP_LED0 B_FP_LED1 B_FP_LED2 B_FP_LED3 B_CPU_RUNNING B_IOP_RUNNING B_IOP_HALT B_DCH_ACTIVE B_FP_SWITCH B_TEMP_REF B_TEMP_SENSE

PR222 A00 PUP0 PUP1 PUP2 PUP3 PUP4 PUP5

PR222 A00 PDN0 PDN1

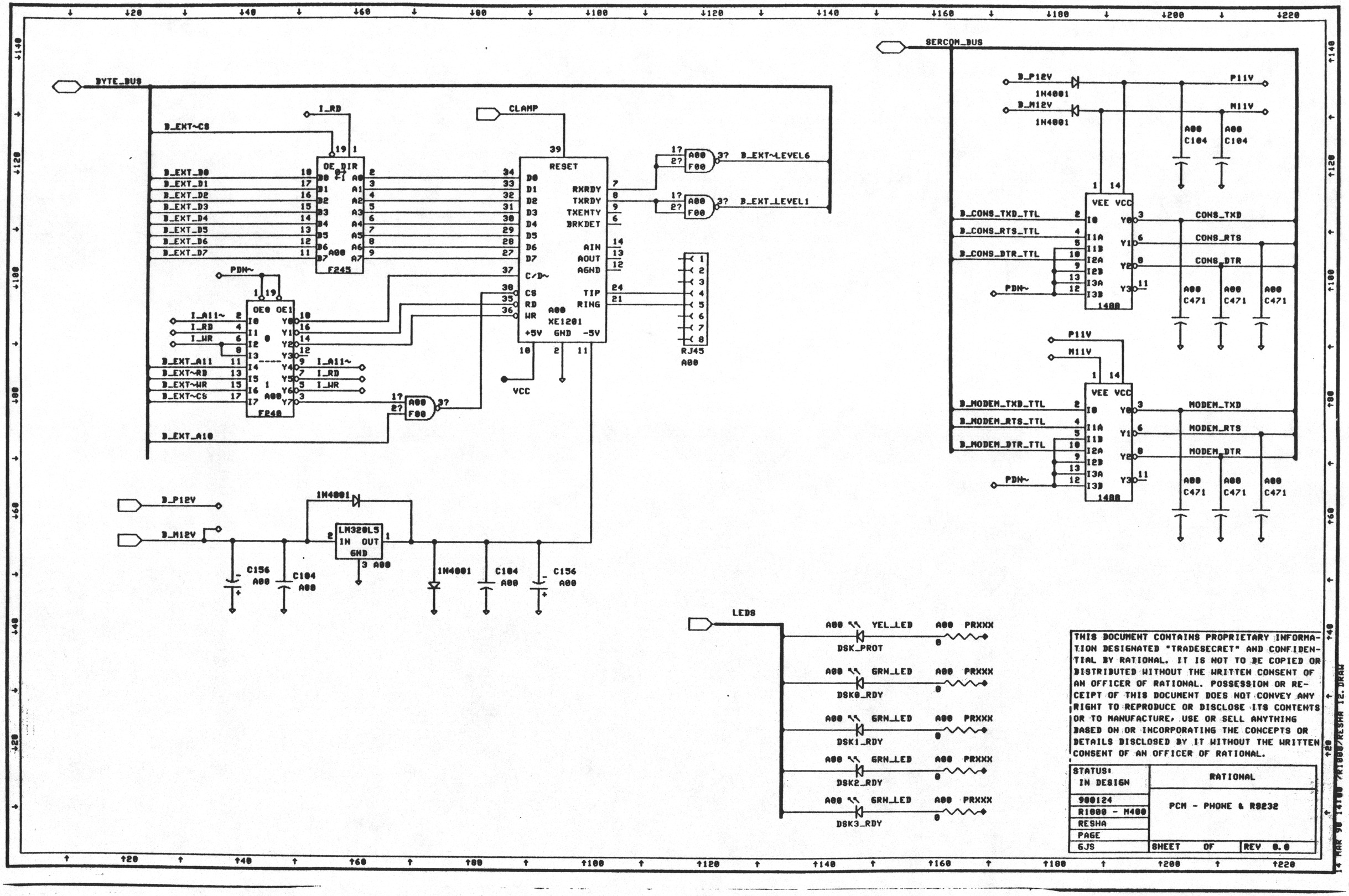
B_CLK_2X A00 1804 CLK_2X_B0 CLK_2X_B1 CLK_2X_B2

B_CLK~2X

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STATUS: IN DESIGN	RATIONAL
900221	BACK PANEL CONNECTIONS
R1000 - M400	
RESHA	
PAGE	
GJS	SHEET OF REV 0.0

14 MAR 90 13:43 /R1000/RESHA 11.DRAW



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STATUS: IN DESIGN	RATIONAL
900124	PCM - PHONE & RS232
R1000 - M400	
RESHA	
PAGE	
6JS	SHEET OF REV 0.0

14-MAR-90 14:00 /R1000/RESHA/12.DRAW