R1000 Systems

For the R1000 systems there were 4 "Series" created; 100, 200, 300 and 400. With the progression to each new system the changes were mainly in the IO area, and the packaging changes enabled by these changes. The packaging changes, smaller physical frame size, was mostly a function of Disk /Tape Drive sizes.

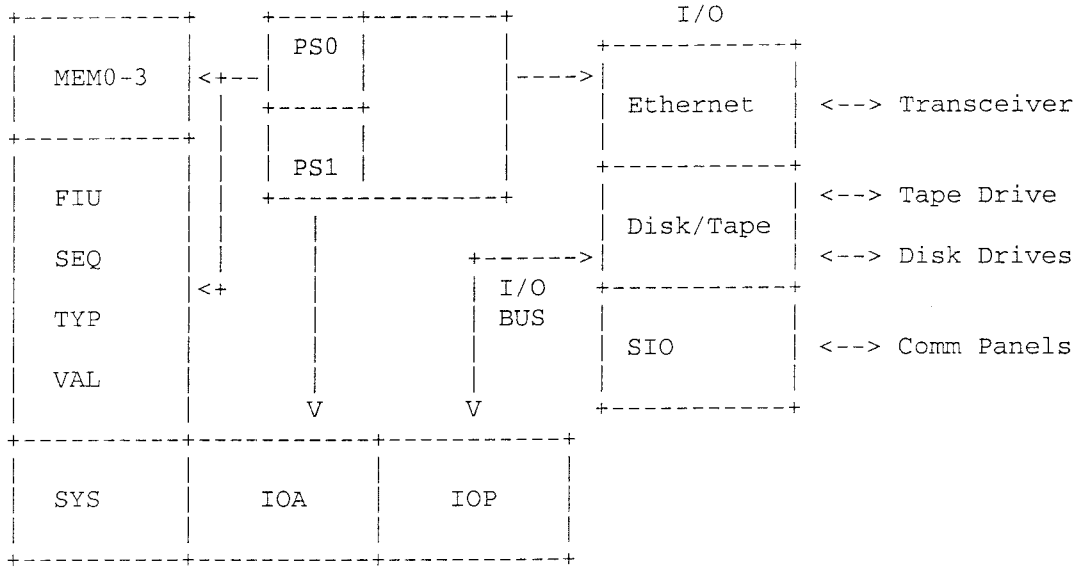
An R1000 system can be broken up into several major functional blocks. The R1000 module is composed of several boards which are the CPU and Memory. The R1000 does not directly control its peripherals, rather issues commands to the I/O Processor module which directly communicates with the peripheral controller boards located in the I/O cardcage. The path which the R1000 takes to communicate with the IOP is through the I/O Adapter module, which functionally has control over all modules in the system, and is the first active module in the boot process, providing the physical interface to the operations console and diagnostic modem, running self tests on all modules (IOA, IOP, R1000 boards, etc...) and controlling the power to the R1000 board.

The IOP and IOA reside on separate boards on the series 100. On the series 200 and later, the IOP, IOA, and SYSBUS modules all reside on a single board called the I/O Controller (IOC). With the 400 Series the system moved from the use of third-party peripheral controller boards, to implementing these functions on our own board. The new board being the RESHA.

Across the Series, the CPU itself has not really changed. The CPU is based on TTL logic. With the creation of the Series 400, the edge connectors were changed.

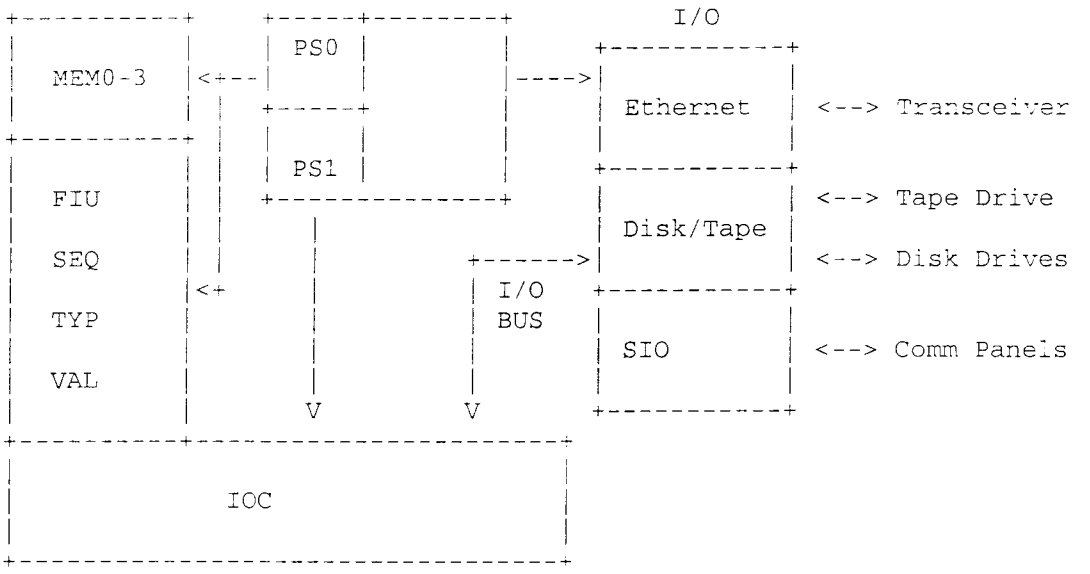
Following are some basic diagrams of the different Systems. More detail information can be found for the 200 through 400 in the System Manager's Guide.

SERIES 100


I/O
PS0
MEM0-3
Ethernet
<--> Transceiver
PS1
FIU
Disk/Tape
<--> Tape Drive
SEQ
<--> Disk Drives
I/O
BUS
TYP
SIO
<--> Comm Panels
VAL
SYS
IOA
IOP

SERIES 200 /300

Main change was to consolidate the SYS,IOA and IOP into the new IOC board.

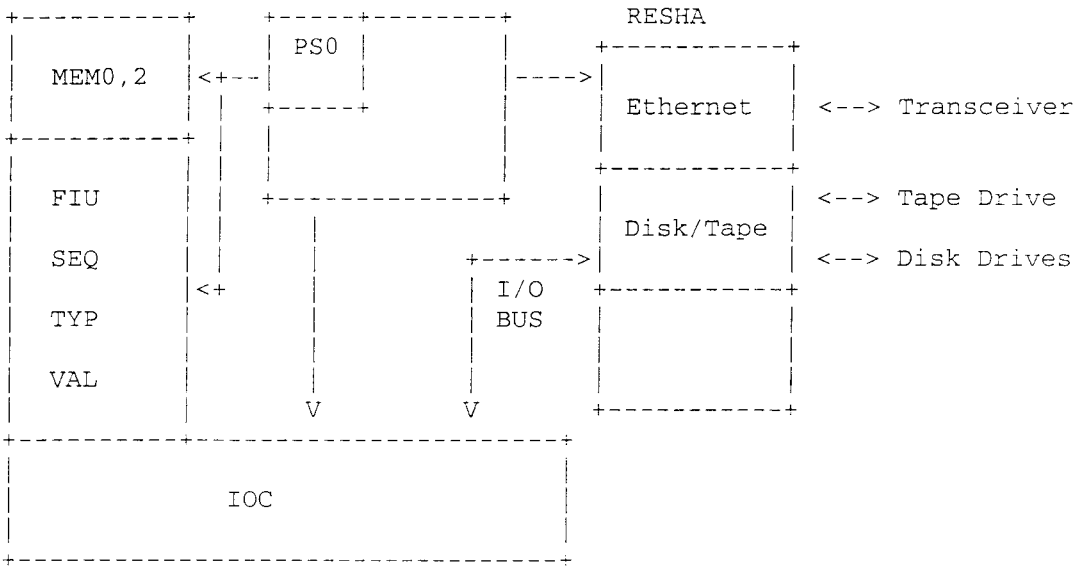


SERIES 300

Introduced 32 meg memory boards, allowing systems to have up to 64 meg of memory. Moved to using 8mm tape drive as standard tape unit. Disk drive in separate frame, and system could be setup to either use local disk, or access drives on another server over a "coprocessor" link.

SERIES 400

Introduced Resha Board that implement all IO. System only supported 32 meg memory boards. A coprocessor version was initially implemented by due to lack of interest and complexities of implementation it was dropped. Moved to SCSI disk drives.



Series 400 Boards Set

The R1000 processor is composed of a CPU board set and memory. The boards are housed in the R1000 board section and have both a backplane and a foreplane. Access to the boards requires removal of the foreplane. The location of the boards, when viewing the system from the front, and starting from the left to right are:

CPU Board Set

Slot	Board	Description
1	Mem2	Memory 2 (32 meg)
2	Mem0	Memory 0 (32 meg)
3	FIU	Field Isolation Unit
4	SEQ	Sequencer
5	TYP	Type
6	VAL	Value
7	IOC	I/O Controller

To the right of the CPU boards is the RESHA. This card connects only through the backplane and does not share the foreplane. The RESHA implements the connection and communication to peripherals. The front edge of the RESHA is the Input/Output Panel that contains:

- Two RS232 ports (Comm and operator's console)
- network ports
- Other assorted devices interfaces, switches and status LEDs.

RESHA (Rational Ethernet SCSI Host Adapter)

All I/O in one. Contains SCSI controller for Disk and Tape drive, Control Panel logic, VMEGEN board for CMC Ethernet Controller, PCM functions, Diagnostic Modem, "White Button", EEPROM that contains Bootstrap Software (Disk, Tape)and Self-test.

IOC (Input/Output Controller)

I/O Processor (68020)
I/O Processor Memory
Memory Error Correction
Microaddress Trace RAM
Bus Control Logic
IO bus Generation
Operator Console Interface
EEPROM – containing
  IOC selftest
  Bootstrap manager (Boot/Crash options and IOP configuration)
  NOVRAM that holds IOC serial number, cluster ID, etc...
  Battery and Clock/Calendar Chip

VAL (Value)
Responsible for VALUE calculations
Contains 16 x 16 multiplier, 64-bit Arithmetic/Logical Unit
1K x 64 Bit Register File (Includes control Stack accelerator)

TYP (Type)
Contains Type checking hardware
Memory address register
64-bit Arithmetic/Logical Unit
1K x 64 Bit Register File (Includes control Stack accelerator)

SEQ (Sequencer)
Macro-instruction processing
Micro-instruction sequencing

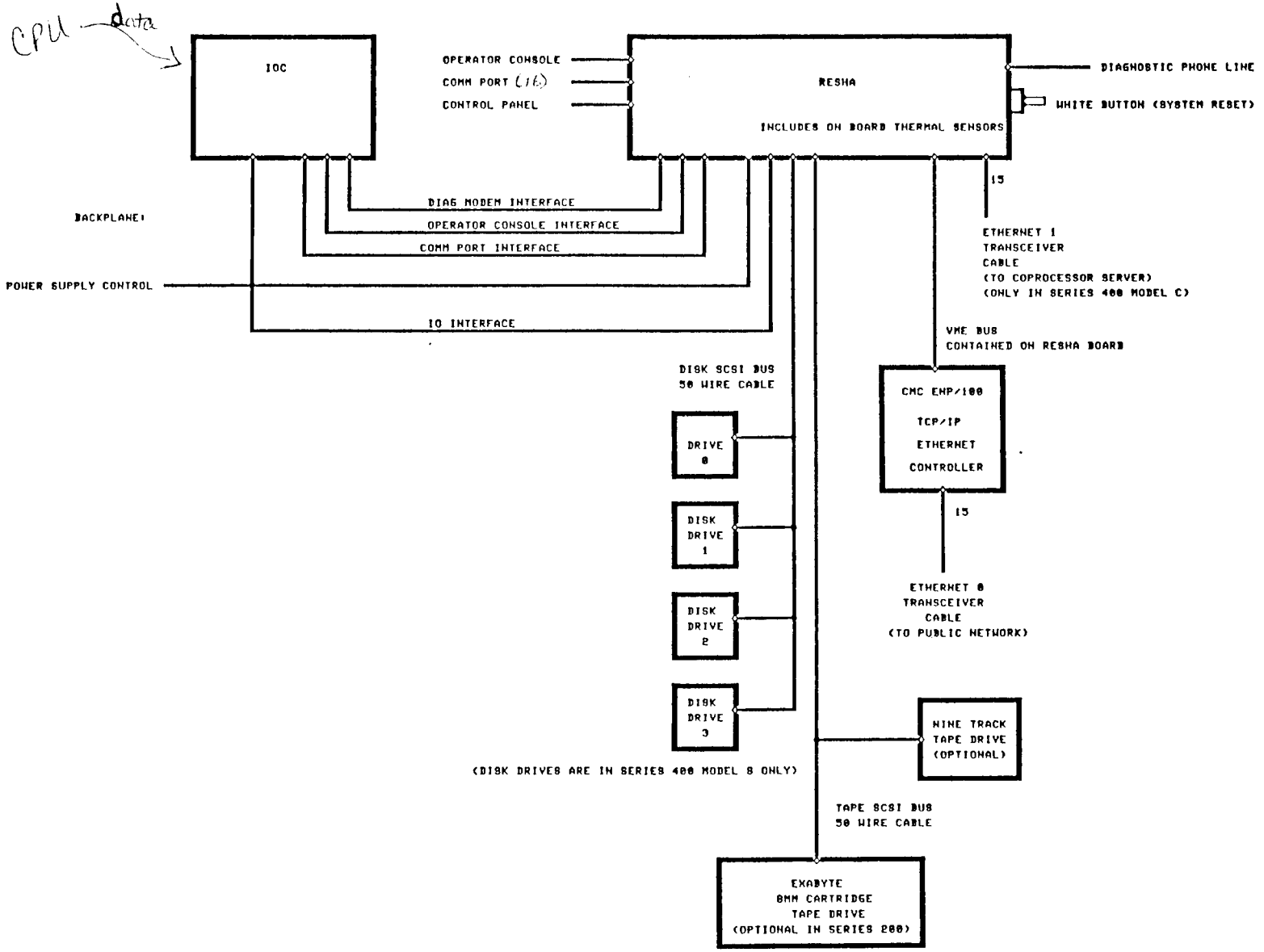
FIU (Field Isolation Unit)
Contains Control Stack Accelerator logic
Memory Control logic
64 into 128 Bit Field Insertion
128 to 64 Bit Field Extraction

MEM32 (32 MB Memory)
Main memory for system, one board required for a total of 32 MB, organized in words of 137 bits (128 data bits and 9 ECC bits)
Memory is divided into 1024 byte pages
Memory boards response directly to Virtual Addresses

Tape Drive
The series 400 makes use of an Exabyte EXB-8200 8mm tape drive. The system is setup to house on one of these drives.

Disk Drives
The series 400 makes use of 5-1/4 Inch SCSI disk drives. The system driver software is limited to support of only the Fujitsu M2266 drive. The drives are mounted on a special series 400 specific carrier that allows for them to be easily installed and removed from the systems disk backplane. The system will support up to four drives on the backplane. The position of the drive on the backplane determines unit number.

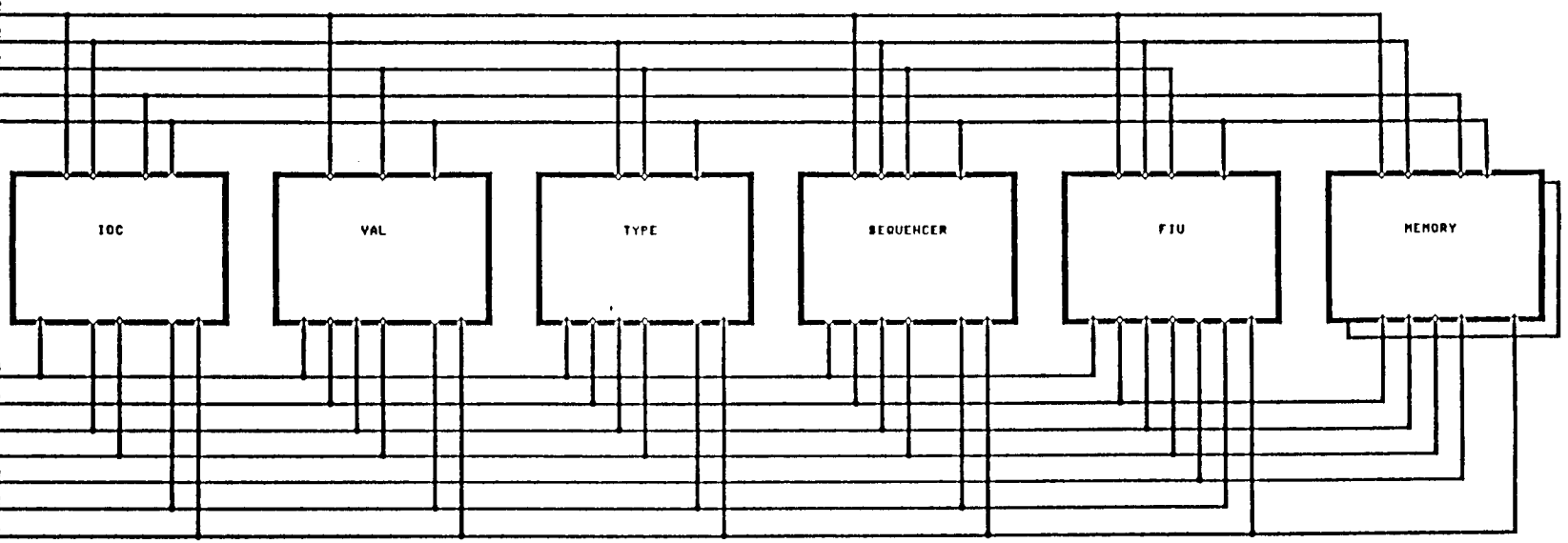
DC Power
One Power Supply
PS0 for CPU and Peripherals +5VDC, +12VDC, -12VDC



STATUS:	RATIONAL
17-SEP-90	R1000 IO DIAGRAM
R1000	SERIES 400
	SHEET 1 OF 1 REV 0.0

FOREPLANE:

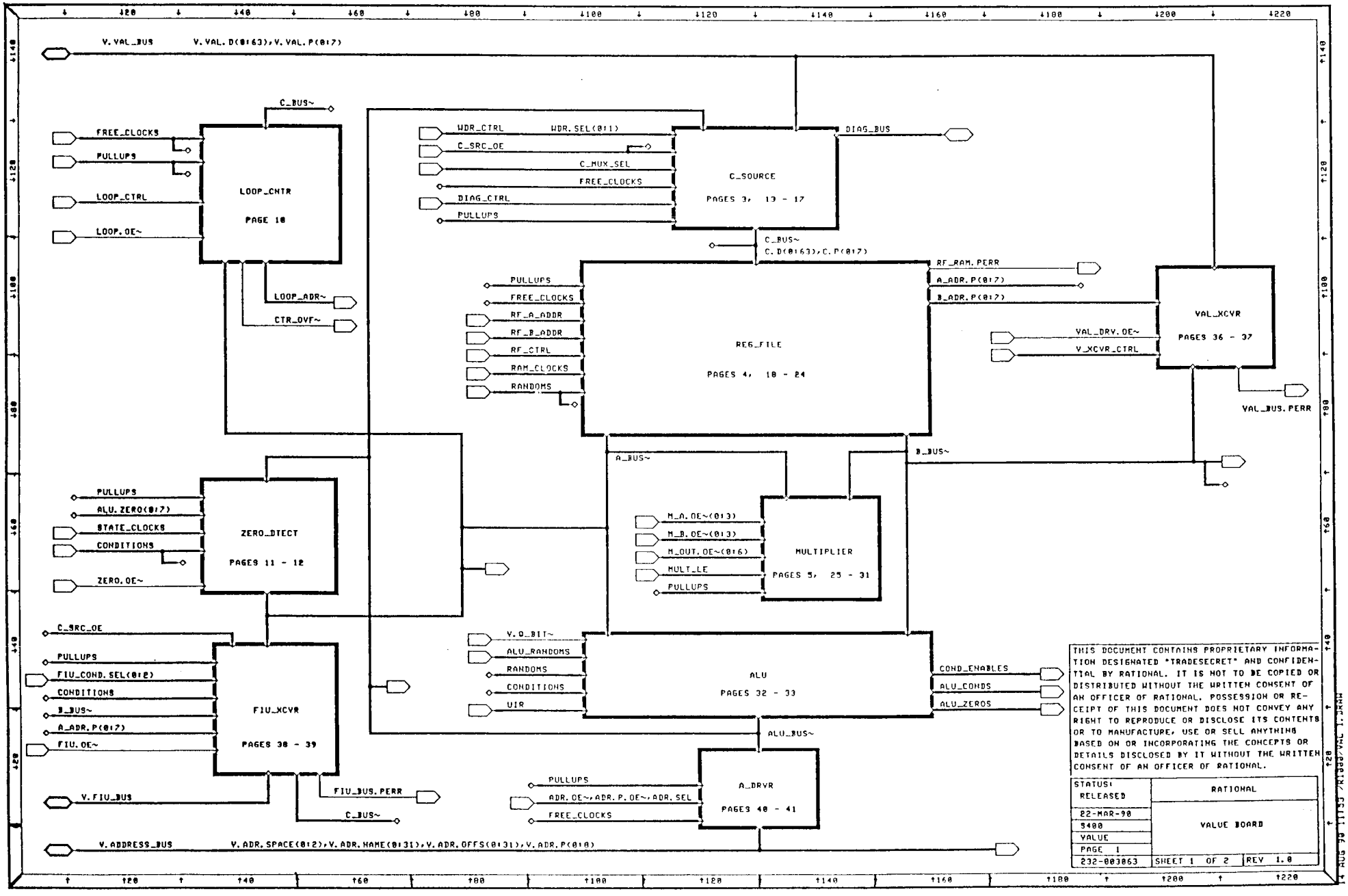
VAL(0:63),VP(0:7) 72
TYP(0:63),TP(0:7) 72
FIU(0:63),FP(0:7) 72
CHECK_BITS(0:8) 9
BUS CONTROL SIGNALS 9



BACKPLANE:

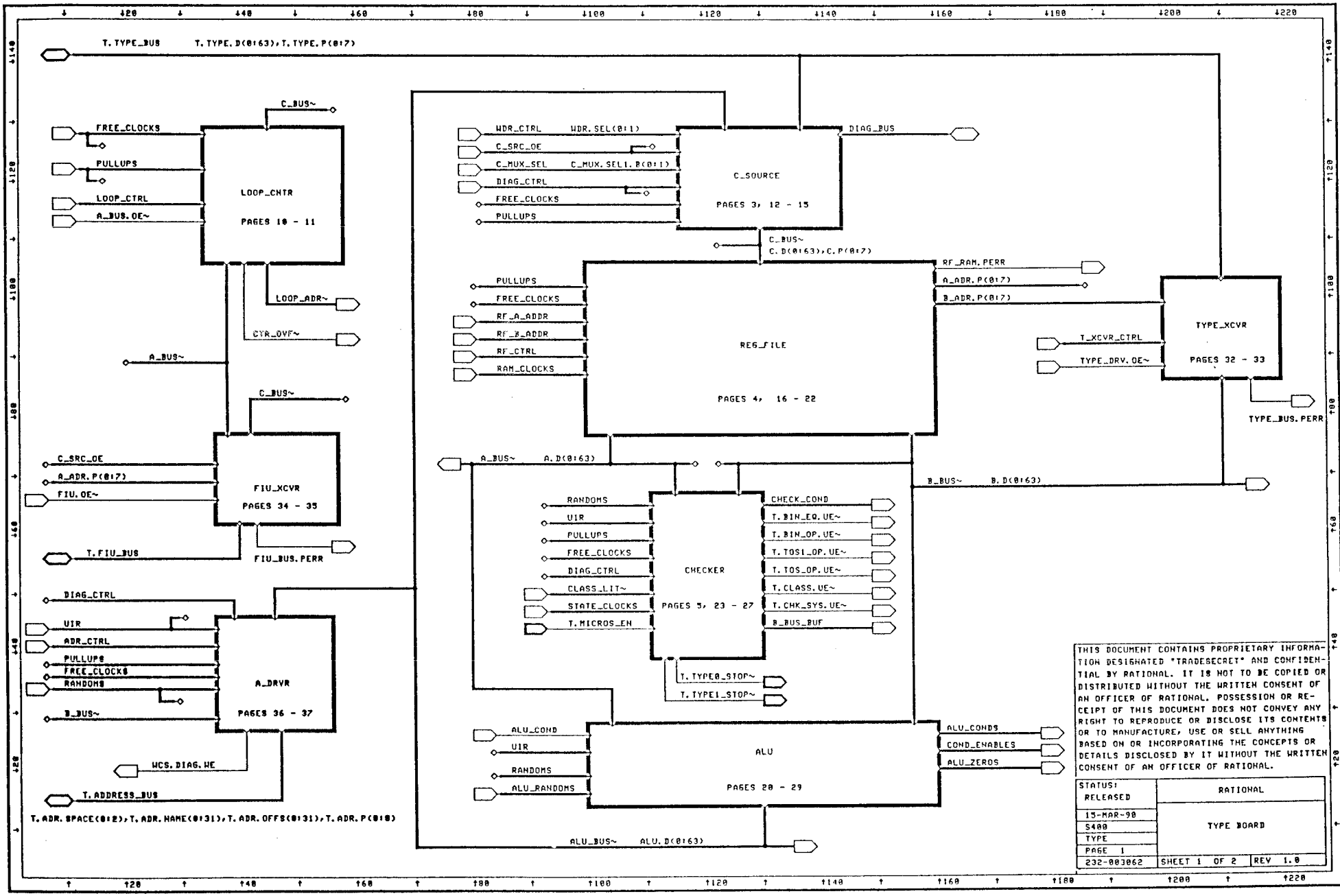
UABR(0:13),UABRP 15
ABBR(0:66),ABBR.P(0:8) 76
CLOCKS 3
DIAGNOSTIC CONN 2
MEMORY CONTROL 10
CONDITIONS 12
DC POWER 64

STATUS:	RATIONAL
17-SEP-90	R1000 CPU
R1000	INTERCONNECT DIAGRA
	SHEET 1 OF 1 REV 0.

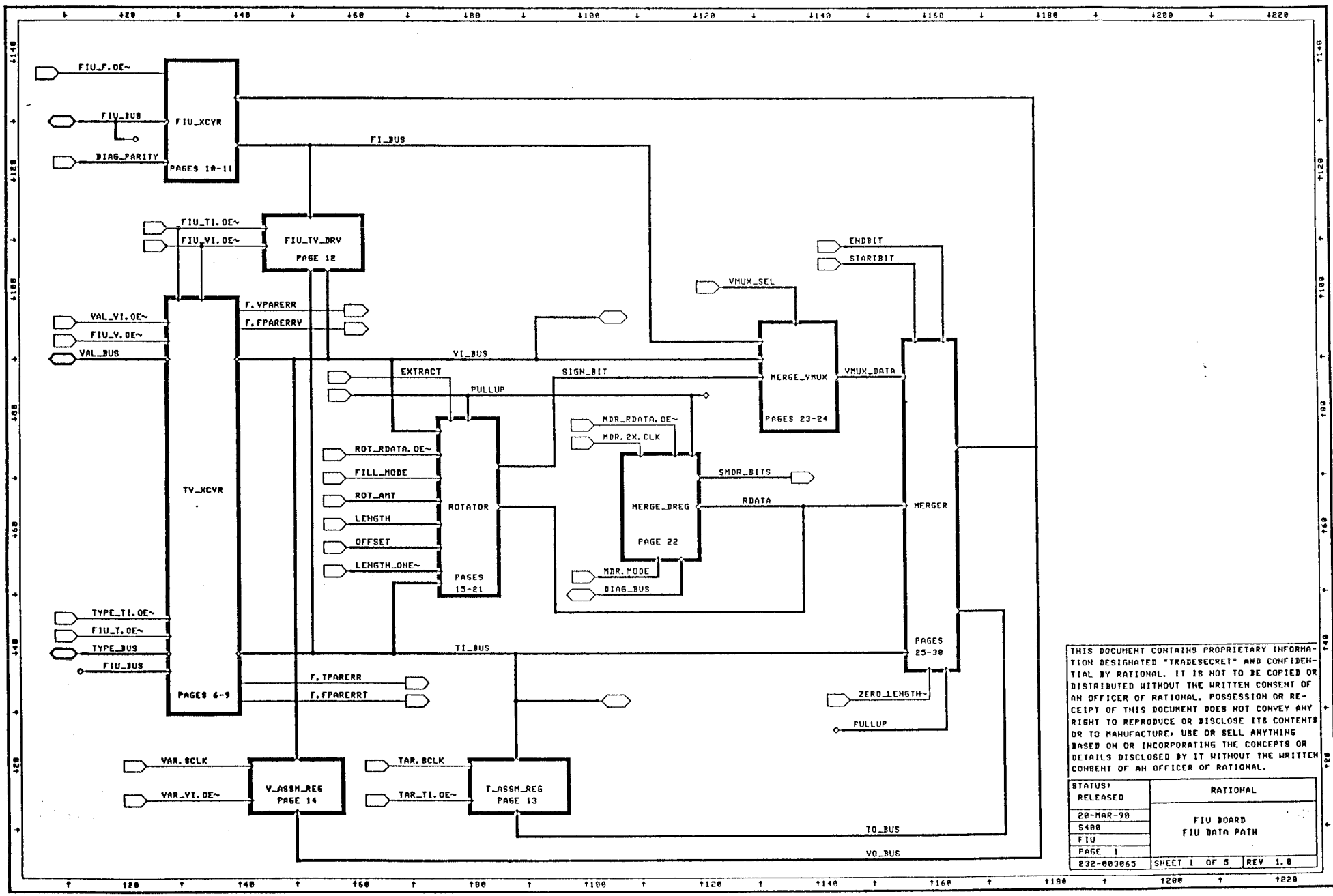


STATUS: RELEASED	RATIONAL
22-MAR-90	VALUE BOARD
9400	
VALUE	
PAGE 1	
232-003863	SHEET 1 OF 2 REV 1.0

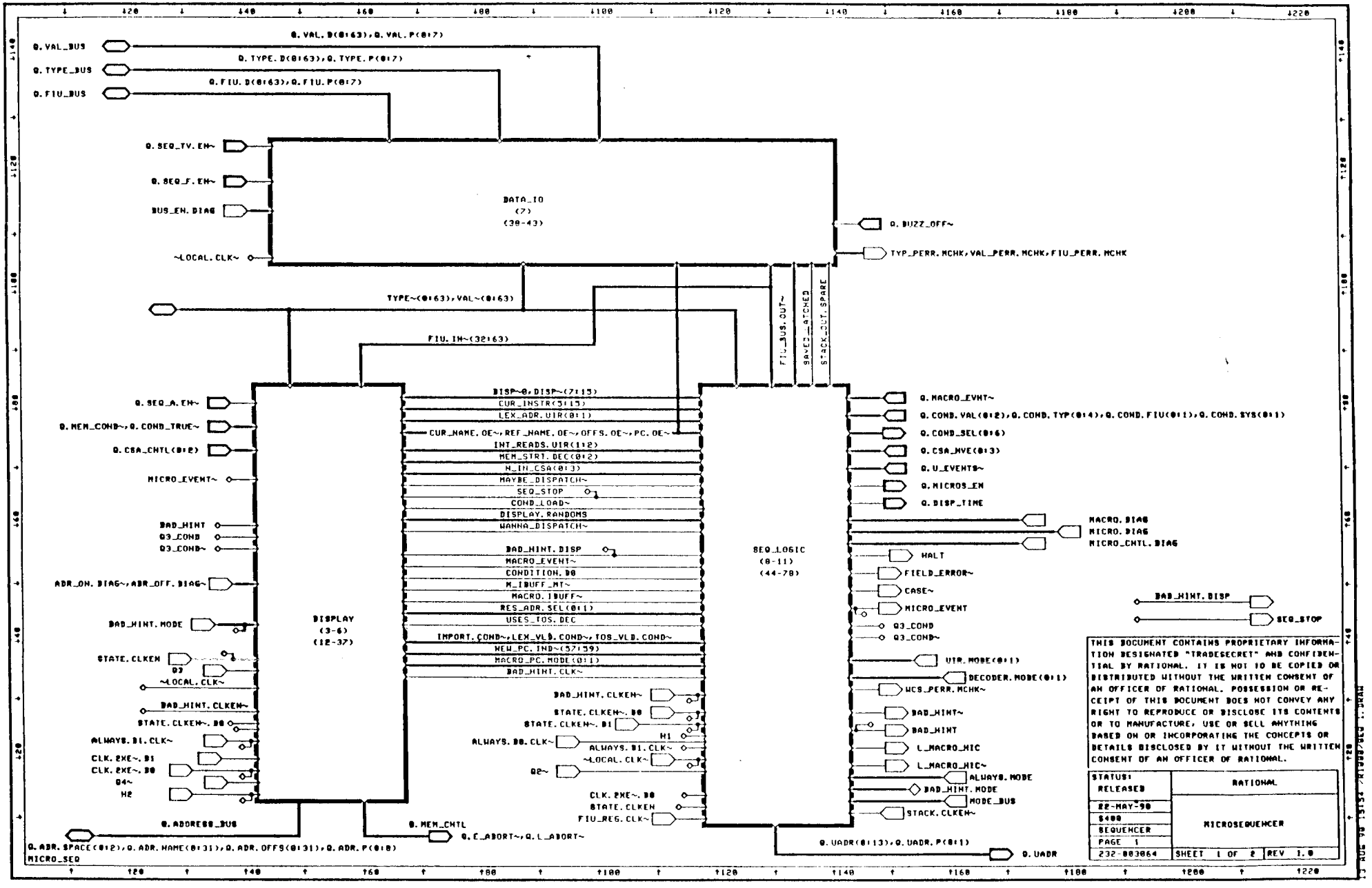
14-AUG-90 11:55 /RATS/VAL 1.MNT



STATUS: RELEASED	RATIONAL
15-MAR-90	TYPE BOARD
S400	
TYPE	
PAGE 1	
232-003062	SHEET 1 OF 2 REV 1.0



STATUS: RELEASED	RATIONAL
20-MAR-90	FIU BOARD FIU DATA PATH
S400	
FIU	
PAGE 1	
232-003065	SHEET 1 OF 5 REV 1.0


Q.VAL_BUS
Q.VAL.D(0:63),Q.VAL.P(0:7)
Q.TYPE_BUS
Q.TYPE.D(0:63),Q.TYPE.P(0:7)
Q.FIU_BUS
Q.FIU.D(0:63),Q.FIU.P(0:7)
Q.SEQ_TV.EN~
Q.SEQ_F.EN~
BUS_EN.DIAG
~LOCAL.CLK~
DATA_IO
(7)
(38-43)
Q.BUZZ_OFF~
TYP_PERR.MCHK,VAL_PERR.MCHK,FIU_PERR.MCHK
TYPE~(0:63),VAL~(0:63)
FIU.IN~(32:63)
FIU_BUS.OUT~
SAVED_LATCHED
STACK_OUT.SPARE
Q.SEQ_A.EN~
Q.MEM_COND~,Q.COND_TRUE~
Q.CSA_CNTL(0:2)
MICRO_EVENT~
BAD_HINT
Q3_COND
Q3_COND~
ADR_ON.DIAG~,ADR_OFF.DIAG~
BAD_HINT.MODE
STATE.CLKEN
Q3
~LOCAL.CLK~
BAD_HINT.CLKEN~
STATE.CLKEN~.B0
ALWAYS.B1.CLK~
CLK.2XE~.B1
CLK.2XE~.B0
Q4~
H2
DISPLAY
(3-6)
(12-37)
DISP~0,DISP~(7:15)
CUR_INSTR(3:15)
LEX_ADR.VIR(0:1)
CUR_NAME.OE~,REF_NAME.OE~,OFFS.OE~,PC.OE~
INT_READS.VIR(1:2)
MEM_STRT.DEC(0:2)
M_IN_CSA(0:3)
MAYBE_DISPATCH~
SEQ_STOP
COND_LOAD~
DISPLAY.RANDOMS
WANNA_DISPATCH~
BAD_HINT.DISP
MACRO_EVENT~
CONDITION.B0
M_IBUFF_MT~
MACRO.IBUFF~
RES_ADR.SEL(0:1)
USES_TOS.DEC
IMPORT.COND~,LEX_VLD.COND~,TOS_VLD.COND~
NEW_PC.IND~(57:59)
MACRO_PC.MODE(0:1)
BAD_HINT.CLK~
BAD_HINT.CLKEN~
STATE.CLKEN~.B0
STATE.CLKEN~.B1
H1
ALWAYS.B0.CLK~
ALWAYS.B1.CLK~
~LOCAL.CLK~
Q2~
CLK.2XE~.B0
STATE.CLKEN
FIU_REG.CLK~
SEQ_LOGIC
(8-11)
(44-78)
Q.MACRO_EVNT~
Q.COND.VAL(0:2),Q.COND.TYP(0:4),Q.COND.FIU(0:1),Q.COND.SYS(0:1)
Q.COND_SEL(0:6)
Q.CSA_MVE(0:3)
Q.U_EVENTS~
Q.MICROS_EN
Q.DISP_TIME
MACRO.DIAG
MICRO.DIAG
MICRO_CNTL.DIAG
HALT
FIELD_ERROR~
CASE~
MICRO_EVENT
Q3_COND
Q3_COND~
VIR.MODE(0:1)
DECODER.MODE(0:1)
WCS_PERR.MCHK~
BAD_HINT~
BAD_HINT
L_MACRO_HIC
L_MACRO_HIC~
ALWAYS.MODE
BAD_HINT.MODE
MODE_BUS
STACK.CLKEN~
BAD_HINT.DISP
SEQ_STOP
Q.ADDRESS_BUS
Q.ADR.SPACE(0:2),Q.ADR.NAME(0:31),Q.ADR.OFFS(0:31),Q.ADR.P(0:8)
MICRO_SEQ
Q.MEM_CNTL
Q.E_ABORT~,Q.L_ABORT~
Q.UADR(0:13),Q.UADR.P(0:1)
Q.UADR
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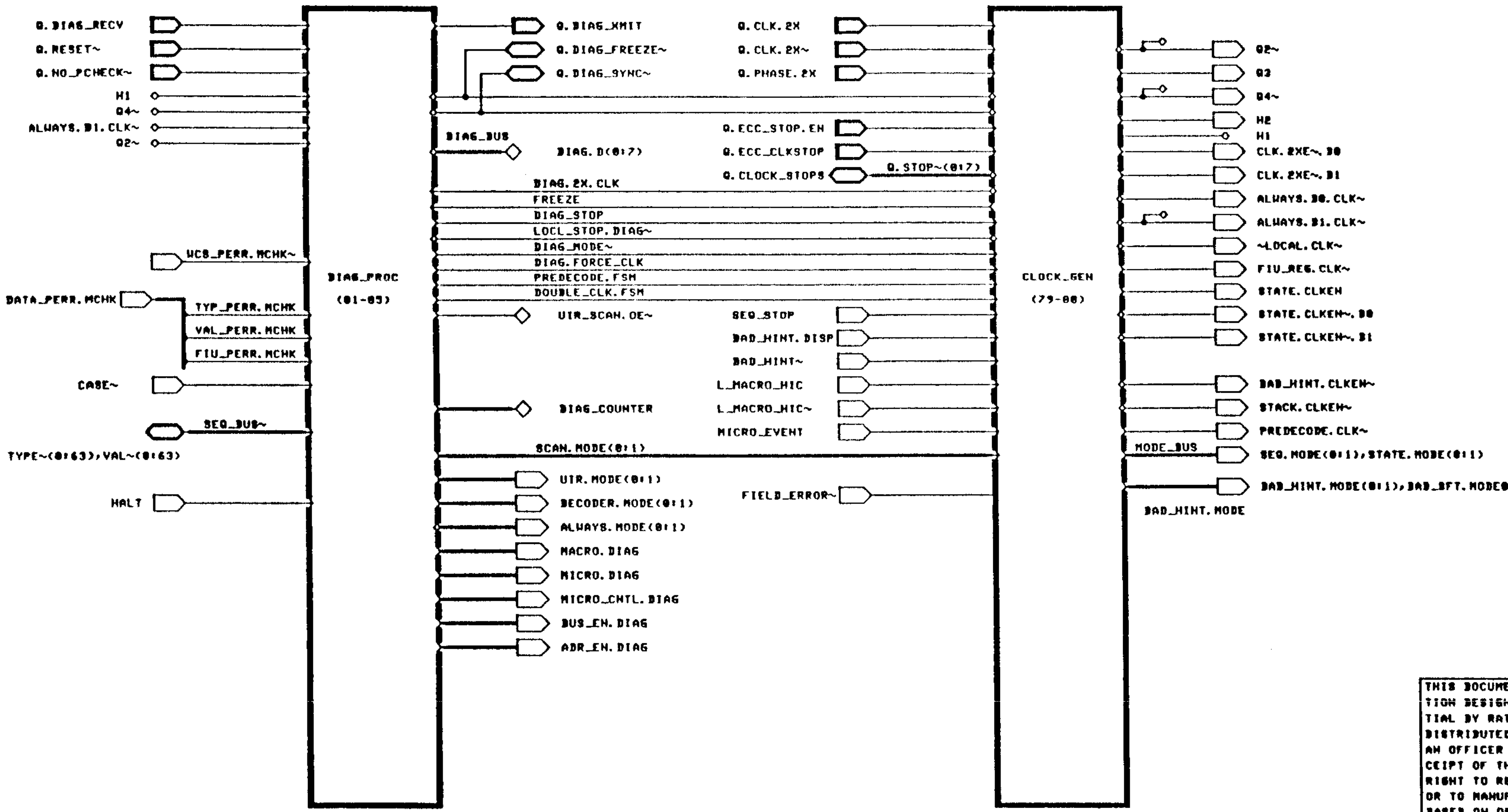
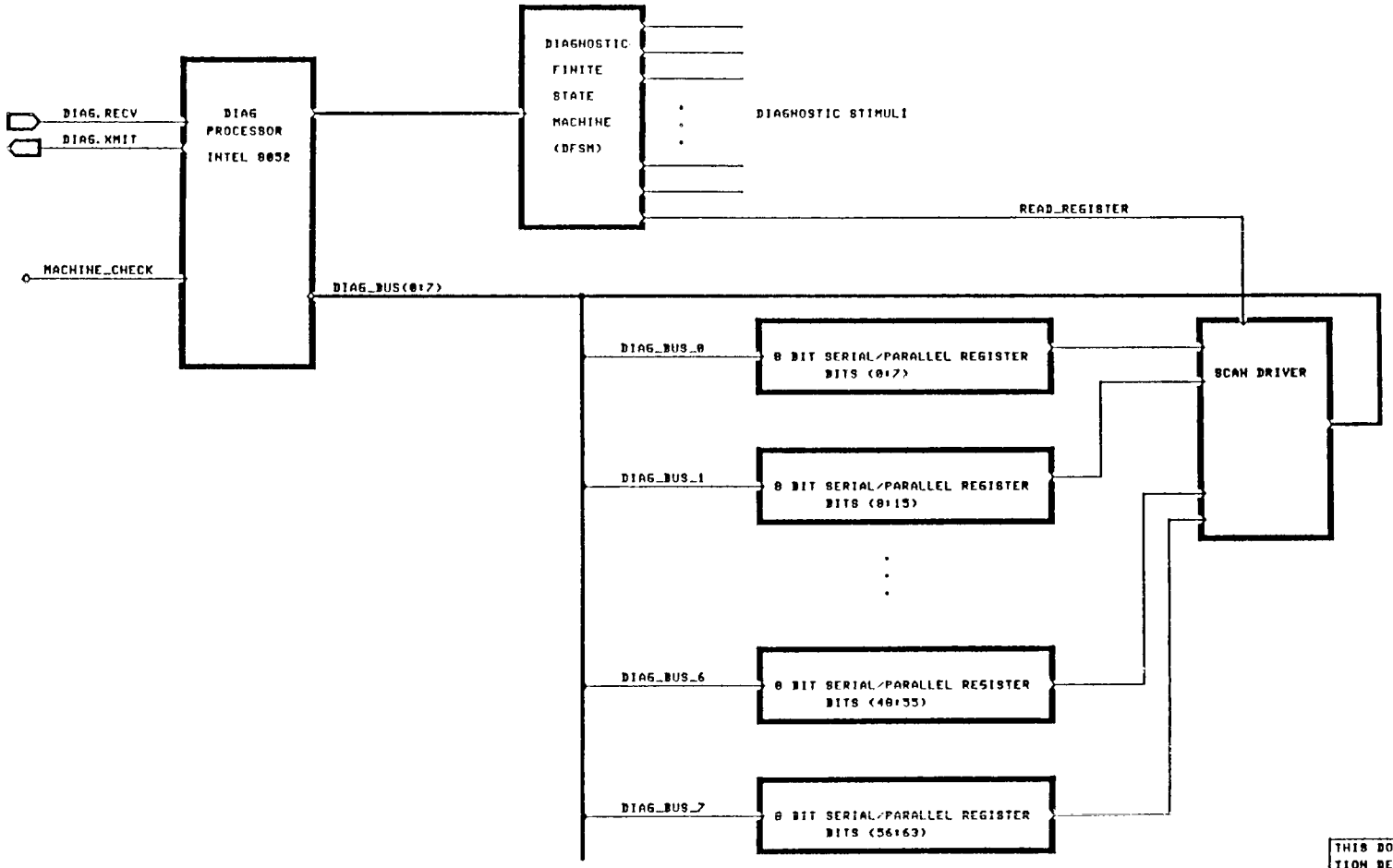
STATUS: RELEASED
22-MAY-90
5400
SEQUENCER
PAGE 1
232-003064
RATIONAL
MICROSEQUENCER
SHEET 1 OF 2
REV 1.0


Q.DIAG_RECV
Q.RESET~
Q.NO_PCHECK~
H1
Q4~
ALWAYS.D1.CLK~
Q2~
UCS_PERR.MCHK~
DATA_PERR.MCHK
TYP_PERR.MCHK
VAL_PERR.MCHK
FIU_PERR.MCHK
CASE~
SEQ_BUS~
TYPE~(0:63),VAL~(0:63)
HALT
DIAG_PROC
(01-05)
Q.DIAG_XMIT
Q.DIAG_FREEZE~
Q.DIAG_SYNC~
DIAG_BUS
DIAG.D(0:7)
DIAG.2X.CLK
FREEZE
DIAG_STOP
LOCL_STOP.DIAG~
DIAG_MODE~
DIAG.FORCE_CLK
PREDECODE.FSM
DOUBLE_CLK.FSM
UIR_SCAN.OE~
DIAG_COUNTER
SCAN.MODE(0:1)
UIR.MODE(0:1)
DECODER.MODE(0:1)
ALWAYS.MODE(0:1)
MACRO.DIAG
MICRO.DIAG
MICRO_CNTL.DIAG
BUS_EN.DIAG
ADR_EN.DIAG
Q.CLK.2X
Q.CLK.2X~
Q.PHASE.2X
Q.ECC_STOP.EN
Q.ECC_CLKSTOP
Q.CLOCK_STOPS
Q.STOP~(0:7)
SEQ_STOP
BAD_HINT.DISP
BAD_HINT~
L_MACRO_HIC
L_MACRO_HIC~
MICRO_EVENT
FIELD_ERROR~
CLOCK_GEN
(79-80)
Q2~
Q3
Q4~
H2
H1
CLK.2XE~.D0
CLK.2XE~.D1
ALWAYS.D0.CLK~
ALWAYS.D1.CLK~
~LOCAL.CLK~
FIU_REG.CLK~
STATE.CLKEN
STATE.CLKEN~.D0
STATE.CLKEN~.D1
BAD_HINT.CLKEN~
STACK.CLKEN~
PREDECODE.CLK~
MODE_BUS
SEQ.MODE(0:1),STATE.MODE(0:1)
BAD_HINT.MODE(0:1),BAD_SFT.MODE0
BAD_HINT.MODE

STATUS: RELEASED	RATIONAL	
22-MAY-90	CLOCKS AND DIAGNOSTICS	
S400		
SEQUENCER		
PAGE 2		
232-003064	SHEET 2 OF 2	REV 1.0

CPU - FRU's



STATUS:	RATIONAL	
17-SEP-90	R1000 DIAGNOSTIC SYSTE	
R1000	PER BOARD HARDWARE	
	SHEET 1 OF 1	REV 0.0