RCSL No: 44-RT1978

Edition: January 1981

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Title:

RC791 Lineselector
Technical Manual

RCSL 42-11592

A/S REGNECENTRALEN
af 1979

Keywords:

RC791, LIS701, Lineselector

Abstract:

This manual contains technical information on the RC791 lineselector.

(28 printed pages)

Printed by A/S Regnecentralen af 1979, Copenhagen

RCSL 42-i1592

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1. DESCRIPTION 1.

1.1 General Description 1.1

LIS701 is a V24-switch able to connect two of eight DTE's with two DCE's, as requested by the DTE's.

A DTE performs a connection request by means of the signals Data Terminal Ready and Request To Send.

RTS is used to select the DCE, and DTR indicates connection request.

If the selected DCE is not busy, the signals are connected through, and the connection persists as long as DTR is true.

To each DCE output, is assigned a scanner, which, when the DCE is not busy, scans the DTE-inputs for a possible connection request.

1.2 Functional Description 1.2

The signal inputs from the DTE ports are connected through line receivers to tristate gates connecting them to the A-bus or B-bus (see the block diagram). The tristate enable signals ¬ASEL(1) to ¬ASEL(8) and ¬BSEL(1) to ¬BSEL(8) are the decoded values of A(0:2) and B(0:2). (The number 000 is converted into sel(8), creating a sequence 1 to 8 rather than 0 to 7). The pointers A(0:2) and B(0:2) are the outputs of two binary counters, which when ABUSY and BBUSY are false, are scanning the DTE inputs for a possible DTR.

If the A-scanner meets a DTR together with a ¬RTS, ABUSY is set, blocking the clockpulses to the A-scanner, turning on the A-display indicating the value on the A-scanner, gating the signals through between the DTE and the DCE and finally sending DTR to the DCE.

1.3 Power Supply

The power supply supplies ±12 V for the V24 transmitters, and +5 V for the logic. The ±12 V are supplied via monolitic serial regulators. Due to the greater power dissipation resulting if a linear regulator was used for the 5 V, a switch mode regulator is used for this voltage.

The function of this regulator is best understood by rewriting the diagram as done in figs. 1 and 2.

The box in fig. 1 contains a comparator and a 5 V reference. The voltage on the output of this switches between +25 V and 0 V with an average value of 5 V. The voltage developed across C is this average superposed a small ripple voltage, equal to the hysteresis defined by R1 and R2: Uripple.pp. = (r2/(R1+R2))*25 V.

The operation cyclus is thus: point 1 outputs 25 V until the voltage on C has increased to 5 V + Uripple, then the voltage on point 1 switches to 0 V, and the voltage on C decreases to 5 V, at which voltage, point 1 again switches to +25 V, etc.

Fig. 2 shows what the box in fig. 1 really contains. The IC LM78L05 contains the 5 V reference plus the comparator except the "output stage". This consists of the transistor T and the "freewheeling" diode D. Current flows always out of point 1 either through T from 25 V or through D from 0 V.

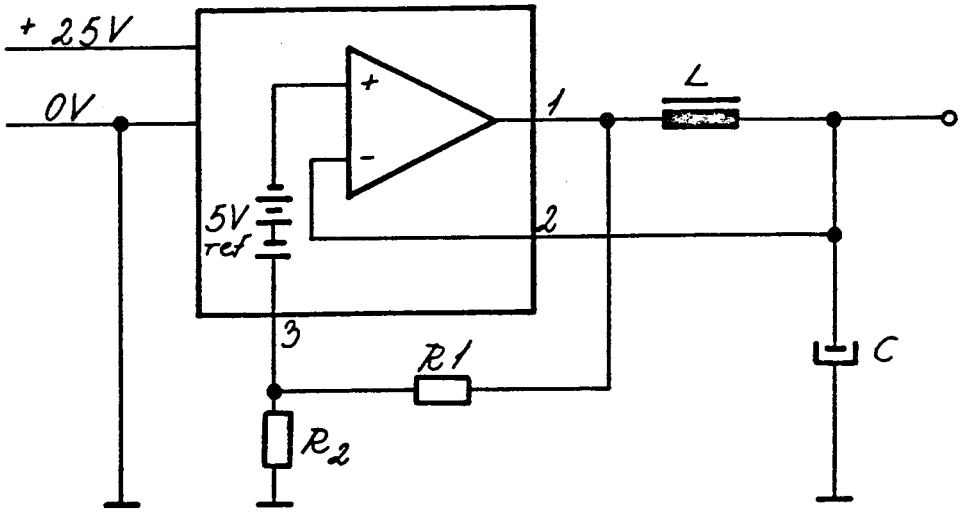


Fig. 1

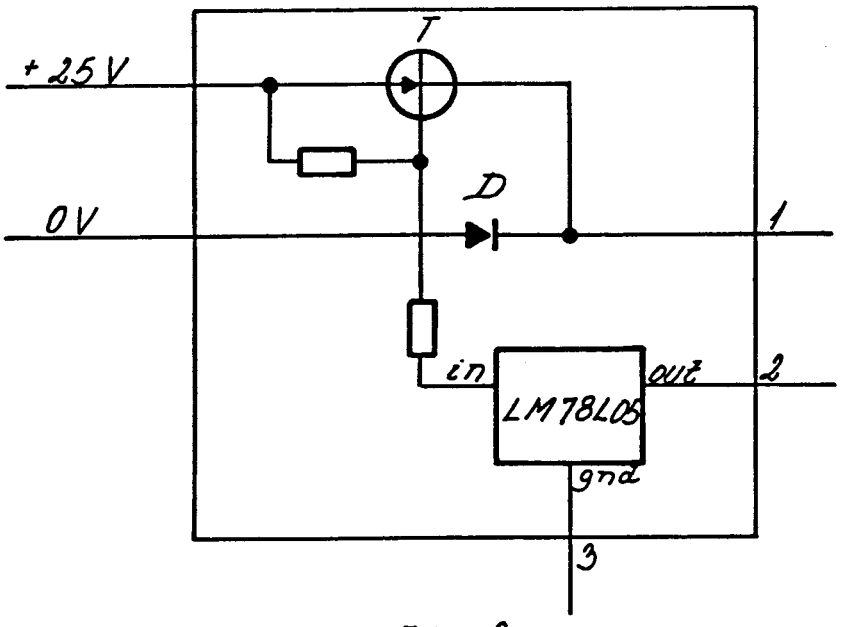
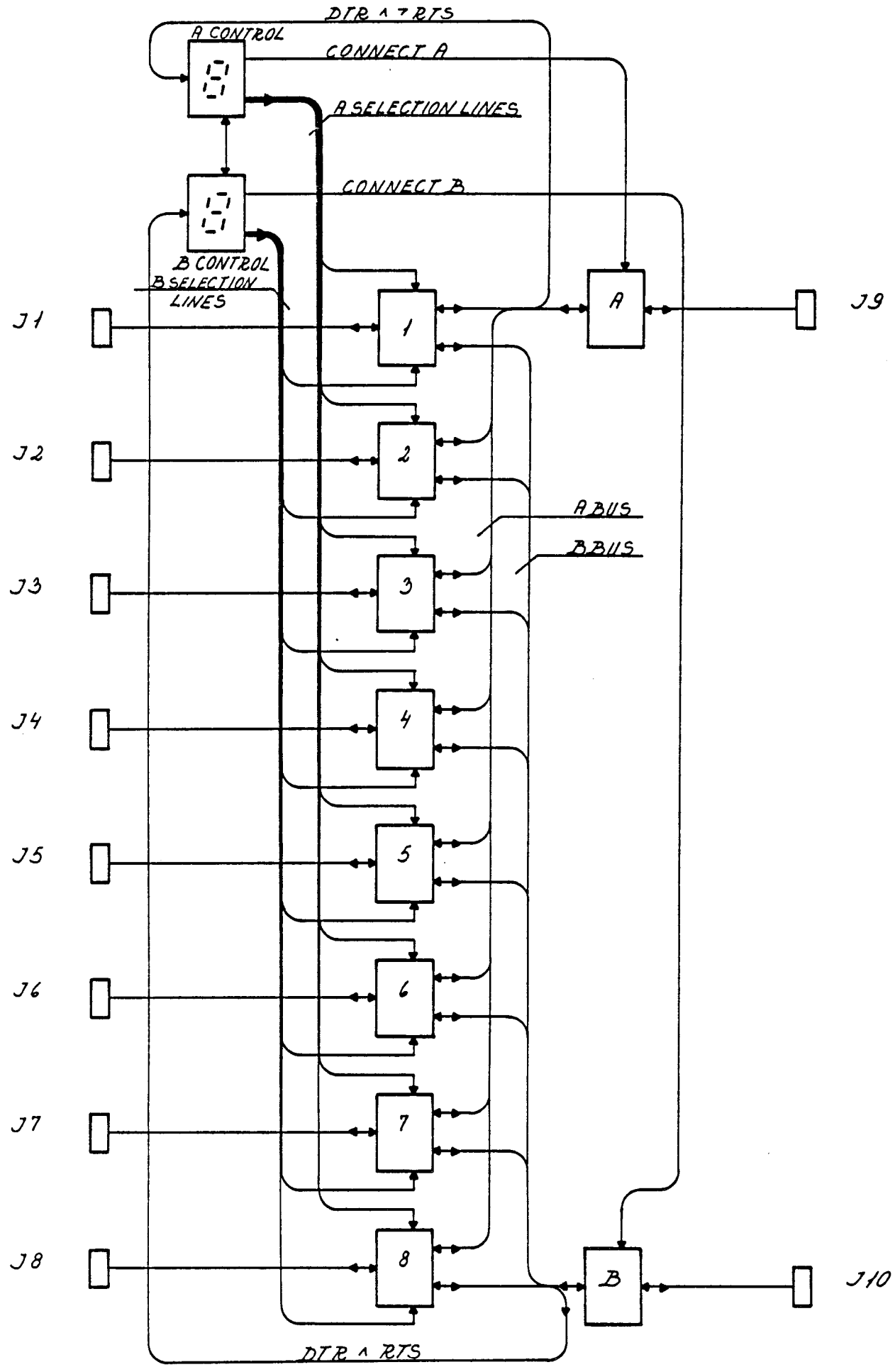


Fig. 2

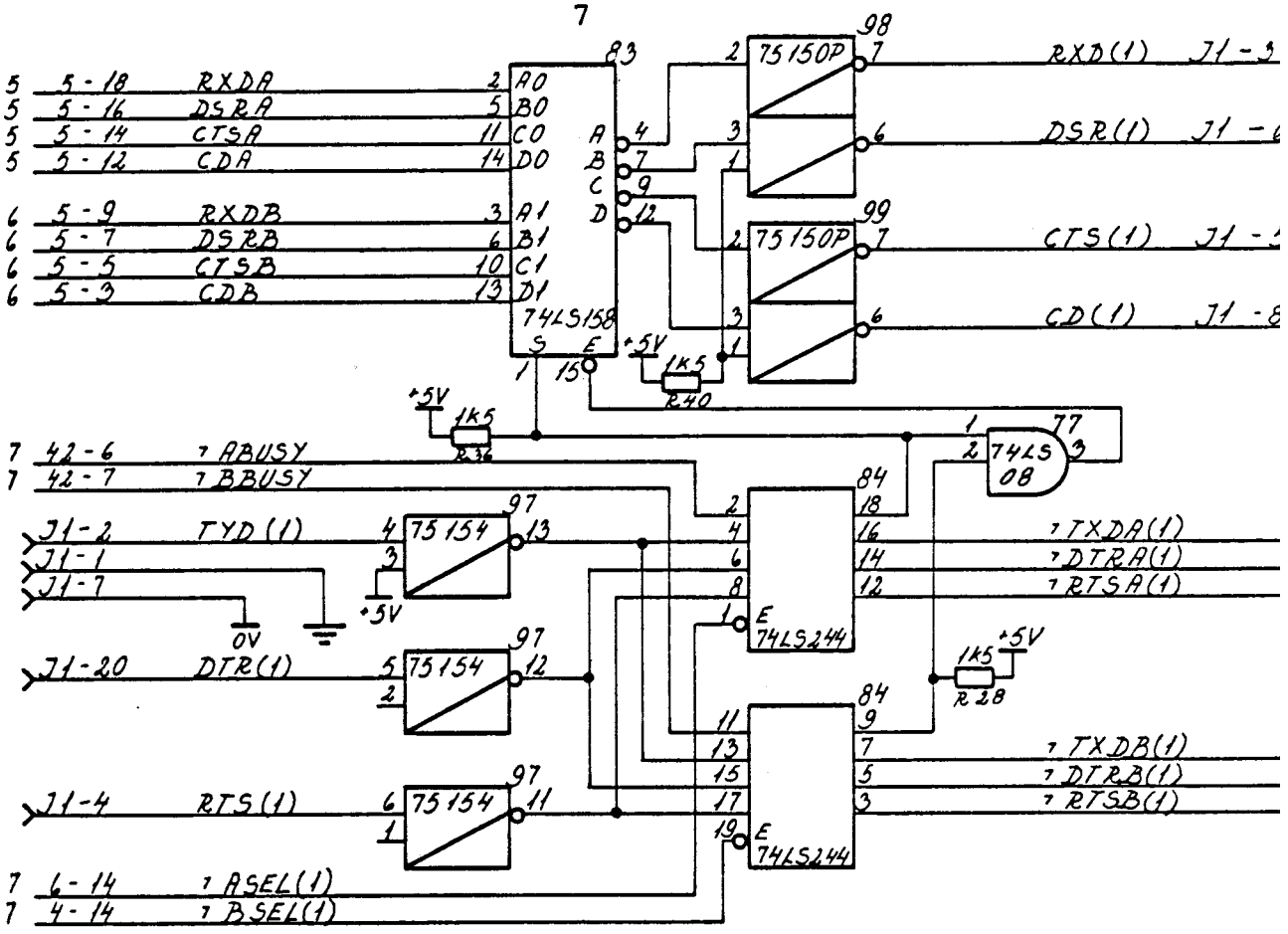


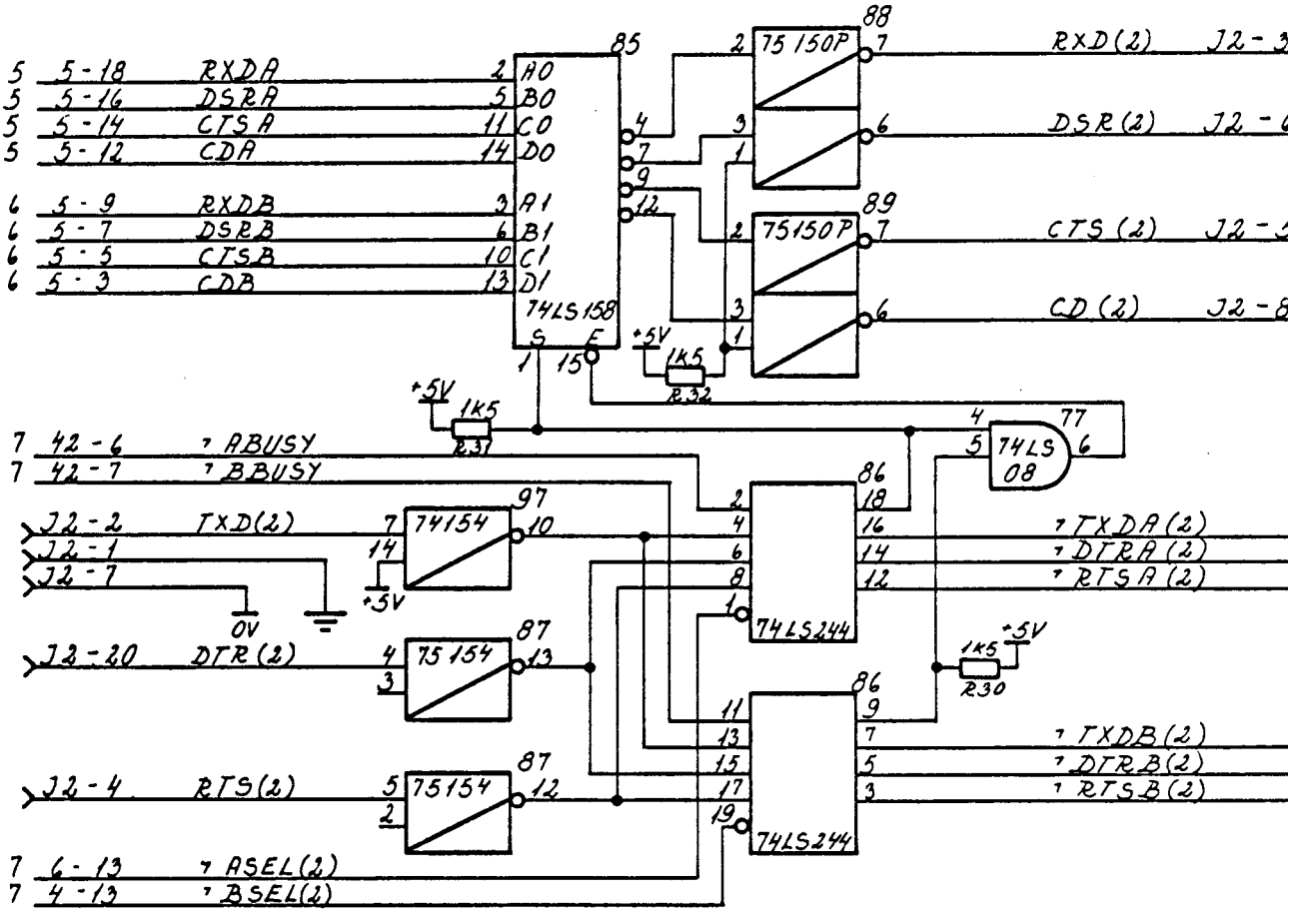
LIS701

BLOCK DIAGRAM

R 13098

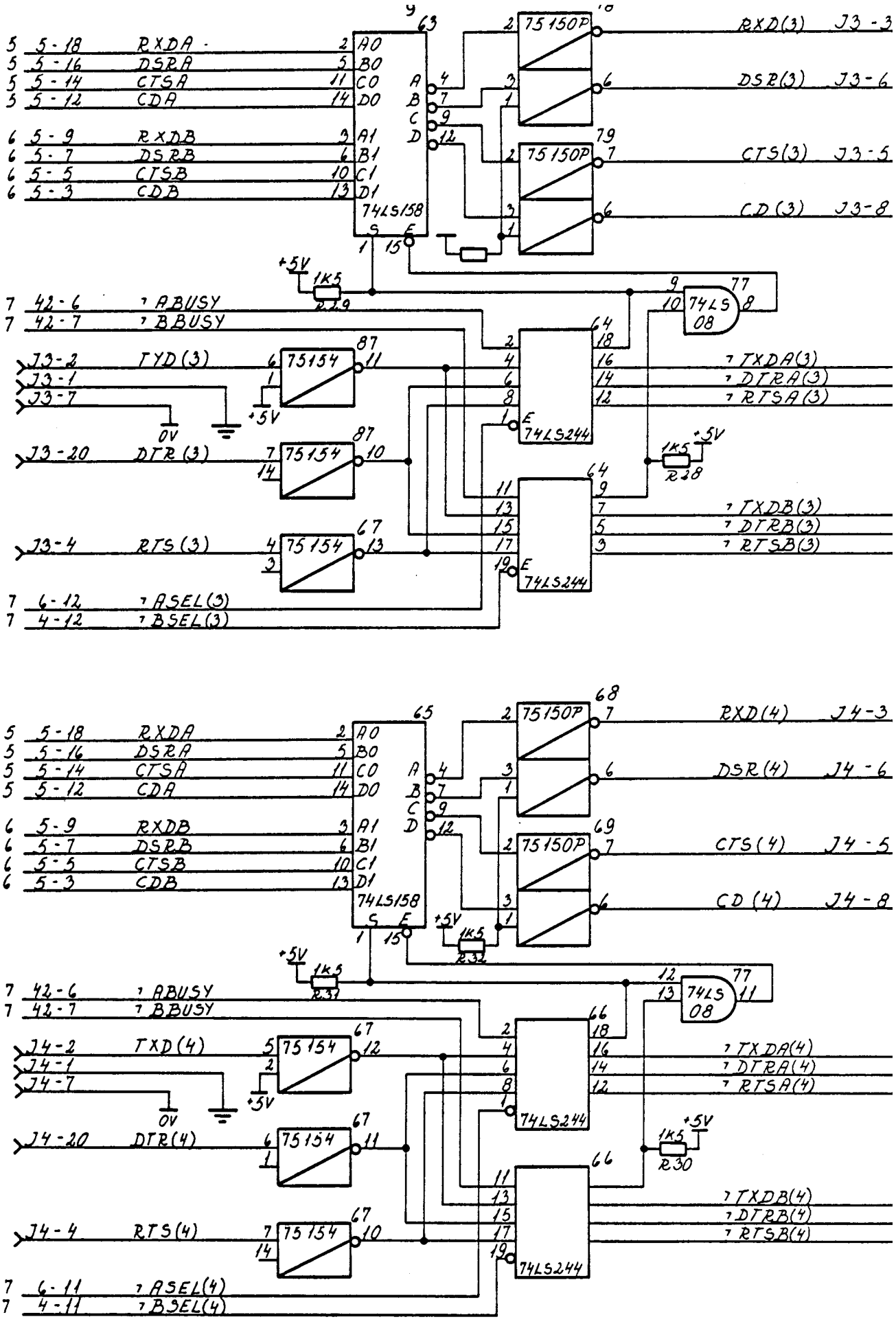
Signal	Destination	Description
RXD(1)	J1	Received Data to J1 V24-levels
DSR(1)	J1	Data Set Ready to J1 V24-levels
CTS(1)	J1	Clear To Send to J1 V24-levels
CD(1)	J1	Carrier Detect to J1 V24-levels
¬TXDA(1)	p. 5	Transmitted Data from J1 tristate-multiplexed to A bus
¬DTRA(1)	p. 5	Data Terminal Ready from J1 tristate-multiplexed to A bus
¬RTSA(1)	p. 5	Request To Send from J1 tristate-multiplexed to A bus
¬TXD(1)	p. 6	Transmitted Data from J1 tristate-multiplexed to B bus
¬DTR B(1)	p. 6	Data Terminal Ready from J1 tristate-multiplexed to B bus
¬RTS B(1)	p. 6	Request To send from J1 tristate-multiplexed to B bus
RXD(2)	J2	Received Data to J2 V24-levels
DSR(2)	J2	Data Set Ready to J2 V24-levels
CTS(2)	J2	Clear To Send to J2 V24-levels
CD(2)	J2	Carrier Detect to J2 V24-levels
¬TXDA(2)	p. 5	Transmitted Data from J2 tristate-multiplexed to A bus
¬DTRA(2)	p. 5	Data Terminal Ready from J2 tristate-multiplexed to A bus
¬RTSA(2)	p. 5	Request To Send from J2 tristate-multiplexed to A bus
¬TXD(2)	p. 6	Transmitted Data from J2 tristate-multiplexed to B bus
¬DTR B(2)	p. 6	Data Terminal Ready from J2 tristate-multiplexed to B bus
¬RTS B(2)	p. 6	Request To send from J2 tristate-multiplexed to B bus


5 5-18 RXDA
5 5-16 DSRA
5 5-14 CTSA
5 5-12 CDA
6 5-9 RXDB
6 5-7 DSRB
6 5-5 CTSB
6 5-3 CDB
74LS158
75150P
RXD(1) J1-3
DSR(1) J1-6
CTS(1) J1-5
CD(1) J1-8
+5V
1K5
R40
7 42-6 ↑ABUSY
7 42-7 ↑BBUSY
74LS 08
J1-2 TYD(1)
J1-1
J1-7
0V
75154
74LS244
↑TXDA(1)
↑DTRA(1)
↑RTSA(1)
J1-20 DTR(1)
R28
↑TXDB(1)
↑DTRB(1)
↑RTSB(1)
J1-4 RTS(1)
7 6-14 ↑ASEL(1)
7 4-14 ↑BSEL(1)

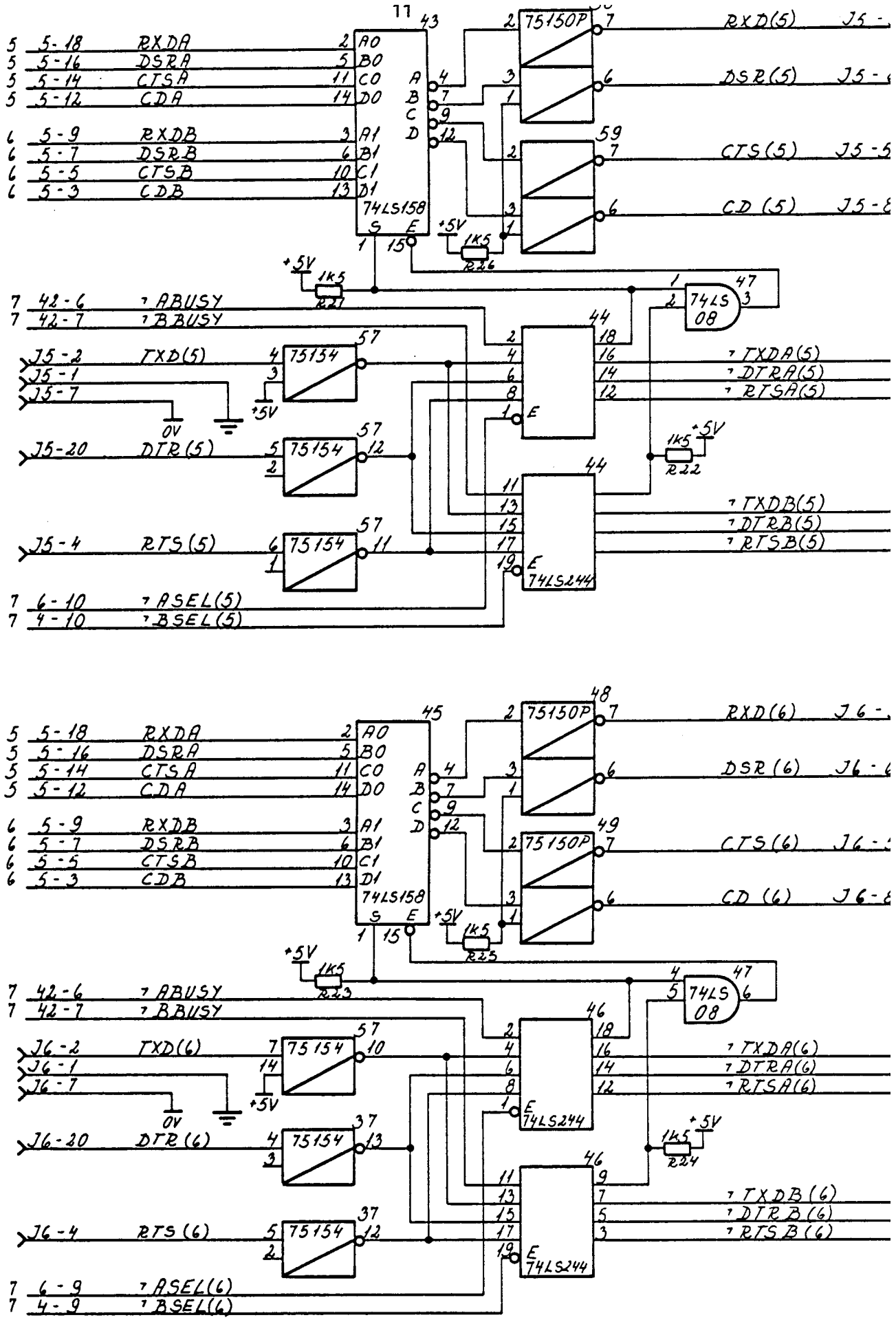

5 5-18 RXDA
5 5-16 DSRA
5 5-14 CTSA
5 5-12 CDA
6 5-9 RXDB
6 5-7 DSRB
6 5-5 CTSB
6 5-3 CDB
74LS158
75150P
RXD(2) J2-3
DSR(2) J2-6
CTS(2) J2-5
CD(2) J2-8
+5V
1K5
R32
7 42-6 ↑ABUSY
7 42-7 ↑BBUSY
74LS 08
J2-2 TXD(2)
J2-1
J2-7
0V
74154
74LS244
↑TXDA(2)
↑DTRA(2)
↑RTSA(2)
J2-20 DTR(2)
R30
↑TXDB(2)
↑DTRB(2)
↑RTSB(2)
J2-4 RTS(2)
7 6-13 ↑ASEL(2)
7 4-13 ↑BSEL(2)

PKA AGA

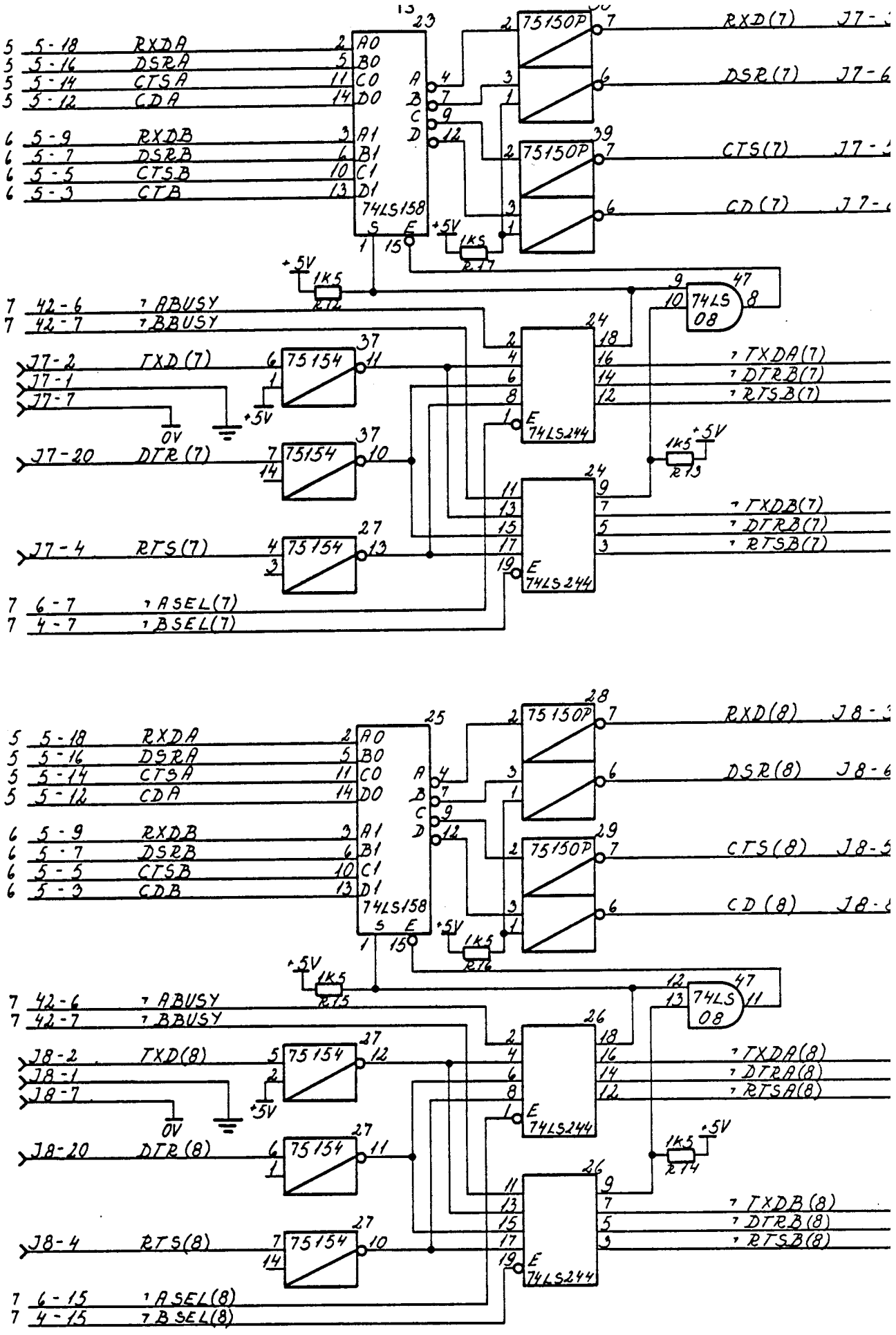
Signal	Destination	Description
RXD(3)	J3	Received Data to J3 V24-levels
DSR(3)	J3	Data Set Ready to J3 V24-levels
CTS(3)	J3	Clear To Send to J3 V24-levels
CD(3)	J3	Carrier Detect to J3 V24-levels
¬TXDA(3)	p. 5	Transmitted Data from J3 tristate-multiplexed to A bus
¬DTRA(3)	p. 5	Data Terminal Ready from J3 tristate-multiplexed to A bus
¬RTSA(3)	p. 5	Request To Send from J3 tristate-multiplexed to A bus
¬TXD(3)	p. 6	Transmitted Data from J3 tristate-multiplexed to B bus
¬DTR B(3)	p. 6	Data Terminal Ready from J3 tristate-multiplexed to B bus
¬RTS B(3)	p. 6	Request To send from J3 tristate-multiplexed to B bus
RXD(4)	J4	Received Data to J4 V24-levels
DSR(4)	J4	Data Set Ready to J4 V24-levels
CTS(4)	J4	Clear To Send to J4 V24-levels
CD(4)	J4	Carrier Detect to J4 V24-levels
¬TXDA(4)	p. 5	Transmitted Data from J4 tristate-multiplexed to A bus
¬DTRA(4)	p. 5	Data Terminal Ready from J4 tristate-multiplexed to A bus
¬RTSA(4)	p. 5	Request To Send from J4 tristate-multiplexed to A bus
¬TXD(4)	p. 6	Transmitted Data from J4 tristate-multiplexed to B bus
¬DTR B(4)	p. 6	Data Terminal Ready from J4 tristate-multiplexed to B bus
¬RTS B(4)	p. 6	Request To send from J4 tristate-multiplexed to B bus


RXDA
DSRA
CTSA
CDA
RXDB
DSRB
CTSB
CDB
74LS158
75150P
RXD(3) J3-3
DSR(3) J3-6
CTS(3) J3-5
CD(3) J3-8
+5V
1K5
R29
R28
R30
R31
R32
74LS08
74LS244
75154
ABUSY
BBUSY
TXD(3)
DTR(3)
RTS(3)
TXDA(3)
DTRA(3)
RTSA(3)
TXDB(3)
DTRB(3)
RTSB(3)
ASEL(3)
BSEL(3)
RXD(4) J4-3
DSR(4) J4-6
CTS(4) J4-5
CD(4) J4-8
TXD(4)
DTR(4)
RTS(4)
TXDA(4)
DTRA(4)
RTSA(4)
TXDB(4)
DTRB(4)
RTSB(4)
ASEL(4)
BSEL(4)
0V

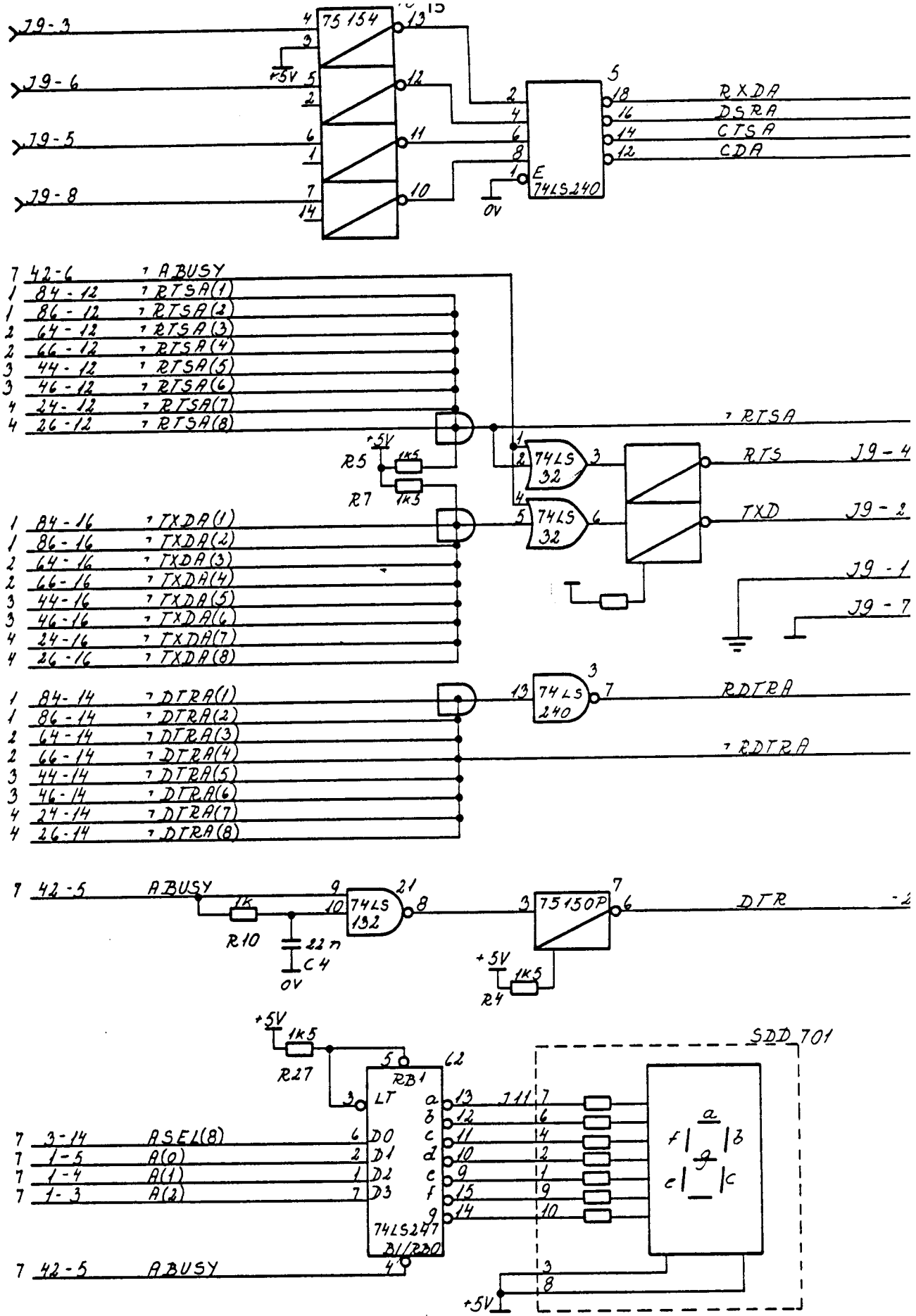
Signal	Destination	Description
RXD(5)	J5	Received Data to J5 V24-levels
DSR(5)	J5	Data Set Ready to J5 V24-levels
CTS(5)	J5	Clear To Send to J5 V24-levels
CD(5)	J5	Carrier Detect to J5 V24-levels
¬TXDA(5)	p. 5	Transmitted Data from J5 tristate-multiplexed to A bus
¬DTRA(5)	p. 5	Data Terminal Ready from J5 tristate-multiplexed to A bus
¬RTSA(5)	p. 5	Request To Send from J5 tristate-multiplexed to A bus
¬TXD(5)	p. 6	Transmitted Data from J5 tristate-multiplexed to B bus
¬DTR B(5)	p. 6	Data Terminal Ready from J5 tristate-multiplexed to B bus
¬RTS B(5)	p. 6	Request To send from J5 tristate-multiplexed to B bus
RXD(6)	J6	Received Data to J6 V24-levels
DSR(6)	J6	Data Set Ready to J6 V24-levels
CTS(6)	J6	Clear To Send to J6 V24-levels
CD(6)	J6	Carrier Detect to J6 V24-levels
¬TXDA(6)	p. 5	Transmitted Data from J6 tristate-multiplexed to A bus
¬DTRA(6)	p. 5	Data Terminal Ready from J6 tristate-multiplexed to A bus
¬RTSA(6)	p. 5	Request To Send from J6 tristate-multiplexed to A bus
¬TXD(6)	p. 6	Transmitted Data from J6 tristate-multiplexed to B bus
¬DTR B(6)	p. 6	Data Terminal Ready from J6 tristate-multiplexed to B bus
¬RTS B(6)	p. 6	Request To send from J6 tristate-multiplexed to B bus


5 5-18 RXDA
5 5-16 DSRA
5 5-14 CTSA
5 5-12 CDA
6 5-9 RXDB
6 5-7 DSRB
6 5-5 CTSB
6 5-3 CDB
74LS158
75150P
RXD(5)
DSR(5)
CTS(5)
CD (5)
+5V
1K5
R26
R27
7 42-6 ABUSY
7 42-7 BBUSY
74LS 08
J5-2 TXD(5)
J5-1
J5-7
0V
75154
J5-20 DTR(5)
J5-4 RTS(5)
7 6-10 ASEL(5)
7 4-10 BSEL(5)
7 TXDA(5)
7 DTRA(5)
7 RTSA(5)
7 TXDB(5)
7 DTRB(5)
7 RTSB(5)
R22
74LS244
RXD(6)
DSR(6)
CTS(6)
CD (6)
R25
R23
J6-2 TXD(6)
J6-1
J6-7
J6-20 DTR(6)
J6-4 RTS(6)
7 6-9 ASEL(6)
7 4-9 BSEL(6)
7 TXDA(6)
7 DTRA(6)
7 RTSA(6)
7 TXDB(6)
7 DTRB(6)
7 RTSB(6)
R24

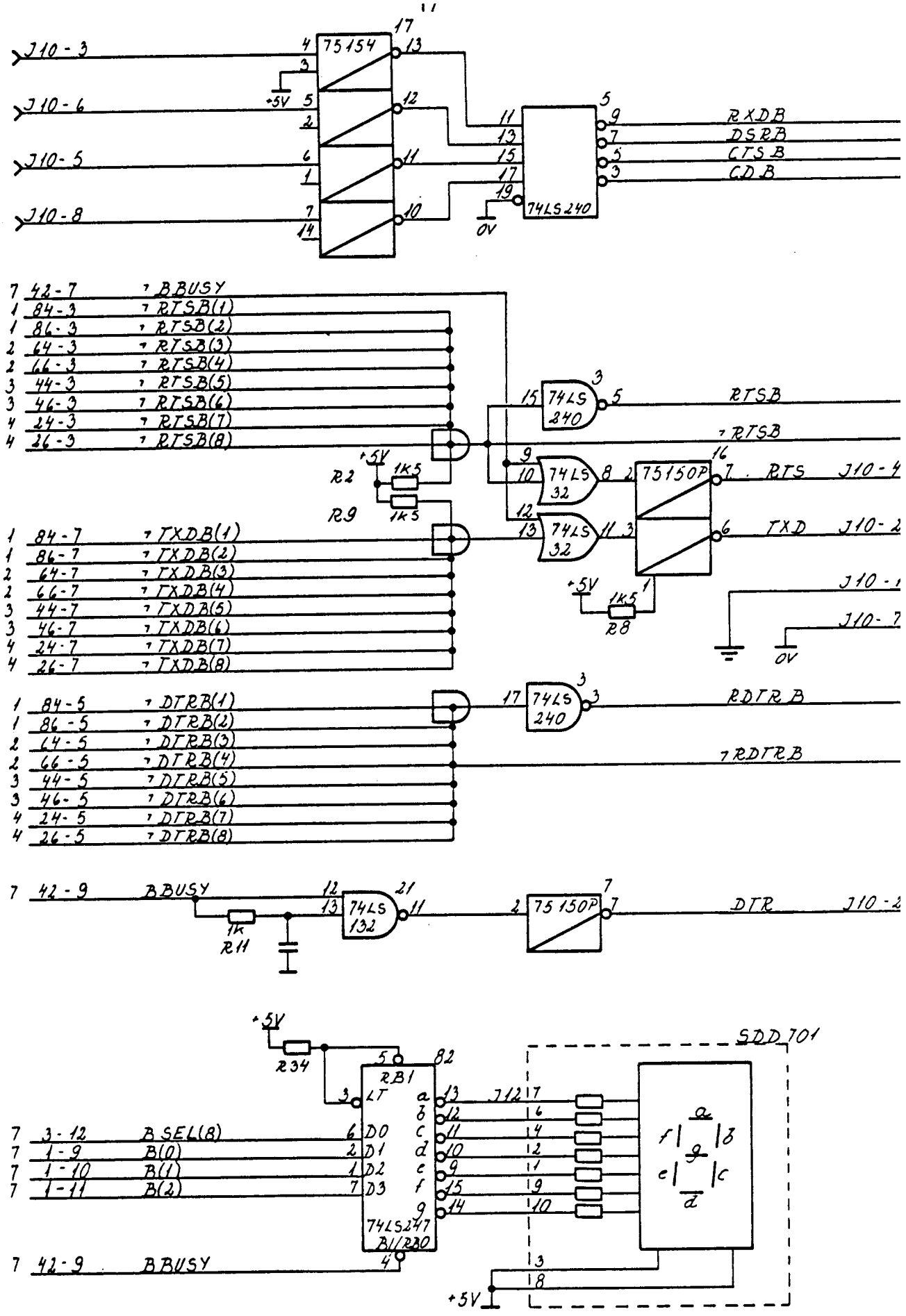
Signal	Destination	Description
RXD(7)	J7	Received Data to J7 V24-levels
DSR(7)	J7	Data Set Ready to J7 V24-levels
CTS(7)	J7	Clear To Send to J7 V24-levels
CD(7)	J7	Carrier Detect to J7 V24-levels
¬TXDA(7)	p. 5	Transmitted Data from J7 tristate-multiplexed to A bus
¬DTRA(7)	p. 5	Data Terminal Ready from J7 tristate-multiplexed to A bus
¬RTSA(7)	p. 5	Request To Send from J7 tristate-multiplexed to A bus
¬TXD(7)	p. 6	Transmitted Data from J7 tristate-multiplexed to B bus
¬DTR B(7)	p. 6	Data Terminal Ready from J7 tristate-multiplexed to B bus
¬RTS B(7)	p. 6	Request To send from J7 tristate-multiplexed to B bus
RXD(8)	J8	Received Data to J8 V24-levels
DSR(8)	J8	Data Set Ready to J8 V24-levels
CTS(8)	J8	Clear To Send to J8 V24-levels
CD(8)	J8	Carrier Detect to J8 V24-levels
¬TXDA(8)	p. 5	Transmitted Data from J8 tristate-multiplexed to A bus
¬DTRA(8)	p. 5	Data Terminal Ready from J8 tristate-multiplexed to A bus
¬RTSA(8)	p. 5	Request To Send from J8 tristate-multiplexed to A bus
¬TXD(8)	p. 6	Transmitted Data from J8 tristate-multiplexed to B bus
¬DTR B(8)	p. 6	Data Terminal Ready from J8 tristate-multiplexed to B bus
¬RTS B(8)	p. 6	Request To send from J8 tristate-multiplexed to B bus


5 5-18 RXDA
5 5-16 DSRA
5 5-14 CTSA
5 5-12 CDA
6 5-9 RXDB
6 5-7 DSRB
6 5-5 CTSB
6 5-3 CTB
74LS158
75150P
RXD(7)
DSR(7)
CTS(7)
CD(7)
+5V
1K5
7 42-6 ↑ABUSY
7 42-7 ↑BBUSY
74LS 08
J7-2 TXD(7)
J7-1
J7-7
0V
75154
J7-20 DTR(7)
J7-4 RTS(7)
74LS244
↑TXDA(7)
↑DTRB(7)
↑RTSB(7)
↑TXDB(7)
↑DTRB(7)
↑RTSB(7)
7 6-7 ↑ASEL(7)
7 4-7 ↑BSEL(7)
RXD(8)
DSR(8)
CTS(8)
CD(8)
J8-2 TXD(8)
J8-1
J8-7
J8-20 DTR(8)
J8-4 RTS(8)
↑TXDA(8)
↑DTRA(8)
↑RTSA(8)
↑TXDB(8)
↑DTRB(8)
↑RTSB(8)
7 6-15 ↑ASEL(8)
7 4-15 ↑BSEL(8)

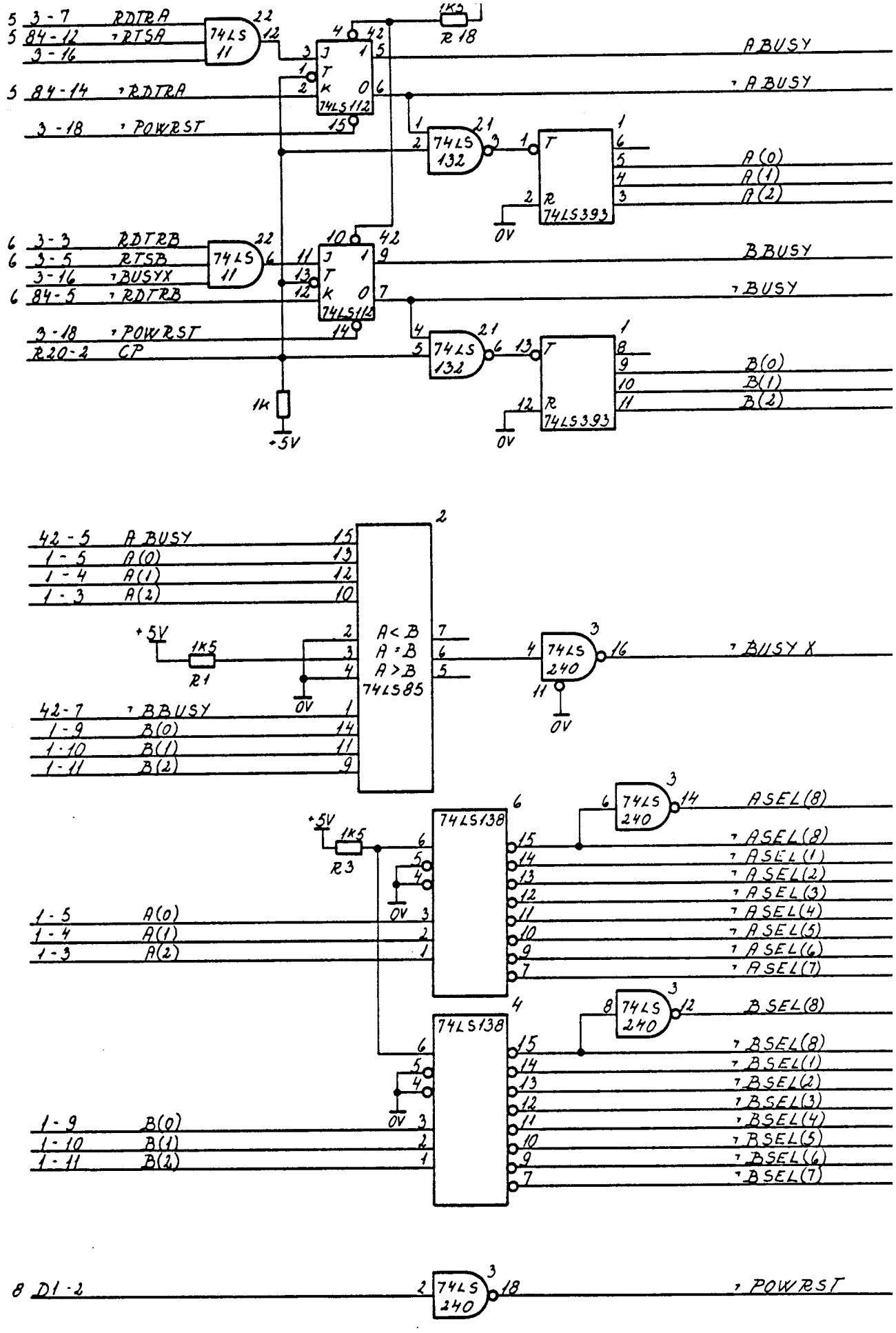
Signal	Destination	Description
RXDA	p. 1. 2. 3. 4	Received Data to J9
DSRA	p. 1. 2. 3. 4	Data Set Ready to J9
CTSA	p. 1. 2. 3. 4	Clear To Send to J9
CDA	p. 1. 2. 3. 4	Carrier Detected from J9
¬RTSA(7)	p. 5, 7	Request To Send from A bus V24-levels
TXD	J9	Transmitted Data to J9 V24-levels
¬RDTR A, RDTR A	p. 7	Data Terminal Ready from A bus
DTR	J9	Data Terminal Ready to J9 V24-levels


J9-3
J9-6
J9-5
J9-8
75154
+5V
0V
74LS240
RXDA
DSRA
CTSA
CDA
7 42-6 ↑ABUSY
1 84-12 ↑RTSA(1)
1 86-12 ↑RTSA(2)
2 64-12 ↑RTSA(3)
2 66-12 ↑RTSA(4)
3 44-12 ↑RTSA(5)
3 46-12 ↑RTSA(6)
4 24-12 ↑RTSA(7)
4 26-12 ↑RTSA(8)
↑RTSA
R5 1K5
R7 1K5
74LS 32
RTS
TXD
J9-4
J9-2
J9-1
J9-7
1 84-16 ↑TXDA(1)
1 86-16 ↑TXDA(2)
2 64-16 ↑TXDA(3)
2 66-16 ↑TXDA(4)
3 44-16 ↑TXDA(5)
3 46-16 ↑TXDA(6)
4 24-16 ↑TXDA(7)
4 26-16 ↑TXDA(8)
1 84-14 ↑DTRA(1)
1 86-14 ↑DTRA(2)
2 64-14 ↑DTRA(3)
2 66-14 ↑DTRA(4)
3 44-14 ↑DTRA(5)
3 46-14 ↑DTRA(6)
4 24-14 ↑DTRA(7)
4 26-14 ↑DTRA(8)
74LS 240
RDTRA
↑RDTRA
7 42-5 ABUSY
R10 1K
C4 22n
74LS 132
75150P
DTR
R4 1K5
+5V
0V
R27 1K5
RB1
LT
D0
D1
D2
D3
74LS247
7 3-14 ASEL(8)
7 1-5 A(0)
7 1-4 A(1)
7 1-3 A(2)
7 42-5 ABUSY
SDD 701
a
b
c
d
e
f
g

Signal	Destination	Description
RXDB	p. 1. 2. 3. 4	Received Data from J10
DSRB	p. 1. 2. 3. 4	Data Set Ready from J10
CTSB	p. 1. 2. 3. 4	Clear To Send from J10
CDB	p. 1. 2. 3. 4	Carrier Detected from J10
RTSB	p. 7	Request To Send from B bus
¬RTSB	p. 5	
RTS	J10	Request To Send to J10 V24-levels
TXD	J10	Transmitted Data to J10
¬RDTR B, DTR B	p. 7	Data Terminal Ready from B bus
DTR	J10	Data Terminal Ready to J10 V24-levels


J10-3
J10-6
J10-5
J10-8
75154
+5V
74LS240
0V
RXDB
DSRB
CTSB
CDB
7 42-7 BBUSY
1 84-3 RTSB(1)
1 86-3 RTSB(2)
2 64-3 RTSB(3)
2 66-3 RTSB(4)
3 44-3 RTSB(5)
3 46-3 RTSB(6)
4 24-3 RTSB(7)
4 26-3 RTSB(8)
74LS 240
RTSB
R2
1K5
R9
74LS 32
75150P
RTS J10-4
TXD J10-2
R8
1 84-7 TXDB(1)
1 86-7 TXDB(2)
2 64-7 TXDB(3)
2 66-7 TXDB(4)
3 44-7 TXDB(5)
3 46-7 TXDB(6)
4 24-7 TXDB(7)
4 26-7 TXDB(8)
1 84-5 DTRB(1)
1 86-5 DTRB(2)
2 64-5 DTRB(3)
2 66-5 DTRB(4)
3 44-5 DTRB(5)
3 46-5 DTRB(6)
4 24-5 DTRB(7)
4 26-5 DTRB(8)
RDTRB
RDTRB
7 42-9 BBUSY
1K
R11
74LS 132
DTR J10-2
+5V
R34
RB1
LT
DO D1 D2 D3
a b c d e f g
74LS247
BI/RBO
7 3-12 BSEL(8)
7 1-9 B(0)
7 1-10 B(1)
7 1-11 B(2)
7 42-9 BBUSY
J12
SDD701
RGA
PKA

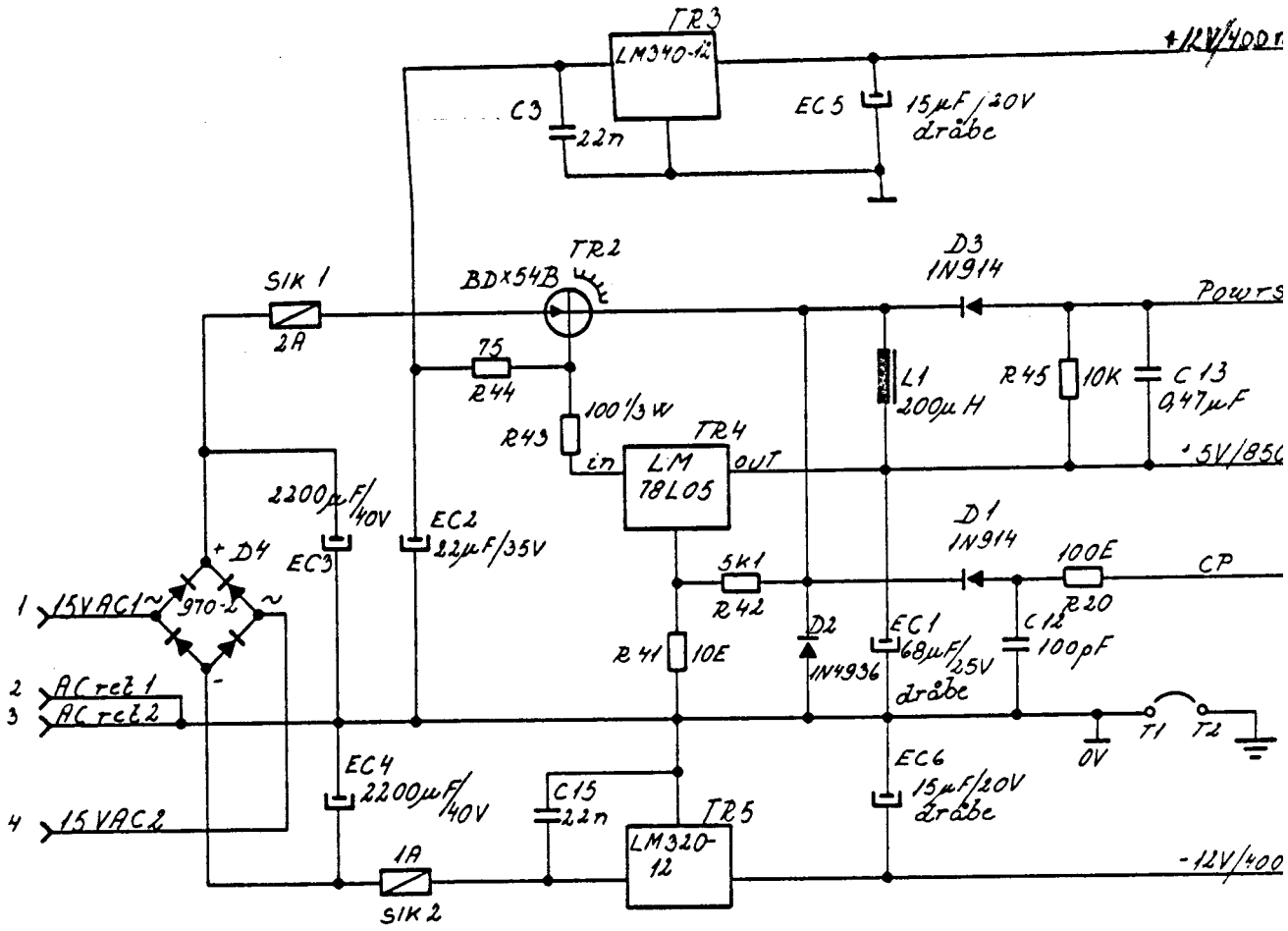
Signal	Destination	Description
ABUSY	p. 5, 7	port A busy, indicates that
¬ABUSY	p. 1, 2, 3, 4, 7	A(0:2) points at an input port which is currently connected to port A.
A(0:2)	p. 5, 7	A-Scanner output
BBUSY	p. 6, 7	port B busy, indicates that
¬BBUSY	p. 1, 2, 3, 4, 7	B(0:2) points at an input port which is currently connected to port B.
¬BUSYX	p. 7	low when both scanners point at same input port, and one is busy. Used to prevent one input from connecting to both outputs, at the same time.
¬ASEL(1), ¬ASEL(2)	p. 1	
¬ASEL(3), ¬ASEL(4)	p. 2	tristate-enable signals for
¬ASEL(5), ¬ASEL(6)	p. 3	the A bus.
¬ASEL(7), ¬ASEL(8)	p. 4	
ASEL8	p. 5	most significant bit of A(-1:2)
¬BSEL(1), ¬BSEL(2)	p. 1	
¬BSEL(3), ¬BSEL(4)	p. 2	tristate-enable signals for
¬BSEL(5), ¬BSEL(6)	p. 3	the B bus.
¬BSEL(7), ¬BSEL(8)	p. 4	
BSEL8	p. 6	most significant bit of B(-1:2)

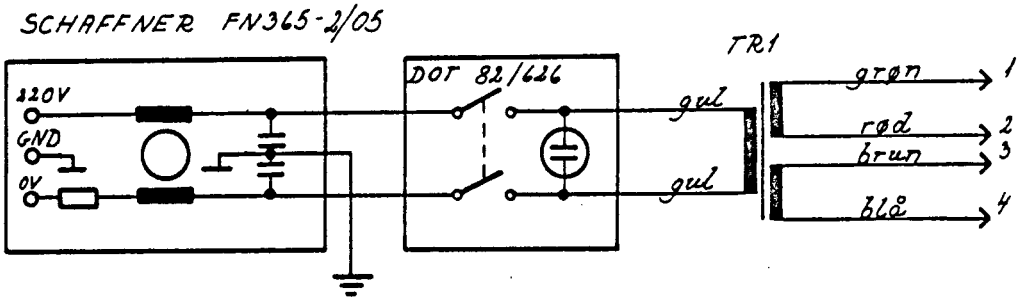

5 3-7 RDTRA
5 84-12 ↑RTSA
3-16
5 84-14 ↑RDTRA
3-18 ↑POWRST
74LS 11
74LS112
R 18
A BUSY
↑A BUSY
74LS 132
74LS393
A(0)
A(1)
A(2)
0V
6 3-3 RDTRB
6 3-5 RTSB
3-16 ↑BUSYX
6 84-5 ↑RDTRB
3-18 ↑POWRST
R20-2 CP
B BUSY
↑BUSY
B(0)
B(1)
B(2)
1K
+5V
42-5 A BUSY
1-5 A(0)
1-4 A(1)
1-3 A(2)
A<B
A=B
A>B
74LS85
+5V
1K5
R1
42-7 ↑BBUSY
1-9 B(0)
1-10 B(1)
1-11 B(2)
74LS 240
↑BUSY X
74LS138
R3
ASEL(8)
↑ASEL(8)
↑ASEL(1)
↑ASEL(2)
↑ASEL(3)
↑ASEL(4)
↑ASEL(5)
↑ASEL(6)
↑ASEL(7)
BSEL(8)
↑BSEL(8)
↑BSEL(1)
↑BSEL(2)
↑BSEL(3)
↑BSEL(4)
↑BSEL(5)
↑BSEL(6)
↑BSEL(7)
8 D1-2
↑POWRST

AGA

PKA

Signal	Destination	Description
12 V/400 mA, -12 V/400 mA		Power supply for V24 transmitters
+5 V/850 mA		Power supply for all logic circuits, and LED-displays.
T1, T2		Jumper is installed, when signal ground is required connected to protective ground.
Powrst	p. 7	Logic reset signal, goes low when 5 V regulator starts switching (when 5 V is up).
CP	p. 7	Clockpulse for driving the scanners, derived from the 5 V switches. Frequency is about 30 KHz.


TR3
LM340-12
+12V/400
C3
22n
EC5
15µF/20V
dråbe
TR2
BDx54B
SIK 1
2A
D3
IN914
Powrs
75
R44
100 1/3W
R43
L1
200µH
R45
10K
C13
0,47µF
TR4
LM
78L05
in
out
+5V/850
2200µF/
40V
EC3
EC2
22µF/35V
+D4
D1
IN914
100E
CP
5K1
R42
R20
1
15VAC1~
970-2
~
R41
10E
D2
IN4936
EC1
68µF/25V
dråbe
C12
100pF
2
AC ret 1
3
AC ret 2
0V
T1
T2
EC4
2200µF/
40V
C15
22n
TR5
EC6
15µF/20V
dråbe
4
15VAC2
LM320-
12
1A
SIK 2
-12V/400


SCHAFFNER FN365-2/05
220V
GND
0V
DOR 82/626
TR1
gul
gul
grøn
1
rød
2
brun
3
blå
4

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