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RC702 Microcomputer
Technical Manual

RCSL 42-11592

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af 1979

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Abstract:

This manual contains a technical description of the RC702 Microcomputer

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1. DESCRIPTION 1.

The RC702 Microcomputer is a selfcontained computer system, which together with keyboard, videomonitor, and zero, one, or two flexible disc drives make a complete computer system.

The keyboard used may be an RC721 or an RC722. The video monitor used may be an RC752. The flexible disc drive may be an RC761 or an RC762. All theese units are described in their own manuals. Fig. 1.1 shows an example of how to connect these units.

The RC702 itself is built up by the following parts:

1. MIC702 Microcomputer board
2. ROAxxx Character generator
3. KBN702 Cabinet with cables, transformer, and rectifier unit
4. CBL921 Internal video cable
5. CBL903 Internal power cable
6. CBL928 Internal sync. cable
7. CBL440 External power cable
8. POW739 Power supply

Part 1 and 2 are described in chapter 2 of this manual. Part 3 to 7 are described in chapter 3 of this manual, and part 8 is described in chapter 4 of this manual.

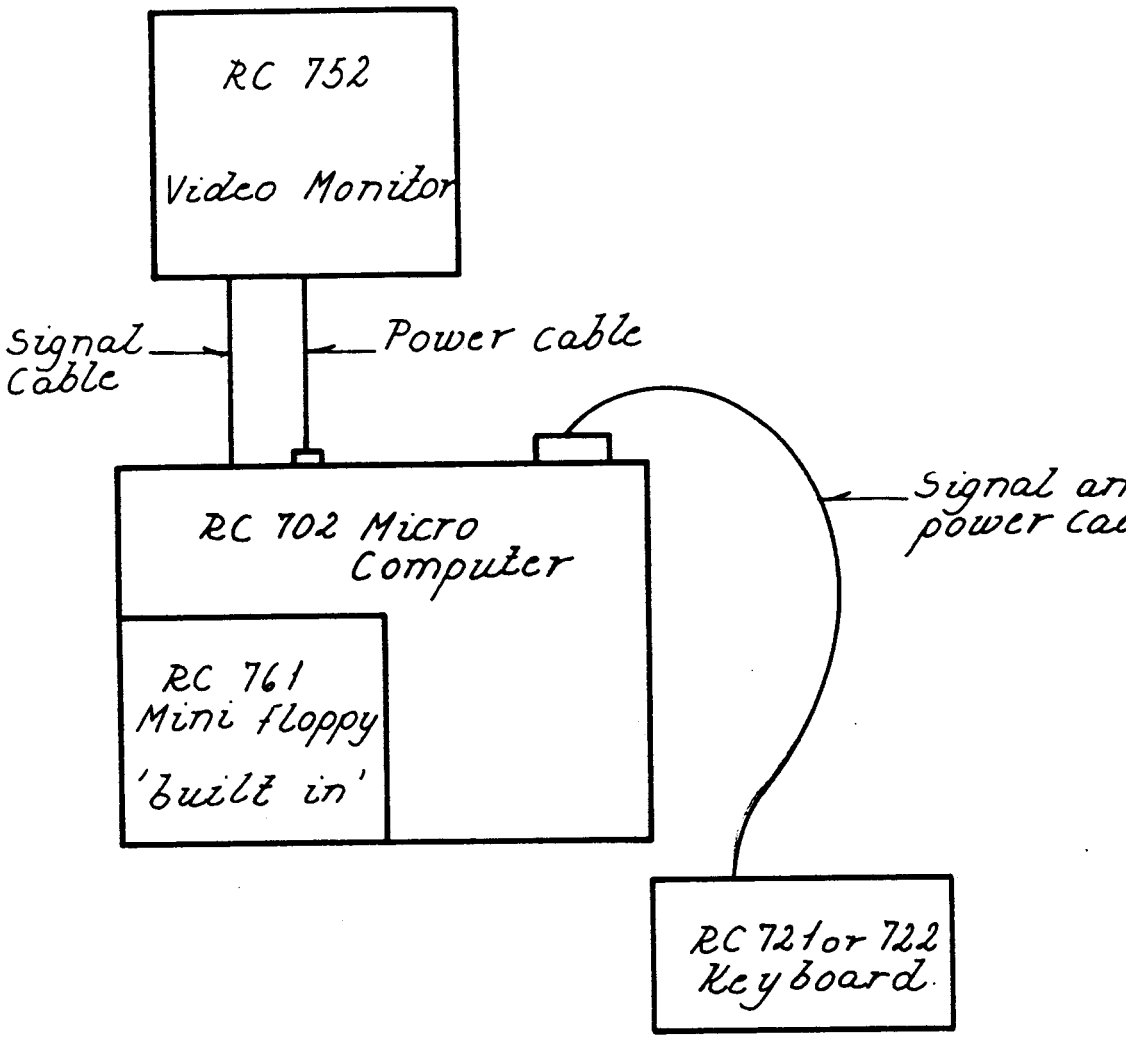
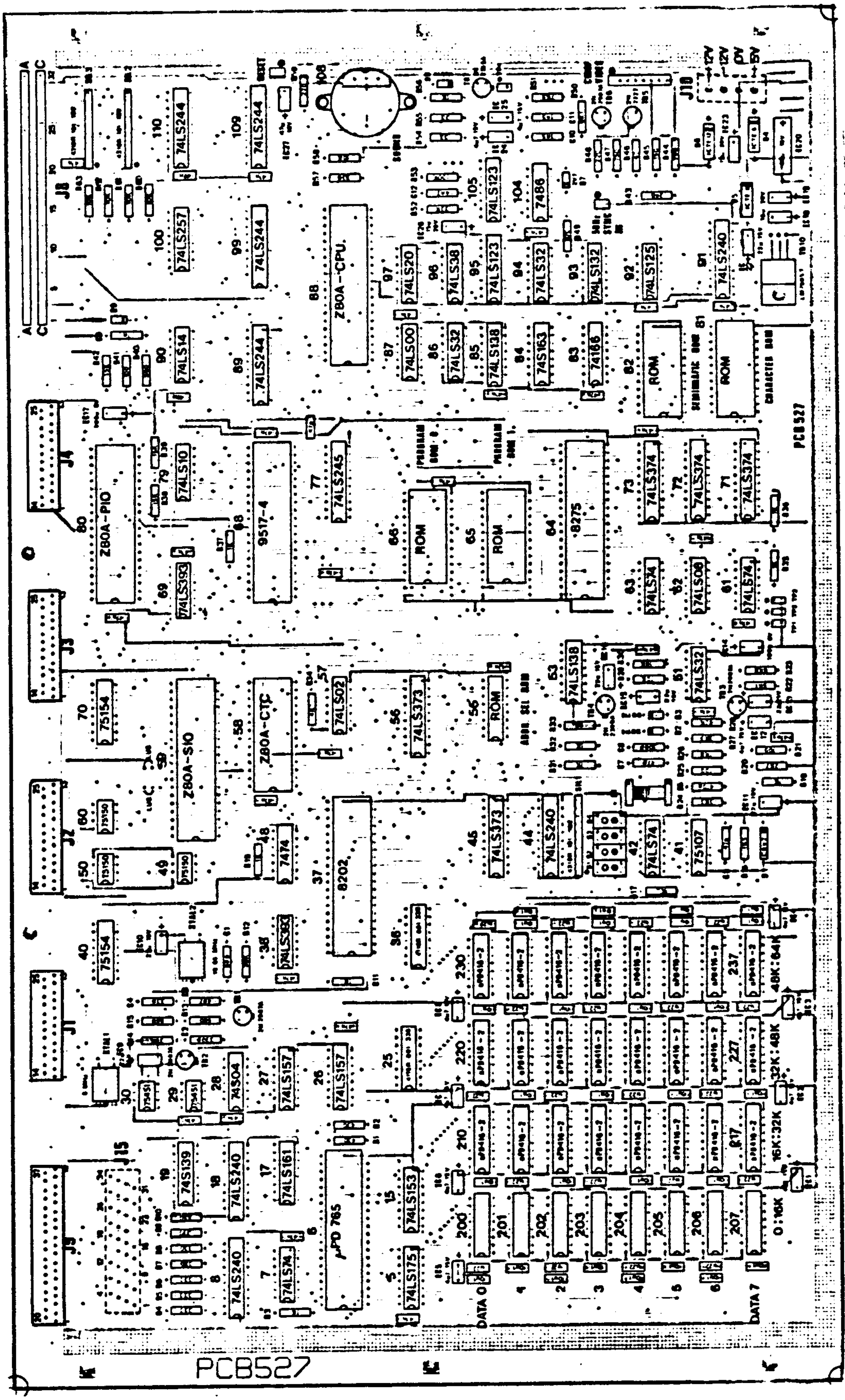


Fig. 1.1. Example of an RC 700 System made of an RC 702 Microcomputer, Video Monitor, Keyboard, and Mini floppy disk drive.



56 ROM
65 —"—
66 —"—
81 —"—
82 —"—

Fig. 2.1. BOARD LAY OUT.

2. MIC702 MICROCOMPUTER AND CHARACTER GENERATOR 2.

2.1 General Description 2.1

The MIC 702 is built on a single circuit board. Power is supplied via a 4 pin connector, and MIC702 needs the following supply:

+5 V typical 2.5 Amp.
+12 V typical 0.1 Amp.
-12 V typical 0.1 Amp.

The board layout is shown in fig. 2.1 which also shows the input/output connections.

2.2 Block Diagram 2.2

Fig. 2.2 shows a block diagram of MIC702. In the diagram is shown where each block is found in the circuit diagrams.

2.3 Functional Description 2.3

The functional description follows the block diagram. This paper does not contain a full description of all the functions of the VLSI circuits used in MIC702. This kind of informations may be supplied by the manufactures of the VLSI circuits.

2.3.1 CPU Description 2.3.1

A block diagram of the architecture of the Z-80A CPU is shown in fig. 2.3.1. The diagram shows all the major elements in the CPU and it should be referred to throughout the following description.

Z-80A CPU contains 208 bits of R/W memory that are accessible to the programmers. Fig. 2.3.2 illustrates how this memory is configurated into eighteen 8-bit registers and four 16-bit registers.

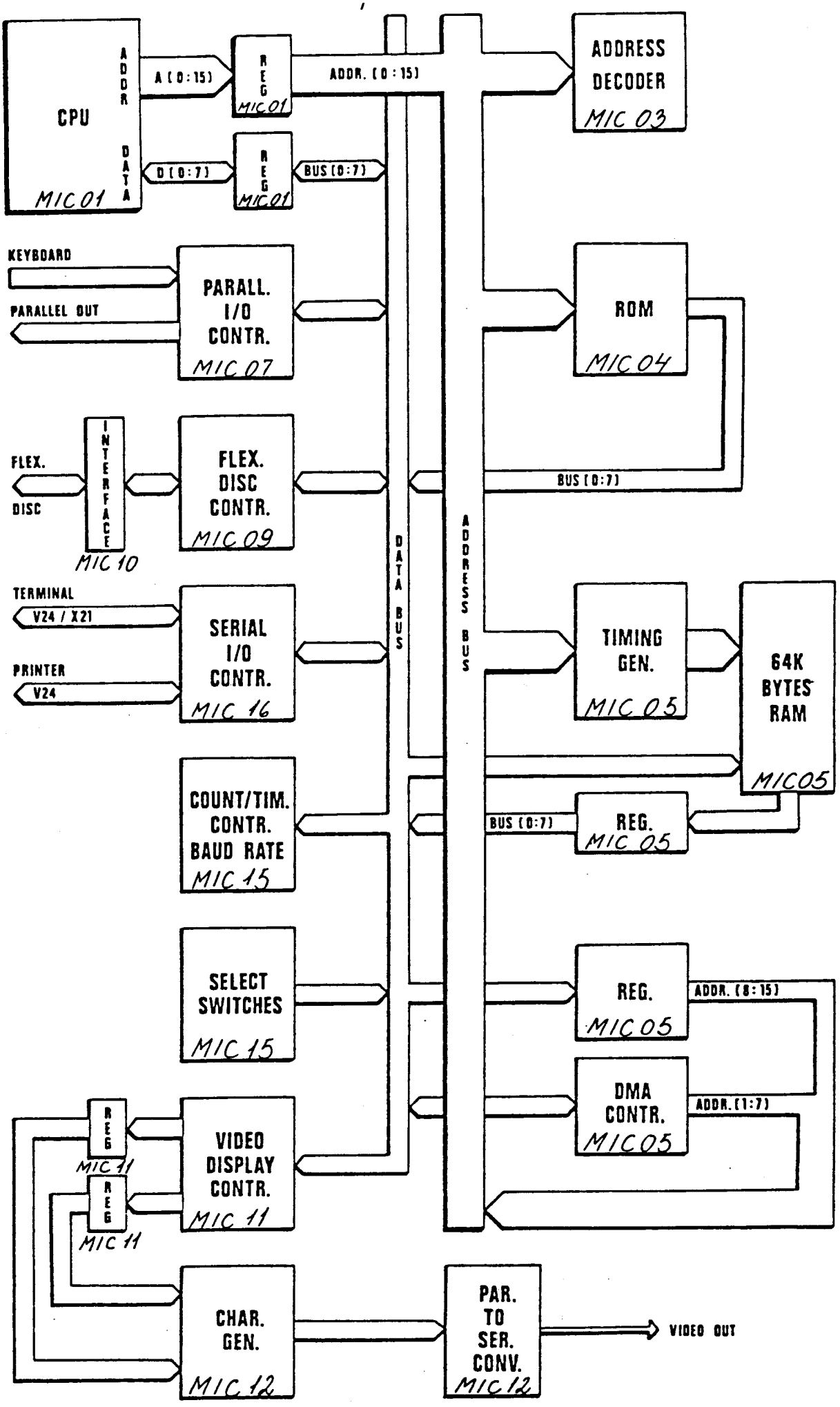


Fig. 2.2. Block Diagram RC 702.

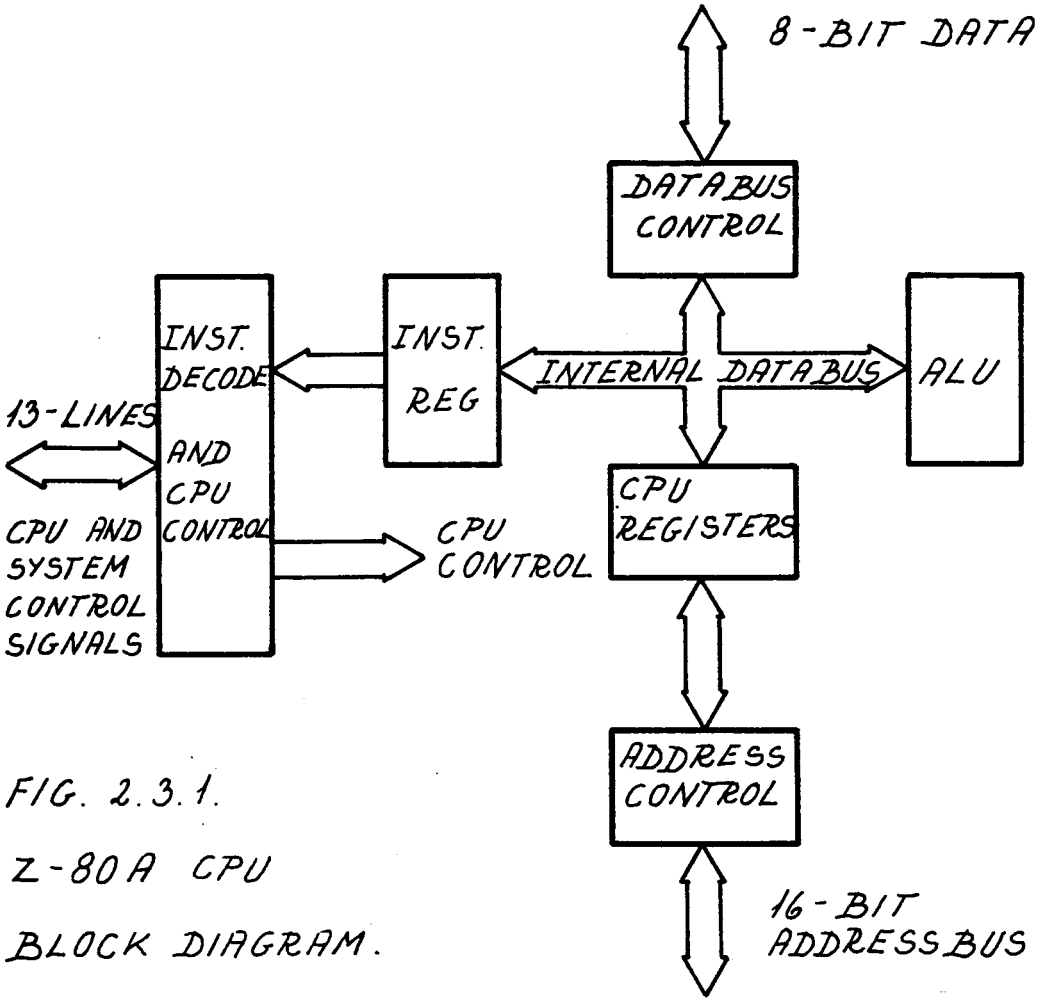


FIG. 2.3.1.

Z-80A CPU

BLOCK DIAGRAM.

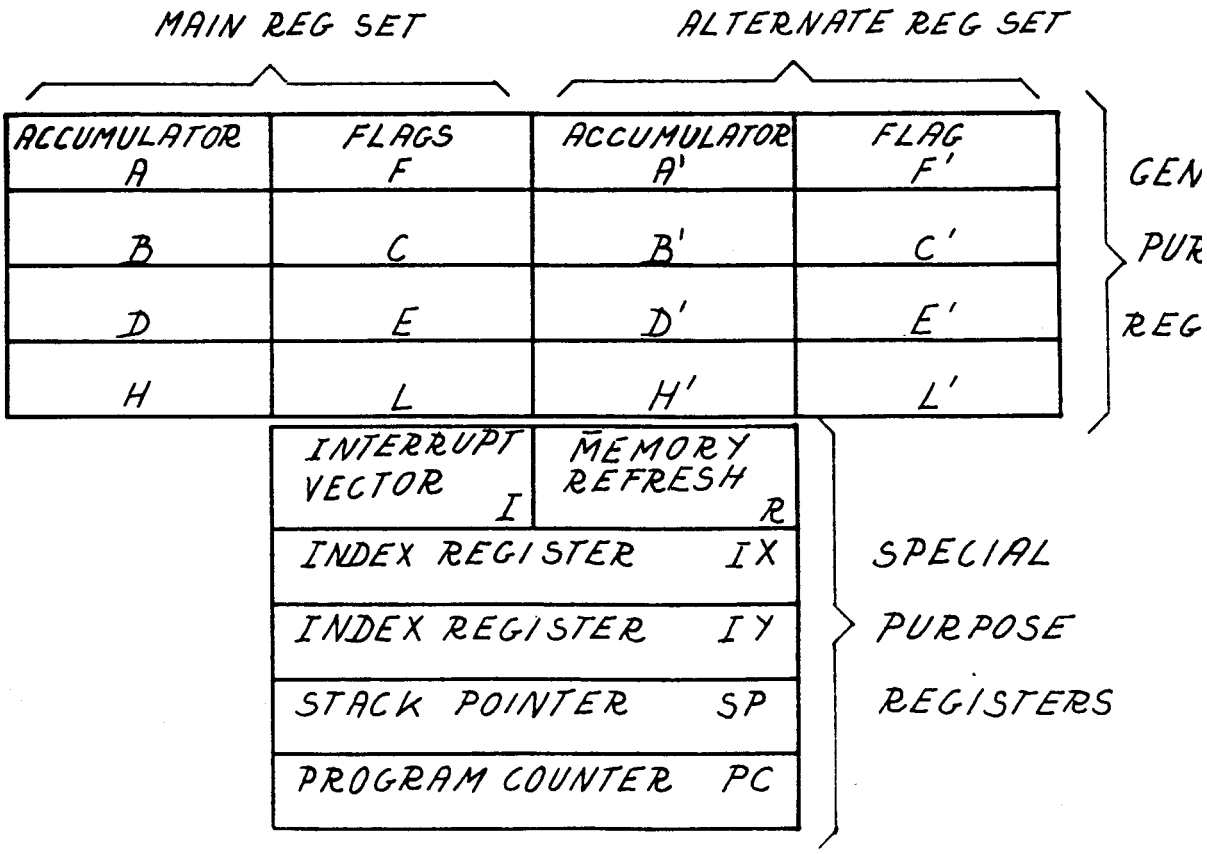


FIG 2.3.2. Z 80A CPU REGISTERS

All Z-80A registers are implemented using static RAM. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or in pairs as 16-bit registers. There are also two sets of accumulators and flag registers.

CPU timing can be broken down into a few very simple timing diagrams. The diagrams show basic operations with one wait state (the wait state is added to synchronize the CPU to the RAM memory). Figs. 2.3.3 to 2.3.5 show the CPU timing.

The Z80A CPU can execute 158 different instruction types including all 78 of the 8.080A CPU. A description of this may be obtained from Zilog Z80A CPU Technical Manual.

2.3.2 Address Decoder 2.3.2

The addressing of devices is made very simple with the circuit shown in diagram page MIC03. Each device uses 4 addresses except the DMA controller which uses 16 addresses. This is shown in fig. 2.3.6.

Addressing of dynamic RAM and ROM is made using the PROM in Pos. 55. Most significant bit in the PROM is controlled by the flip-flop in Pos. 42. The flip-flop is reset by the RESET signal and set by the program using the following instruction:

OUT (18 Hex), A

The resulting addressing is shown in fig. 2.3.7.

This circuit makes it possible for the program to disconnect the program stored in PROM 0 and in PROM 1.

2.3.3 Parallel I/O Controller 2.3.3

The Z-80A parallel I/O (PIO) interface controller is a program-

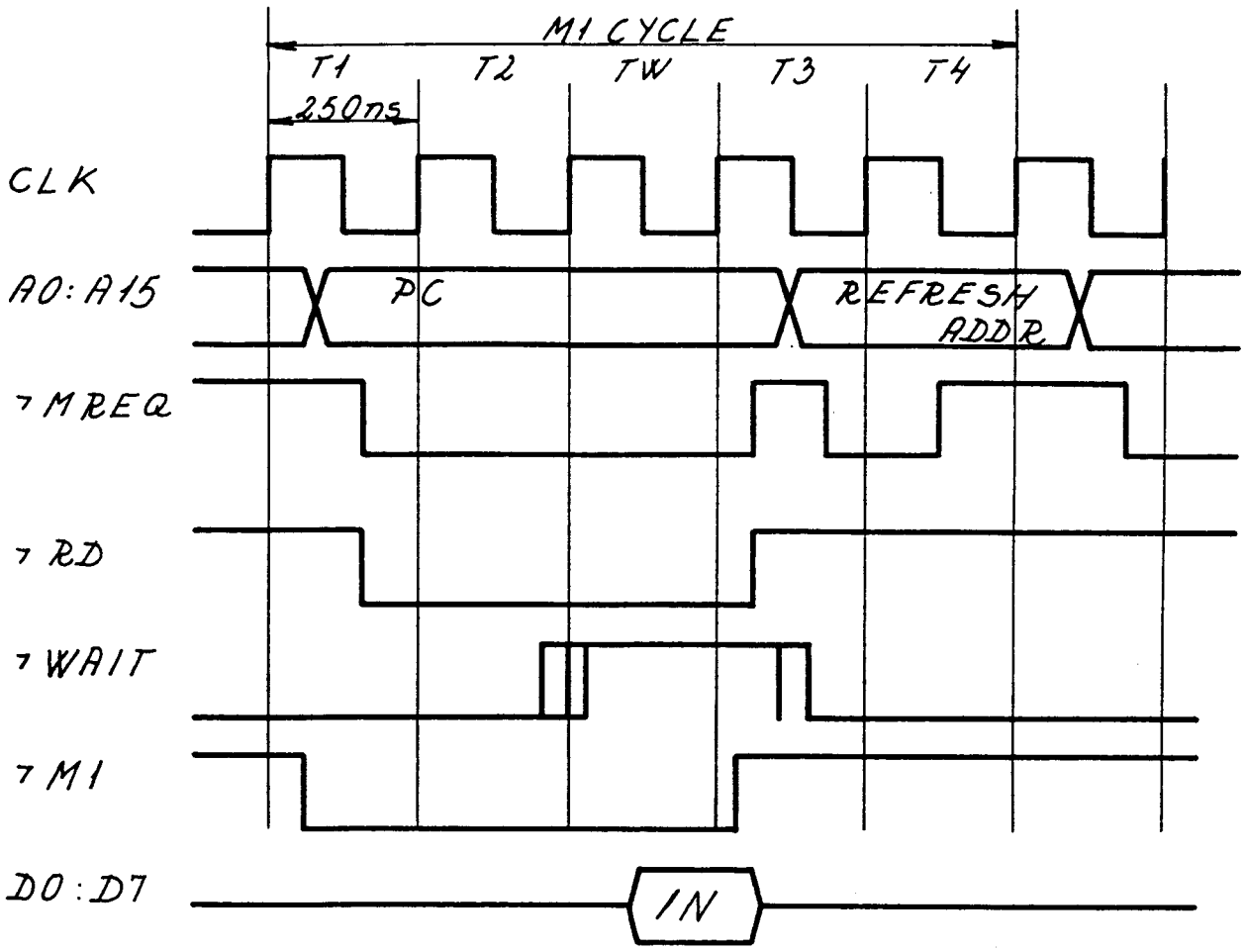


Fig. 2.3.3. INSTRUCTION OP CODE FETCH.

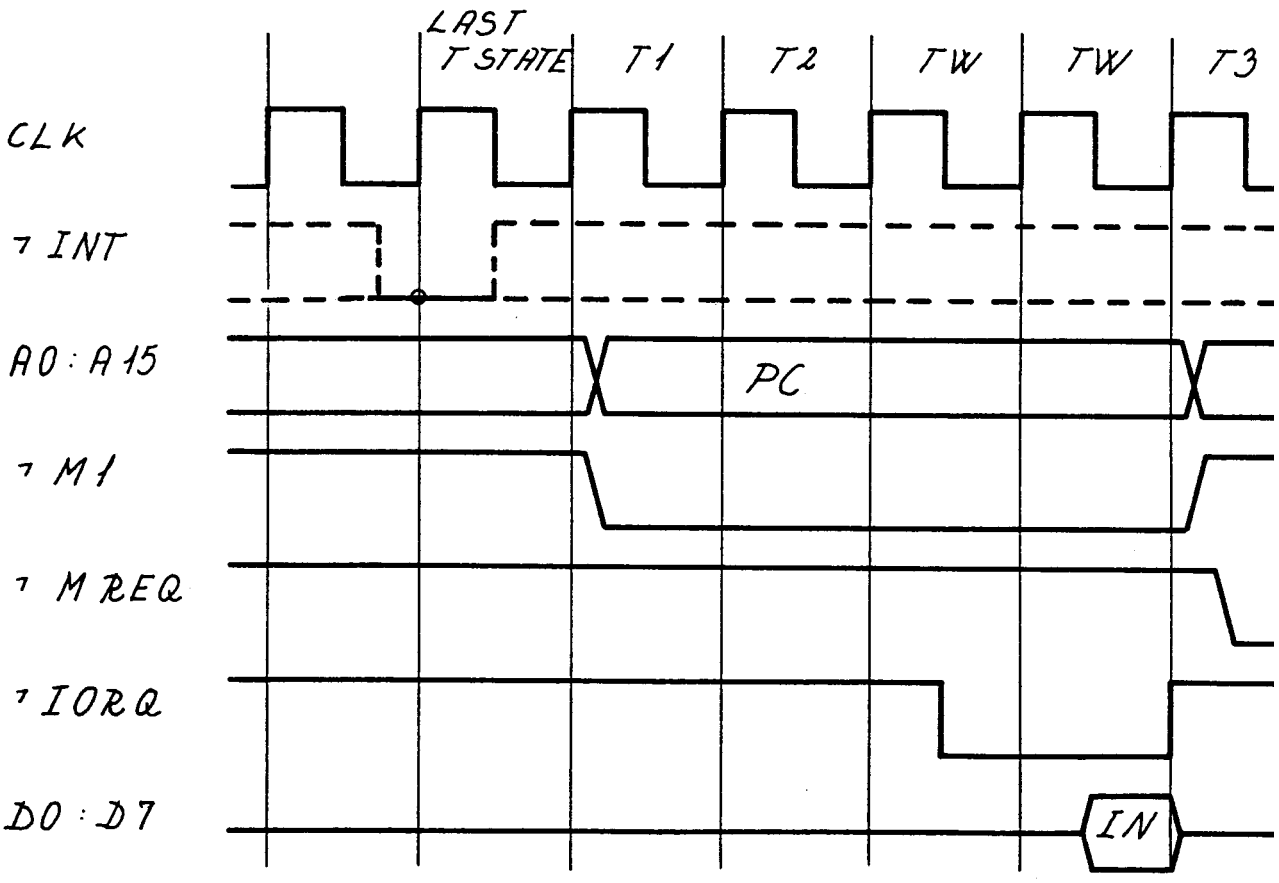


Fig. 2.3.4. INTERRUPT REQUEST/ACKNOWLEDGE.

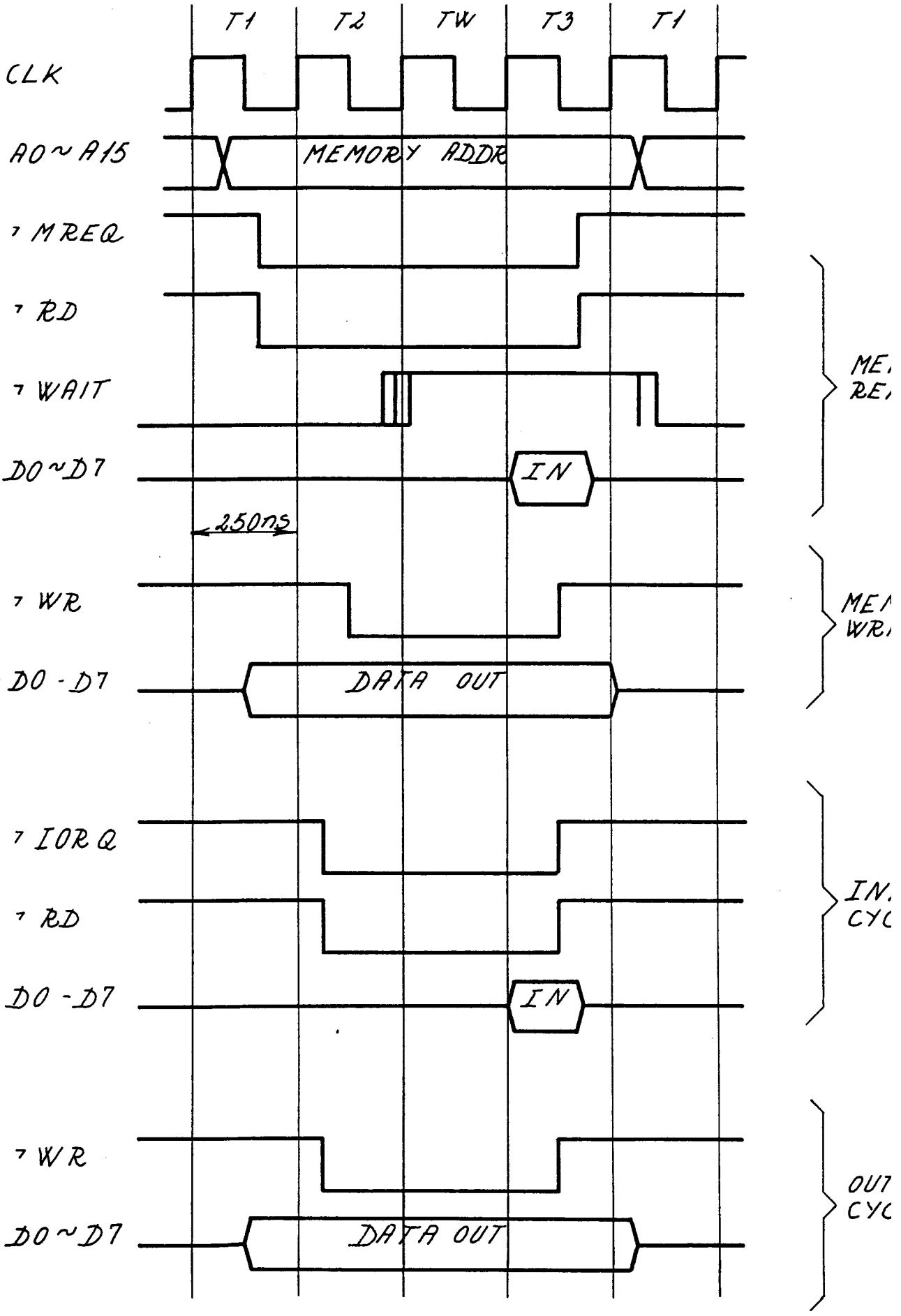


Fig. 2.3.5 TIMING WAVEFORM FOR Z-80A DIAGRAM

Address No.	Name	IC type	Comments
00	DISP	I 8275	PARAMETER PORT
01	-		COMMAND PORT
02	-		
03	-		
04	FLOP	μPD 765	MAIN STATUS REG
05	-		DATA REG
06	-	or I 8272	
07	-		
08	SIO	Z 80A - SIO2	DATA CHANNEL A
09	-		DATA CHANNEL B
0A	-		CONTROL CHANNEL A
0B	-		CONTROL CHANNEL B
0C	CTC	Z 80A - CTC	CHANNEL 0 to SIO A
0D	-		CHANNEL 1 to SIO B
0E	-		CHANNEL 2 INT DISP
0F	-		CHANNEL 3 INT FLOP
10	PIO	Z 80A - PIO	DATA KEYBOARD
11	-		DATA PARALLEL I/O
12	-		CONTROL KEYBOARD
13	-		CONTROL PARALLEL I/O
14	SWITCH		INPUT: 8 bit from switch
15	-		
16	-		OUTPUT: Enable Motor
17	-		to FLOP
18	DIS PROM		
19	-		
1A	-		
1B	-		
1C	SOUND		
1D	-		
1E	-		
1F	-		
20			
21			
EE			
EF			
F0	DMA	AM 9517A-4	Use of the 16 Registers
⋮	-	or	is described in the
⋮	-	I 8237-2	MANUFACTURER'S MANUAL
⋮	-		
⋮	-		
⋮	-		
⋮	-		
FF	-		

Fig. 2.3.6. ADDRESS DECODING

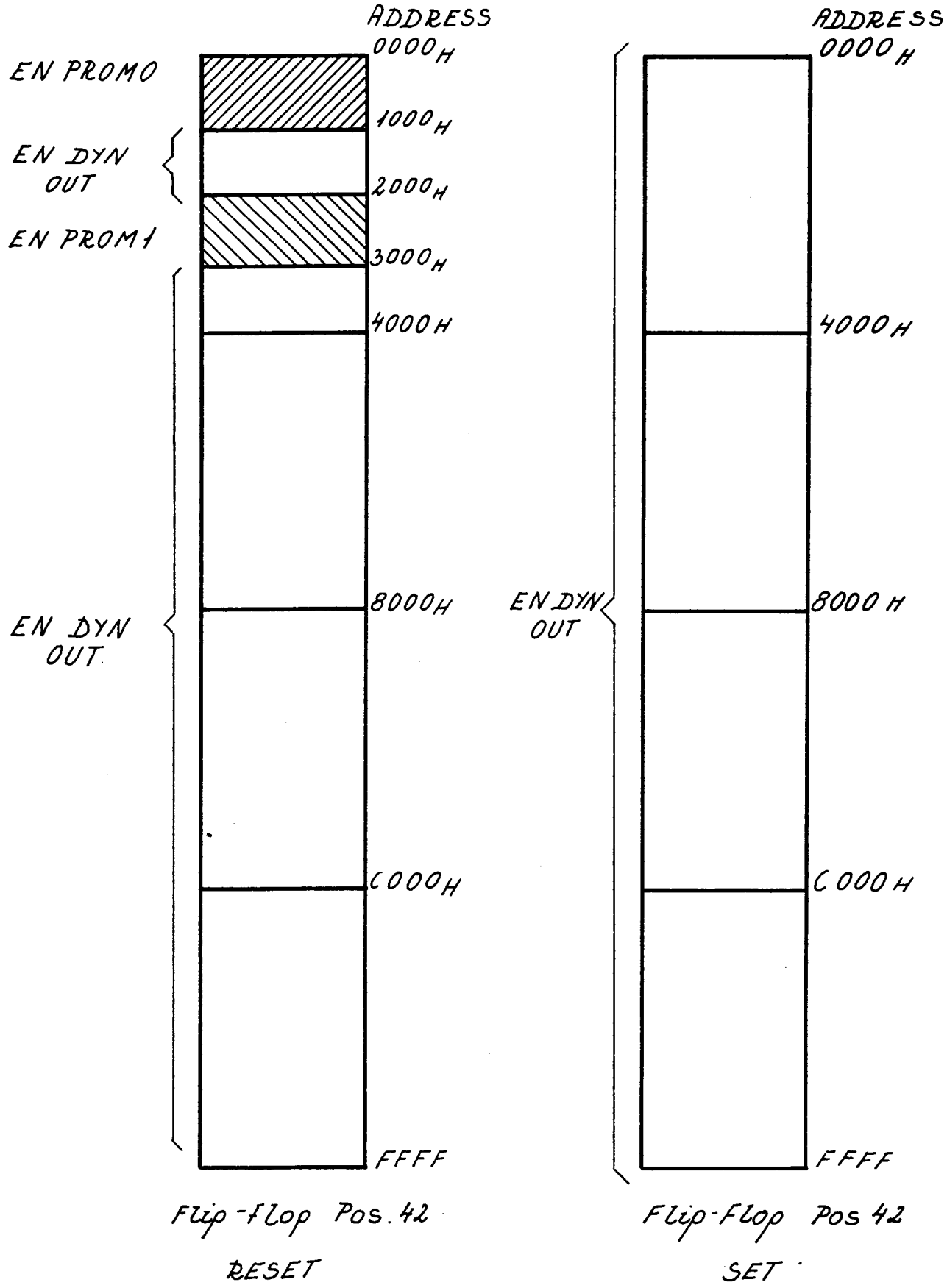


Fig 2.3.7. ADDRESS SPACE IN MIC 702.

mable, two port device which provides interface between the CPU and the two connectors for keyboard and for parallel I/O. The diagram is shown on page MIC07. The block diagram is shown in fig. 2.3.8. The internal structure of the Z80A-PIO consists of a bus interface, internal control logic, port A I/O logic, port B I/O logic, and interrupt control logic.

Each of the two port I/O logic is composed of 6 registers. The registers include: an 8-bit input register, an 8-bit output register, a 2-bit moderegister, an 8-bit mask register, an 8-bit input/output select register, and a 2-bit mask control register.

Before using the PIO it has to be programmed to the wanted Interrupt Vector and operating mode. This is described in manuals from Zilog.

The timing diagram in fig. 2.3.9 shows input from keyboard. The interrupt system is described in subsection 2.3.7.

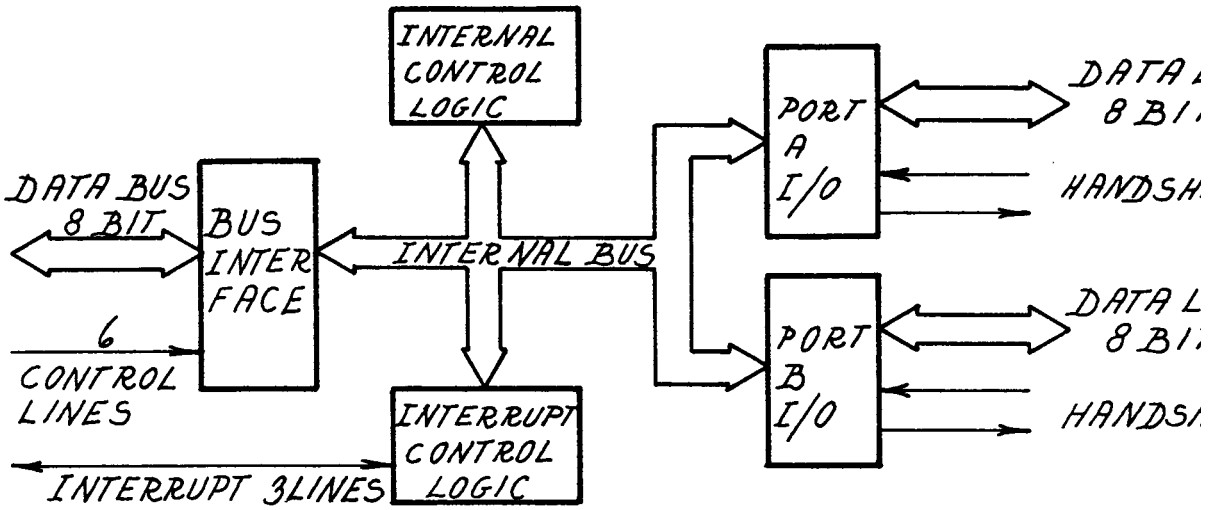
2.3.4 Serial Input/Output Controller

2.3.4

The Z80-SIO/2 (Serial Input/Output) is a dual-channel multi-function peripheral component designed to satisfy a wide varity of serial data communications requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller, but - within that role - it is configurable by system software so its "personality" can be optimized for a given serial data communications application.

The Z80-SIO/2 is in RC702 capable of handling asynchronous formats.

The Z80-SIO/2 can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. Block diagram for the Z80-SIO/2 is shown in fig. 2.3.10.
The internal structure includes Z80A CPU interface, internal con-



*
HANDSHAKE not used to KEYBOARD

Fig. 2.3.8. BLOCK DIAGRAM Z-80A PIO

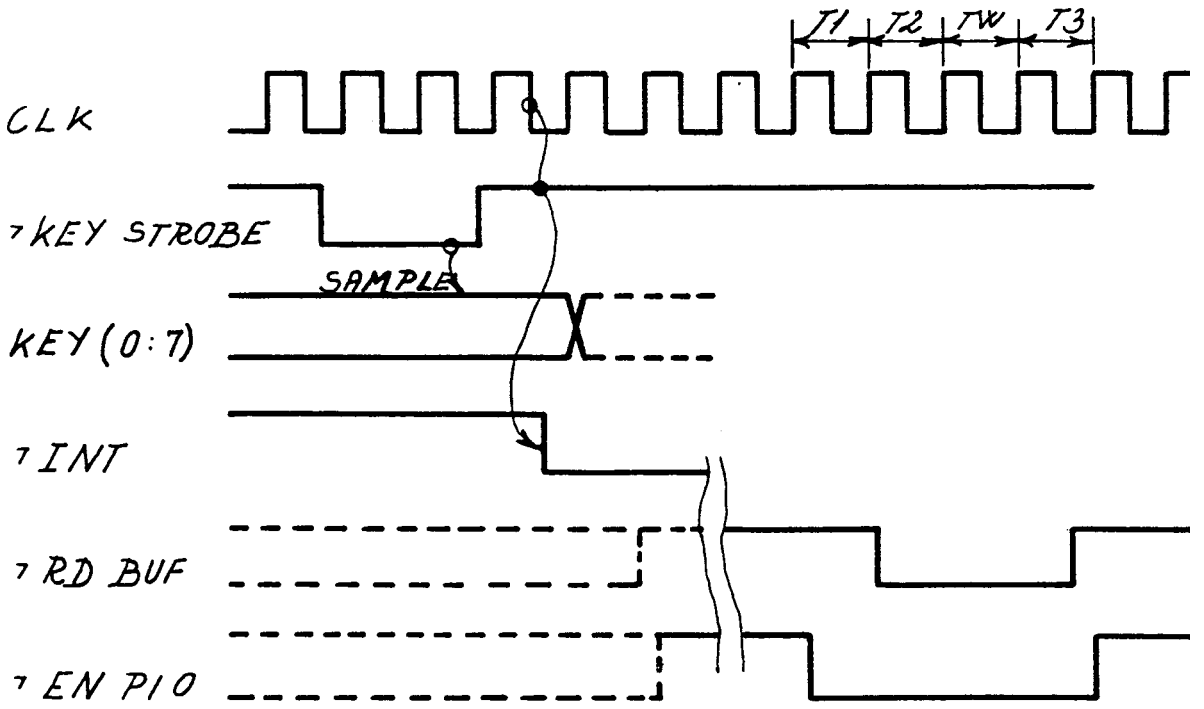


FIG. 2.3.9. TIMING DIAGRAM SHOWING INPUT FROM KEYBOARD

trol and interrupt logic, and two full duplex channels. Each channel contains read and write registers, and discreet control and status logic that provides interface to modems.

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs, Clear to Send (CTS) and Data Carrier Detect (DCD) are monitored by the discreet control logic under program control. All the modem control signals are general purpose in nature.

The programming for the SIO/2 is very complex and is described in manuals from Zilog.

2.3.5 Counter Timer Controller

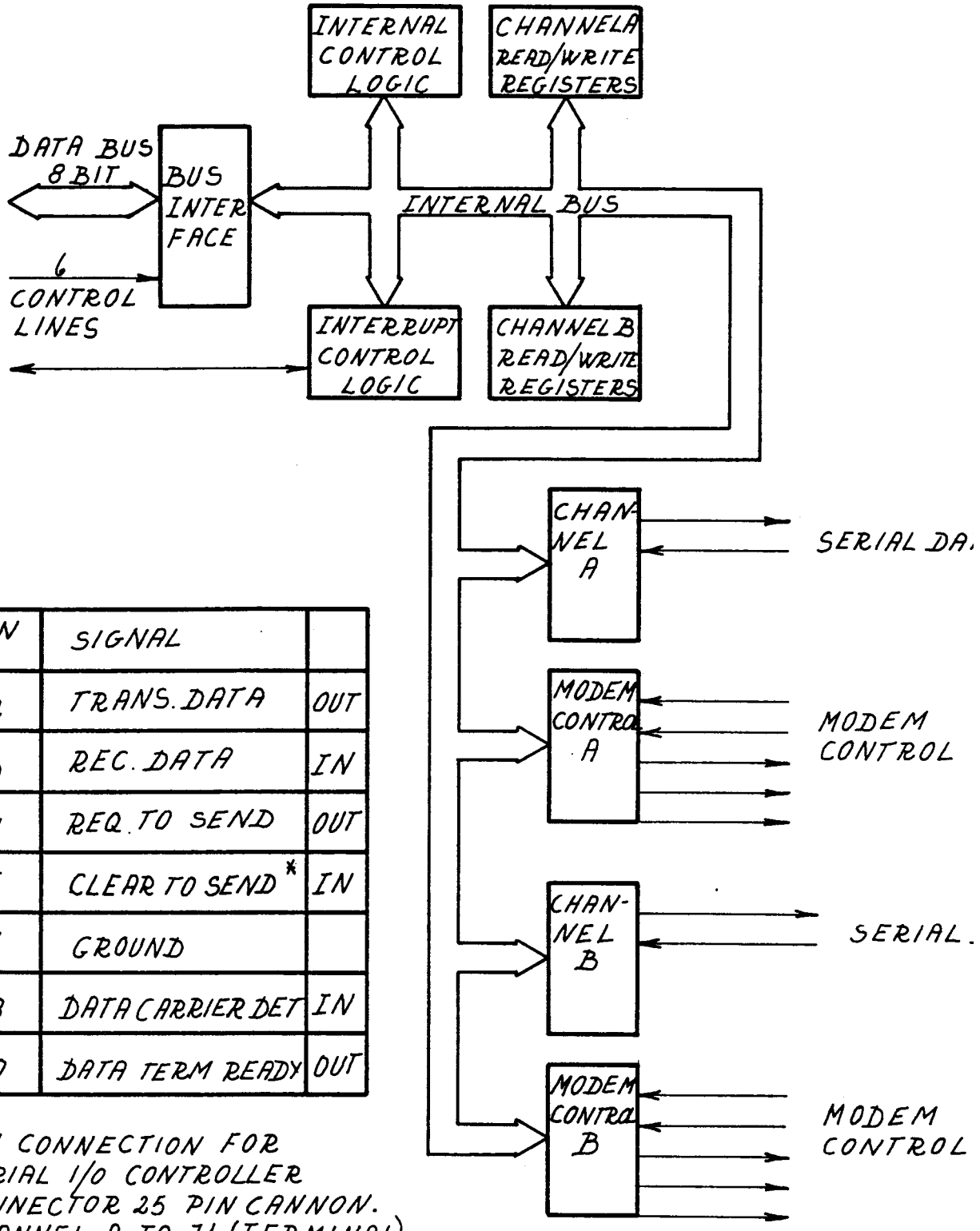
2.3.5

The Z80A Counter Timer Controller (CTC) is a programmable four channel device that provides counting and timing functions for the system. The diagram is shown in page MIC15 and the block diagram is shown in fig. 2.3.11.

The internal structure of the Z80-CTC consists of a Z80 CPU bus interface, internal control logic, four counter channels, and interrupt control logic. Each channel has an interrupt vector for automatic interrupt vectoring, and interrupt priority is determined by channel number with channel 0 having the highest priority.

The channel logic is composed of 2 registers, 2 counters, and control logic as shown in fig. 2.3.12. The registers include an 8-bit constant register and an 8-bit channel control register. The counters include an 8-bit readable down counter and an 8-bit prescaler. The prescaler may be programmed to divide the system clock by either 16 or 256.

Channel 0 and 1 are used to generate the clock to channel A and B in the Z80A-SIO/2. The clock delivered to the SIO is again divided in the SIO to make the baudrate for the terminal and printer connections. Input to these two channels is a clock of



PIN	SIGNAL	
2	TRANS. DATA	OUT
3	REC. DATA	IN
4	REQ. TO SEND	OUT
5	CLEAR TO SEND *	IN
7	GROUND	
8	DATA CARRIER DET	IN
20	DATA TERM READY	OUT

PIN CONNECTION FOR
SERIAL I/O CONTROLLER
CONNECTOR 25 PIN CANNON.
CHANNEL A TO J1 (TERMINAL)
CHANNEL B TO J2 (PRINTER)
* IF PRINTER CONNECTOR TO ↑ BUSY.

Fig. 2.3.10. BLOCK DIAGRAM FOR Z-80A SIO/2
AND SIGNAL CONNECTION TO J1 AND J2.

0.614 MHz. How the clock is divided in the SIO is shown in fig. 2.3.13.

Channel 2 and 3 are initiated in counter mode with interrupt enabled and with a time constant of 1. This means that for every clock input an interrupt is sent to the CPU. Channel 2 is connected to the display controller and channel 3 is connected to the floppy controller, and in this way their interrupt is connected to the CPU.

2.3.6 Interrupt System

2.3.6

The CPU has two interrupt inputs, a software maskable interrupt and a non-maskable interrupt. The non-maskable interrupt (NMI) cannot be disabled by the program and is not used in MIC702. The CPU can be programmed to respond to maskable interrupts in one of three modes. In MIC702 mode 2 is selected. In this mode a single 8-bit byte from the controller (the interrupt vector) is used to make an indirect call instruction.

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted a special M1 cycle (INTA) is generated. During this M1 cycle IORQ becomes active (instead of MREQ) indicating the INTA cycle. The Z80 peripherals have an interrupt enable input (IEI) and an interrupt enable output (IEO) and are connected in daisy chain. The peripheral with IEI high and IEO low, will during INTA place the preprogrammed 8-bit interrupt vector on the data bus.

IEO is held low until a return from interrupt (RETI) instruction is executed by the CPU while IEI is high. The 2-byte RETI instruction is decoded internally by the peripheral for this purpose.

Fig. 2.3.14 shows the daisy chain interrupt system in MIC702.

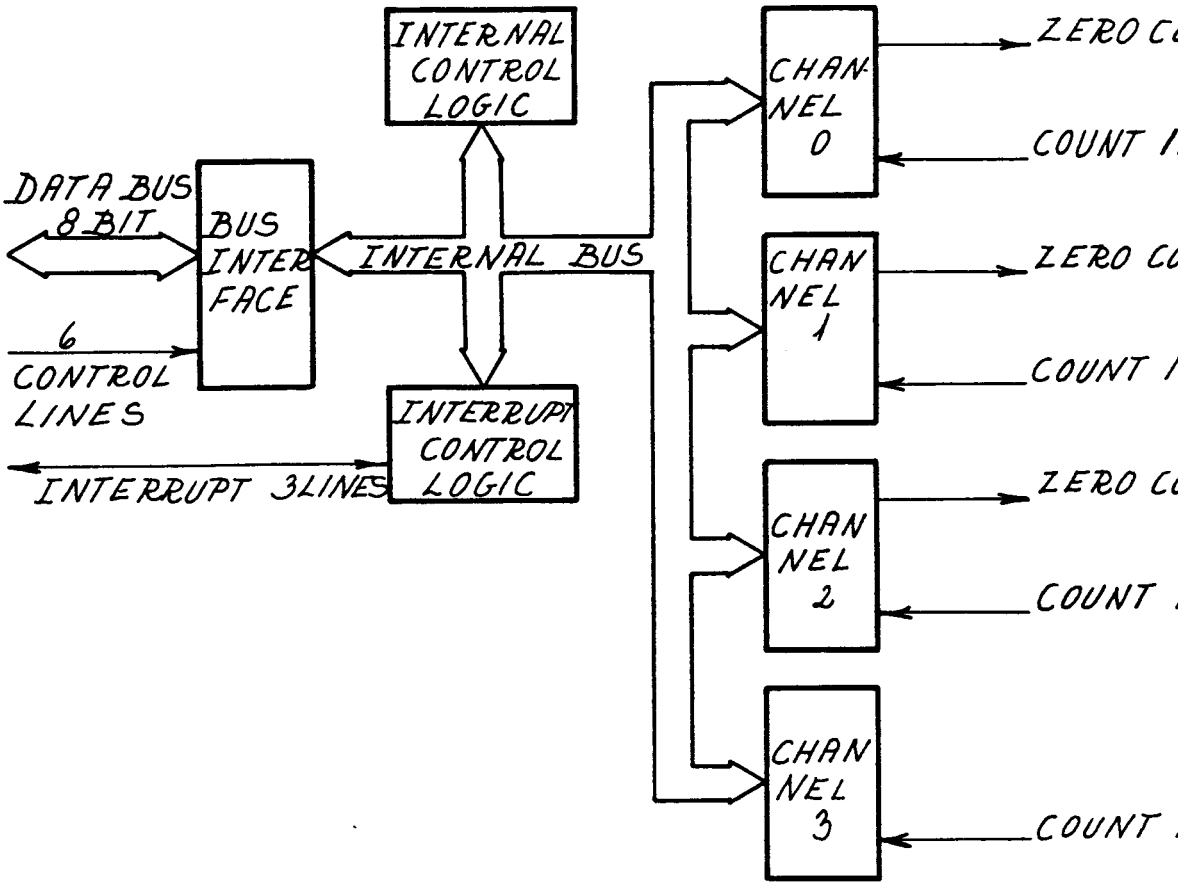


Fig. 2.3.11. BLOCK DIAGRAM FOR Z-80A CTC.

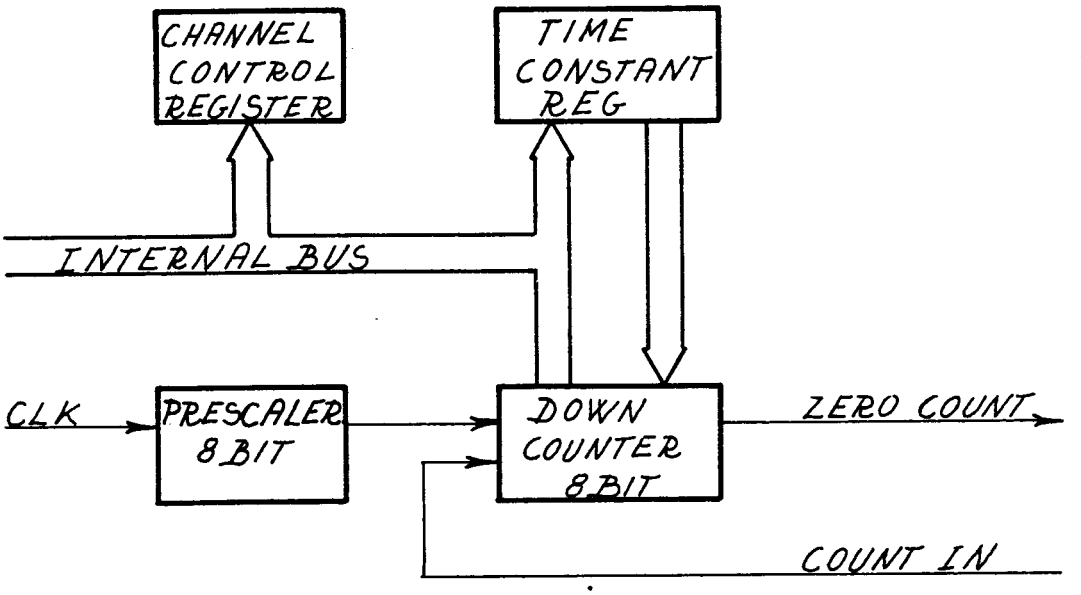
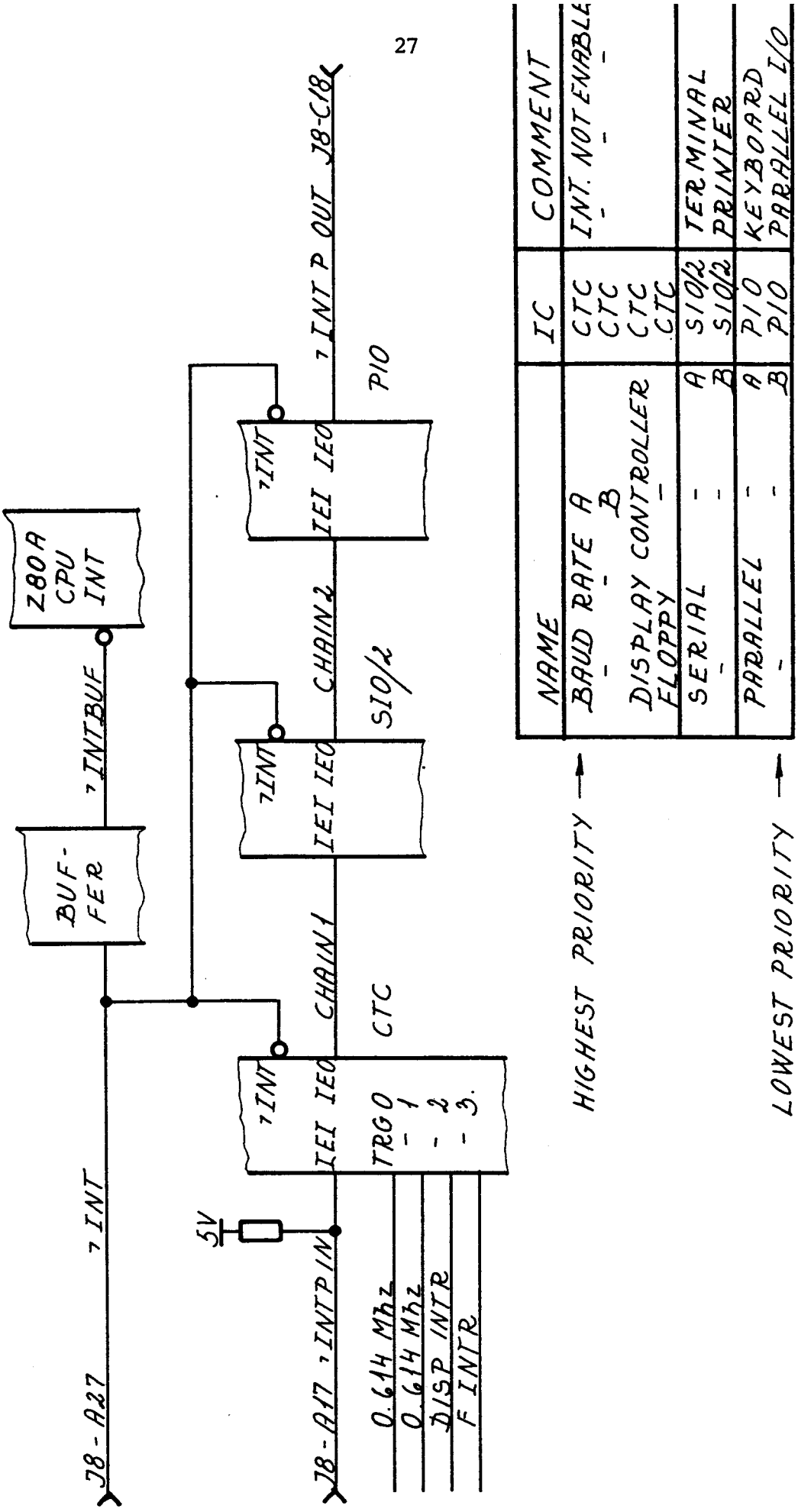


Fig. 2.3.12. BLOCK DIAGRAM for ONE CHANNEL in Z-80A CTC.

CTC INPUT	CLOCK Devided by	CTC OUTPUT	SIO Devided by	SIO Periode time	SIO BAUDRATE
T in µsec	decimal	T in µsec	decimal	µsec	
0.614	193	314	64	19.970	50
0.614	128	208	64	13.310	75
0.614	88	144	64	9.222	110
0.614	64	104	64	6.667	150
0.614	32	52	64	3.333	300
0.614	64	104	16	1.667	600
0.614	32	52	16	833.3	1200
0.614	16	26	16	416.7	2400
0.614	8	13	16	208.3	4800
0.614	64	104	1	104.2	9600
0.614	32	52	1	52.1	19200

Fig. 2.3.13. GENERATING BAUDRATE in RC 702.



NAME		IC	COMMENT
BAUD RATE A		CTC	INT. NOT ENABLE
- B		CTC	-
DISPLAY CONTROLLER		CTC	
FLOPPY		CTC	
SERIAL	A	SIO/2	TERMINAL
-	B	SIO/2	PRINTER
PARALLEL	A	PIO	KEYBOARD
-	B	PIO	PARALLEL I/O

Fig. 2.3.14. INTERRUPT PRIOITY IN RC 702

2.3.7 ROM Memory

The ROM, Read Only Memory, contains the autoload program. After a reset signal is generated, the CPU starts to execute the program stored in POS. 66. In subsection 2.3.3 is shown how this addressing is made. In a test situation both ROM POS. 66 and 65 may contain a ROM. The ROMs are normally 2 K bytes PROM.

2.3.8 RAM Memory

The RAM, Random Access Memory, is shown in 3 blocks in the block diagram: the TIMING GEN block, the 64 K BYTES RAM block, and the REG. block. This subsection describes these 3 blocks. The circuit diagram is on page MIC05. The timing generator is made using the IC I8202. This circuit makes all the signals which the RAM circuits need. Fig. 2.3.15 shows the block diagram for the I8202 and the timing diagram for the whole RAM circuit is shown in fig. 2.3.16.

2.3.9 DMA Controller

The DMA controller to MIC702 is based on the Am9517A-4 from Advance Micro Devices or an 8237-2 from Intel. The IC is designed to be used in conjunction with an external 8-bit address register made by an 74LS373. The circuit diagram is shown in MIC06. The Am9517A-4 contains 4 channels which have full 64 K address and word count capability.

The four channels are in MIC702 used in the following way:

channel 0 : External debugger
channel 1 : Floppy disk controller
channel 2 : Visual display controller
chAnnel 3 : Visual display controller.

The block diagram for Am9517A-4 is shown in fig. 2.3.17.

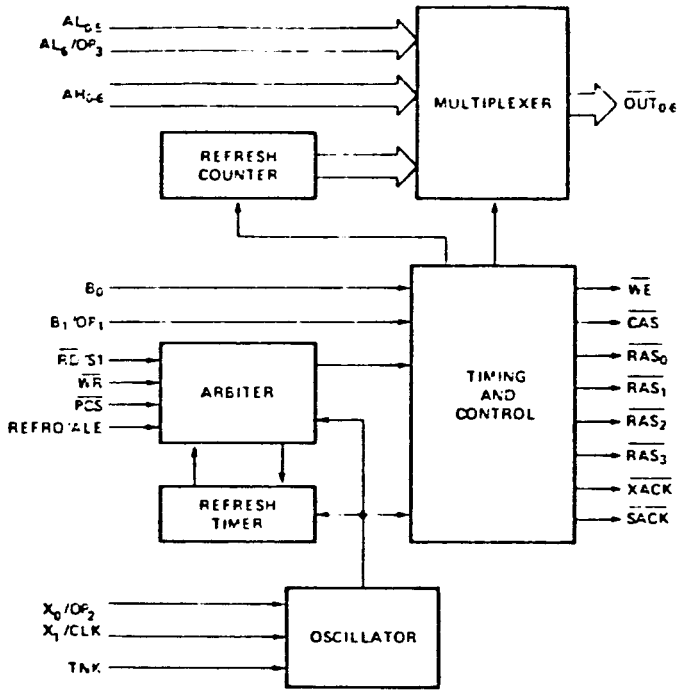


Fig. 2.3.15 . Block Diagram for I 8202 RAM Controller

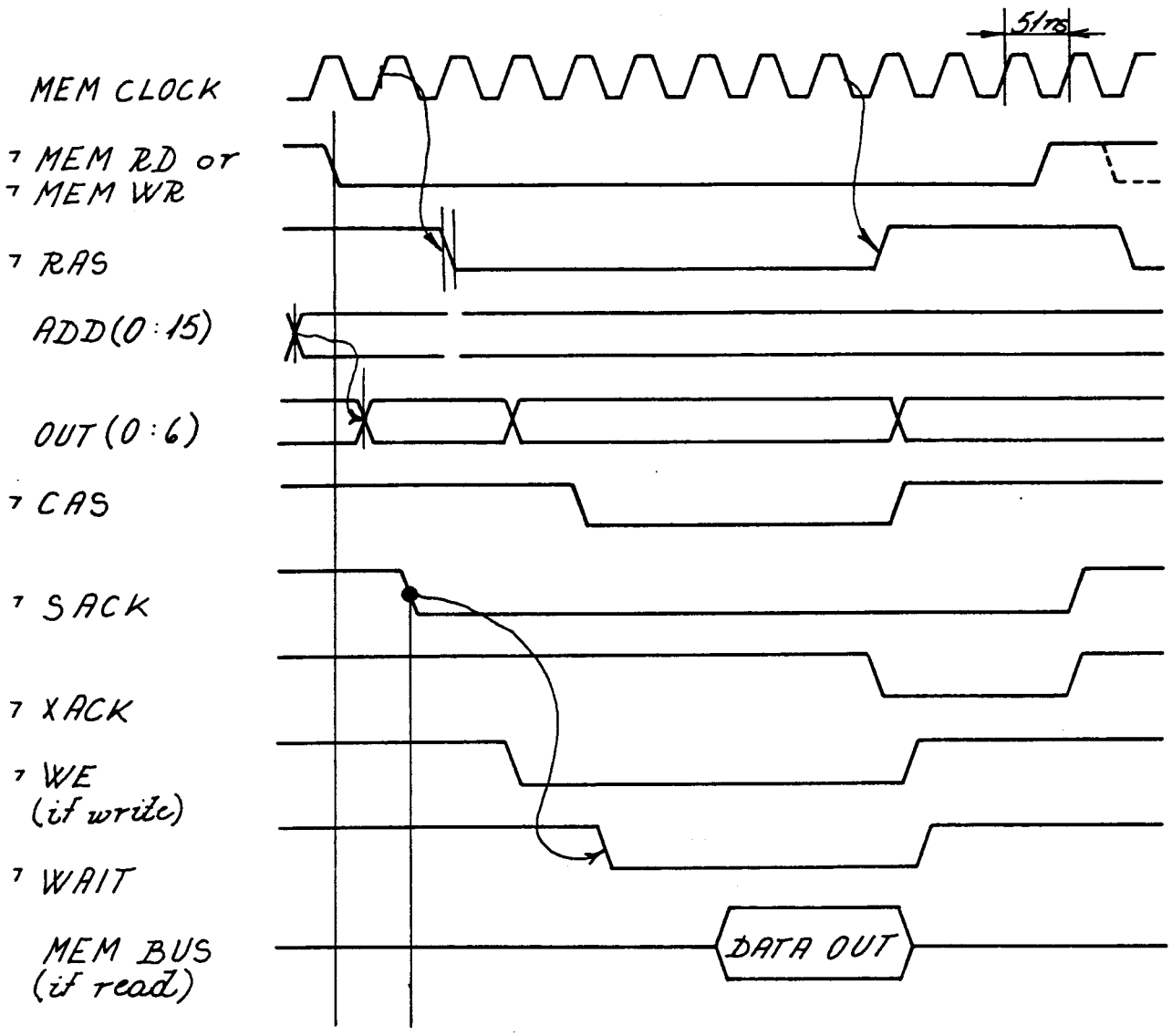


Fig. 2.3.16. TIMING DIAGRAM for RAM SYSTEM

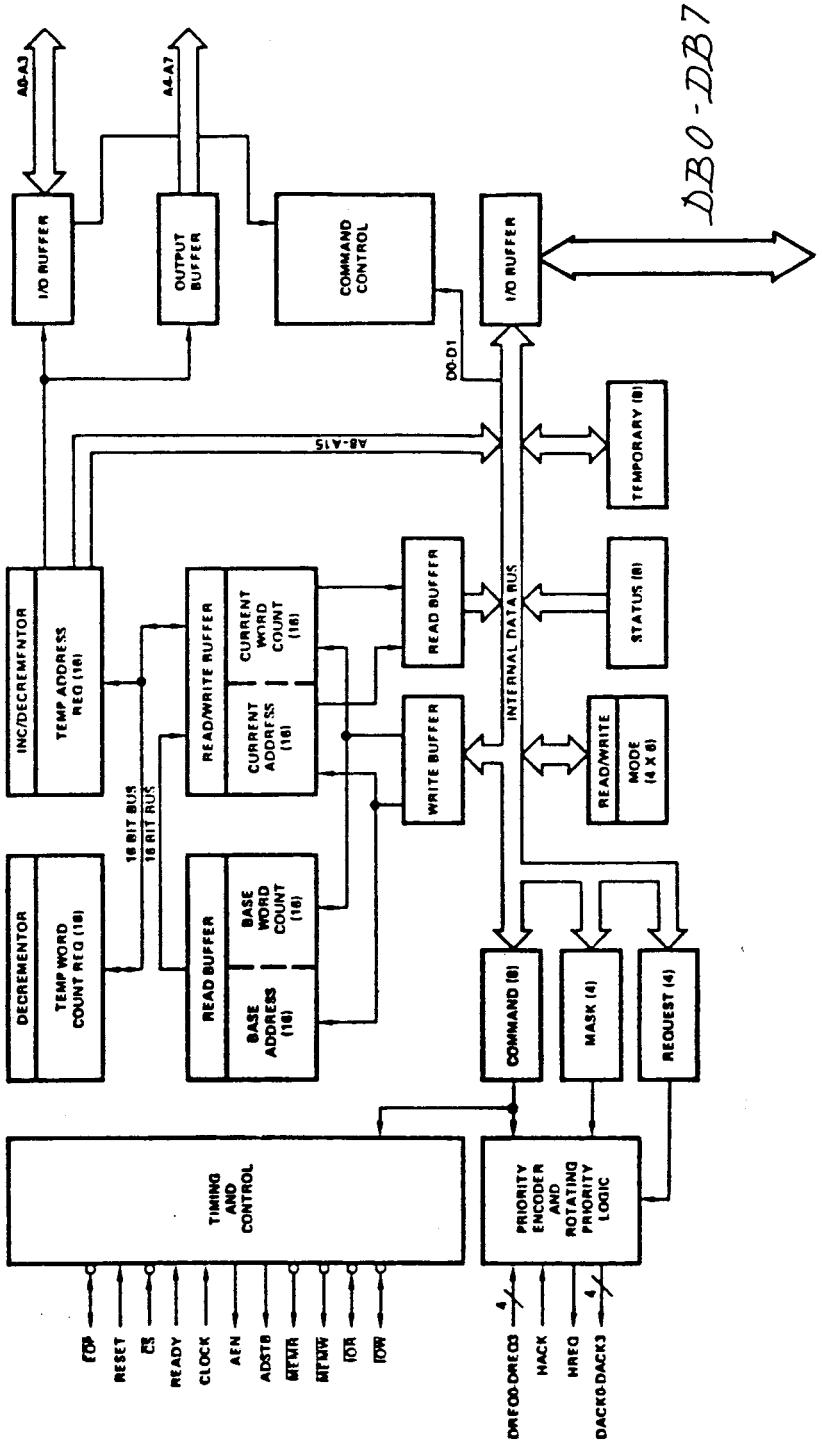
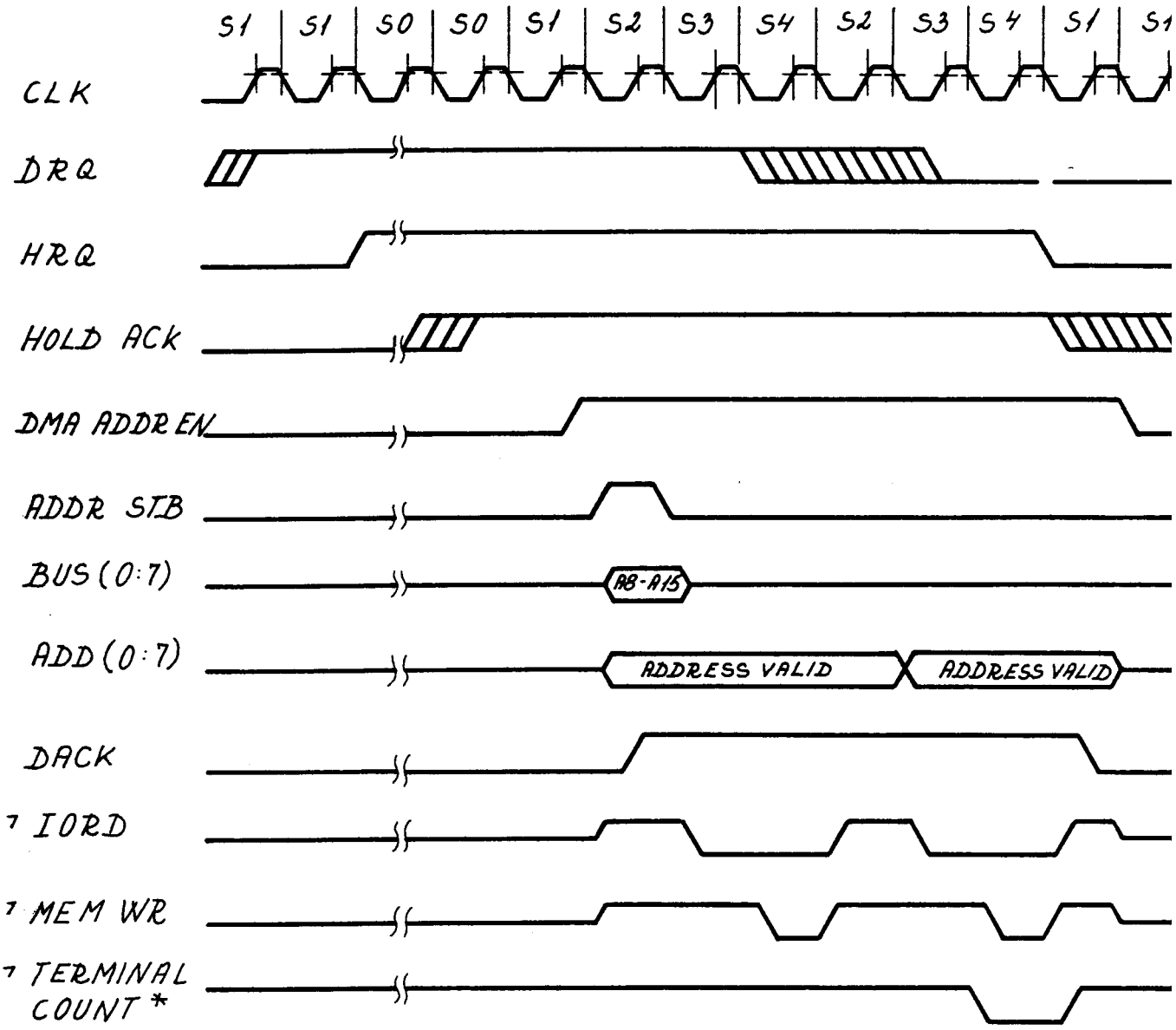


Fig. 2.3.17. Block Diagram for Am 9517A-4.



* Only if last byte in the block.

Fig. 2.3.18. TIMING DIAGRAM for Am 9517A-4 DMA-CONTROLLER.

Fig. 2.3.18 shows the timing diagram for a normal operation of Am9517A-4.

More specific description of the units. may be obtained from one of the two manufacturers.

2.3.10 Select Switches 2.3.10

8 switches are situated on the board. Their position may be sensed by the program. The switches are mainly used when the ROM is replaced with a testprogram ROM. One switch (BUS 7) is used to switch between Mini and Maxi floppy. The circuit may be seen in diagram MIC15.

2.3.11 Video Display Controller 2.3.11

The video display controller is based on the 8275 programmable CRT controller from Intel. The device interfaces the CRT raster scan display with the system. The controller refreshes the display by buffering the information from the memory and it keeps track of the display position of the screen. Fig. 2.3.19 shows a block diagram for the 8275 controller. The program initiates the controller to make the wanted picture. The initiations needed may be seen in the description from Intel.

The initiation made in MIC702 is listed in fig. 2.3.20.

The video display controller needs a number of registers, etc. to support it. This circuits are shown in diagram pages MIC11 to MIC14. Fig. 2.3.21 shows a block diagram with this circuit.

The output from the video display controller system is made with comp. sync and with normal TTL signal output. In RC702 the comp. sync. is used and fig. 2.3.22 shows the timing of this signal.

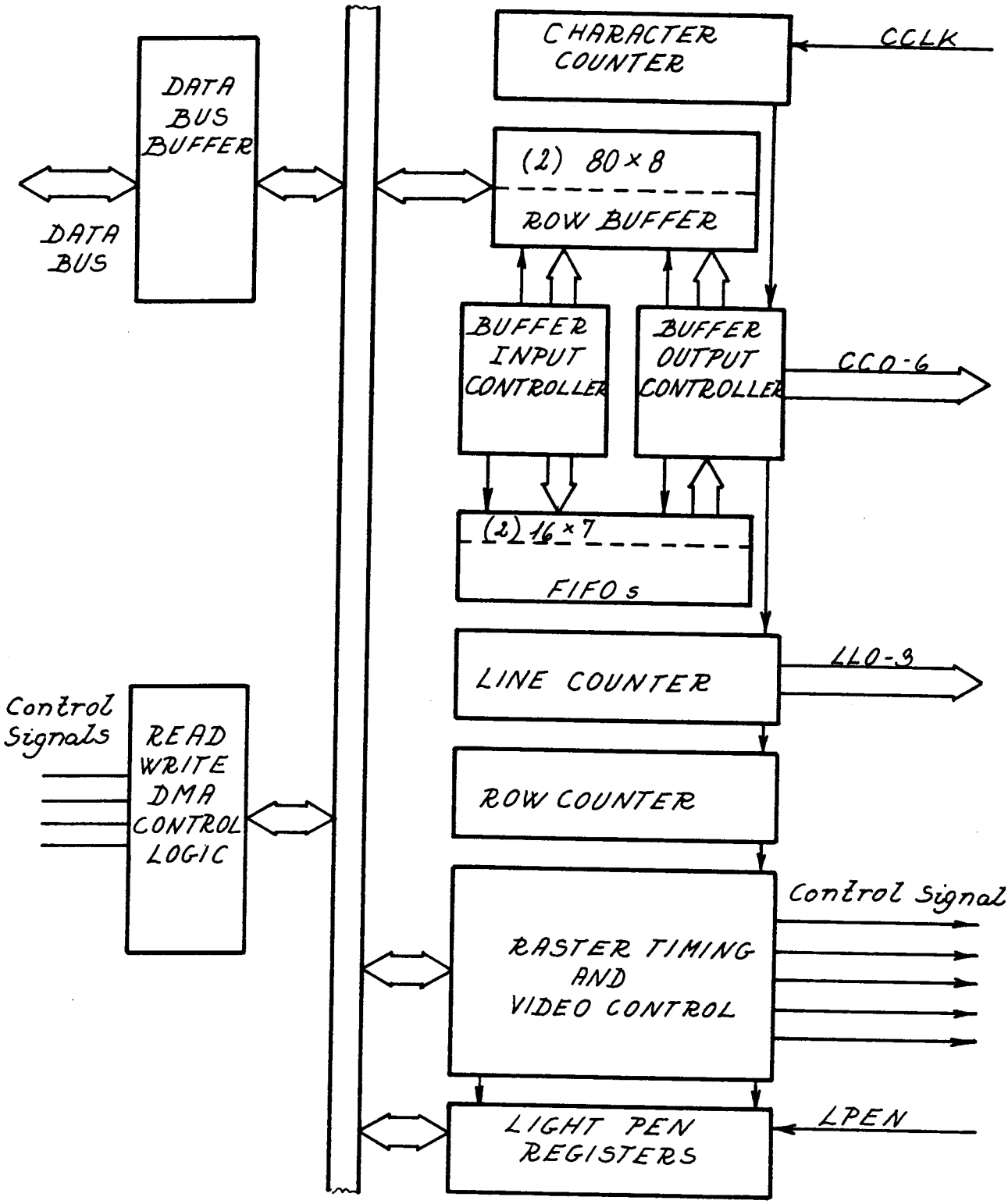


Fig. 2.3.19 BLOCK DIAGRAM FOR 8275.

Initiation of 8275 makes the following picture on the monitor used.

		Comments
80	Chars pr. row	
25	Rows of charaters	
5	Char. Dot matrix width	Made in Char. generato
9	- - - height	- - - -
7	Char cell width	
11	- - height	
50 Hz	frame freguency	Sync. with mains freq
275	active scan lines	
33	vertical blanking intervals	
308	Total scan lines	
15.4 Khz	line frequency	
65 µsec	line periode time	
150 µsec	vertical sync time	Made with monostable
28	char. time for horz. blank	
108	char. time each line	
0.601 µsec	char time	
86 nsec	DOT time	
11.64 MHz	DOT frequency	
4.5 µsec	Horizontal sync width	Made with monostable
5,8 µsec	- - delay	- - -
	Blinking field cursor	

Fig. 2.3.20. INITIAtion of 8275 in MIC 702.

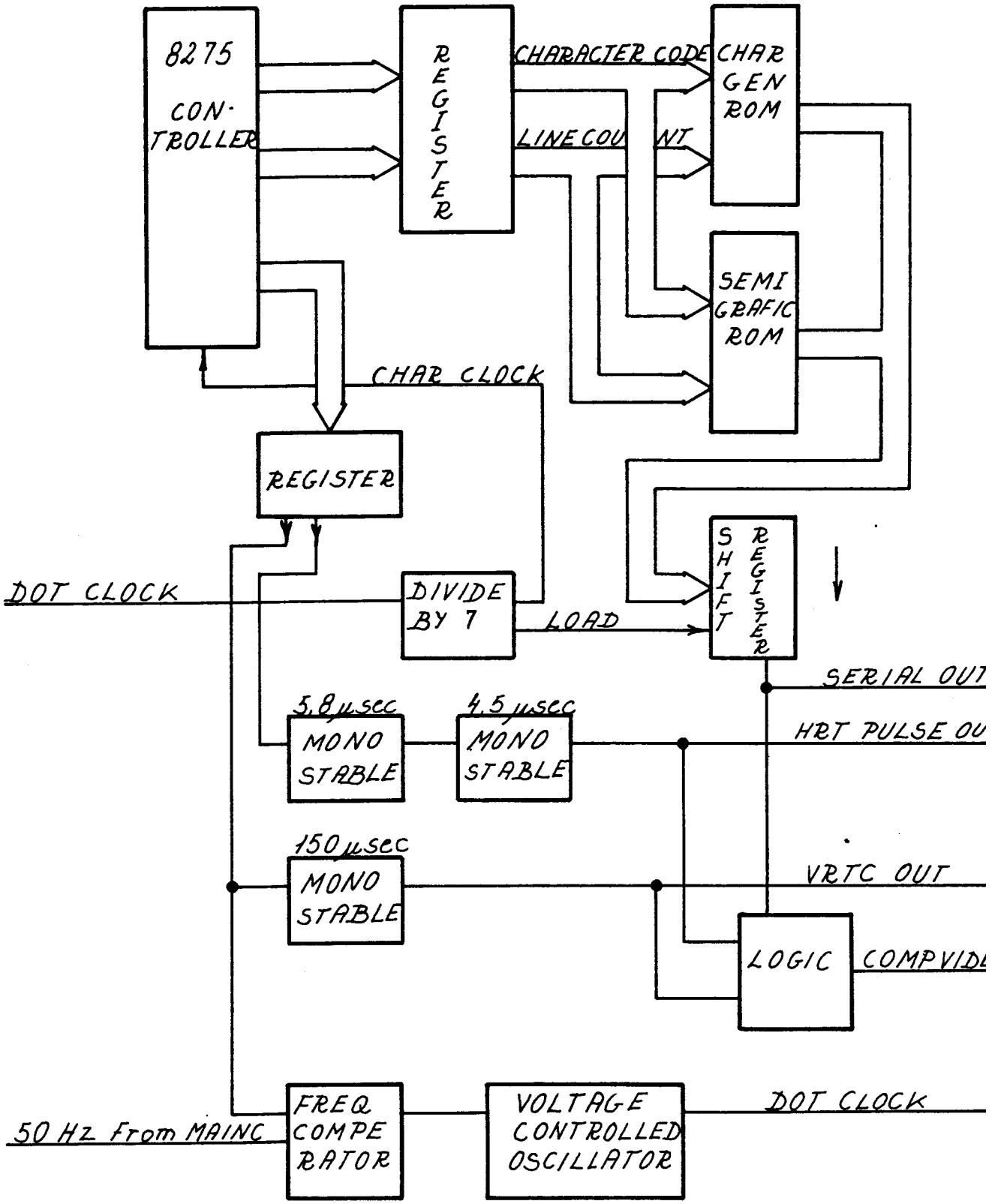
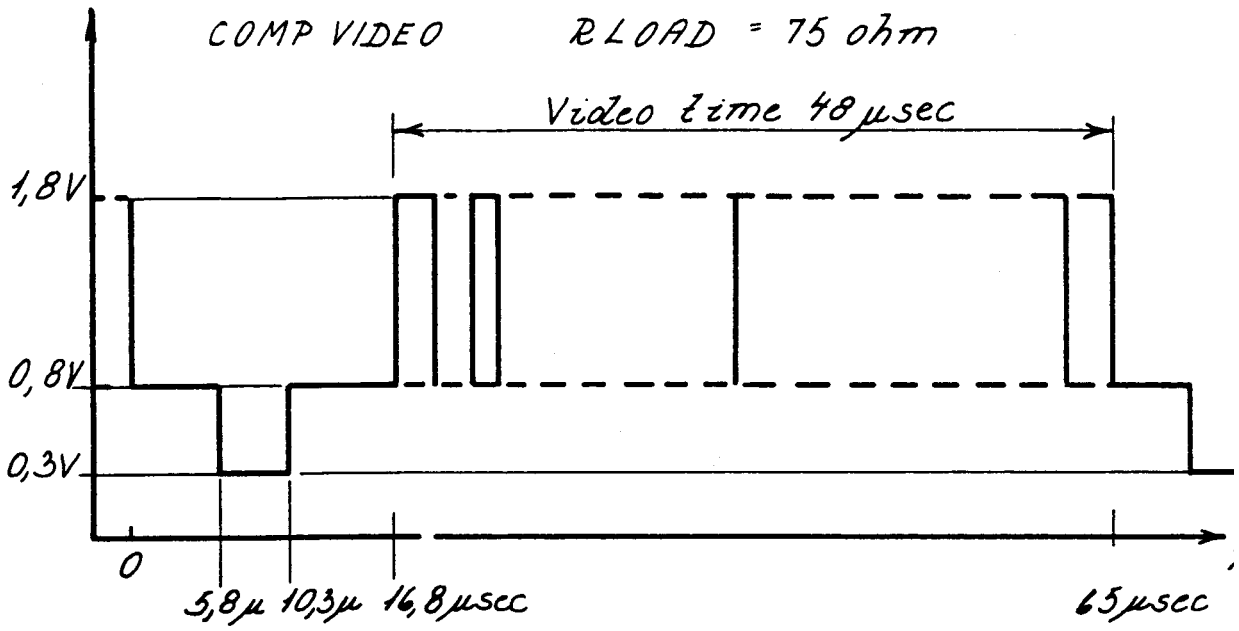
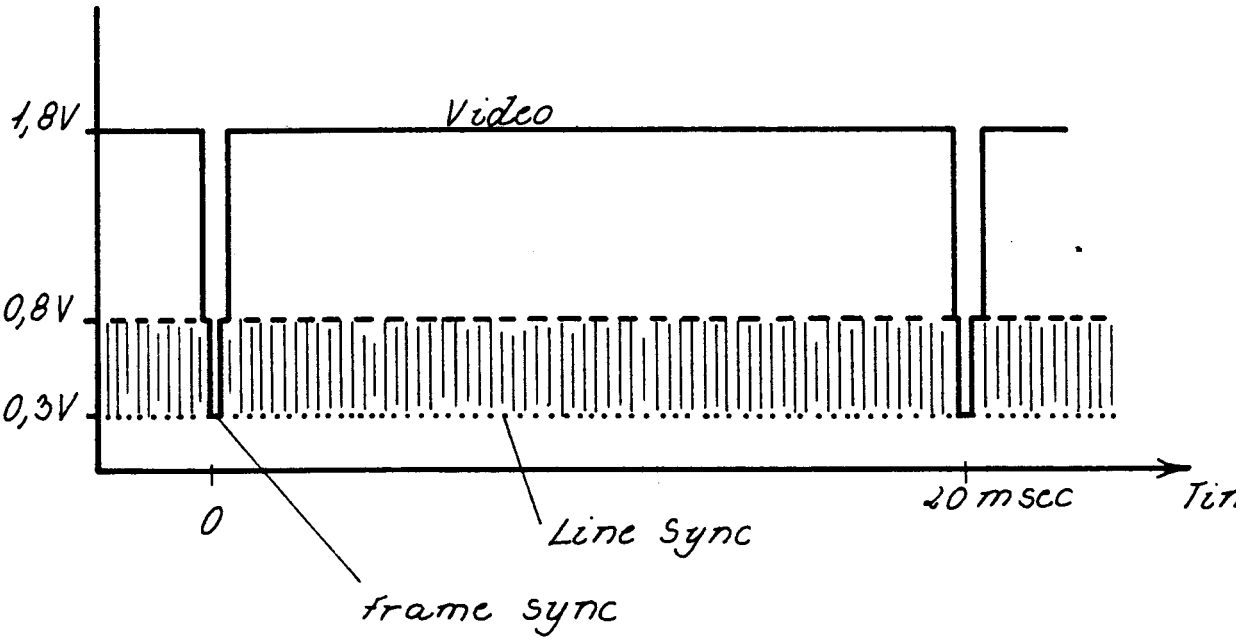


Fig. 2.3.21. BLOCK DIAGRAM FOR VIDEO DISPLAY SYSTE

NOTE ONLY COMP SYNC IS USED I MIC 702.



Comp. Sync signal for one Line.



Comp. Sync signal for one frame.

Fig. 2.3.22. TIMING DIAGRAM COMP. SYNC SIGNAL
To RC 702.

2.3.12 Floppy Disk Controller

The floppy disk controller to MIC702 is based on the FDC chip uPD765 from NEC or 8272 from Intel. The chip contains the circuitry and control functions for interfacing the processor to 4 floppy disk drives. It supports both IBM3740 single density format (FM) and IBM system 34 double density format including double sided recording.

Fig. 2.3.23 shows a block diagram for the controller chip.

The uPD765 contains two registers which may be accessed by the program. The 8-bit main status register contains the status information of the FDC and may be accessed at any time. The 8-bit data register (actually consists of several registers in stack with only one register present to the bus at a time), which stores data, commands, parameters, and floppy disk drive information. Fig. 2.3.24 shows the information stored in the status register.

Fig. 2.3.25 shows the information delivered to and from the data register during a read or write instruction to the controller. The programming of uPD765 is very complex and is described by the manufacturer. The controller interfaced to both Maxi- and Mini disk drives. The circuits on diagrams MIC09 and MIC10 show this.

Fig. 2.3.26 shows the data media floppy diskette. The diskette contains a number of tracks which again are divided into a number of sectors as shown in fig. 2.3.26. The controller is able to format, read, or write the diskette. Information about the actual formats used is available in the software manuals. Fig. 2.3.28 shows the two recording methods used.

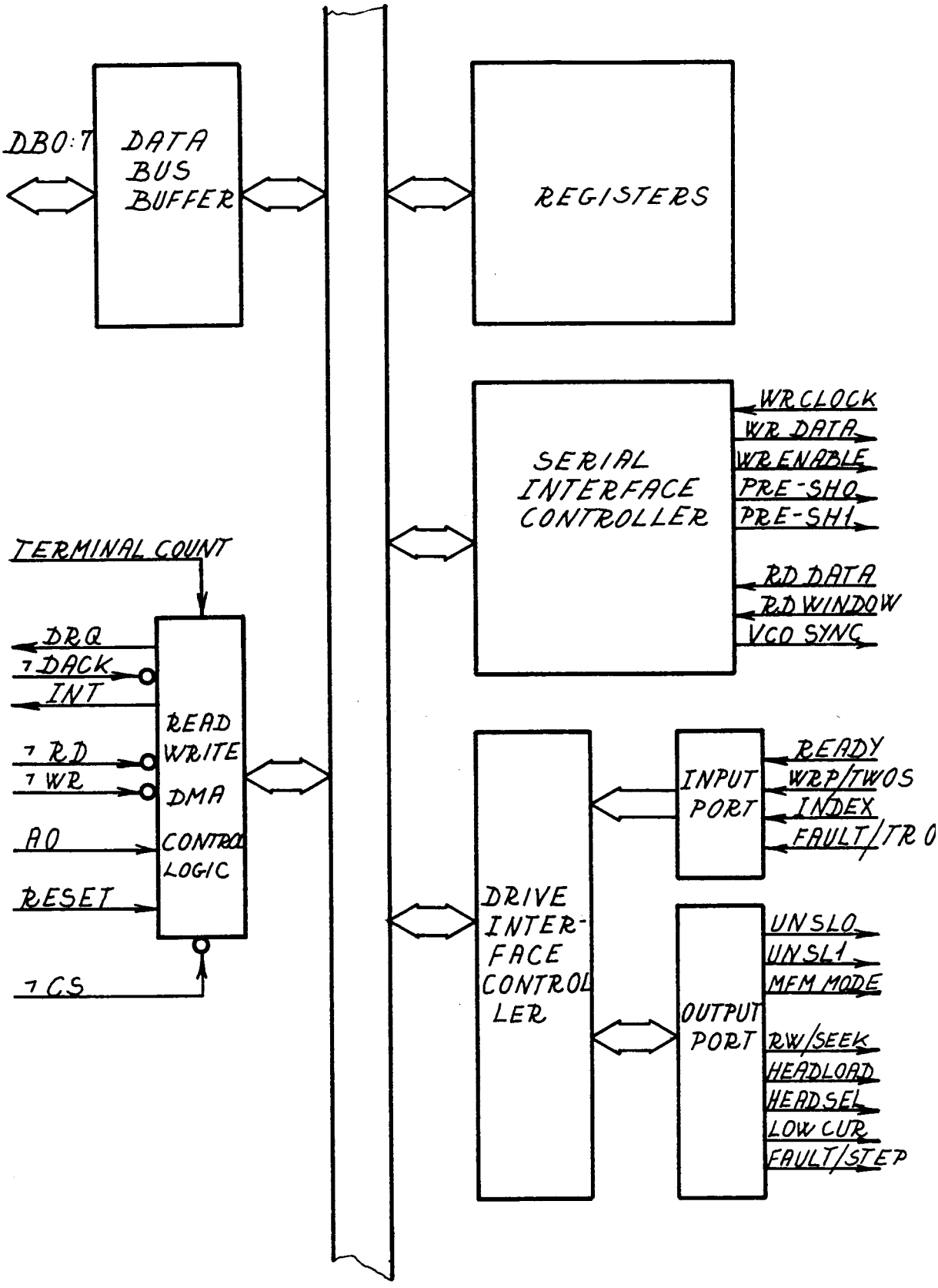
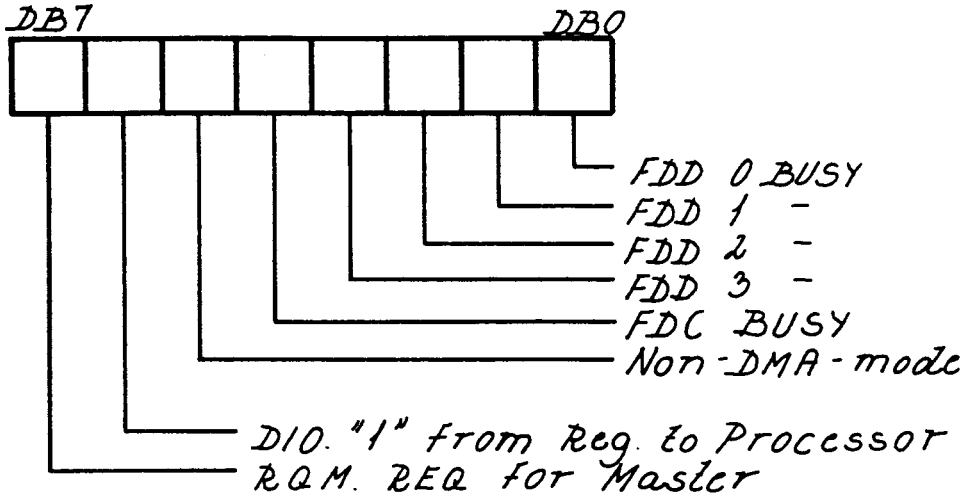
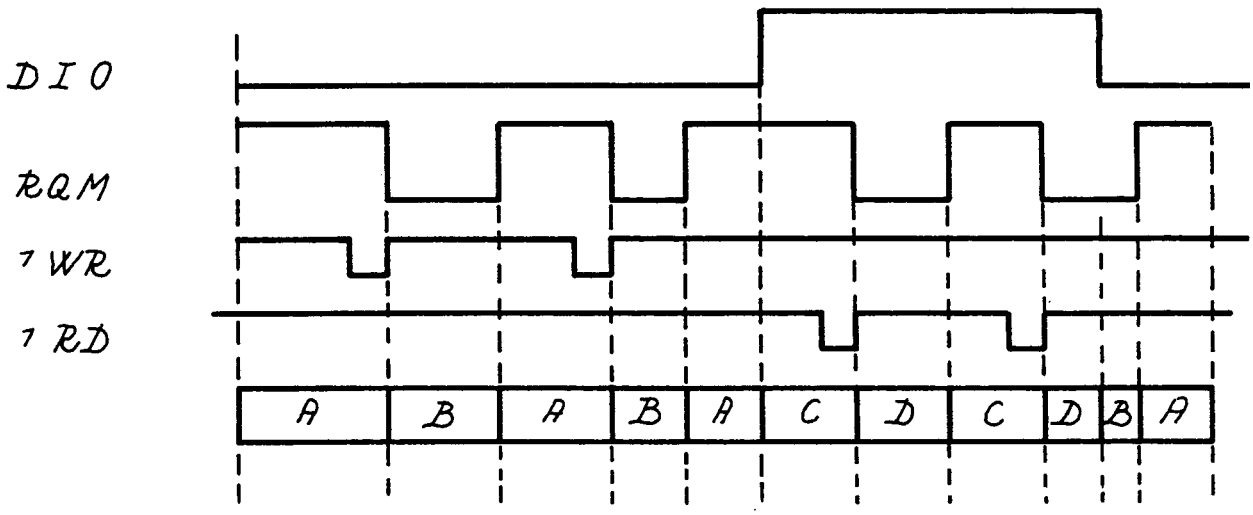


Fig. 2.3.23. BLOCK DIAGRAM FOR μ PD 765 FLOPPY DISK CONTROLLER CHIP.

STATUS REGISTER (MAIN STATUS REGISTER)

One 8-bit byte with inf. of the controller.





A Data register ready to be written into by

B - - not ready - - - - -

C - - ready for next byte to be read

D - - not ready - - - - -

Fig. 2.3.24. STATUS REGISTER IN μ PD 765.

Data Register of 8-bit bytes
(Several registers in a stack)
All commands contains a command phase, an execution phase and a result phase.

PHASE	R/W	DATA BUS D7 D6 D5 D4 D3 D2 D2 D0	REMARKS
READ DATA			
Command	W	MT MF SK 0 0 1 1 0	
	W	X X X X X HD US1 US0	
	W	Cylinder number (current)	
	W	Head address	
	W	Record (Sector number)	
	W	Number (of data bytes/sector)	
	W	End of track	
	W	Gap Length	
	W	Data Length	
Execute			
Result	R	Status 0	
	R	- 1	
	R	- 2	
	R	Cylinder number (current)	
	R	Head address	
	R	Record (sector number)	
	R	Number (of data bytes/sector)	

Fig. 2.3.25. INFORMATION SUPPLIED TO AND FROM DATA REGISTER IN μPD 765 DURING READ OR WRITE.

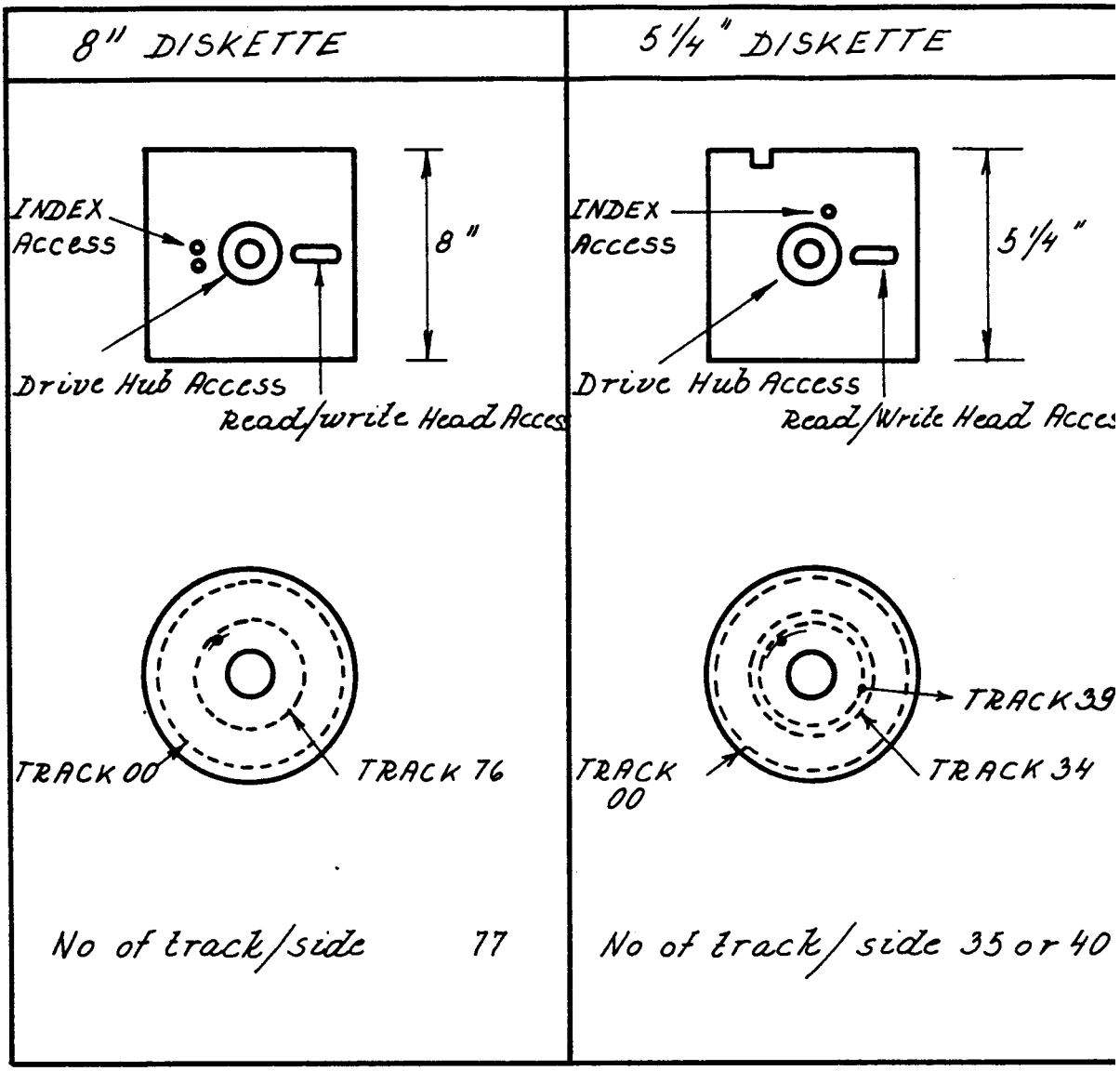
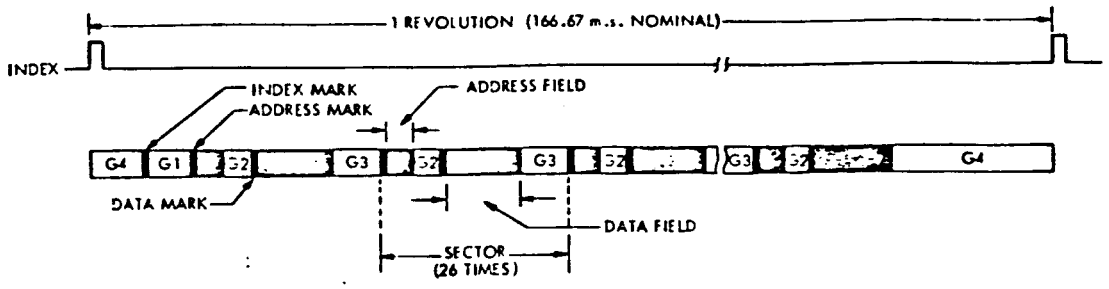
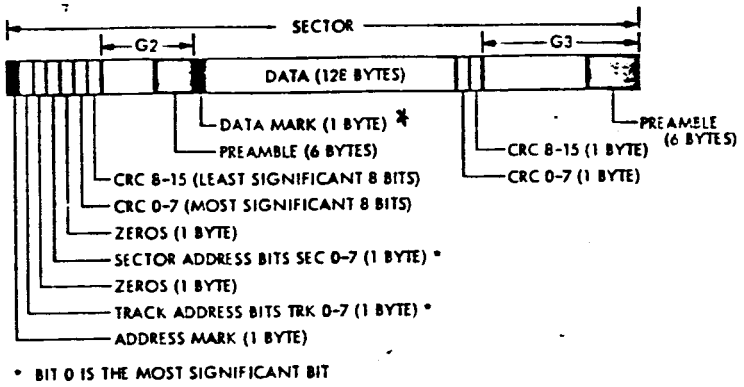


FIG. 2.3.26. FLOPPY DISK DATA MEDIA.



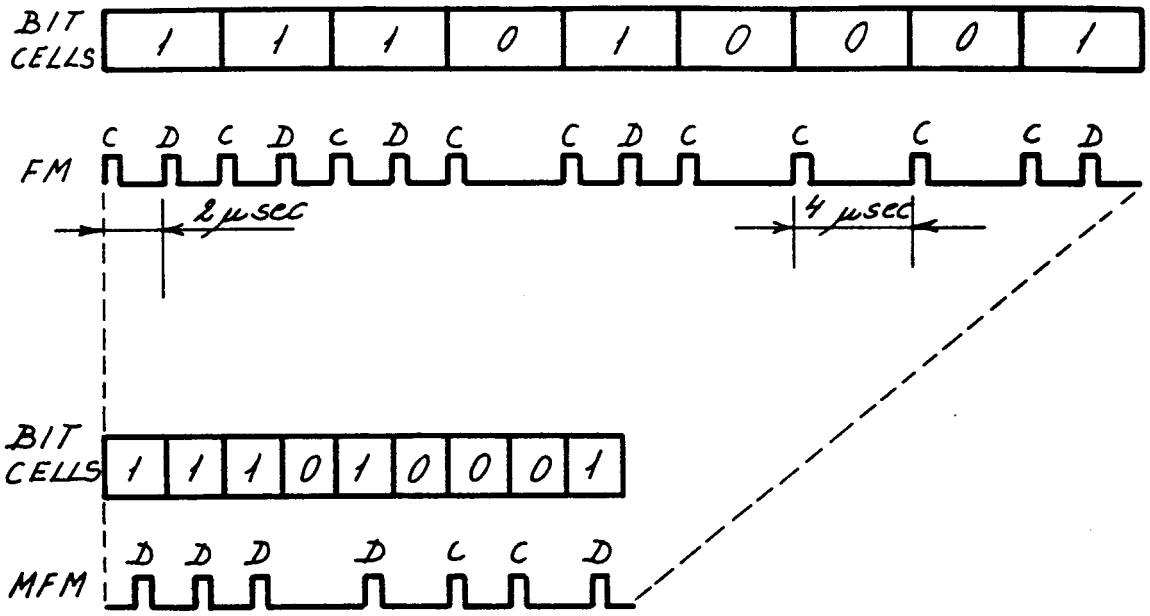


GAP FIELDS

G1 = 26 BYTES HEX FF
6 BYTES HEX 00
G2 = 11 BYTES HEX FF
6 BYTES HEX 00
G3 = 27 BYTES HEX FF
6 BYTES HEX 00
G4 =314 BYTES HEX FF
6 BYTES HEX 00

* DATA MARK is also called 'Data Address Mark'

Fig. 2.3.27 Information stored on one Track of a Diskette. The Example here shows a 8" Diskette.



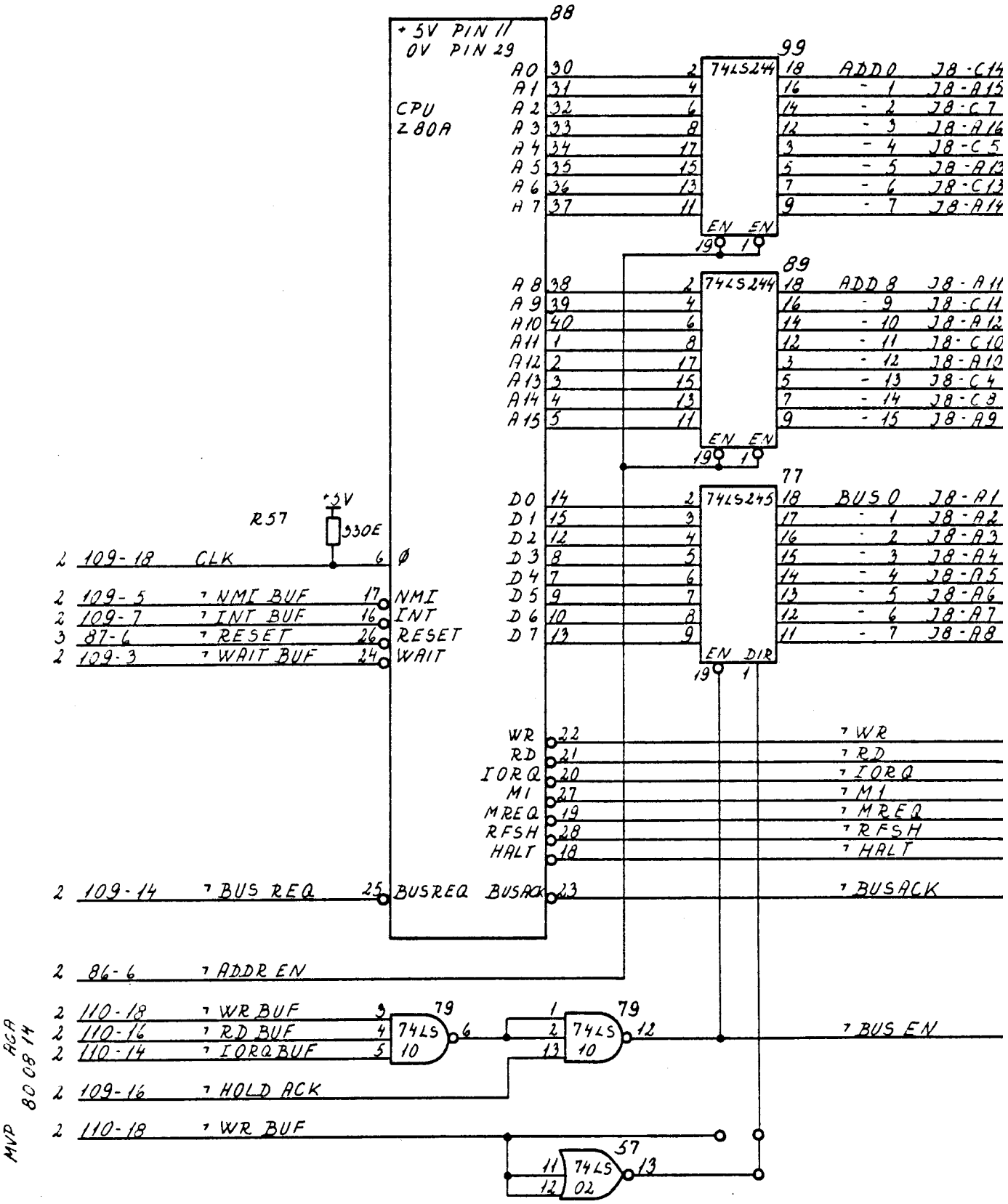
D ~ Data Pulse
C ~ Clock

FM is also called single Density.
MFM - - - double -

	8" DISK		5¼" DISK	
	FM	MFM	FM	MFM
Bit Cell	4 μs	2 μs	8 μs	4 μsec
Flux Changes/Cell	2	1	2	1
- - /Inch	6536	6536	2728	5456
Kilo Bits/sec	250	500	125	250
Frecuency Ratios	2/1	2/1	2/1	2/1
Bit to Bit spacing	2 μs 4 μs	2 μs 3 μs 4 μs	4 μs 8 μs	4 μs 6 μs 8 μs

Fig. 2.3.28. RECORDING METHODS OF FLOPPY DISKS.

Signal	Destination MIC No.	Description
ADD(0:15)	3, 4, 5, 6, 7, 9, 11, 15, 16	The address bus is the TRI-state bus supplying address information to all the controllers.
BUS(0:7)	3, 5, 6, 7, 9	The data bus is the TRI-state bus supplying data information between the CPU and the controllers.
WR	2	WRITE output from the CPU.
RD	2	READ - - - -
IORQ	2	INPUT OUTPUT REQUEST, when active the WR or RD pulse is addressing a controller and not the memory.
M1	2	MACHINE CYCLE ONE, indicates the op code fetch cycle of the CPU.
MREQ	2	MEMORY REQUEST, indicates a read or write memory cycle.
RFSH	2	REFRESH, indicates a refresh cycle by the CPU, the signal is not used in MIC702.
HALT		HALT indicates that the CPU is executing a halt instruction. An error situation.
BUS ACK	2	BUS ACKNOWLEDGE, the CPU has received a BUS REQ and lets the DMA use the BUS.
BUS EN	1	BUS ENABLE for the CPU.



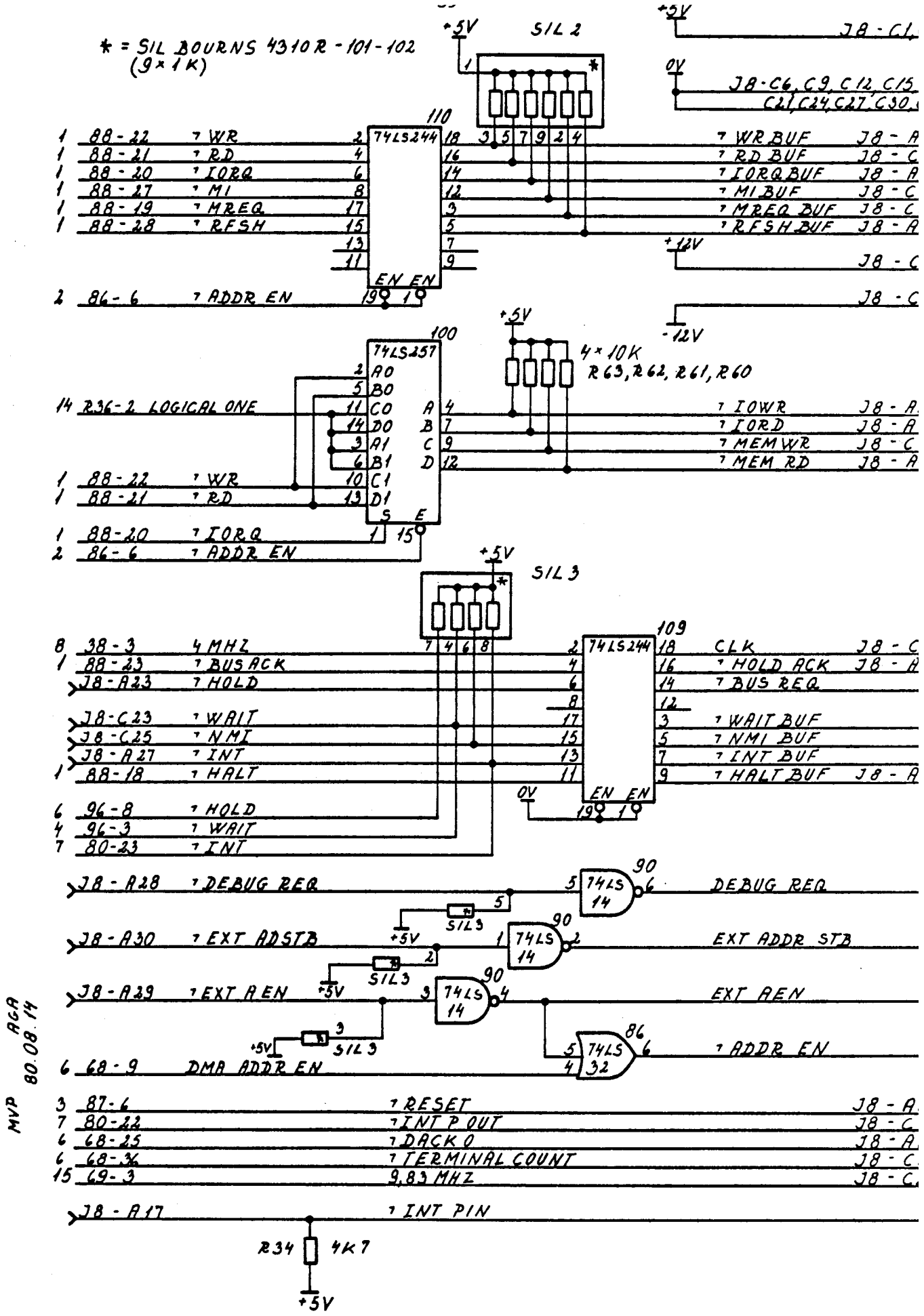
MIC 702 MICROPROCESSOR CPU AND ADDR/DATA REGISTERS MIC (

R 13077

Signal	Destination MIC No.	Description
WR BUF	1	* WRITE output pulse from the CPU
RD BUF	1, 7, 15, 16	* READ - - - - -
IORQ BUF	1, 7, 15, 16	* IORQ - - - - -
M1 BUF	7, 15, 16	* M1 - - - - -
M REQ BUF	4	* M REQ - - - - -
RFSH BUF		* RFSH - - - - -
IOWR	3, 6, 7, 9	** INPUT/OUTPUT WRITE, write pulse to controllers which are not of the Zilog type.
IORD	6, 9, 11, 15	** INPUT/OUTPUT READ, read pulse to controllers which are not of the Zilog type.
MEM WR	4, 5	** MEMORY WRITE pulse.
MEM RD	3, 4, 5	** MEMORY READ pulse.
CLK	1, 4, 6, 7, 15, 16	4 MHz symmetric clock to the system.
HOLD ACK	1, 6	BUS ACK signal through a buffer.
BUS REQ	1	The DMA controller or the tester demand control over the BUS.
WAIT BUF	1	This signal inserts at least one wait state in each CPU cycle.
NMI BUF	1	NON MASKABLE INTERRUPT, only used by a tester.
INT BUF	1	INTERRUPT REQUEST to CPU.
HALT BUF		HALT signal through a buffer.
DEBUG REQ	6	DMA REQUEST from a tester.
EXT ADDR STB	6	DMA REQUEST signal from a tester.
EXT AEN		- - - - - -
ADDR EN	1, 2, 3, 4, 6	ADDRESS ENABLE when active the CPU controls the BUS system.
INT PIN	15	INT PIN may be used by a unit connected to J8 and is interrupt priority in.

* signal is only active, when ADDR EN is active.

** Signal may also be active when ADDR EN is active. The DMA also uses these signals, which are of the TRI-state type.

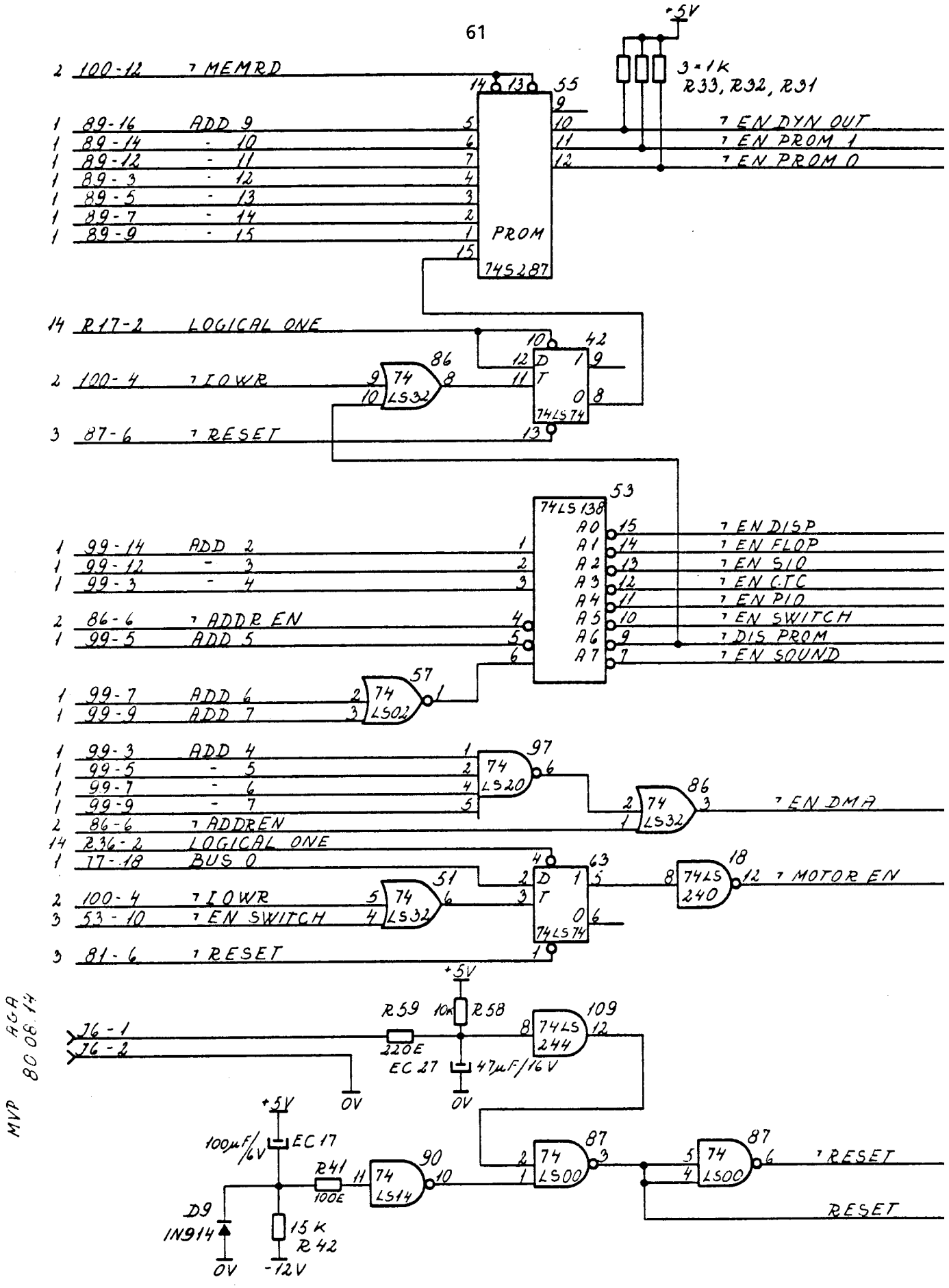


MIC 702

CONTROL SIGNALS RECEIVERS AND TRANSMITTERS

R 13078

Signal	Destination MIC No.	Description
EN DYN OUT	5	* This signal enables the output register from the RAM.
EN PROM 1	4	* This signal enables the output from PROM 1 which is only used when running a testprogram.
EN PROM 0	4	* This signal enables the output from PROM 0 which contains the program used under initiation.
EN DISP	11	* ENABLE DISPLAY controller
EN FLOP	9	* ENABLE FLOPPY controller
EN SIO	16	* ENABLE SERIAL IN/OUT controller
EN CTC	15	* ENABLE COUNTER/TIMER controller
EN PIO	7	* ENABLE PARALLEL IN/OUT controller
EN SWITCH	3, 15	* ENABLE SWITCHES
DIS PROM		* DISABLE PROM, the signal is used to disable the PROM and enable the whole RAM
EN SOUND	7	* ENABLE SOUND gives the acoustic signal
EN DMA	6	* ENABLE DMA controller
MOTOR EN	10	MOTOR ENABLE is used to switch on and off the motor used in the Mini floppy disk drive.
RESET	1, 3, 6, 9, 11 15, 16	RESET is the power up reset or a RESET initiated from the switch on the front of the computer.
		* Subsection 2.3.3. describes the actual addresses used in MIC702.



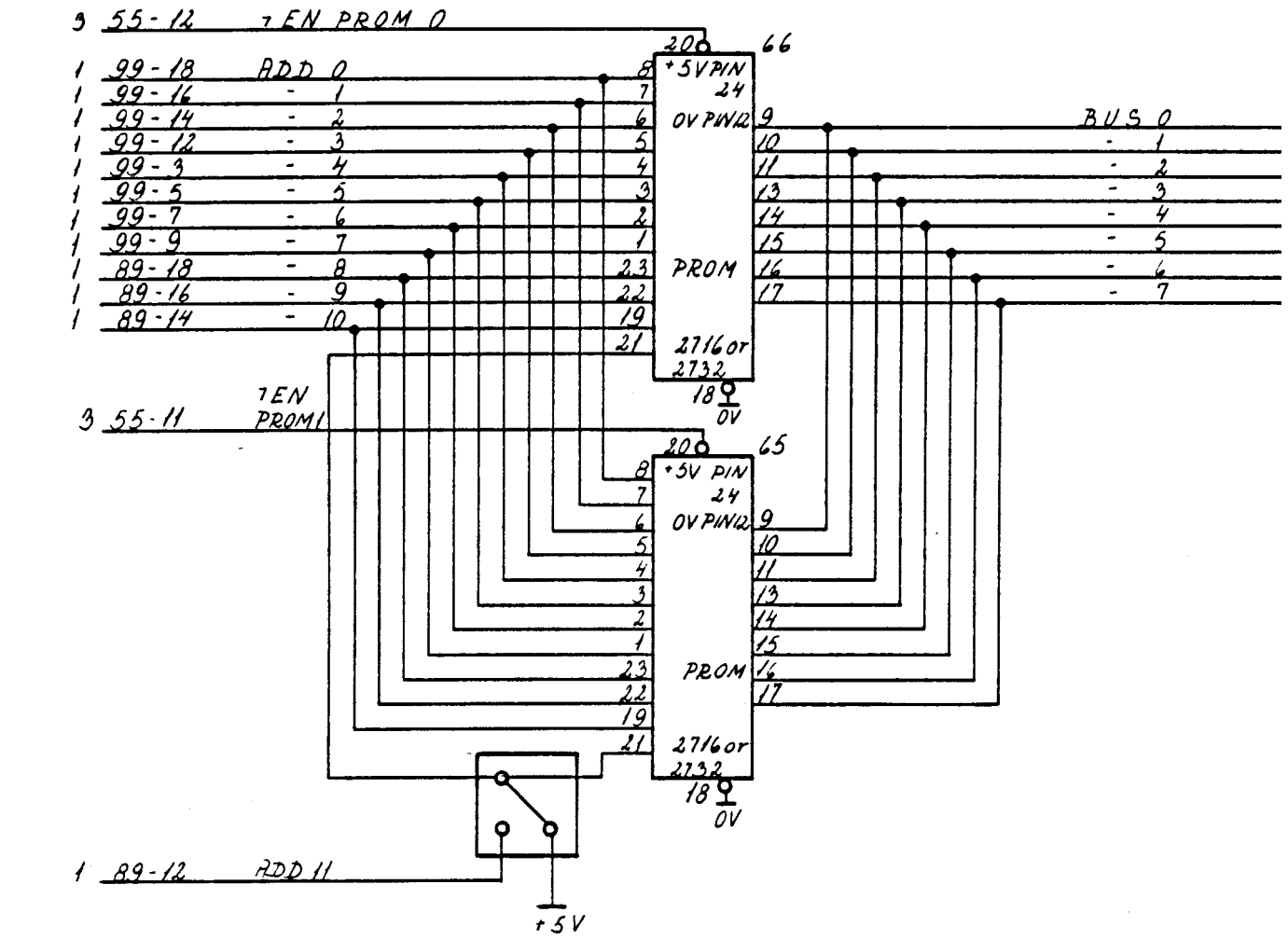
MIC 702 ADDRESS DECODERS & RESET CIRCUIT MIC

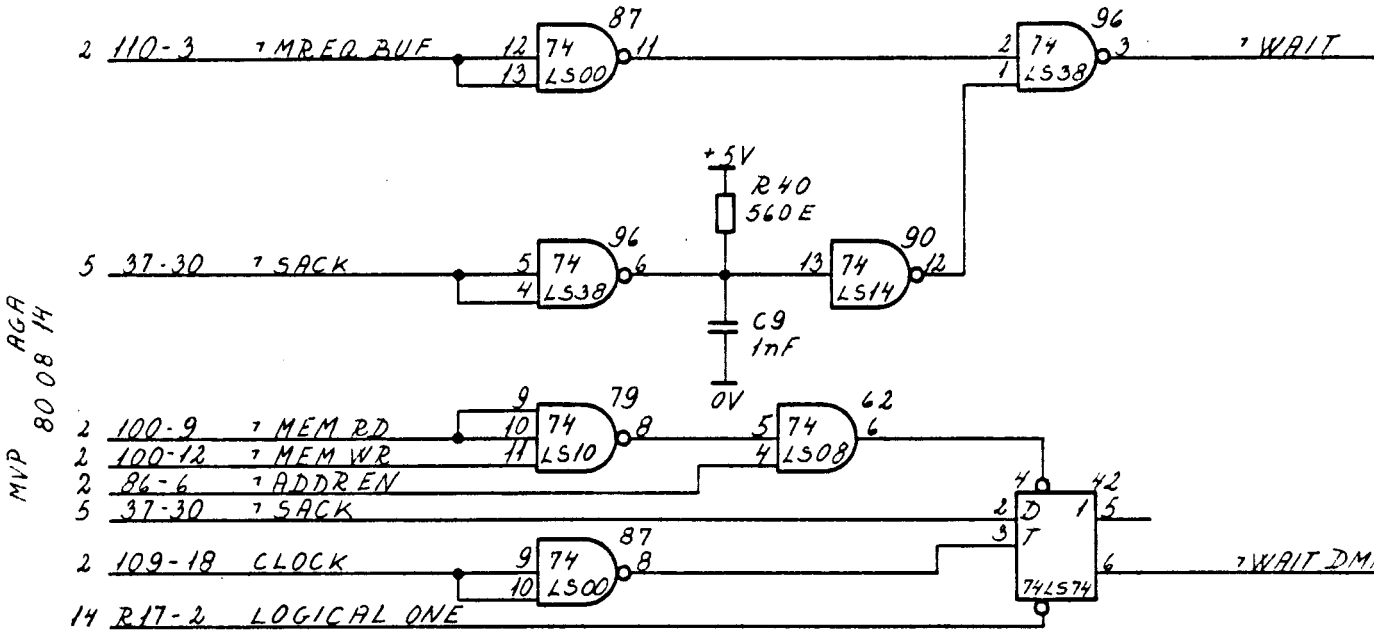
R 13079

Signal	Destination MIC No.	Description
BUS(0:7)		The data bus is the TRI-state bus supplying data information between the CPU and the controllers.
WAIT	2	WAIT supplies at least one wait state to the CPU-fetch cycle. More wait states are inseted when the RAM controller is making a refresh cycle.
WAIT DMA	6	WAIT DMA supplies at least one wait state in the DMA-cycle. More wait states are supplied when the memory controller is making a refresh cycle.

702 ROB 358

703 ROB 357.

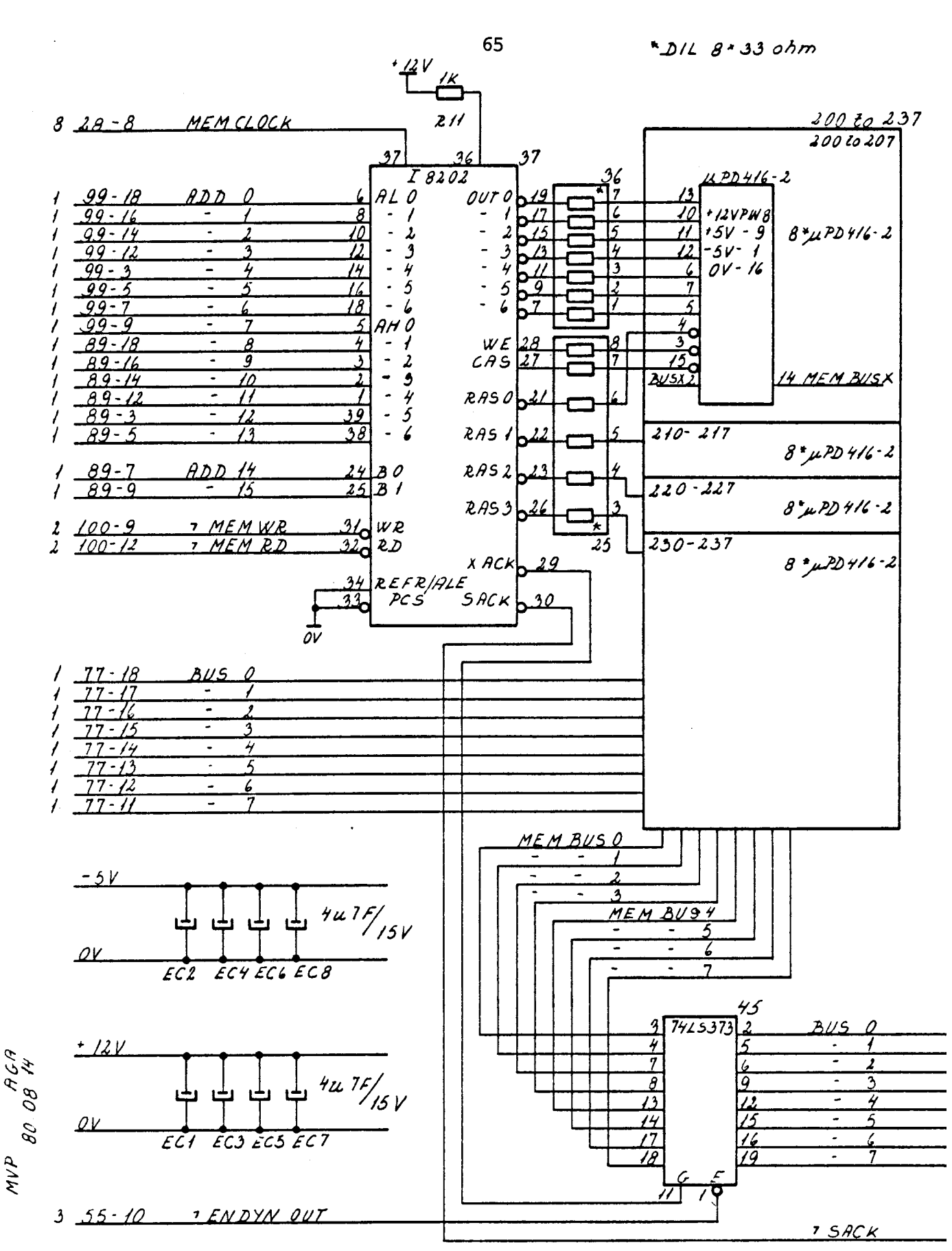




MIC 702 PROM MEMORY & WAIT STATE GENERATION MIC

R15080

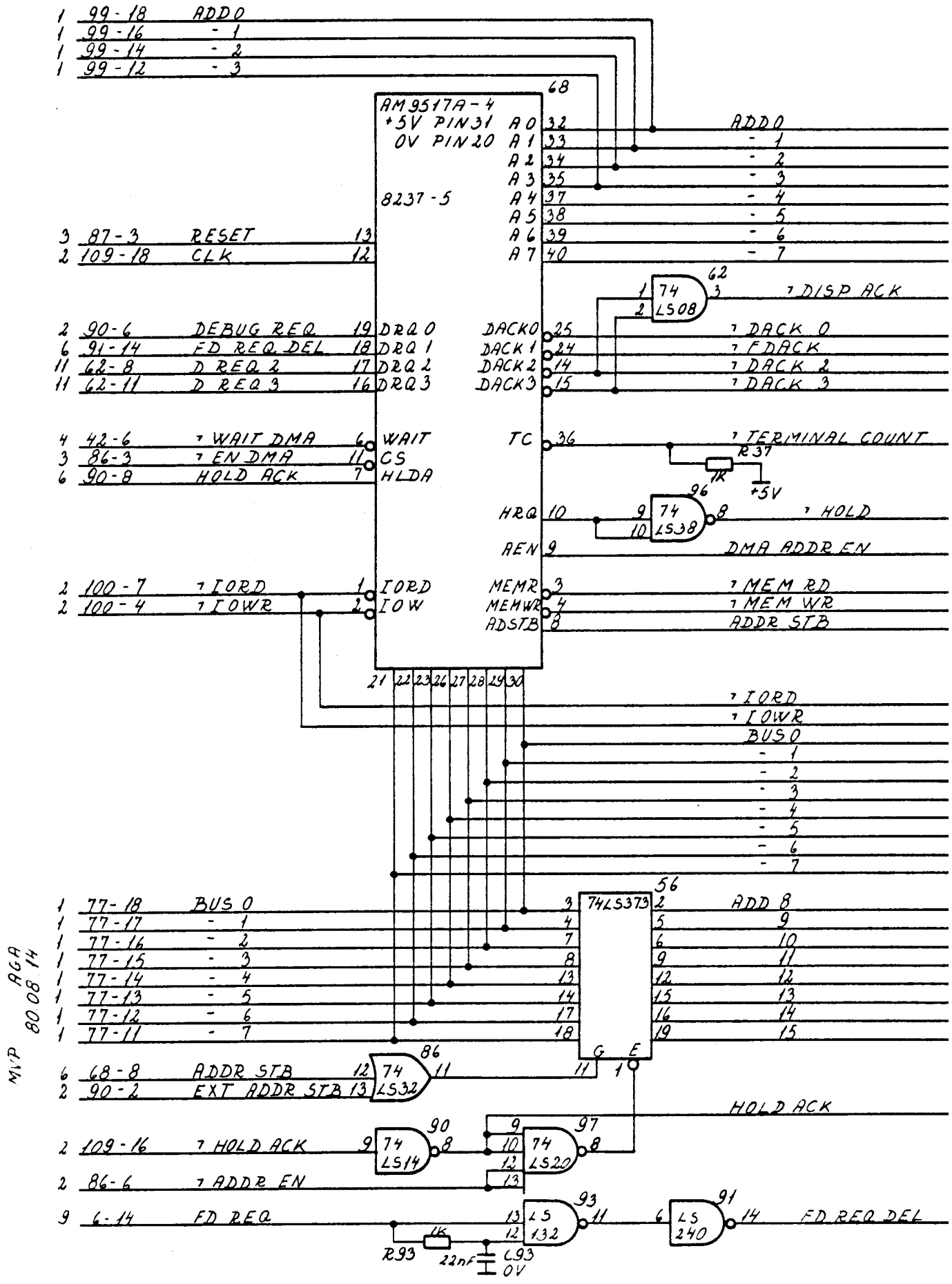
Signal	Destination MIC No.	Description
BUS(0:7)		The data bus is the TRI-state bus supplying data information between the CPU and the controllers.
SACK	4	Output signal from the RAM controller showing that the cycle is finished. (SACK means System Acknowledge).



MIC 702 64 K BYTES DYNAMIC RAM ARRAY & TIMING MIC 0.

R 13081

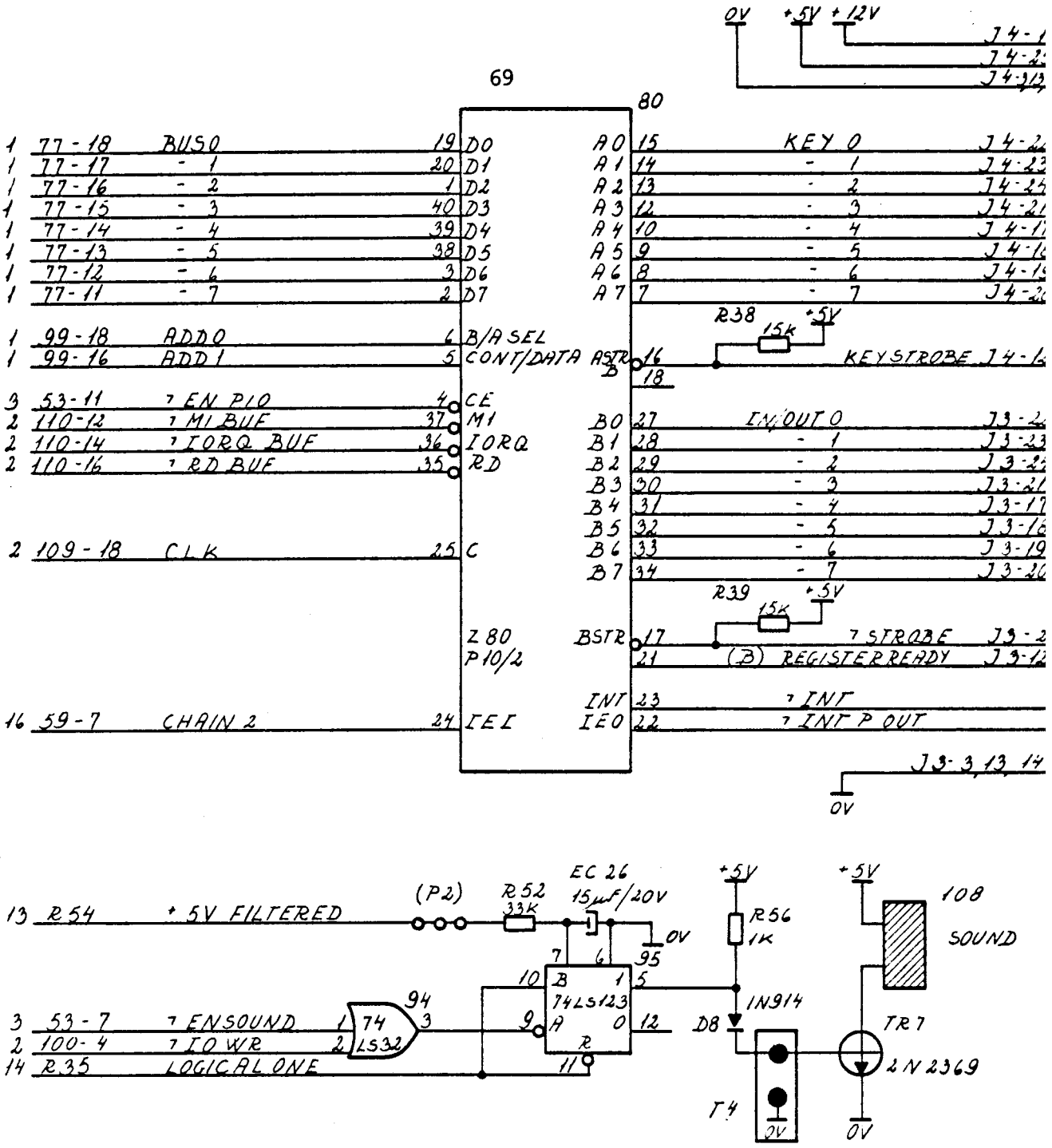
Signal	Destination MIC No	Description
ADD(0:7)		Address lines containing the 8 most significant bits. Bit (0:4) is both input to the DMA controller (under programming) and output from the DMA controller (under DMA-cycle).
DACK 0	2	Data acknowledge answer to debug request.
FDACK	9	Floppy data acknowledge, answer to FD req. delay.
DACK 2	11	Data acknowledge answer to DREQ2.
DACK 3		Data acknowledge answer to DREQ3.
DISP ACK	11	Display acknowledge. The display controller uses two channels in the DMA.
TERMINAL COUNT	2, 9, 11	The signal is used to terminate the operation.
HOLD	2	Request to stop the CPU.
DMA ADDR EN	2	Request to gain control over the data and address bus.
MEM RD		Memory read output from the DMA.
MEM WR		Memory write output from the DMA.
ADDR STROBE	6	Address strobe is a pulse to load the address register.
BUS(0:7)		Data bus used to supply information between the CPU and the controllers. Here also used to send address information from the DMA controller to the address register.
HOLD ACK		Hold acknowledge is the replay from the CPU that the bus is idle.
FD REQ DEL		DMA request signal from floppy disk controller.



MIC 702 DMA-CONTROLLER MIC

R 13082

Signal	Destination MIC No.	Description
KEY(0:7)		8-bit parallel input used to receive information from the keyboard.
KEY STROBE		Input strobe from the keyboard.
IN/OUT(0:7)		8-bit parallel input/output used to receive or transmit information to and from an external unit.
STROBE		Input strobe from external unit.
REGISTER READY		Output showing that output from the 8-bit input/output port is ready.
INT	2	Interrupt request.
INT P OUT	2	Interrupt priority out.

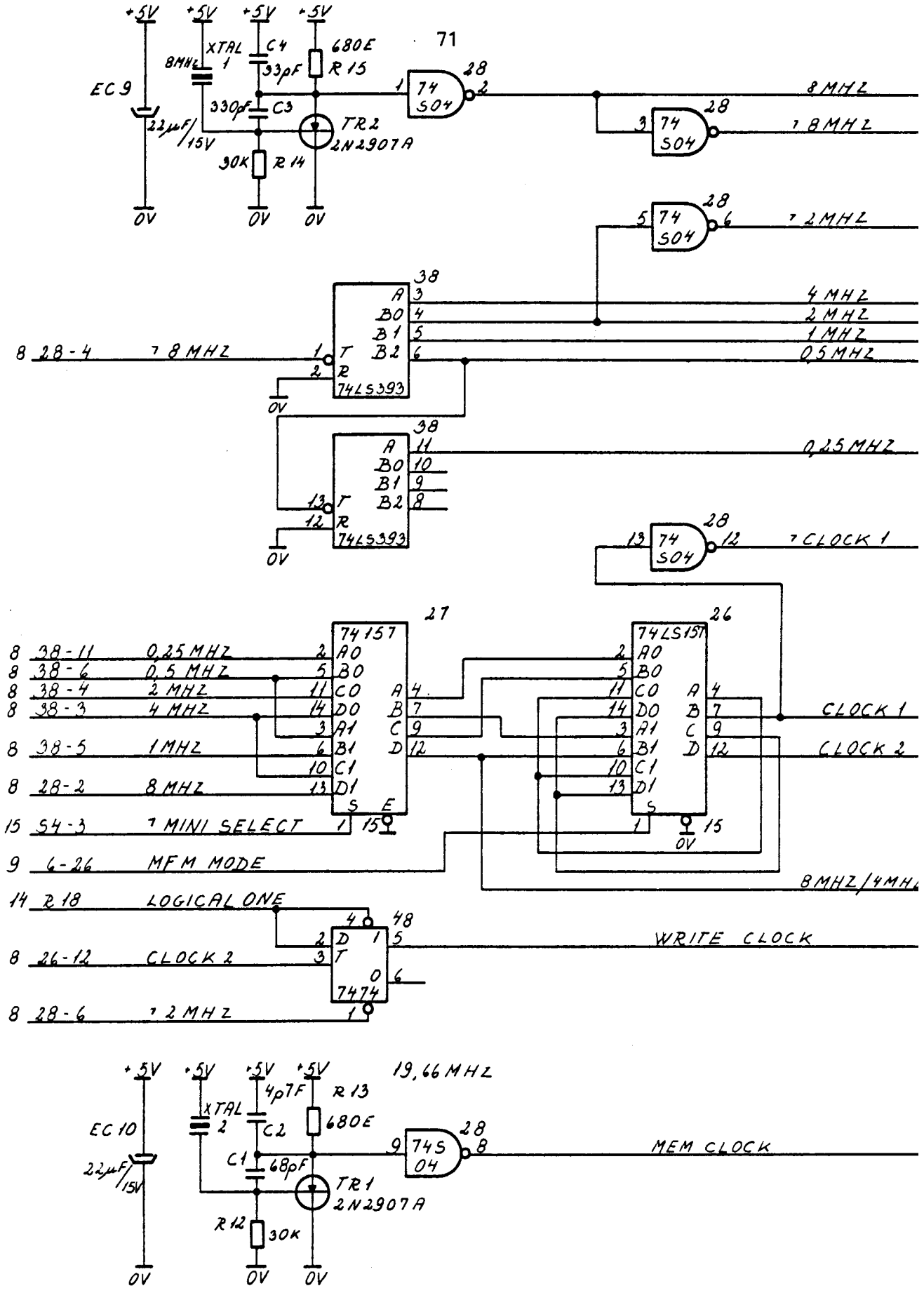


MVP 80 08 HGA 14

MIC 702 KEYBOARD & PARALLEL IN/OUT MIC

R 1.0.83

Signal	Destination MIC No.	Description
8 MHz	8, 9	Symmetric clock signal of 8 MHz
4 MHz	2, 8	- - - - 4 MHz
2 MHz	8	- - - - 2 MHz
1 MHz	8	- - - - 1 MHz
0.5 MHz	8	- - - - 0.5 MHz
0.25 MHz	8	- - - - 0.25 MHz
CLOCK 1	10	Clock to read logic for the
CLOCK 2	8	floppy controller. Frequency is selected by the controller and by the MINI SELECT switch.
8 MHz/4 MHz	9	Clock to the floppy controller 8 MHz for Maxi floppy and 4 MHz for Mini floppy drive.
WRITE CLOCK	9	Clock input to floppy controller. The frequency is selected by the controller and by the MINI SELECT switch.
MEM CLOCK	5, 15	Clock to the memory controller. The frequency is 19.66 MHz.

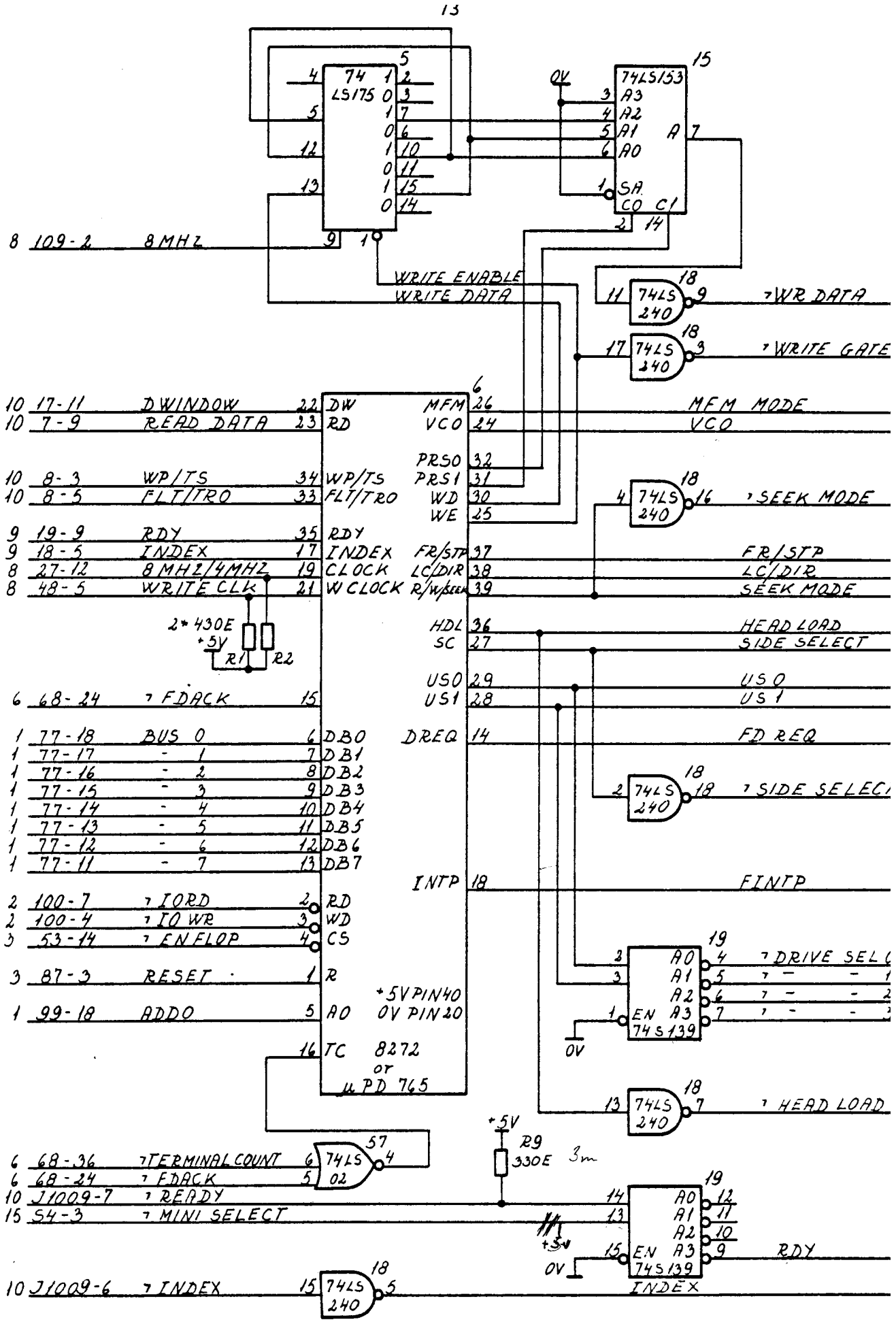


MVP 80 08 14 FGA

MIC 702 CLOCK SYSTEM MIC

R 13084

Signal	Destination MIC No.	Description
WR DATA	10	WRITE DATA to the floppy disk drive. Valid when WRITE GATE is on.
WRITE GATE	10	Control signal to floppy disk drive. Informs that now the WR DATA is valid.
MFM MODE	8	MFM mode is dual density, FM mode is single density.
VCO	10	Signal to control the voltage controlled oscillator.
SEEK MODE	10	Sets the selectors in seek mode.
FR/STP	10	Control signal; Fault Reset/ Step
LC/DIR	10	Control signal; Low Current/ Direction
HEAD LOAD	10	Control signal; Head Load
SIDE SELECT	10	Control signal; Side Select
US0, US1		Unit select decoded to:
DRIVE SEL 0	10	Drive Select 0
DRIVE SEL 1	10	Drive Select 1
DRIVE SEL 2	10	Drive Select 2
DRIVE SEL 3	10	Drive Select 3.
FD REQ	6	DMA reguest from floppy controller.
F INTP	15	Floppy controller interrupt request.
RDY	9	Ready from floppy controller. Note that Mini floppy is always ready.
INDEX	9	Index mark from floppy disk drive.

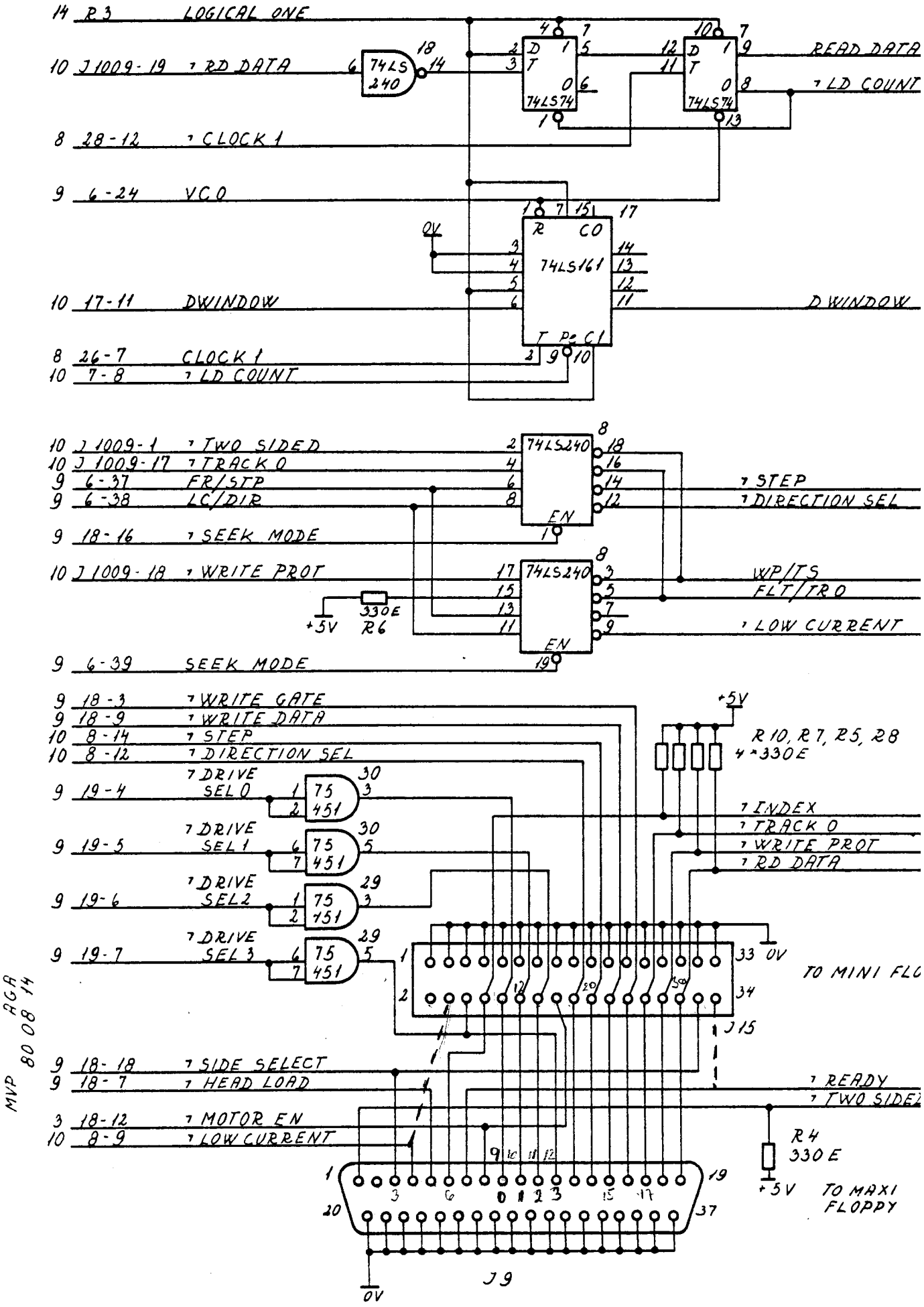


MVP AGA 80.08.14

MIC 702 FLOPPY DISK CONTROLLER MIC

R 13085

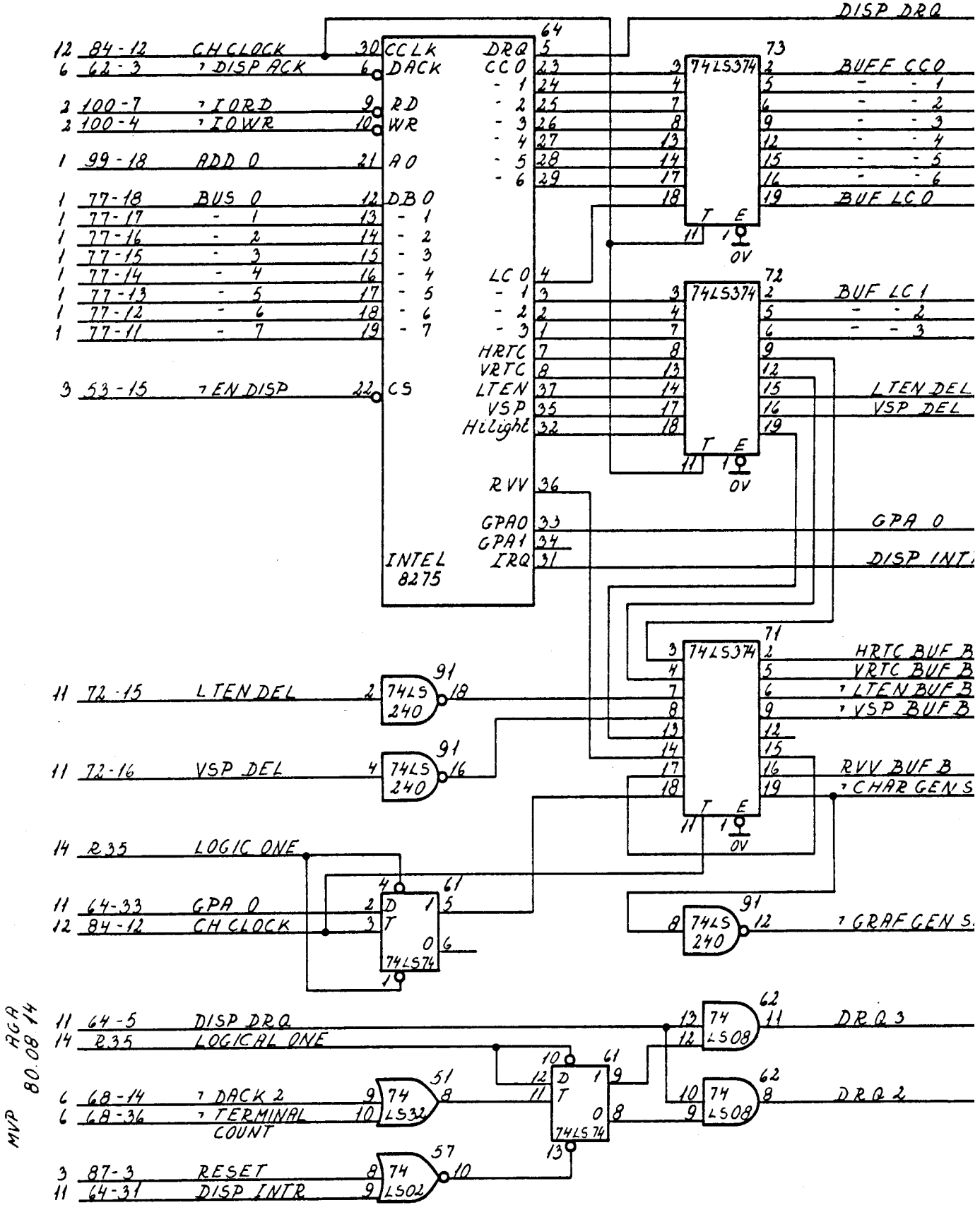
Signal	Destination MIC No.	Description
READ DATA	9	Read data from the floppy, synchronized with the VCO to separate phase bits and data bits.
LD COUNT	10	Load counter is used to synchronize the window counter.
D WINDOW	9, 10	Data Window is used by the controller to separate data bits from phase bits.
STEP	10	Output pulse to make the floppy head move from one cylinder to the next.
DIRECTION SEL	10	Direction select is used together with the STEP pulse. A low signal and the head moves towards the counter of the disc.
WP/TS	9	Write Protect/Two Sided signal from the floppy disk drive.
FLT/TRO	9	Fault/Track 0 signal from floppy disk drive.
LOW CURRENT	10	Output signal to Maxi floppy disc drive. Used to decrease the write current when close to the center of the disk.
INDEX	9	Index mark signal from the floppy.
TRACK 0	10	Track 0 signal from the floppy.
WRITE PROT	10	The diskette used is writeprotected.
RD DATA	10	Read data supplied from the floppy disk drive including data and phase bits.
READY	9	Ready signal from the Maxi floppy drive.
TWO SIDED	10	The Maxi floppy is a two sided version.



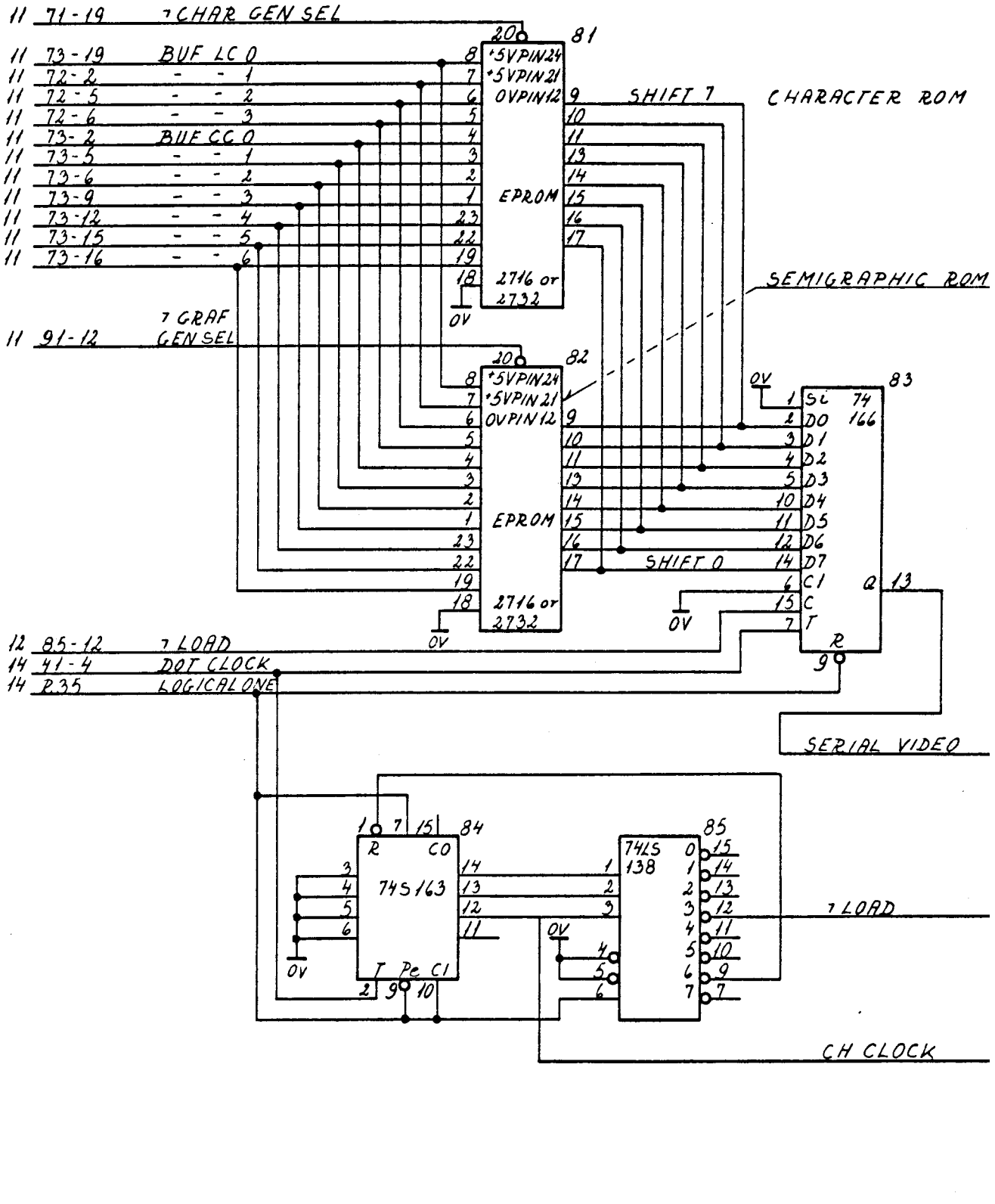
MIC 702 FLOPPY DISK READ & SELECT CIRCUIT MIC

R 13086

Signal	Destination MIC No.	Description
DSP DRQ	11	DMA request from the display controller.
BUFF CC(0:6)	12	Output from the display controller containing the address of the character to be written on the display.
BUFF LC(0:3)	12	Output from the display controller containing the line number written on the display.
LTEN DEL	11	Light enable from the display.
VSP DEL	11	Video suppression. This output signal is used to blank the video to the display.
GPA 0	11	Control signal used to select semigraphic PROM.
DISP INTR	11, 15	Display interrupt request.
HRTC BUF B	13	Horizontal retrace signal.
VRTC BUF B	13	Vertical retrace signal.
LTEN BUF B	13, 14	LTEN DEL delayed one CHAR CLOCK
VSP BUF B	13	VSP DEL delayed one CHAR CLOCK
RVV BUF B	13	REVERSE VIDEO. This output is used to reverse the video signal to the display.
CHAR GEN SEL	12	This signal selects the standard character generator.
GRAF GEN SEL	12	This signal selects the semigraphic character generator.
DRQ3 and DRQ2	6	The display controller uses two channels out of the DMA's four channels. This is done to make the roll function of the display. DRQ2 and DRQ3 are the two data request signals.


DISP DRQ
12 84-12 CH CLOCK
6 62-3 ↑ DISP ACK
2 100-7 ↑ IORD
2 100-4 ↑ IOWR
1 99-18 ADD 0
1 77-18 BUS 0
1 77-17 - 1
1 77-16 - 2
1 77-15 - 3
1 77-14 - 4
1 77-13 - 5
1 77-12 - 6
1 77-11 - 7
3 53-15 ↑ EN DISP
CCLK
DACK
RD
WR
A0
DB0
CS
INTEL 8275
DRQ
CC0
LC0
HRTC
VRTC
LTEN
VSP
Hilight
RVV
GPA0
GPA1
IRQ
64
74LS374
73
72
71
BUFF CC0
BUF LC0
BUF LC1
LTEN DEL
VSP DEL
GPA 0
DISP INT
HRTC BUF B
VRTC BUF B
↑ LTEN BUF B
↑ VSP BUF B
RVV BUF B
↑ CHAR GEN S
11 72-15 LTEN DEL
11 72-16 VSP DEL
74LS 240
91
14 R35 LOGIC ONE
11 64-33 GPA 0
12 84-12 CH CLOCK
74LS74
61
↑ GRAF GEN S
11 64-5 DISP DRQ
14 R35 LOGICAL ONE
74 LS08
62
DRQ 3
DRQ 2
6 68-14 ↑ DACK 2
6 68-36 ↑ TERMINAL COUNT
74 LS32
51
3 87-3 RESET
11 64-31 DISP INTR
74 LS02
57
MVP AGA 80.08.14

Signal	Destination MIC No.	Description
SERIAL VIDEO	13	The video output from the shift register.
LOAD	12	Signal to load the output from the character ROM or the semigraphic ROM into the shift register.
CH CLOCK	11	Character clock. The period time of this clock is 7 times the DOT CLOCK time. 7 x 86 nsec. = 0.601 usec.

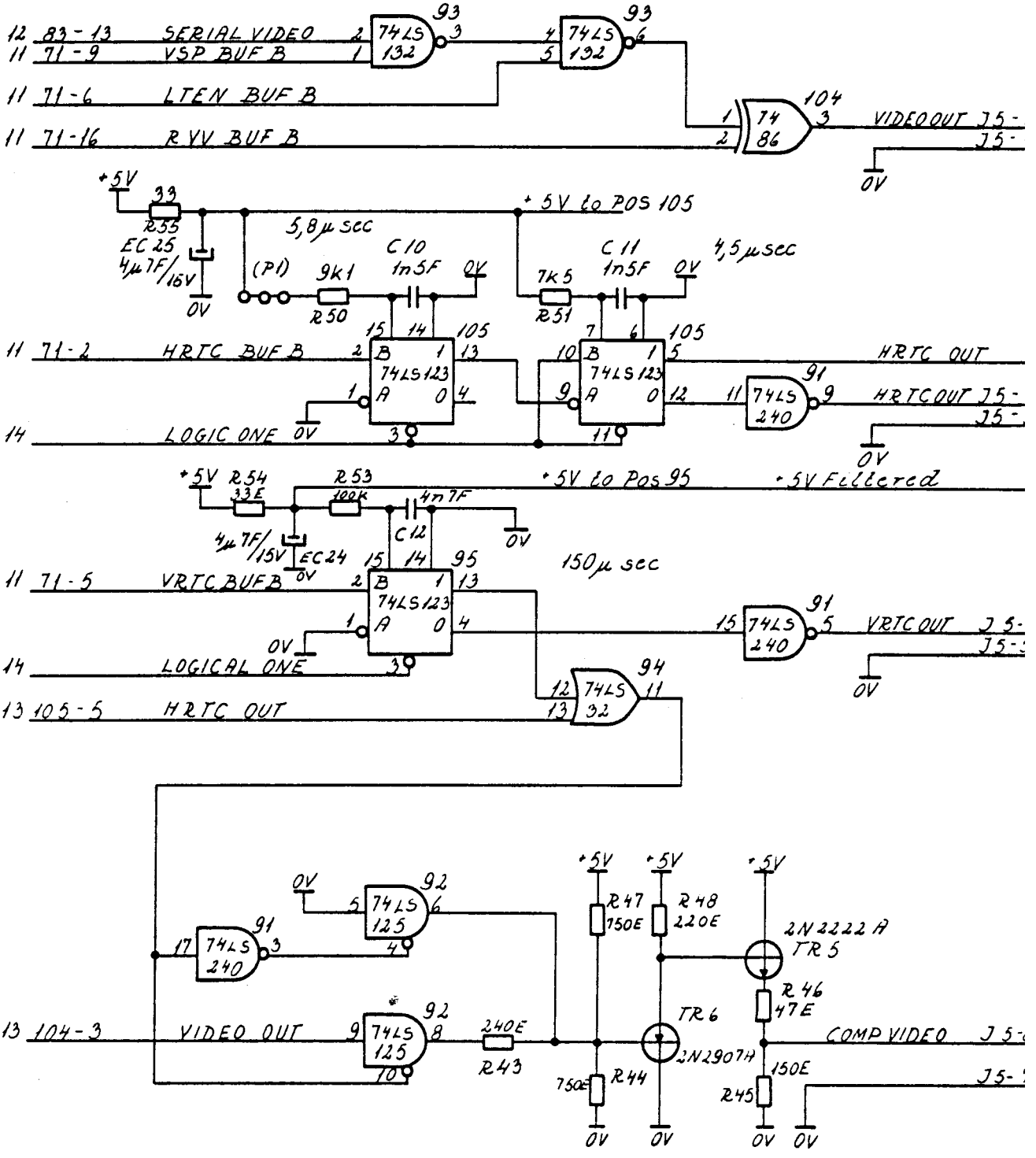


MVP 80 08 AGA 44

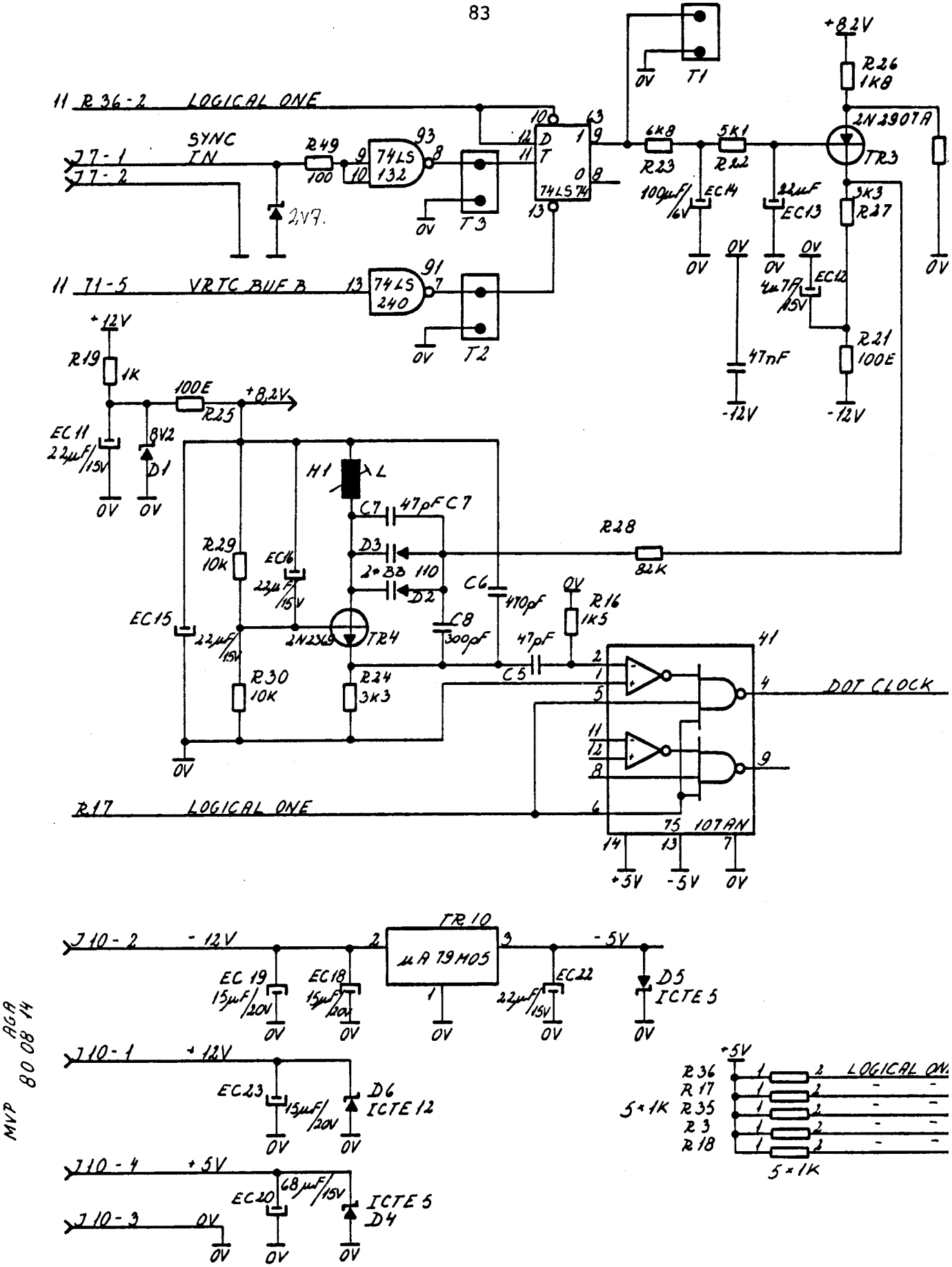
MIC 702 CHARACTER GENERATOR, VIDIO SHIFT REGISTER & DOT COUNTER MIC

R 13088

Signal	Destination MIC No.	Description
VIDEO OUT	13	Video out signal. *)
HRTC OUT	13	Horizontal output pulse. *)
VRTC OUT		Vertical output pulse. *)
		*) These three signals are ready to be used if a video monitor without decoding for comp. video is used. RC702 uses comp. video signals.
COMP VIDEO		Compressed video is the signal containing both video horizontal sync. and vertical sync.
+5 V filtered	7	+5 V supply after an RC filter.


12 83-13 SERIAL VIDEO
11 71-9 VSP BUF B
11 71-6 LTEN BUF B
11 71-16 RVV BUF B
74LS 132
74LS 132
74 86
VIDEOOUT J5-
+5V
R55 33
EC25 4µ7F/16V
5,8µ sec
(P1)
9k1 R50
C10 1n5F
+5V to POS 105
C11 1n5F
4,5µ sec
7k5 R51
11 71-2 HRTC BUF B
74LS123
HRTC OUT
74LS 240
HRTCOUT J5-
14 LOGIC ONE
+5V R54 33E
R53 100K
4n7F C12
4µ7F/15V EC24
+5V to Pos 95
+5V Filtered
150µ sec
11 71-5 VRTC BUF B
VRTC OUT J5-
14 LOGICAL ONE
13 105-5 HRTC OUT
74LS 32
74LS 125
74LS 240
13 104-3 VIDEO OUT
240E R43
R47 750E
R48 220E
2N2222A TR5
R46 47E
TR6 2N2907A
R44 750E
R45 150E
COMP VIDEO J5-
MVP AGA 80 08.14

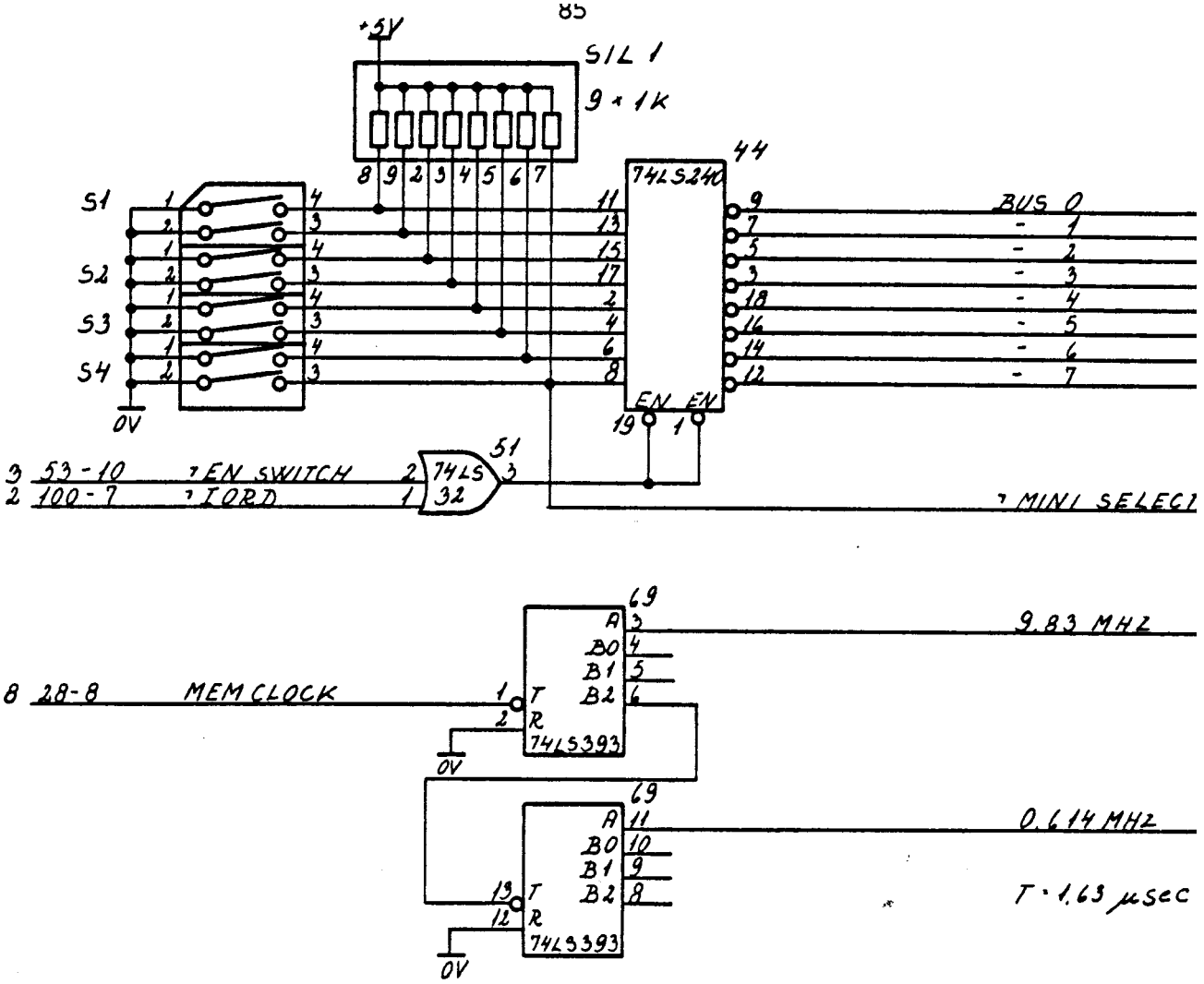
Signal	Destination MIC No.	Description
DOT CLOCK	12	The dot clock is an 11.64 MHz clock which is synchronized with the main frequency.
SYNC IN		The input is a 50 Hz signal from the REC701 rectifier unit.
T1		Testpoint 1. The signal here is a 50 Hz signal and the coil H1 is adjusted until the dutycycle of this signal is 50%.
-5 V		The -5 V is used to the dynamic RAM.

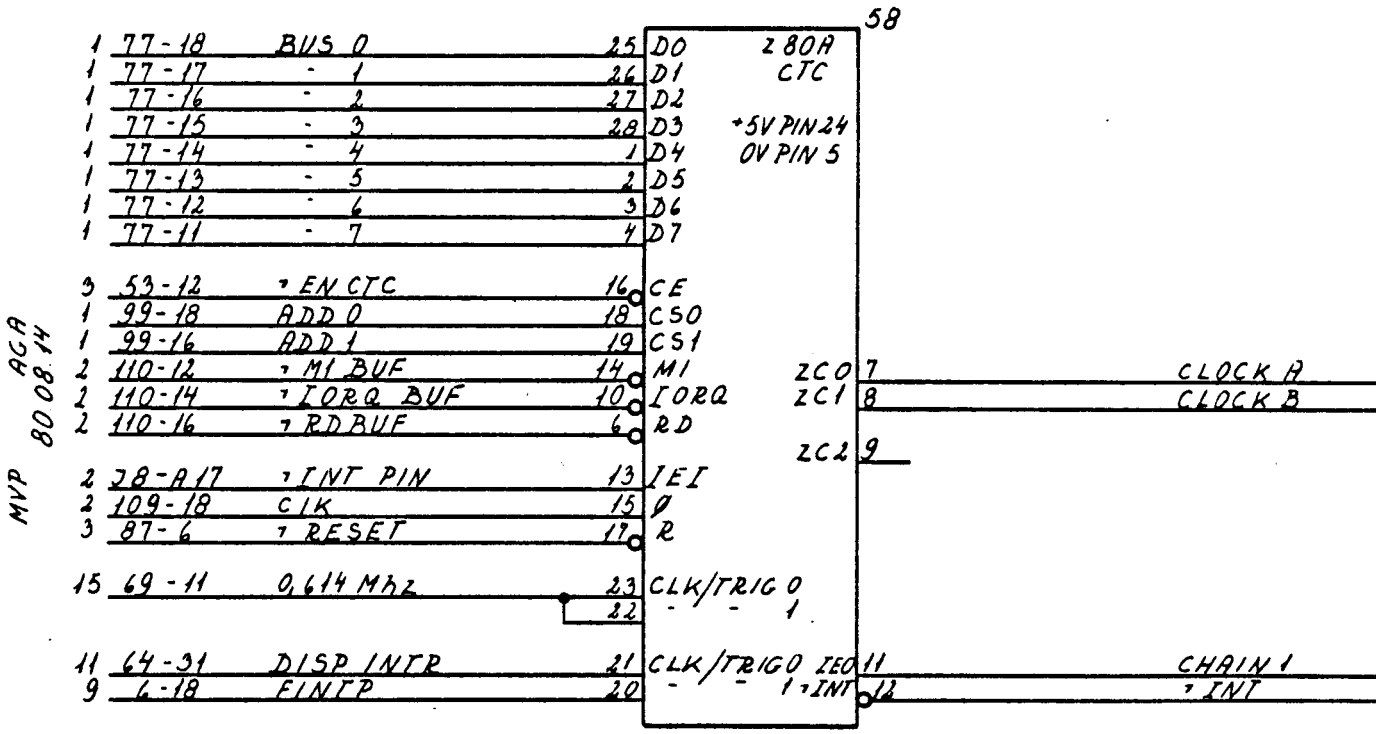


MIC 702 PHASE LOCK LOOP MIC 1

R 13090

Signal	Destination MIC No.	Description
BUS(0:7)	1	The data bus is the TRI-state bus supplying data information between the CPU and all of the controllers.
MINI SELECT	8, 9	Control signal selects Mini floppy disk drives. The signal is supplied to the clock generator and divides the clock signals to the floppy controller by two.
9.63 MHz	2	Clock of 9.63 MHz is not used on the board but supplied to the output plug J8.
0.614 MHZ	15	Clock of 0.614 MHz is used as input to the counter timer controller to be counted down to make the clock signal to the two Serial In/Out Channels.
CLOCK A CLOCK B	16 16	Clock signal to the two Serial In/Out Channels just mentioned.
CHAIN 1	16	Interrupt priority chain
INT		Interrupt from the counter timer controller.

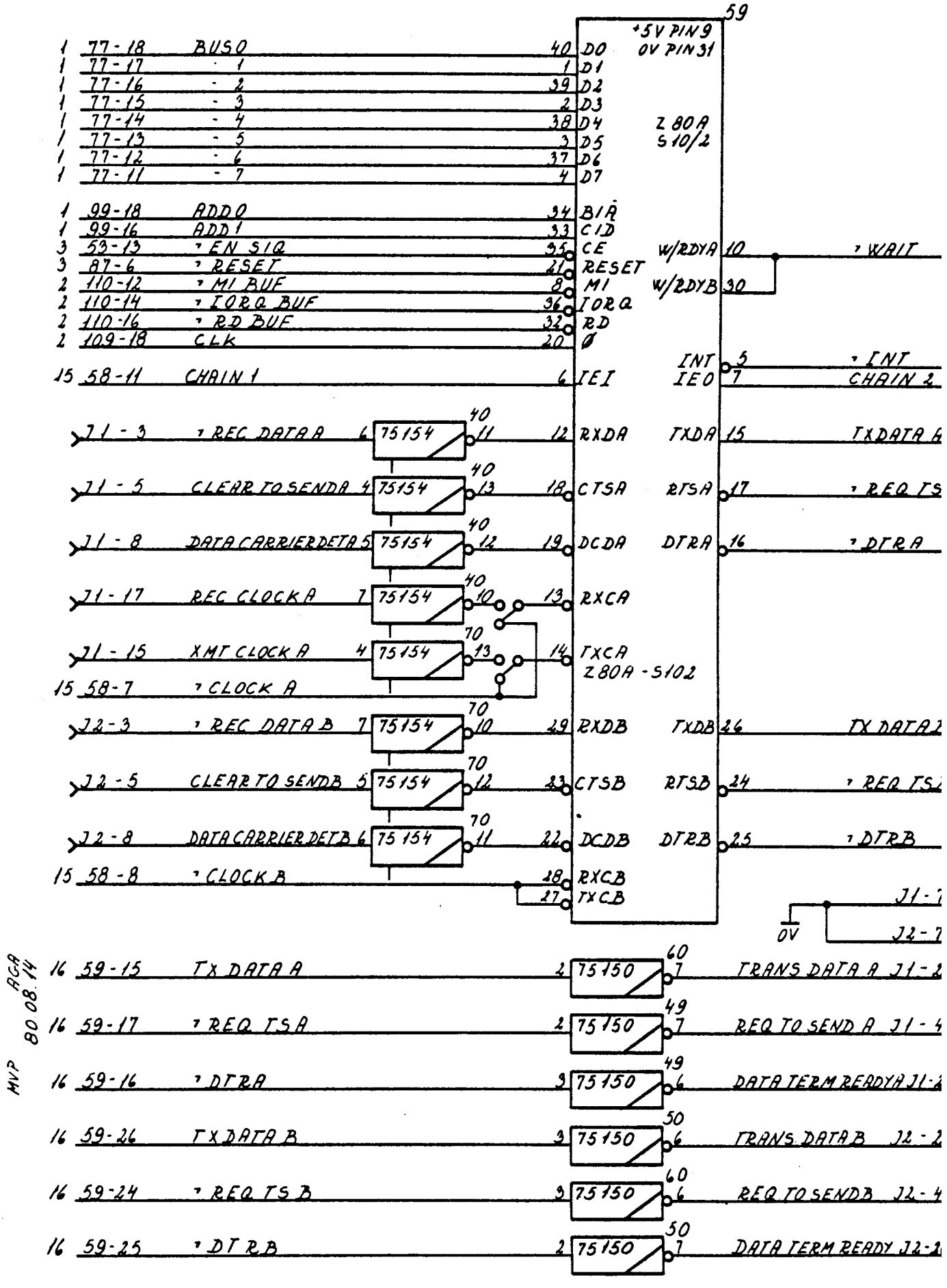




MIC 702 SWITCH INPUT TO PROGRAM & BAUD RATE GENERATOR MIC

R 13091

Signal	Destination MIC No.	Description
WAIT	4	This open collector output from the SIO is connected to the WAIT signal generated on page 04 and slows the CPU down to wait for the SIO.
INT	2	Interrupt request from the SIO/2.
CHAIN	2	Interrupt priority chain out from the SIO/2.
V.24 input outputs		Pin 2 TRANS DATA - 3 REC DATA - 4 REQ TO SEND - 5 CLEAR TO SEND - 7 Ground - 8 DATA CARRIER DETECT - 20 DATA TERM READY J1 to channel A (Terminal) J2 to channel B (Printer)



MIC 702 SERIAL INPUT OUTPUT MIC

R 13092

2.4 Character Generator 2.4

The character generator is made of the ROM with the technical name ROA296 and the layout is shown in fig. 2.5. The different national alphabets are chosen via the software.

Fig. 2.6 shows the ROM with the name ROA327 which makes the semigraphic alphabeth.

Fig. 2.5. CHARACTER GENERATOR ROA 296

MIC 702
R 13093

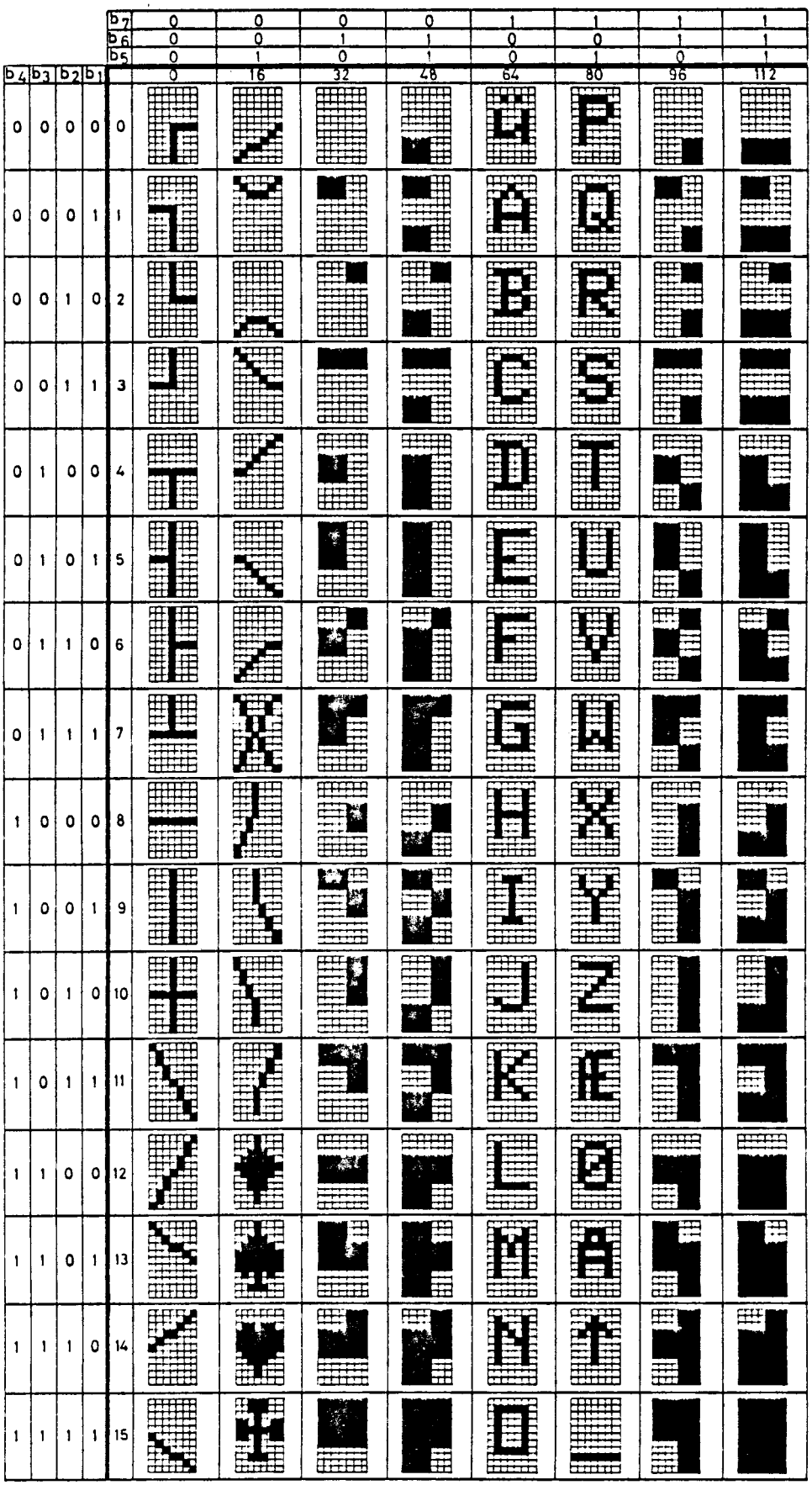


Fig. 2.6 SEMIGRAPHIC CHARACTER GENERATOR ROA 327

3. KBN702 CABINET WITH CABLES ECT. 3.

Fig. 3.1 shows the cabinet KBN702 with the power supply POW739 mounted. The cabinet itself contains transformer, blower, mains connection, rectifier unit RC702, and the internal cable.

Fig. 3.2 shows the cabinet with MIC702 mounted.

Fig. 3.3 shows diagram for rectifier unit and transformer, blower, and main connection.

Fig. 3.4 shows the internal cable in the KBN702.

Fig. 3.5 shows the cables connection KBN702 to MIC702 and POW739.

Fig. 3.6 shows the power cable CBL440.

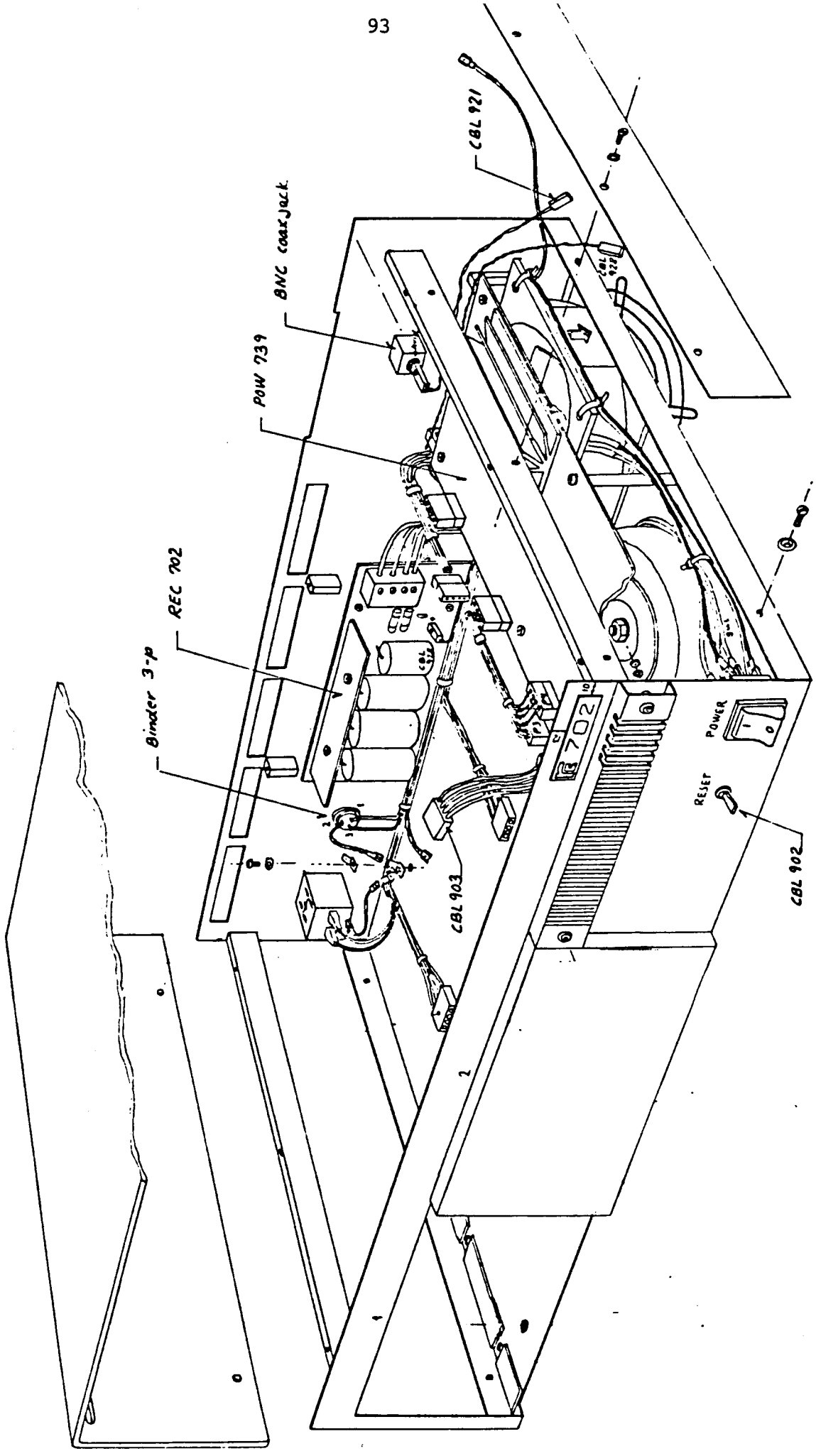


Fig. 3.1. KBN 702 with POW 739 mounted.

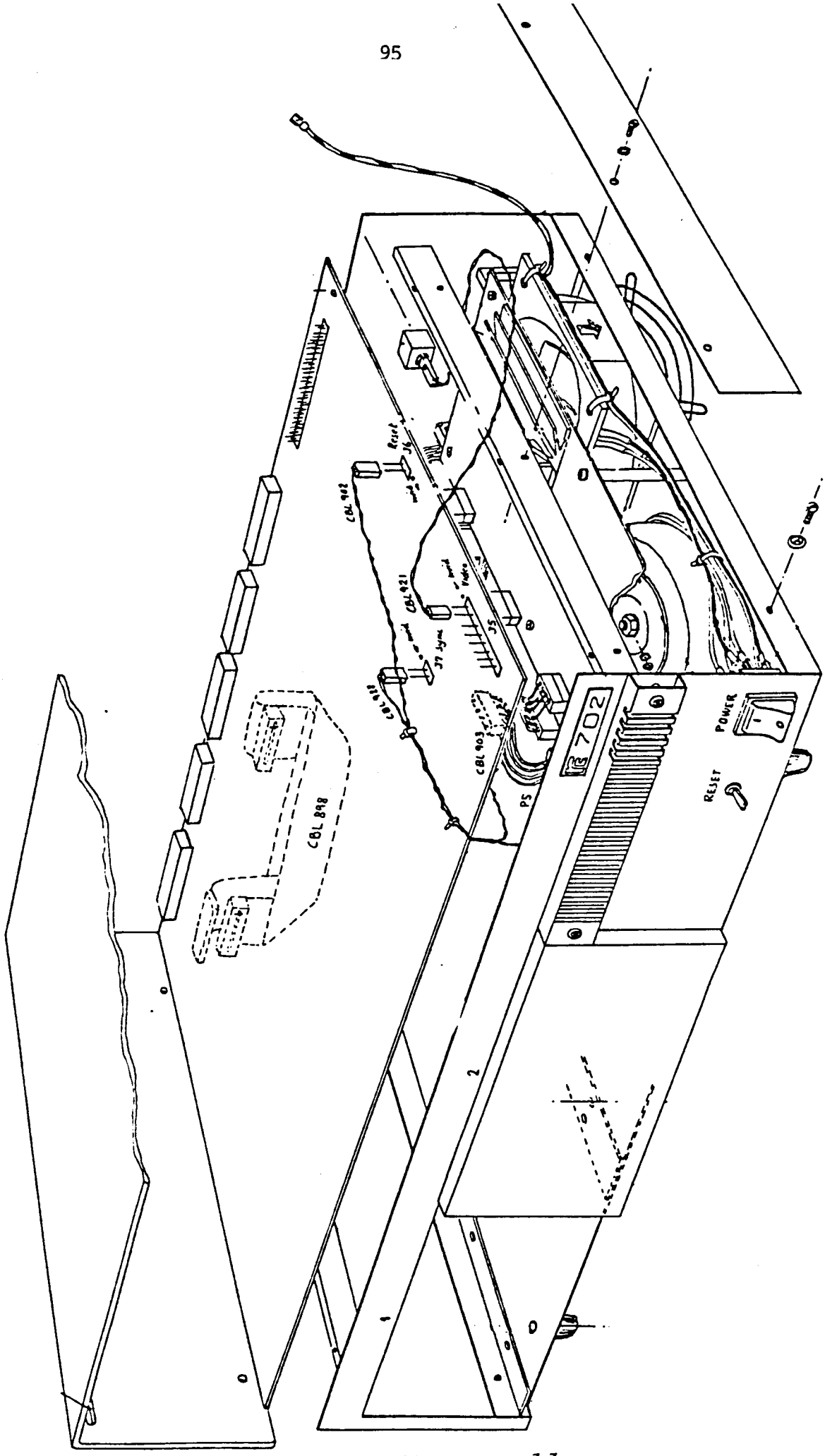
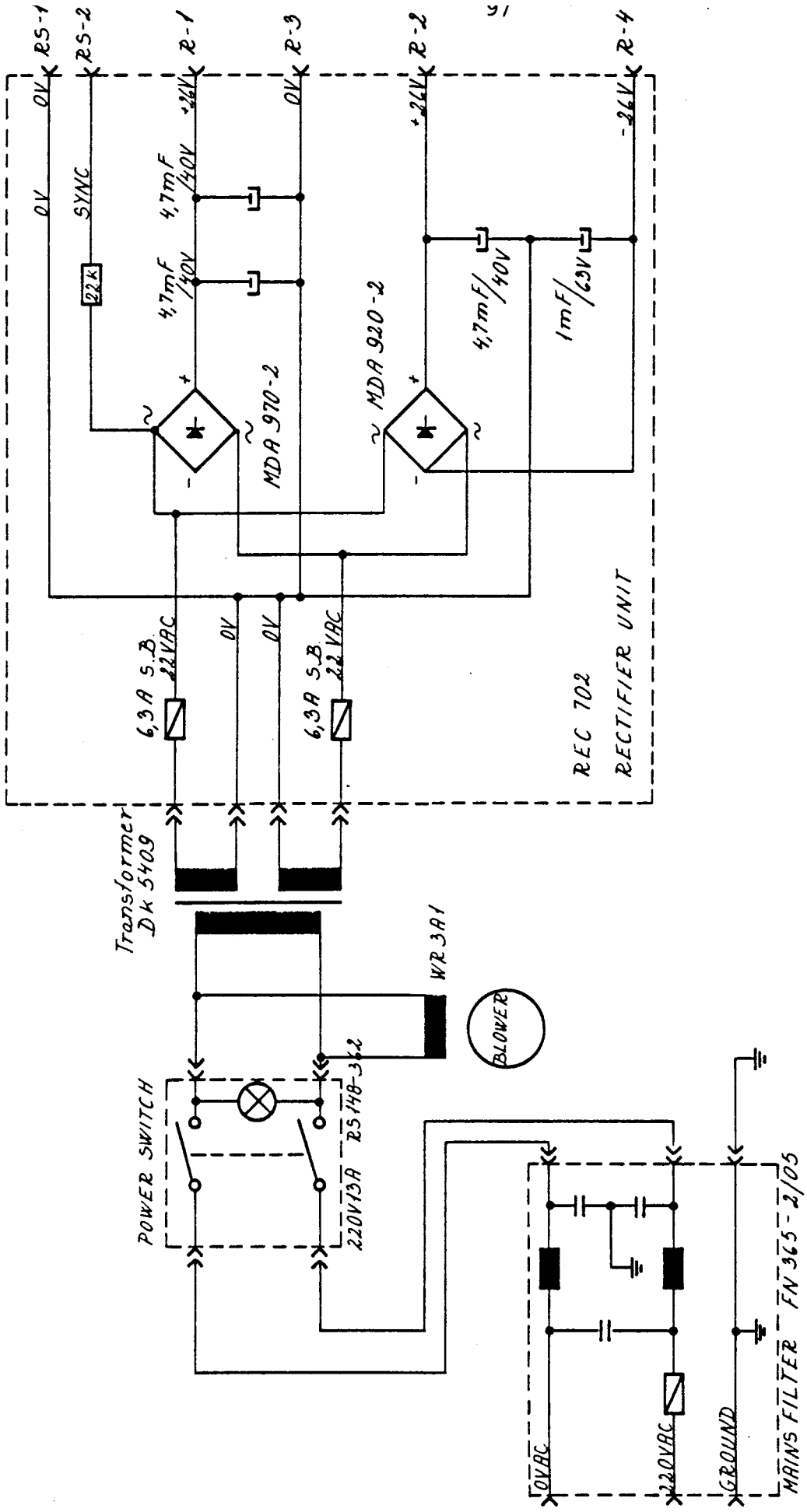
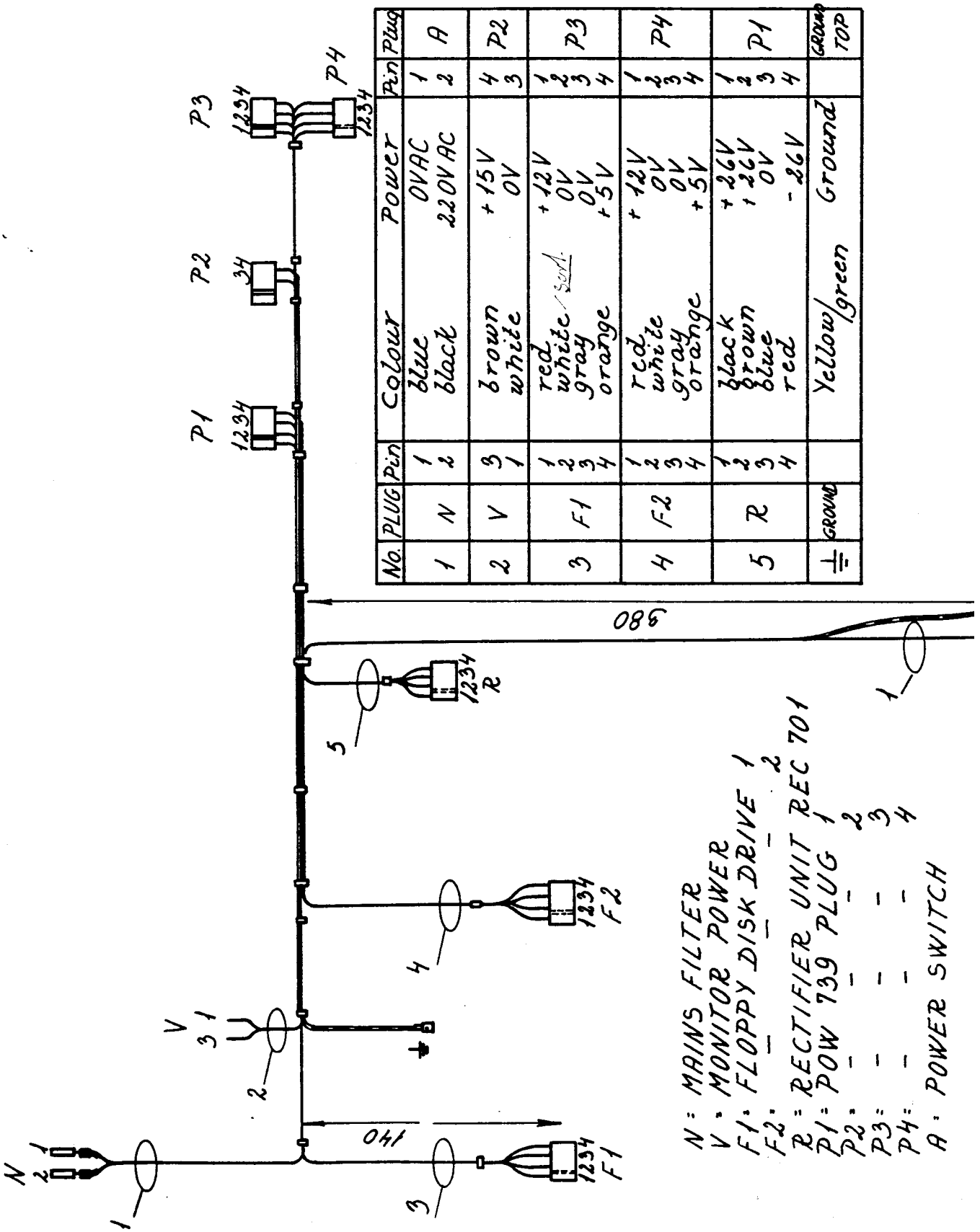


Fig. 3.2. KBN 702 with MIC 702 mounted.



MIC 702 Fig. 33. Filter, Transformer, Blower and REC 702.
R 13095



No.	PLUG	Pin	Colour	Power	Pin	Plug
1	N	1	blue	0VAC	1	A
		2	black	220VAC	2	
2	V	3	brown	+15V	4	P2
		1	white	0V	3	
3	F1	1	red	+12V	1	P3
		2	white/black	0V	2	
		3	gray	0V	3	
		4	orange	+5V	4	
4	F2	1	red	+12V	1	P4
		2	white	0V	2	
		3	gray	0V	3	
		4	orange	+5V	4	
5	R	1	black	+26V	1	P1
		2	brown	+26V	2	
		3	blue	0V	3	
		4	red	-26V	4	
⏚	GROUND		Yellow/green	Ground		GROUND TOP

Fig. 3.4. Internal Cable in KBN 701.

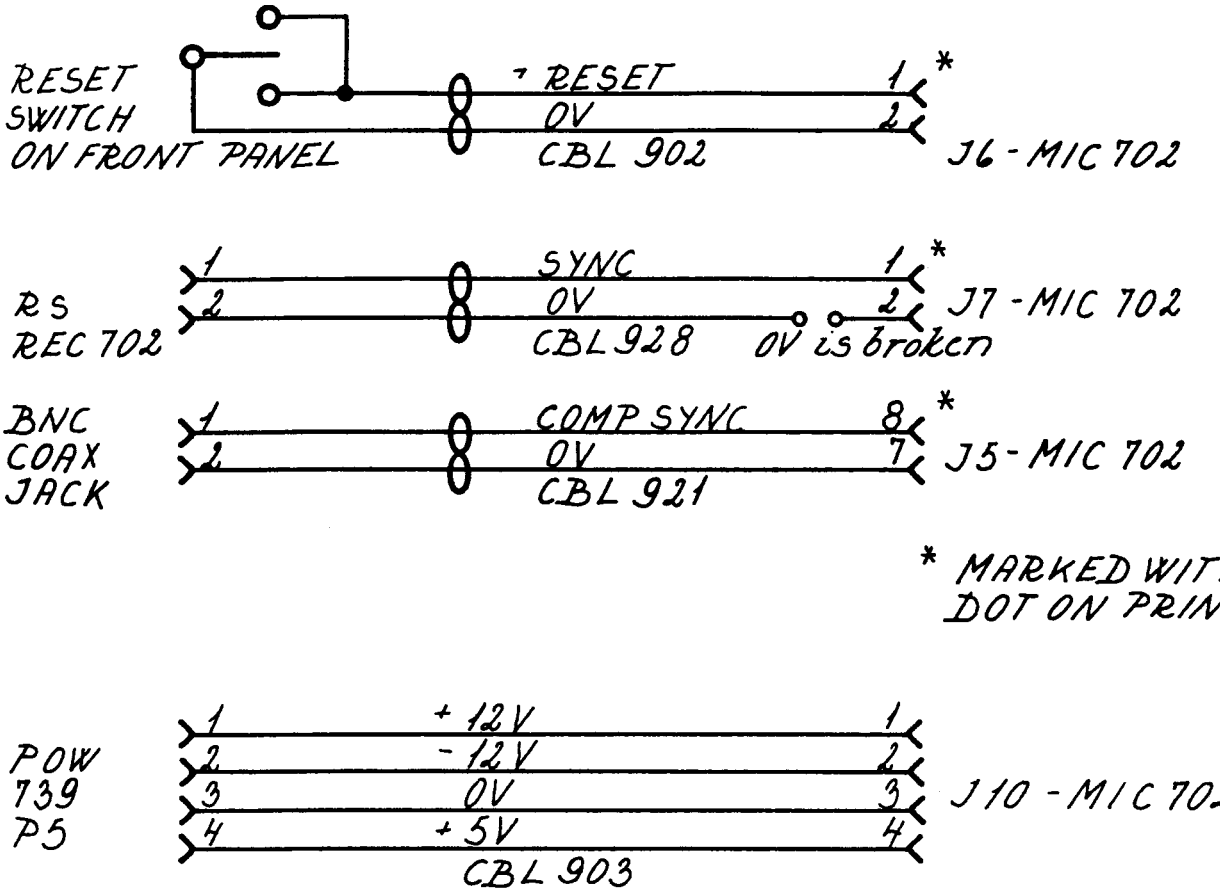
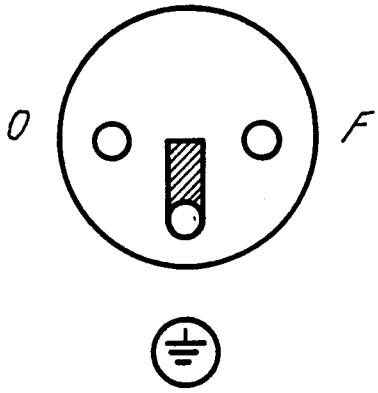


Fig. 3.5. Cable connections KBN 702 to MIC 702 and POW 739.

Connector1	Wire	Connector2
F	BROWN	L
⏚	YELLOW/GREEN	⏚
O	BLUE	N



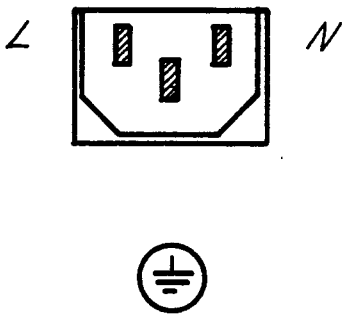


Fig. 3.6. Power Cable CBL 440.

4. POW739 POWER SUPPLY 4.

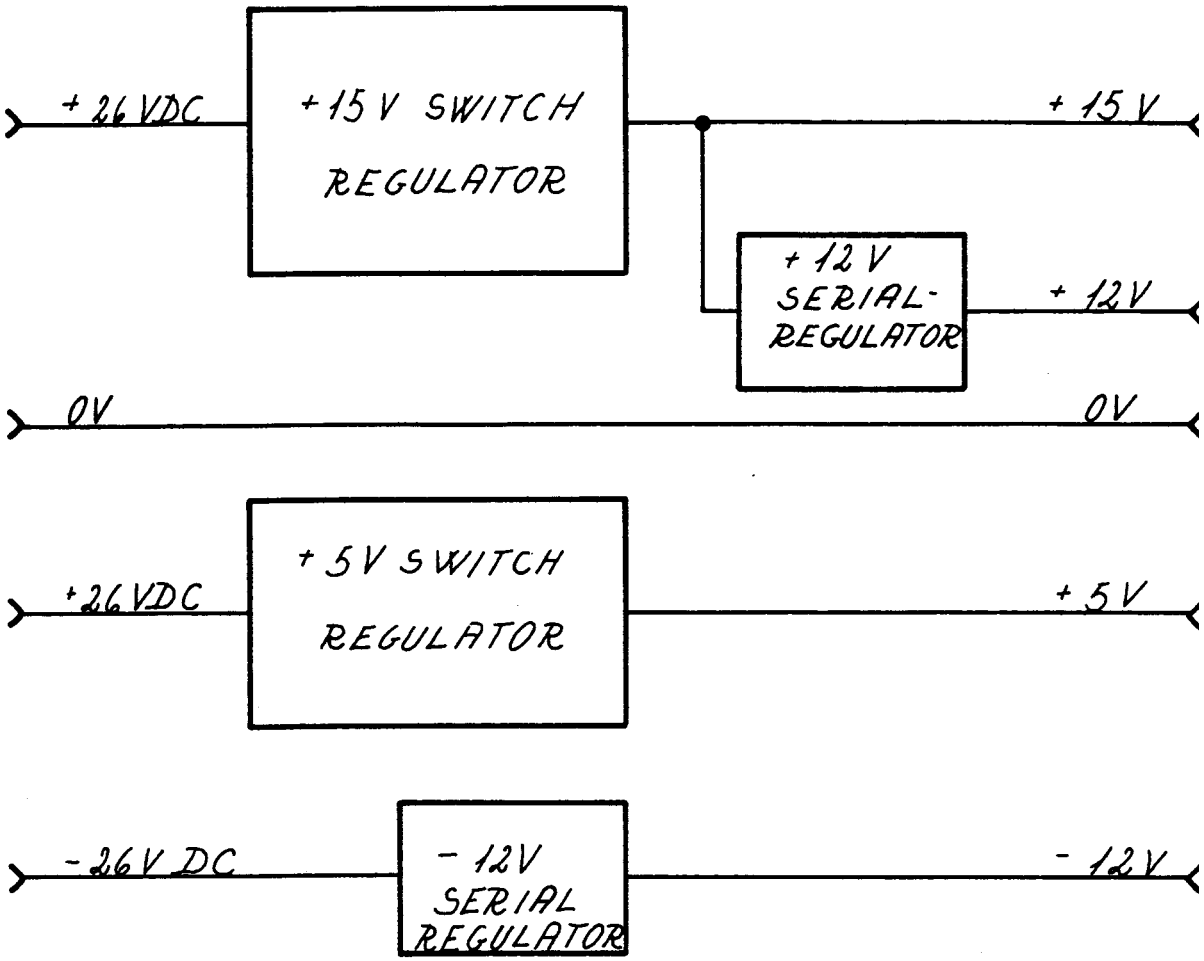
The power supply to RC702 is built on a single printed circuit board. Fig. 4.1 shows a block diagram for the POW739.

Input to the powersupply is +26 V DC or -26 V DC delivered from REC702 rectifier unit. This unit is described in chapter 3.

Fig. 4.2 shows the layout of the printed circuit board.

Fig. 4.3 and fig. 4.4 show the circuit diagram for the unit.

Fig. 4.5 and fig. 4.6 show the timing diagram for the unit.



V OUT	IMAX	ΔV MAX
+15 V	1,4 A	± 0,5 V
+12 V	2,6 A	± 0,5 V
+5 V	5,0 A	± 0,1 V
-12 V	0,2 A	± 0,5 V

Fig. 4.1. POW 739 Block Diagram.

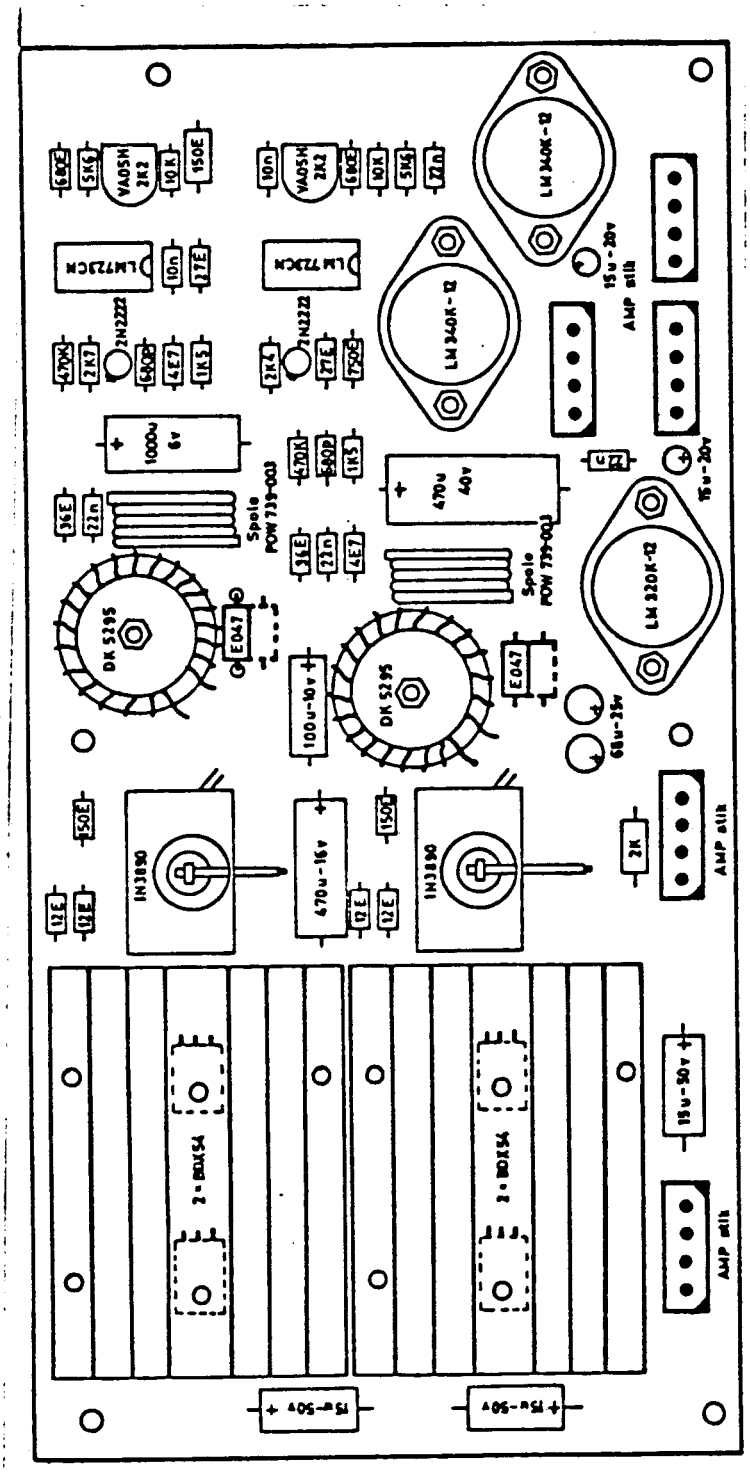
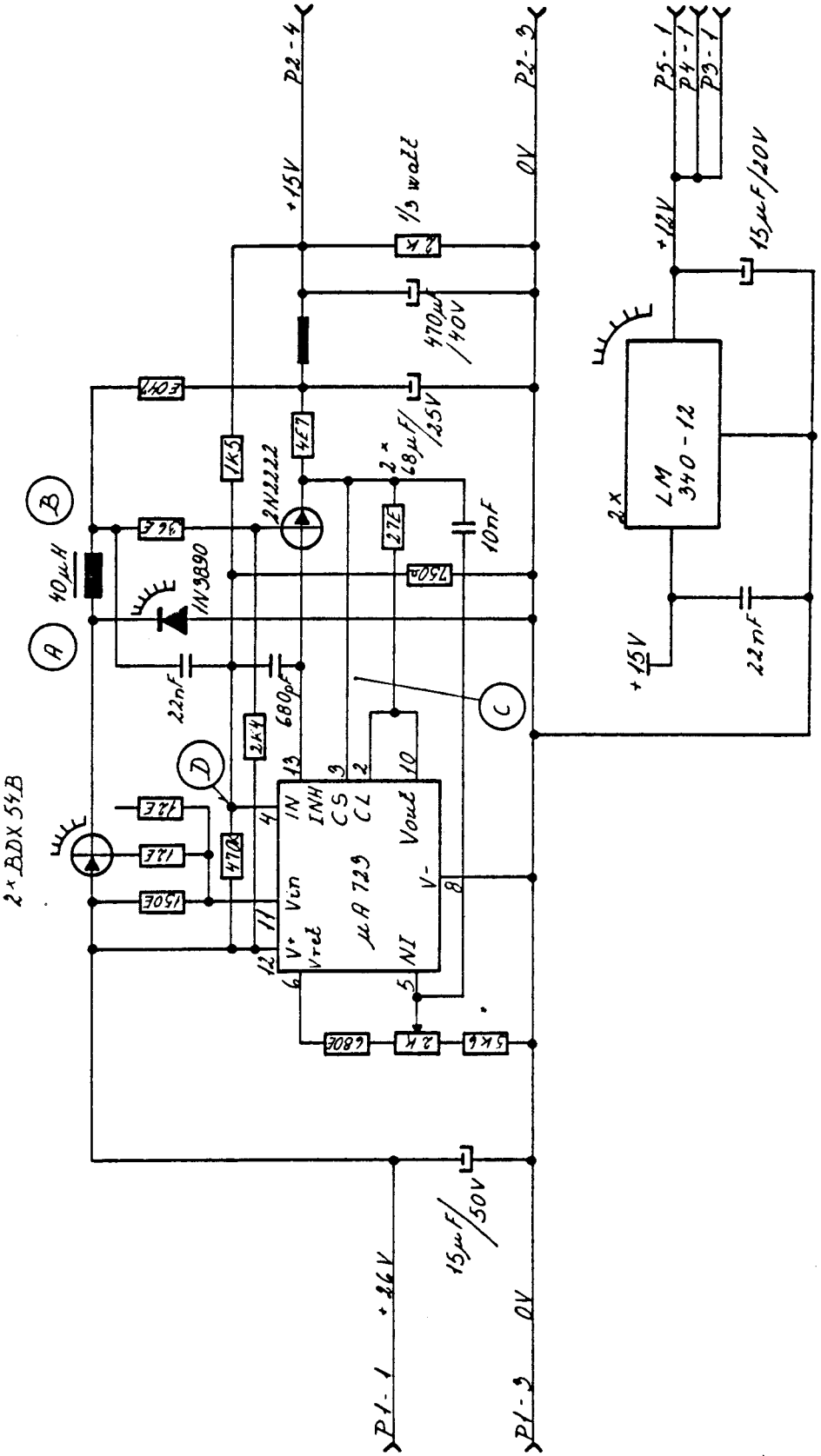
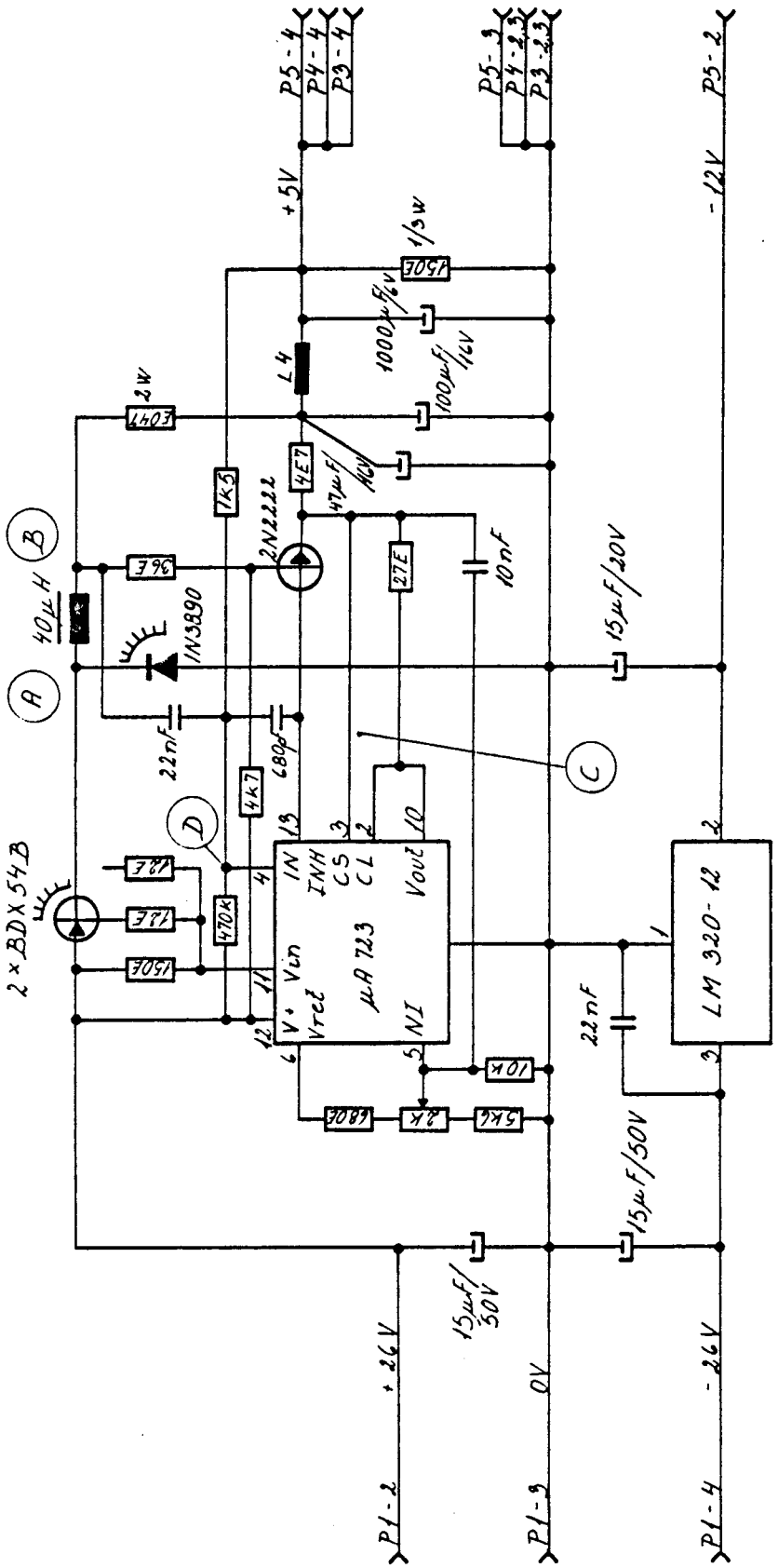


Fig. 4.2. POW 739 LAY OUT



MIC 702
R 13096

Fig. 43. POW 739, +15V and +12V



MIC 702
R 13097

Fig 4.4 POW 739, +5V and -12V

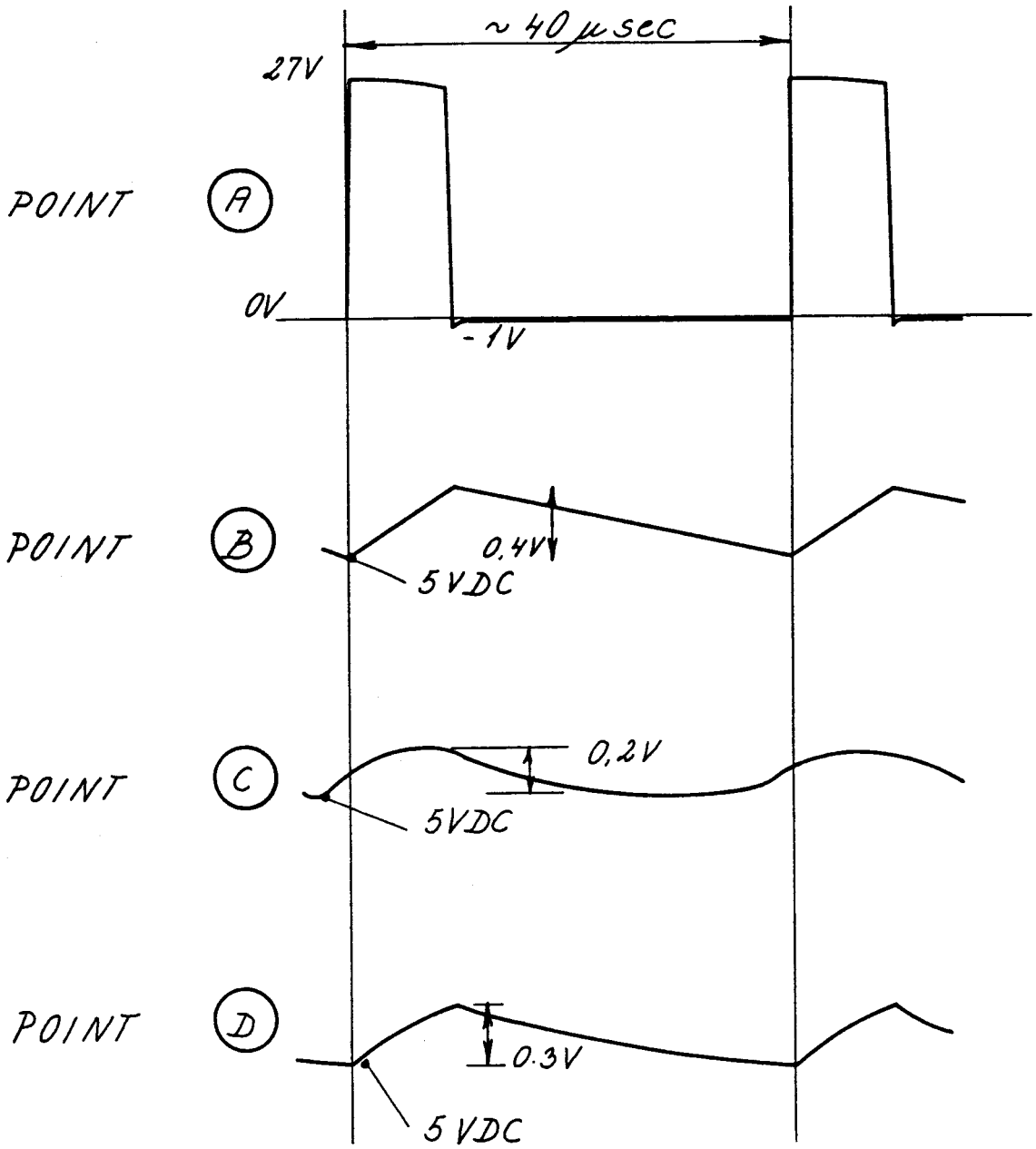


Fig. 4.5. Timing diagram for +5V supply loaded with MIC 702 and one mini floppy.

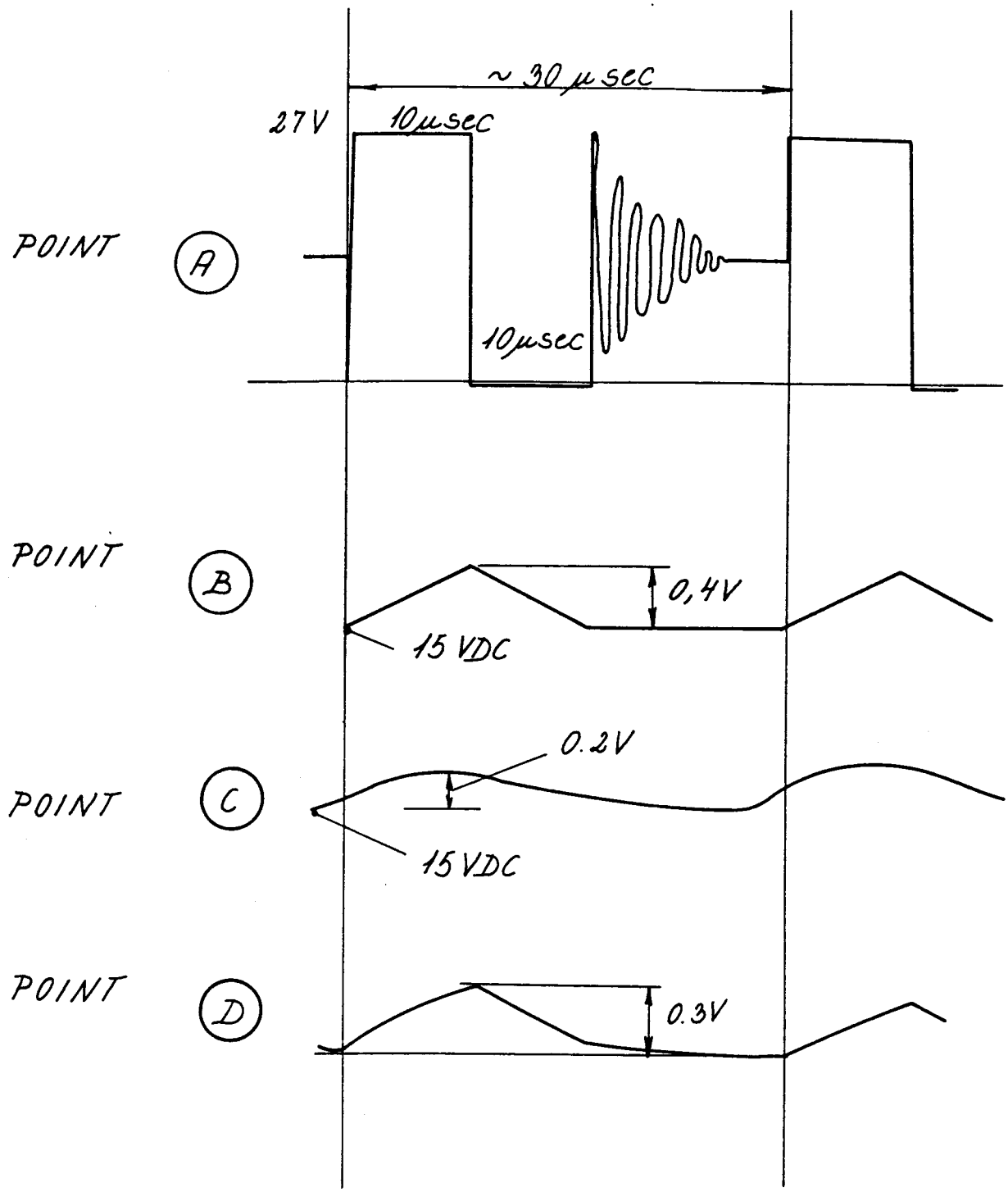


Fig. 4.6. Timing Diagram for +15V supply Loaded with MIC 702 and mini Flopp and RC 752.

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