Title:

TECHNICAL DESCRIPTION
FOR
MEM 805 SEMICONDUCTOR MEMORY

A/S REGNECENTRALEN

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TECHNICAL DESCRIPTION

Abstract:

This publication is a Technical Description
of Semiconductor Memory - MEM 805 - designed
for the RC 8000 computer family

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1. DESCRIPTION

The memory is a semiconductor memory, which is designed to be used by the RC 8000 computer family.

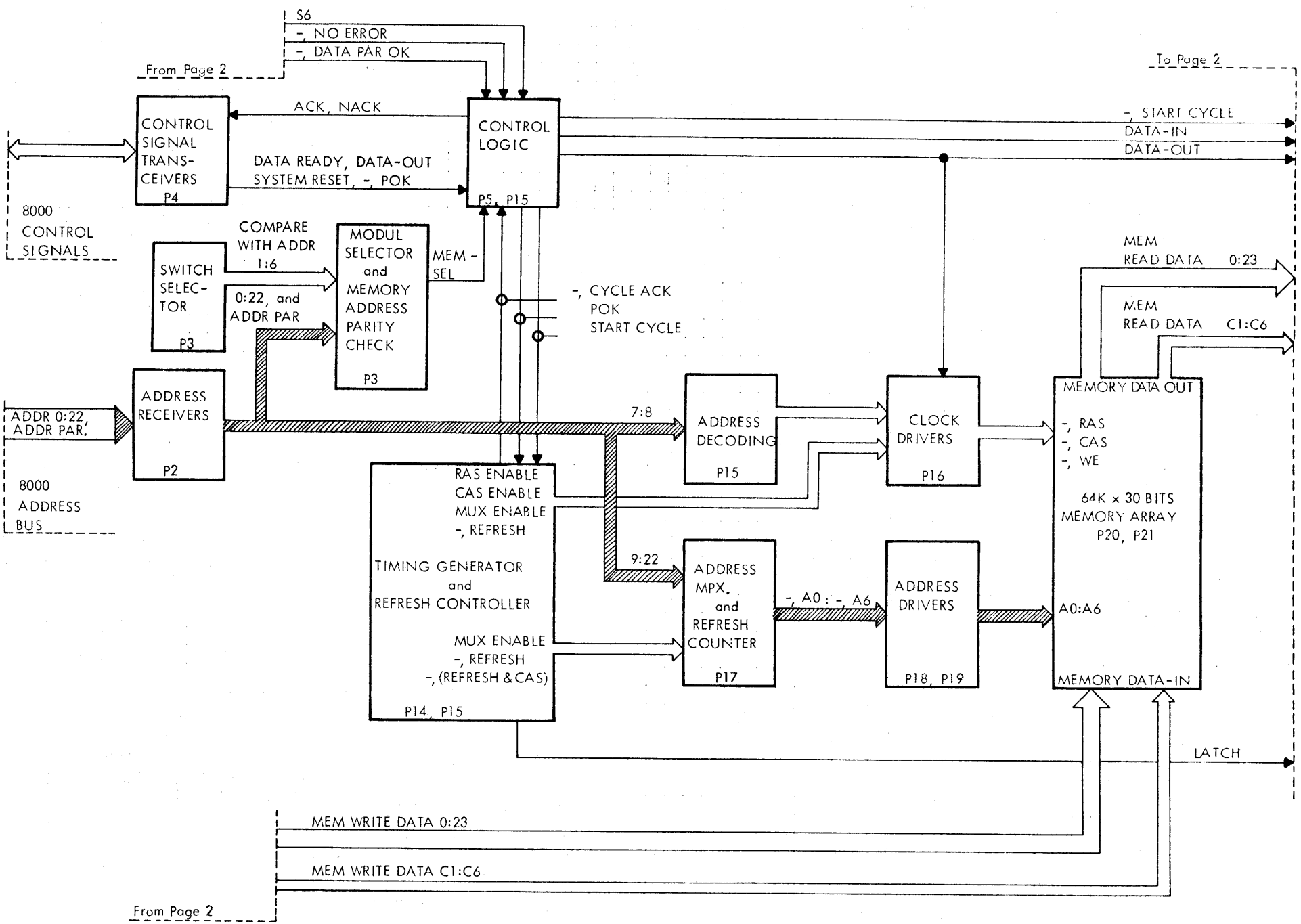
The memory consists of one multilayer printed circuit card, which provides 64K x 30 bits.

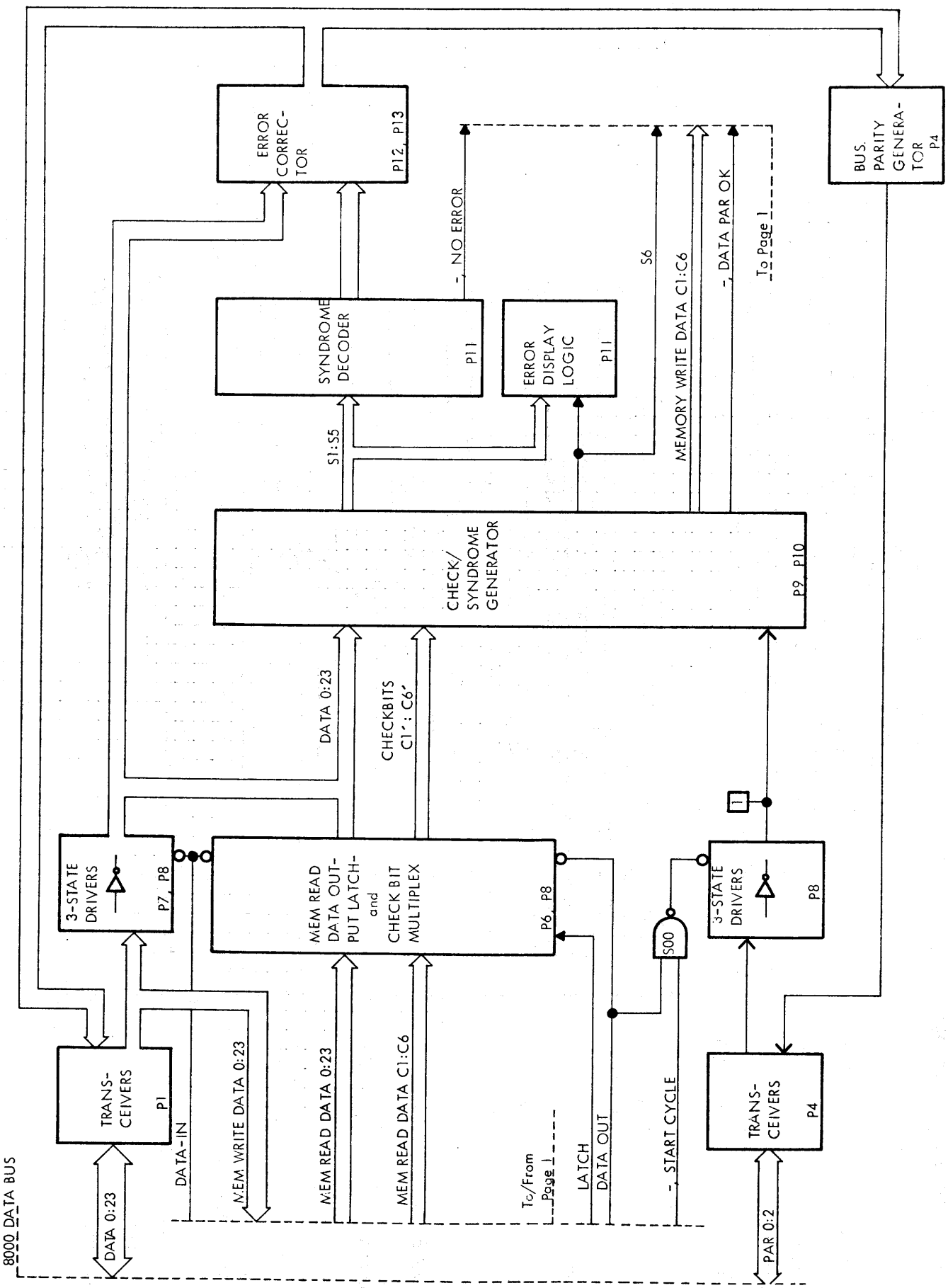
The memory can be connected directly to the RC 8000 system bus. The PCB contains all of the circuits necessary for a CPU or peripheral device to read data stored in the dynamic RAM, or to write data into the dynamic RAM. The memory array consists of 120 memory chips each of which contains 16384 words by one bit.

To increase memory reliability a single error correction and double error detection (SEC - DED) code has been incorporated. This code requires 6 check bits / data words.

Blockdiagrams 1 and 2 in section 2 show the structure of the memory. The figures in the boxes refer to the corresponding logic diagram.

A13565 MEM 805 BLOCKDIAGRAM 1





781108 VH 781221 ABP

MEM 805

BLOCKDIAGRAM

p. 2 of 2

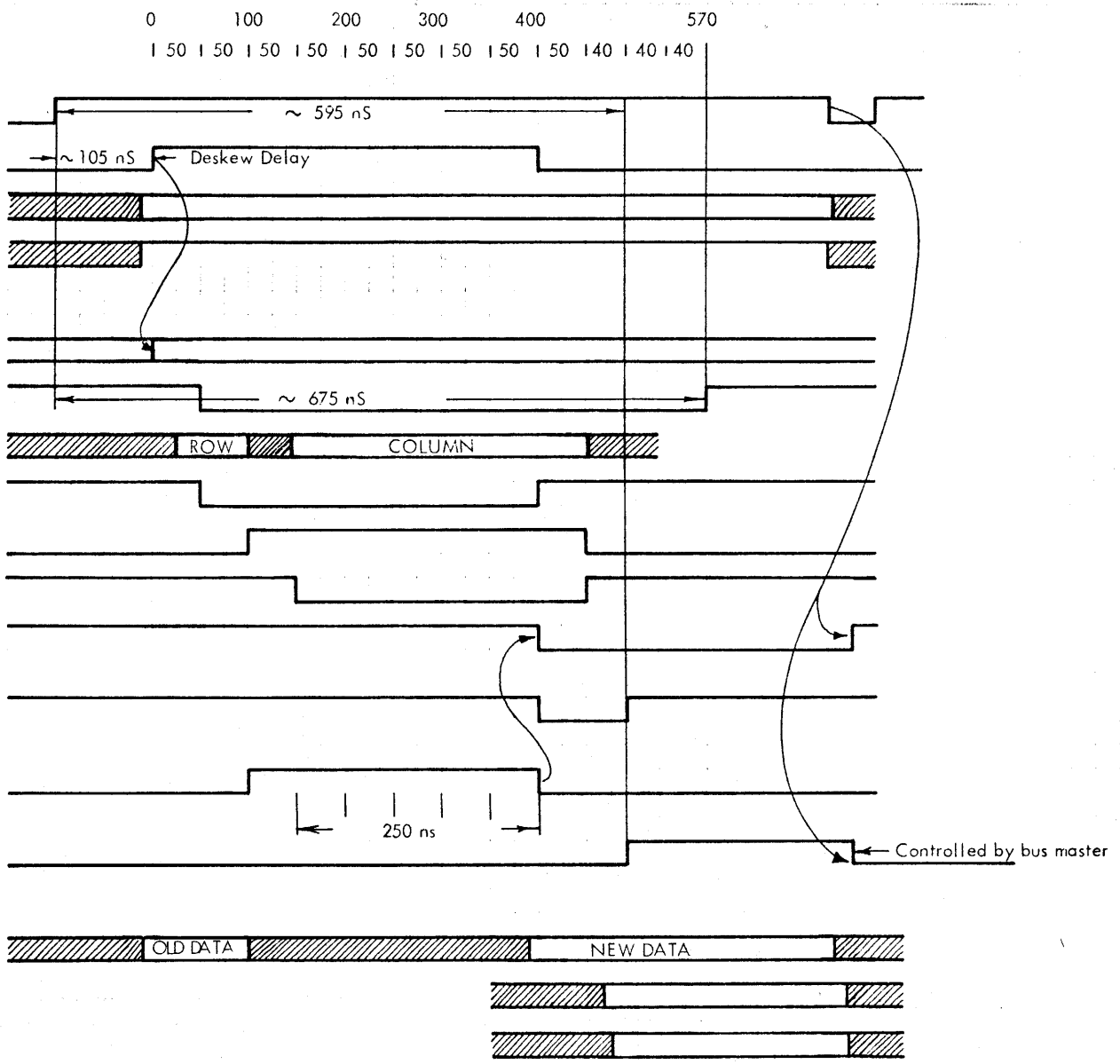
A13566

A13567

MEM 805

TIMING CHART
READ CYCLE

TIME nS		
DATA READY A	4	104-6
START CYCLE	5	78-5
ADDR 0:22, PAR	2	
DATA IN	15	110-12
TO	14	55-5
READY	15	111-11
-, A0:-, A6	17	
-, RAS	16	
MUX	15	
-, CAS	16	
-, SEND DATA	5	85-6
-, CYCLE ACK	14	75-6
LATCH	14	55-9
ACK or NACK (Nack if double error)	5	
READ DATA OUTPUT LATCH	6	
CORRECTED DATA	12, 13	
-, 8000 DATA BUS	1	



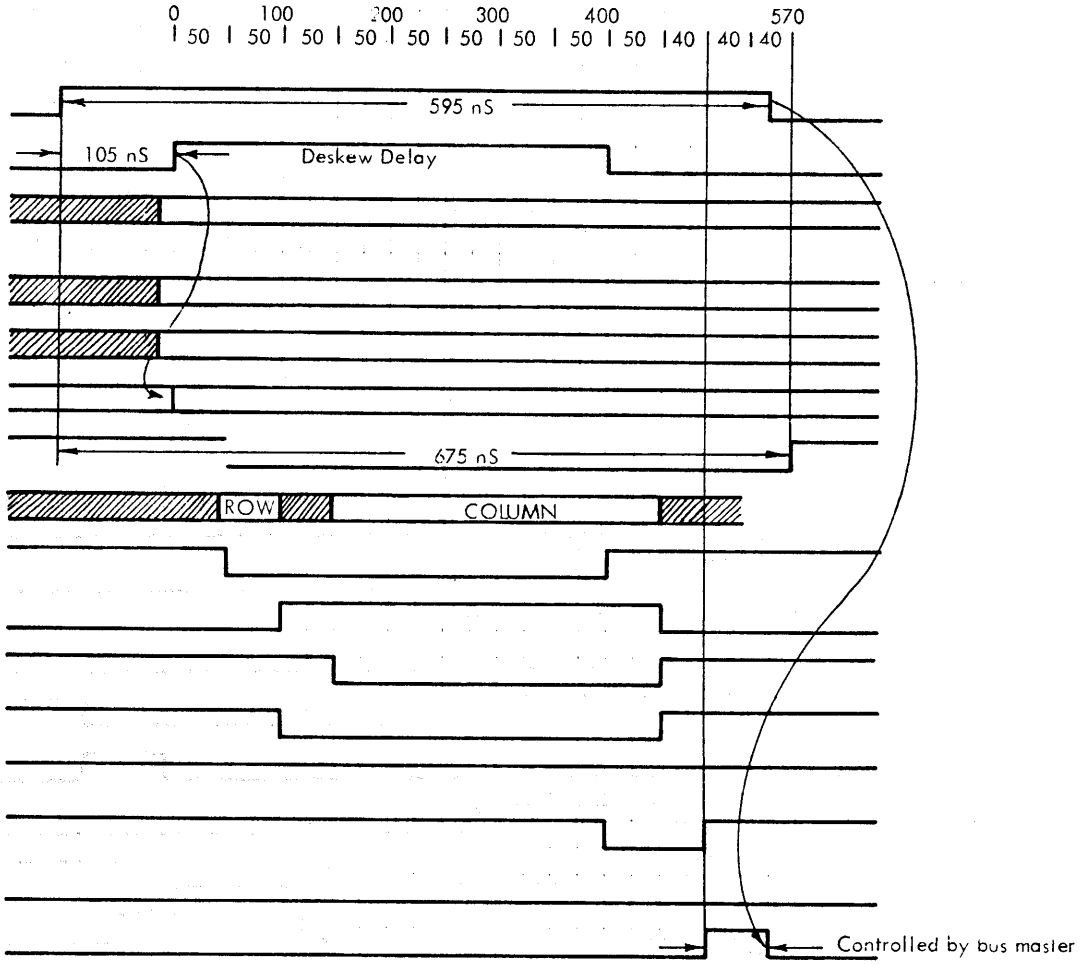
TC 1

MEM 805

A13568

TIMING CHART
WRITE CYCLE

	781207 VH	781222 ABP
TIME nS		
DATA READY A	4	104-6
START CYCLE	5	78-5
ADDR 0:22, PARITY	2	
8000 DATA REC 0:23, PARITY REC 0:2	1 4	
8000 DATA OUT REC	4	
TO	14	55-5
READY	15	111-11
-, A0 - -, A6	17	
-, RAS	16	
MUX	15	
-, CAS	16	
-, WE	16	
-, SEND DATA	5	85-6
-, CYCLE ACK	14	75-6
LATCH	14	55-9
ACK	5	88-8

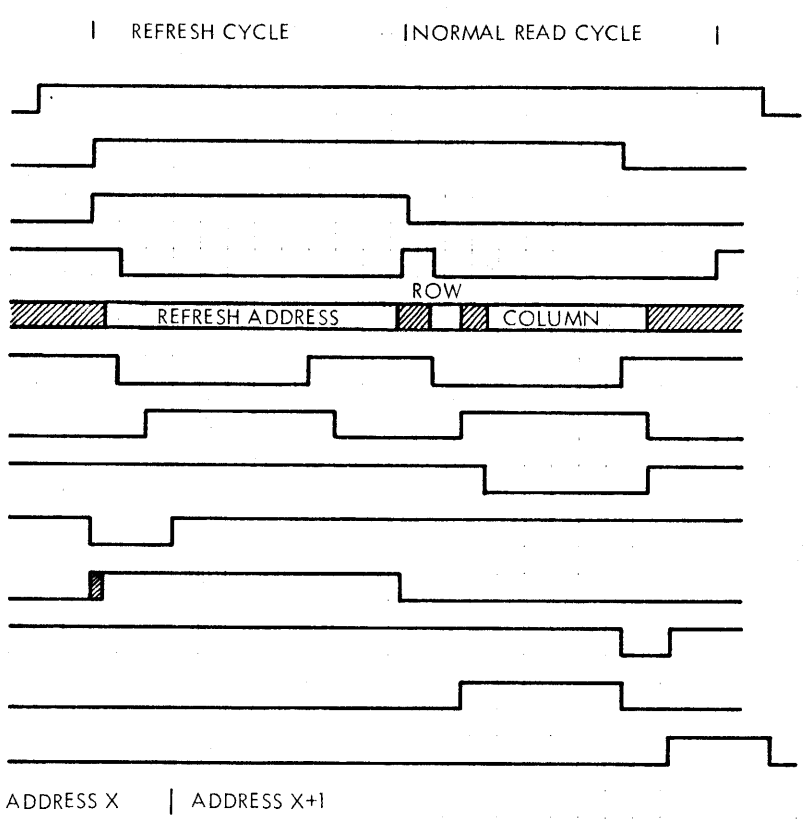


TC 2

TIMING CHART
REFRESH INTERFERENCE

781207 VH 781227 ABP

DATA READY A	4	104-6
START CYCLE	5	78-5
TO	14	55-5
READY	15	111-11
-, A0 : -, A6	17	
-, RAS	16	
MUX	15	
-, CAS	16	
-, REFRESH REQ	14	65-5
REFRESH	14	85-11
-, CYCLE ACK	14	75-6
LATCH	14	55-9
ACK	5	88-8
REFRESH COUNTER	17	



4. FUNCTIONAL DESCRIPTION

The functional description will refer to blockdiagrams (section 2) and logic diagrams (section 5) using the abbreviations BD and LD.

4.1 Internally RAM Chip Organization

The RAM chip is organized internally as two 8K sub-arrays which form a single 128 x 128 balanced matrix (128 rows x 128 columns). The column decoder and sense-refresh amplifiers are in the middle of the matrix and "dummy cells" are located at each side. The "dummy cells" establish a voltage reference for the balanced sense amplifiers. One of the array halves inverts data and will store an input "one" as a low level in the storage cell. A second inversion is performed by the output circuitry so that the internal inversion is not seen at the chip terminals. The control circuitry surrounding the matrix is controlled by networks of clock generators which are activated by the externally applied Row and Column Address Strobes, which also latches the Row/Column Addresses into internally located latches.

4.2 Refresh

Since charge leaks of the storage capacitor of a dynamic RAM chip it must be replenished periodically to retain its data. Refresh of a 16K dynamic RAM chip is accomplished by performing a memory cycle at each of the 128 row addresses within the retention time. All of the 120 RAM chips in this RC 8000 memory array are refreshed simultaneously. The need for refresh cycles is selfdetermined by the memory control logic, which times out an interval of 1/128 of the retention time. At the end of each interval, the logic either initiates a special refresh cycle or steals the next cycle for refresh, if a normal cycle is in progress.

4.3 Memory Operation

The RC 8000 semiconductor memory is capable of performing operatious in the Read and Write modes. Each operational mode is defined in the following paragraphs.

4.3.1 Read

Read cycles are initiated by the bus master, which places the address on the ADDRESS bus, places the transfer direction code on the DATA OUT line (DATA OUT = 0), and sets the DATA READY control signal to logical 1. The memory delays the DATA READY signal to compensate for skews, device address decoding, and address parity check. At the end of the delay, a memory read cycle is started if the memory is addressed, which means:

1. ADDR (0) equal to logical 0.

2. ADDR (1:6) equal to the same value as selected by the memory device selector switches (IC 107 , LD 3).

3. Odd parity of ADDR (0:22) and ADDR PAR.

Information stored in the addressed memory location are latched into a register at the end of the access time. To increase memory reliability a single error correction and double error detection code has been incorporated. The information stored consists of 24 data bits and 6 check bits. When this information has been latched into the register they generate a syndrome pattern that corrects any single error and detects all double errors. After error correction, data bus parity generation and activation of the data bus transmitters, the DATA ACK signal is sent to the bus master. DATA NACK signal is sent if a double error has been detected. Short time after the leading edge of DATA ACK / DATA NACK the memory cycle is terminated. The memory timing generator is described in section 4.4.

4.3.2 Write

Write cycles are initiated by the bus master, which places the address on the ADDRESS bus, the data on the DATA bus, the transfer direction code on the DATA OUT line (DATA OUT = 1), and sets the DATA READY signal to logical 1. The memory delays the DATA READY signal to compensate for skews, device address decoding, address parity check, and data bus parity check. At the end of the delay, a memory write cycle is started if the memory is addressed and data bus parity ok. In case of data bus parity error a DATA NACK signal is sent to the bus master, which terminates the bus cycle. To increase memory reliability a single error correction and double error detection code has been incorporated. The code uses 6 check bits, which are generated from the 24 data bits. After check bit generation the total information (30 bits) is written into the memory and the DATA ACK signal is set to logical 1. Short time after the leading edge of DATA ACK the memory write cycle is terminated. The memory timing generator is described in section 4.4.

4.4 Memory Timing Generator (LD 14 , LD 15)

The memory timing generator is started by either the bus master read/write cycle request or by the internally generated refresh request. The timing generator generates the same signals regardless of the type of cycle being performed. The signals generated are Row Address Strobe enable (RAS ENABLE), Column Address Strobe enable (CAS ENABLE), Multiplex enable (MUX ENABLE), Finish, and Ready. The ready signal when 0 volt indicates that a cycle is in progress. RAS and CAS timing signals latches row respective column addresses into row and column latches located internally in the memory chips. 16K - 16 pins dynamic RAM's requires the total 14 bits address to be multiplexed into two 7 bits addresses. The multiplexing is done by means of the mulitplex signal, and the memory address selector (LD 17). The trailing edge of the finish signal sets DATA ACK / DATA NACK at the end of the timing sequence.

The timing generator uses digital delay lines. When a memory cycle is started the 74S74 FF is triggered. The 74S74 FF is used as a divide by two circuits so only one transition edge will pass down the delay line. The 74S86 ex- or gates detect the transition at the appropriate tap down the delay line. The ex- or gates respond with a pulse whose width is equal to the spacings of the inputs along the delay line. The pulse will have the same polarity regardless of the polarity of the transition passing through the delay line.

4.5 Memory Refresh Controller and Refresh Counter (LD 14 , LD 17) 4.5

The request for a refresh cycle is executed by means of an oscillator, a counter, and a FF. This circuit times-out when a refresh cycle is required. A refresh cycle is required every 15.625 µS (15.625 x 128 = 2000 µS). The time-out time of the circuit is 15.61 µS. The output from the counter sets the request FF, which sets the refresh cycle FF provided a normal cycle is not in progress. If a normal cycle is in progress the refresh FF will not be set until this cycle is terminated.

The refresh signal gates the contents of the refresh counter to the A0:A6 address lines of the memory array and activates all of the row address strobes thus refreshing the entire memory array. During the refresh cycle the refresh request FF is cleared and the refresh counter incremented by one thus preparing the refresh controller for the next refresh cycle. The refresh FF will be reset at the end of the refresh cycle.

During refresh cycles the Cycle Acknowledge signal, the Read Data Available signal, and the Latch signal are disabled.

4.6 Address Path (BD 1) 4.6

RC 8000 address bus uses 23 address lines and one address parity line, which makes the parity odd.

Address bus receivers are standard RC 8000 transceivers TEXAS INSTRUMENTS SN 75138, only the receiver part of 75138 is used (LD 2). After the address receivers the address lines are named ADDR (0:22) and ADDR PAR, with ADDR 22 as the least significant bit.

All of the ADDR lines are routed to the memory modul selector and address parity checker (LD 3), which makes out whether the memory is addressed or not. The memory is only started if it is addressed, which means:

1. ADDR (0) equal to logical 0.

2. ADDR (1:6) equal to the same value as selected by the memory modul selector switches.

3. Odd parity of ADDR (0:22) and ADDR PAR.

4. Data Ready control signal equal to logical 1.

ADDR (7:8) are routed to an one of four decoder (LD 15), which select one of four 16K x 30 bits memory groups. ADDR 9:22 are via address multiplexer (LD 17) and address line drivers (LD 18 , 19) routed to all of the dynamic RAM JC's to select one 30 bits word out of 16384 words. Three types of addresses must be supplied to a dynamic RAM JC. These are the row address, the column address, and the refresh address. The address multiplexer multiplexes ADDR 9:22 to two 7 bits output addresses, which are used as row and column address. ADDR 16:22 becomes the row address and 9:15 becomes the column address. During refresh cycles the contents of the refresh counter becomes the output of the address multiplexer.

The outputs of the address multiplexer are inputs to the address line drivers. Damping resistors are inserted between the outputs of the drivers and the address inputs of the dynamic RAM JC's. These damping resistors preserve the clean wave shape of the address signals.

4.7 Memory Clock Signal Drivers (LD 16) 4.7

RAS, CAS, and WE drivers are two input 74S37 buffer gates. Since it is the presence of both RAS and CAS that starts the internal timing of a dynamic RAM both RAS and CAS can be decoded for chip selection. The memory uses the RAS signal as chip select. Address bits 7:8 from the bus master selects between four pair of RAS drivers. Each pair of buffer gates drives one 16K x 30 bits memory group. Each driver of the pair drives 15 bits. During refresh cycles the refresh signal makes all of the RAS drivers active. CAS drivers are not active during refresh cycles. The CAS signal is not needed during refresh since all 128 cells in the selected row of a memory chip will be refreshed simultaneously via the 128 sense amplifiers, and the RAS signal. No data is transferred to the data-in or data-out buffer of the memory chip when CAS is inactive. Each CAS driver drives 15 memory chips. The WE drivers are active during write into memory. The WE signal many change state during refresh cycles, however, this has no effect since CAS is not active. By means of a manual switch it is possible to disable writing of check bits. This feature, which is used for diagnostic purposes, dictates use of separate WE drivers for the check bit part of the memory. WE drivers for check bits are shown on LD 21. Each check bit driver drives 12 memory chips. WE drivers for the data part of the memory drives 15 memory chips (bits 0:14) and 9 memory chips (bits 15:23). A damping resistor is inserted between the clock drivers and the clock inputs of the memory array. This damping resistor preserve the clean waveshape of the signal.

4.8 Error Control (BD 2) 4.8

The RC 8000 data bus uses 27 bidirectional data lines. A word is divided into three octets with one parity bit per octet. The parity bit makes the parity of the octet odd. The parity bits are not written into memory. During write operations data received from the bus are checked for correct parity. A parity error causes a DATA NACK to be sent to the bus master. During read operations a parity of the data read from memory is generated and sent to the bus. Error control with the memory is executed through the use of a single error correction/double error detection code.

4.9 Error Correction and Detection Logic (BD 2) 4.9

To correct single bit error, information in the form of check bits is required to address the bit in error. Since an error also may occur in the check bits, they are required to address themselves also. For a memory system with a specified word length, the number of check bits needed for a Single Error Correction code (SEC) can be determined by the Hamming relationship:

$$2^c \geq m + 1 + c$$

where m = number of data bits, and c = number of check bits. For a 24 bits RC 8000 word, five check bits are needed. For double error detection only one more check bit is needed.

Data written into memory are the inputs to a check bit generator (LD 9 , LD 10). The check bit generator is a parity generation circuit, which constructs the check bit field from selected fields of the data word. Figure 4.9.1 shows the parity check matrix used. The check bit generator generates an odd parity sum for some bit combinations and an even parity sum for others.

The odd-even mixture makes it possible to detect failures that manifest themselves as all 0's or all 1's combinations. C6 check bit is generated as an even parity sum of data bits 0:23 and check bits 1:5. Check bits are stored alongside corresponding data bits in the memory.

During memory access the syndrome generator (LD 9 , LD 10) generates new check bits from the fetched data. These new check bits are individually compared with the stored check bits that were fetched from memory. When fetched data or check bit contain an error, old and new check bits differ. The comparison produces five syndrome bits (S1:S5). Each syndrome bit is 0 if the respective old and new check bits are equal, and 1 if they are different. If the five syndrome bits are other than zeros an error exists, and the syndrome bit pattern uniquely pinouts the bit in error. The sixth syndrome bit (S6) is the parity sum of the stored data and check bits. If this parity sum is odd, S6 is 1; if even S6 is 0. These six syndrome bits can correct single bit errors and detect double bit error according to the following simple rules:

If S6 = 1 and S1:S5 $\neq$ 0 in general, a single error has occurred. The syndrome decoder (LD 11) decodes the syndrome bits 1:5, and pinouts the bit in error. The error corrector (LD 12 , LD 13) corrects the error merely by inverting the bit. However, occasionally the five syndrome bits will indicate a code not existing in the parity check matrix (3_{10} , 31_{10}); if this happens and S6 = 1, an odd number of errors is in the word. These errors are treated as single errors.

If S6 = 1 and S1:S5 = 0 an error in the stored C6 bit is present.

If S6 = 0 and S1:S5 $\neq$ 0 an uncorrectable double error or an other even error is present. In this case a DATA NACK is sent to the bus master.

If S6 = 0 and S1:S5 = 0 no error exists in the word.

An example is shown in Figure 4.9.2 of how the error correction works.

The single error correction circuits may be disabled by means of the corrector ON/OFF switch (LD 11). This feature is used for diagnostic purposes.

SYNDROME BIT PATTERN ↓	DATA BIT																								CHECK BIT						PARITY OF DATA AND CHECK BIT
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	C1	C2	C3	C4	C5	C6	
S1	1	1	1	1	1	1	1	1							1	1				1	1	1		1	1						ODD
S2	1				1	1		1	1	1	1	1	1	1	1	1							1	1		1					EVEN
S3		1			1				1			1	1		1		1	1	1	1	1	1	1	1			1				ODD
S4			1				1	1		1		1		1	1	1	1		1	1		1	1					1			EVEN
S5				1		1	1				1		1	1		1		1	1		1	1	1	1					1		ODD
S6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	EVEN

SEC-DED PARITY CHECK MATRIX

Fig. 4.9.1

Parity check matrix for Single Error Correction and Double Error Detection for 24 data bits and six check bits. Check bit C6 represents the overall parity bit, which makes double error correction possible. Each columb (S1 to S6) represents the syndrome pattern associated with corresponding data and check bits.

No error : S_1 through S6 = 0

Single error : S6 = 1; S_1 through S6 indicates the corresponding syndrome pattern.

Double error : S6 = 0; S_1 through S5 ≠ 0

WRITE

	DATA BITS																							CHECK BITS					
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	C1	C2	C3	C4	C5	C6
WRITE DATA →	0	0	0	1	1	0	1	0	1	1	0	1	1	1	0	0	0	0	0	1	1	0	1	0	0	1	0	0	1	1

READ

	DATA BITS																							CHECK BITS					
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	C1	C2	C3	C4	C5	C6
READ DATA →	0	0	0	1	1	0	1	1	1	1	0	1	1	1	0	0	0	0	0	1	1	0	1	0	0	1	0	0	1	1
NEW CHECK BITS →																									1	0	0	1	1	0

HOW ERROR CORRECTION WORKS
Fig. 4.9.2

For the data word shown, the check bit field is 010011.
The check bit field is stored along with the data at the same address. As that location is read, the data and check bit field are used to compute the syndrome bit patterns 11010. By decoding of the syndrome bit pattern using the parity check matrix fig. 4.9.1 we see that bit 7 is in error and should be inverted.

SYNDROME BITS					
S1	S2	S3	S4	S5	S6
1	1	0	1	0	1

4.10 Error Display Logic (LD 11) 4.10

Whenever an error occurs (S6 = 1 or S1:S5 ≠ 0), syndrome bit S1:S6 and ADDR 7:8 are stored in a 8-bits register, which controls 8 Light Emitting Diodes Located on the front panel. In this way the error display will always indicate the error status of the latest error occurred. By means of the parity check matrix, the bit in error can be identified. The address bits displayed will identify the group of the memory array - one 16K x 30 bits group out of four - so that the defective memory chip can be readily located. The Error Display ON/OFF switch may be used to clear the error status or to disable the display.

4.11 Memory Array (LD 20 , LD 21) 4.11

The memory array consists of 120 16 pins standard dual-in-line packages. The memory chips are MOS dynamic random access circuits organized as 16384 words by 1 bit.

The first function the chip performs regardless of whether the cycle will be a read cycle, write cycle, or refresh cycle is to latch and decode the 7 row address bits. One of the 128 rows will be selected. Next the contents of all 128 cells in the selected row will be sensed by the sense amplifiers at the top of the column and data held there for use later in the cycle.

Since the first function of the chip is to read the information contained in a row of cells, inputs such as column address, write enable, and data-in are not needed until the row of cells is read by the sense amps. This allows time to first strobe in the row address and later with CAS-strobe to latch the column address. Next, the column address is decoded and one of the 128 sense amps will be selected to output data to the output buffer. The -, Write Enable signal is high during read cycles. Also the data is rewritten into the row from which the data was read initially. If -, Write Enable is low, the data on the data-in line is latched by the "and" of CAS, RAS, and WE. The selected sense amp now receives the new data and the information being held by the other 127 sense amps will be rewritten into the selected row. Thus, the information in the selected row is refreshed by any cycle. Each row must receive at least one cycle to refresh it every 2 mS.

The memory chips, which stores the check bits, receives a special -, Write Enable signal. This signal is under control of a switch capable of disabling the signal. This feature is used for diagnostic purposes.

SIGNAL	DESTINATION	DESCRIPTION
8000 DATA REC. 0:15	p 7 p 20 p 21	Received data 0:15 from the RC 8000 system bus
8000 DATA REC. 16:23		
8000 DATA REC. 16:23	p 8 p 21	Received data 16:23 from the RC 8000 system bus

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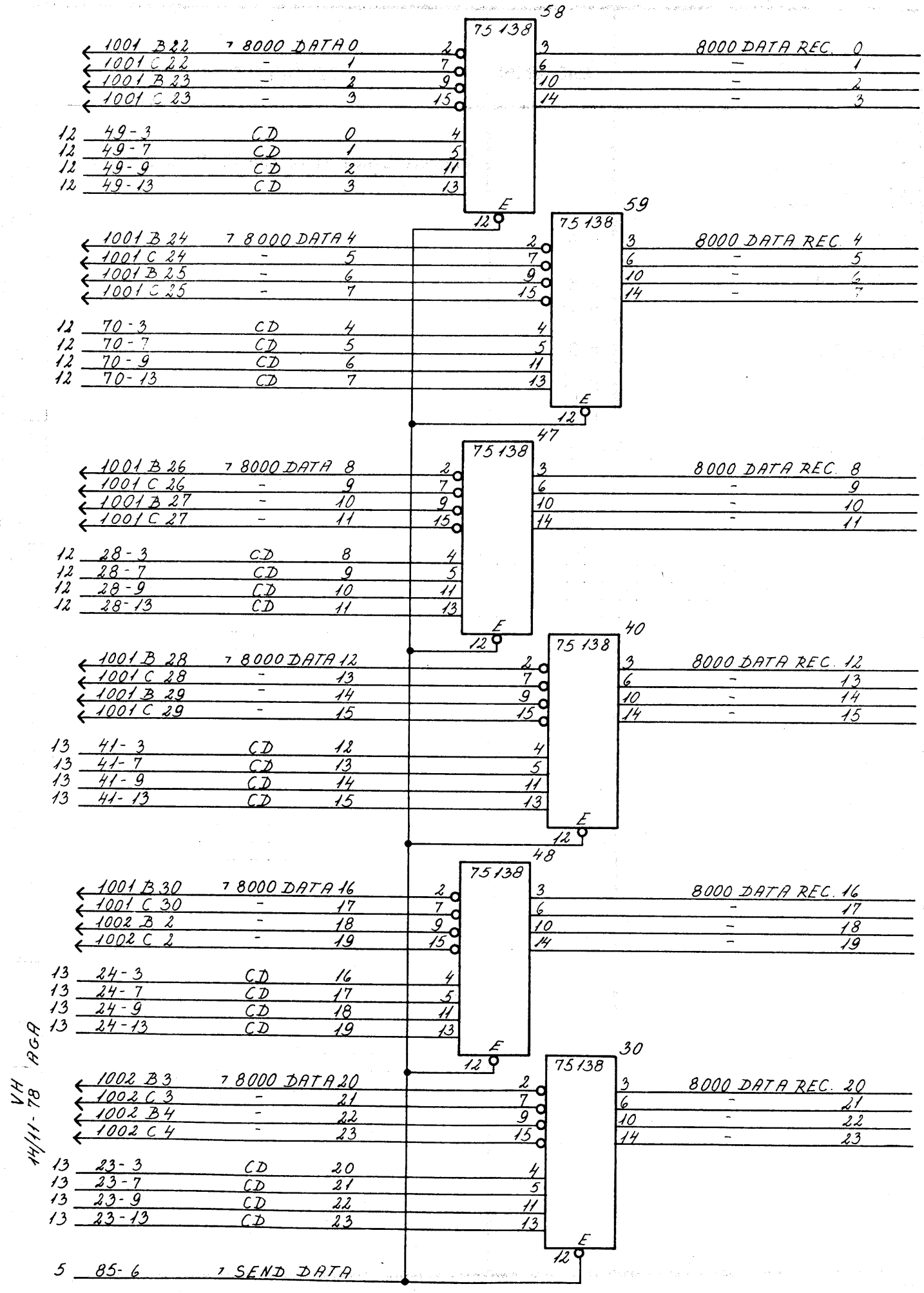
78.12.12.VH	78.12.12.KISH	78.12.21.VH



MEM 805

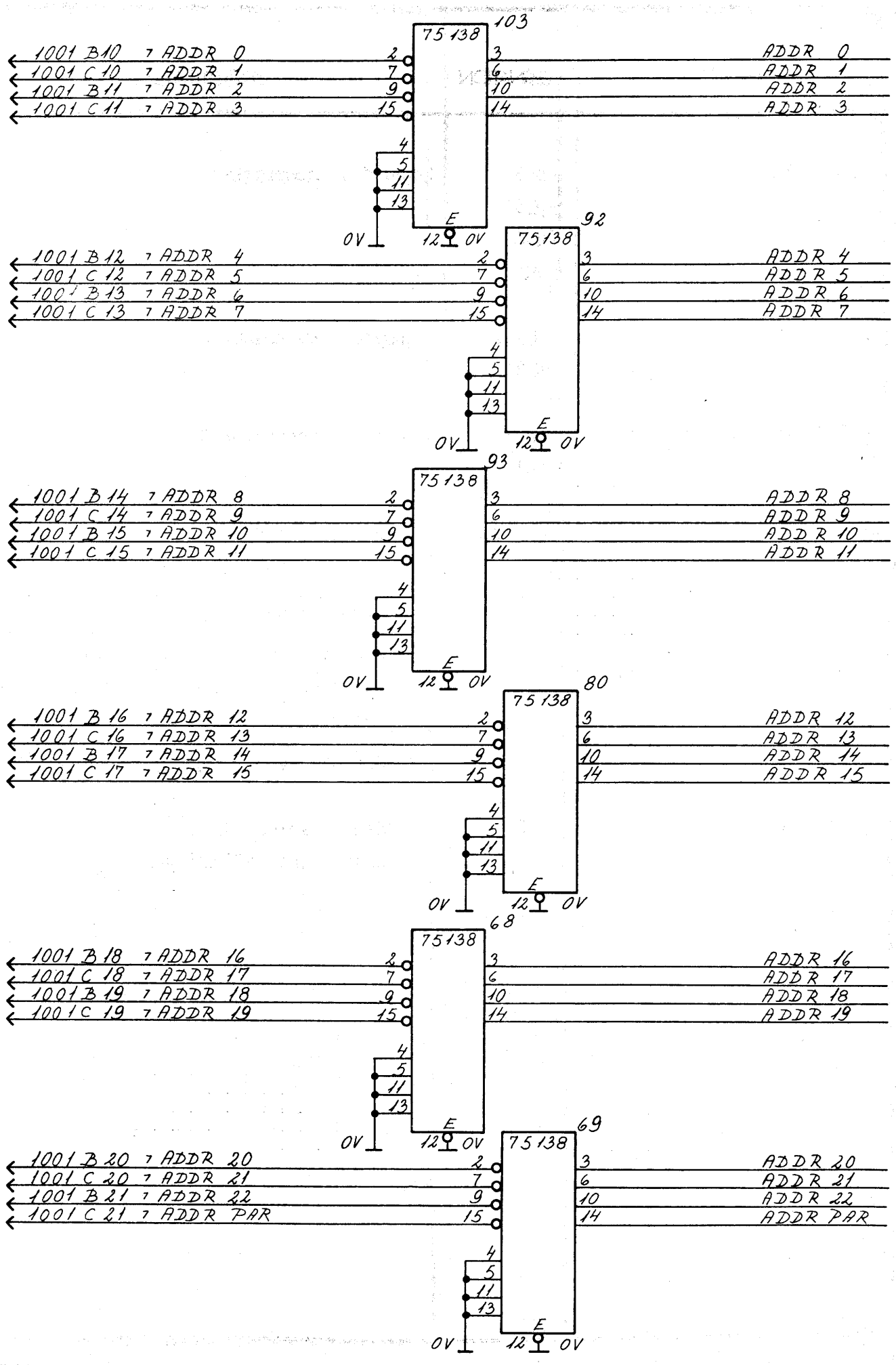
8000 DATA TRANSCEIVERS

1.

A13592

SIGNAL	DESTINATION	DESCRIPTION
ADDR 0:23 and ADDR PAR		Address Lines from the RC 8000 system bus
ADDR 0:4	p 3	
ADDR 5:6	p 3 p 15	
ADDR 7:8	p 3 p 15 p 17	
ADDR 9:22	p 3 p 17	
ADDR PAR.	p 3	

Designed by	Drawn by	Dwg. Office Check
78.12.12.VH	78.12.12.KISH	78.12.21.VH



VH 14/11-78 AGA

MEM805

8000 ADDRESS RECEIVER

2

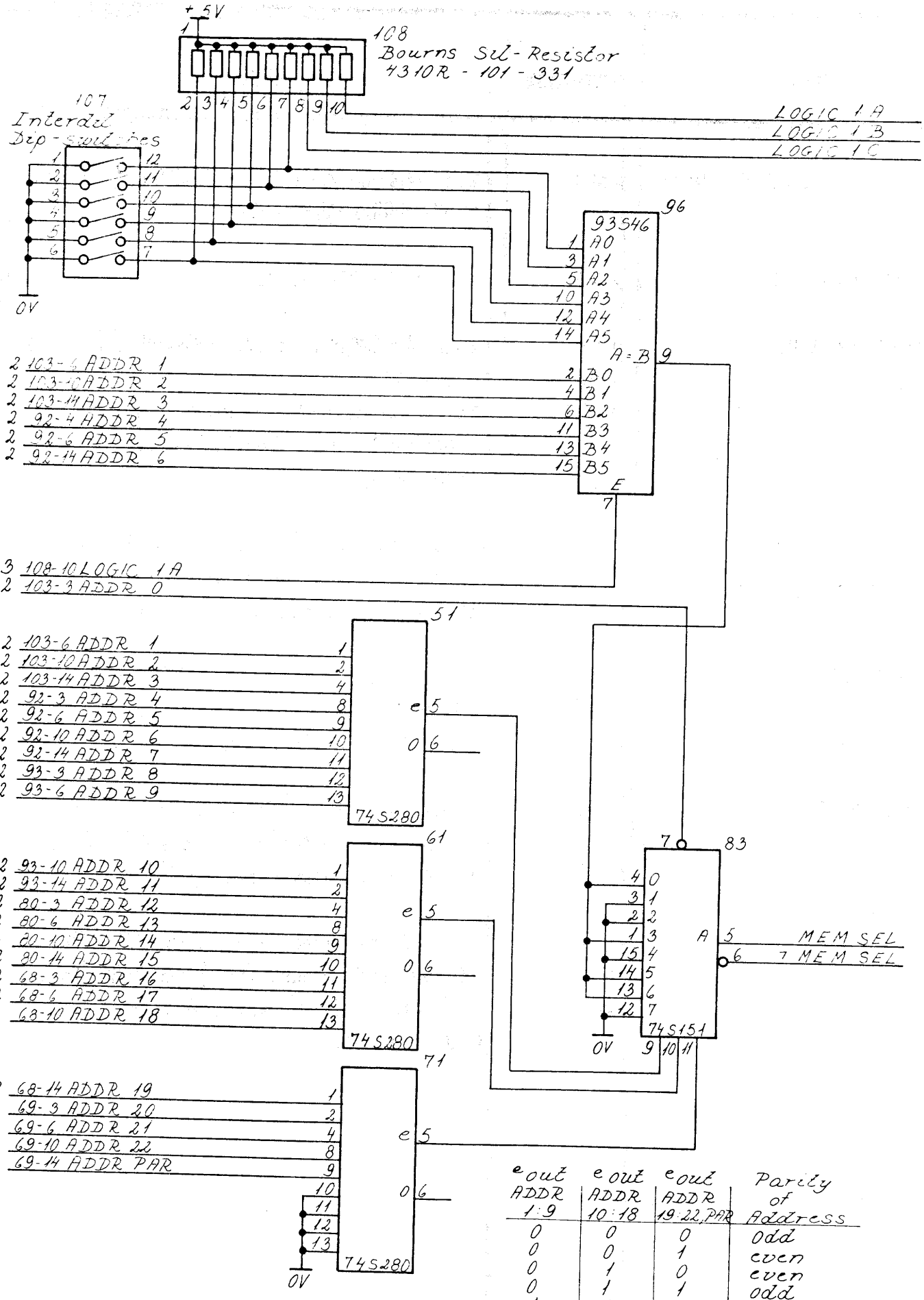
A13593

SIGNAL	DESTINATION	DESCRIPTION
LOGIC 1A	p 3 p 5 p 8 p 10	Logic 1 generator A
LOGIC 1B	p 12 p 13	Logic 1 generator B
LOGIC 1C	p 11 p 14	Logic 1 generator C
MEM SEL	NOT USED	Memory selected. This signal is high if: 1) ADDR 0 equals logical 0 2) ADDR 1:6 equals the same value as selected by the memory modul selector 3) Odd parity of ADDR 0:22 and ADDR PAR.
-, MEM SEL	p 5	-, Memory selected. Inverse signal of MEM SEL

Designed by 78.12.12.VH

Drawn by 78.12.12.KISH

Design Office Check 78.12.21.VH



e out ADDR 1:9	e out ADDR 10:18	e out ADDR 19:22, PAR	Parity of Address
0	0	0	odd
0	0	1	even
0	1	0	even
0	1	1	odd
1	0	0	even
1	0	1	odd
1	1	0	odd
1	1	1	even

MEM805

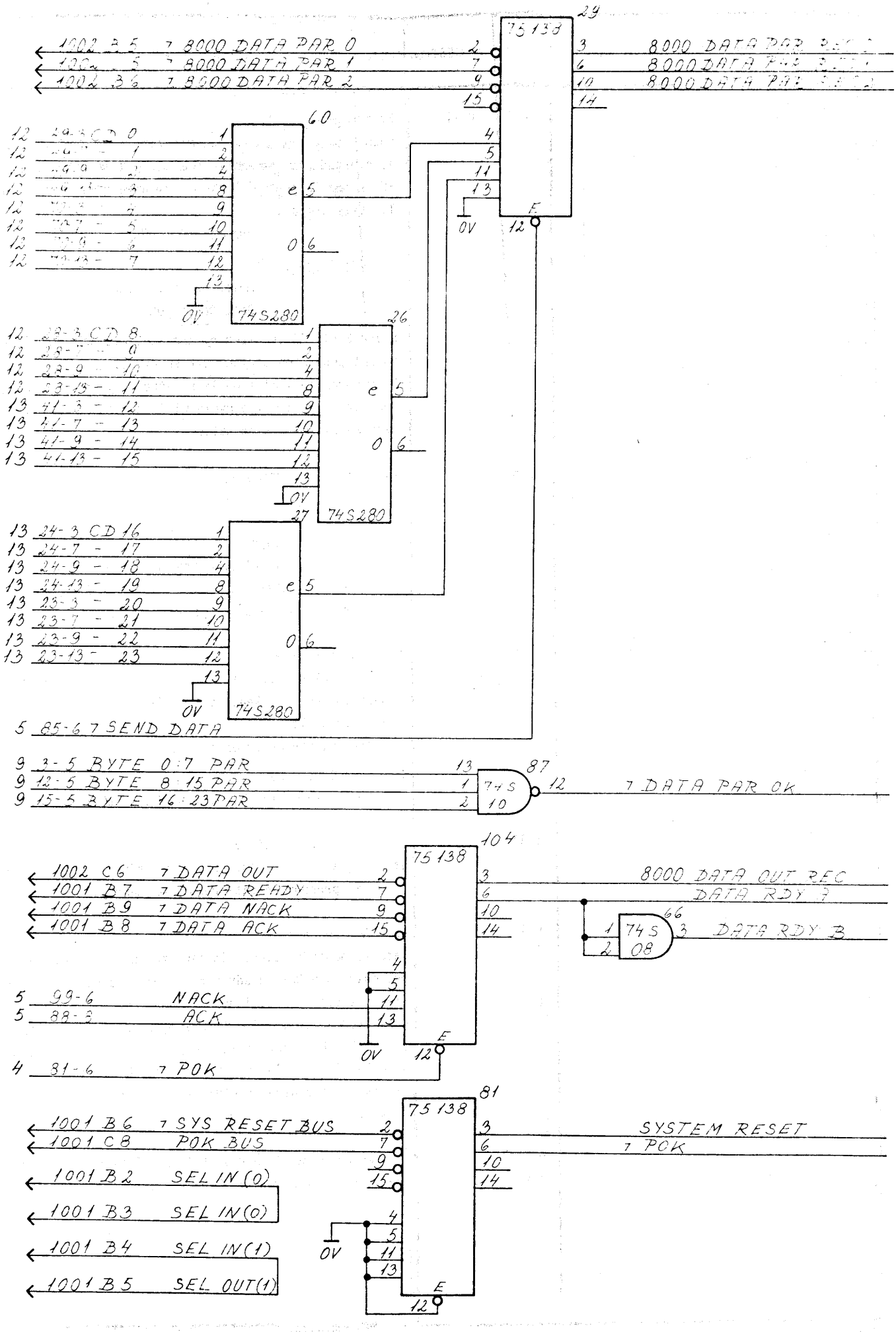
A13594

MEMORY ADDRESS DECODER

SIGNAL	DESTINATION	DESCRIPTION
8000 DATA PAR. REC. 0:2	p 8	Data bus parity bits 0:2 as received from the RC 8000 system bus
-, DATA PAR. OK	p 5	-, Data bus parity ok
8000 DATA OUT REC.	p 6 p 8 p 15	Data out signal received from the RC 8000 system bus. Data out when high, indicates that the operation is an output operation (write into memory)
DATA RDY.A	p 5	Data ready control signal from the RC 8000 system bus. Data ready is high, when the bus master requests a memory cycle
DATA RDY.B	p 5 p 11	Data ready control signal from the RC 8000 system bus. Data ready is high, when the bus master requests a memory cycle
SYSTEM RESET	P 15	This signal is a general reset signal from the RC 8000 system bus. The signal resets the error display status (p 11)
-, POK	p 4 p 14 p 15	-, Power ok signal as received from the RC 8000 system bus. The signal when low, indicates that all voltages have reached proper- levels

Designed by	Drawn by	Dwg. Office Check
78.12.12.VH	78.12.12.KISH	78.12.21.VH

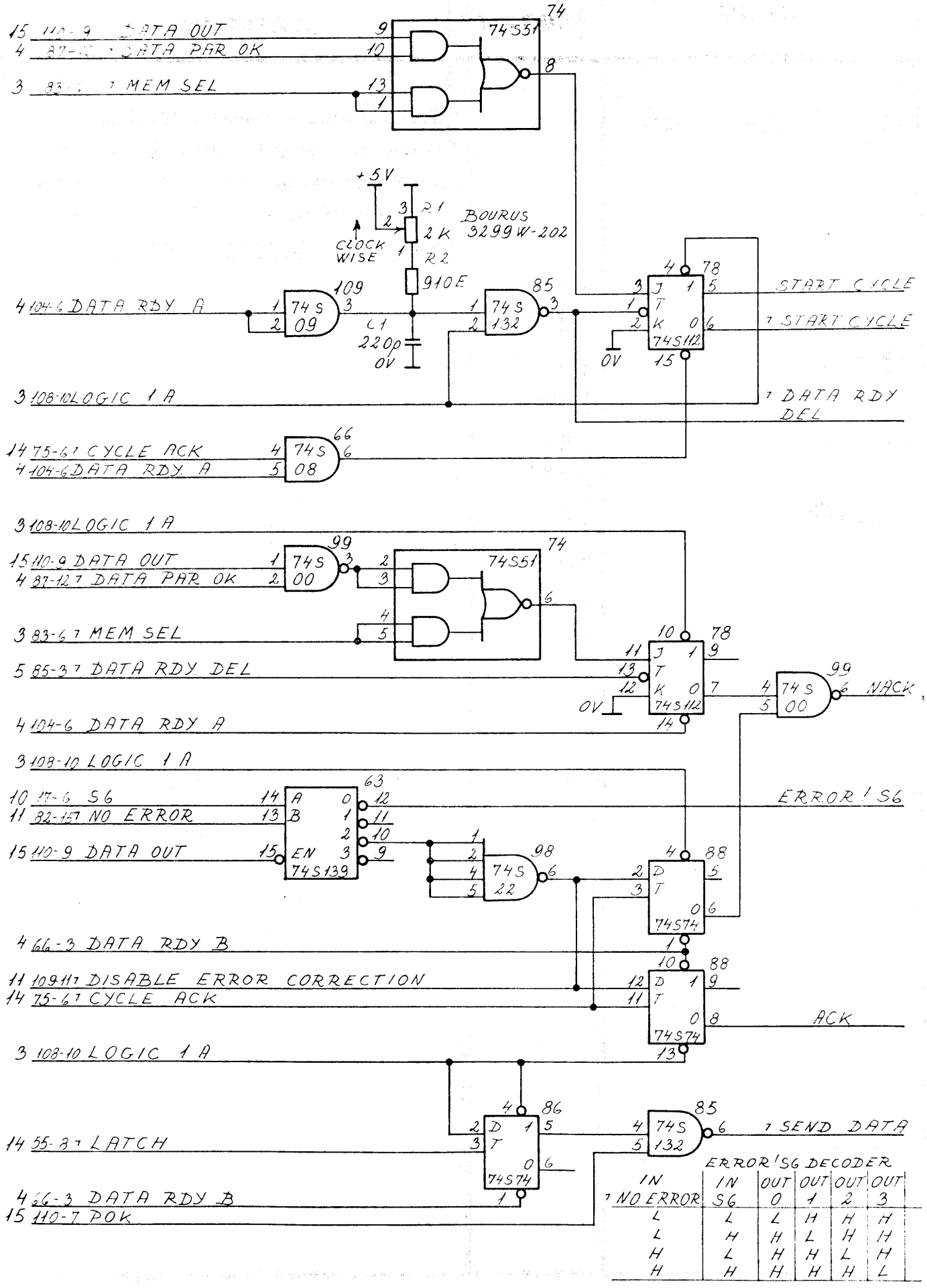
Unit	8000 DATA BUS PARITY CHECK/GENERATION AND CONTROL SIGNAL TRANSCEIVERS	
MEM 805		
Dwg. No. A 25555		



MEM 805
A13595

8000 DATA BUS PARITY CHECK/GENERATION and CONTROL SIGNAL TRANSCEIVERS

SIGNAL	DESTINATION	DESCRIPTION
START CYCLE	p 11	Start Memory Cycle. When a DATA RDY signal has arrived to the memory a delay is started. At the end of the delay time, the START CYCLE FF is set to logical 1 in the following two situations: 1. Read cycle if: Memory Selected 2. Write cycle if: Memory selected and Data Parity OK Start Cycle FF is reset by the -, Cycle Ack signal, which is not generated during refresh cycles. If the Start Cycle FF becomes logical 1 while a refresh cycle is in progress, the normal read/write cycle will be postponed until the refresh cycle is terminated.
-, START CYCLE	p 8	Inverted Start Memory Cycle.
-, DATA RDY.DEL.	p 5	-, Data Ready Delayed. The Data Ready signal from the bus master is delayed to compensate for skews, device address decoding, address parity check and data bus parity check.
NACK	p 4	Data Not Acknowledge. Data Not Acknowledge is sent to the bus master as a response to the Data Ready signal if: 1. Write Cycle and Data Parity error on the bus 2. Read Cycle and Double Error in the data read from memory.
ERROR!S6	p 11	Error or Syndrome bit 6. This signal becomes logical 1 if a single error or double error is present in data read from memory.
ACK	p 4	Data Acknowledge. Data Acknowledge signal is sent to the bus master as a response to a Data Ready signal when a successful read or write cycle is finished. Data Acknowledge is also generated in cycles in which single error corrections occur. If the error correction/detection circuits are disabled (correction switch off) the Data Acknowledge signal is generated regardless of whether an error occurs or not.
-, SEND.DATA	p 1 p 4	-, Send Data to RC 8000 system bus. This signal gates memory read data to the RC 8000 system bus.



ERROR 1S6 DECODER

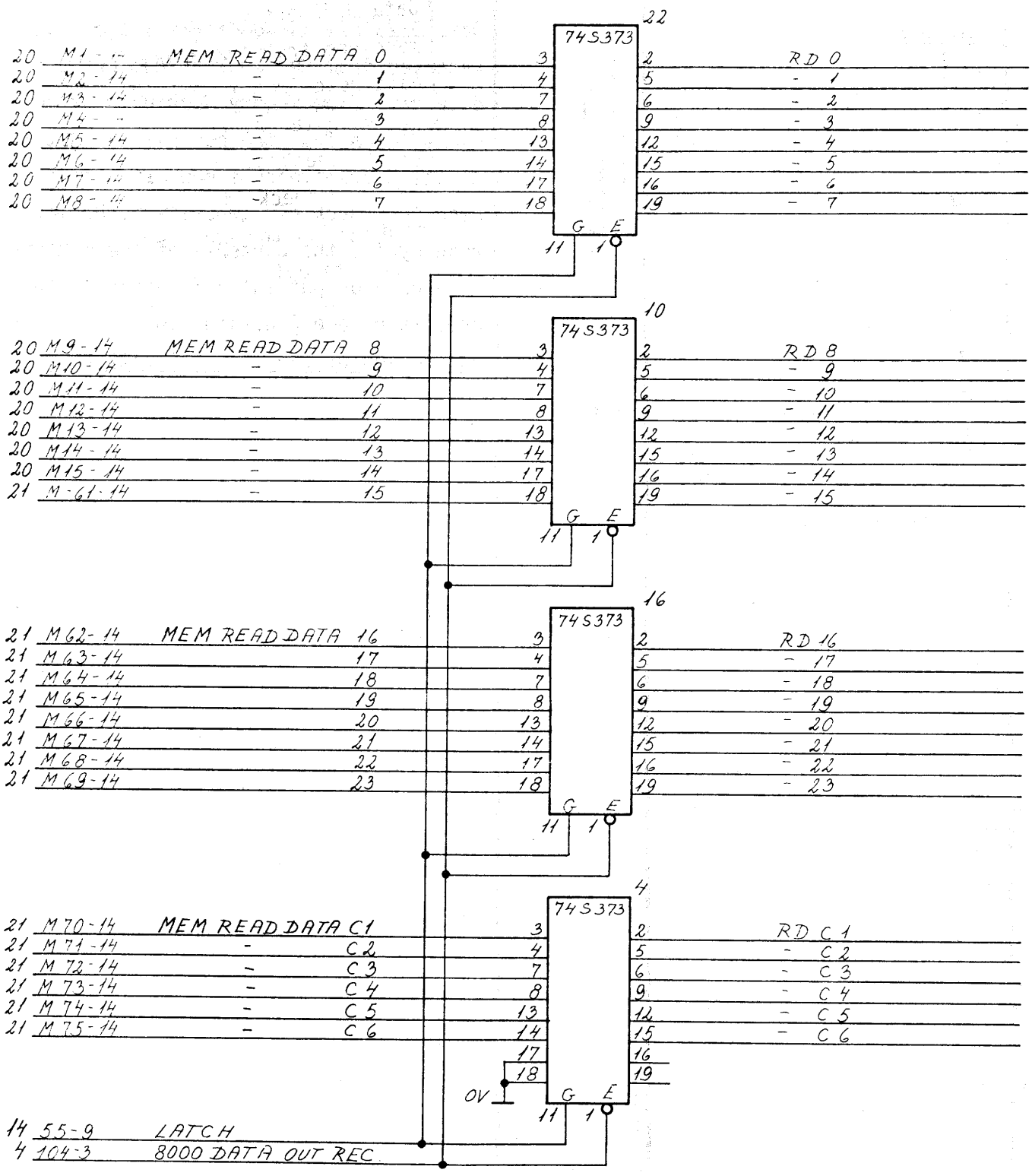
IN 1 NO ERROR	IN S6	OUT 0	OUT 1	OUT 2	OUT 3
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L

VH AGA 14/11-78

SIGNAL	DESTINATION	DESCRIPTION
RD 0:23, and RD C1:C6		Read Data 0:23 and Read Data C1:C6. The memory Read Data Output Latch holds data read from the memory. The register is loaded during a normal read cycle when memory data are available
RD 0:11	p 7 p 12	
RD 12:15	p 7 p 13	
RD 16:23	p 8 p 13	
RD C1:C5	p 8	
RD C6	p 10	

Designed by	Drawn by	Dwg. Office Check
78.12.12.VH	78.12.12.KISH	78.12.12.VH

Unit		
MEM 805	MEMORY READ DATA OUTPUT LATCH	p 6 of 23
Dwg. No. A 25556		



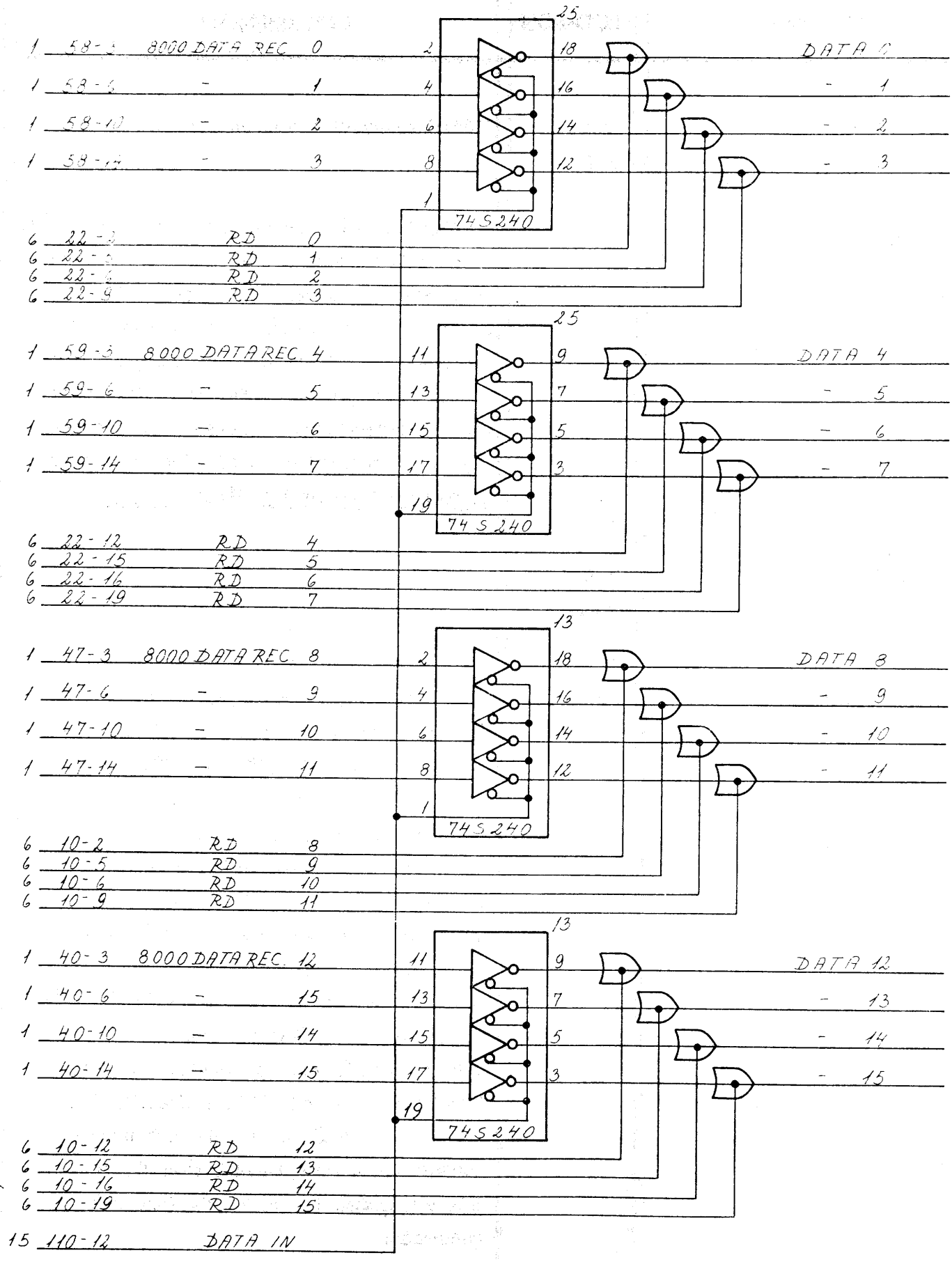
MEM805 MEMORY READ DATA OUTPUT LATCH 6

A13597

SIGNAL	DESTINATION	DESCRIPTION
DATA 0:23		Data 0:23 are wired-or results of data received from the 8000 system bus and data read from memory. During write cycles data from the bus will be gated to the check/syndrome generator to be used for check bit generation. During read cycles the contents of the memory read data output latch is gated to the check/syndrome generator to be used for generation of syndrome bit pattern.
DATA 0, 1, 4, 8	p 9	
Data 2, 3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15		

Designed by	Drawn by	Dw	ffice Check
78.12.12.VH	78.12.12.KISH	78.12.21.VH	

Unit		
MEM 805	DATA 0:15 TO CHECK/SYNDROME GENERATOR	p 7 of 23
Dwg. No. A 25557		



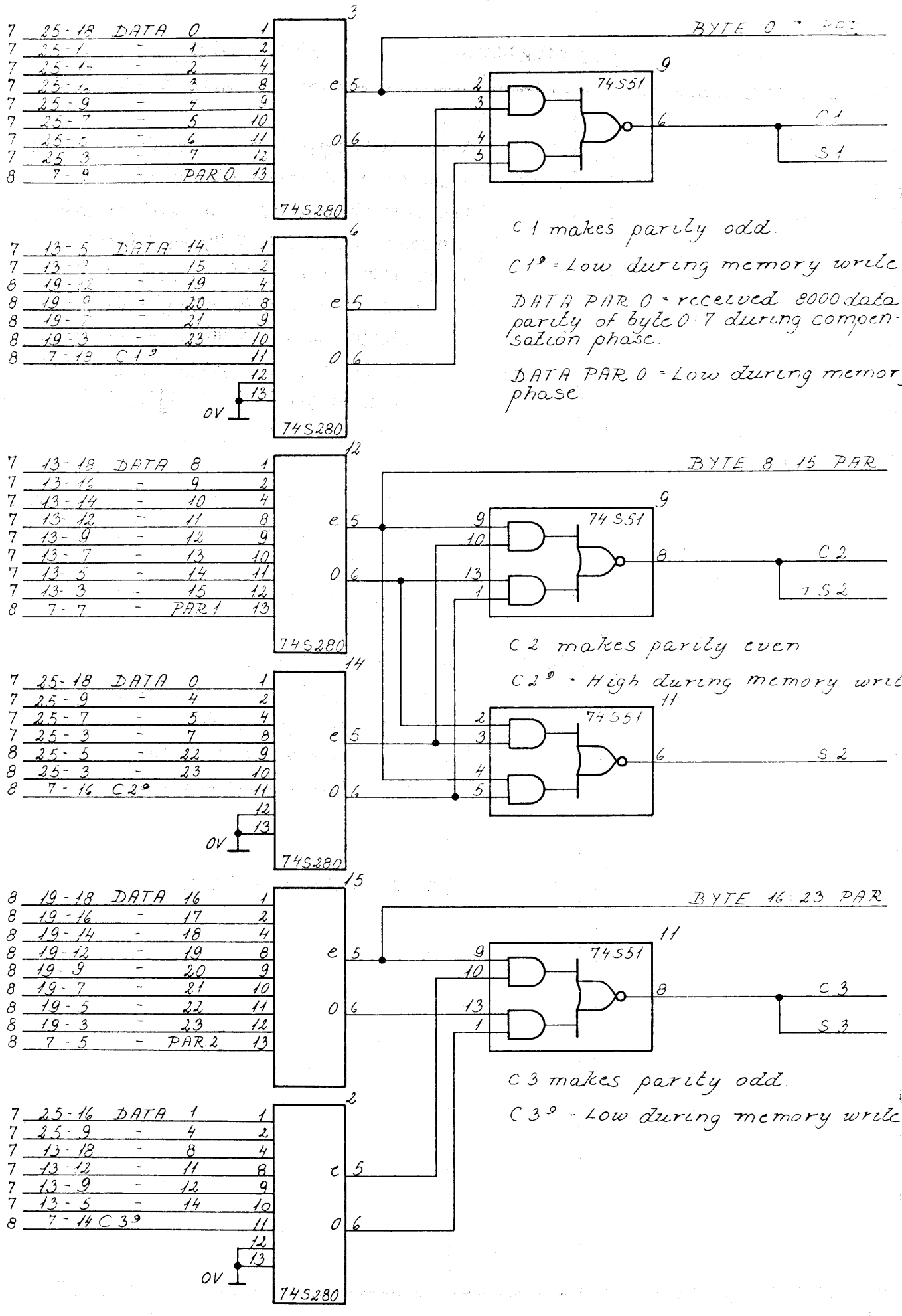
MEM 805

A13598

DATA 0-15 to CHECK / SYNDROME GENERATOR

SIGNAL	DESTINATION	DESCRIPTION
DATA 16:23	p 9 p 10	Refer to description on page 7.
C1':C5'		C1':C5' are wired-or results of logical 1/ logical 0 generators and check bits read from memory. During write cycles the I/O generators are gated to the check/syndrome generator to be used for check bit generation. During read cycles the check bits read from memory are gated to the check/ syndrome generator to be used for generation of syndrome bit pattern.
C1':C3'	p 9 p 10	
C4':C5'	p 10	
DATA PAR 0:2	p 9	DATA PARITY 0:2 are wired-or results of logical 1 generators and the bus parity lines received from the RC 8000 system bus. During write cycles the bus parity bits are gated to the check/syndrome generator. This generator is also used to check the bus parity. The generator produces three signals BYTE 0:7 PAR, BYTE 8:15 PAR, and BYTE 16:23 PAR. These signals are "anded" to the -, DATA PARITY OK signal. When the bus parity has been checked and if parity is ok, the memory timing is started. This causes logical 1's to be gated to the check/syndrome generator. During read cycles logical 1's are gated to the check/syndrome generator.

Designed by	Drawn by	Dwg. Office Check
78.12.12.VH	78.12.12.KISH	78.12.21.VH



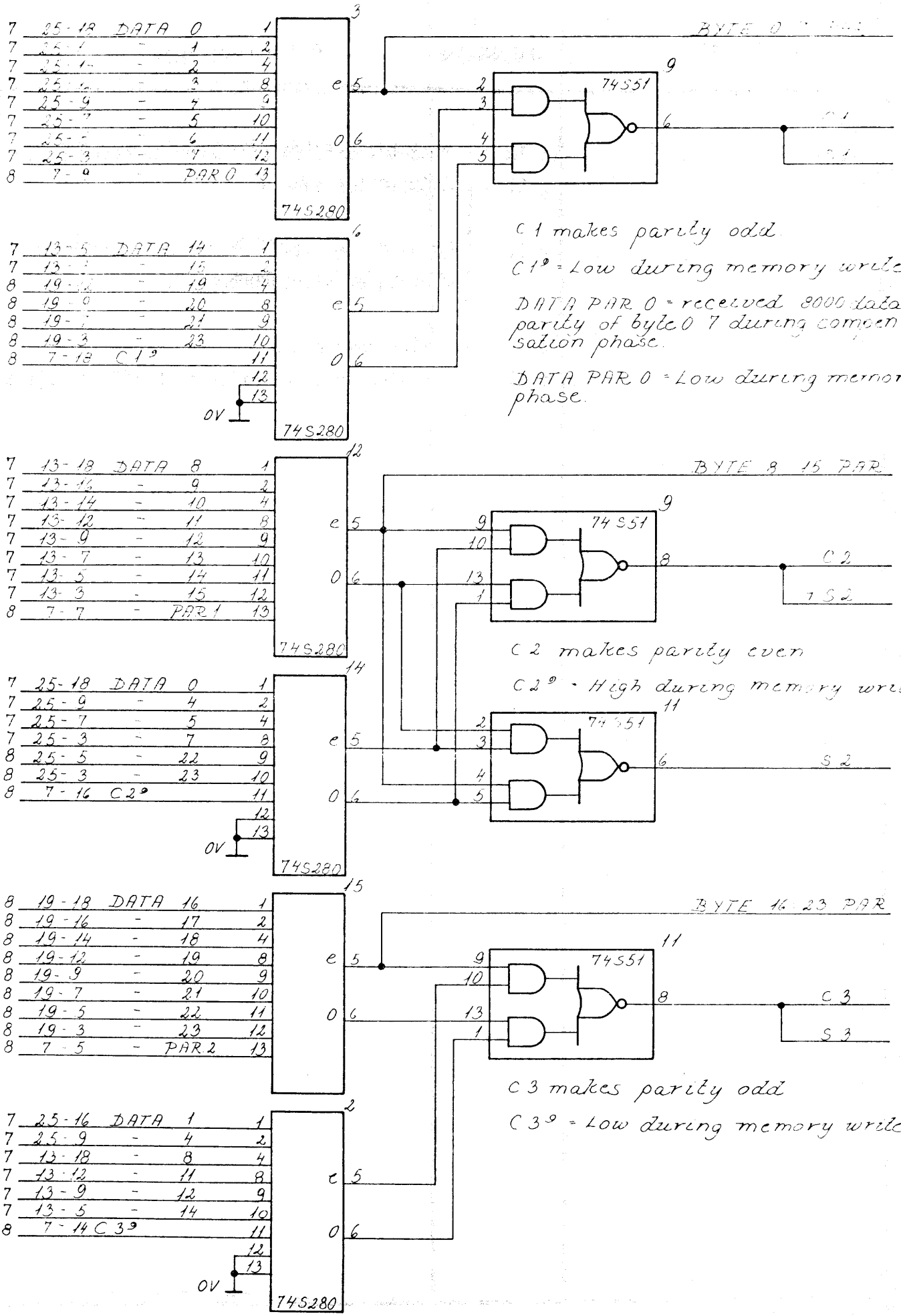
VH AGA
14/11-78

SIGNAL	DESTINATION	DESCRIPTION
BYTE 0:7 PAR, BYTE 8:15 PAR, and BYTE 16:23 PAR	p 4 p 10	At the beginning of write cycles, these signals are used to check the bus parity. Each signal is at high level if parity of the respective byte is ok (see also description of DATA PAR 0:2 on page 8). If parity is ok the memory timing is started and the BYTE PARITY signals are now used to generate check bit 6. In read cycles the BYTE PARITY signals are used to generate syndrome bit 6.
C1:C3	p 10	While data are written into memory, check/ syndrome generator generates check bits C1:C6, these check bits are stored alongside corresponding data bits in memory.
S1:S3	p 11	Syndrome bits 1:3. On reading data and check bits from memory, they generate the syndrome pattern (S1:S6), that correts any single bit error and detects double bit errors.
-, S2	p 11	Inverted syndrome bit 2.

Designed by 78.12.12.VH

Drawn by 78.12.12.KISH

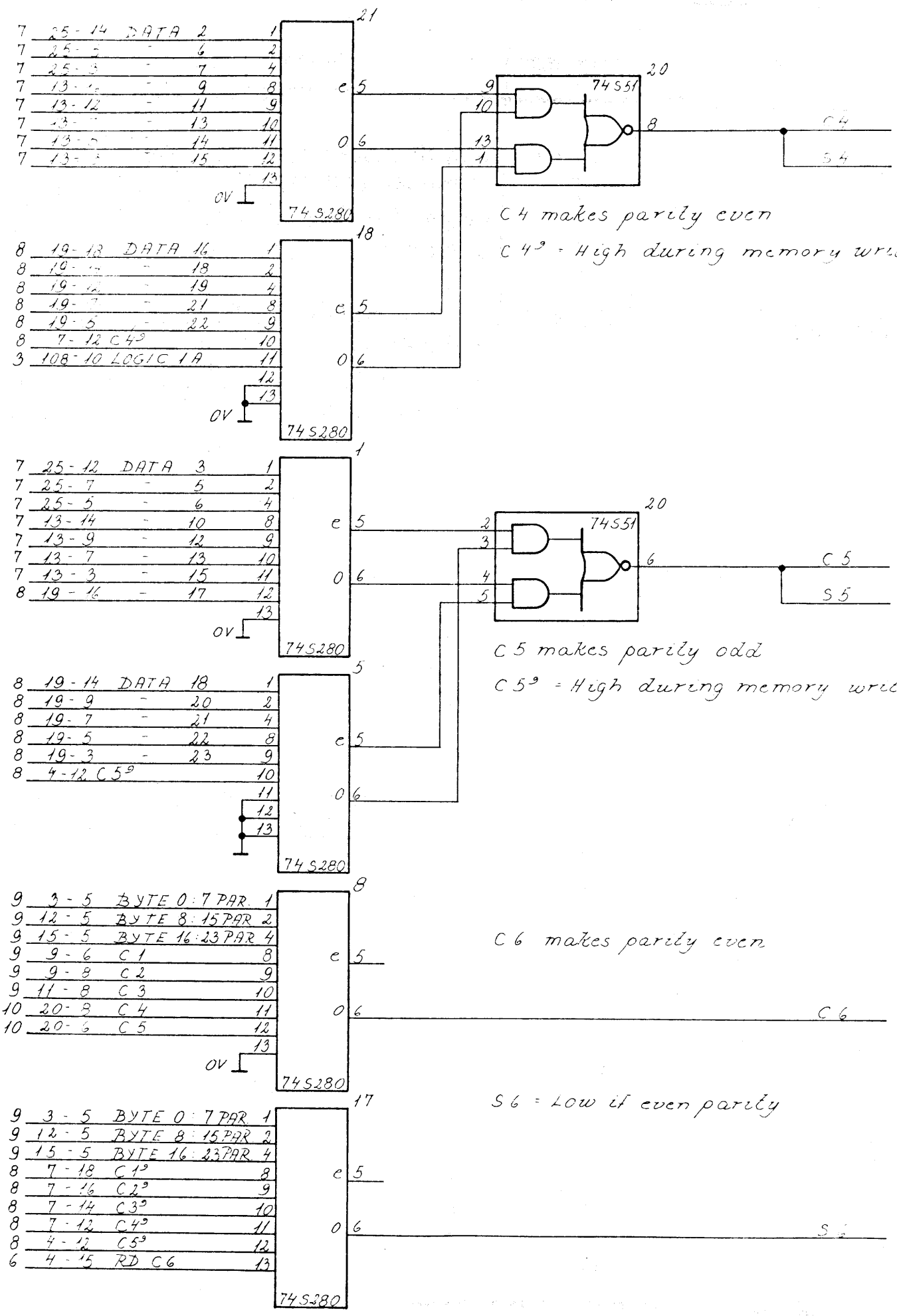
Dw... Office Check 78.12.21.VH



14/11-78 VH AGA

SIGNAL	DESTINATION	DESCRIPTION
C4:C6	p 10 p 21	Check bits C4:C6. Refer to description of C1:C3 on page 9.
S4, S5	p 11	Syndrome bits 4 and 5. Refer to description of S1:S3 on page 9.
S6	p 5 p 11	Syndrome bit 6. Refer to description of S1:S3 on page 9.

Designed by	Drawn by	Dwg. Office Check
78.12.12.VH	78.12.12.KISH	78.12.21.VH

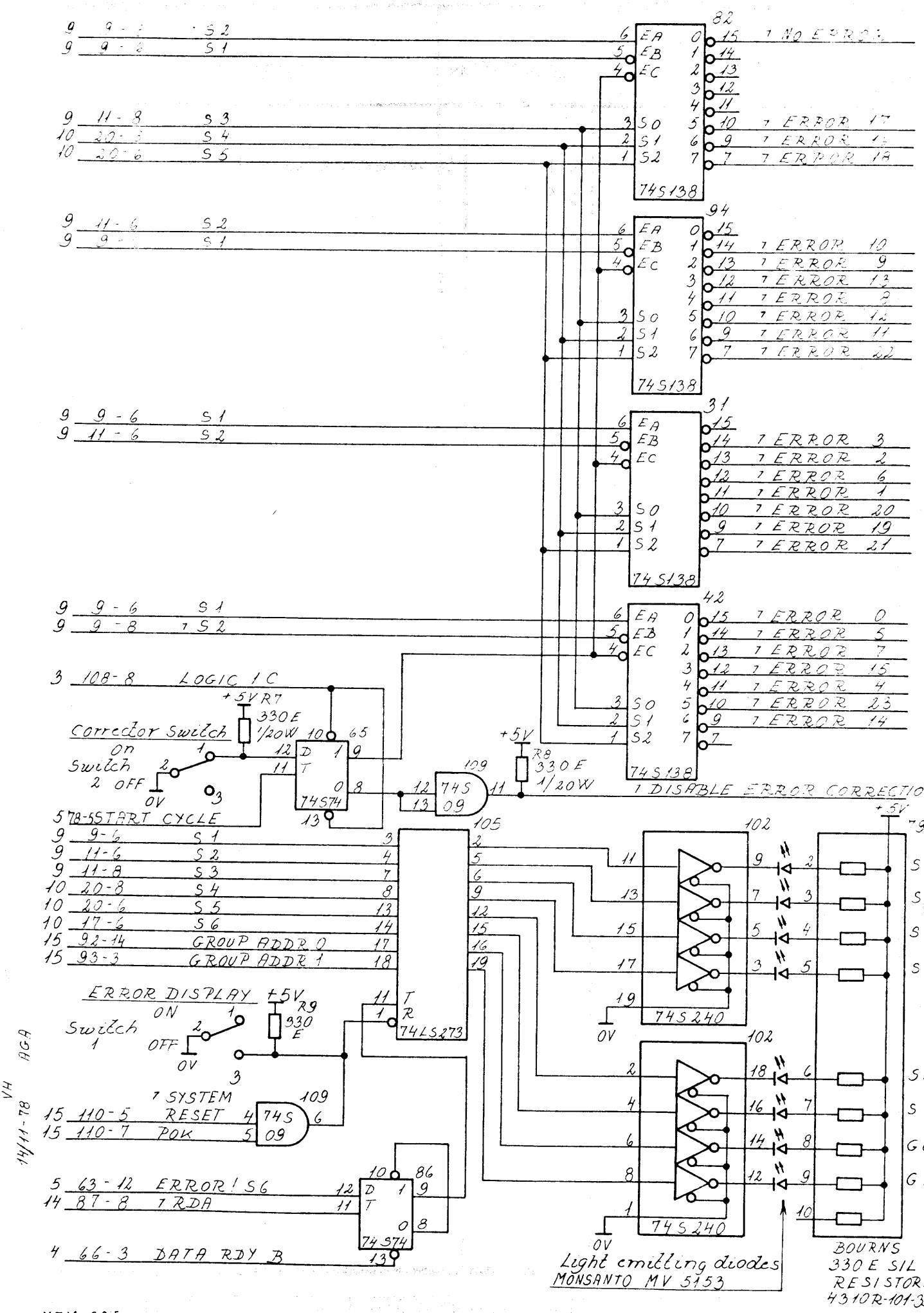


MEM 805
A13601

CHECK/SYNDROME GENERATOR
C4/S4 : C6/S6

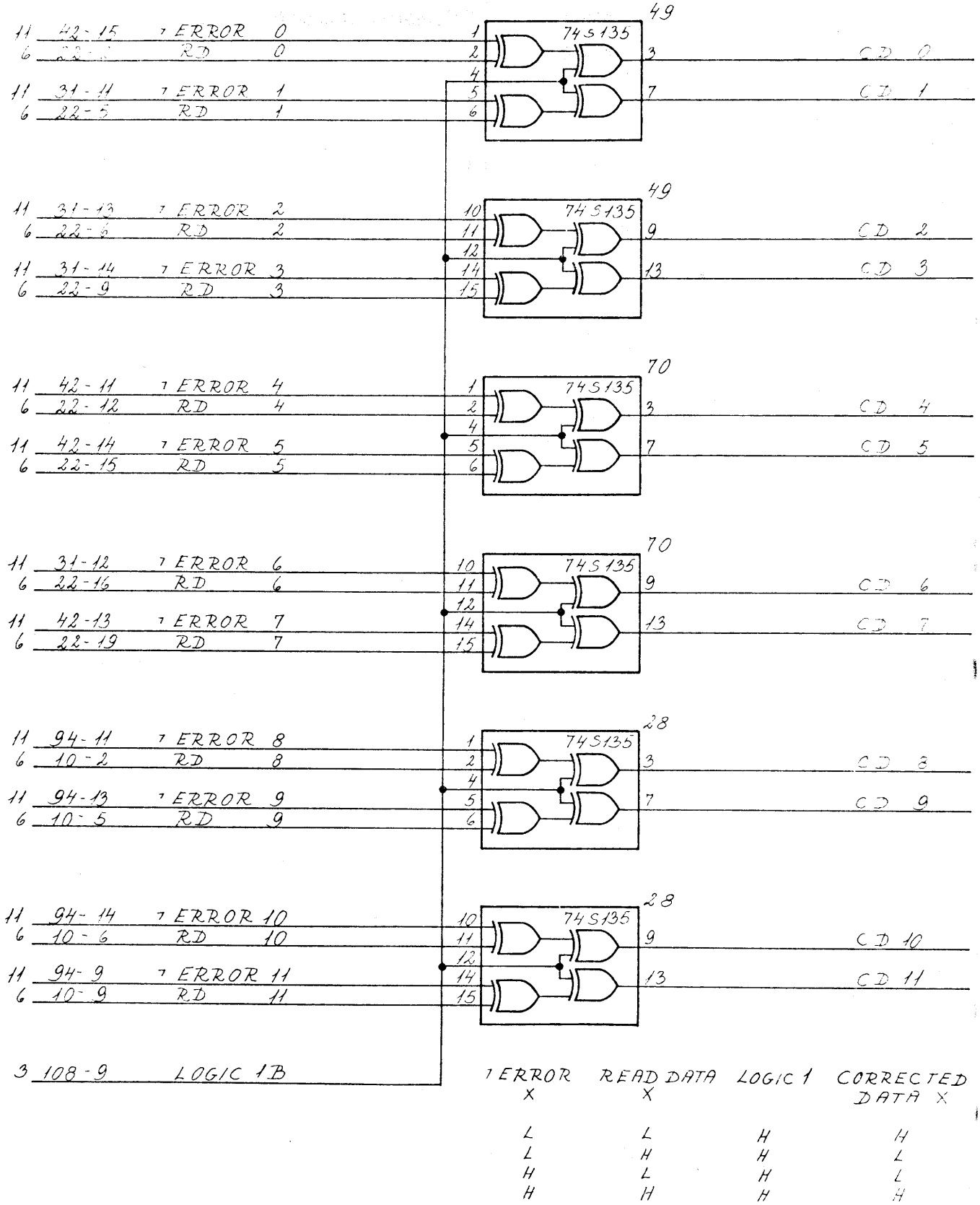
SIGNAL	DESTINATION	DESCRIPTION
-, ERROR	p 5	This signal is low when syndrome bits S1:S5 = 0, which indicate that no error was found in data 0:23 and check bits C1:C5 read from memory.
-, ERROR 0:11	p 12	The error signals are decoded syndrome bits (S1:S5). If one of the ERROR signals are low while S6=1 a single error has been detected. The error is corrected by inversion of the bit in error.
-, ERROR 12:23	p 13	Refer to description above.
-, DISABLE ERROR CORRECTION	p 5	This signal is low when the CORRECTOR switch is in OFF position, which disables the syndrome decoder. Also DATA ACK signal is sent to the bus master regardless of whether an error has been detected or not. NOTE! Error status are not correctly displayed when the CORRECTOR switch is in off position.

Designed by	Drawn by	D	Office Check
78.12.12.VH	78.12.12.KISH	78.12.21.VH	


82
94
31
42
74S138
74S574
74S09
74S240
74LS273
LOGIC 1 C
Corrector Switch
ON
OFF
START CYCLE
ERROR DISPLAY
SYSTEM RESET
POK
ERROR 1 S6
DATA RDY B
DISABLE ERROR CORRECTIO
NO ERROR
Light emitting diodes
MONSANTO MV 5153
BOURNS
330 E SIL
RESISTOR
4310R-101-3
MEM 805
SYNDROME DECODER and ERROR DISPLAY
A13602
11

SIGNAL	DESTINATION	DESCRIPTION
CD 0:11	p 1 p 4	Corrected data bits 0:11.

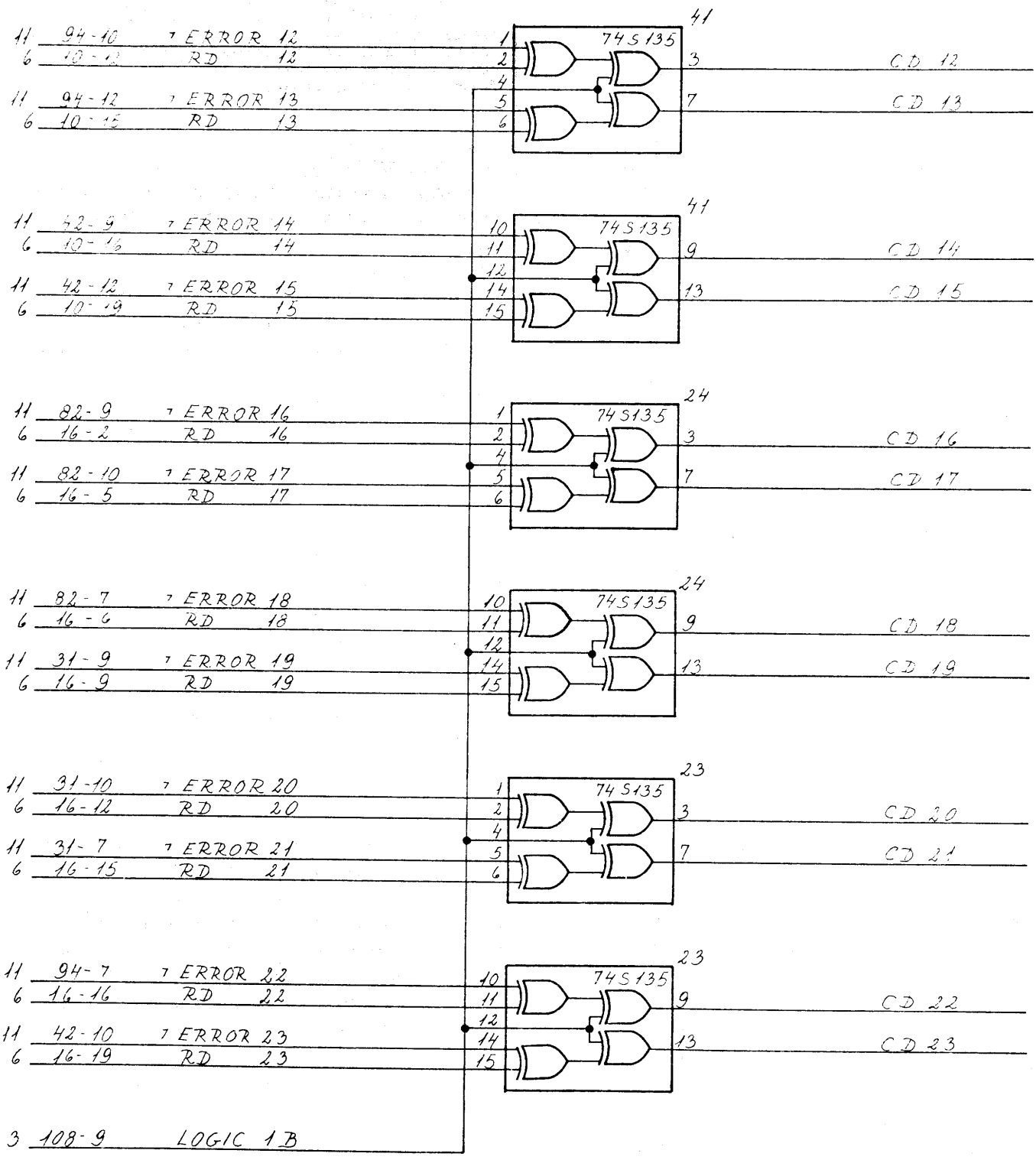
Designed by	Drawn by	Dwg. Office Check
78.12.12.VH	78.12.12.KISH	78.12.21.VH


49
74S135
11 42-15 ↑ ERROR 0
6 22- RD 0
11 31-11 ↑ ERROR 1
6 22-5 RD 1
CD 0
CD 1
49
74S135
11 31-13 ↑ ERROR 2
6 22-6 RD 2
11 31-14 ↑ ERROR 3
6 22-9 RD 3
CD 2
CD 3
70
74S135
11 42-11 ↑ ERROR 4
6 22-12 RD 4
11 42-14 ↑ ERROR 5
6 22-15 RD 5
CD 4
CD 5
70
74S135
11 31-12 ↑ ERROR 6
6 22-16 RD 6
11 42-13 ↑ ERROR 7
6 22-19 RD 7
CD 6
CD 7
28
74S135
11 94-11 ↑ ERROR 8
6 10-2 RD 8
11 94-13 ↑ ERROR 9
6 10-5 RD 9
CD 8
CD 9
28
74S135
11 94-14 ↑ ERROR 10
6 10-6 RD 10
11 94-9 ↑ ERROR 11
6 10-9 RD 11
CD 10
CD 11
3 108-9 LOGIC 1B
14/11-78 VH AGA
↑ ERROR X
READ DATA X
LOGIC 1
CORRECTED DATA X
L L H H
L H H L
H L H L
H H H H

SIGNAL	DESTINATION	DESCRIPTION
CD 12:23	p 1 p 4	Corrected data bits 12:23.

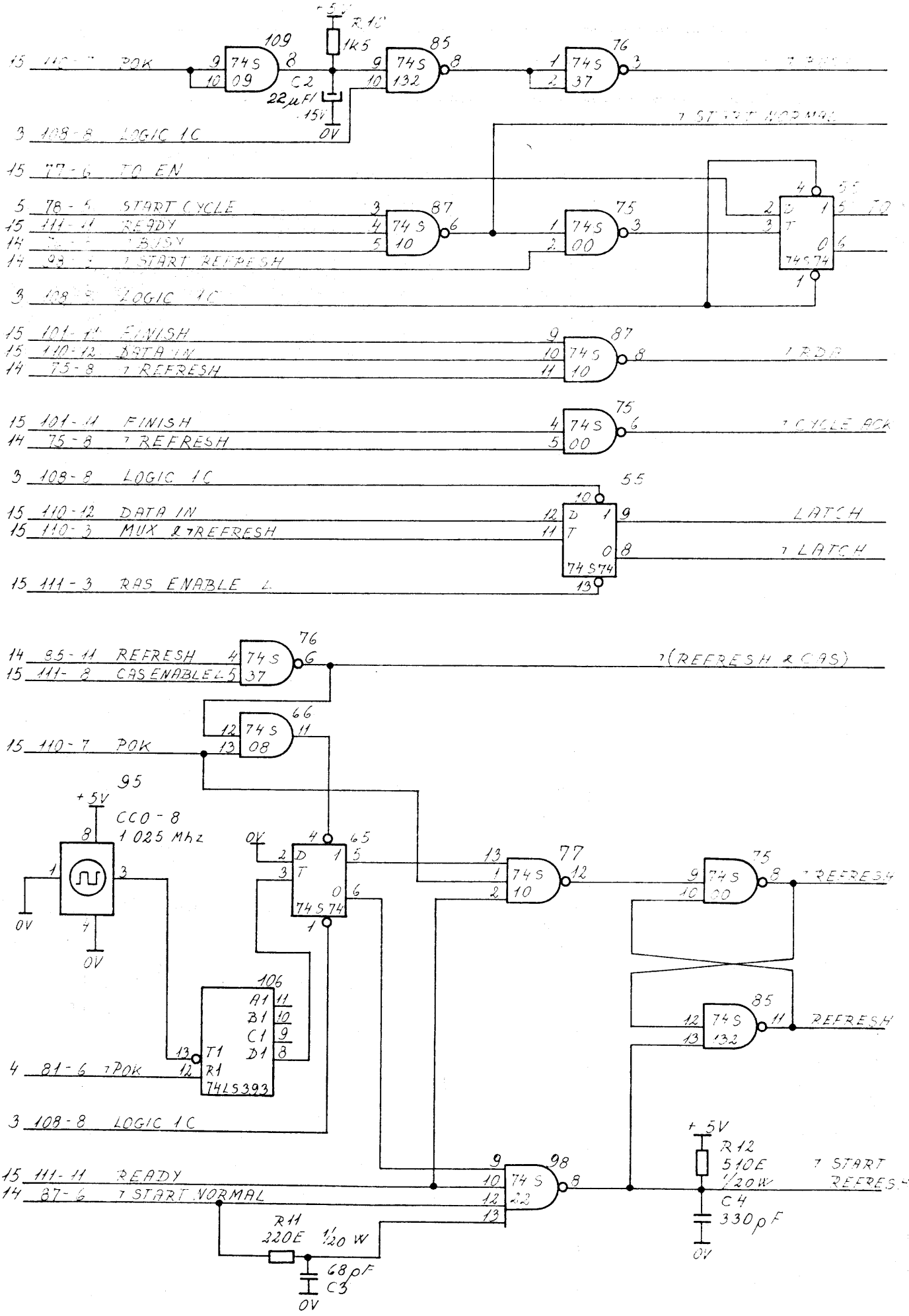
Designed by	Drawn by	Dwg. Office Check
78.12.12.VH	78.12.12.KISH	78.12.21.VH

Unit		
MEM 805	ERROR CORRECTOR BITS 12:23	p 13 of 23
Dwg. No. A 25563		

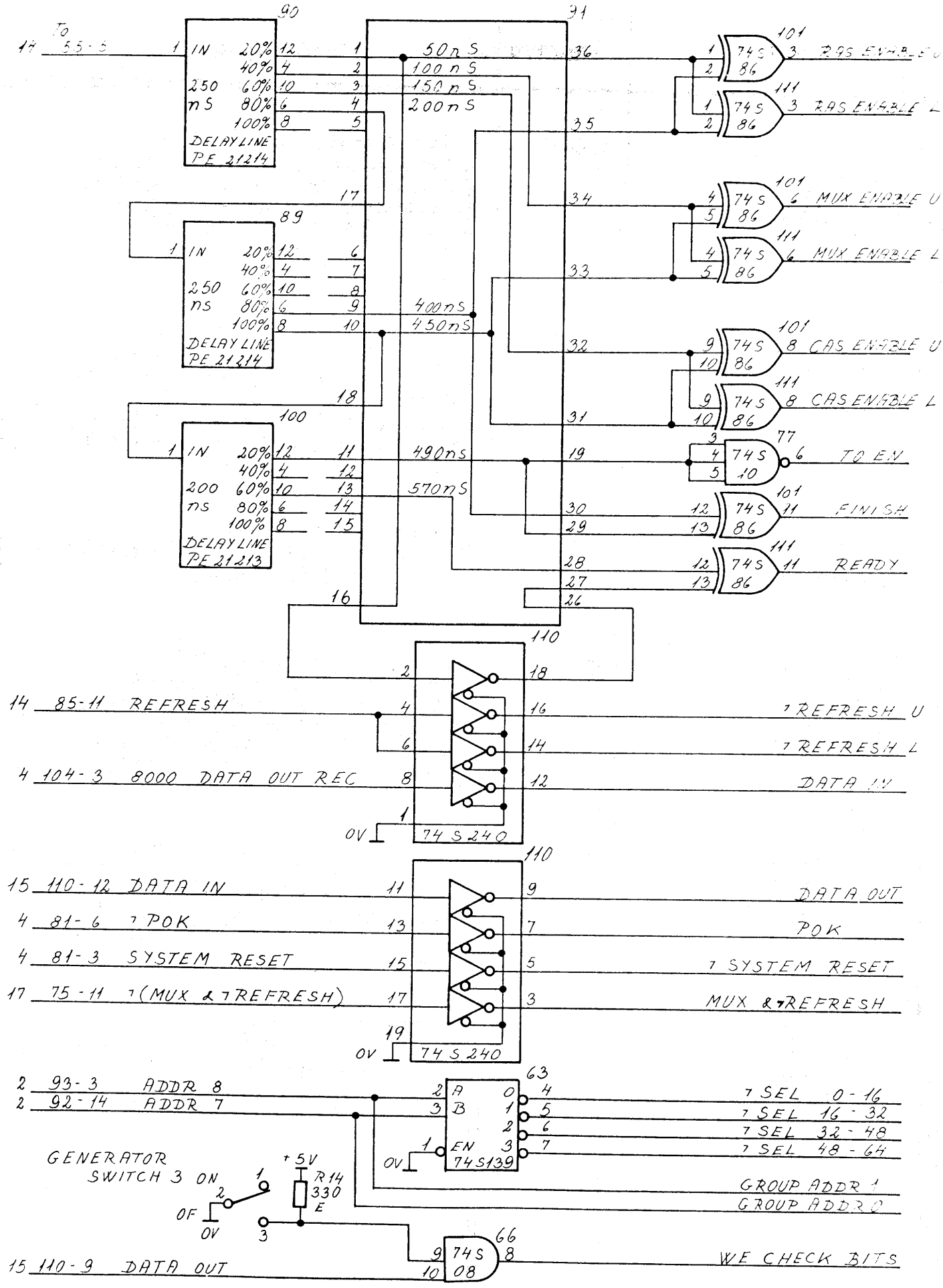


V4 AGA
14/11-78

SIGNAL	DESTINATION	DESCRIPTION
-, BUSY	p 14	This signal when low indicates that power is not ok. The signal will remain low for approx. 600 µS after POK has changed to logical 1. During this time only refresh cycles can be initiated. Several cycles are required after power-up before proper memory chip operation is achieved. Refresh cycles are adequate for this purpose.
-, START NORMAL	p 14	-, Start Normal Cycle. If a memory cycle is not in progress, this signal is generated when the bus master wants access to the memory.
TO	p 15	Time 0. When a memory cycle is started this FF is triggered. The 74S74 FF is used as a divide by two circuits so only one transition edge will pass down the delay line on page 15.
-, RDA	p 11	-, Read Data Available. The trailing edge of this signal upaates the Error Status register.
-, CYCLE ACK	p 5 p 11	-, Cycle Acknowledge signal. When this signal is generated the Start Memory Cycle FF is reset. The trailing edge of the signal sets the Double Error FF if a double error is detected in the data read from memory. In case of no error during read and no bus parity error during write, the Ack FF is set.
LATCH	p 6	This signal latches memory read data into the Memory Read Data output latch. Data are hold there until next normal read cycle.
-, LATCH	p 5	Inverted Latch signal.
-, (REFRESH & CAS)	p 17	This signal resets the refresh request FF and increments the refresh counter by one.
-, REFRESH	p 14 p 17	This signal is low when a refresh cycle is in progress. The memory is refreshed in the Ras only mode, which refresh the row of storage cells (1 of 128 rows) addressed by A0 to A6. 128 cycles are required each 2 msec. to refresh the stored data.
REFRESH	p 14 p 15	This signal is high when a refresh cycle is in progress.
-, START REFRESH	p 14	-, Start Refresh Cycle. If a memory cycle is not in progress, this signal is generated when a refresh cycle is required.


R10
1K5
C2
22µF/15V
109
74S 09
85
74S 132
76
74S 37
3 108-8 LOGIC 1C
15 77-6 TO EN
5 78-5 START CYCLE
15 111-11 READY
14 87-6 ↑START NORMAL
14 99-2 ↑START REFRESH
87
74S 10
75
74S 00
74S 74
15 101-11 FINISH
15 110-12 DATA IN
14 75-8 ↑REFRESH
↑RDA
↑CYCLE ACK
55
LATCH
↑LATCH
15 111-3 RAS ENABLE L
14 95-11 REFRESH
15 111-8 CASENABLE L
↑(REFRESH & CAS)
66
74S 08
15 110-7 POK
95
+5V
CCO-8
1.025 MHz
0V
65
77
↑REFRESH
106
74LS393
4 81-6 ↑POK
3 108-8 LOGIC 1C
98
74S 22
15 111-11 READY
14 87-6 ↑START NORMAL
R11
220E 1/20 W
68pF
C3
R12
510E 1/20W
C4
330pF
↑START REFRESH
14/11-78 VH AGA
MEM 805
MEMORY CONTROL LOGIC
14
A13605

SIGNAL	DESTINATION	DESCRIPTION
RAS ENABLE U/L	p 16	Row Address Strobe Enable. These signals enables the Row Address Strobes to the memory array.
MUX ENABLE U	p 16	Multiplex Enable Upper. This signal enables the Write Enable signal to bits 0:14 of the memory array.
MUX ENABLE L	p 16 p 17 p 21	Multiplex Enable Lower. This signal enables the Write Enable signal to bits 15:23 and check bits C1:C6 of the memory array. Also this signal multiplexes ADDR 9:22 to 2 x 7 output addresses, which are used as row and column address. The row address (ADDR 16:22) is gated to the memory array when MUX Enable L and Refresh are both logical 0. The column address (ADDR 9:15) is gated to the memory array when MUX Enable L is logical 1 and Refresh is logical 0.
CAS ENABLE U	p 16	Column Address Strobe Enable upper. This signal enables the Column Address Strobe to bits 0:14 of the memory array.
CAS ENABLE L	p 14 p 16	Column Address Strobe Enable lower. This signal enables the Column Address Strobe to bits 15:23 and check bits C1:C6 of the memory array. During refresh cycles this signal resets the refresh request FF, and increments the refresh counter.
TO EN	p 14	Time 0 Enable. Enable signal to Time 0 FF.
FINISH	p 14	This signal is generated by the timing generator at the end of the cycle. The signal enables the -, Read Data Available signal and the -, Cycle Ack signal.
READY	p 14	This signal when logical 0 indicates that a memory cycle (refresh or normal cycle) is in progress.
-, REFRESH U/L	p 16	During refresh cycles these signals disables Column Address Strobe and enables all of the Row Address Strobes to the memory array.
DATA IN	p 7 p 8 p 14 p 15	Data In signal when high, indicates that the present bus cycle is an input operation (read from memory).
DATA OUT	p 5 p 15 p 16	Data Out signal when high, indicates that the present bus cycle is an output operation (write into memory).
POK	p 5 p 11 p 14	Power OK signal, which indicates that all dc-voltages have reached proper levels.
-, SYSTEM RESET	p 11	This signal is a general reset signal from the RC 8000 system bus, when low the signal resets the error display.
MUX & -, REFRESH	p 14	The leading edge of this signal sets the Latch FF during read cycles.
-, SEL. 0-16 -, SEL. 16-32 -, SEL. 32-48 -, SEL. 48-64	p 16	These signals enables the Row Address strobe to the respective memory array groups.
GROUP ADDR 0:1	p 11	Group Address 0 and 1 are equal to Address 7 and 8 from the bus. In case of errors these address bits are displayed to identify the memory chip group in error.
WE CHECK BITS	p 21	Write Enable signal to check bit memory.



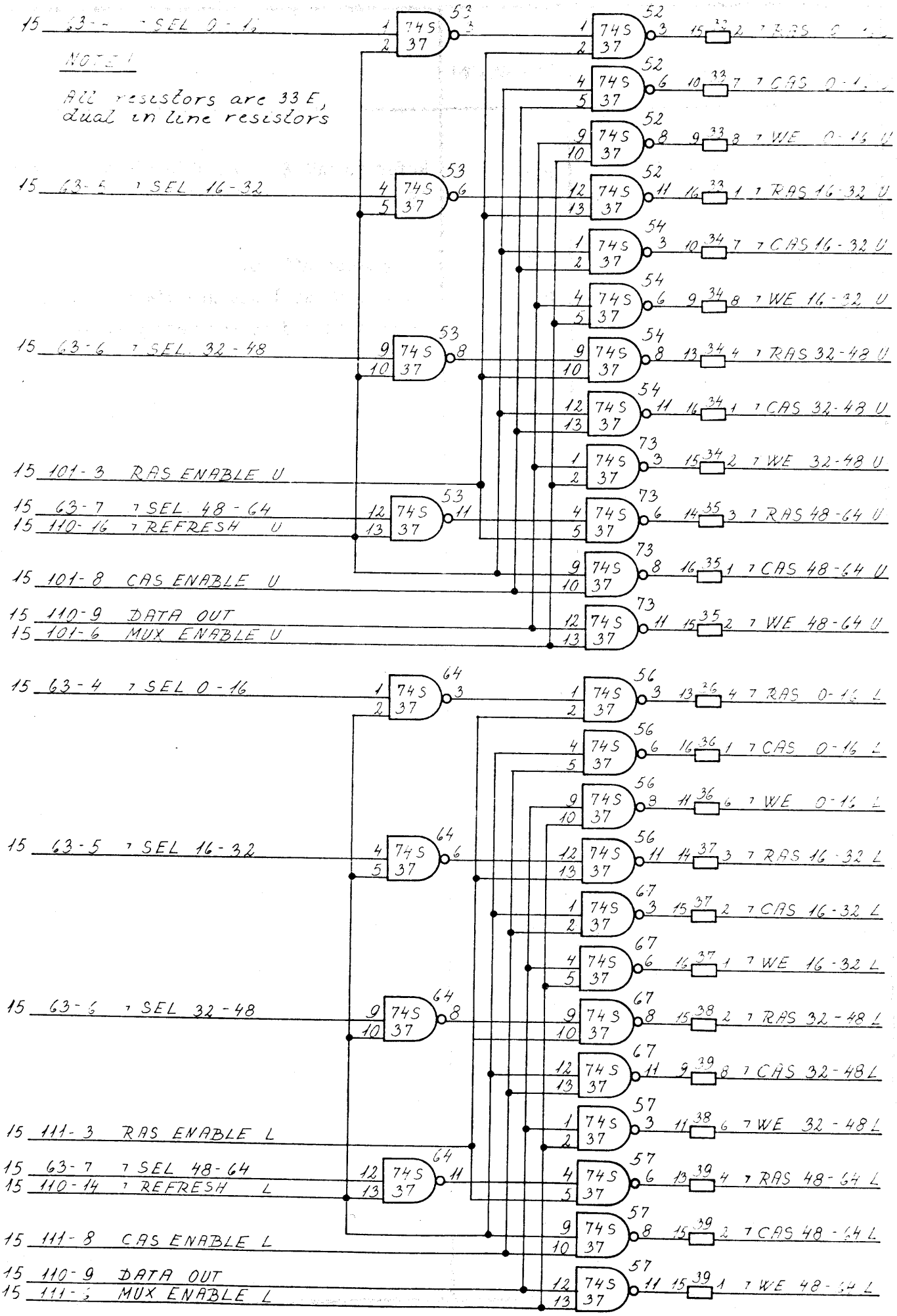
VH 14/11-78 AGA

SIGNAL	DESTINATION	DESCRIPTION
-, RAS 0-16 U -, RAS 16-32 U -, RAS 32-48 U -, RAS 48-64 U	p 20	-, Row Address Strobe Upper. Row Address Strobes to the upper part (bits 0:14) of the memory array. The Row Address Strobes latches the row address (ADDR 16:22) into a 7-bits latch, which i located internally in the memory chips.
-, CAS 0-16 U -, CAS 16-32 U -, CAS 32-48 U -, CAS 48-64 U	p 20	-, Column Address Strobe Upper. Column Address Strobes to the upper part (bits 0:14) of the memory array. The Column Address Strobes latches the column address (ADDR 9:15) into a 7-bits latch, which is located internally in the memory chips.
-, WE 0-16 U -, WE 16-32 U -, WE 32-48 U -, WE 48-64 U	p 20	-, Write Enable Upper. Write Enable signal to upper part of the memory array (bits 0:14).
-, RAS 0-16 L -, RAS 16-32 L -, RAS 32-48 L -, RAS 48-64 L	p 21	-, Row Address Strobe Lower. Row Address Strobes to the lower part (bit 15:23 and Check Bits) of the memory array. The Row Address Strobes latches the row address (ADDR 16:22) into a 7-bits latch, which is located internally in the memory chips.
-, CAS 0-16 L -, CAS 16-32 L -, CAS 32-48 L -, CAS 48-64 L	p 21	-, Column Address Strobe Lower. Column Address Strobes to the lower part (bits 15:23 and Check Bits) of the memory array. The Column Address into a 7-bits latch, which is located internally in the memory chips.
-, WE 0-16 L -, WE 16-32 L -, WE 32-48 L -, WE 48-64 L	p 21	-, Write Enable Lower. Write Enable signal to the lower part of the memory array (bits 15:23).

Designed by 78.12.12.VH

Drawn by 78.12.12.KISH

Dwg. Office Check 78.12.21.VH



14/11-78 VH AGA

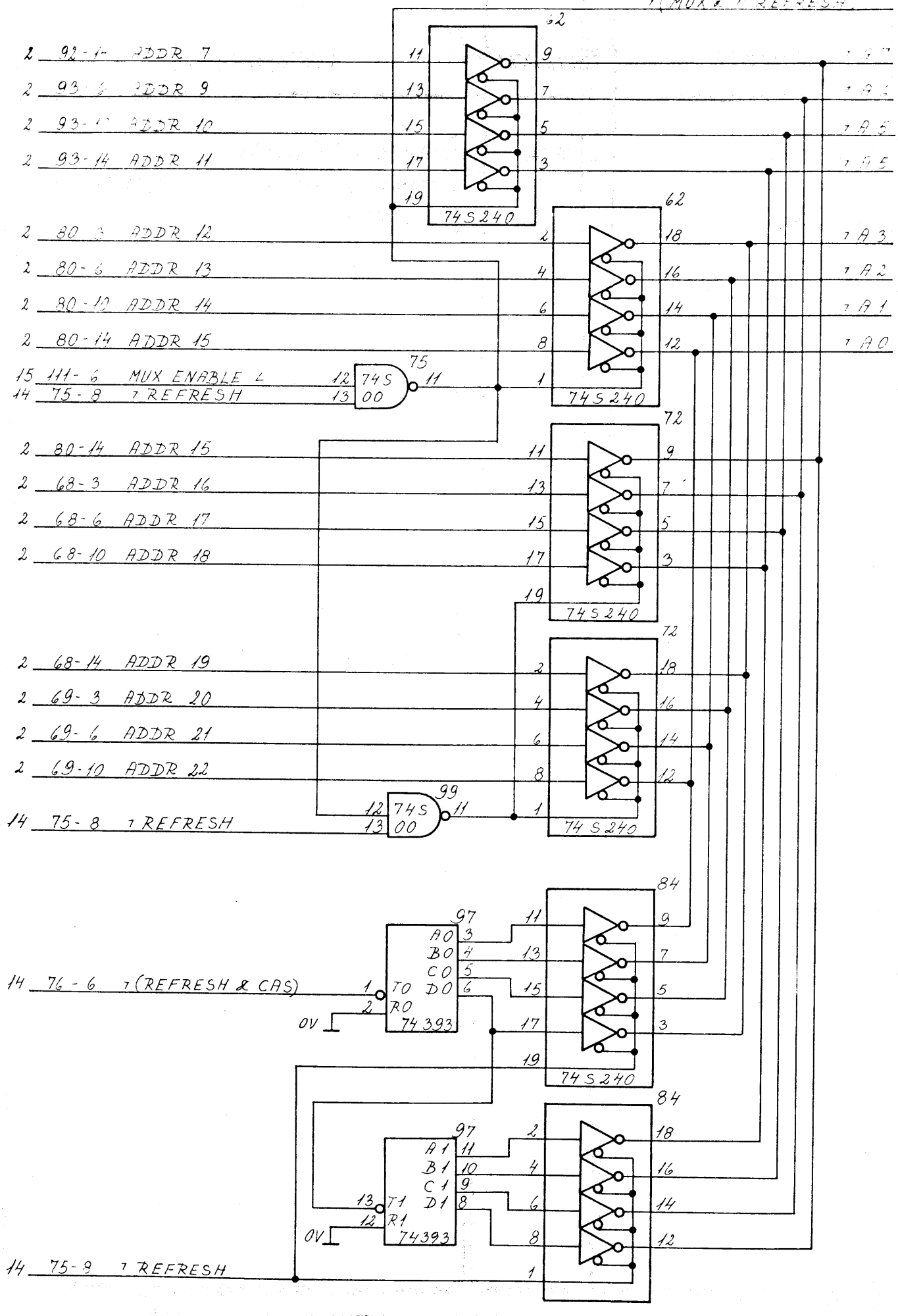
MEM805

A13607

CLOCK DRIVERS

SIGNAL	DESTINATION	DESCRIPTION
-, (MUX & -, REFRESH)	p 15	Refer to MUX & -, REFRESH signal on page 15.
-, A0:A6	p 18 p 19	-, Address bits 0:6. These address lines are via the address drivers routed to the memory array.

Designed by	Drawn by	Dy[illegible]ffice Check
78.12.12.VH	78.12.12.KISH	78.12.21.VH



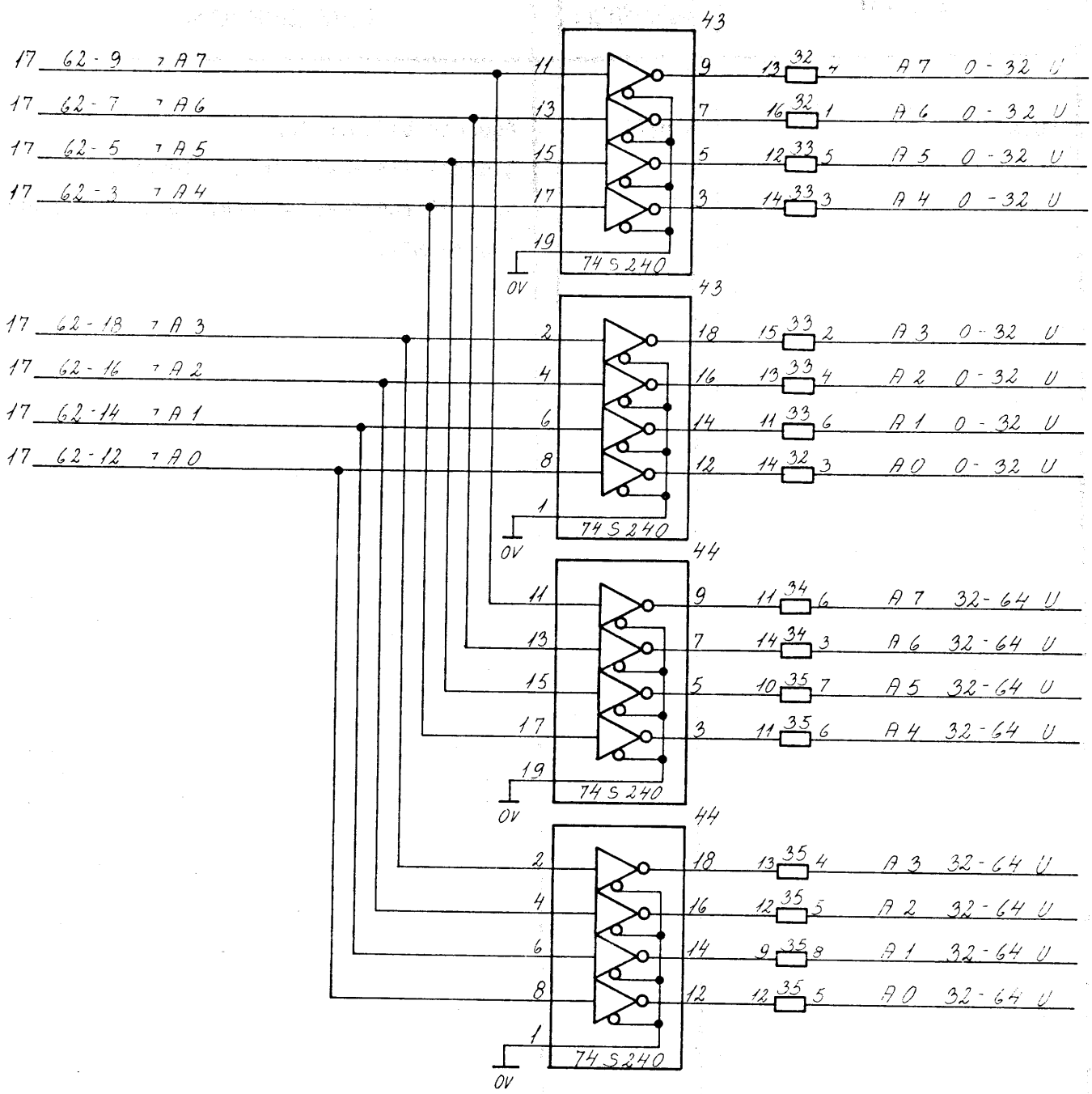
MEM 805 MEMORY ADDRESS SELECTOR and MEMORY REFRESH COUNTER 17

A13608

SIGNAL	DESTINATION	DESCRIPTION
A0:A6 0-32 U A0:A6 32-64 U	p 20	Address bit 0:6 upper. Address Lines 0:6 to bits 0:14 of the memory array.

Designed by	Drawn by	Dw	Office Check
78.12.12.VH	78.12.12.KISH	78.	12.21.VH

Unit		
MEM 805	UPPER ADDRESS DRIVERS	p 18 of 23
Dwg. No. A 25566		



Note!

All resistors are 33 E, dual-in line resistors!

Note!

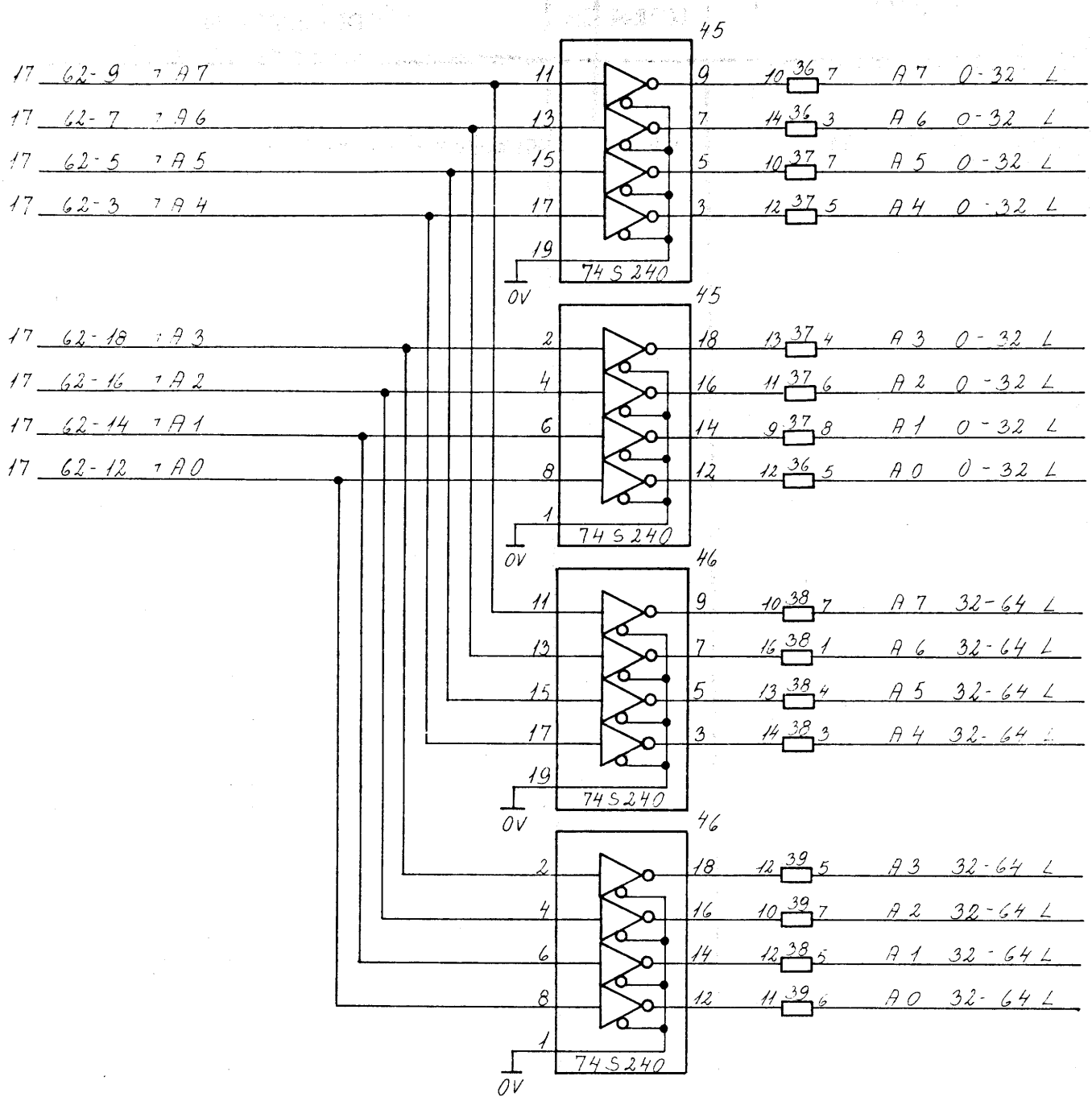
A7 signals are not used. These signals are for future use.

VH AGA 14'11-78

SIGNAL	DESTINATION	DESCRIPTION
A0:A6 0-32 L	p 21	Address bit 0:6 lower. Address lines 0:6 to the lower part of Part of the memory array (bits 15:23 and Check bits).

Designed by	Drawn by	Dy	ffice Check
78.12.12.VH	78.12.12.KISH	78.12.21.VH	

Unit		
MEM 805	LOWER ADDRESS DRIVERS	p 19 of 23
Dwg. No. A 25567		



Note!

All resistors are 33 E, dual in line resistors.

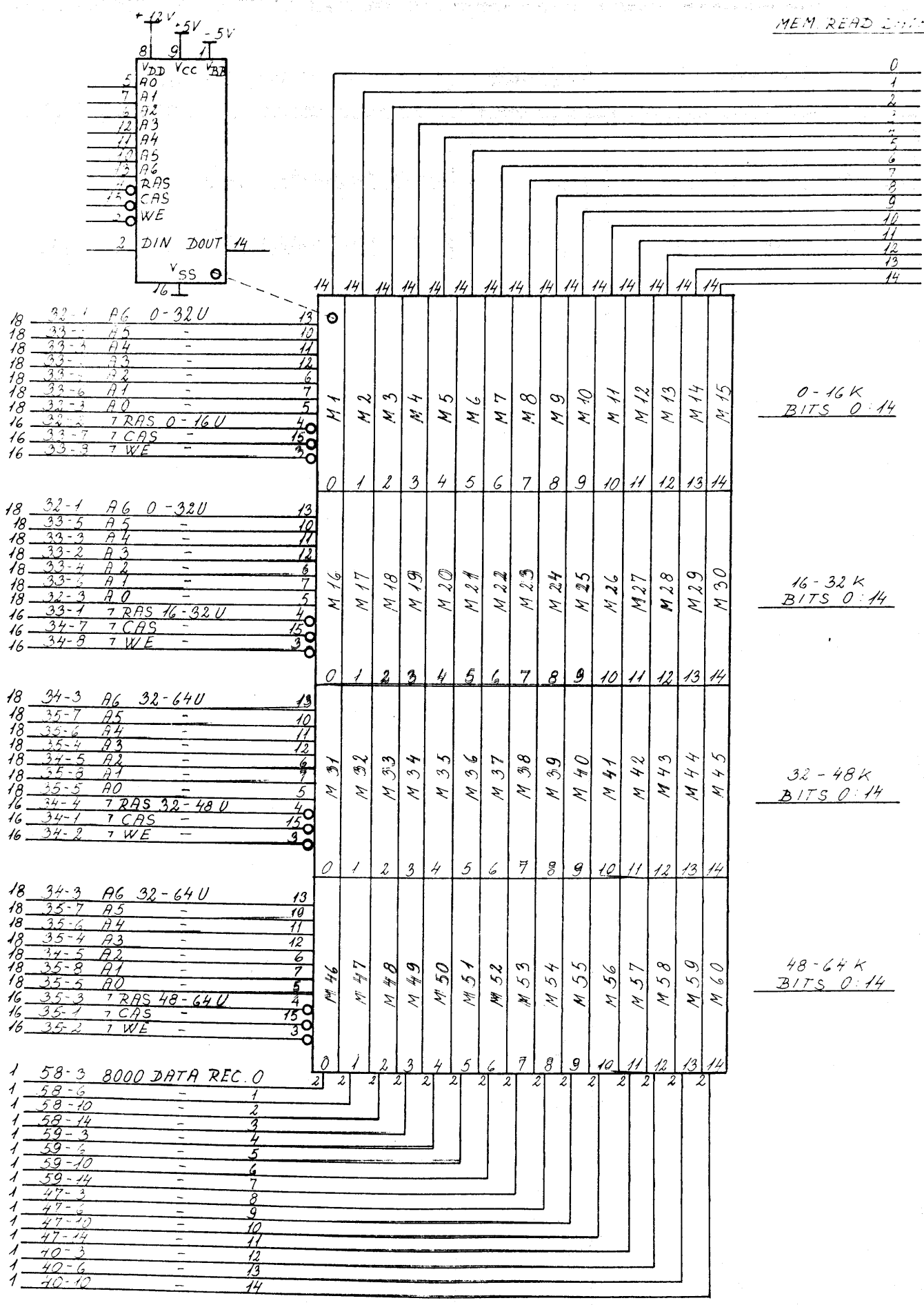
Note!

A7 signals are not used. These signals are for future use.

V.H 14/11-78 96.9

SIGNAL	DESTINATION	DESCRIPTION
MEM. READ DATA 0:14	p 6	Memory Read Data 0:14.

Designed by	Drawn by	Dw	Office Check
78.12.12.VH	78.12.12.KISH	78.	12.21.VH



V4 AG 12 14/11-78

NOTE! For Memory chip types refer to diagram 21A.

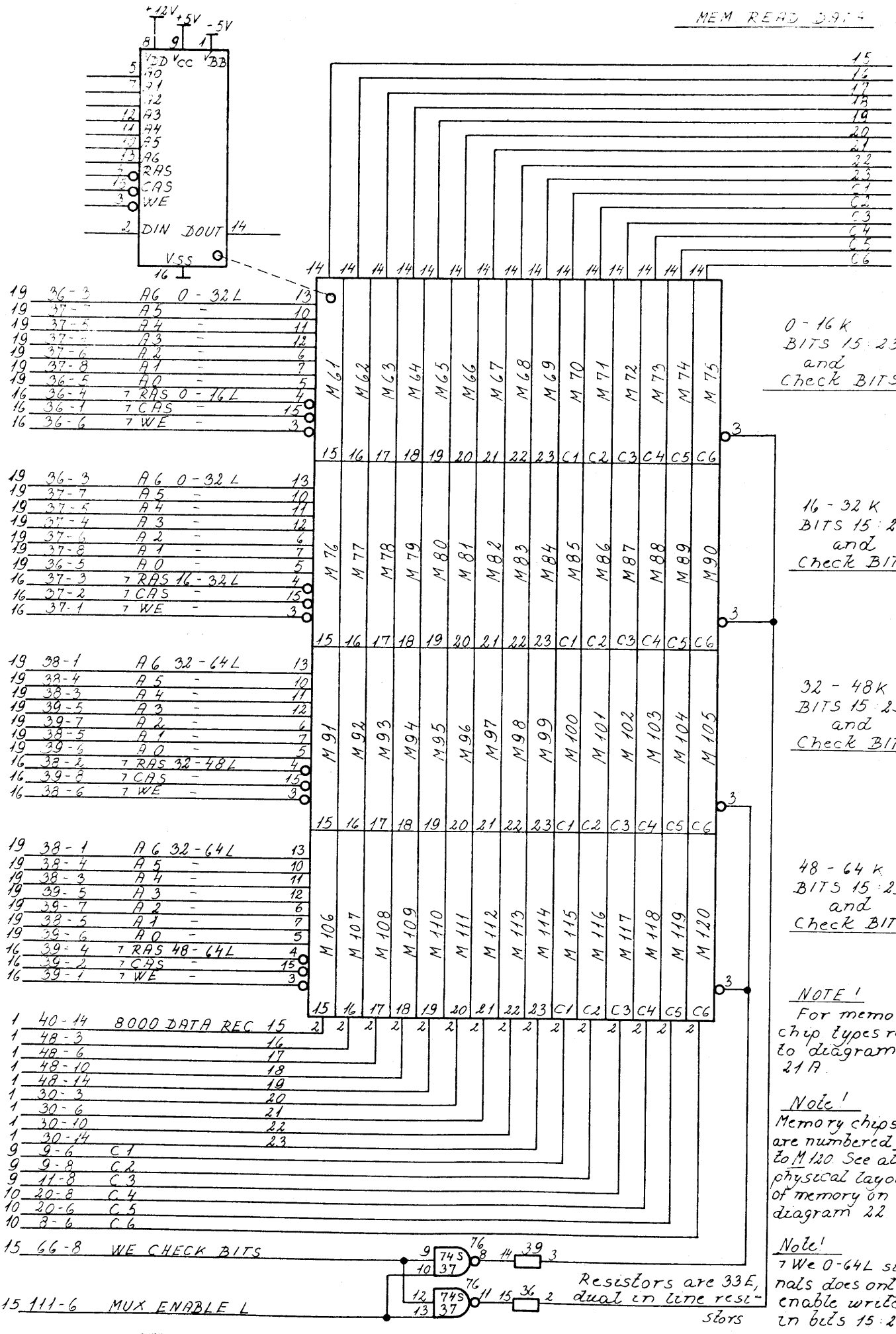
NOTE! Memory chips are numbered M1 to M120 Se also physical layout of memory array on diagram 22.

MEM 805 MEMORY ARRAY BITS 0:14

A13611

SIGNAL	DESTINATION	DESCRIPTION
MEM. READ DATA 15:23	p 6	Memory Read Data 15:23.
MEM. READ DATA C1:C6	p 6	Memory Read Data C1:C6 (check bits).

Designed by	Drawn by	Office Check
78.12.12.VH	78.12.12.KISH	78.12.21.VH



0 - 16 K BITS 15 23 and Check BITS

16 - 32 K BITS 15 23 and Check BITS

32 - 48K BITS 15 23 and Check BITS

48 - 64 K BITS 15 23 and Check BITS

NOTE !
For memory chip types refe to diagram 21 A.

Note !
Memory chips are numbered M1 to M120. See also physical layout of memory on diagram 22

Note!
⁊We 0-64L signals does only enable write in bits 15 23

VH 14-11-78 AGA

Designed by	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.
78.12.12.VH	78.12.12.KISH	78.12.21.VH				

Dynamic RAM types are: NEC μPD 416D

NATIONAL MM 5290-4

MOSTEK MK 4116-3

ITT 4116-4

A/S REGNECENTRALEN

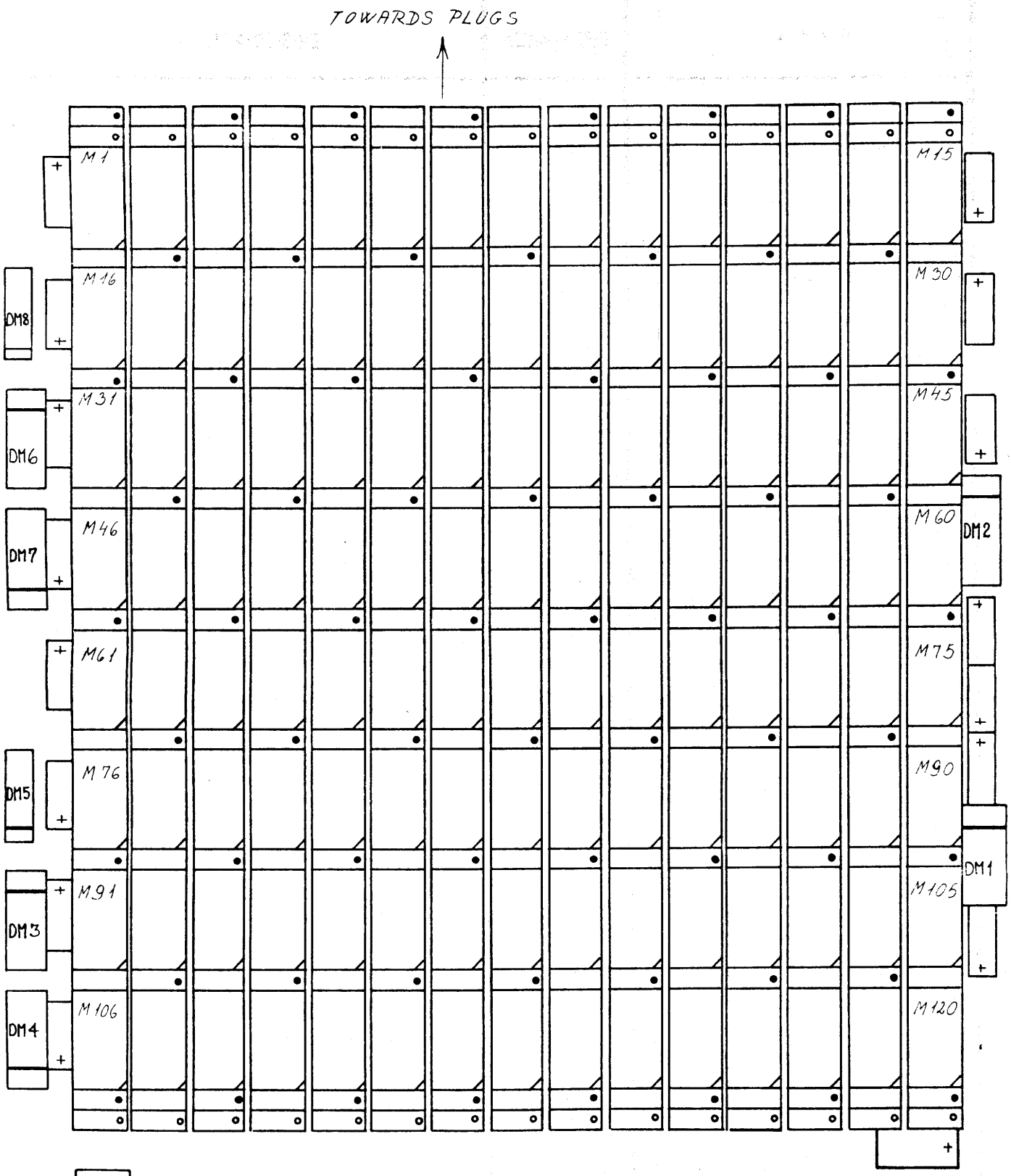
RC doc: VB 139

Unit		
MEM 805	MEMORY ARRAY BITS 0:23 AND CHECK BITS	21A of 23
Dwg. No. A 25580	DYNAMIC RAM TYPES	

SIGNAL	DESTINATION	DESCRIPTION
- NO COMMENTS -		

Designed by	Drawn by	Dr. Office Check
78.12.12.VH	78.12.12.KISH	78.12.21.VH

Unit		
MEM 805		p 22 of 23
Dwg. No.		
A 25570		


TOWARDS PLUGS
M1
M15
M16
M30
DM8
M31
M45
DM6
M46
M60
DM2
DM7
M61
M75
M76
M90
DM5
DM1
M91
M105
DM3
M106
M120
DM4
Rev. 790220 VH/ABP
AGA
14-11-79
= Ceramic 0.22 µF + 12V to 0V
= Ceramic 0,1 µF + 5V to 0V
= Ceramic 0.1µF - 5V to 0V
= TANTAL 4,7µF/15V + 12V to 0V
= TANTAL 4,7µF/10V - 5V to 0V
DM5,DM8 - 1N 5818 -5V to 0V
DM1,DM2 = ICTE 5 TRANS ZORB + 5V to 0V
DM3,DM6 = ICTE 12 TRANSZORB + 12 V to 0V.
DM4,DM7 - ICTE 5 TRANS ZORB - 5V to 0V

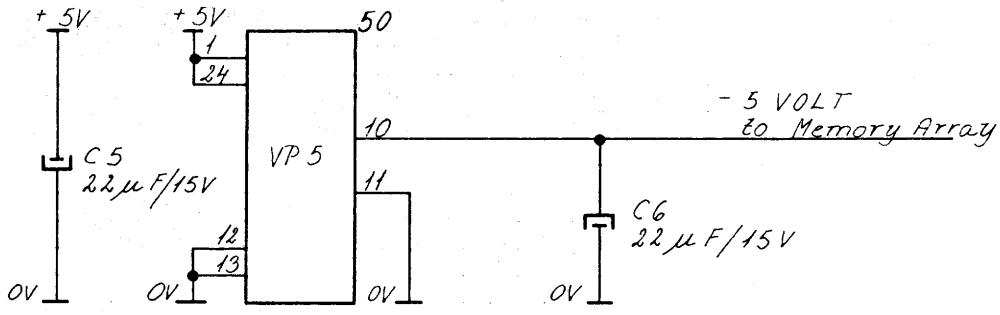
SIGNAL	DESTINATION	DESCRIPTION
- NO COMMENTS -		

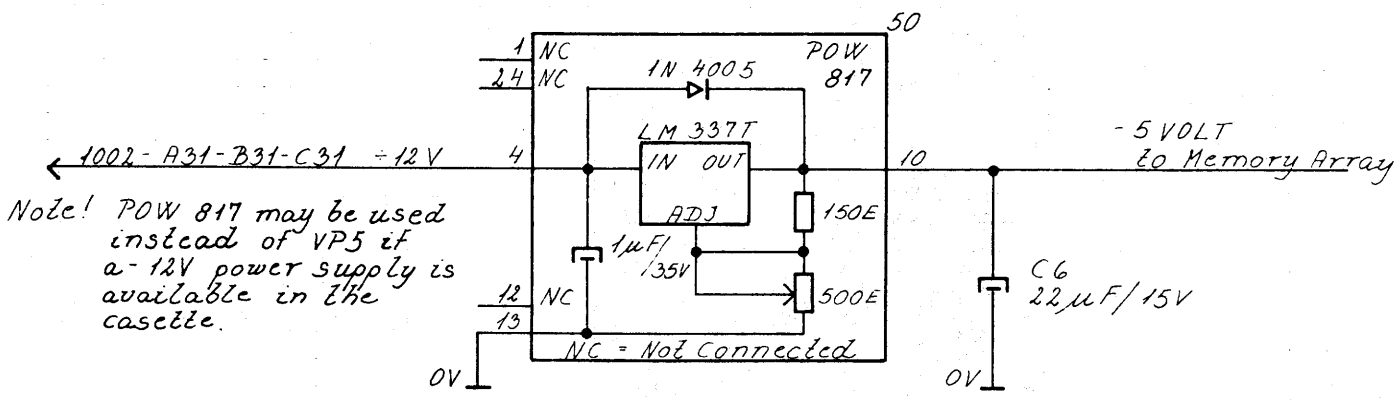
Designed by	Drawn by	Dw... Office Check
78.12.12.VH	78.12.12.KISH	78.12.21.VH

Capacitor number CC xx	Located at IC number
01	2
02	5
03	6
04	11
05	16
06	17
07	90
08	23
09	28
10	29
11	37
12	47
13	60
14	68
15	82
16	92

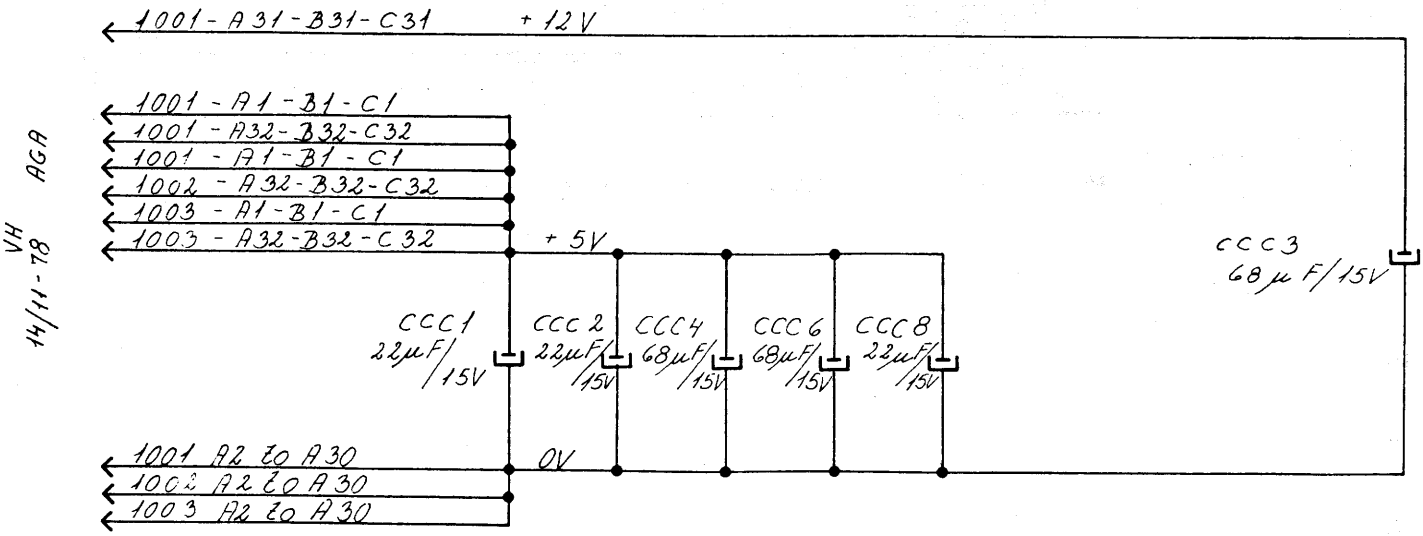
Capacitor number CC xx	Located at IC number
17	105
18	51
19	61
20	71
21	83
22	96
23	106
24	53
25	63
26	74
27	85
28	98
29	110
30	67

+ 5 VOLT High Frequency decoupling capacitors. 47nF/ /16V





Note! POW 817 may be used instead of VP5 if a -12V power supply is available in the casette.



VH AGA 14/11-78

RC doc. VB 140

A/S REGNECENTRALEN	Designed by	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.

Unit MEM 805

Dwg. No. A13572

ASSEMBLY DRAWING

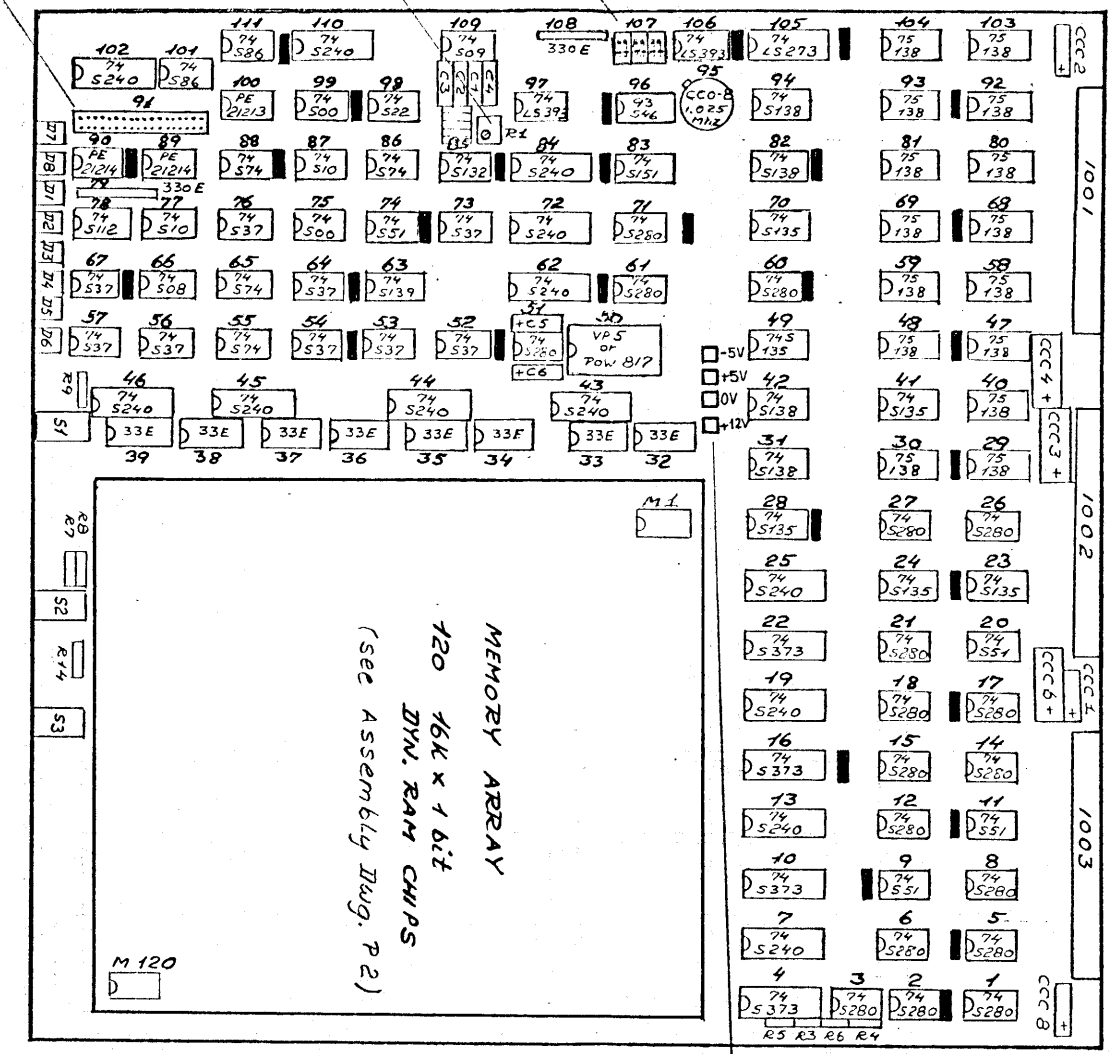
P1 of 2

Delay Line Strap

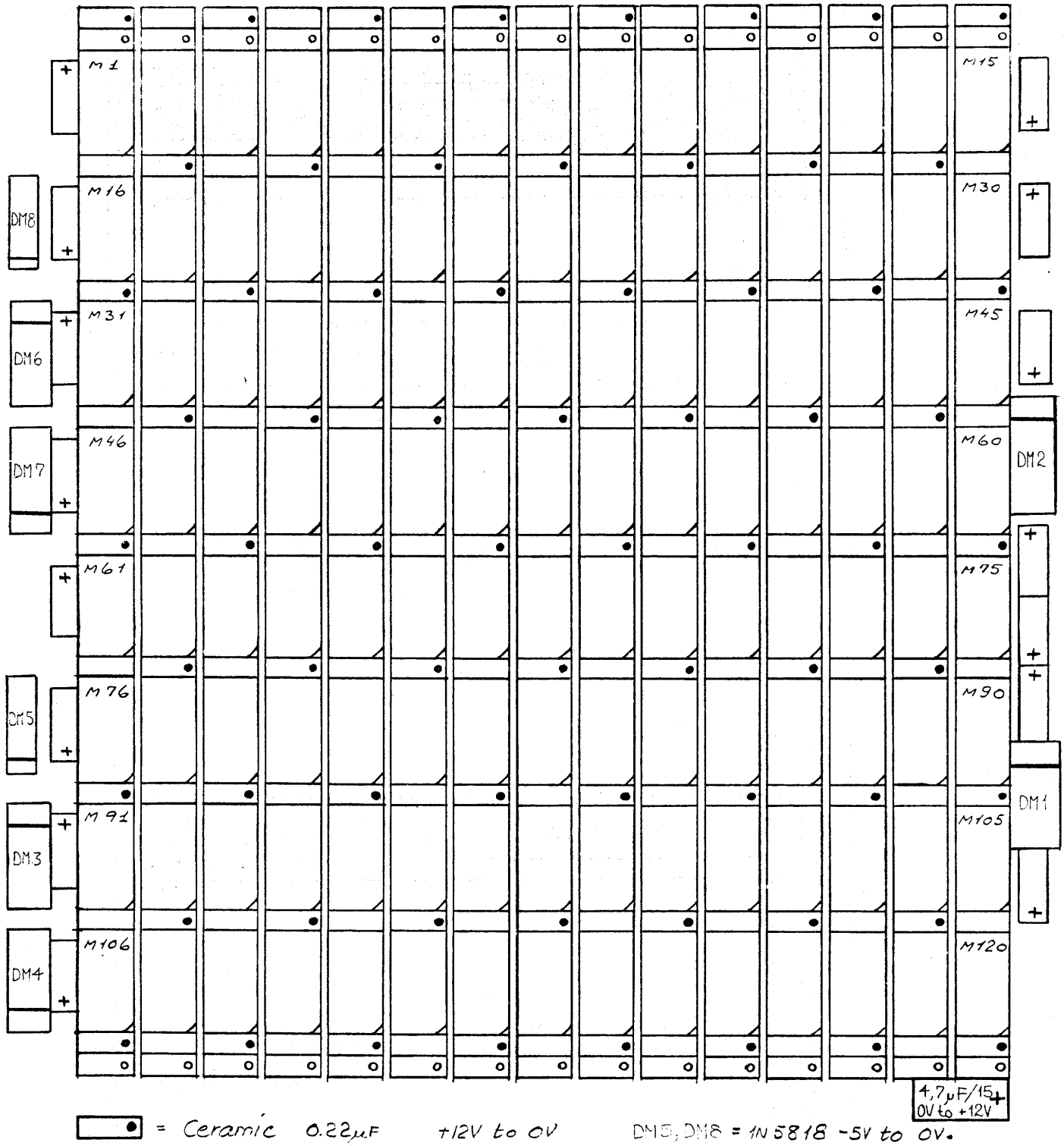
Eastern Acc.

Address Selector Switches

■ = 47 nF / 16 V decoupling +5V to 0V.



TEST POINTS DC-voltages



= Ceramic 0.22µF +12V to 0V

= Ceramic 0.1µF +5V to 0V

= Ceramic 0.1µF -5V to 0V

= TANTAL 4.7µF/5V +12V to 0V

= TANTAL 4.7µF/10V -5V to 0V

DM5, DM8 = 1N 5818 -5V to 0V.

DM1, DM2 = ICTE 5 TRANSZORB +5V to 0V.

DM3, DM6 = ICTE 12 TRANSZORB +12V to 0V.

DM4, DM7 = ICTE 5 TRANSZORB -5V to 0V.

A/S RECENTRALEN

Designed by MJ 5/12-74

Drawn by

Dwg. Check

Design Check

Replaces Dwg. No.

due to ECN

ed by Dwg. No.

RC doc V8 14

Unit
MEM 805

Dwg. No.
A 13573

ASSEMBLY DRAWING

P2 of 2

AGF 1973

MEM 805
A13574

1001 Plug List for
MEM 805 connection to RC 8000 system bus

CONNECTOR : 1001								
PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME
A1		+5 VOLT	B1		+ 5 VOLT	C1		+5 VOLT
A2		0 VOLT	B2		-, SEL IN (0)	C2		-, BUS REQ (0) 1)
A3		0 VOLT	B3	1001-B2	-, SEL OUT (0)	C3		-, BUS REQ (1) 1)
A4		0 VOLT	B4		-, SEL IN (1)	C4		-, COM SEL 1)
A5		0 VOLT	B5	1001-B4	-, SEL OUT (1)	C5		-, SEL ACK 1)
A6		0 VOLT	B6		-, SYS RESET	C6		POB 1)
A7		0 VOLT	B7		-, DATA RDY	C7		-, BUS BUSY 1)
A8		0 VOLT	B8		-, DATA ACK	C8		POK
A9		0 VOLT	B9		-, DATA NACK	C9		-, PINT 1)
A10		0 VOLT	B10		-, ADDR (0)	C10		-, ADDR (1)
A11		0 VOLT	B11		-, ADDR (2)	C11		-, ADDR (3)
A12		$\bar{0}$ VOLT	B12		-, ADDR (4)	C12		-, ADDR (5)
A13		0 VOLT	B13		-, ADDR (6)	C13		-, ADDR (7)
A14		0 VOLT	B14		-, ADDR (8)	C14		-, ADDR (9)
A15		0 VOLT	B15		-, ADDR (10)	C15		-, ADDR (11)
A16		0 VOLT	B16		-, ADDR (12)	C16		-, ADDR (13)
A17		0 VOLT	B17		-, ADDR (14)	C17		-, ADDR (15)
A18		0 VOLT	B18		-, ADDR (16)	C18		-, ADDR (17)
A19		0 VOLT	B19		-, ADDR (18)	C19		-, ADDR (19)
A20		0 VOLT	B20		-, ADDR (20)	C20		-, ADDR (21)
A21		0 VOLT	B21		-, ADDR (22)	C21		-, ADDR PAR
A22		0 VOLT	B22		-, DATA (0)	C22		-, DATA (1)
A23		0 VOLT	B23		-, DATA (2)	C23		-, DATA (3)
A24		0 VOLT	B24		-, DATA (4)	C24		-, DATA (5)
A25		0 VOLT	B25		-, DATA (6)	C25		-, DATA (7)
A26		0 VOLT	B26		-, DATA (8)	C26		-, DATA (9)
A27		0 VOLT	B27		-, DATA (10)	C27		-, DATA (11)
A28		0 VOLT	B28		-, DATA (12)	C28		-, DATA (13)
A29		0 VOLT	B29		-, DATA (14)	C29		-, DATA (15)
A30		0 VOLT	B30		-, DATA (16)	C30		-, DATA (17)
A31		+ 12 VOLT	B31		+12 VOLT	C31		+12 VOLT
A32		+ 5 VOLT	B32		+5 VOLT	C32		+5 VOLT

1) NOT USED

MEM 805

A13575

1002 Plug List for

MEM 805 connection to RC 8000 system bus

CONNECTOR : 1002								
PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME
A1		+5 VOLT	B1		+5 VOLT	C1		+5 VOLT
A2		0 VOLT	B2		-, DATA (18)	C2		-, DATA (19)
A3		0 VOLT	B3		-, DATA (20)	C3		-, DATA (21)
A4		0 VOLT	B4		-, DATA (22)	C4		-, DATA (23)
A5		0 VOLT	B5		-, DATA PAR (0)	C5		-, DATA PAR (1)
A6		0 VOLT	B6		-, DATA PAR (2)	C6		-, DATA OUT
A7		0 VOLT	B7			C7		
A8		0 VOLT	B8			C8		
A9		0 VOLT	B9			C9		
A10		0 VOLT	B10			C10		
A11		0 VOLT	B11			C11		
A12		0 VOLT	B12			C12		
A13		0 VOLT	B13			C13		
A14		0 VOLT	B14			C14		
A15		0 VOLT	B15			C15		
A16		0 VOLT	B16			C16		
A17		0 VOLT	B17			C17		
A18		0 VOLT	B18			C18		
A19		0 VOLT	B19			C19		
A20		0 VOLT	B20			C20		
A21		0 VOLT	B21			C21		
A22		0 VOLT	B22			C22		
A23		0 VOLT	B23			C23		
A24		0 VOLT	B24			C24		
A25		0 VOLT	B25			C25		
A26		0 VOLT	B26			C26		
A27		0 VOLT	B27			C27		
A28		0 VOLT	B28			C28		
A29		0 VOLT	B29			C29		
A30		0 VOLT	B30			C30		
A31		-12 VOLT	B31		-12 VOLT	C31		-12 VOLT
A32		+5 VOLT	B32		+5 VOLT	C32		+5 VOLT

MEM 805
A13576

1003 Plug List for
MEM 805 Connection to RC 8000 system bus

CONNECTOR : 1003								
PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME
A1		+5 VOLT	B1		+5 VOLT	C1		+5 VOLT
A2		0 VOLT	B2			C2		
A3		0 VOLT	B3			C3		
A4		0 VOLT	B4			C4		
A5		0 VOLT	B5			C5		
A6		0 VOLT	B6			C6		
A7		0 VOLT	B7			C7		
A8		0 VOLT	B8			C8		
A9		0 VOLT	B9			C9		
A10		0 VOLT	B10			C10		
A11		0 VOLT	B11			C11		
A12		0 VOLT	B12			C12		
A13		0 VOLT	B13			C13		
A14		0 VOLT	B14			C14		
A15		0 VOLT	B15			C15		
A16		0 VOLT	B16			C16		
A17		0 VOLT	B17			C17		
A18		0 VOLT	B18			C18		
A19		0 VOLT	B19			C19		
A20		0 VOLT	B20			C20		
A21		0 VOLT	B21			C21		
A22		0 VOLT	B22			C22		
A23		0 VOLT	B23			C23		
A24		0 VOLT	B24			C24		
A25		0 VOLT	B25			C25		
A26		0 VOLT	B26			C26		
A27		0 VOLT	B27			C27		
A28		0 VOLT	B28			C28		
A29		0 VOLT	B29			C29		
A30			B30			C30		
A31			B31			C31		
A32		+5 VOLT	B32		+5 VOLT	C32		+5 VOLT