Title:

GENERAL INFORMATION
FOR
MEM 805 SEMICONDUCTOR MEMORY

A/S REGNECENTRALEN

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GENERAL INFORMATION

Abstract:

This publication is a general information of semiconductor memory - MEM 805 designed for the RC 8000 computer family

C O N T E N T S PAGE

1. GENERAL DESCRIPTION 1.

MEM 805 is a dynamic semiconductor memory, which is designed to be used by the RC 8000 computer family.

MEM 805 consists of one multilayer printed circuit card, which provides 64K x 30 bits.

MEM 805 can be connected directly to the RC 8000 unified bus. The PCB contains all of the circuits necessary for a CPU or peripheral divice to read data stored in the dynamic RAM chips, or to write data into the dynamic RAM chips.

MEM 805 does also include memory device selection switches, which makes it possible to connect a theoretical maximum of 64 MEM 805 to the unified bus.

To increase memory reliability a single error correction and double error detection (SEC-DED) code has been incorporated. This code requires 6 check bits/data words. MEM 805 returns data nack if a double error is detected.

2. SPECIFICATIONS

2.1 Performance Specifications

MEMORY TYPE:	Dynamic random access memory, using standard 16384 words by 1 bit dynamic N channel MOS RAM integrated circuits
WORD LENGTH:	24 data bits + 6 check bits
CAPACITY:	65536 words
ACCESS TIME:	600 nS typ. - from data ready to data ack
CYCLE TIME:	680 nS typ. - from data ready to memory ready
WIDTH OF ACCESS/CYCLE:	1 word
OPERATIONAL MODES:	Read-Write
ERROR CONTROL:	Single error correction - Double error detection
ERROR INDICATION:	8 light emitting diodes on front panel (6 syndrome bits - 2 address bits)
INTERFACE CHARACTERISTIC:	Standard RC 8000 unified bus interface

2.2 Electrical Specifications 2.2

SUPPLY VOLTAGES:

+ 5V dc ± 5% / 7A
+ 12V dc ± 5% / 1A
(frequency of access being 1 Mhz)

- 5V dc
to the memory array is normally supplied via a + 5V to - 5V converter (VP 5) located in IC position 50, however, an adjustable - 5V regulator (POW 817) may be mounted in IC position 50 instead of VP 5. If POW 817 is used a - 12V power supply must be present in the cassette. This power supply must be capable to supply:
- 12V dc ± 10% / 0.1 A

2.3 Environmental Specifications 2.3

AMBIENT TEMPERATURE: 10 - 35°C

RELATIVE HUMIDITY: 20 - 80% (non-condensing)

2.4 Physical Specifications 2.4

MULTILAYER PRINTED CIRCUIT CARD DIMENTIONS:

359.7 mm wide
369.7 mm deep

3. IDENTIFICATION OF ITEMS

3.

item	reference number	description
1	MEM 805	64K semiconductor memory module
2	POW 817	- 5V adjustable voltage regulator

4. INSTALLATION 4.

4.1 Installation of the Memory 4.1

The memory may be inserted in any position of the cassette.

CAUTION: The PCB board must not be removed from or inserted in the cassette whilst dc-power is present

4.2 Memory Addressing 4.2

Switches for selection of the memory device address are located in IC position 107 (refer to Fig. 4.1 and 4.2). Address bit 0 is always 0.

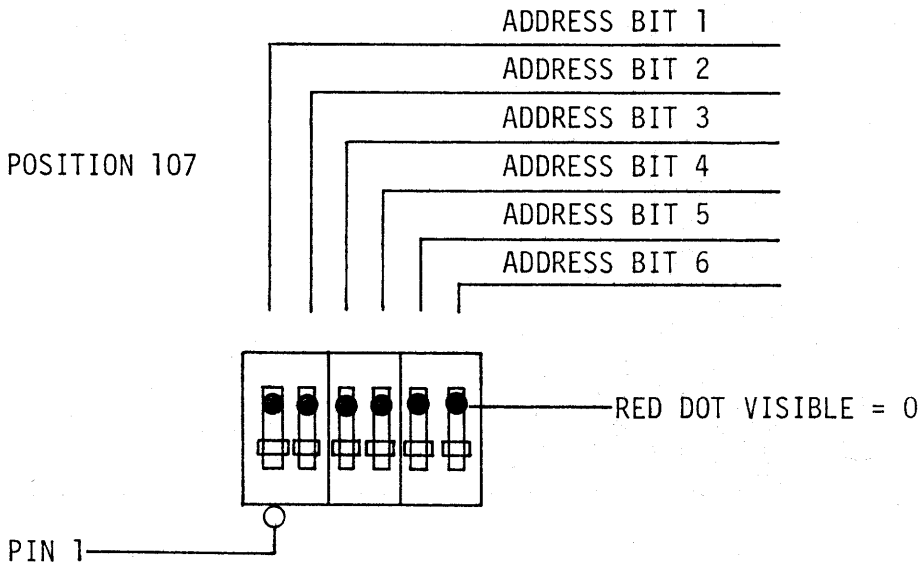
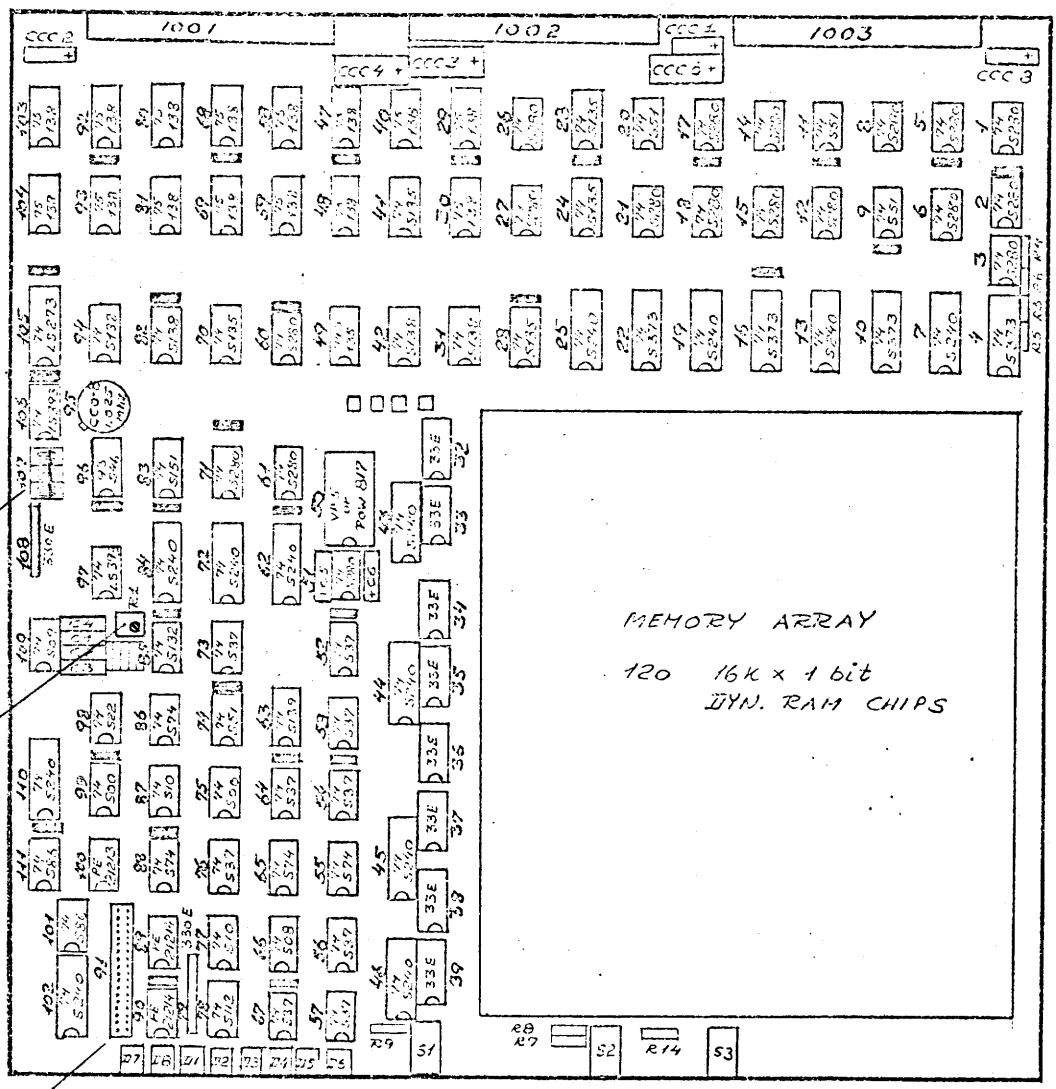


FIGURE 4.1

DEVICE ADDRESS SELECTORS IN THE MEMORY



ADDRESS SELECTOR SWITCHES

DESKEW ADJ.
Turn, clockwise to increase delay.

DELAY LINE STRAP

A/S REGISTERCENTRALEN	Designed by	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Rev. by Dwg. No.

Unit		
MEM 805	Address Selector Switches, Delay Line Strap and Deskew Delay Location	FIG. 42
Dwg. No.		

The address of the first installed memory is:

ADDRESS BITS (1:6) = 000000

For more than one MEM 805 the table shown in Figure 4.3 must be followed.

	ADDRESS BIT AND SWITCH POS 107 PIN					
	1	2	3	4	5	6
0K / 64K	x	x	x	x	x	x
64K / 128K	x	x	x	x	x	
128K / 192K	x	x	x	x		x
192K / 256K	x	x	x	x		
256K / 320K	x	x	x		x	x
320K / 384K	x	x	x		x	
384K / 448K	x	x	x			x
448K / 512K	x	x	x			
512K / 576K	x	x		x	x	x
576K / 640K	x	x		x	x	
640K / 704K	x	x		x		x
704K / 768K	x	x		x		
768K / 832K	x	x			x	x
832K / 896K	x	x			x	
896K / 960K	x	x				x
960K / 1024K	x	x				
1024K / 1088K	x		x	x	x	x
1088K / 1152K	x		x	x	x	
1152K / 1216K	x		x	x		x
1216K / 1280K	x		x	x		
1280K / 1344K	x		x		x	x
1344K / 1408K	x		x		x	
1408K / 1472K	x		x			x
1472K / 1536K	x		x			
1536K / 1600K	x			x	x	x
1600K / 1664K	x			x	x	
1664K / 1728K	x			x		x
1728K / 1792K	x			x		
1792K / 1856K	x				x	x
1856K / 1920K	x				x	
1920K / 1984K	x					x
1984K / 2048K	x					

x = read dot visible

	ADDRESS BIT AND SWITCH POS 107 PIN					
	1	2	3	4	5	6
2048K / 2112K		x	x	x	x	x
2112K / 2176K		x	x	x	x	
2176K / 2240K		x	x	x		x
2240K / 2304K		x	x	x		
2304K / 2368K		x	x		x	x
2368K / 2432K		x	x		x	
2432K / 2496K		x	x			x
2496K / 2560K		x	x			
2560K / 2624K		x		x	x	x
2624K / 2688K		x		x	x	
2688K / 2752K		x		x		x
2752K / 2816K		x		x		
2816K / 2880K		x			x	x
2880K / 2944K		x			x	
2944K / 3008K		x				x
3008K / 3072K		x				
3072K / 3136K			x	x	x	x
3136K / 3200K			x	x	x	
3200K / 3264K			x	x		x
3264K / 3328K			x	x		
3328K / 3392K			x		x	x
3392K / 3456K			x		x	
3456K / 3520K			x			x
3520K / 3584K			x			
3584K / 3648K				x	x	x
3648K / 3712K				x	x	
3712K / 3776K				x		x
3776K / 3840K				x		
3840K / 3904K					x	x
3904K / 3968K					x	
3968K / 4032K						x
4032K / 4096K						

64K means 64 x 1024 words

FIGURE 4.3

MEMORY ADDRESS SELECTION TABLE

4.3 Deskew Delay Adjustment

4.3

The deskew delay for DRDY DEL. may be adjusted by means of the potentiometer R1 on the PCB (refer to Fig. 4.2 and 4.4).

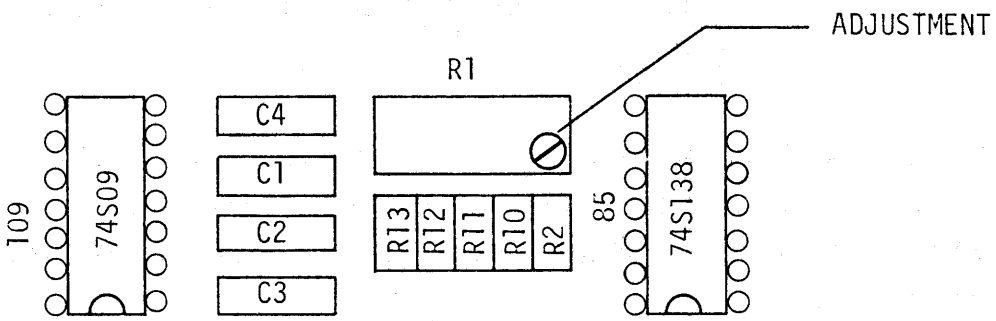


FIGURE 4.4
POTENTIOMETER FOR DESKEW DELAY ADJUSTMENT

The following procedure is recommended for adjustment of the deskew delay:

1. Turn the potentiometer fully clockwise (max. delay).

2. Start testprogram
   e.g. CPU 810 microprogrammed test operated in continuous mode via the OCP.
   Refer to "CPU 810 MICROPROGRAMMED TEST, USERS MANUAL RCSL: 30-M 167".

3. Adjust delay according to Figure 4.5

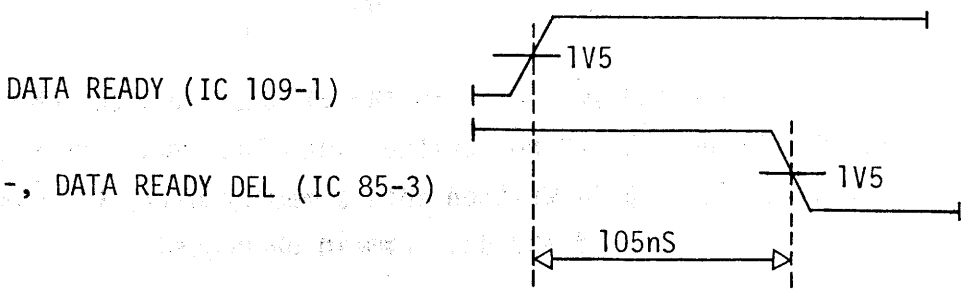


FIGURE 4.5
DESKEW DELAY

4.4 Front Panel Indicators and Switches 4.4

4.4.1 Error Display with Enable Switch 4.4.1

Error display for the Error Detection and Correction circuits is located on the front panel (refer to Fig. 4.6).

8 light emitting diodes indicates the possible error cases as shown in Fig. 4.7. The error display will be updated whenever an error occurs, thus displaying the error status of the latest error case.

The error display may be reset or disabled by means of the ERROR DISPLAY ON/OFF switch.

4.4.2 Error Detection and Correction Switches (EDC) 4.4.2

Two switches enables/disables the error corrector and the check bit generator. The switches may be used for diagnostic purposes. The switches are named CORRECTOR ON/OFF switch and GENERATOR ON/OFF switch.

When the CORRECTOR switch is in the off position no error correction takes place, and the memory returns DATA ACK even if an error is detected.

NOTE

Error status are not correctly displayed when the CORRECTOR switch is in the off position

When the GENERATOR switch is in the off position the check bits C1 through C6 are not written into the check bit memory i.e. when new data is written into a memory cell, the check bits C1 through C6 of the cell remain unchanged.

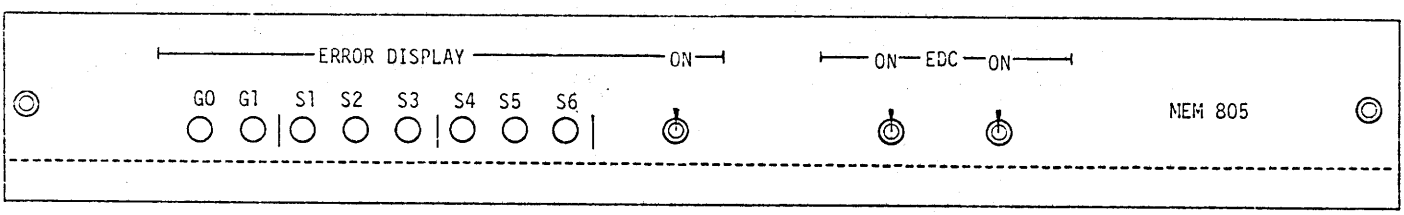


FIGURE 4.6
FRONT PANEL INDICATORS AND SWITCHES

TABLE 1

S1 through S5	S6	COMMENTS
= 0	= 0	No ERROR
= 0	= 1	Check bit 6 itself in ERROR
≠ 0	= 0	DOUBLE ERROR
≠ 0	= 1	SINGLE ERROR S1 through S5 indicates the bit position in error (see table 2) G0, G1 indicates the memory chip group in error (see table 3)

TABLE 2

S1	S2	S3	S4	S5	S6	S1 through S6 octal	Bit position in error
1	1	0	0	0	1	61	0
1	0	1	0	0	1	51	1
1	0	0	1	0	1	45	2
1	0	0	0	1	1	43	3
1	1	1	0	0	1	71	4
1	1	0	0	1	1	63	5
1	0	0	1	1	1	47	6
1	1	0	1	0	1	65	7
0	1	1	0	0	1	31	8
0	1	0	1	0	1	25	9
0	1	0	0	1	1	23	10
0	1	1	1	0	1	35	11
0	1	1	0	1	1	33	12
0	1	0	1	1	1	27	13
1	1	1	1	0	1	75	14
1	1	0	1	1	1	67	15
0	0	1	1	0	1	15	16
0	0	1	0	1	1	13	17
0	0	1	1	1	1	17	18
1	0	1	1	0	1	55	19
1	0	1	0	1	1	53	20
1	0	1	1	1	1	57	21
0	1	1	1	1	1	37	22
1	1	1	0	1	1	73	23
1	0	0	0	0	1	41	CHECK BIT 1
0	1	0	0	0	1	21	CHECK BIT 2
0	0	1	0	0	1	11	CHECK BIT 3
0	0	0	1	0	1	5	CHECK BIT 4
0	0	0	0	1	1	3	CHECK BIT 5

TABLE 3

G0	G1	MEMORY CHIP GROUP
0	0	0 - 16K
0	1	16 - 32K
1	0	32 - 48K
1	1	48 - 64K

FIGURE 4.7

ERROR DISPLAY INTERPRETATION

4.4.3 How to Locate a Memory Chip in Error 4.4.3

The error display shows:

G0	G1	S1	S2	S3	S4	S5	S6	
0	1	1	1	1	1	0	1	$= 175_8$

S1 through S6 = 75_8 indicates an error in bit 14

G0 , G1 = 1_8 indicates that the bit in error is in the 16 - 32K group. In this case memory chip M30 is in error, see Figure 4.8.

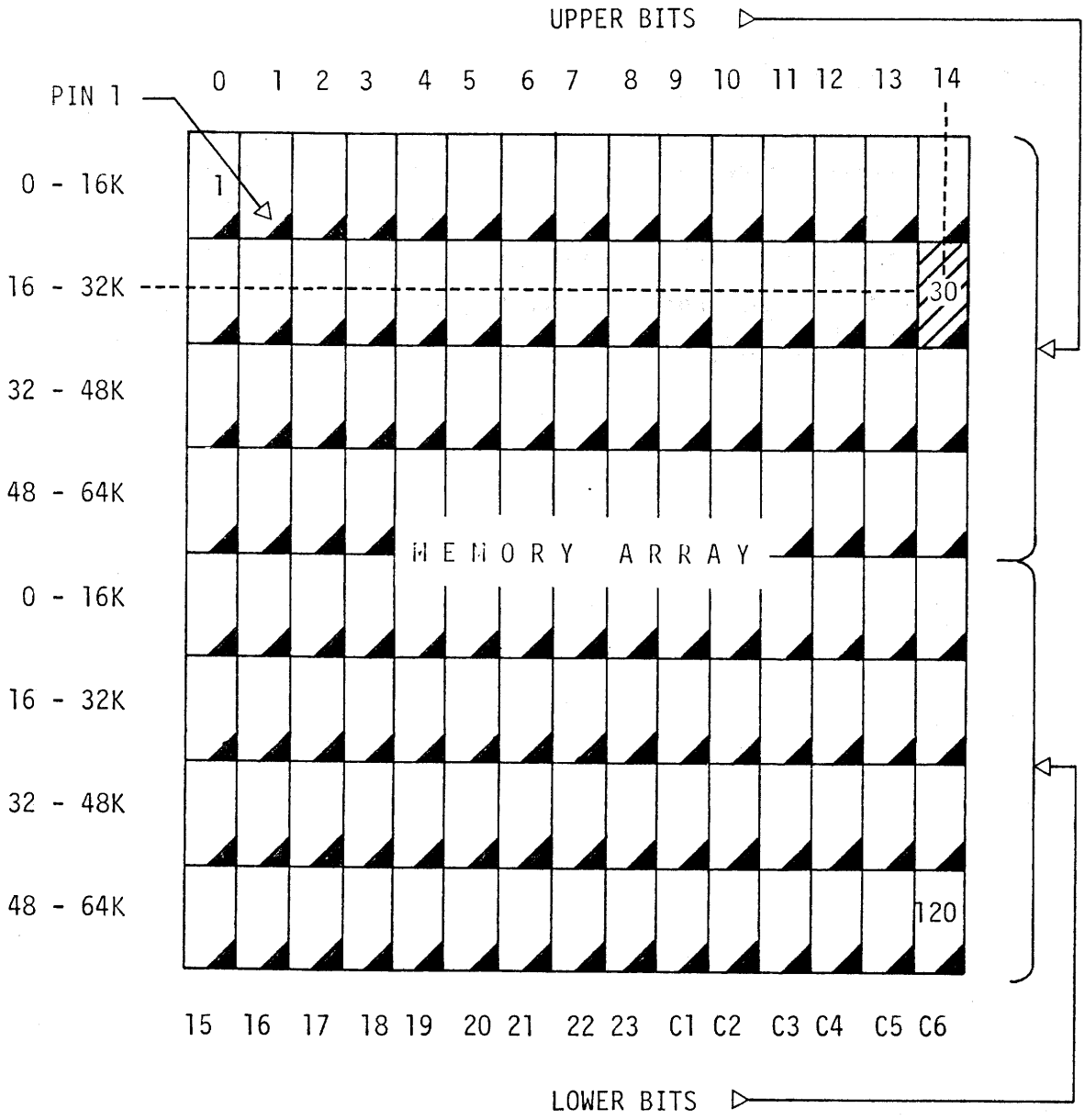


FIGURE 4.8

MEMORY ARRAY PHYSICAL LAYOUT

4.5 Strapping Possibilities (refer to Figure 4.2) 4.5

Following strap positions exist in the memory:

4.5.1 Straps for Delay Lines 4.5.1

Straps for delay lines are located in position 91 (refer to Figure 4.2). These straps define the timing for the memory chips used. These straps are set from the factory and they must not be changed. Logic diagram 15 shows the actual settings of the straps.

5. CHECK-OUT PROCEDURES

5.1 Check-Out Test of the Memory

Check-out test of the memory can be executed by means of following testprograms:

1. CPU 810 microprogrammed test 2 , 3.
   Refer to "CPU 810 MICROPROGRAMMED TEST, USERS MANUAL RCSL: 30-M 167"

2. MEM 805 testpackage
   Manual : 30-M 198
   Listing : 30-M 199
   Bin.tape: 39-M 200

An initial check-out of the memory should be performed by means of the microprogrammed test 2 and 3.

It is recommended to run test 2 via TCP for at least 2 hours. A TCA 801 and a TTY compatible device are required to run these tests. Test 2 may also be executed by means of the OCP, but no exact error messages will then be given.

The MEM 805 testpackage is used to run the more advanced diagnostic tests, which requires an I/O controller with input from paper tape or magnetic tape.