Title:

Technical Manual for Memory Control Unit MCU 802

A/S REGNECENTRALEN

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Abstract:

This paper contains the drawings and the description of MCU 802 Memory Controller.

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CONTENTS PAGE

1. Description

The Memory Controller MCU 802 is a controller to the RC 8000 computer. The controller enables the CPU or a peripheral device to read data stored in the memory, or write data into the memory. MCU 802 contains two adaptors, which are identical. Each adaptor may be connected to an MCH 801 (Memory Chassis 801) which contains 1 to 4 MEM 801's (32 K-word core memory).

2. Data Path in MCU 802

The Data Paths in MCU 802 and MEM 801 housed in MCH 801 are shown in Fig. 2.1. The Fig. is also a block diagram for the unit. To show where in the logic diagram each block is drawn, the page number is written in each block in MCU 802.

This description follows in the main the diagram for the data path.

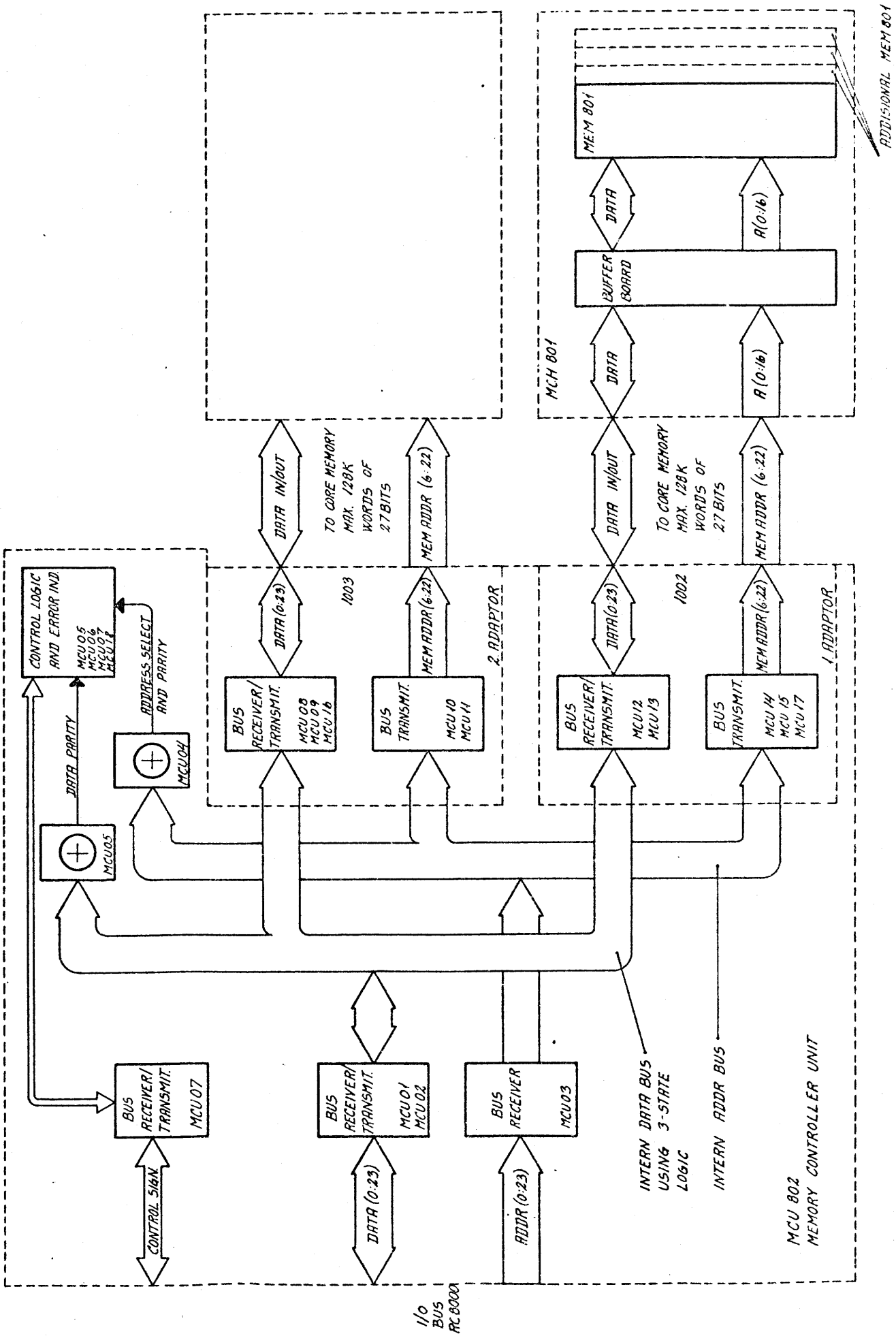
2.1. Internal Data Bus

The RC 8000 uses 27 bidirectional data lines. A word is divided into three 8-bit octets with 1 parity bit per octet. In MCU 802 the data signals use the Internal Data Bus to or from the adaptors and through the selected Adaptor via the MCH 801 to the MEM 801. The Internal Data Bus is supervised by the Control Logic via the parity control circuit.

The 27 data lines are connected to the memory module MEM 801 via the buffer board housed in MCH 801. See Fig. 2.1.

Fig. 2.2. shows the integrated circuits making up the Internal Data Bus. The functions of the circuits are:

SN75138	BUS receiver/transmitter
8T97	TRI-State BUS interface driver
8T98	TRI-State BUS interface driver
SN74538	Nand gate driver



DATA PATH IN MCU 802 AND MEM 801 HOUSED IN MCH 801.

Fig. 2.1 Data Path in MCU 802

2.2. Internal Addr. BUS

The RC 8000 uses 24 bidirectional address lines, viz. Addr (0:22) and Addr parity. MCU 802 receives these 24 lines and the controller starts if it is addressed, which means:

1. ADDR 0 is logical zero.
2. ADDR (1:4) has the same value as selected by the memory device number switches.
3. ADDR (0:23) and ADDR PARITY have odd parity.
4. The control signal Data Ready is logical one.

The circuit is shown in logic diagrams MCU 03 and MCU 04.

The 17 least significant address lines, Addr (6:22), are sent to the memory module MEM 801 via the Buffer Board housed in MCH 801. See Fig. 2.1. The Addr 5 signal is used to select the wanted adaptor. See table Fig. 2.3.

2.3. Control Logic and Error Indication

The Control Logic is shown in the logic diagrams page MCU 05, page MCU 06, and page MCU 07, and the Error Indicator curcuit is shown on page MCU 18. These circuits are very simple and they are shown in the timing diagrams Fig. 2.4.

The timing diagrams also show how the delays in the control logic are adjusted.

The Error Indication circuit is shown on MCU 18. In a read cycle with parity error the information which octet and which module failed is latch in the register.

In a write cycle with parity error in the data received from the I/O Bus, the BUS PARITY indicator is turned on.

The indicator is cleared by a SYS RESET or ¬IPOK, or manually by means of the RESET button on the front panel.

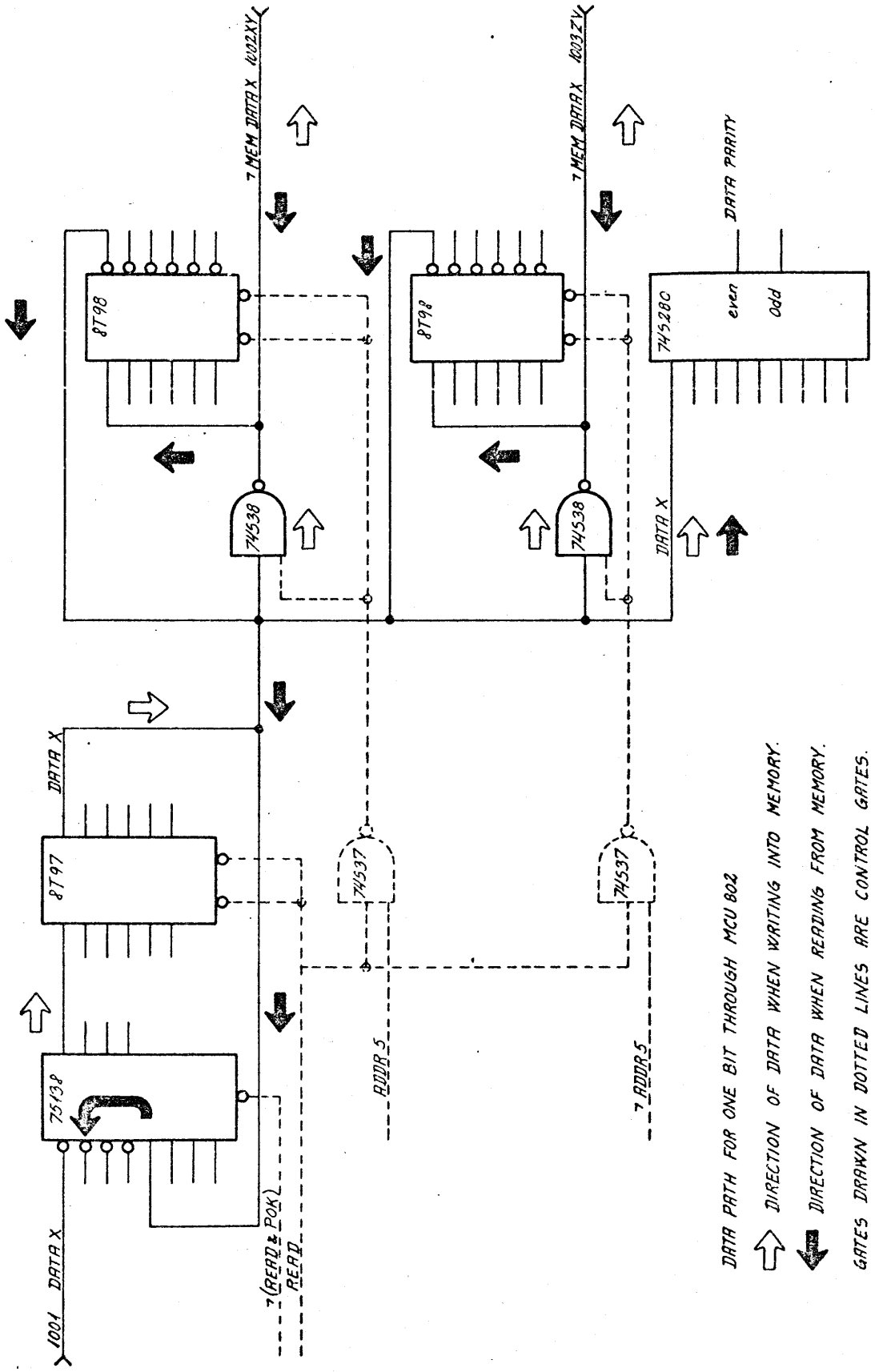


Fig. 2.2 Intern Data Bus.

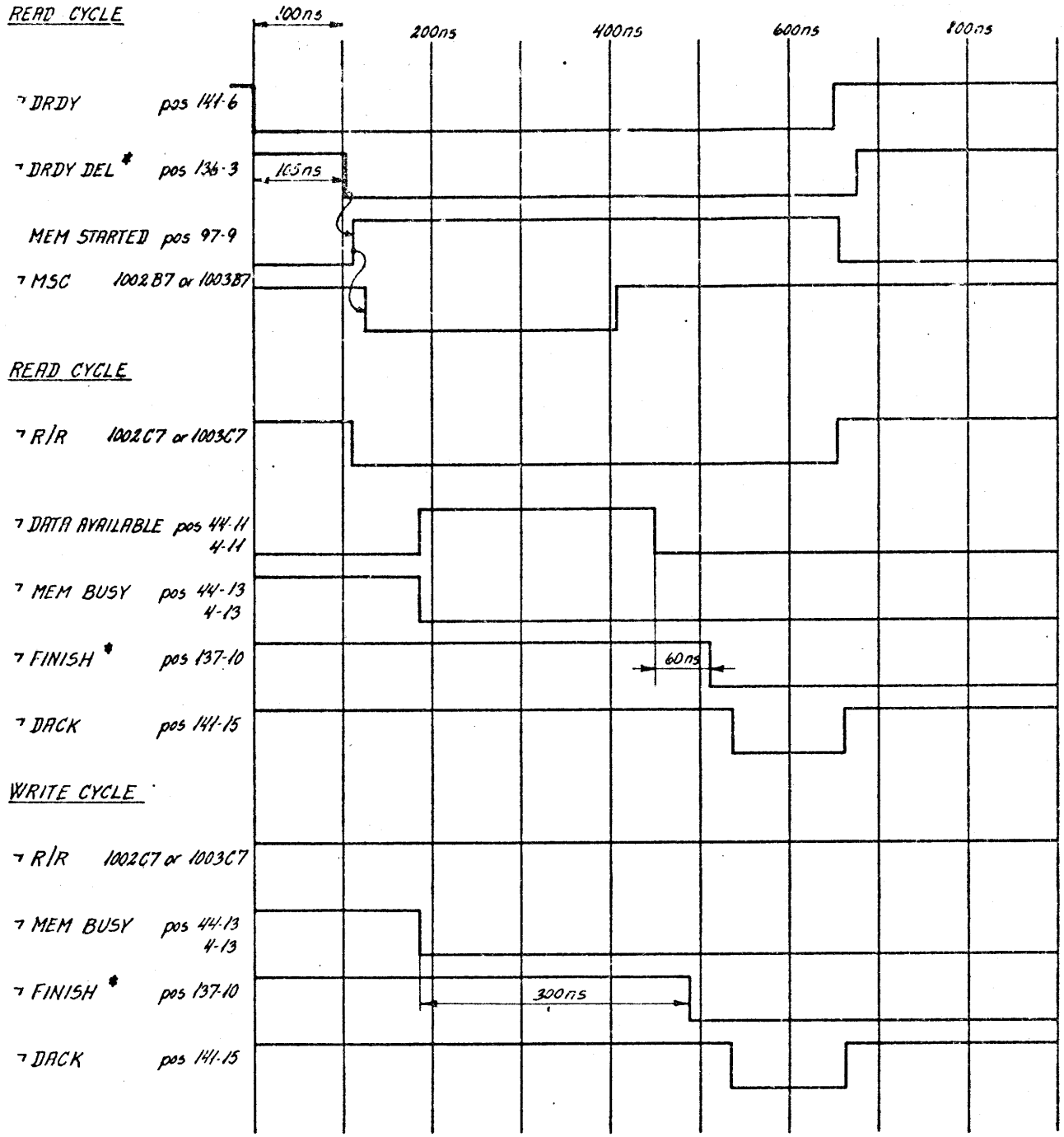
Memory location 1. Adaptor plug 1003	Memory location 2. Adaptor plug 1002	Addr. 1 switch pos 95-1	Addr. 2 switch pos 95-2	Addr. 3 switch pos 95-3	Addr. 4 switch pos 95-4
0/128K	128K/256K	X	X	X	X
256/384K	384K/512K	X	X	X	
512/640K	640K/768K	X	X		X
768/896K	896/1024K	X	X		
1024/1152K	1152/1280K	X		X	X
1280/1408	1408/1536K	X		X	
1536/1664K	1664/1792K	X			X
1792/1920K	1920/2048K	X			
2048/2176K	2176/2304K		X	X	X
2304/2432K	2432/2560K		X	X	
2560/2688K	2688/2816K		X		X
2816/2944K	2944/3072K		X		
3072/3200K	3200/3328K			X	X
3328/3456K	3456/3584K			X	
3584/3712K	3712/3840K				X
3840/3968	3968/4096K				

X = Switch closed ~ logical zero

when a switch is closed the red dot is visible.

128K means 128 * 1024 word

Fig. 2.3 Memory Address Selection table.



* ADJUSTMENT OF MCU802 IS MADE IN ACCORDANCE WITH THIS TIMING DIAGRAM

DRDY DEL IS ADJUSTED USING POTENTIOMETER IN POS 107

FINISH " " " " " POS 128 IN READ CYCLE

FINISH " " " " " POS 127 IN WRITE CYCLE

Fig. 2.4 Timing Diagram for MCU 802

3. Connection from MCU 802 to MEM 801

The figure on this page shows the interconnection from MCU 802 to two MEM 801 housed in MCH 801.

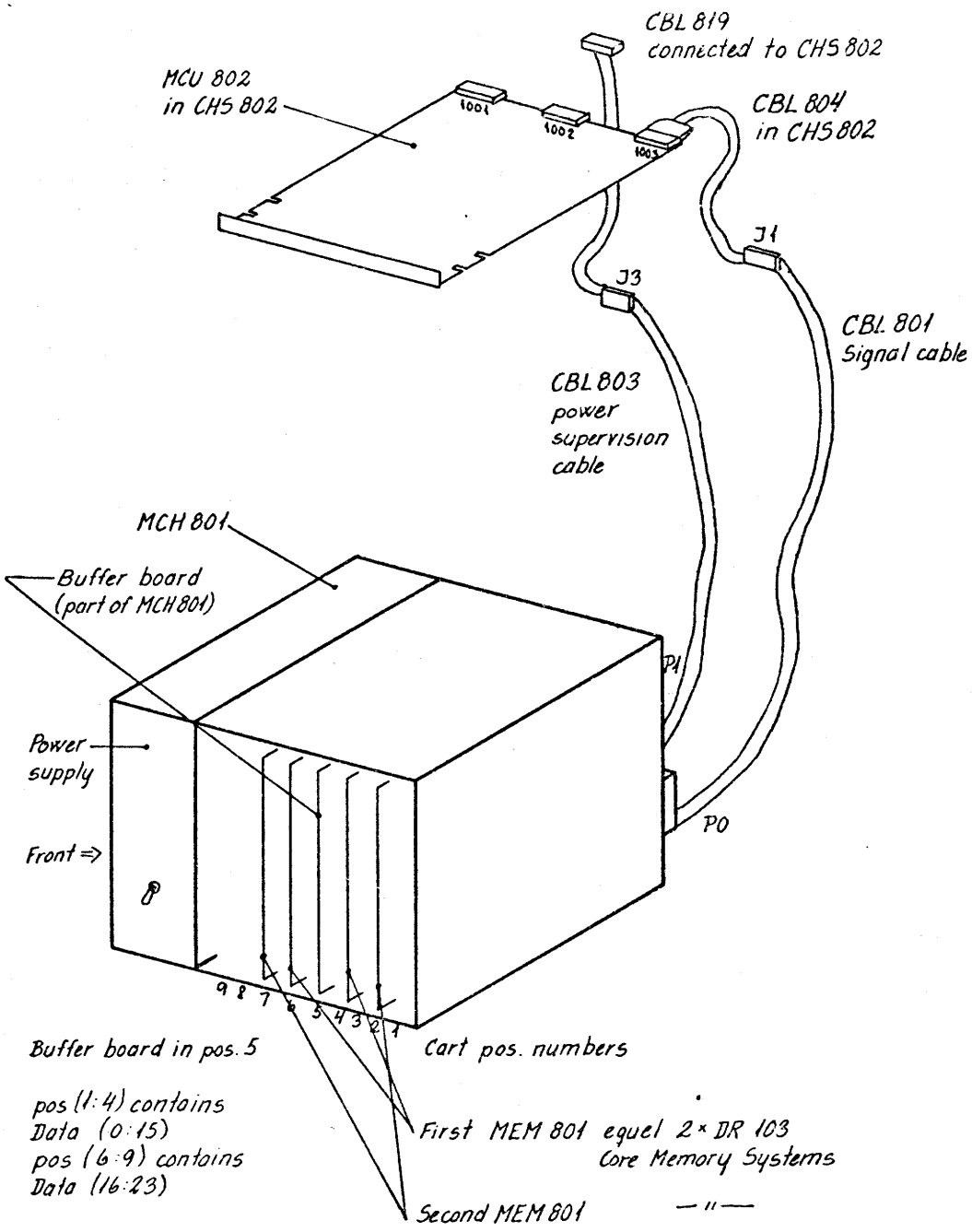


Fig. 3.1 Interconnection of Cables and Units to make a 64 K word system.

Connection between MCU 802 and MEM 801

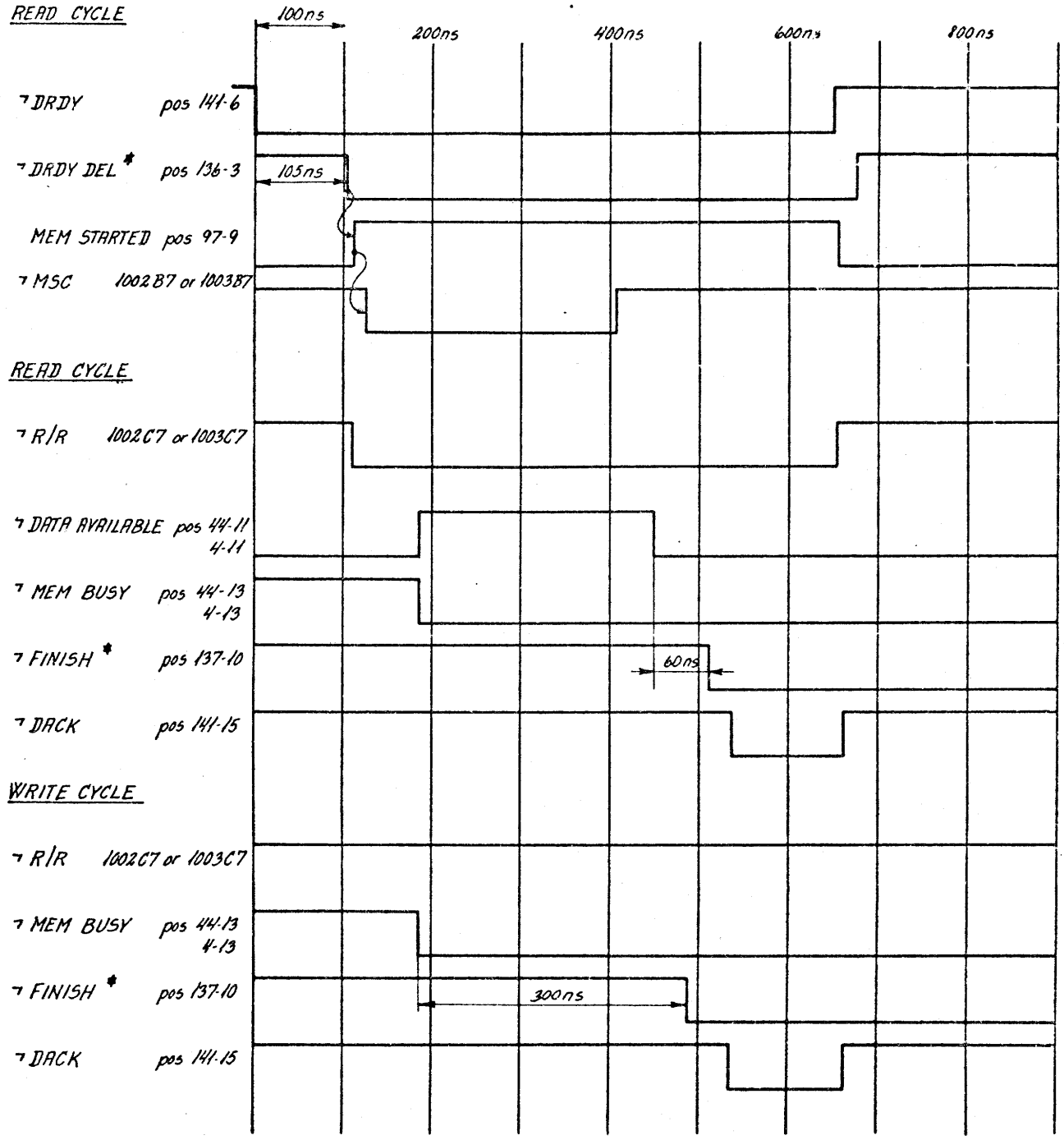
MEM 801 housed in MCH 801

No.	Signal name in MCU 802	Direction	Pin No. on RC 8000 board	Pin No. on 117 pol ELCO Signal	Pin No. on 117 pol ELCO Ground		Pin No. in to MEM CHASSIS	Pin No. out from pos 5 in MEM	Pin No. in Chain in MCH 801	Signal name in MEM 801
1	MEMADDR 6	→	1003 or 1002 B 9	E 1	E 2		5 B-49	5 B-48	B - 61	A 17
2	- 7	→	- C 9	E 3	E 4		- 47	- 50	- 69	A 16
3	- 8	→	- B 10	E 5	E 6		- 51	- 52	- 62	A 15
4	- 9	→	- C 10	E 7	F 7		- 55	- 56	- 67	A 14
5	- 10	→	- B 11	F 6	F 5		- 81	- 82	- 81	A 13
6	- 11	→	- C 11	F 4	F 3		- 77	- 78	- 79	A 12
7	- 12	→	- B 12	F 2	F 1		- 73	- 74	- 77	A 11
8	- 13	→	- C 12	H 2	H 3		- 69	- 70	- 75	A 10
9	- 14	→	- B 13	H 4	H 5		- 63	- 64	- 74	A 9
10	- 15	→	- C 13	H 6	H 7		- 65	- 66	- 73	A 8
11	- 16	→	- B 14	J 7	J 6		- 61	- 62	- 71	A 7
12	- 17	→	- C 14	J 5	J 3		- 59	- 60	- 72	A 6
13	- 18	→	- B 15	J 2	J 1		- 79	- 80	- 82	A 5
14	- 19	→	- C 15	K 1	K 2		- 75	- 76	- 80	A 4
15	- 20	→	- B 16	K 6	K 7		- 57	- 58	- 70	A 3
16	- 21	→	- C 16	M 1	M 2		- 71	- 72	- 78	A 2
17	- 22	→	- B 17	M 6	M 7		- 67	- 68	- 76	A 1
							- 53	- 54	- 68	A 0
18	MEMDATA 0	↔	1003 or 1002 C 17	N 7	N 6		0 A-41 and 47			Data in/out bit 1
19	- 1	↔	- B 18	N 5	N 3		- -39 - 49			- - bit 2
20	- 2	↔	- C 18	N 2	N 1		- -31 - 45			- - bit 3
21	- 3	↔	- B 19	P 2	P 3		- -25 - 55			- - bit 4
22	- 4	↔	- C 19	P 4	P 5		- -37 - 53			- - bit 5
23	- 5	↔	- B 20	P 6	P 7		- -27 - 51			- - bit 6
24	- 6	↔	- C 20	R 7	R 6		- -23 - 57			- - bit 7
25	- 7	↔	- B 21	R 5	R 4		- -19 - 59		Pos(1 : 4)	- - bit 8
26	- 8	↔	- C 21	R 3	R 2		- -17 - 67			- - bit 12
27	- 9	↔	- B 22	R 1	S 1		- -15 - 65			- - bit 13
28	- 10	↔	- C 22	S 2	S 3		- -11 - 63			- - bit 14
29	- 11	↔	- B 23	S 4	S 5		- -13 - 69			- - bit 15
30	- 12	↔	- C 23	S 6	S 7		- - 9 - 71			- - bit 16
31	- 13	↔	- B 24	T 7	T 6		- - 7 - 73			- - bit 17
32	- 14	↔	- C 24	T 5	T 4		- -35- 79			- - bit 18
33	- 15	↔	- B 25	T 3	T 2		- -29- 77			- - bit 19
34	- 16	↔	- C 25	T 1	U 1		9 A-80- 47	5 B-24		- - bit 1
35	- 17	↔	- B 26	U 2	U 3		- -74- 49	- -23		- - bit 2
36	- 18	↔	- C 26	U 4	U 5		- -37- 45	- -18		- - bit 3
37	- 19	↔	- B 27	U 6	U 7		- -36- 55	- -17		- - bit 4
38	- 20	↔	- C 27	V 7	V 6		- -72- 53	- -22	Pos(6 : 9)	- - bit 5
39	- 21	↔	- B 28	V 5	V 4		- -35- 51	- -16		- - bit 6
40	- 22	↔	- C 28	V 3	V 2		- -33- 57	- -14		- - bit 7
41	- 23	↔	- B 29	V 1	X 1		- -31- 59	- -12		- - bit 8
42	MEMPAR 0	↔	- C 29	X 2	X 3		OA -21- 61		Pos(1 : 4)	- - bit 9
43	MEMPAR 1	↔	- B 30	X 4	X 5		OA -33- 75			- - bit 20
44	ME MPAR 2	↔	- C 30	X 6	X 7		10 -34- 61	5 B- 15	Pos(6 : 9)	- - bit 9
45	DATA available	←	- B 8	D 4	D 3		5 B -1		B - 1	DATA available
46	MEM BUSY	←	- C 8	D 2	D 1		5 A -84		B - 35	MEM BUSY
47	MSC	→	- B 7	C 7	D 7		5 B -37	5 B- 38	B - 37	MSC
48	RIR	→	- C 7	D 6	D 5		5 B-29 and 25		B - 25	RIR 1
									B - 29	RIR 2
49	Spare Data	↔	- B 6	C 3	C 4		9 A-32 and 67	5 B- 13	Pos(1 : 4) and (6 : 9)	Data in/out bit 12
50	- -	↔	- C 6	C 5	C 6		- -29 - 65	- - 10		- - bit 13
	- -	↔	- B 5	B 2	B 1		- -27 - 63	- - 8		- - bit 14
	- -	↔	- C 5	C 1	C 2		- -30 -69	- - 11		- - bit 15
	- -	↔	- B 4	B 6	B 5		- -28 - 71	- - 9	pos(6 : 9)	- - bit 16
	- -	↔	- C 4	B 4	B 3		- -25 - 73	- - 7		- - bit 17
	- -	↔	- B 3	A 5	A 6		- -41 - 79	- -21		- - bit 18
	- -	↔	- C 3	A 7	B 7		- -38 - 77	- -19		- - bit 19
	- -	↔	- C 2	A 3	A 4		- -39 -75	- -20		- - bit 20

Signal List

WRITE CYCLE and

READ CYCLE



* ADJUSTMENT OF MCU802 IS MADE IN ACCORDANCE WITH THIS TIMING DIAGRAM

¬DRDY DEL IS ADJUSTED USING POTENTIOMETER IN POS 107

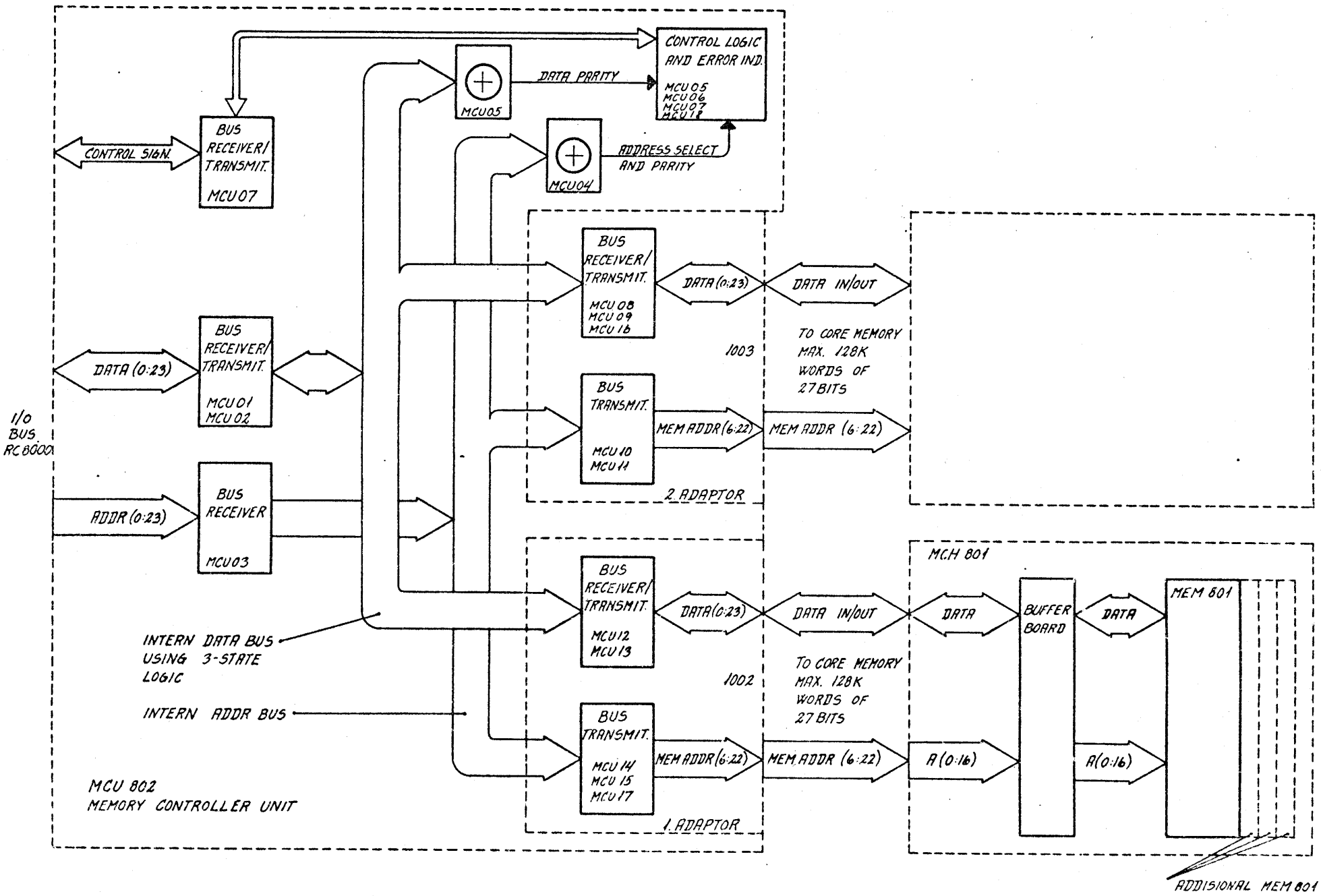
¬FINISH " " " " " POS 128 IN READ CYCLE

¬FINISH " " " " " POS 127 IN WRITE CYCLE

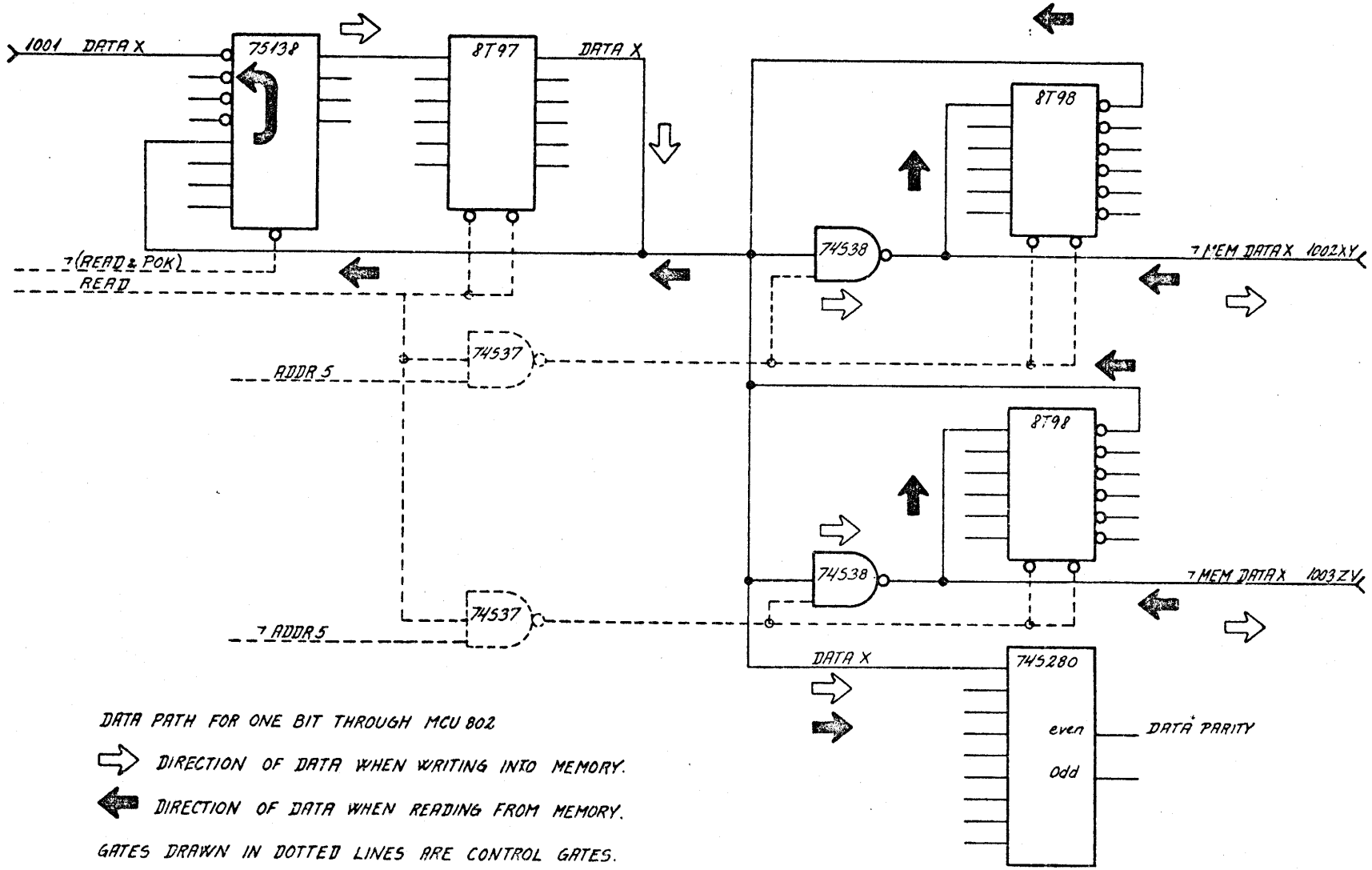
R 11627

A 11628

DATA PATH IN MCU 802 AND MEM 801
HOUSED IN MCH 801.



R 11629

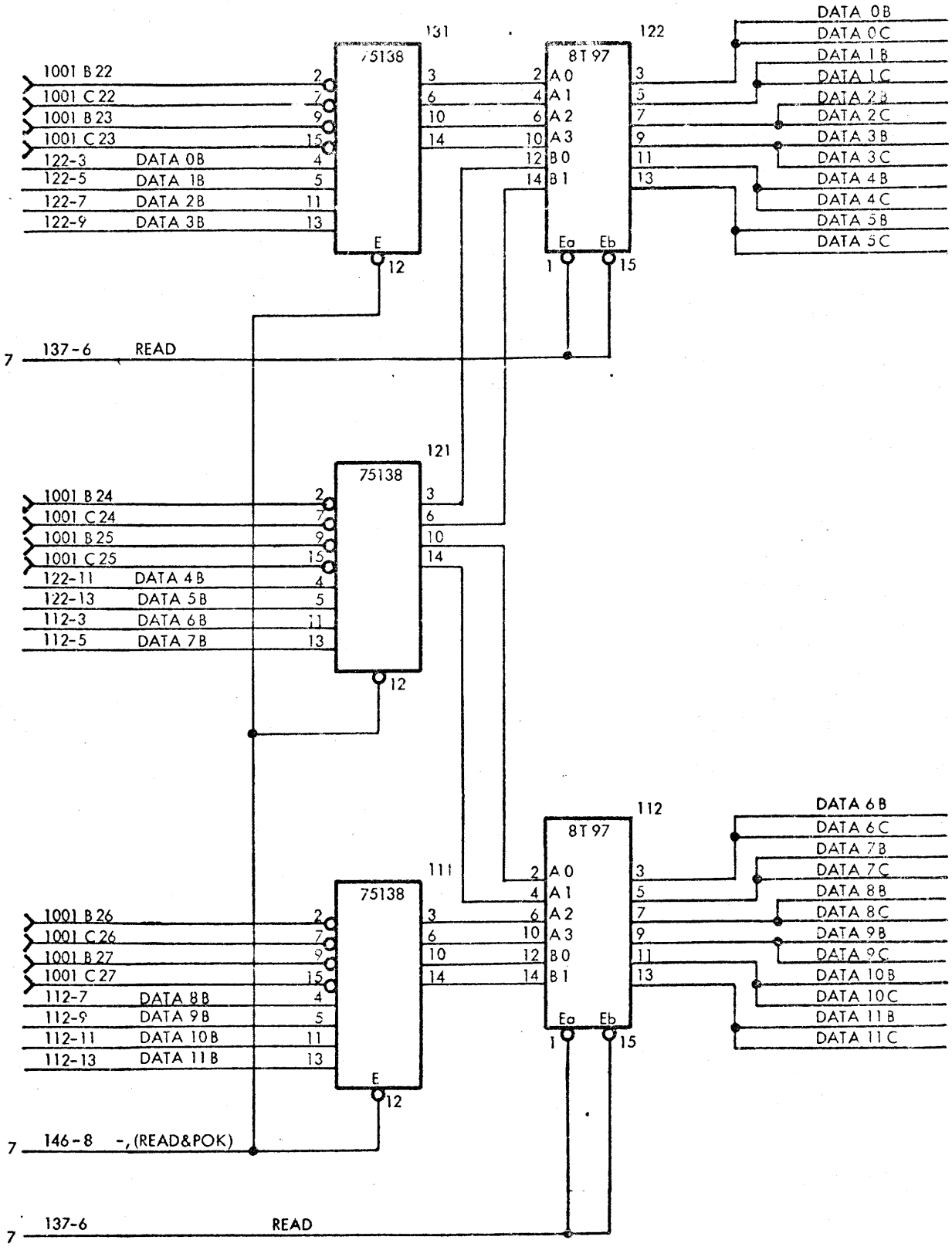


DATA PATH FOR ONE BIT THROUGH MCU 802

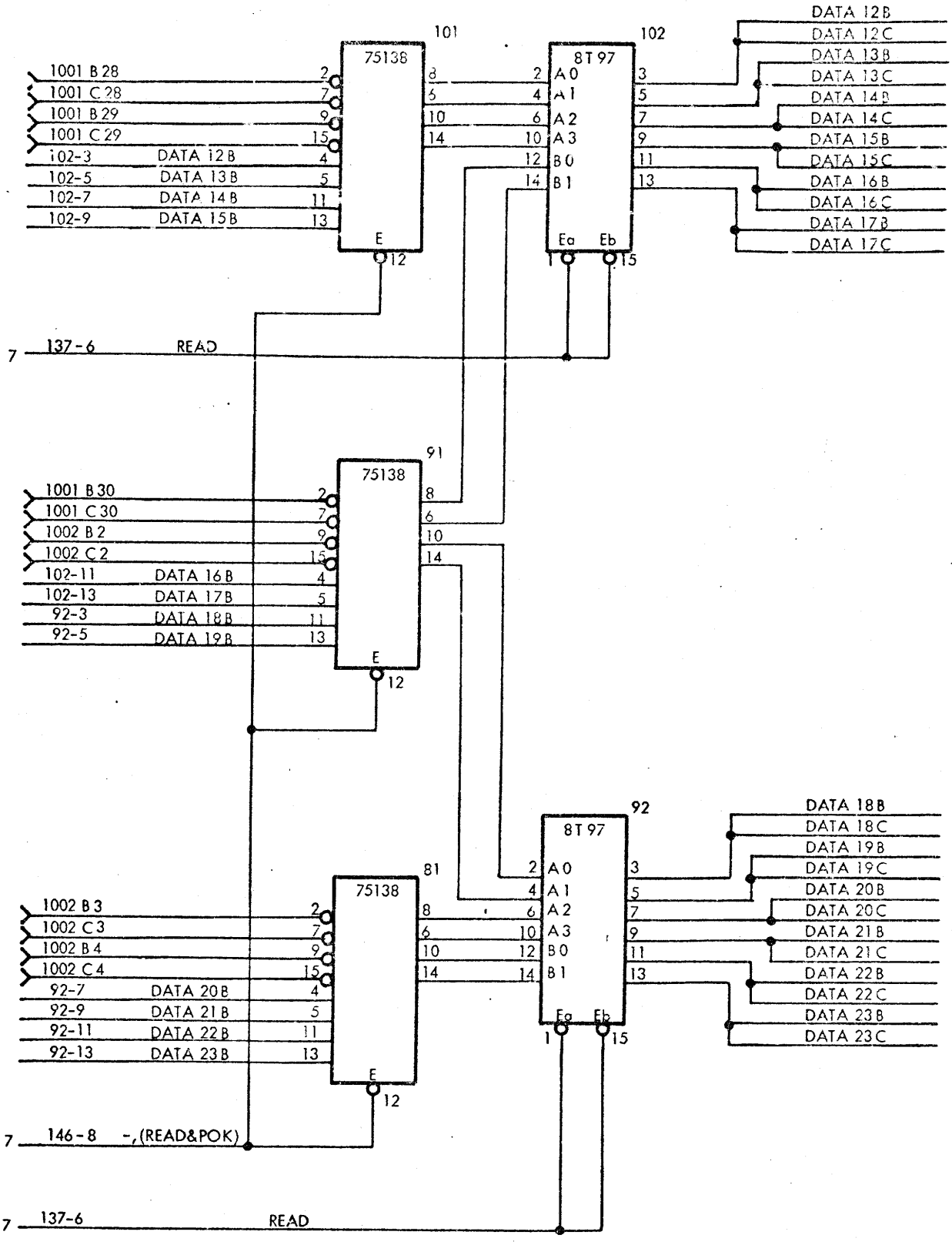
⇨ DIRECTION OF DATA WHEN WRITING INTO MEMORY.

⇦ DIRECTION OF DATA WHEN READING FROM MEMORY.

GATES DRAWN IN DOTTED LINES ARE CONTROL GATES.



100576 MVP 100576 ERC



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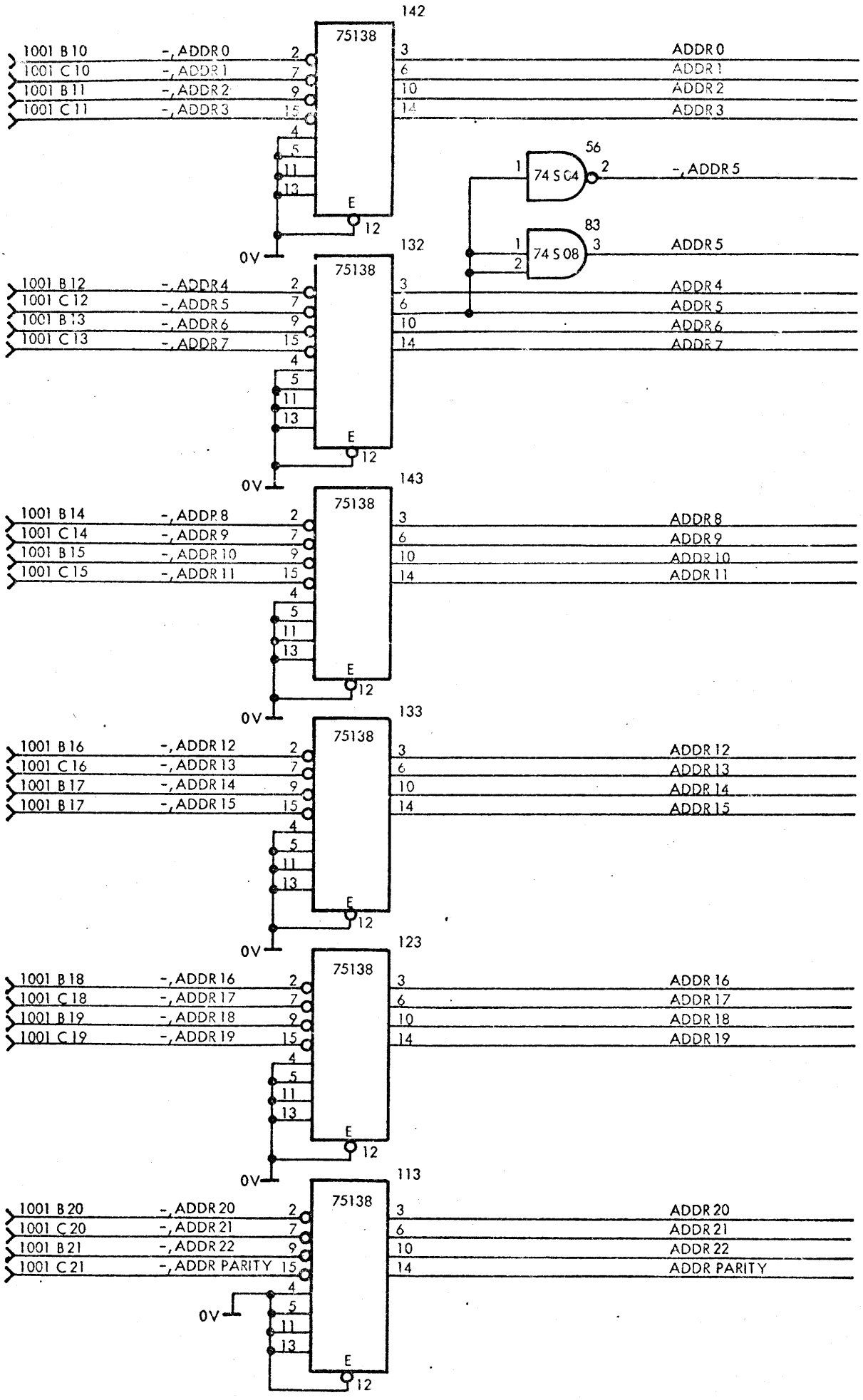


100576 ERC

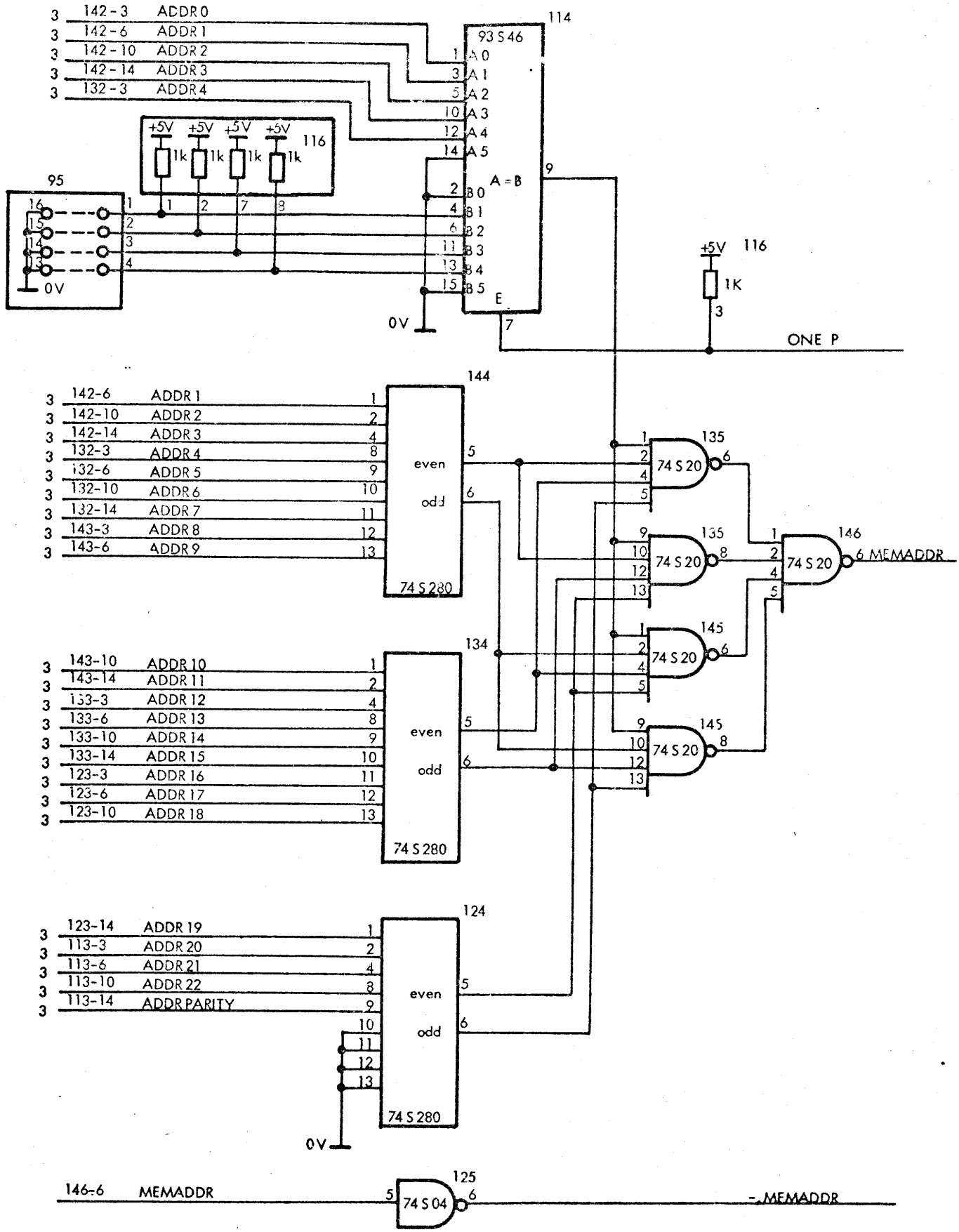
100576 MVP

MCU 802

R 11505

BUS RECEIVER ADDR (0:23)
LOGIC DIAGRAM

MCU003



R 11506

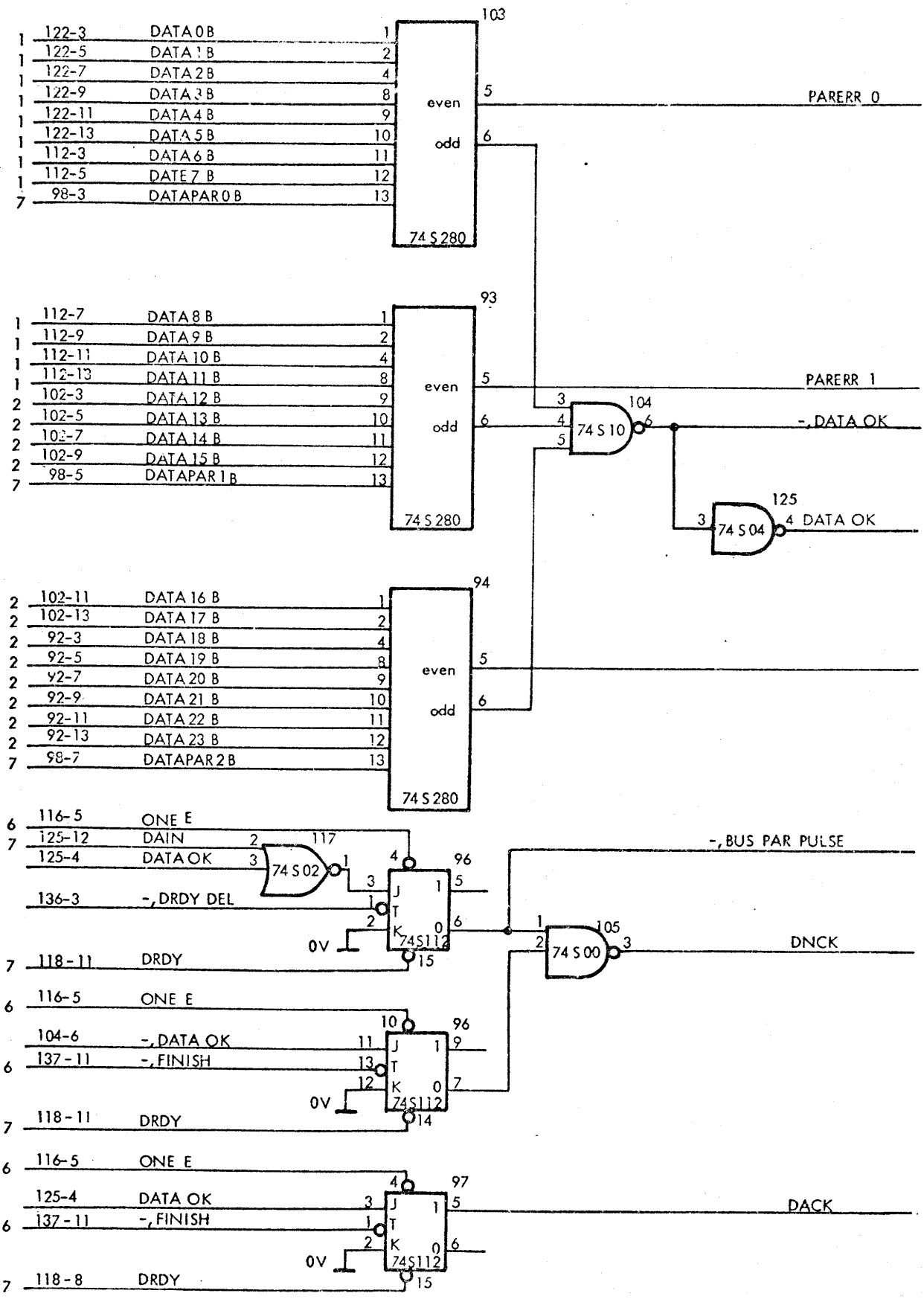
100576 MVP 100576 ERC

MCU 802

R 11591

ADDRESS - PARITY, AND MEMORY DEVICE NUMBER CONTROL LOGIC DIAGRAM

MCU004

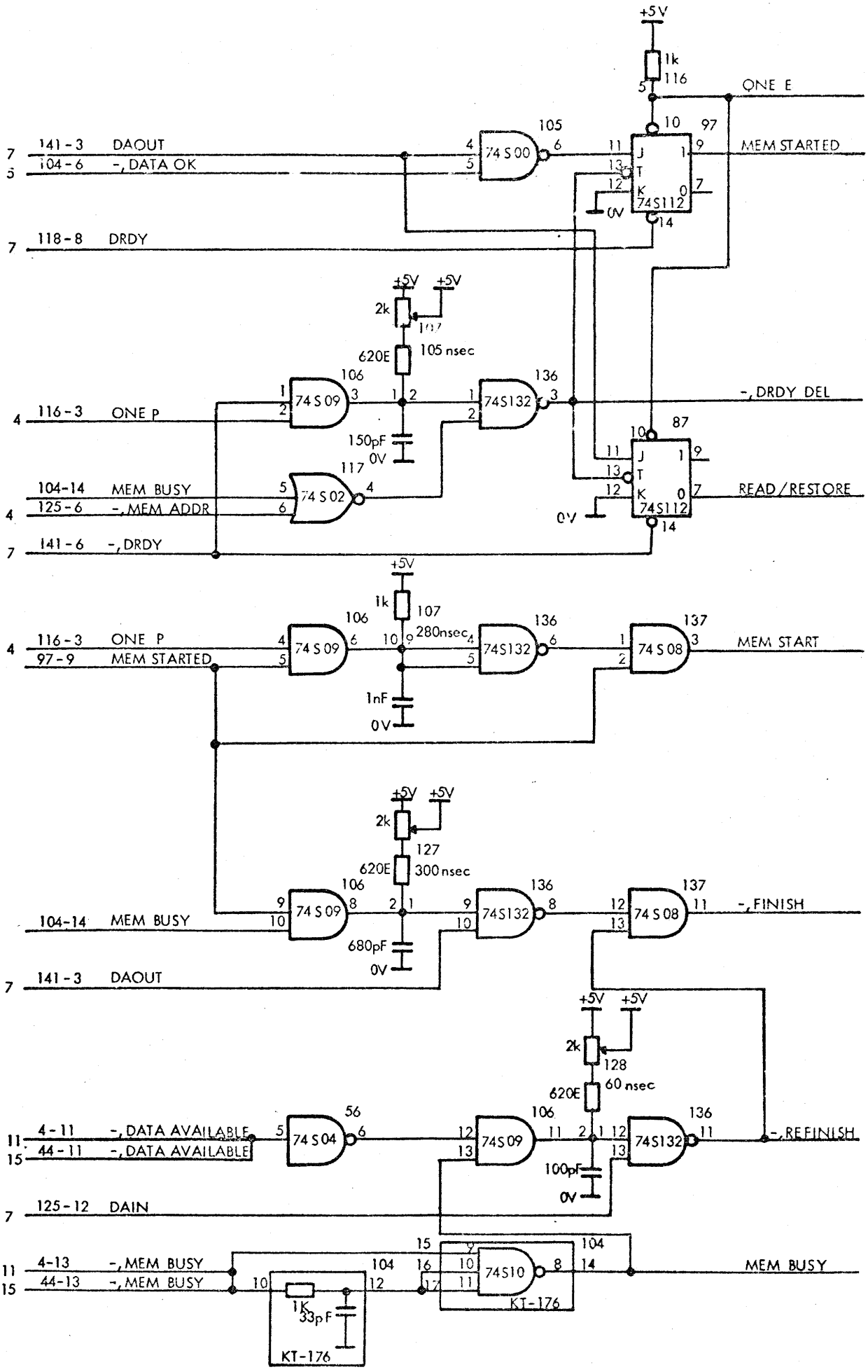


MCU 802

R 11592

DATAPARITYCHECKERS and DACK-/DNCK-CIRCUITS
LOGIC DIAGRAM

MCU 005



R 11504

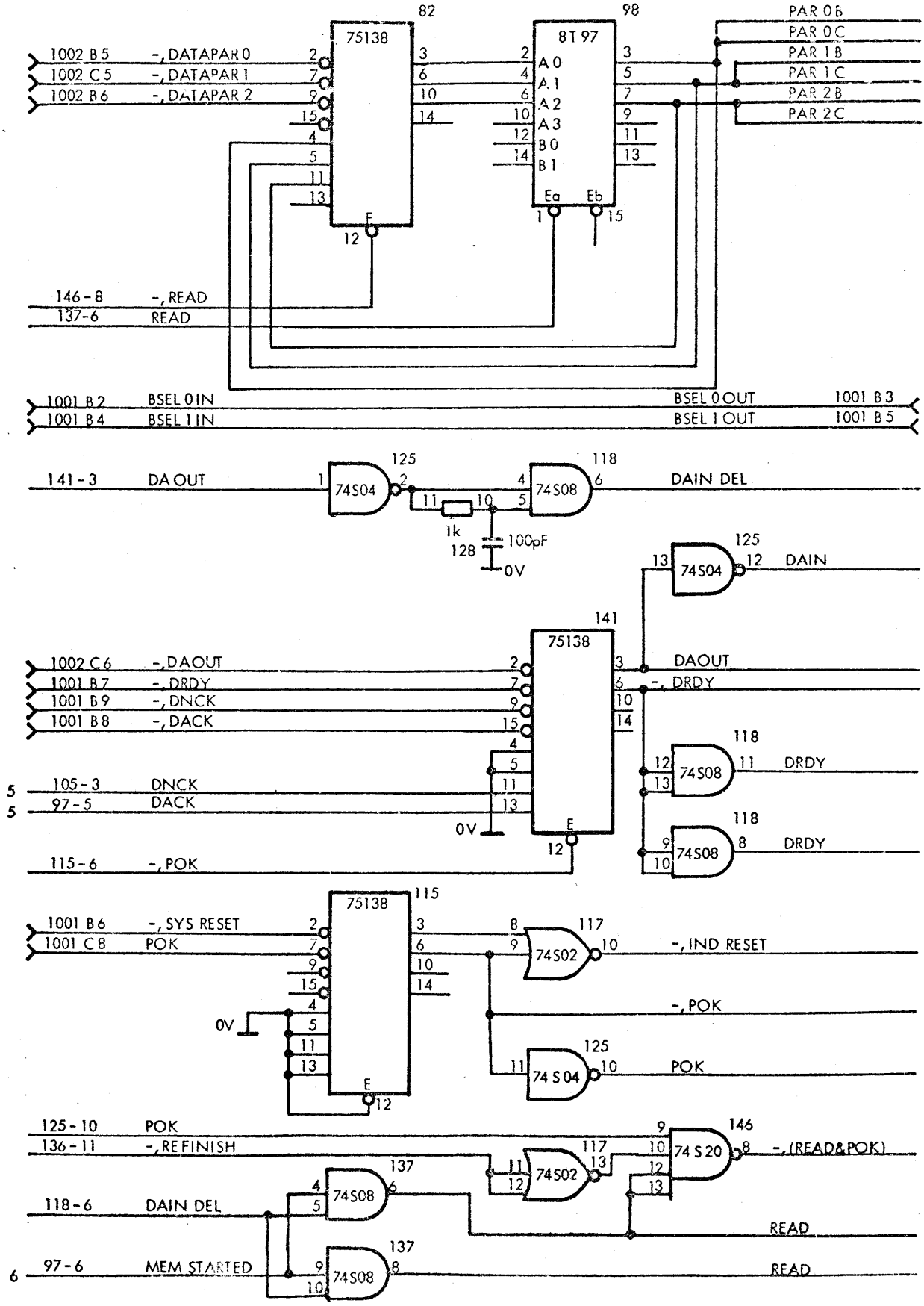
100576 MVP 100576 ERC

MCU 802

R 11593

CONTROL LOGIC 1
LOGIC DIAGRAM

MCU006



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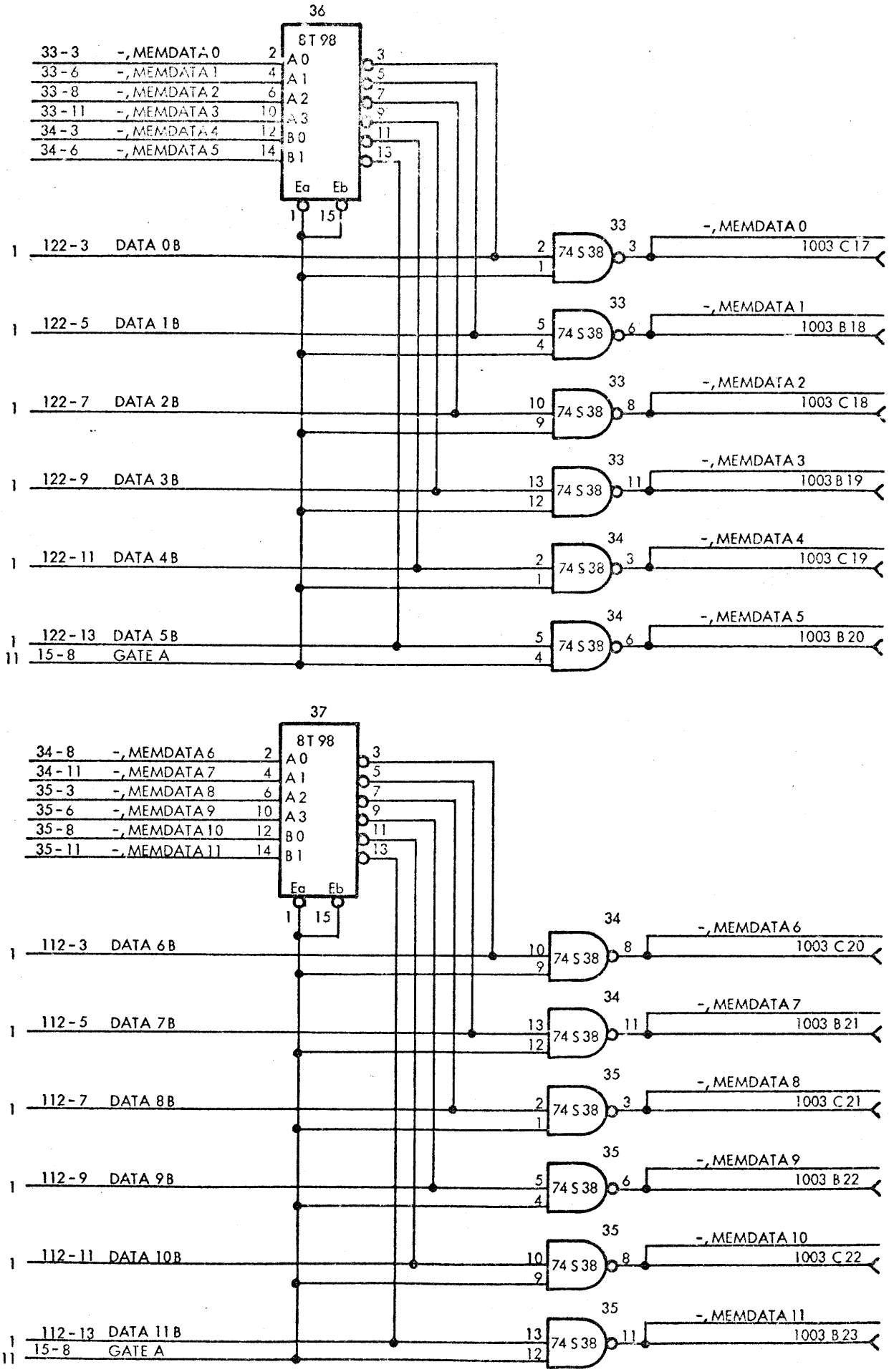
MCU 802

CONTROL LOGIC 2
LOGIC DIAGRAM

MCU007

R 11509



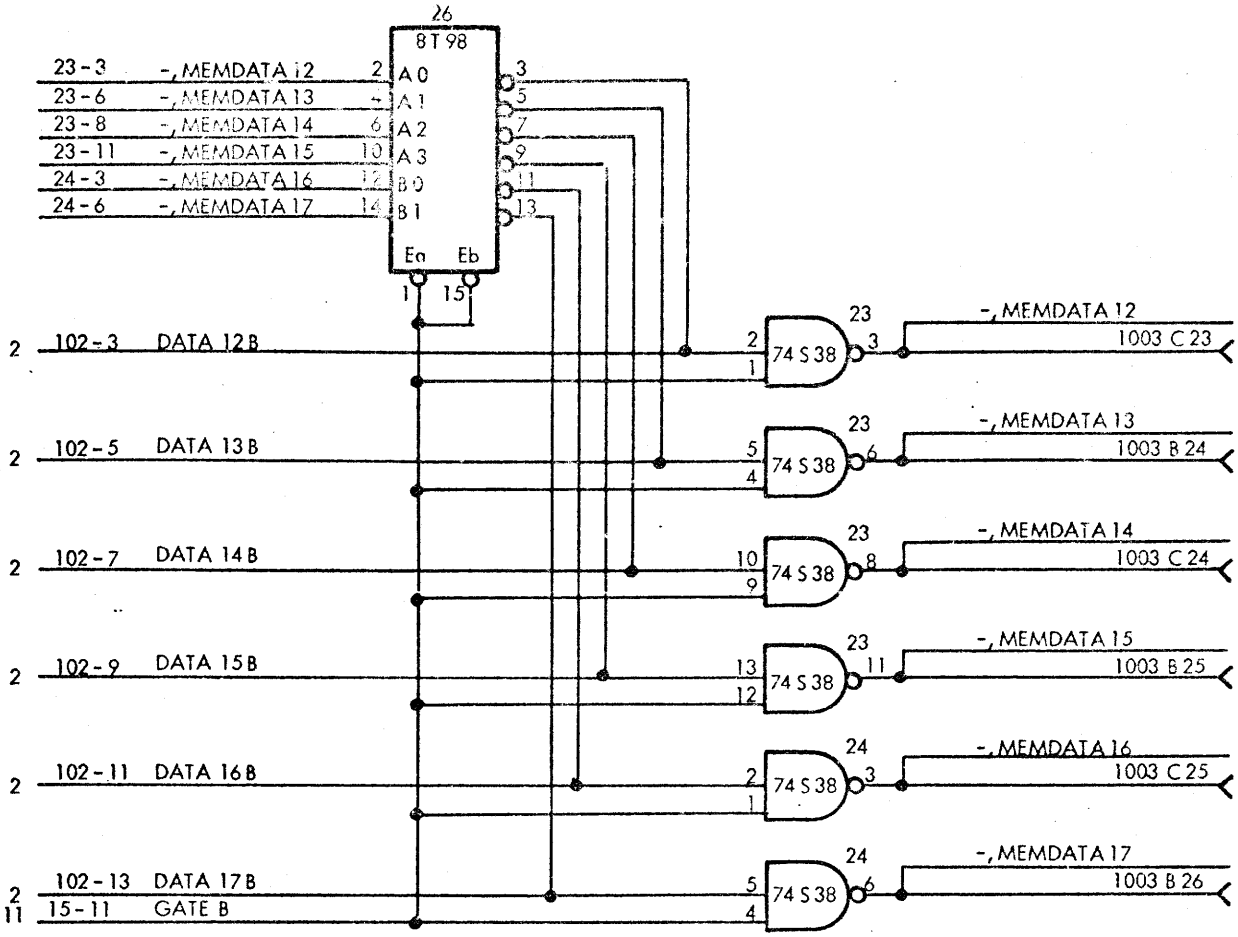
100576 MVP 100576ERC

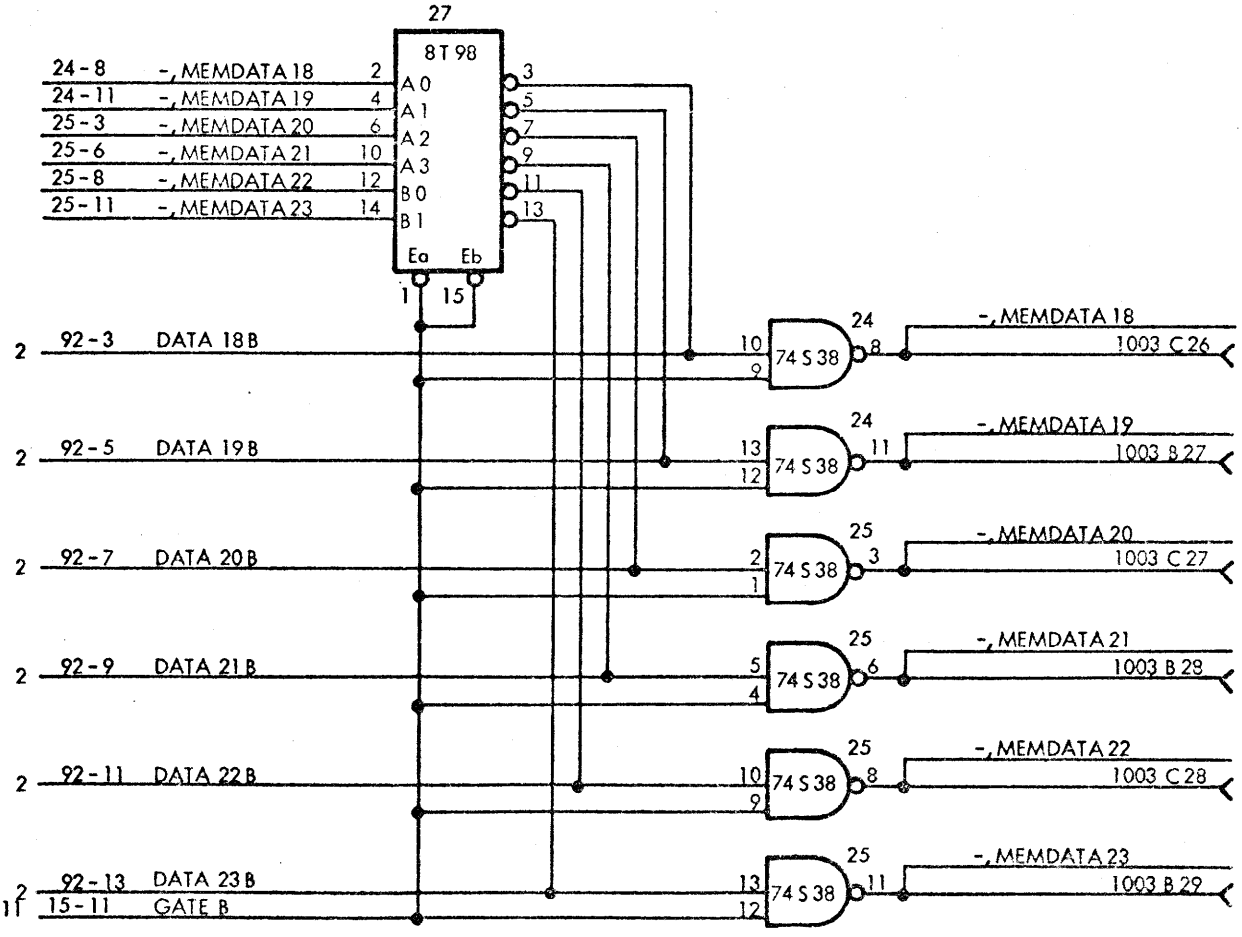
MCU 802

R11510

DATA-TRANSMITTERS/RECEIVERS (0:11)2
LOGIC DIAGRAM

MCU008





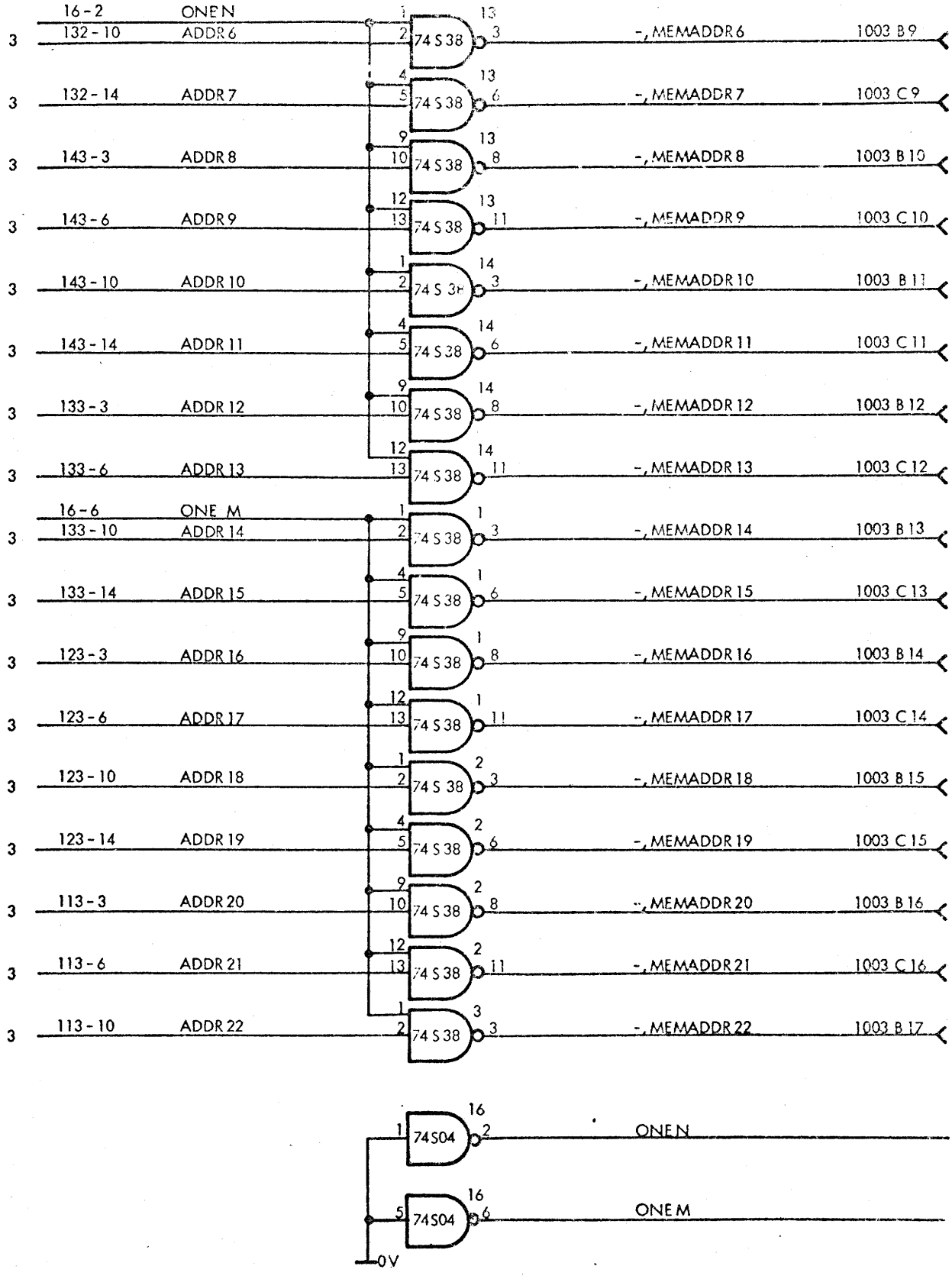
100576 MVP 100576 ERC

MCU 802

R 11511

DATA - TRANSMITTER/RECEIVERS (12:23) 2
LOGIC DIAGRAM

MCU009



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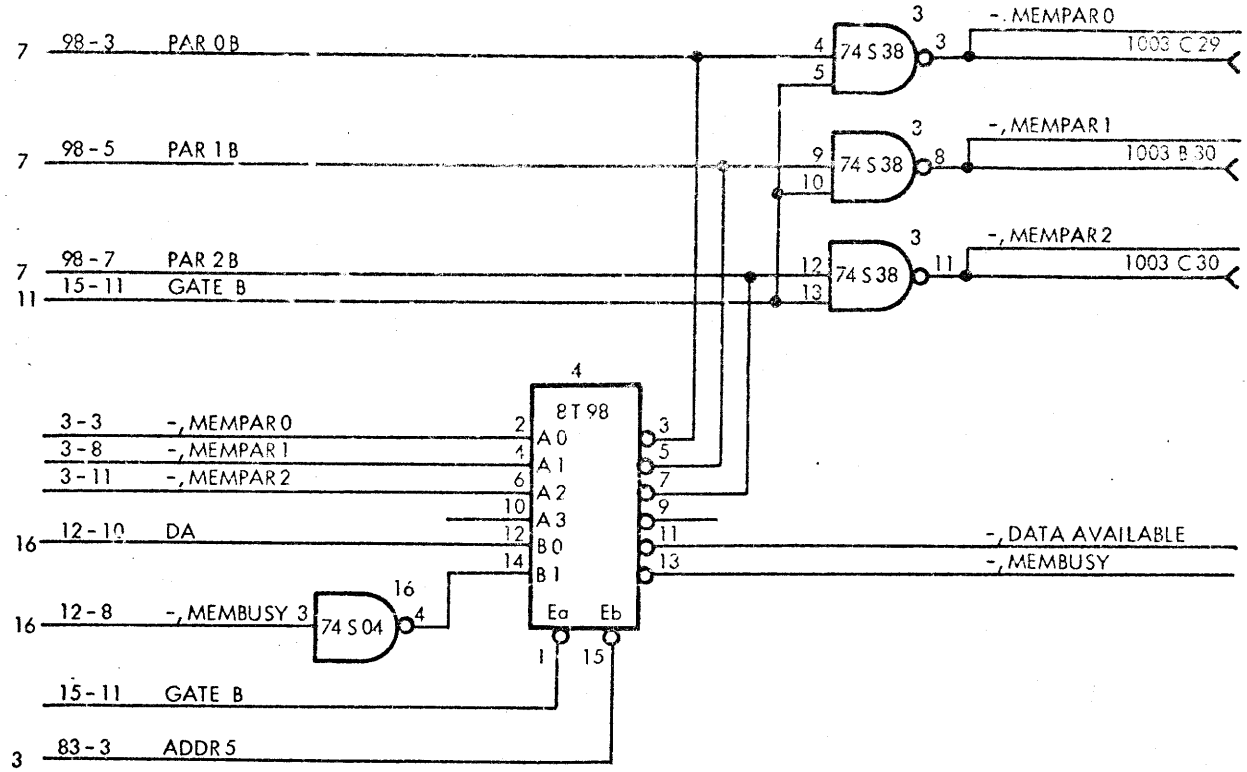

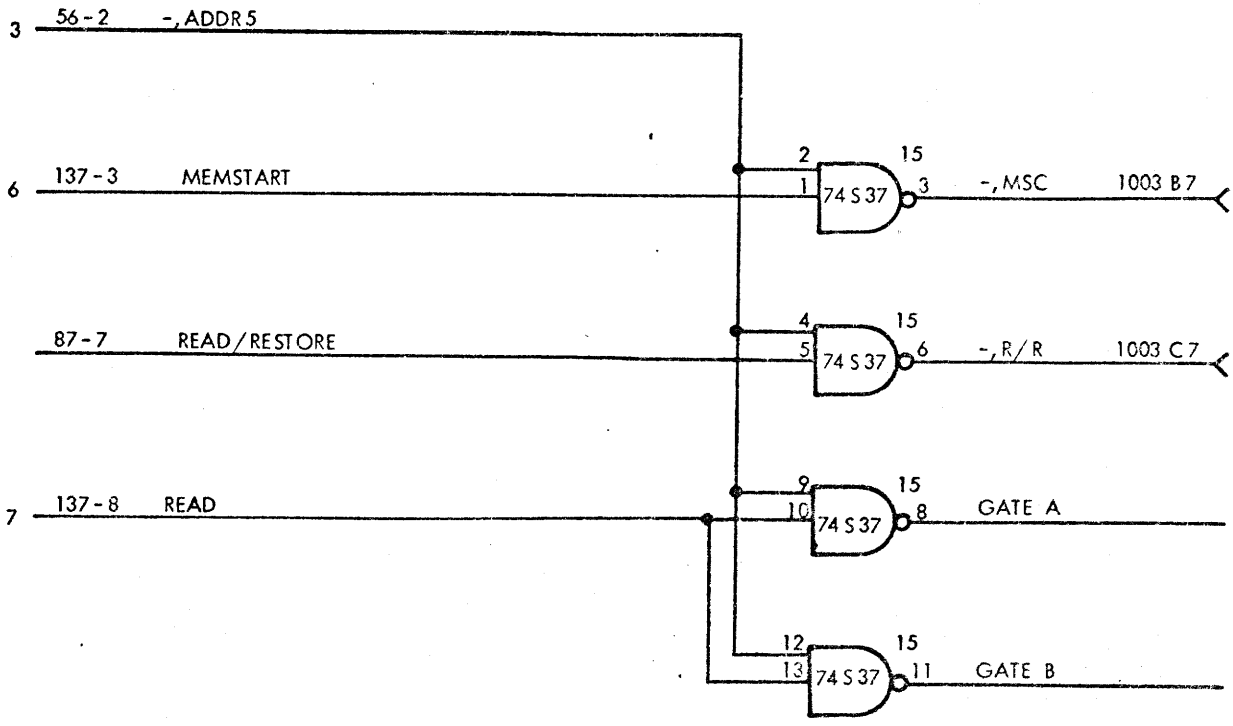

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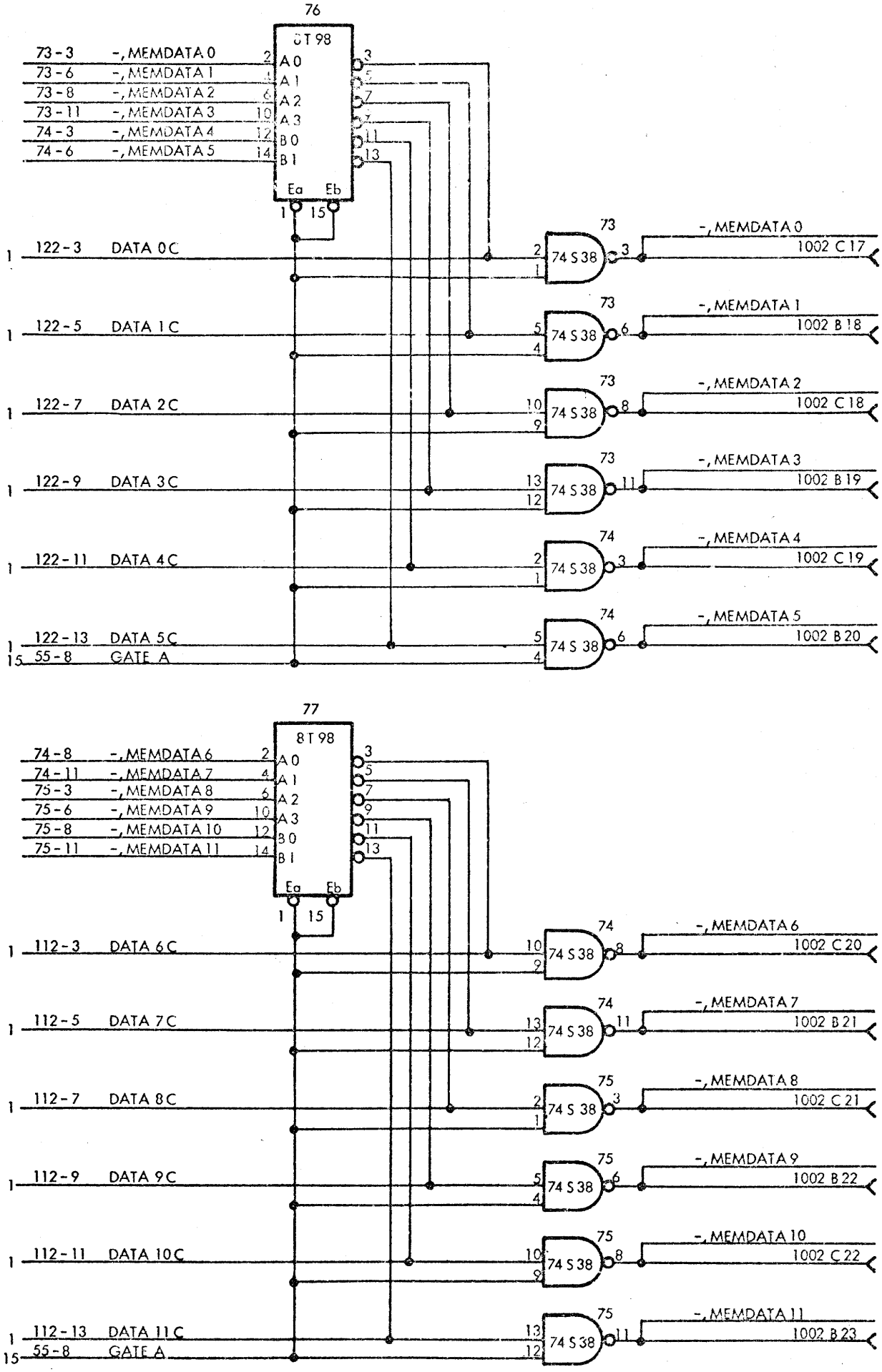

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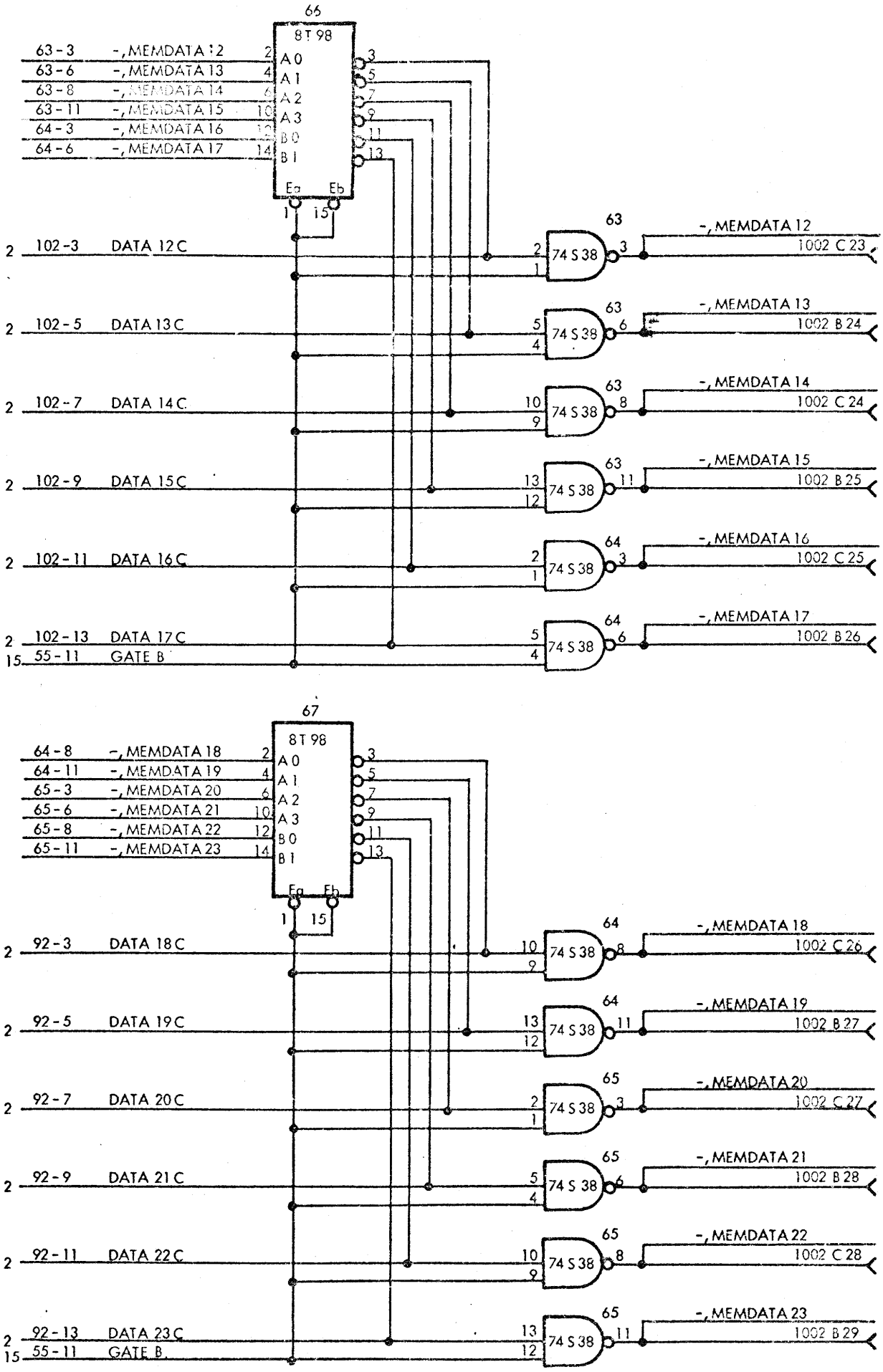

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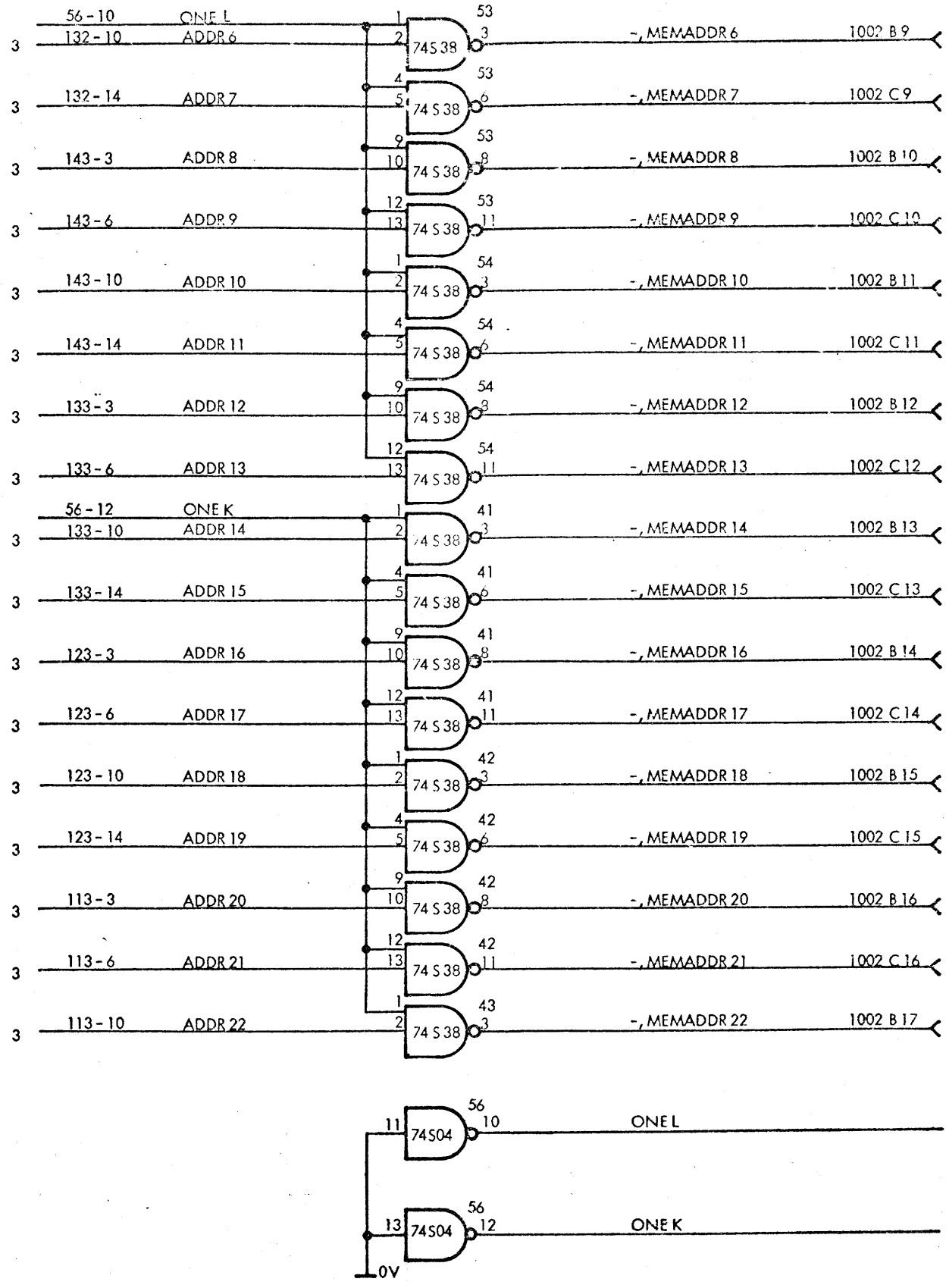


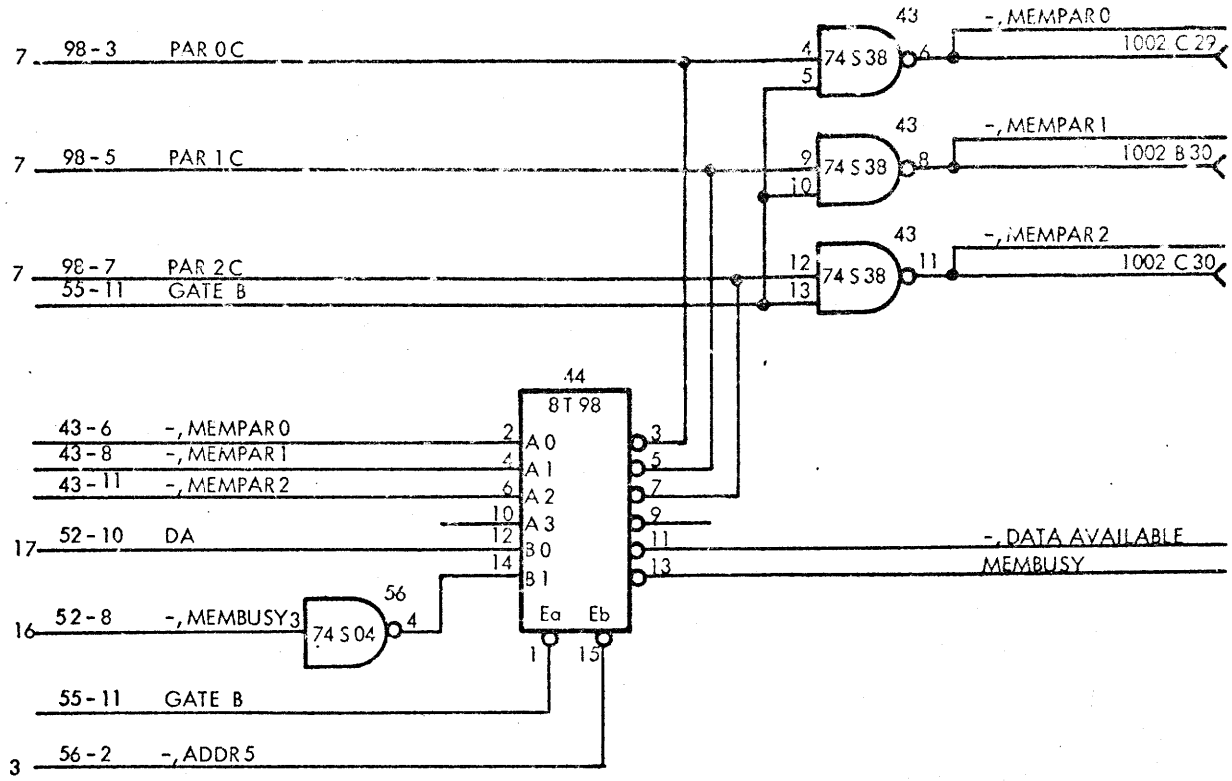
100576 MVP 100576 ERC

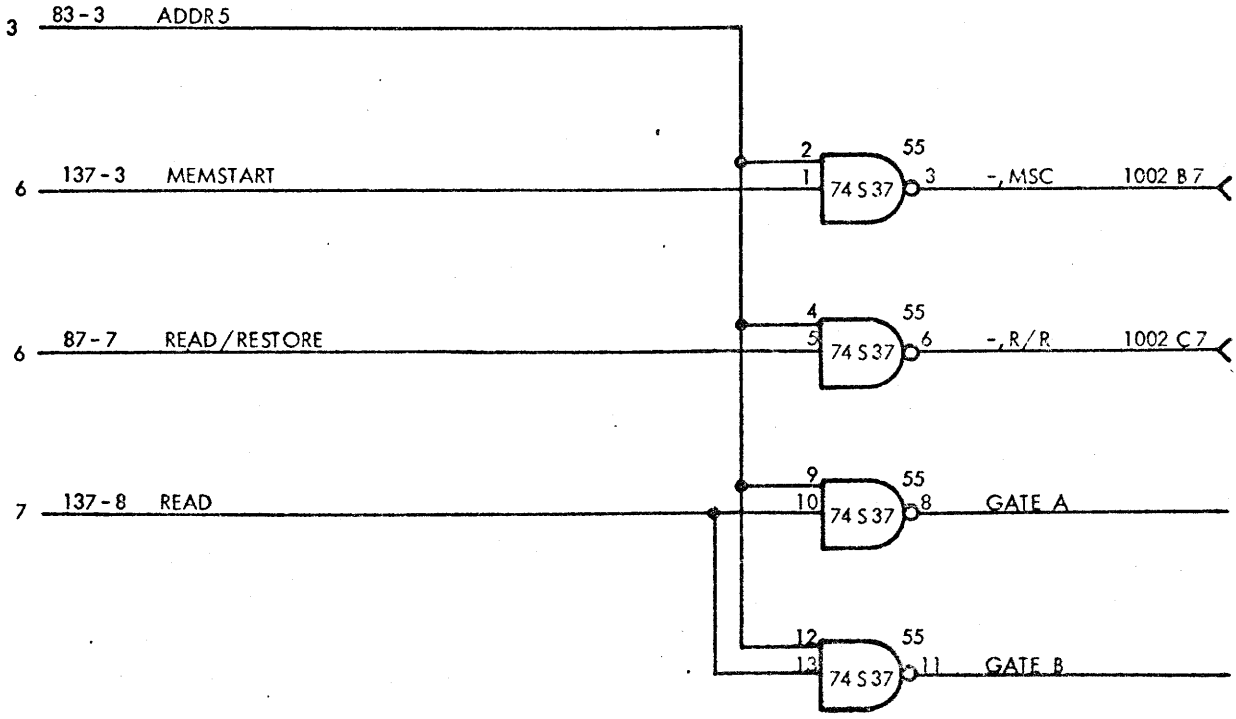
MCU 802

R11516

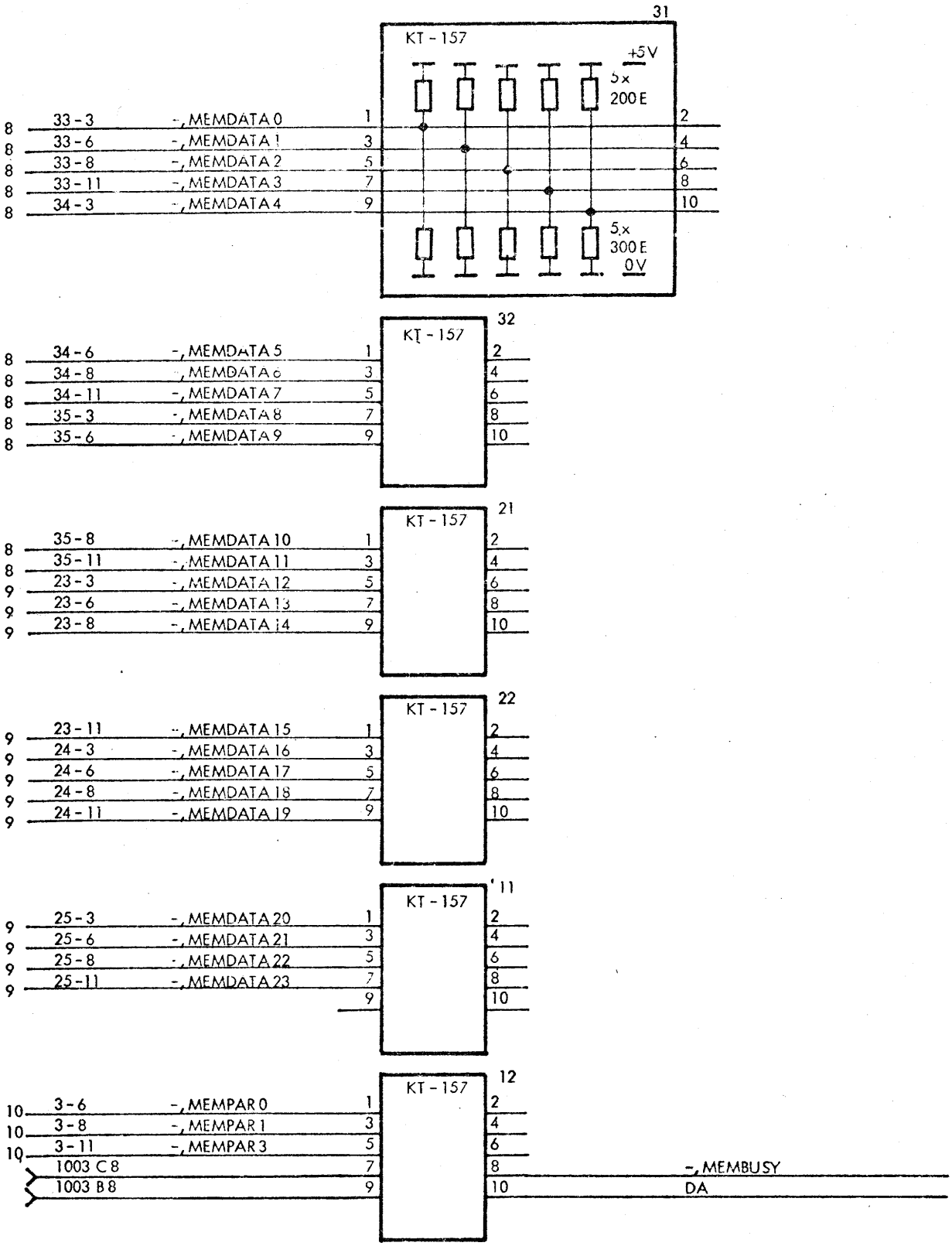
ADDRESS TRANSMITTERS 1
LOGIC DIAGRAM

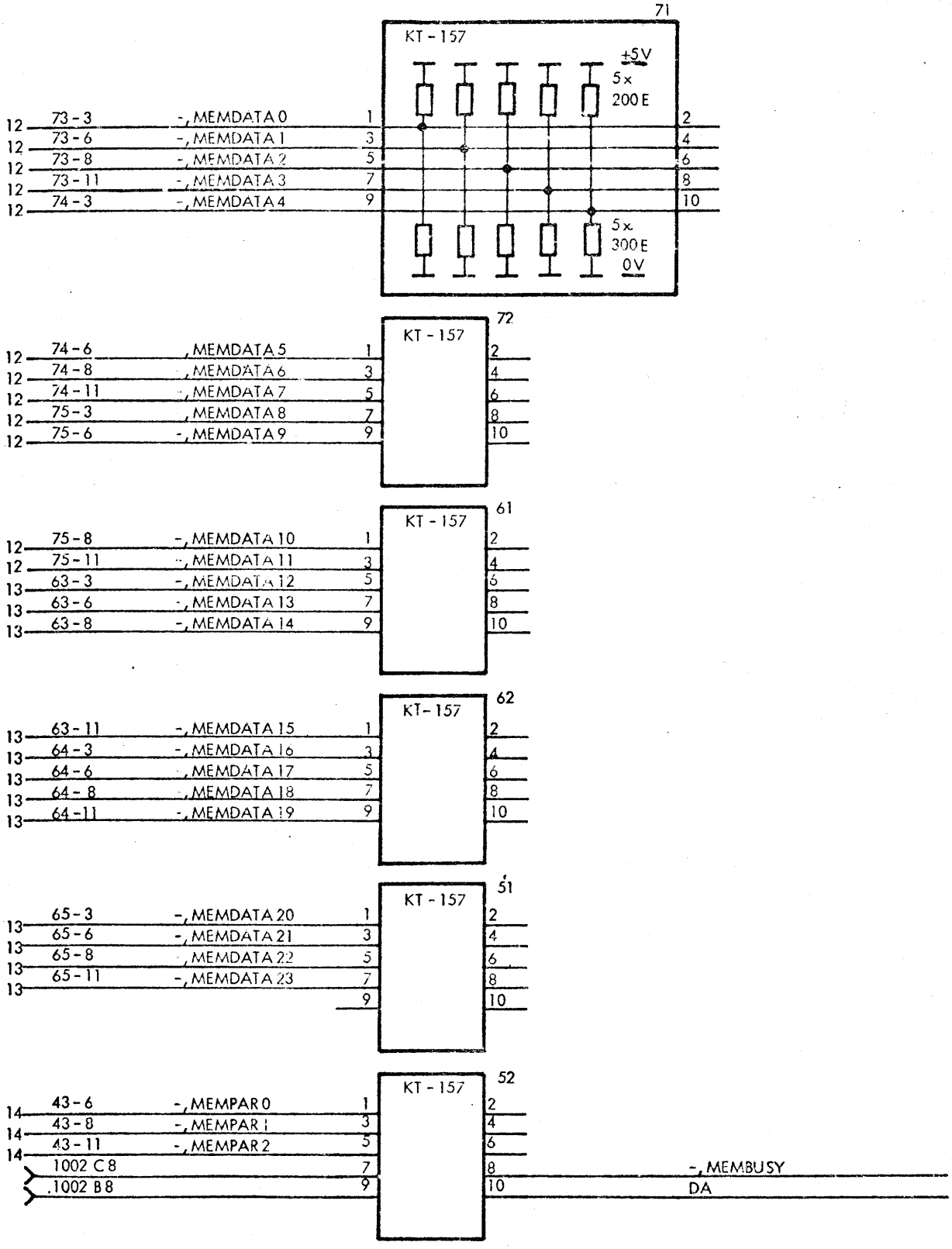
MCU014





100576MVP 100576 ERC


31
KT - 157
+5V
5x
200 E
5x
300 E
0V
8 33 - 3 -, MEMDATA 0 1
8 33 - 6 -, MEMDATA 1 3
8 33 - 8 -, MEMDATA 2 5
8 33 - 11 -, MEMDATA 3 7
8 34 - 3 -, MEMDATA 4 9
2 4 6 8 10
32
KT - 157
8 34 - 6 -, MEMDATA 5 1
8 34 - 8 -, MEMDATA 6 3
8 34 - 11 -, MEMDATA 7 5
8 35 - 3 -, MEMDATA 8 7
8 35 - 6 -, MEMDATA 9 9
2 4 6 8 10
21
KT - 157
8 35 - 8 -, MEMDATA 10 1
8 35 - 11 -, MEMDATA 11 3
9 23 - 3 -, MEMDATA 12 5
9 23 - 6 -, MEMDATA 13 7
9 23 - 8 -, MEMDATA 14 9
2 4 6 8 10
22
KT - 157
9 23 - 11 -, MEMDATA 15 1
9 24 - 3 -, MEMDATA 16 3
9 24 - 6 -, MEMDATA 17 5
9 24 - 8 -, MEMDATA 18 7
9 24 - 11 -, MEMDATA 19 9
2 4 6 8 10
11
KT - 157
9 25 - 3 -, MEMDATA 20 1
9 25 - 6 -, MEMDATA 21 3
9 25 - 8 -, MEMDATA 22 5
9 25 - 11 -, MEMDATA 23 7
9
2 4 6 8 10
12
KT - 157
10 3 - 6 -, MEMPAR 0 1
10 3 - 8 -, MEMPAR 1 3
10 3 - 11 -, MEMPAR 3 5
1003 C 8 7
1003 B 8 9
2 4 6 8 10
-, MEMBUSY
DA

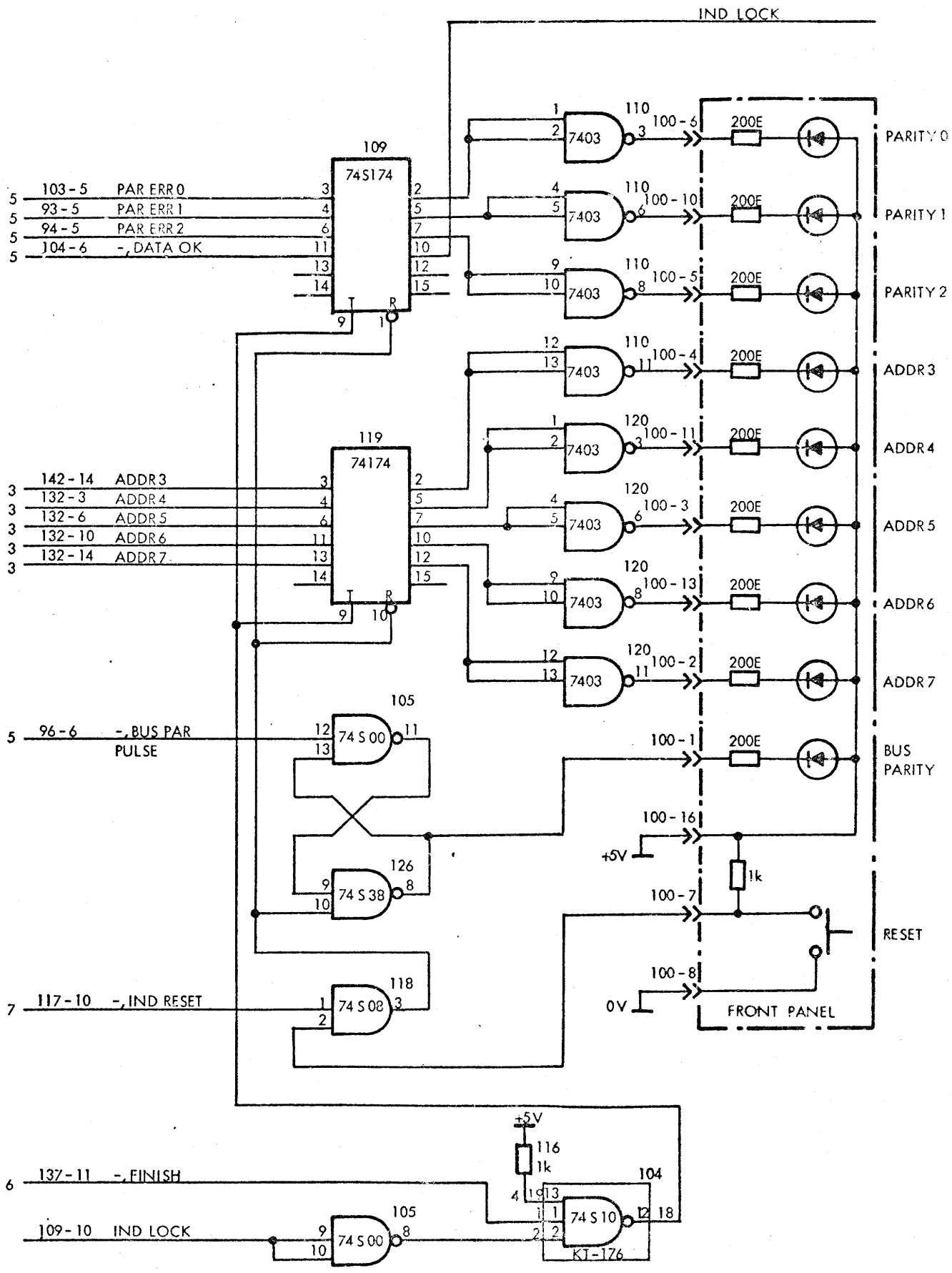


MCU 802

R11519

SIGNAL TERMINATION
LOGIC DIAGRAM

MCU017



R/1520

100576 ERC

100576 MVP

MCU 802

R 11594

ERROR INDICATION LOGIC DIAGRAM

MCU018

Connection between MCU 802 and MEM 801

MEM 801 housed in MCH 801

No.	Signal name in MCU 802	Direction	Pin No. on RC 8000 board	Pin No. on 117 pol ELCO Signal	Pin No. on 117 pol ELCO Ground		Pin No. into MEM CHASSIS	Pin No. out from pos 5 in MEM	Pin No. in Chain in MCH 801	Signal name in MEM 801
							5 B-49	5 B-48	B - 61	A 17
1	MEMADDR 6	→	1003 or 1002 B 9	E 1	E 2		- 47	- 50	- 69	A 16
2	- 7	→	- C 9	E 3	E 4		- 51	- 52	- 62	A 15
3	- 8	→	- B 10	E 5	E 6		- 55	- 56	- 67	A 14
4	- 9	→	- C 10	E 7	F 7		- 81	- 82	- 81	A 13
5	- 10	→	- B 11	F 6	F 5		- 77	- 78	- 79	A 12
6	- 11	→	- C 11	F 4	F 3		- 73	- 74	- 77	A 11
7	- 12	→	- B 12	F 2	F 1		- 69	- 70	- 75	A 10
8	- 13	→	- C 12	H 2	H 3		- 63	- 64	- 74	A 9
9	- 14	→	- B 13	H 4	H 5		- 65	- 66	- 73	A 8
10	- 15	→	- C 13	H 6	H 7		- 61	- 62	- 71	A 7
11	- 16	→	- B 14	J 7	J 6		- 59	- 60	- 72	A 6
12	- 17	→	- C 14	J 5	J 3		- 79	- 80	- 82	A 5
13	- 18	→	- B 15	J 2	J 1		- 75	- 76	- 80	A 4
14	- 19	→	- C 15	K 1	K 2		- 57	- 58	- 70	A 3
15	- 20	→	- B 16	K 6	K 7		- 71	- 72	- 78	A 2
16	- 21	→	- C 16	M 1	M 2		- 67	- 68	- 76	A 1
17	- 22	→	- B 17	M 6	M 7		- 53	- 54	- 68	A 0
18	MEMDATA 0	↔	1003 or 1002 C 17	N 7	N 6		0 A-41 and 47			Data in/out bit 1
19	- 1	↔	- B 18	N 5	N 3		- -39 - 49			- - bit 2
20	- 2	↔	- C 18	N 2	N 1		- -31 - 45			- - bit 3
21	- 3	↔	- B 19	P 2	P 3		- -25 - 55			- - bit 4
22	- 4	↔	- C 19	P 4	P 5		- -37 - 53			- - bit 5
23	- 5	↔	- B 20	P 6	P 7		- -27 - 51			- - bit 6
24	- 6	↔	- C 20	R 7	R 6		- -23 - 57			- - bit 7
25	- 7	↔	- B 21	R 5	R 4		- -19 - 59		Pos(1 : 4)	- - bit 8
26	- 8	↔	- C 21	R 3	R 2		- -17 - 67			- - bit 12
27	- 9	↔	- B 22	R 1	S 1		- -15 - 65			- - bit 13
28	- 10	↔	- C 22	S 2	S 3		- -11 - 63			- - bit 14
29	- 11	↔	- B 23	S 4	S 5		- -13 - 69			- - bit 15
30	- 12	↔	- C 23	S 6	S 7		- - 9 - 71			- - bit 16
31	- 13	↔	- B 24	T 7	T 6		- - 7 - 73			- - bit 17
32	- 14	↔	- C 24	T 5	T 4		- -35 - 79			- - bit 18
33	- 15	↔	- B 25	T 3	T 2		- -29 - 77			- - bit 19
34	- 16	↔	- C 25	T 1	U 1		9 A-80 - 47	5 B-24		- - bit 1
35	- 17	↔	- B 26	U 2	U 3		- -74 - 49	- - 23		- - bit 2
36	- 18	↔	- C 26	U 4	U 5		- -37 - 45	- - 18		- - bit 3
37	- 19	↔	- B 27	U 6	U 7		- -36 - 55	- - 17		- - bit 4
38	- 20	↔	- C 27	V 7	V 6		- -72 - 53	- - 22	Pos(6 : 9)	- - bit 5
39	- 21	↔	- B 28	V 5	V 4		- -35 - 51	- - 16		- - bit 6
40	- 22	↔	- C 28	V 3	V 2		- -33 - 57	- - 14		- - bit 7
41	- 23	↔	- B 29	V 1	X 1		- -31 - 59	- - 12		- - bit 8
42	MEMPAR 0	↔	- C 29	X 2	X 3		OA -21 - 61		Pos(1 : 4)	- - bit 9
43	MEMPAR 1	↔	- B 30	X 4	X 5		OA -33 - 75			- - bit 20
44	ME MPAR 2	↔	- C 30	X 6	X 7		10 -34 - 61	5 B - 15	Pos(6 : 9)	- - bit 9
45	DATA available	←	- B 8	D 4	D 3		5 B -1		B - 1	DATA available
46	MEM BUSY	←	- C 8	D 2	D 1		5 A-84		B - 35	MEM BUSY
47	MSC	→	- B 7	C 7	D 7		5 B -37	5 B- 38	B - 37	MSC
48	RIR	→	- C 7	D 6	D 5		5 B-29 and 25		B - 25	RIR 1
									B - 29	RIR 2
49	Spare Data	↔	- B 6	C 3	C 4		9 A-32 and 67	5 B- 13	Pos(1 : 4) and (6 : 9)	Data in/out bit 12
50	- -	↔	- C 6	C 5	C 6		- -29 - 65	- - 10		- - bit 13
	- -	↔	- B 5	B 2	B 1		- -27 - 63	- - 8		- - bit 14
	- -	↔	- C 5	C 1	C 2		- -30 -69	- - 11		- - bit 15
	- -	↔	- B 4	B 6	B 5		- -28 -71	- - 9	pos(6 : 9)	- - bit 16
	- -	↔	- C 4	B 4	B 3		- -25 - 73	- - 7		- - bit 17
	- -	↔	- B 3	A 5	A 6		- -41 - 79	- - 21		- - bit 18
	- -	↔	- C 3	A 7	B 7		- -38 - 77	- -19		- - bit 19
	- -	↔	- C 2	A 3	A 4		- -39 -75	- -20		- - bit 20

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