

Title:

DRAWINGS FOR
CPU 800

 **REGNECENTRALEN**

RC SYSTEM LIBRARY: FALKONERALLE 1 DK-2000 COPENHAGEN F

RCSL No: 30-M33

Edition: 76.11.24.

Author: Aage Jørgensen

Keywords:

RC 8000, Drawings, Central Processing Unit.

Abstract:

This manual contains the drawings of the RC8005, Central Processing Unit, CPU800.

CONTENTS

Drwg. No.

CONTENTS	Drwg. No.
CPU800 CENTRAL PROCESSING UNIT BLOCK DIAGRAM	R 11654
<u>CPU801</u>	
CPU801 BLOCK DIAGRAM	R 11651
CPU INTERCONNECTIONS	R 11373
MASTER CLOCK OSCILLATOR, CLOCK DRIVERS AND CPU SYSTEM RESET CONTROL	R 11374
CPU CLOCK GENERATOR	R 11375
INTERFACE TO OPERATORS CONTROL PANEL AND REMOTE AUTOLOAD	R 11376
INTERFACE TO TECHNICAL CONTROL PANEL	R 11377
AUTOLOAD, POWER RESTART, AND KEY ADDRESS ENCODER .	R 11378
SINGLE MICROINSTRUCTION AND SINGLE INSTRUCTION CONTROL MICROPROGRAM STORE EXAMINE AND EXAMINE NEXT	R 11379
KEY FUNCTION CONTROL	R 11380
MPS ADDRESS SELECTION CONTROL	R 11381
MICRO INSTRUCTION REGISTER	R 11382
MICROINSTRUCTION COUNTER, MIC AND SUBROUTINE RETURN REGISTER, SUBRRTN	R 11383
JUMP ADDRESS REGISTER SPECIAL RETURN ADDRESS REGISTER.	R 11384
ADDRESS TABLE FOR START OF NEXT INSTRUCTION	R 11385
ADDRESS TABLE FOR START OF INSTRUCTION EXECUTION ...	R 11386
MPS ADDRESS SELECTOR, MPS ADDR (0:3)	R 11387
MPS ADDRESS SELECTOR, MPS ADDR (4:7)	R 11388

CONTENTS	Drwg. No.
MPS ADDRESS SELECTOR, MPS ADDR (8:11)	R 11389
MICRO PROGRAM STORE, WORDS (0:511), BITS (0:15)	R 11390
MICRO PROGRAM STORE, WORDS (0:511), BITS (16:31)	R 11391
MICRO PROGRAM STORE, WORDS (512:1023), BITS (0:15) ...	R 11392
MICRO PROGRAM STORE, WORDS (512:1023), BITS (16:31) ...	R 11393
MICRO PROGRAM STORE, WORDS (1024:1535), BITS (0:15) ...	R 11394
MICRO PROGRAM STORE, WORDS (1024:1535), BITS (16:31) ...	R 11395
MICRO PROGRAM STORE, WORDS (1536:2048), BITS (0:15) ...	R 11396
MICRO PROGRAM STORE, WORDS (1536:2048), BITS (16:31) ...	R 11397
MICROPROGRAM STORE OUTPUT, MPS (0:7)	R 11398
MICROPROGRAM STORE OUTPUT, MPS (8:15)	R 11399
MICROPROGRAM STORE OUTPUT, MPS (16:23)	R 11400
MICROPROGRAM STORE OUTPUT, MPS (24:31)	R 11401
MPS PARITY CONTROL	R 11402
 <u>CPU802</u>	
CPU802 BLOCK DIAGRAM	R 11652
GENERAL REGISTERS A(-1)	R 11403
GENERAL REGISTERS A(0:7)	R 11404
GENERAL REGISTERS A(8:15)	R 11405
GENERAL REGISTERS A(16:23)	R 11406
GENERAL REGISTERS B(0:7)	R 11407
GENERAL REGISTERS B(8:15)	R 11408
GENERAL REGISTERS B(16:23)	R 11409

CONTENTS

Drwg. No.

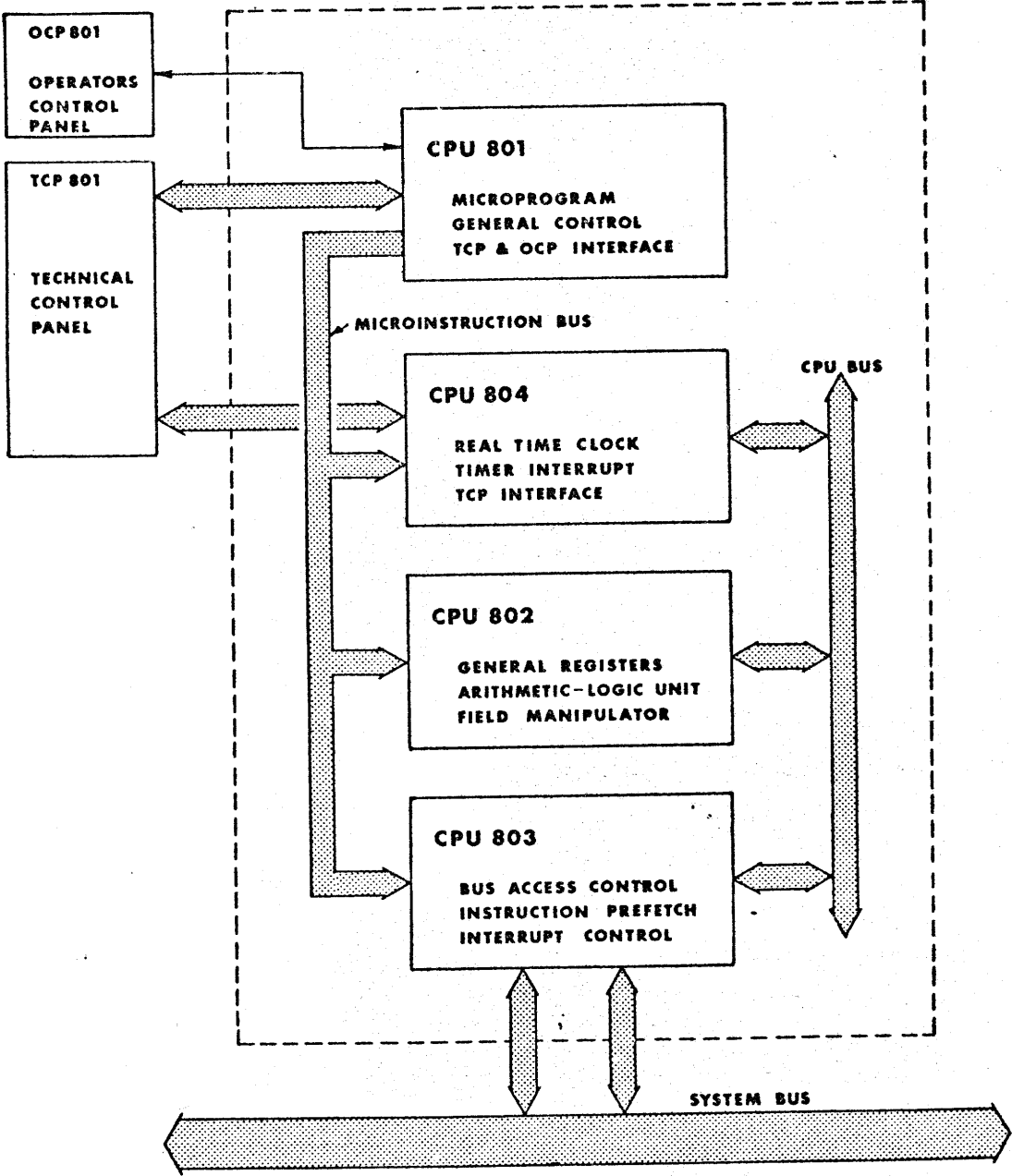
CONTENTS	Drwg. No.
MULTIPLEXERS FOR OPERAND 2 BUS (0:7)	R 11410
MULTIPLEXERS FOR OPERAND 2 BUS (8:15)	R 11411
MULTIPLEXERS FOR OPERAND 2 BUS (16:23)	R 11412
ARITHMETIC LOGIC FUNCTION UNIT	R 11413
ARITHMETIC LOGIC FUNTION UNIT	R 11414
FIELD MANIPULATOR BITS (0:7)	R 11415
FIELD MANIPULATOR BITS (8:11)	R 11416
FIELD MANIPULATOR BITS (12:23)	R 11417
SUM SHIFTER AND MULTIPLEXERS FOR RESULT BUS (-1:7) ...	R 11418
SUM SHIFTER AND MULTIPLEXERS FOR RESULT BUS (8:15) ...	R 11419
SUM SHIFTER AND MULTIPLEXERS FOR RESULT BUS (16:23) ..	R 11420
Q-REGISTER	R 11421
SEQUENTIAL COUNTER, OPERAND INDEX REGISTER AND INSTRUCTION REGISTER BITS 6, 7, 10, 11	R 11422
CPU BUS REGISTER AND CPU STATUS (0:5)	R 11423
DRIVERS FOR CPU BUS	R 11424
OPERAND 1 ADDRESS SELECTOR	R 11425
OPERAND 2 ADDRESS SELECTOR	R 11426
GENERAL REGISTER B ADDRESS SELECTOR AND OPERAND 2 BUS CONTROL	R 11427
REGISTER CLOCK CONTROL	R 11428
ARITHMETIC LOGIC UNIT CONTROL	R 11429
SHIFT CONTROL AND SHIFT CONDITION REGISTER	R 11430

CONTENTS	Drwg. No.
BIT LOAD AND EXCEPTION LOAD	R 11431
CONDITION DECODING AND CONDITION REGISTER	R 11432
CONDITION SELECTOR	R 11433
MICROINSTRUCTION REGISTER	R 11434
MICROINSTRUCTION DECODING AND CPU INTERCONNECTIONS ..	R 11435
CPU INTERCONNECTIONS	R 11436
 <u>CPU 803</u>	
CPU 803 BLOCK DIAGRAM	R 11653
DRIVERS FOR CPUBUS(0:5) AND RECEIVERS FOR CPUBUS(0:7)	R 11437
DRIVERS FOR CPUBUS(6:11) AND RECEIVERS FOR CPUBUS(8:15)	R 11438
DRIVERS FOR CPUBUS(12:17) AND RECEIVERS FOR CPUBUS(16:23) ..	R 11439
DRIVERS FOR CPUBUS(18:23)	R 11440
PREFETCH ADDRESS COUNTER AND I/O ADDRESS REGISTER	R 11441
PREFETCH ADDRESS COUNTER AND I/O ADDRESS REGISTER	R 11442
PREFETCH ADDRESS COUNTER AND I/O ADDRESS REGISTER	R 11443
PARITY GENERATOR FOR I/O ADDRESS AND DECODING FOR REGISTER ADDRESS	R 11444
UPPER AND LOWER LIMIT REGISTERS	R 11445
LOWER LIMIT COMPERATOR	R 11446
UPPER LIMIT COMPERATOR	R 11447
DISPLACEMENT REGISTER	R 11448
I/O DATA-IN AND I/O DATA-OUT REGISTERS	R 11449
PARITY GENERATORS AND CHECKERS FOR I/O DATA	R 11450
PREFETCH INSTRUCTION REGISTERS	R 11451
BUS TRANCEIVER FOR ADDRESS	R 11452
BUS TRANCEIVERS FOR DATA	R 11453
BUS TRANCEIVERS FOR CONTROL SIGNALS	R 11454

CONTENTS	Drwg. No.
SOURCE ADDRESS DECODING AND REGISTER CLOCK CONTROL	R 11455
INSTRUCTION PREFETCH CONTROL AND UNIT FUNCTION CONTROL	R 11456
MICROINSTRUCTION REGISTER AND CONDITION SELECTOR...	R 11457
CPU INTERCONNECTIONS	R 11458
CPU INTERCONNECTIONS AND ONE GENERATORS	R 11459
INTERRUPT CONTROL	R 11460
INTERRUPT CONTROL	R 11461
INTERRUPT CONTROL	R 11462
INTERRUPT CONTROL	R 11463
INTERRUPT CONTROL	R 11464
BUS ACCESS CONTROL	R 11465
BUS ACCESS STATUS REGISTERS	R 11466
BUS ACCESS CONTROL	R 11467
 <u>CPU 804</u>	
CPU 804 BLOCK DIAGRAM	R 11683
DRIVERS FOR CPUBUS	R 11468
PRESALER FOR REAL TIME CLOCK TIMER INTERRUPT DISABLE / ENABLE SWITCH	R 11469
REAL TIME CLOCK	R 11470
INTERFACE TO TECHNICAL CONTROL PANEL DATA SWITCHES AND REGISTER SELECT SWITCHES	R 11471
INTERFACE TO TECHNICAL CONTROL PANEL DISPLAY REGISTER AND LAMP DRIVERS	R 11472
CPU INTERCONNECTIONS, MICROINSTRUCTION REGISTER, AND REGISTER ADDRESS DECODING	R 11473

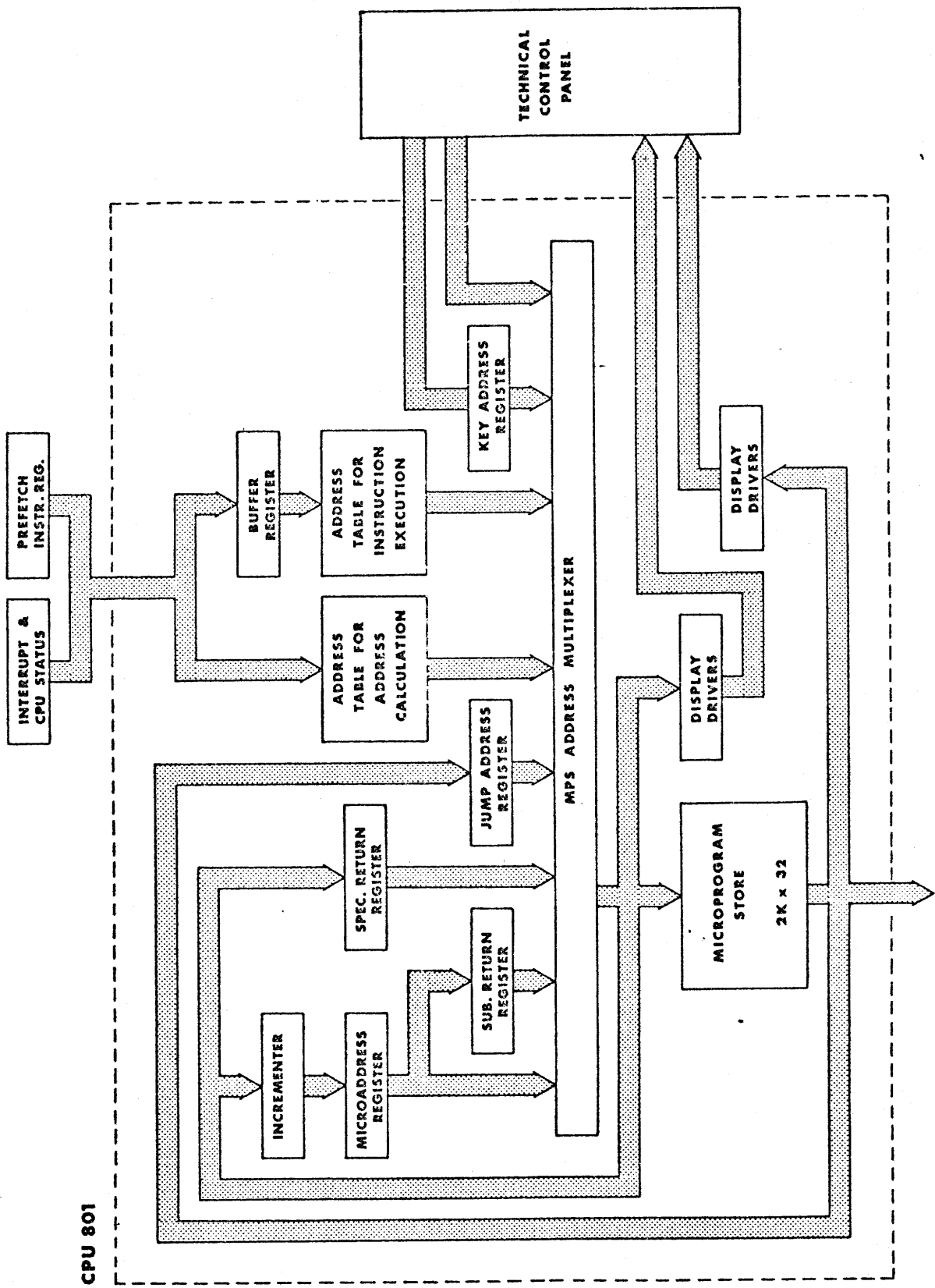
Replaced by Dwg. No. _____
 due to ECN _____
 Replaces Dwg. No. _____
 Design Check _____
 Dwg. Office Check _____
 Drawn by 761110 AOB
 Designed by 761110 AAJ
A/S REGNECENTRALEN
 Unit RC8000
 Dwg. No. R 11654

CPU 800



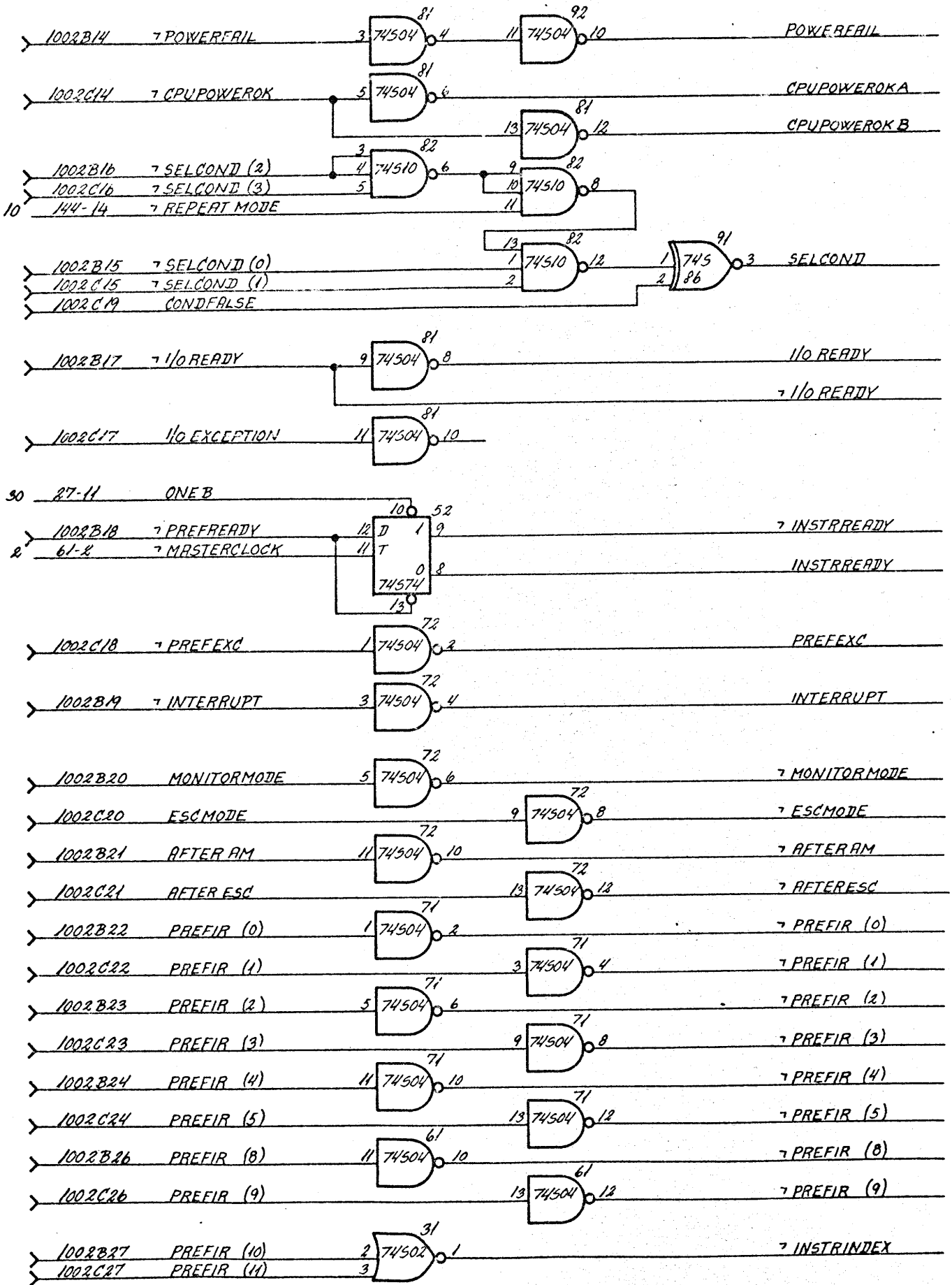
**CPU 800 CENTRAL PROCESSING UNIT
BLOCK DIAGRAM**

RC Sec. VB 149
 A/S RECENTRALEN
 Designed by 761110 AAJ
 Drawn by 761110 AOB
 Dwg. Office
 Design Check
 Repetition Dwg. No.
 due to ECN
 Rep. by Dwg. No.

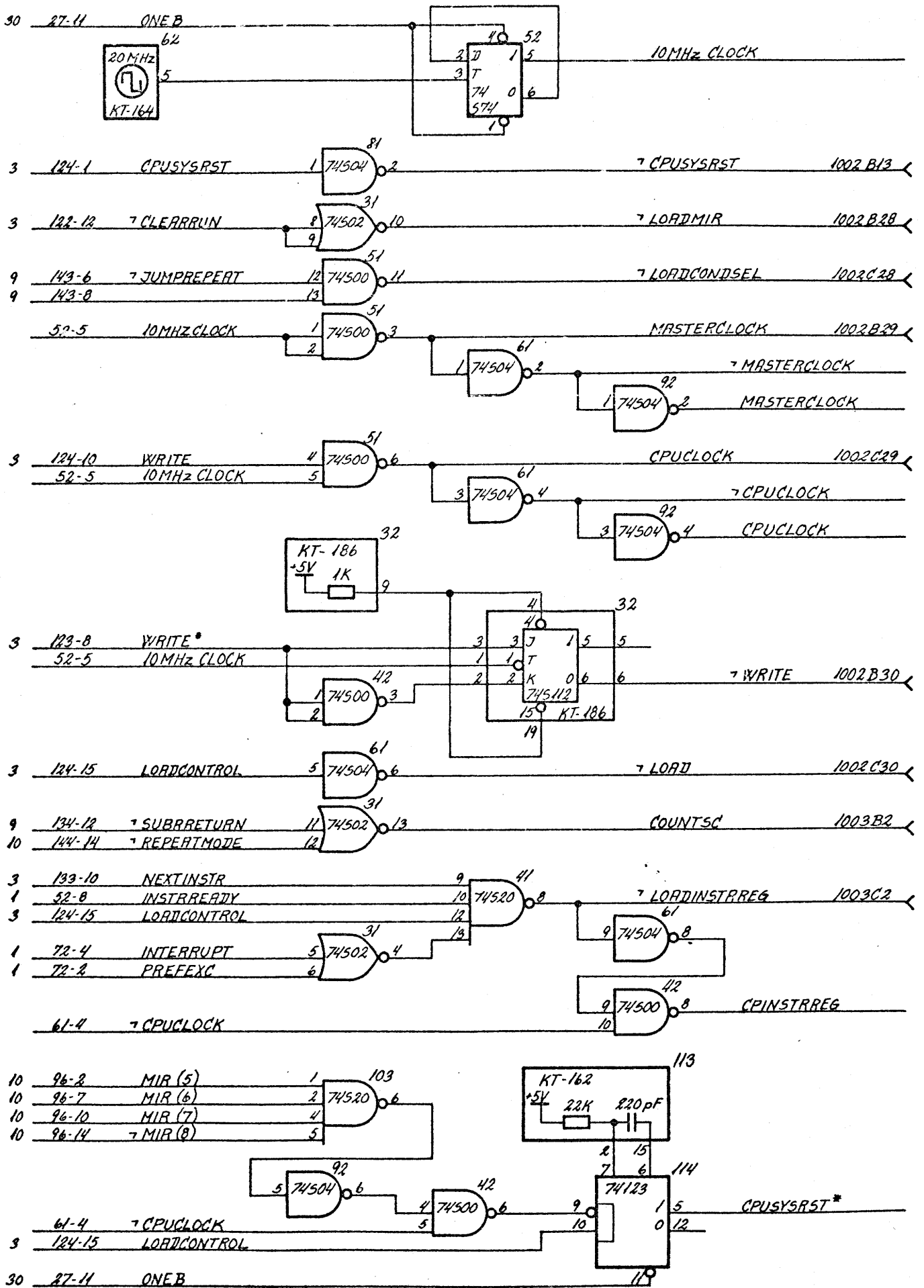


MICROINSTRUCTIONS
 TO CPU802, CPU803, AND CPU804

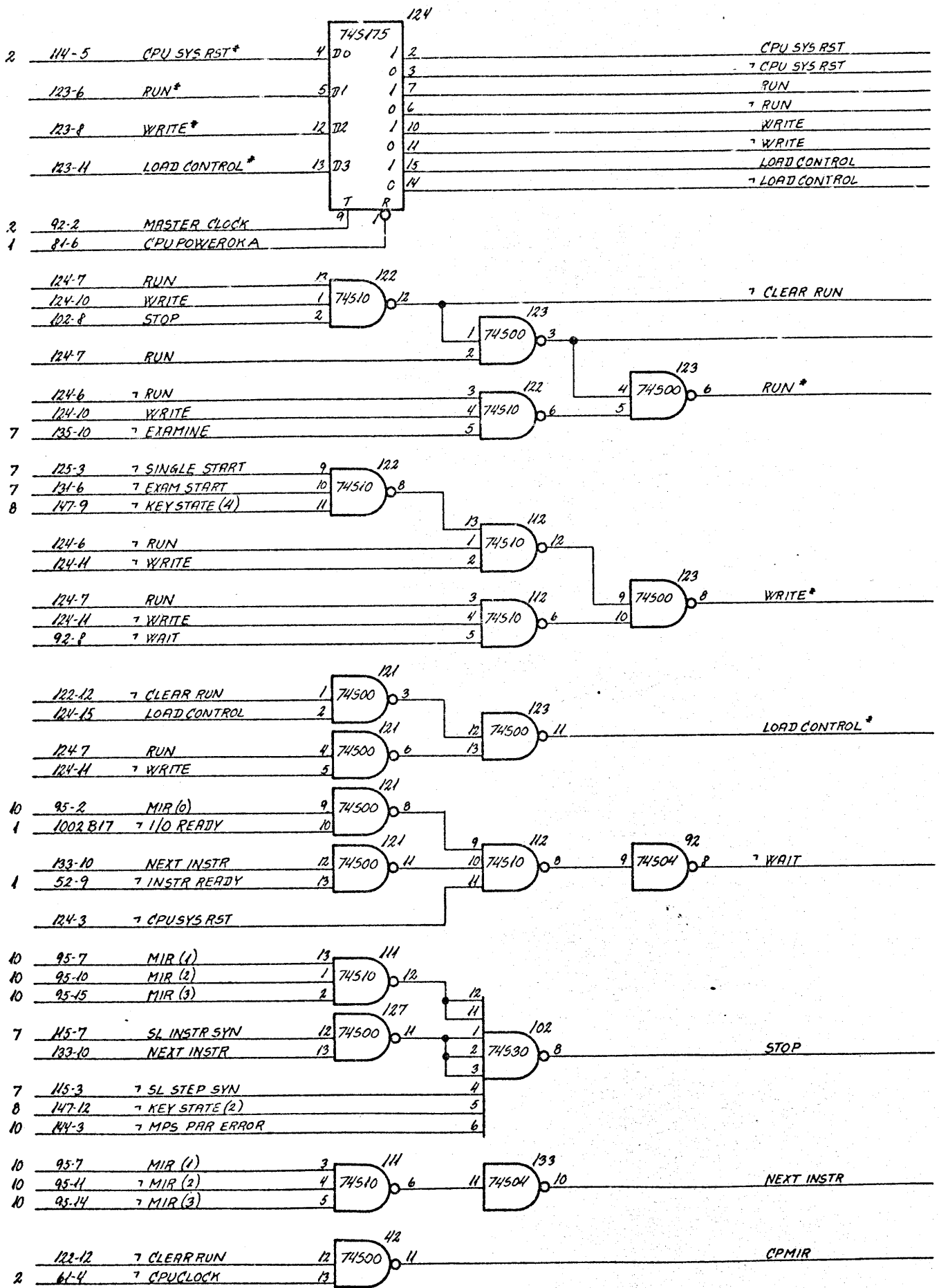
Unit	CPU 801
Dwg. No.	R 11651
CPU 801 BLOCK DIAGRAM	

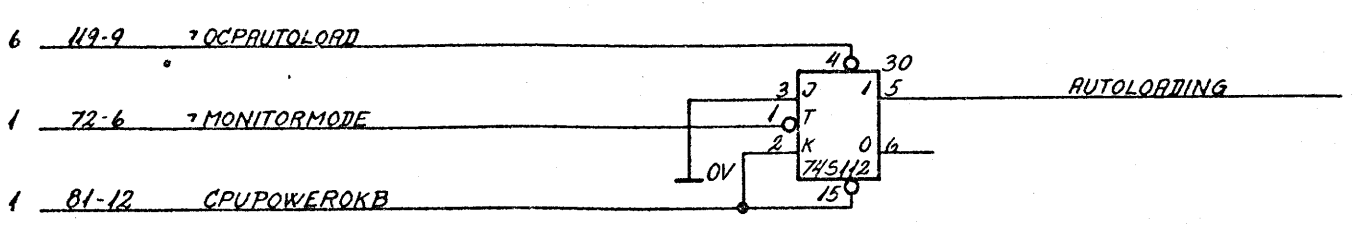
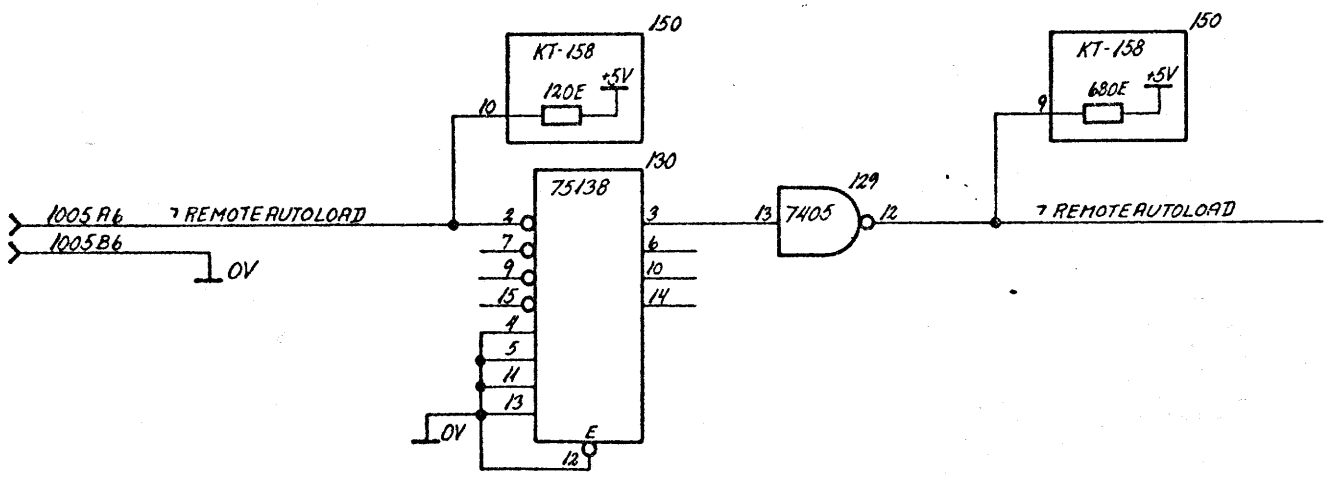
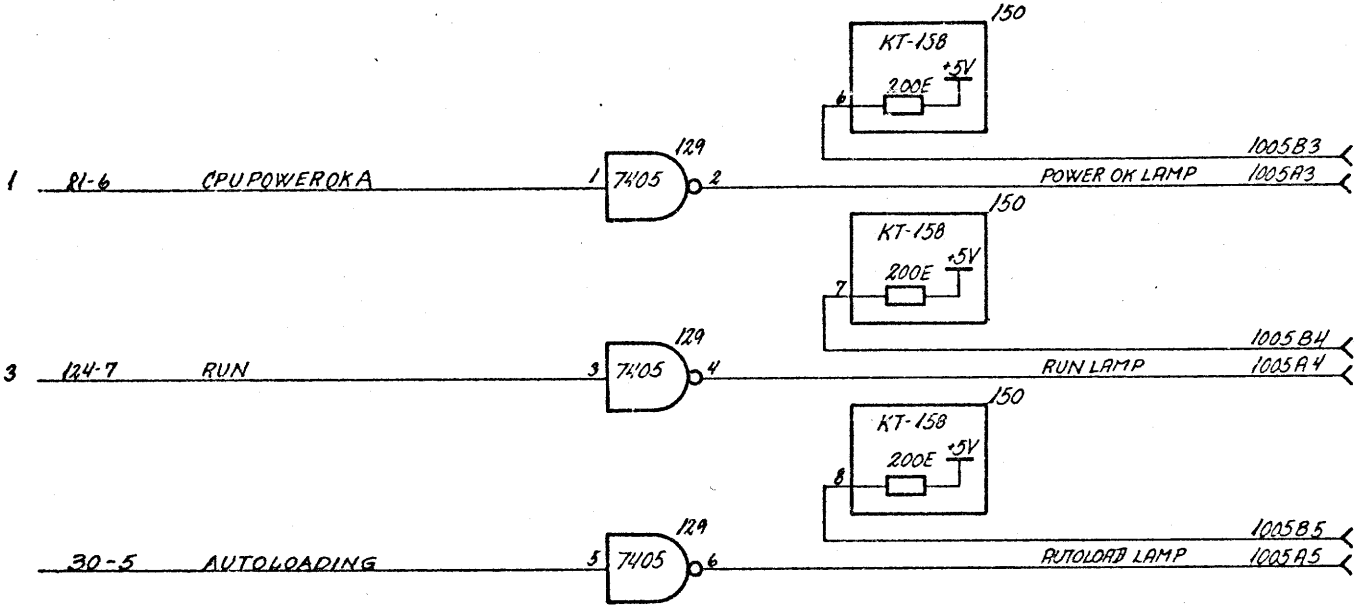
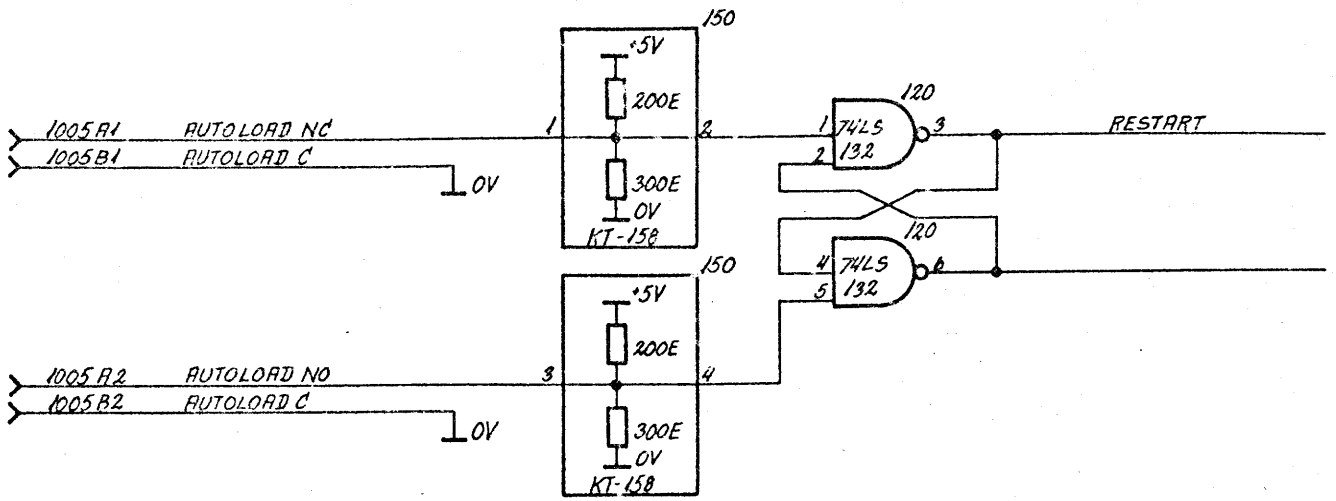


760409 REF 760423 A08



760014 REV 760015 ROB

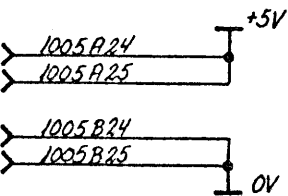
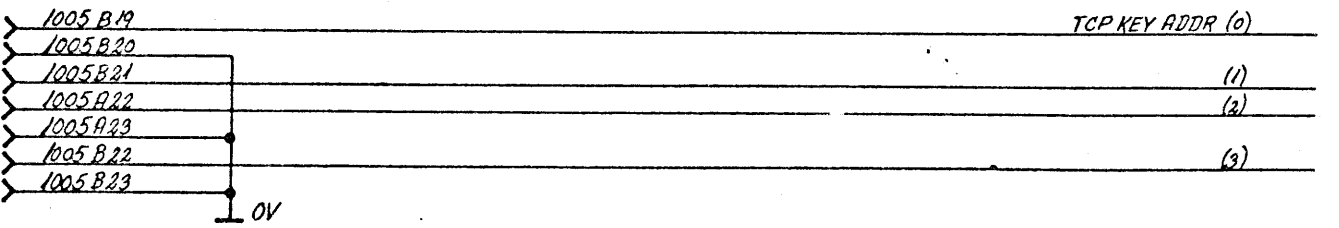
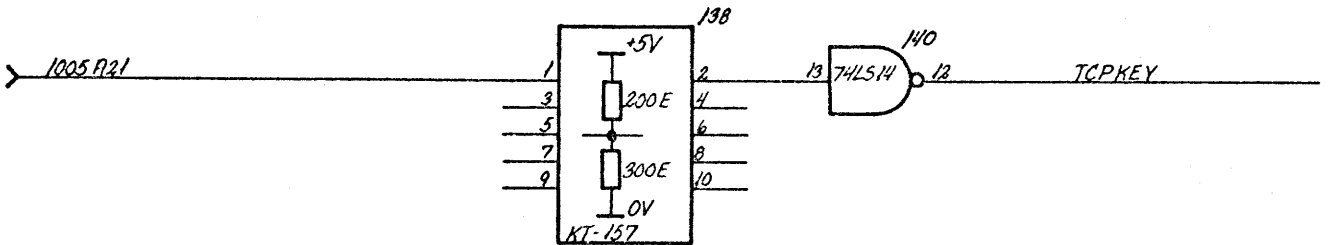
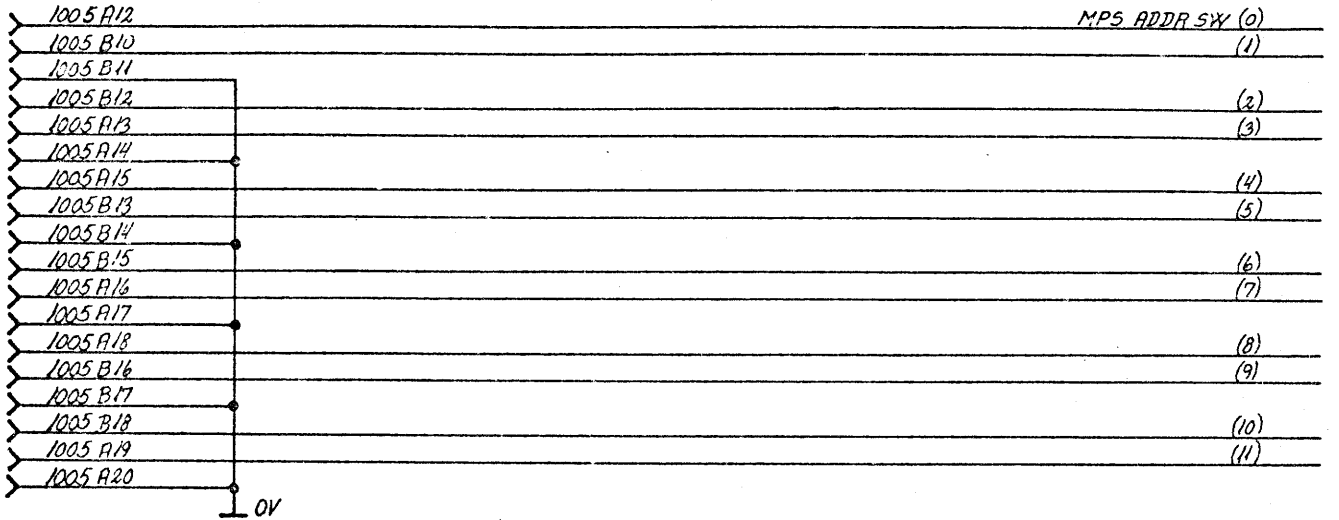
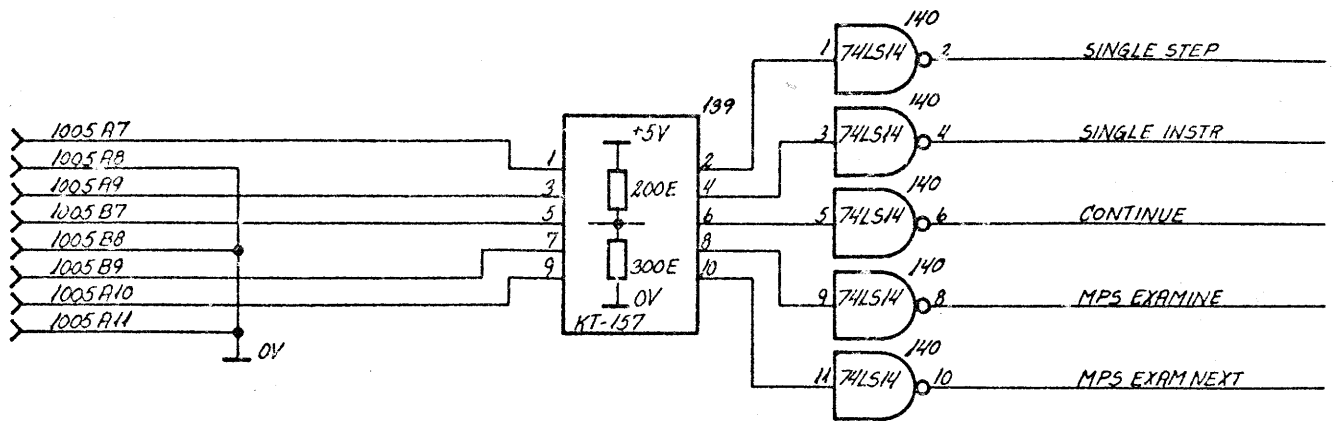




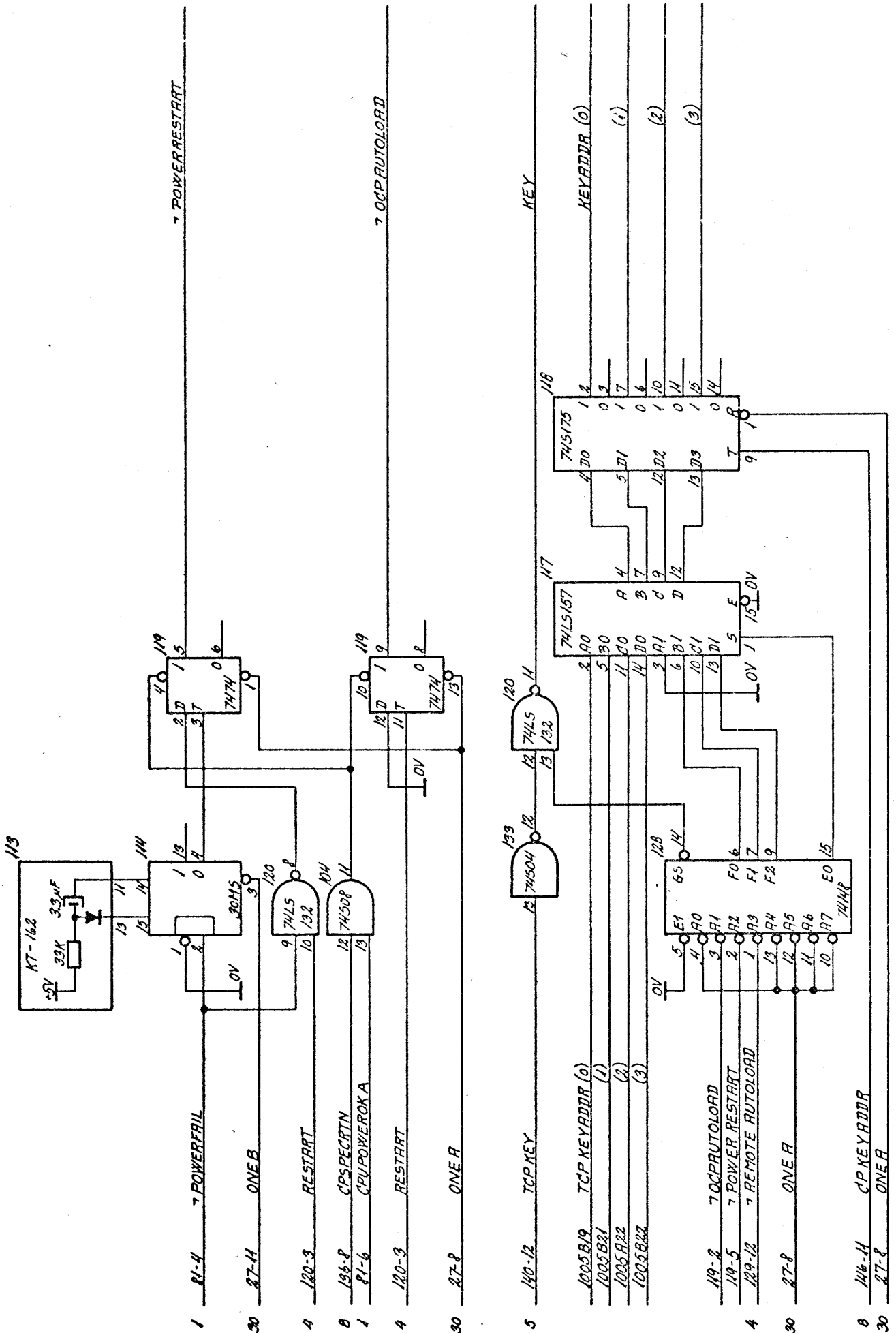
751006 RPT 760204 R08

CPU 801
R 11376

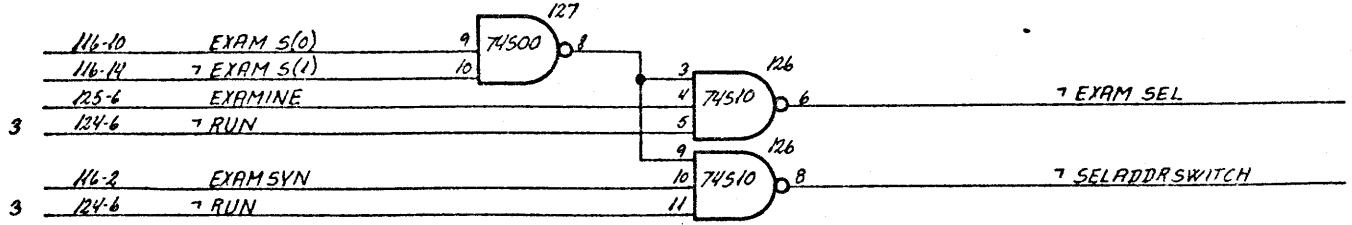
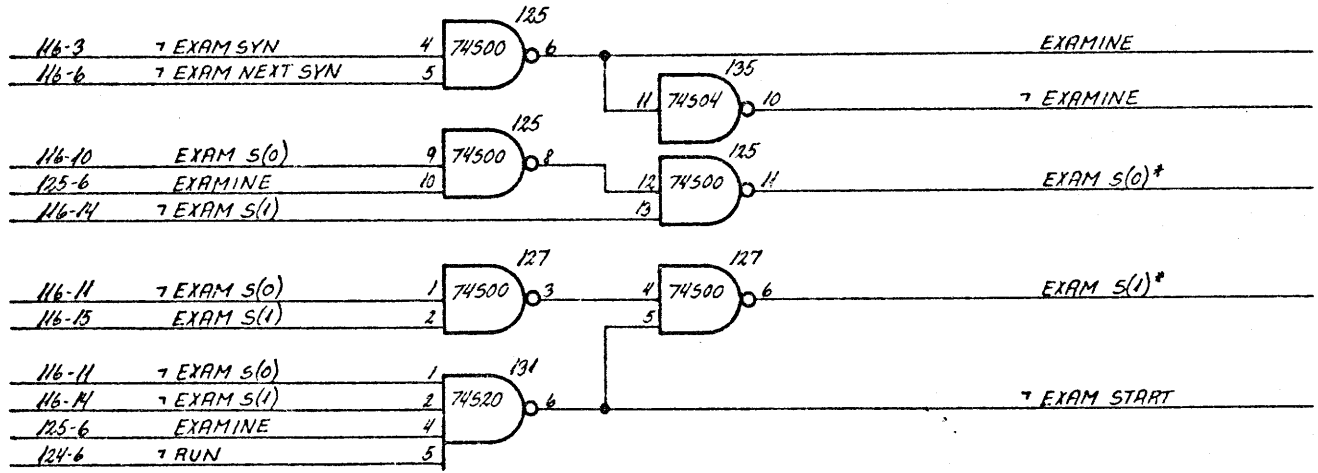
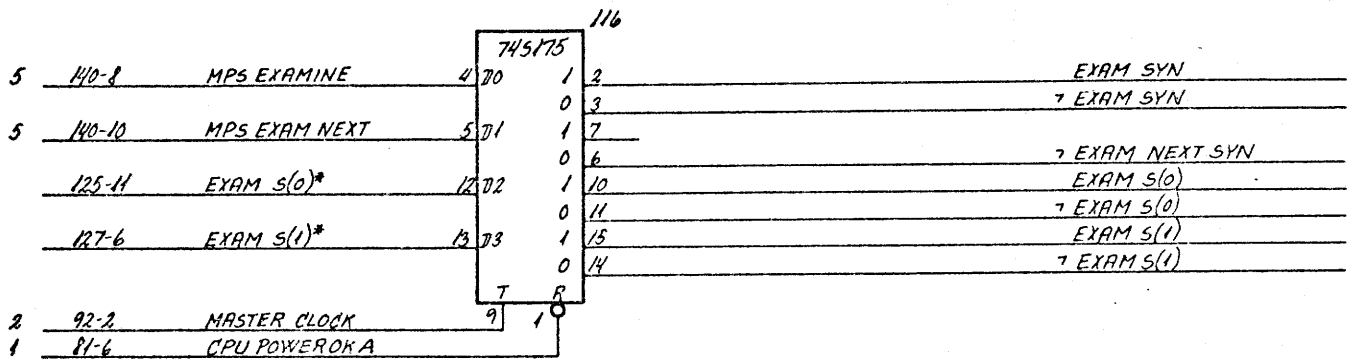
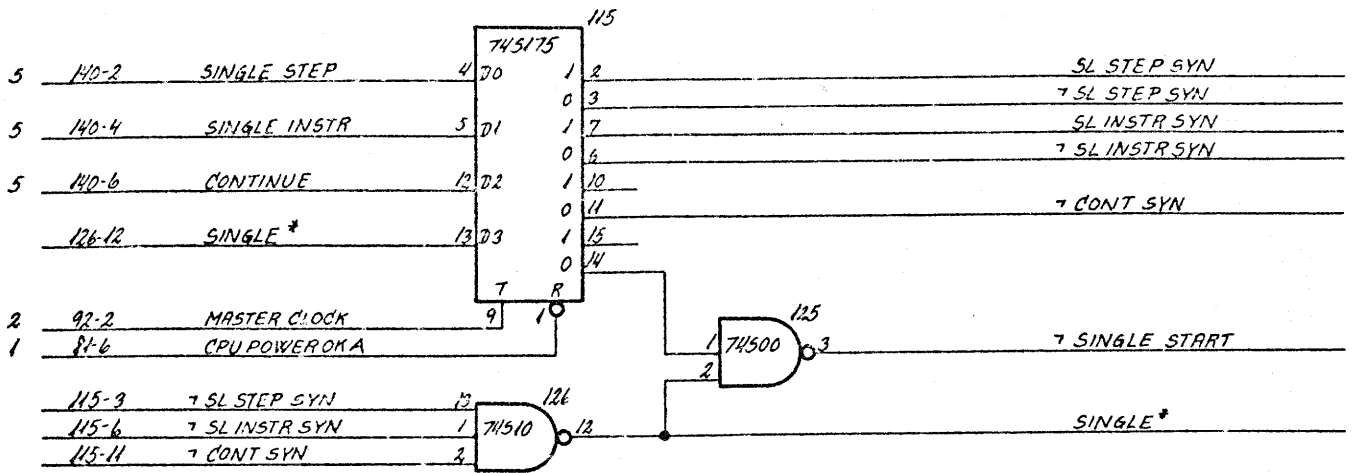
INTERFACE TO OPERATORS CONTROL PANEL
AND REMOTE AUTOLOAD



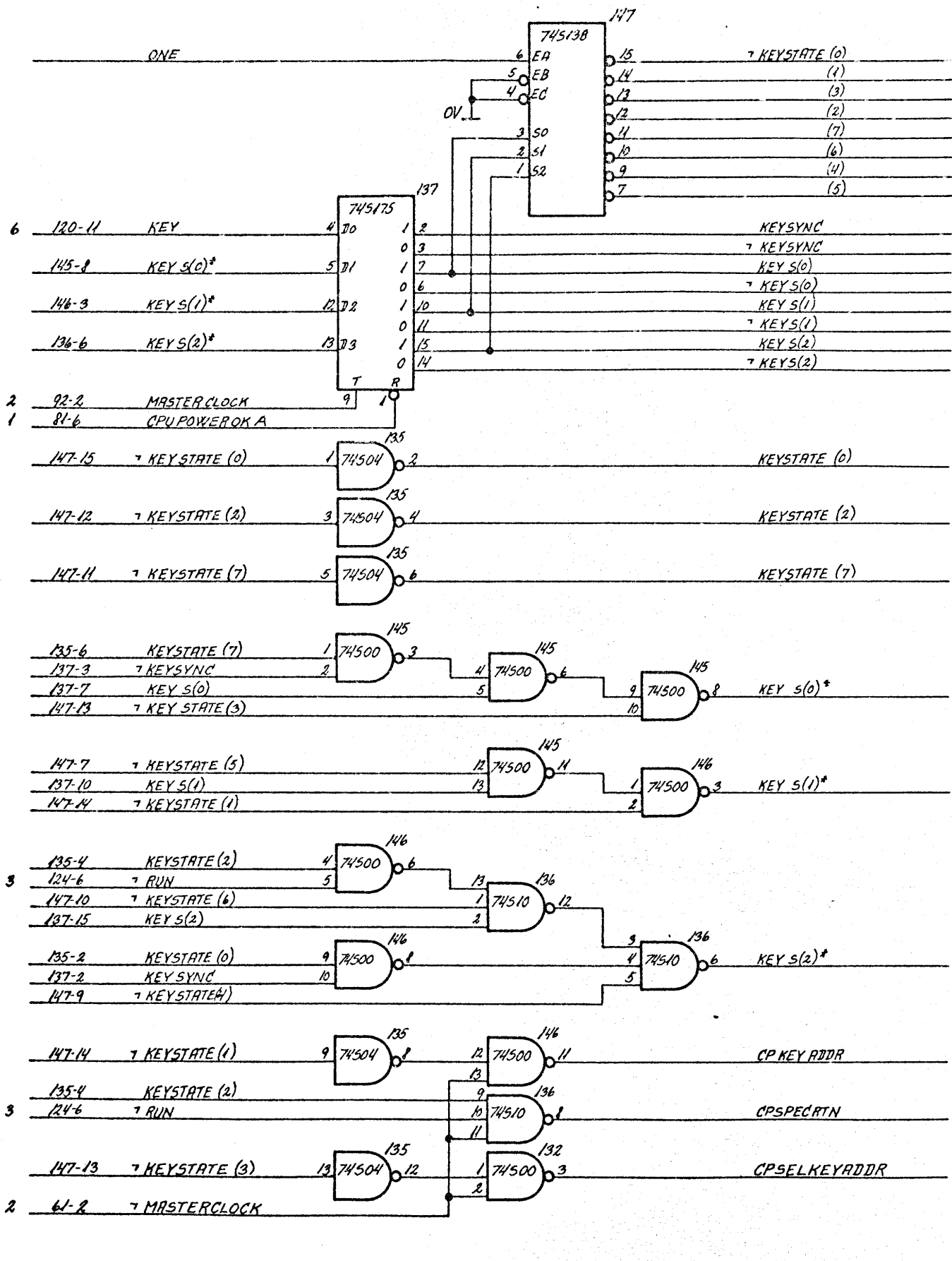
760121 ARJ 760121 ROB



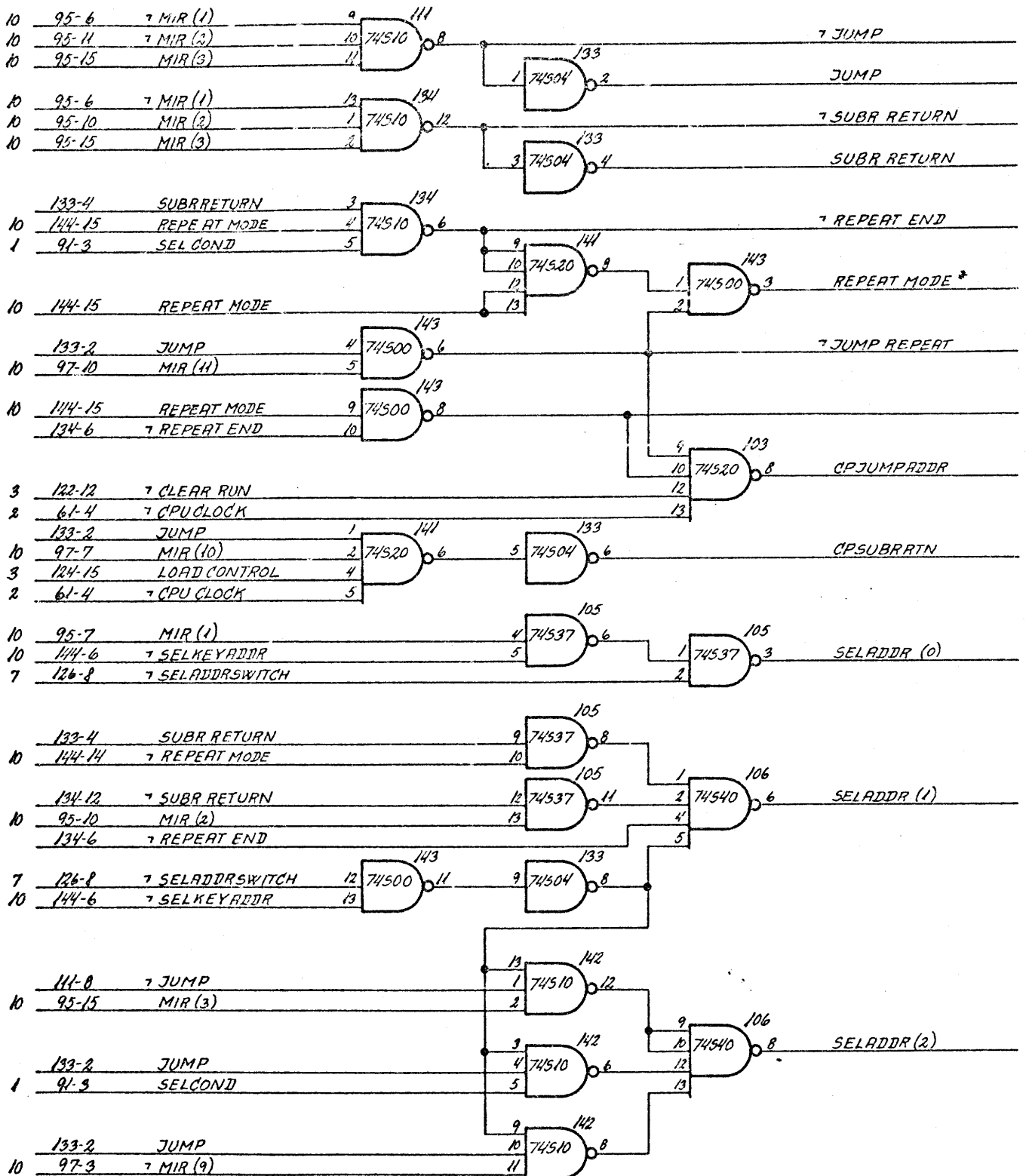
AUTOLOAD, POWER RESTART,
AND KEY ADDRESS ENCODER



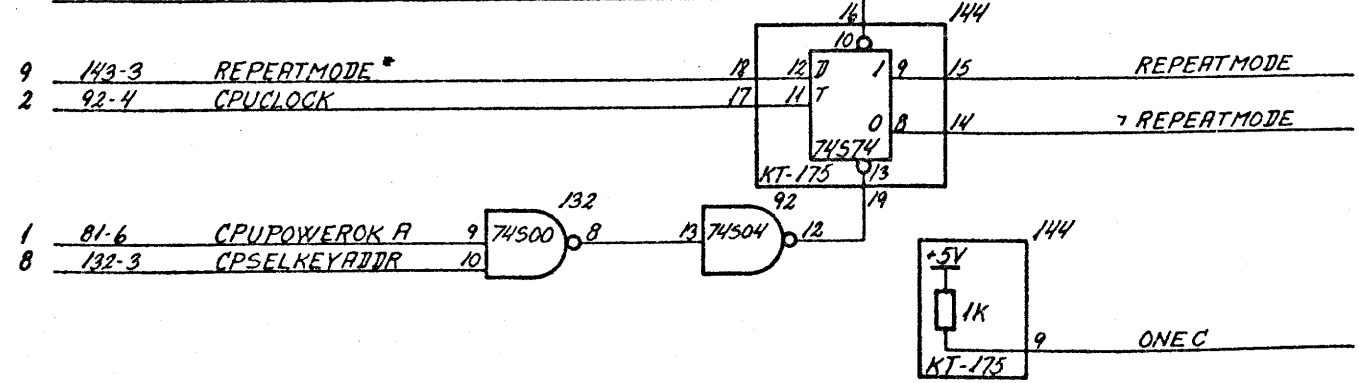
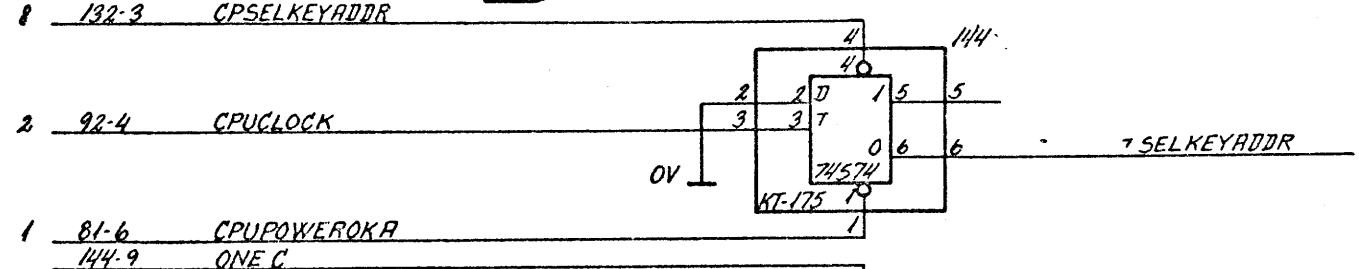
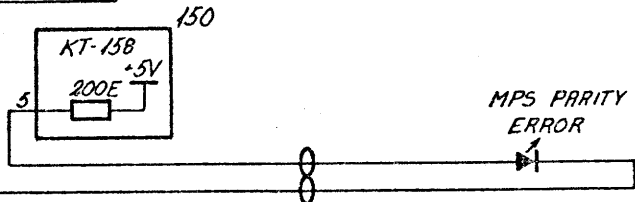
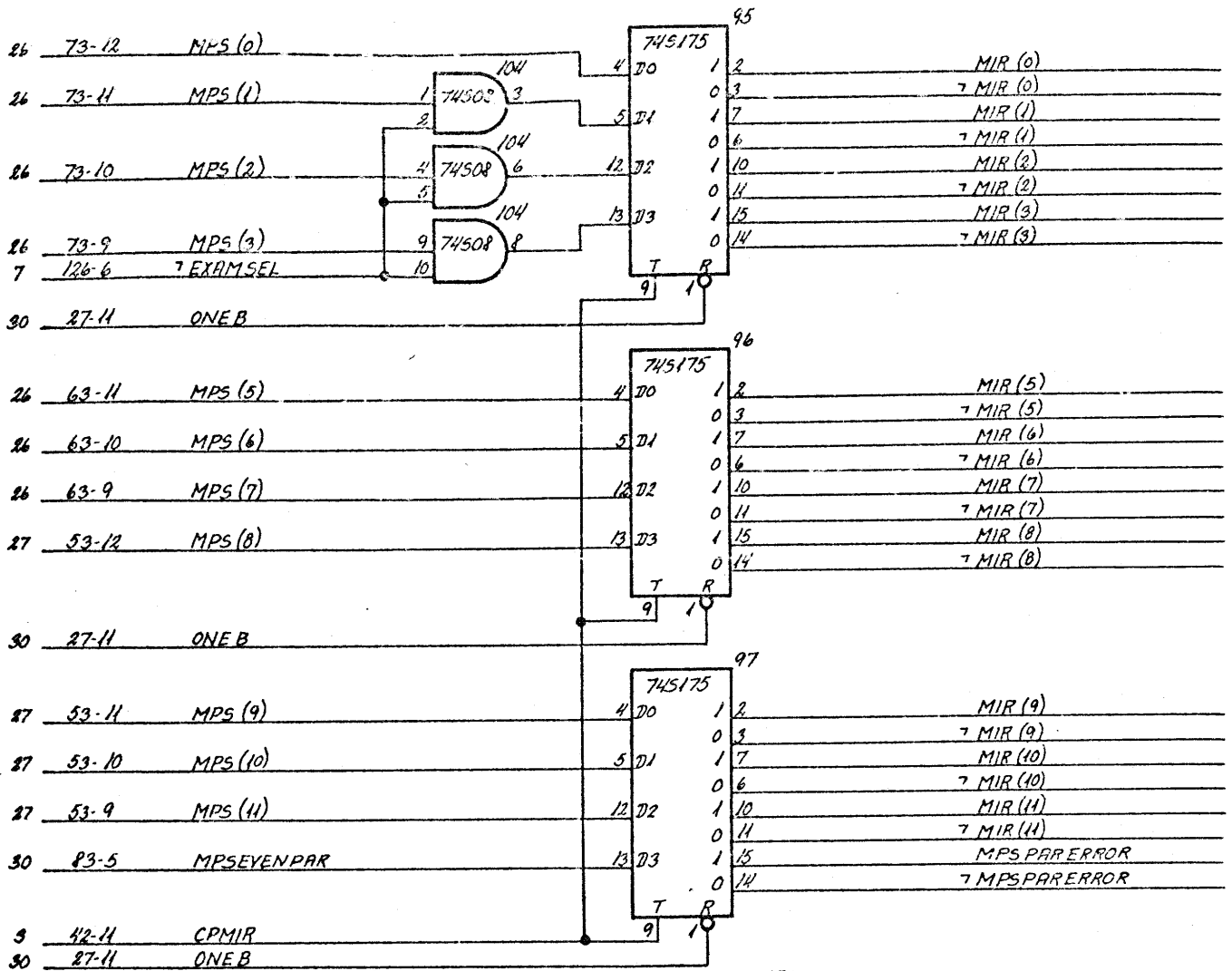
75107 ARJ 7620V A08



760510 REV 760510 ROB

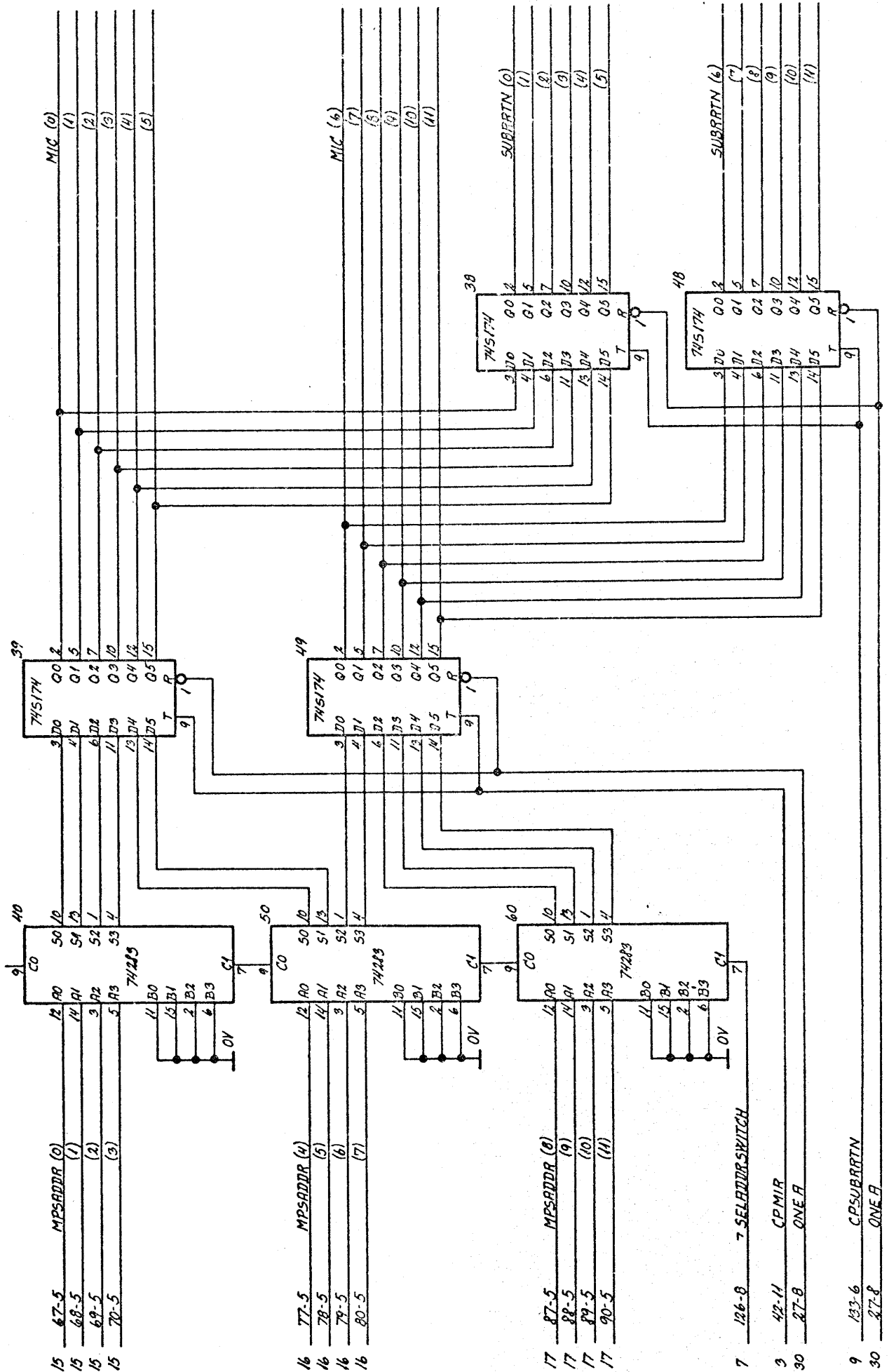


751031 RAJ 760203 ACB

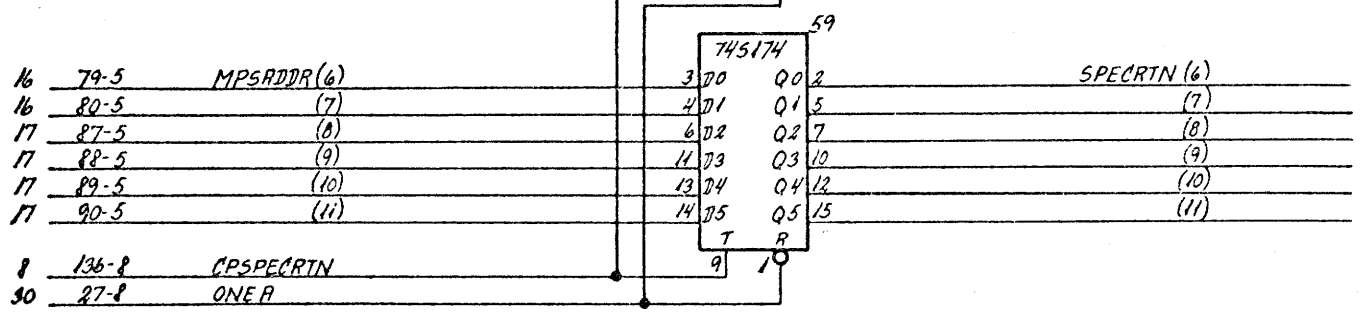
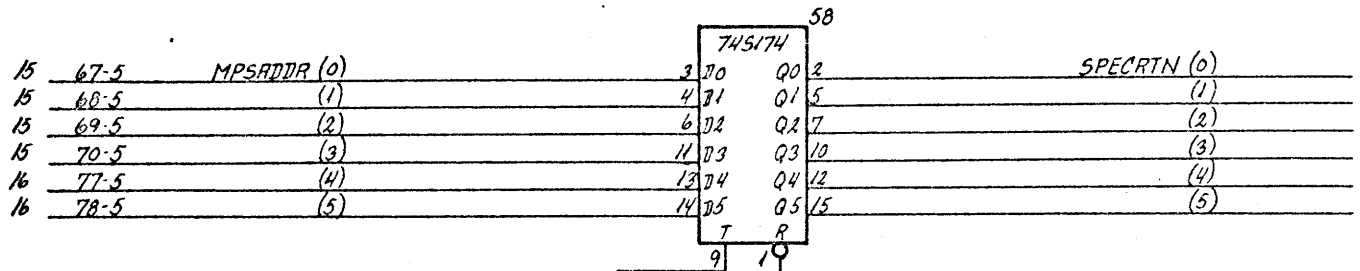
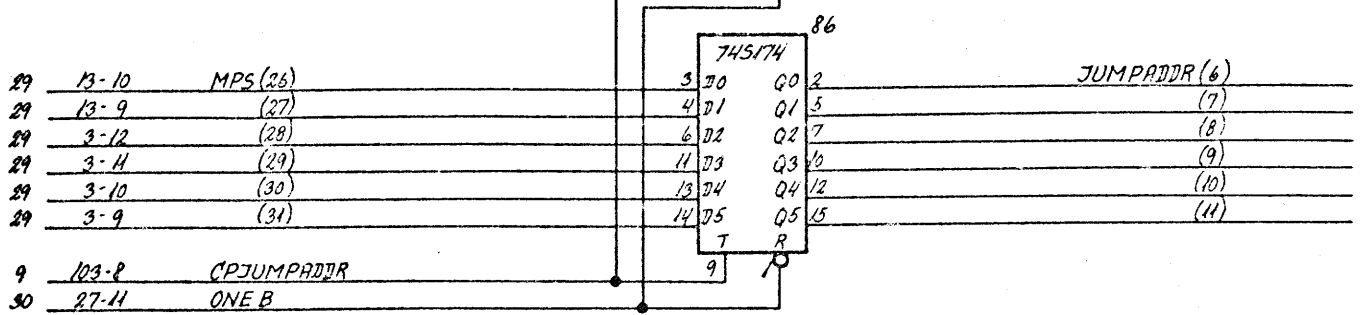
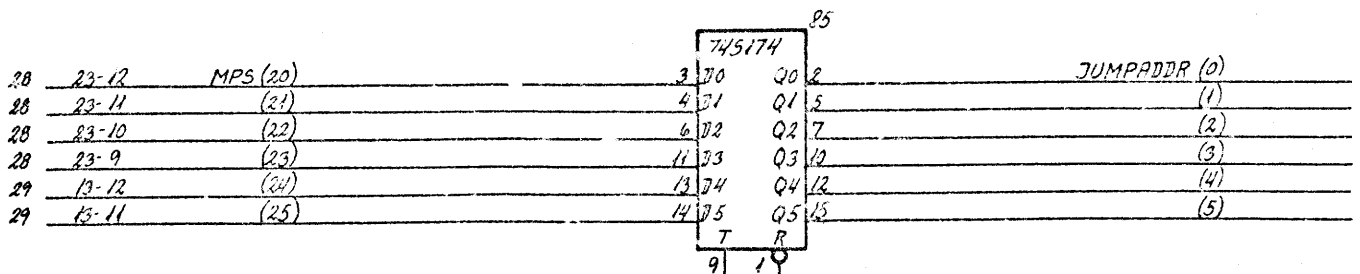


751019 RAJ 760205 A05

CPU801
R 11383



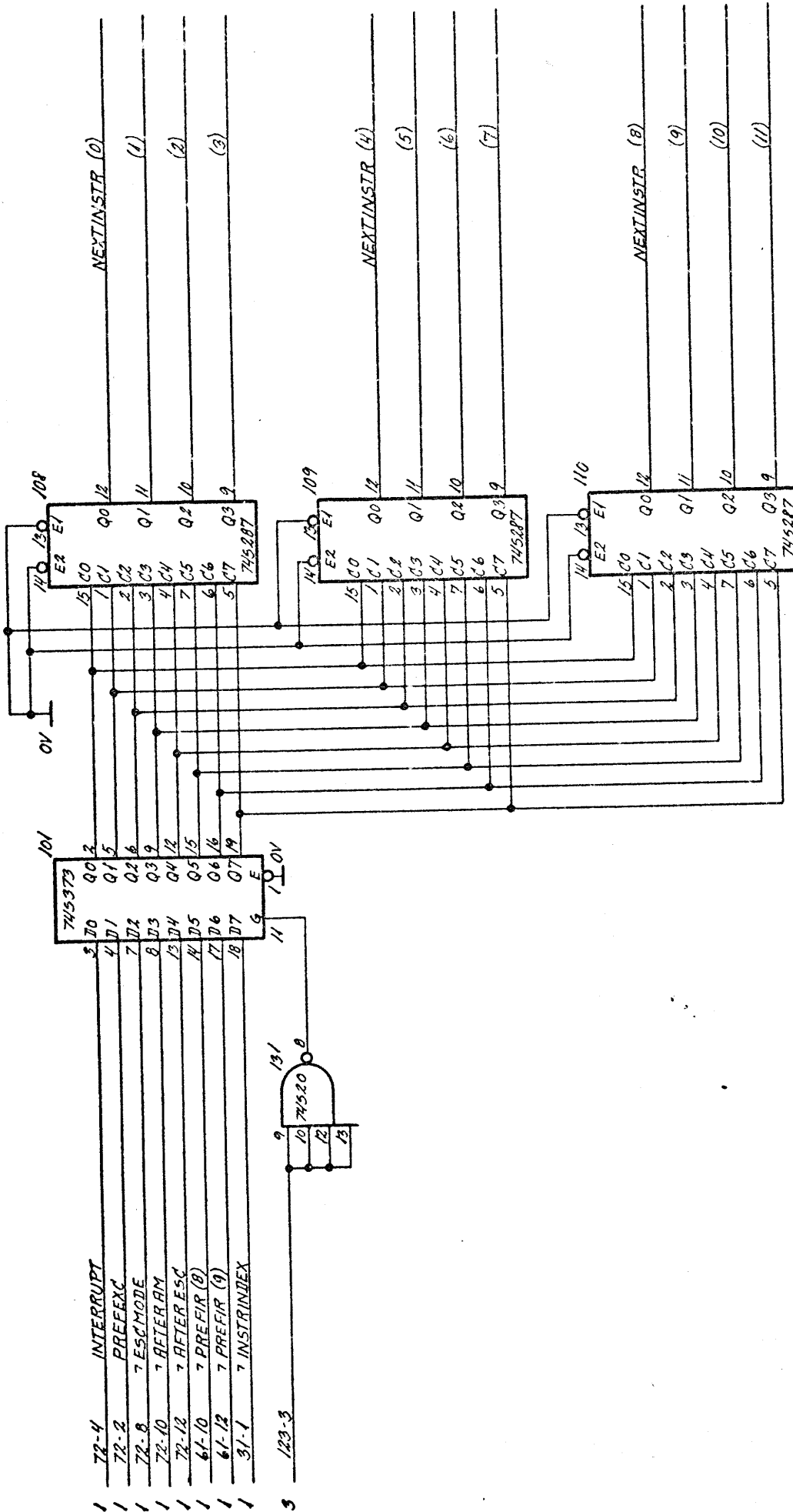
MICROINSTRUCTION COUNTER, MIC
AND SUBROUTINE RETURN REGISTER, SUBRTN



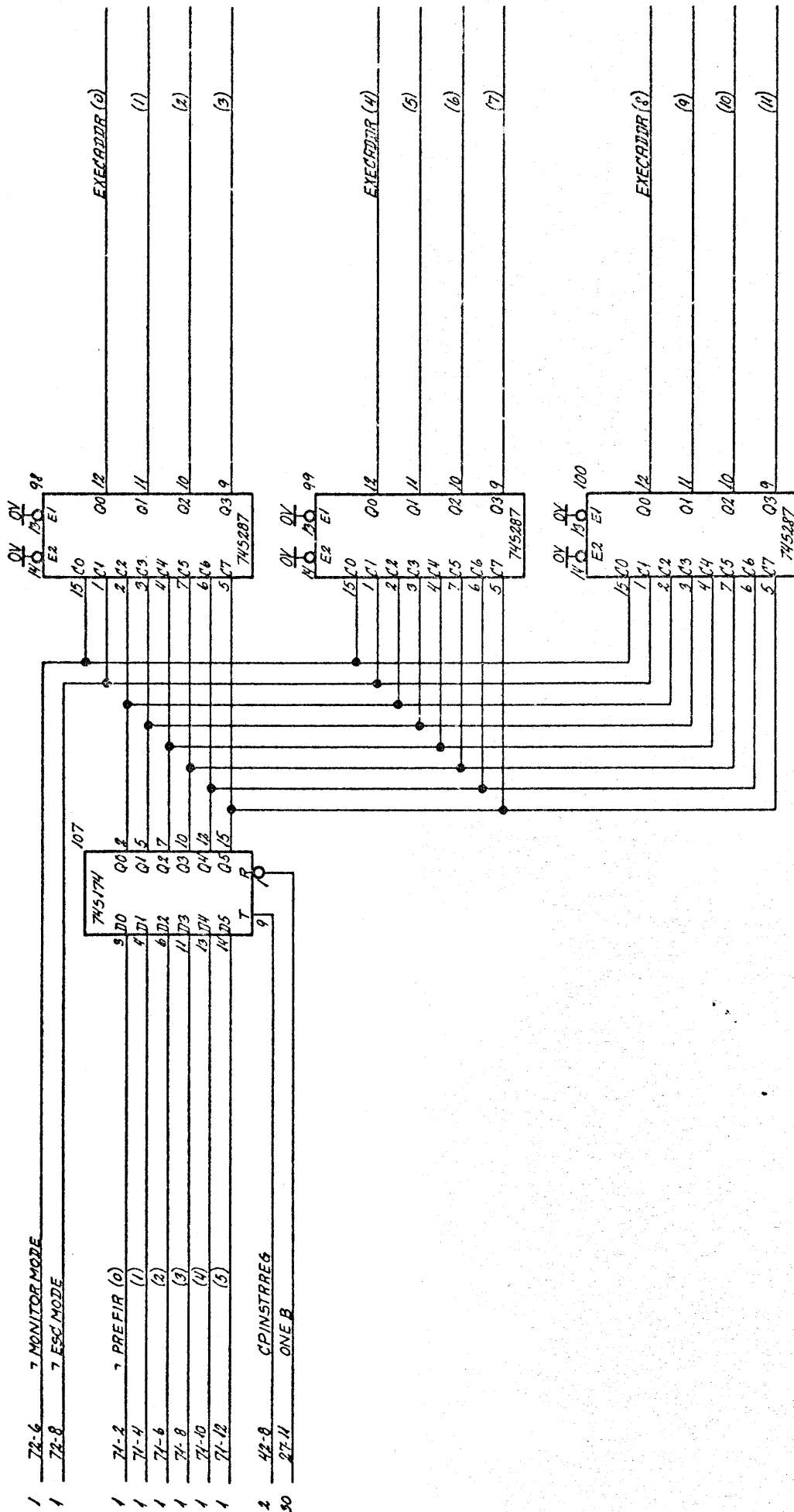
750922 APR 740103 ROB

CPU801
R 11384

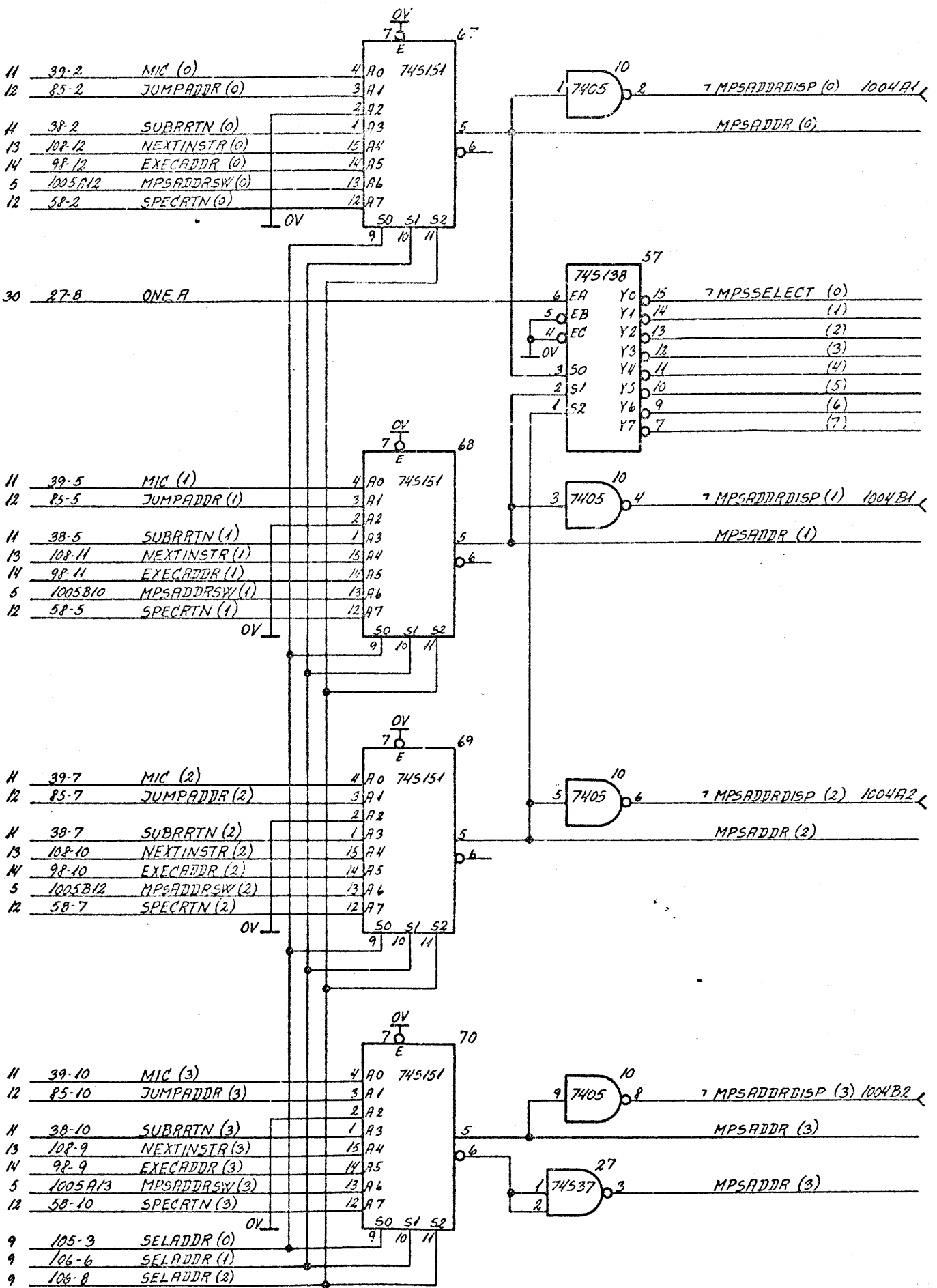
JUMP ADDRESS REGISTER
SPECIAL RETURN ADDRESS REGISTER



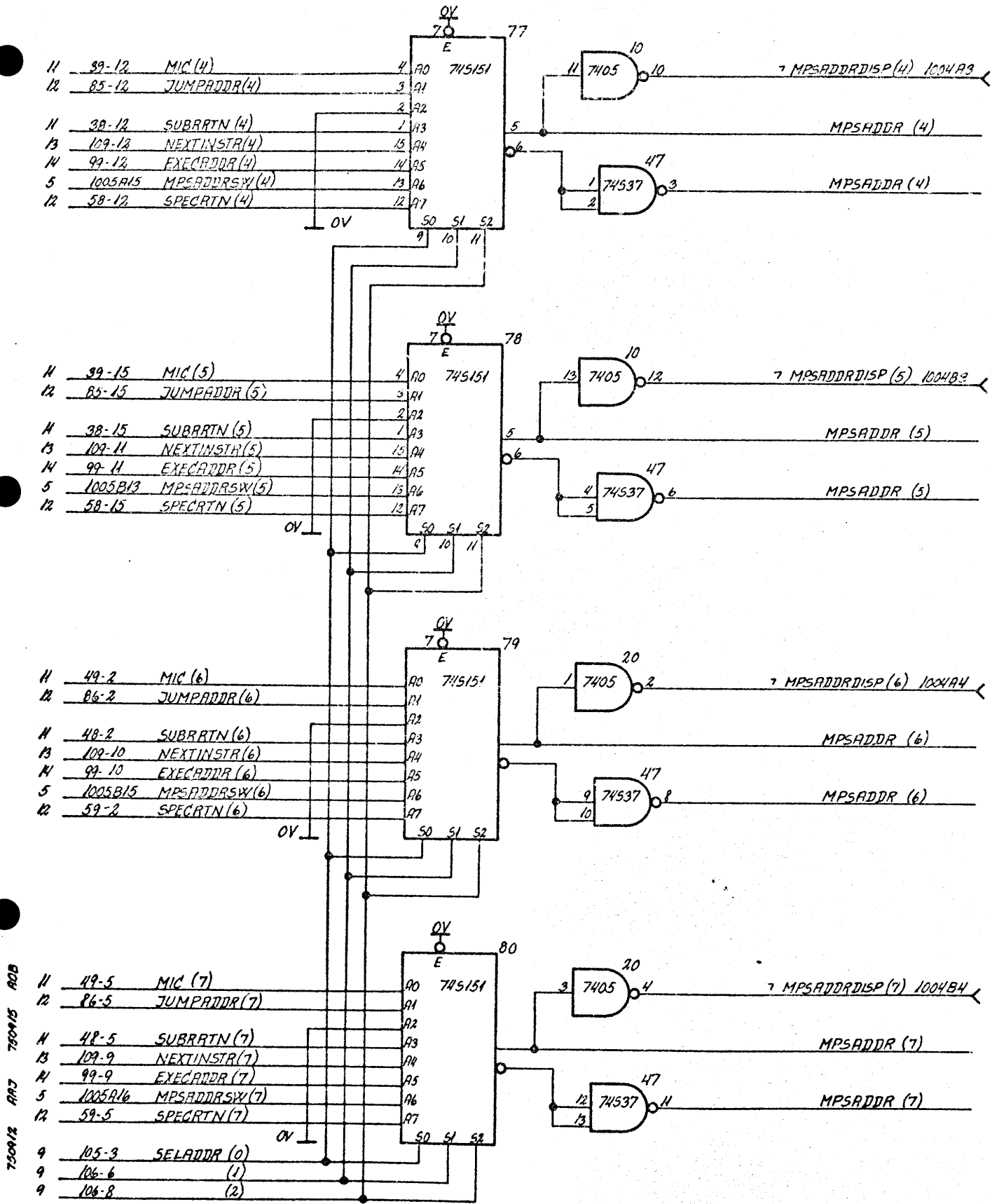
ADDRESS TABLE FOR START OF NEXT INSTRUCTION



ADDRESS TABLE FOR START OF INSTRUCTION EXECUTION

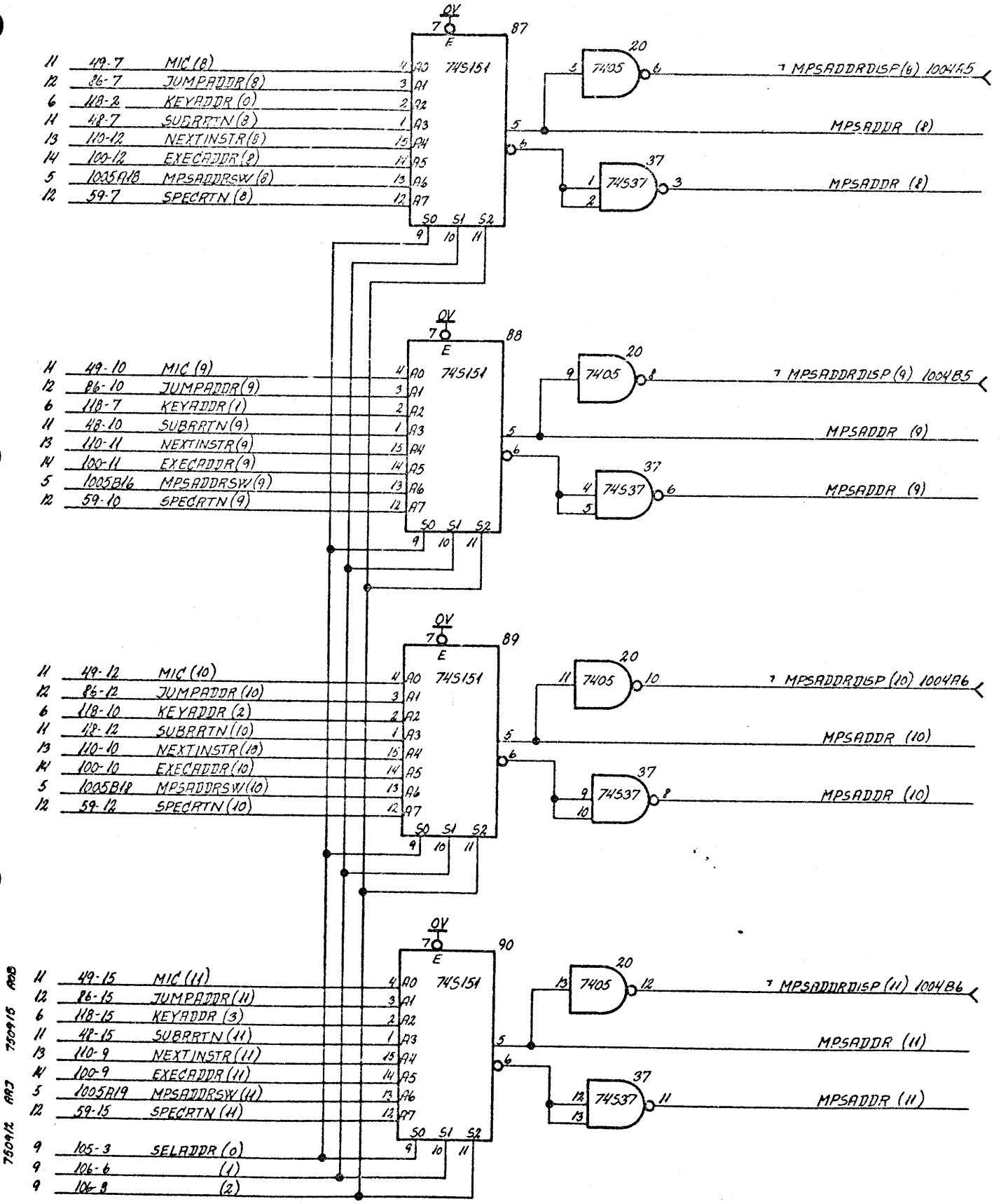


760519 RA7 760530 A0B



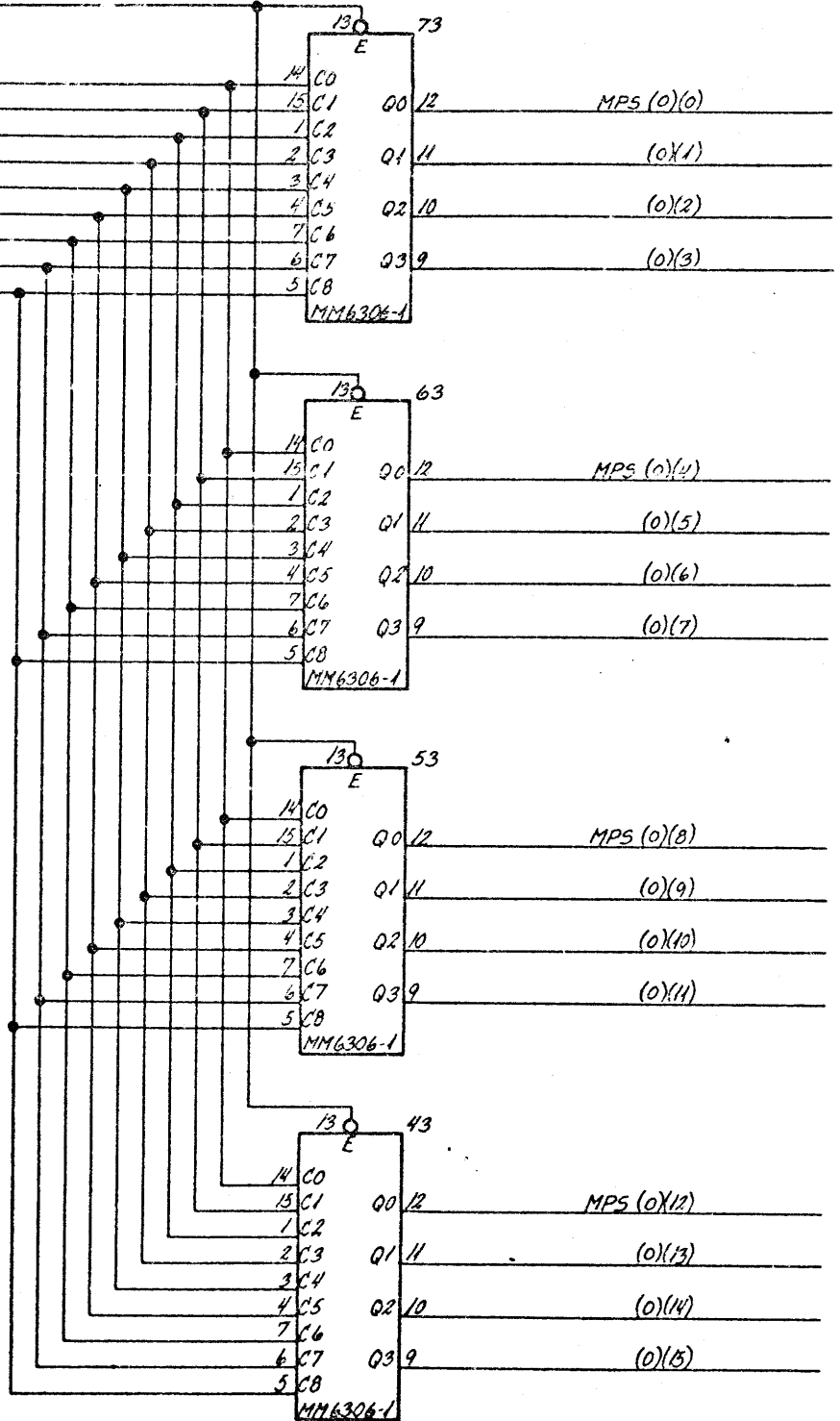
CPU801
R 11388

MPS ADDRESS SELECTION
MPSADDR (4-7)



15 57-15 7MPSSELECT (0)

15 27-3 MPSADDR (3)
 16 47-3 (4)
 16 47-6 (5)
 16 47-8 (6)
 16 47-11 (7)
 17 37-3 (8)
 17 37-6 (9)
 17 37-8 (10)
 17 37-11 (11)



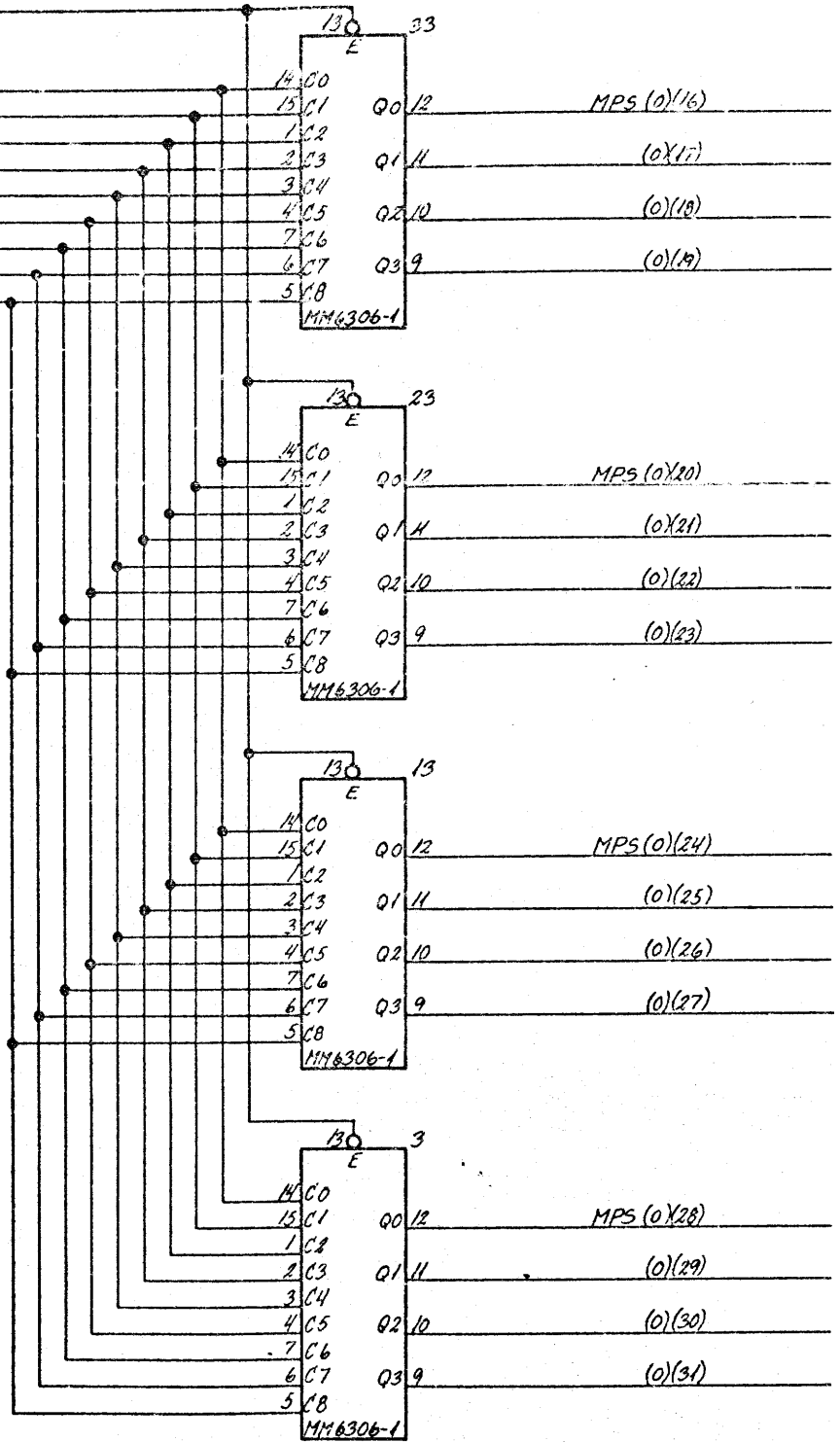
760519 RP7 760520 PCB

CPU 801
 R41390

MICRO PROGRAM STORE
 WORDS (0:511), BITS (0:15)

15 37-15 1 MP55FLECT (0)

15	27-3	MPSADDR (3)
16	47-3	(4)
16	47-6	(5)
16	47-8	(6)
16	47-11	(7)
17	37-3	(8)
17	37-6	(9)
17	37-8	(10)
17	37-11	(11)



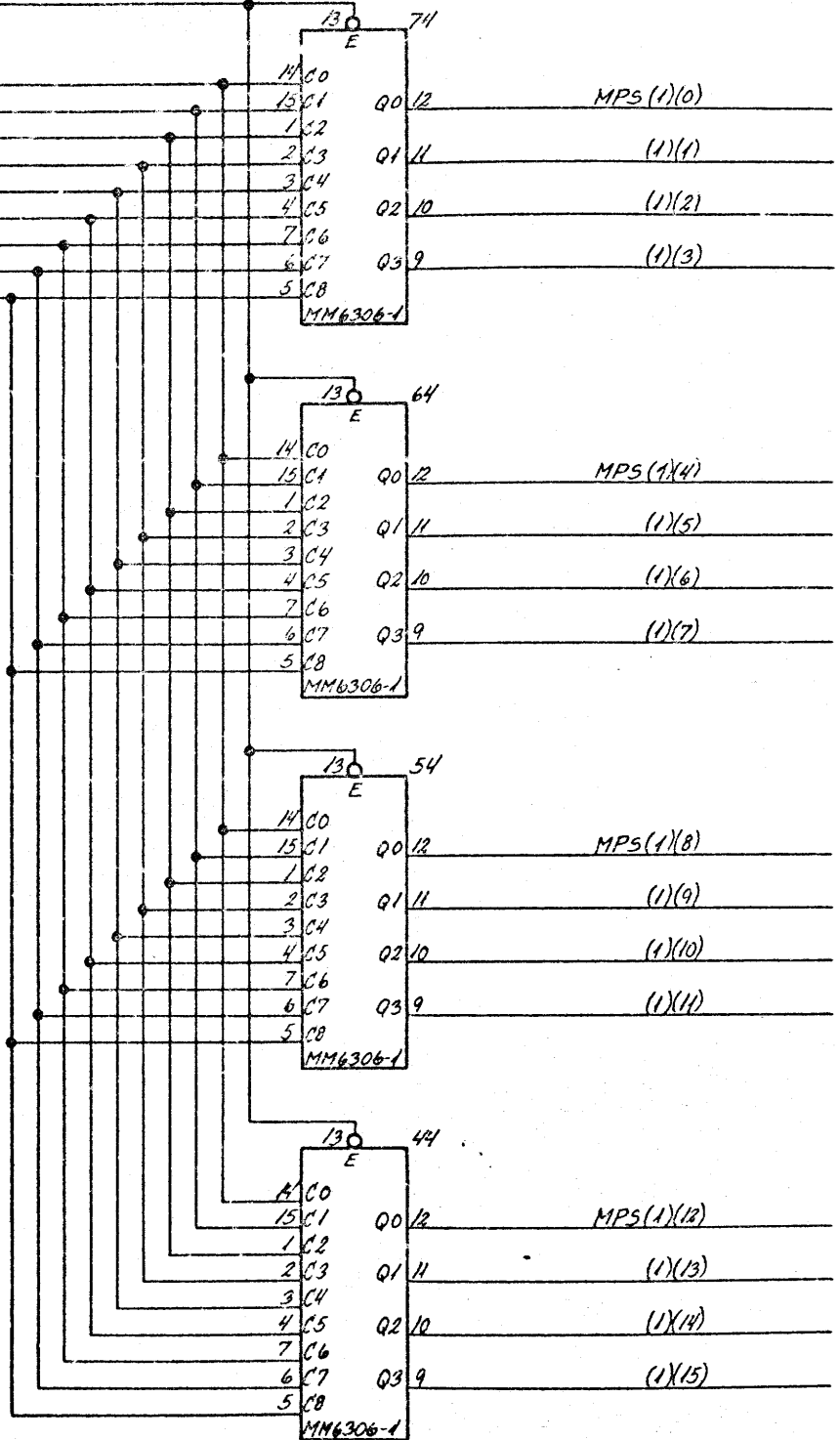
760519 RFI 760530 RO8

CPU 801
R11394

MICRO PROGRAM STORE
WORDS (0:511), BITS (16:31)

15 57-14 2 MPSSELECT (1)

15	27-3	MPSADDR (3)
16	47-3	(4)
16	47-6	(5)
16	47-8	(6)
16	47-11	(7)
17	37-3	(8)
17	37-6	(9)
17	37-8	(10)
17	37-11	(11)



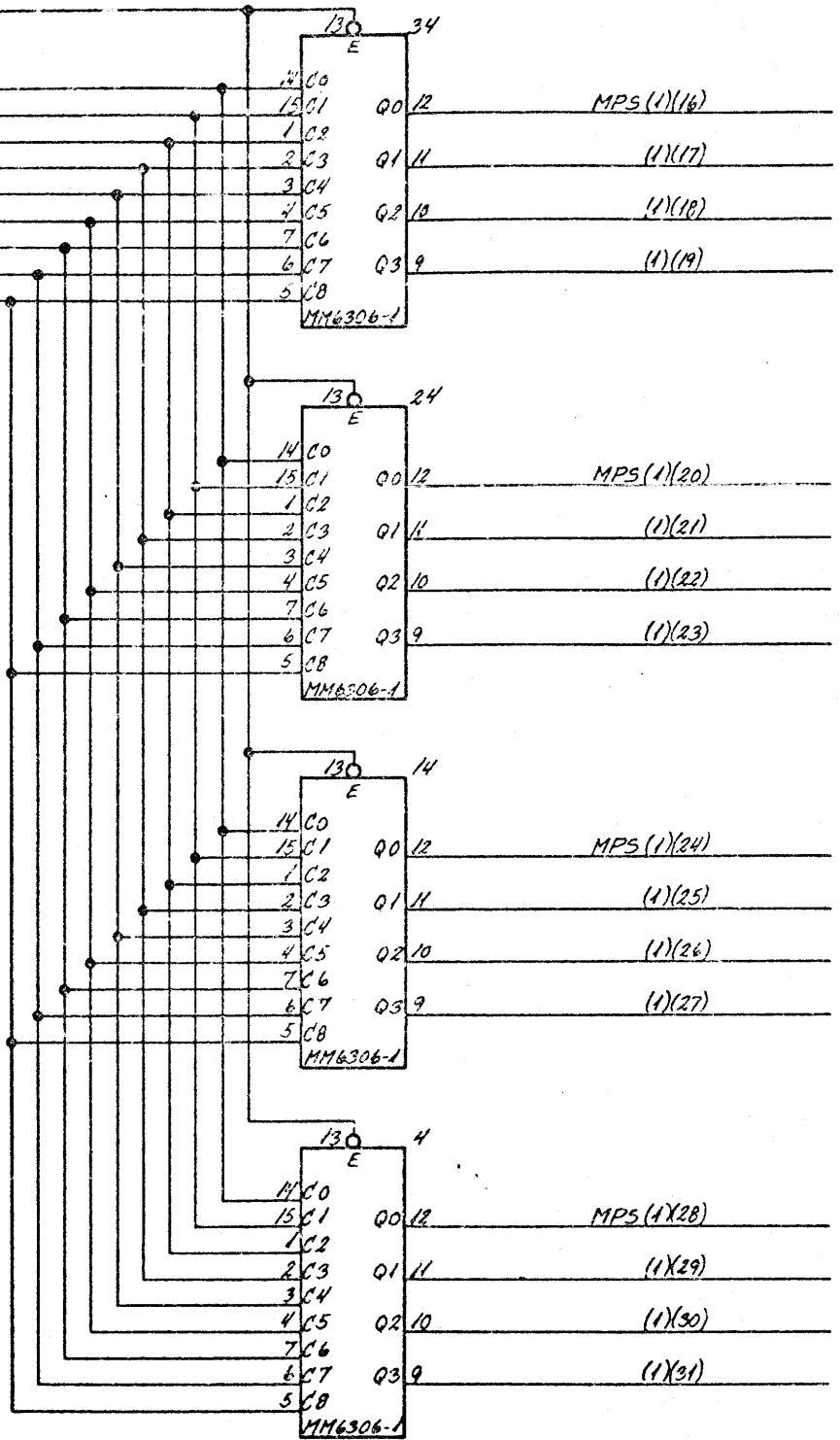
760519 ARR 760530 ROB

CPU 801
R 11392

MICRO PROGRAM STORE
WORDS (512:1023), BITS (0:15)

15 57-14 7 MPSSELECT (1)

15 27-3 MPSADDR (3)
 16 47-3 (4)
 16 47-6 (5)
 16 47-8 (6)
 16 47-11 (7)
 17 37-3 (8)
 17 37-6 (9)
 17 37-8 (10)
 17 37-11 (11)



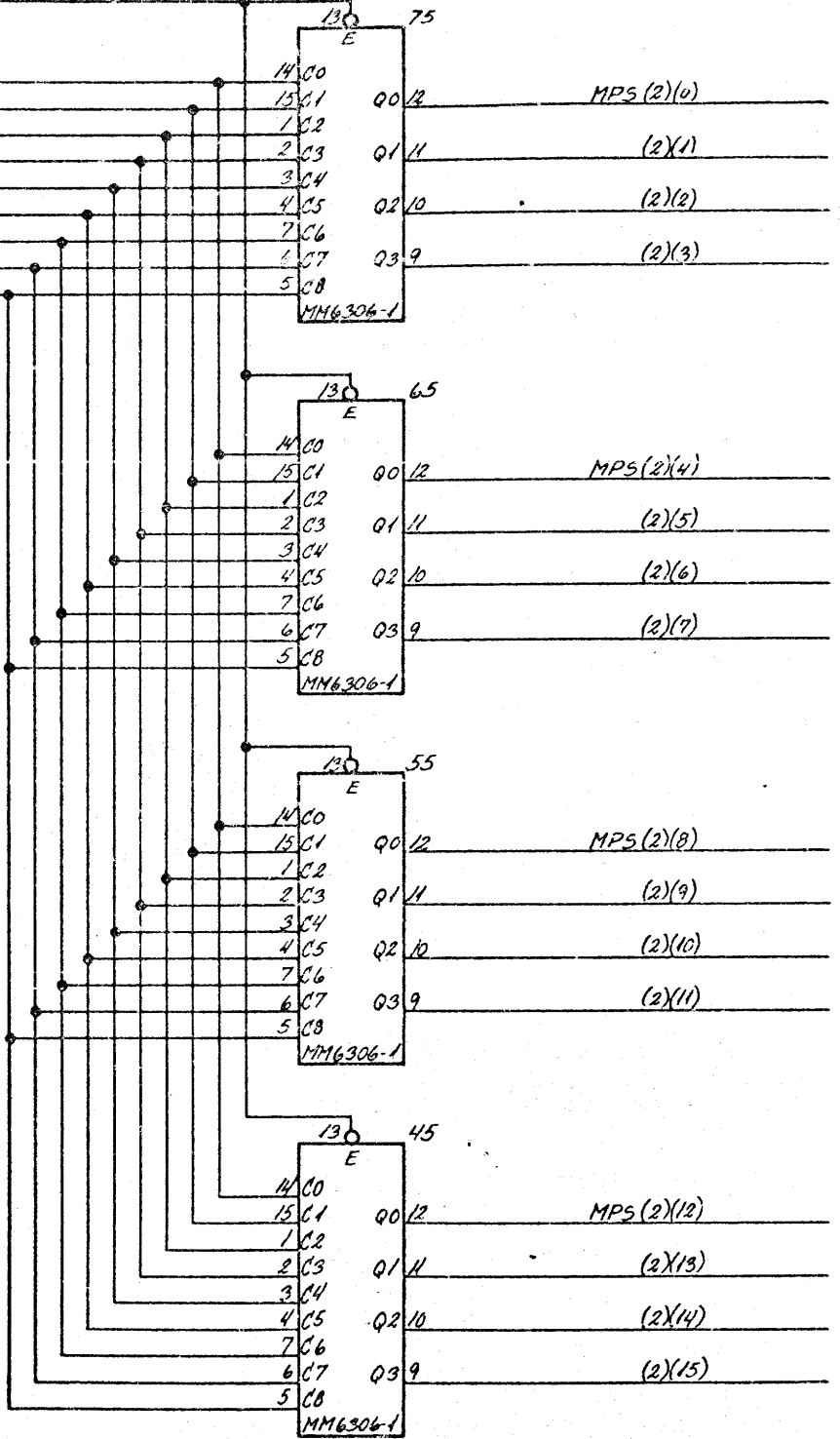
760519 AFJ 760530 RDB

CPU 801
 R 11393

MICRO PROGRAM STORE
 WORDS (512:1023), BITS (16:31)

15 57-13 7 MPSSELECT (2)

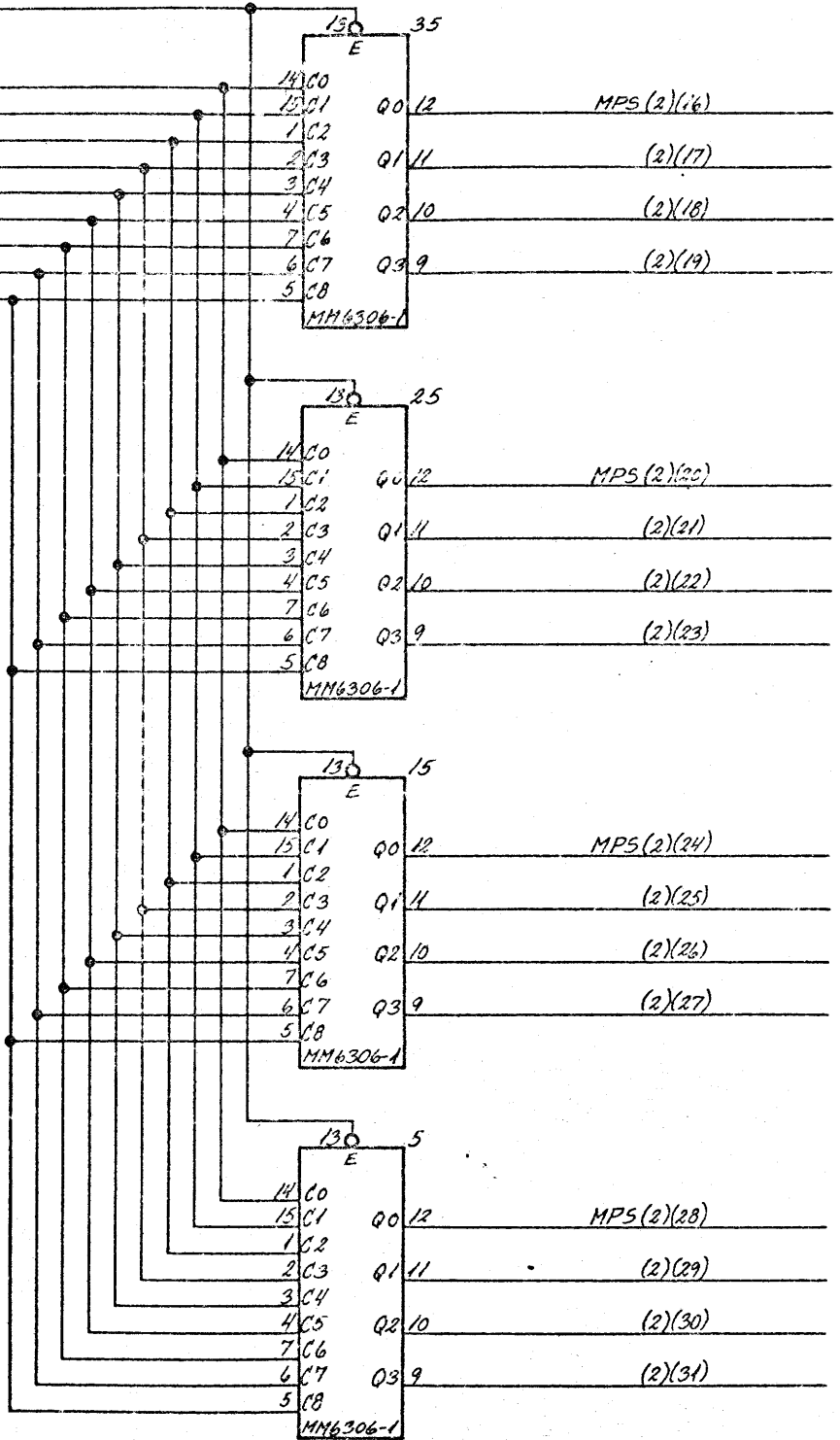
15 27-3 MPSADDR (3)
 16 47-3 (4)
 16 47-6 (5)
 16 47-8 (6)
 16 47-11 (7)
 17 37-3 (8)
 17 37-6 (9)
 17 37-8 (10)
 17 37-11 (11)



760519 ART 760590 R03

15 57-13 7 MPSSELECT (2)

15 27-3 MPSADDR (3)
 16 47-3 (4)
 16 47-6 (5)
 16 47-8 (6)
 16 47-11 (7)
 17 37-3 (8)
 17 37-6 (9)
 17 37-8 (10)
 17 37-11 (11)



760519 RRT 760530 RO8

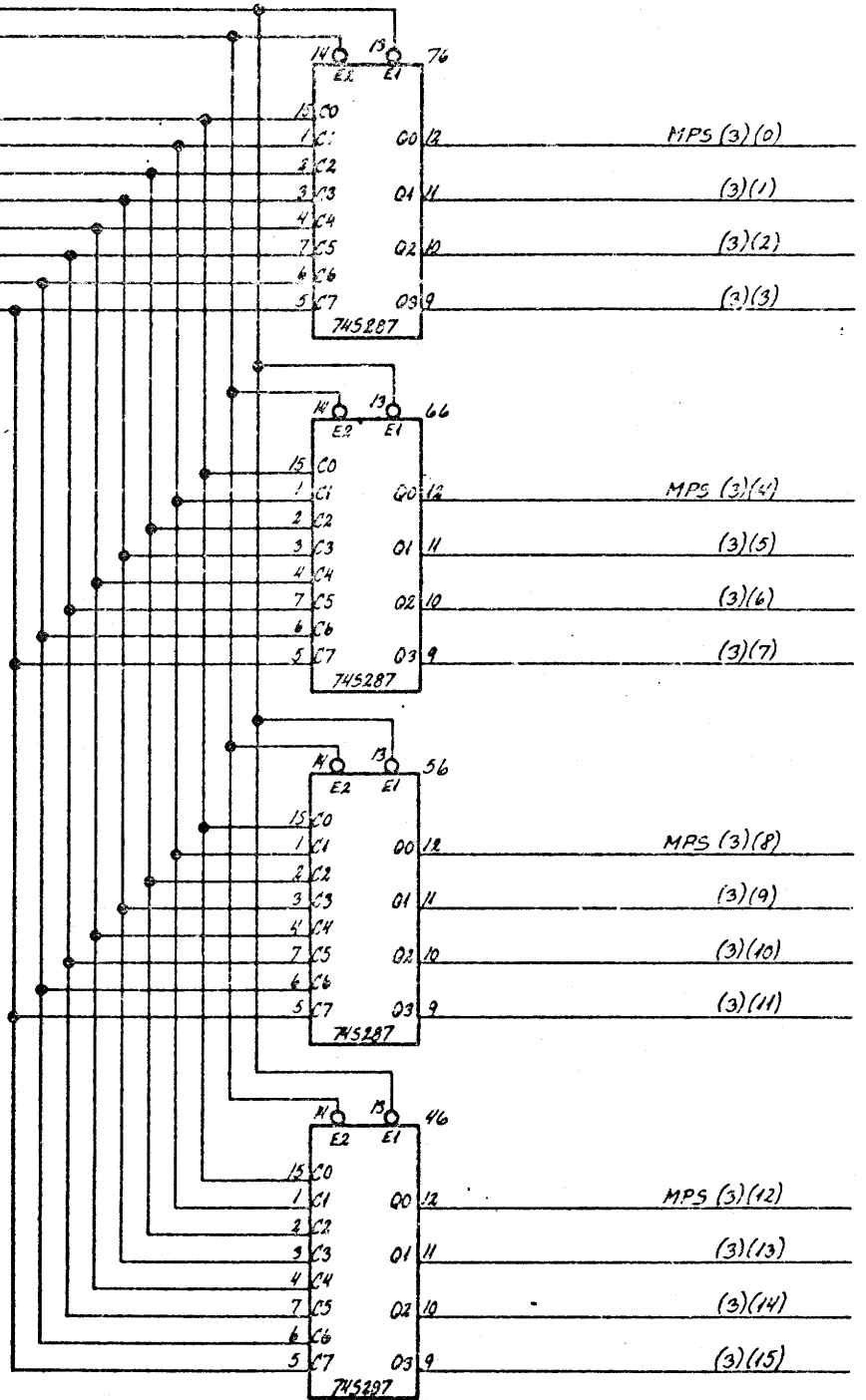
CPU 801

R 11395

MICRO PROGRAM STORE
 WORDS (1024-1535), BITS (16-31)

15 57-12 7 MPSSELECT (3)
 15 27-3 MPSADDR (3)

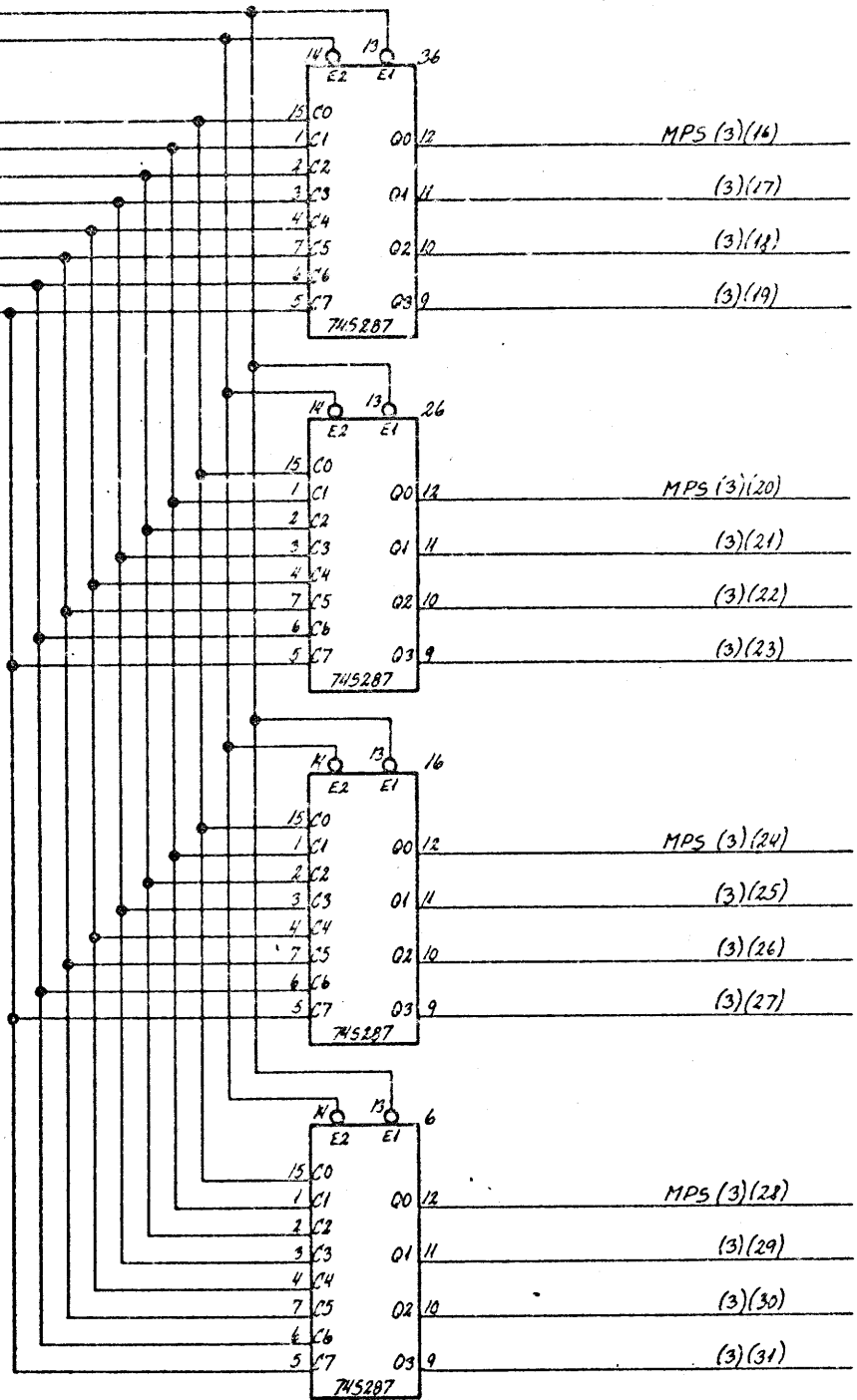
16 47-3 MPSADDR (4)
 16 47-6 (5)
 16 47-8 (6)
 16 47-11 (7)
 17 37-3 (8)
 17 37-6 (9)
 17 37-8 (10)
 17 37-11 (11)



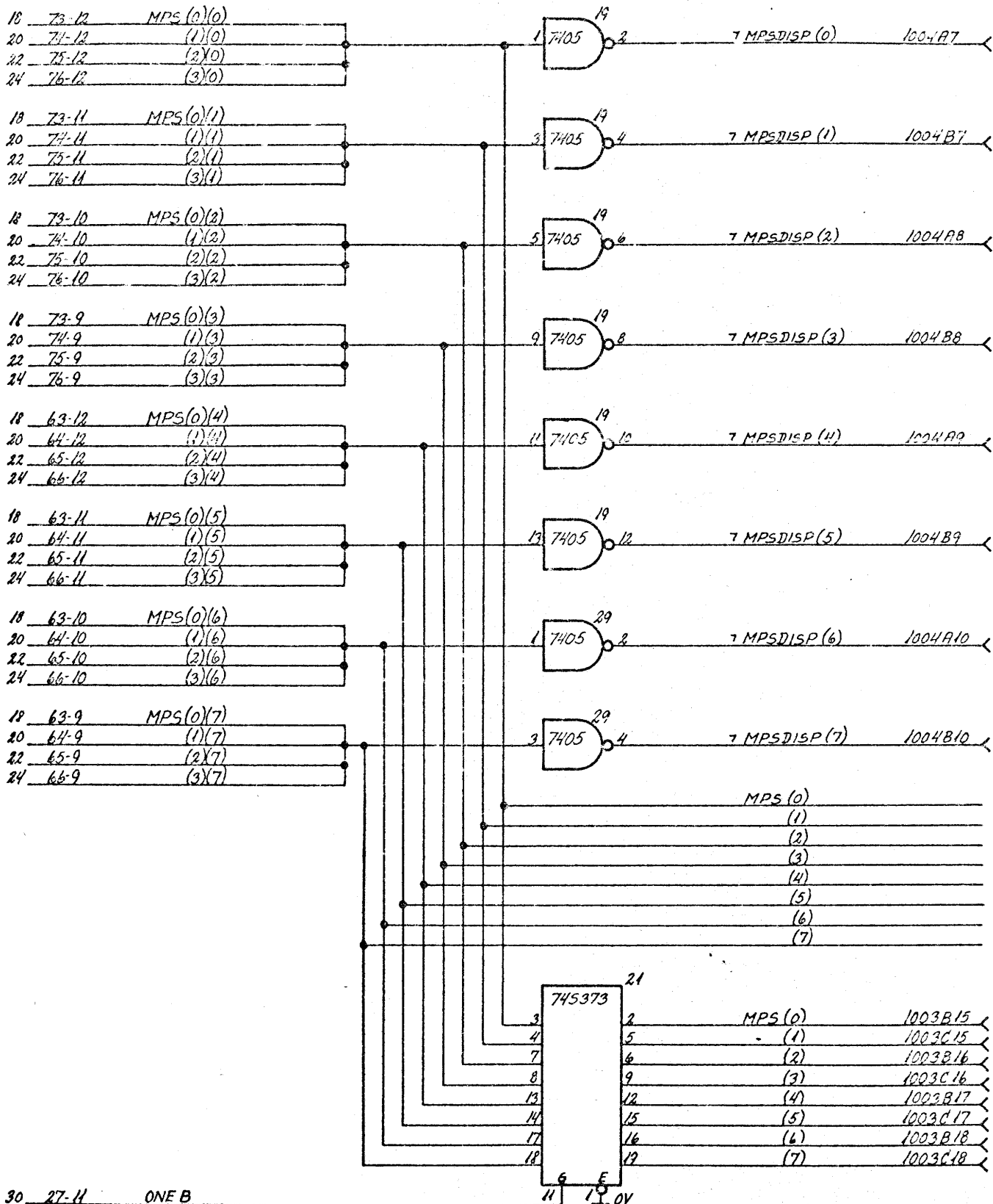
7309M AND 730915 ADD

15 57-12 → MPSSELECT (3)
 15 27-3 MPSADDR (3)

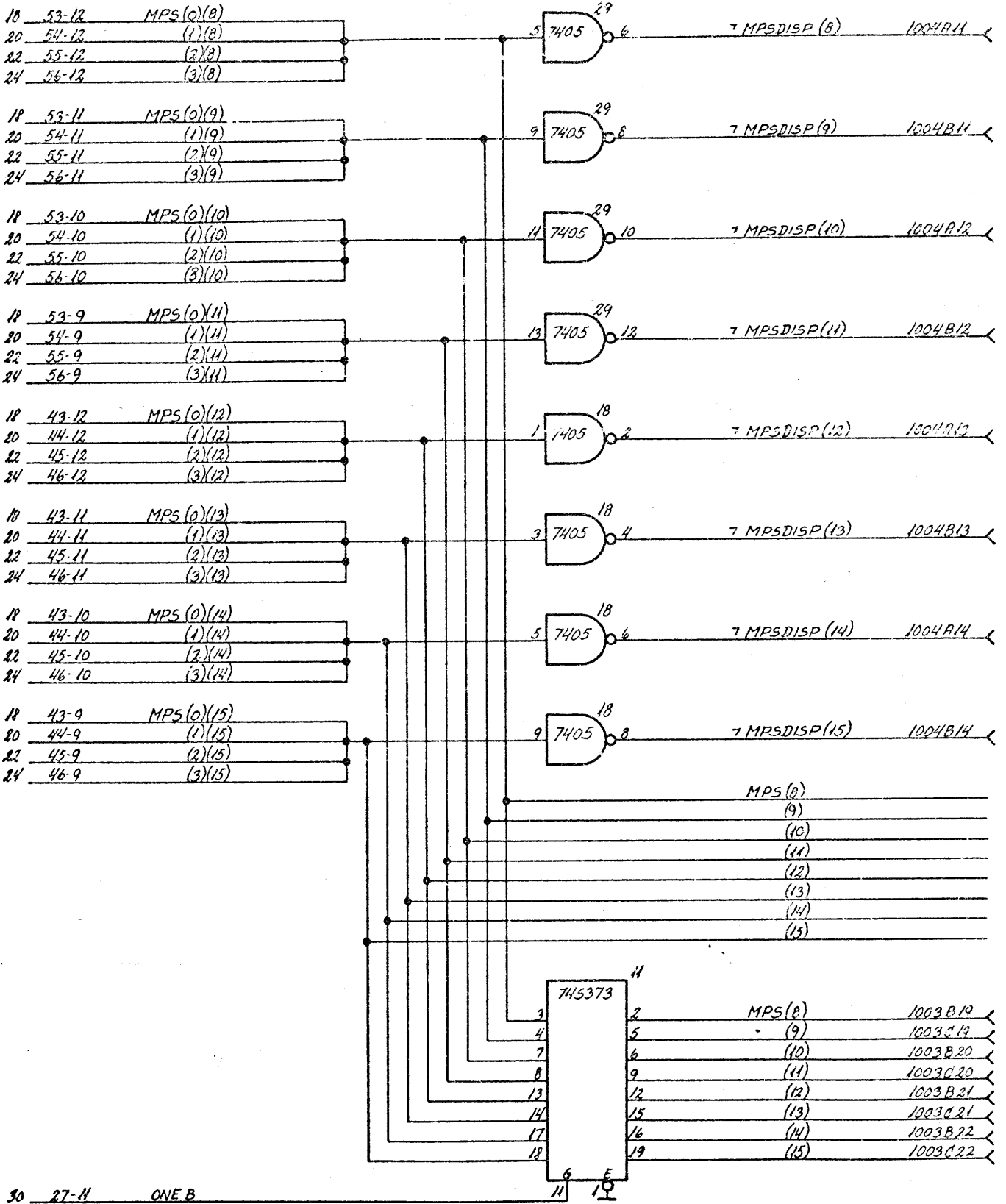
16 47-3 MPSADDR (4)
 16 47-6 (5)
 16 47-8 (6)
 16 47-11 (7)
 17 37-3 (8)
 17 37-6 (9)
 17 37-8 (10)
 17 37-11 (11)



7309M ARR 730915 RDD

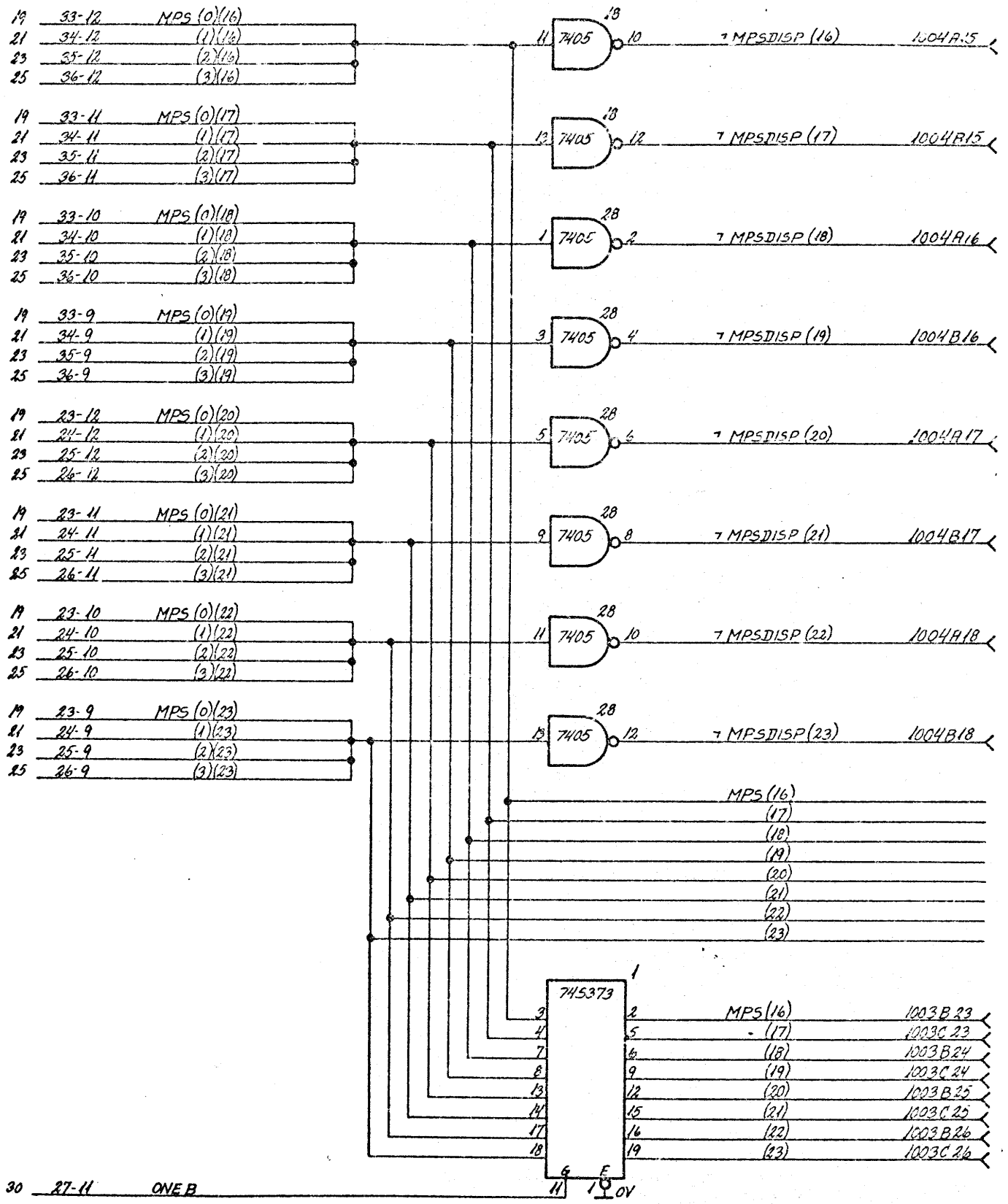


760113 ARJ 760130 ROB



76013 MPJ 760131 ROB

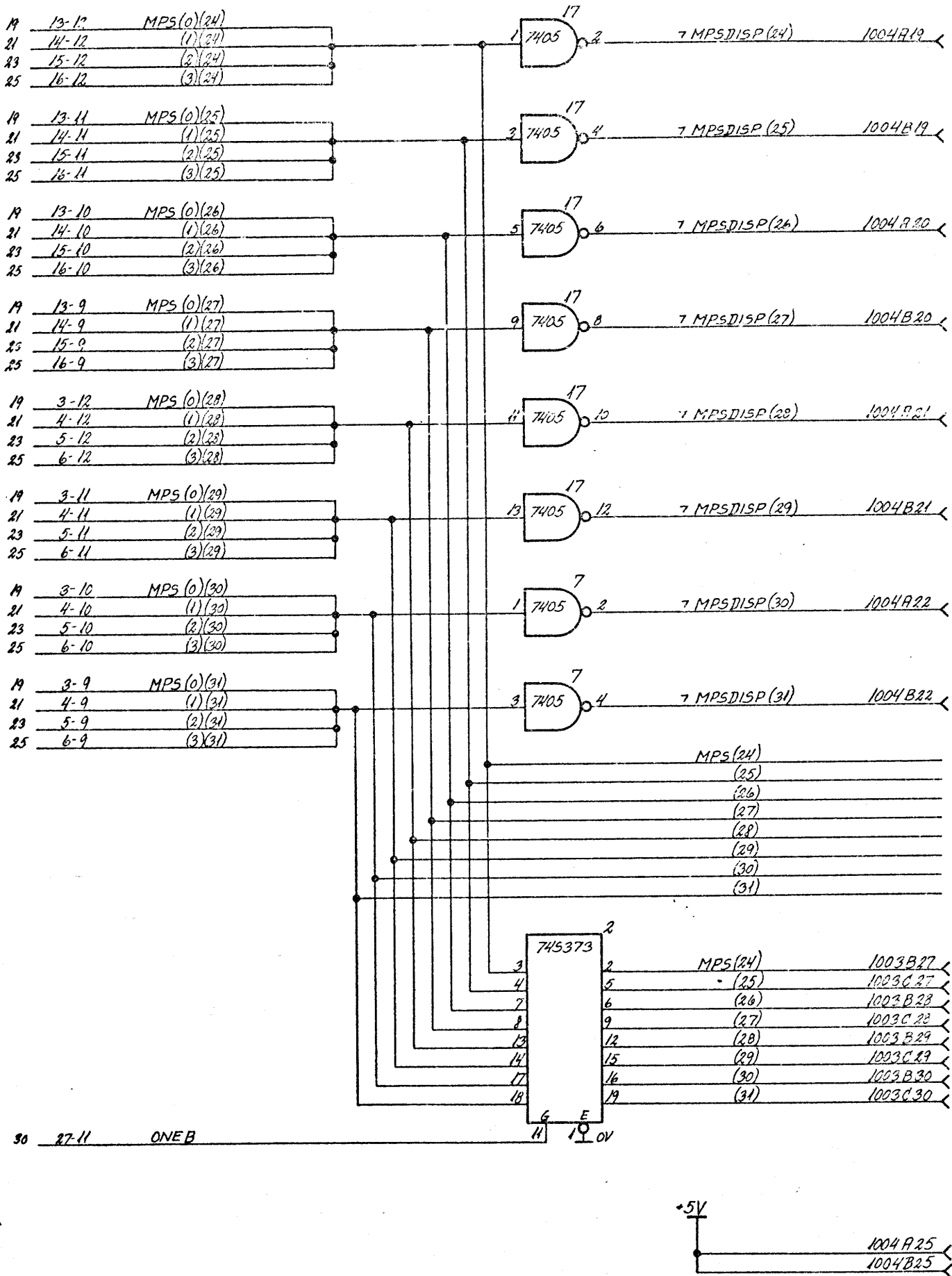
760113 P87 760131 ACB



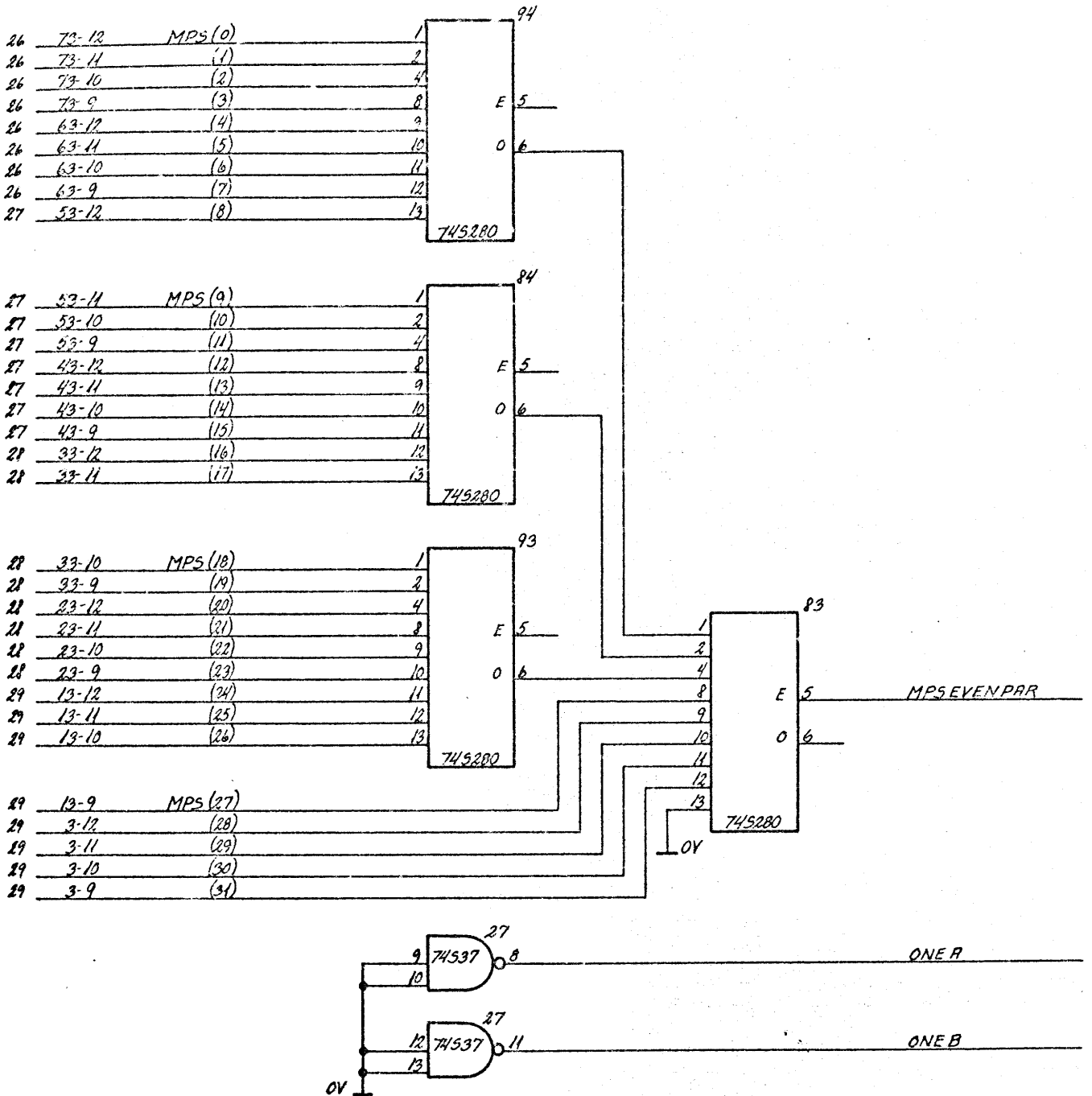
CPU801
R14400

MICROPROGRAM STORE OUTPUT
MPS (16-23)





76019 ARJ 76031 ROB



750926 AR7 780201 A08

CPU801 PROMS

	POS. NO.	ROM NO.
ADDRESS TABLE FOR ADDRESS CALCULATIONS	108	124
	109	125
	110	126
ADDRESS TABLE FOR INSTRUCTION EXECUTION	98	216
	99	219
	100	220
MICROPROGRAM STORE 0 : 511	73	342
	63	343
	53	132
	43	133
	33	134
	23	135
	13	136
	3	137
MICROPROGRAM STORE 512 : 1023	74	334
	64	335
	54	336
	44	337
	34	338
	24	339
	14	340
	4	341
MICROPROGRAM STORE 1024 : 1535	75	243
	65	244
	55	245
	45	246
	35	247
	25	248
	15	249
	5	250
MICROPROGRAM STORE 1536 : 1791	76	154
	66	198
	56	156
	46	199
	36	158
	26	159
	16	160
	6	161

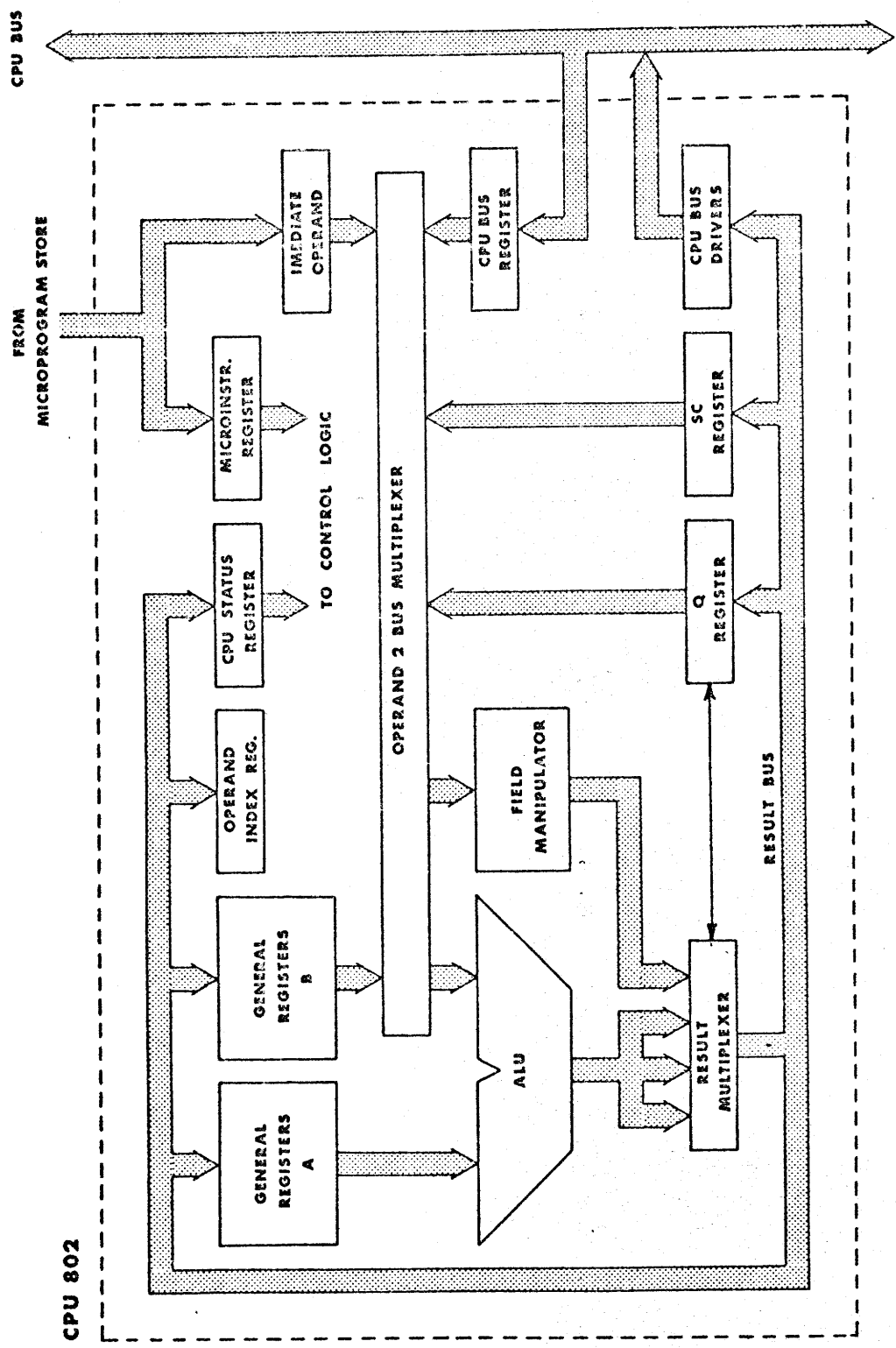
AAJ

~~15.6.76~~

~~28.9.76~~

13.10.76

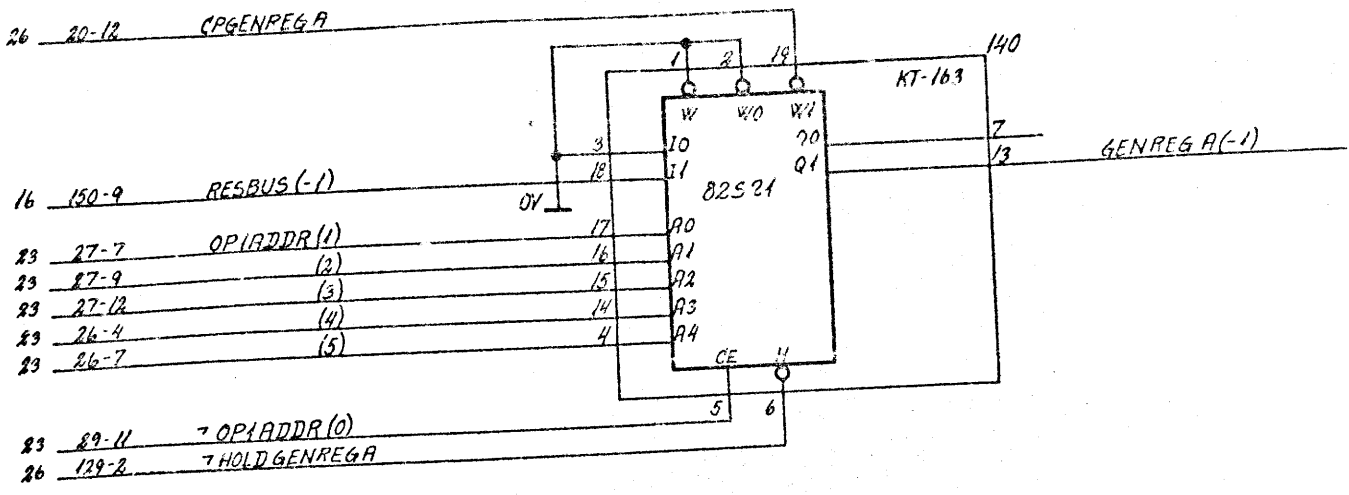
DC doc. V8 140	Designed by 76110 AAJ	Drawn by 76110 AOB	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.
----------------	--------------------------	-----------------------	-------------------	--------------	-------------------	------------	----------------------



CPU 802

Unit
CPU 802
Dwg. No.
R 11652

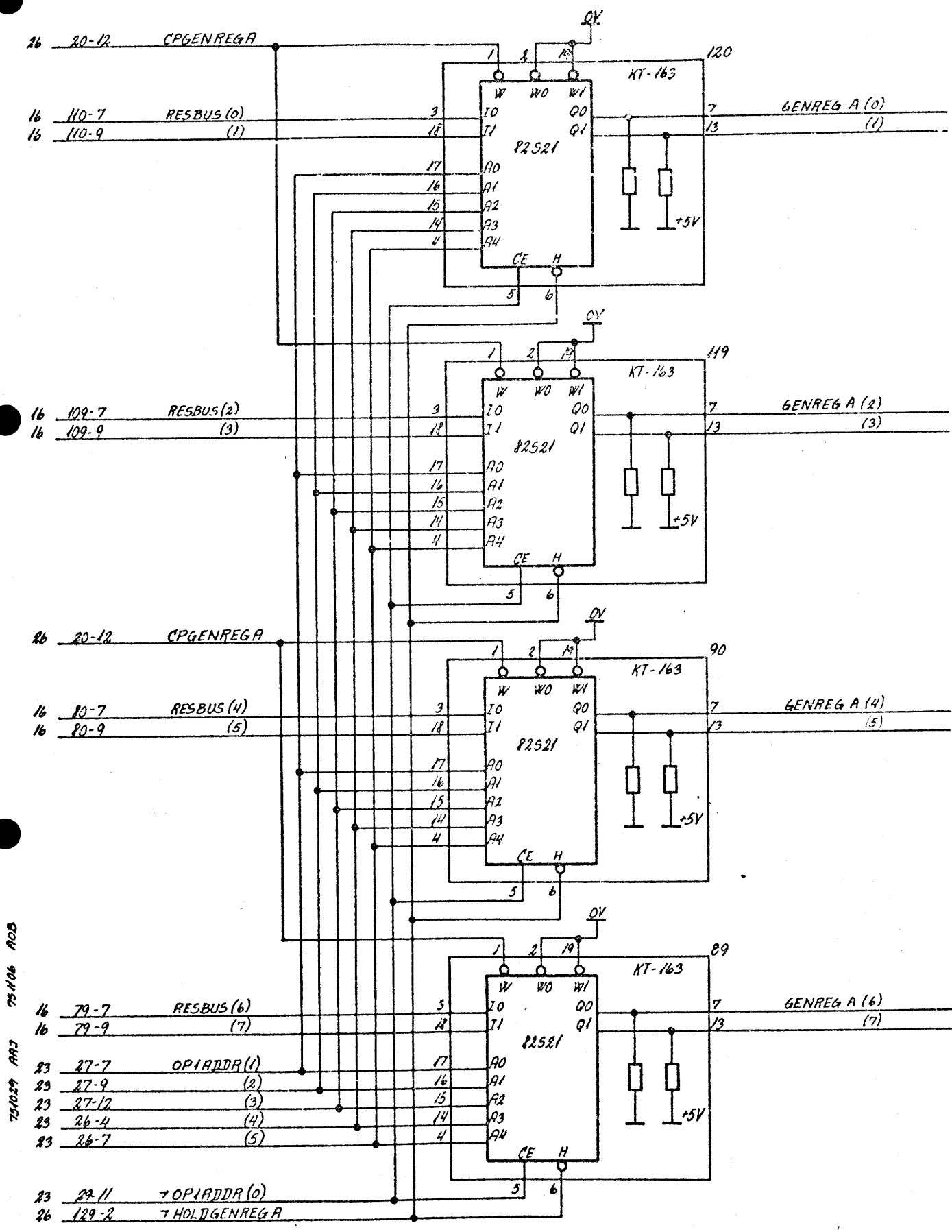
CPU 802 BLOCK DIAGRAM



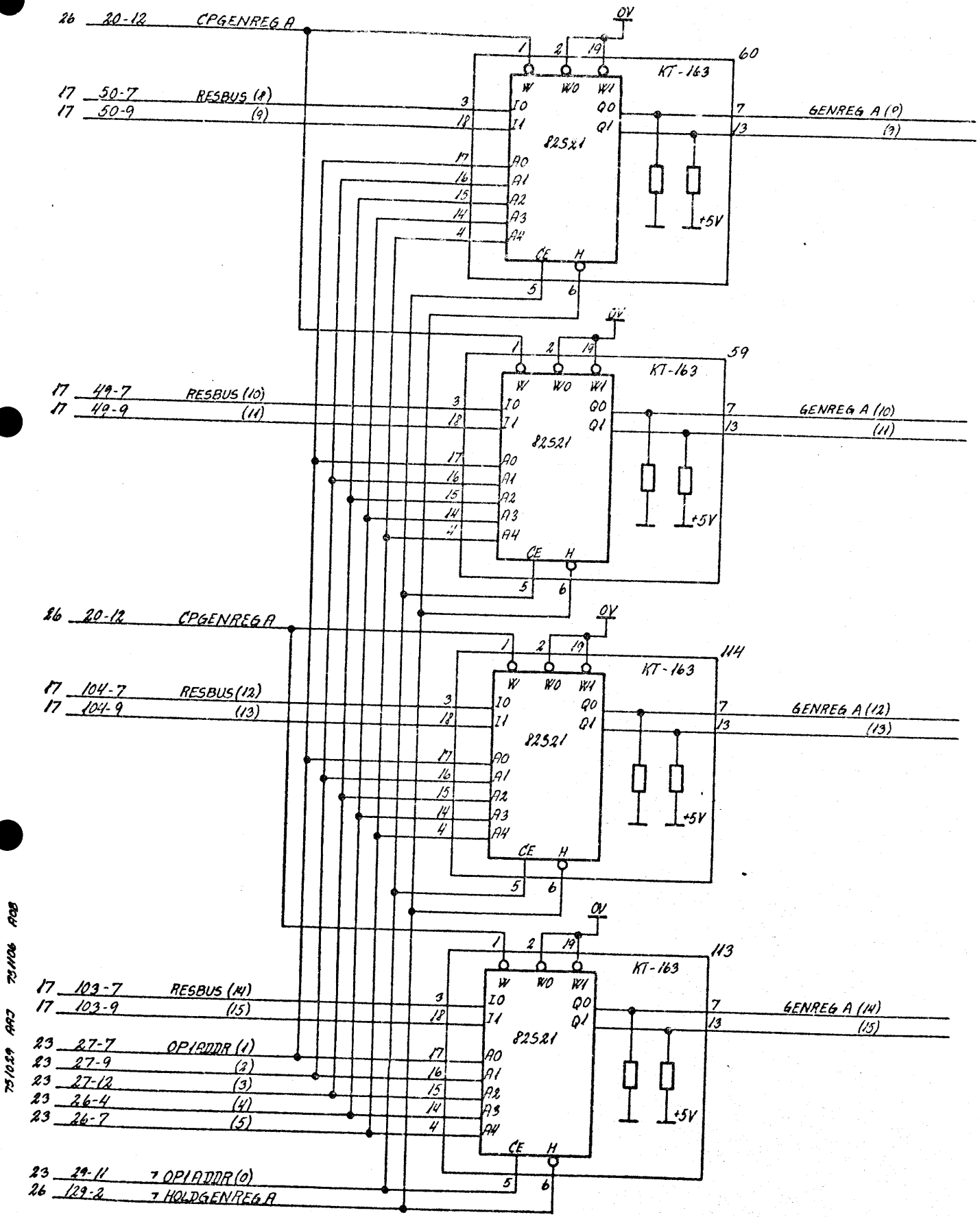
75113 MR3 75127 RO3

CPU802
R 11403

GENERAL REGISTERS A(-1)



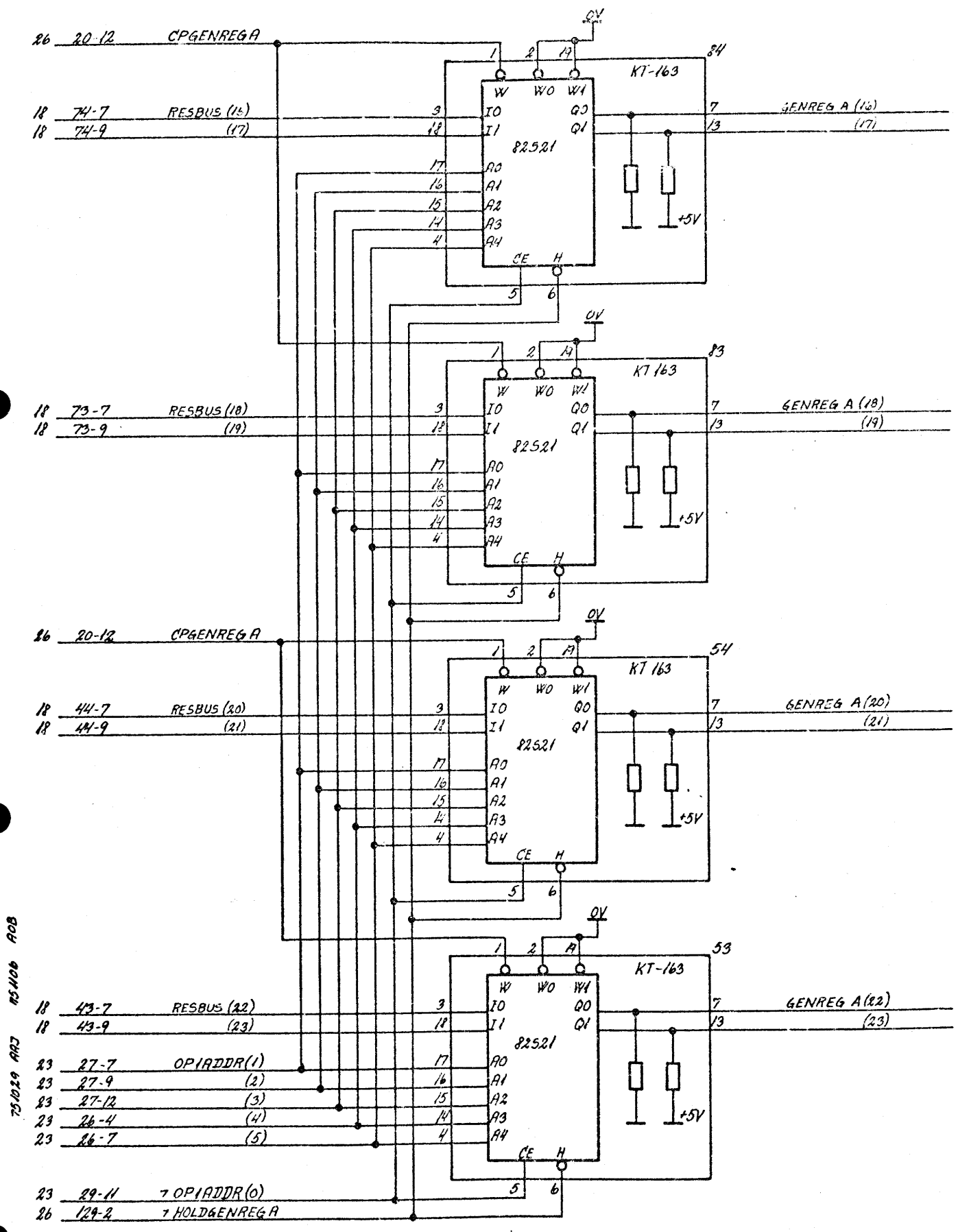
751029 AA7 751106 A0B

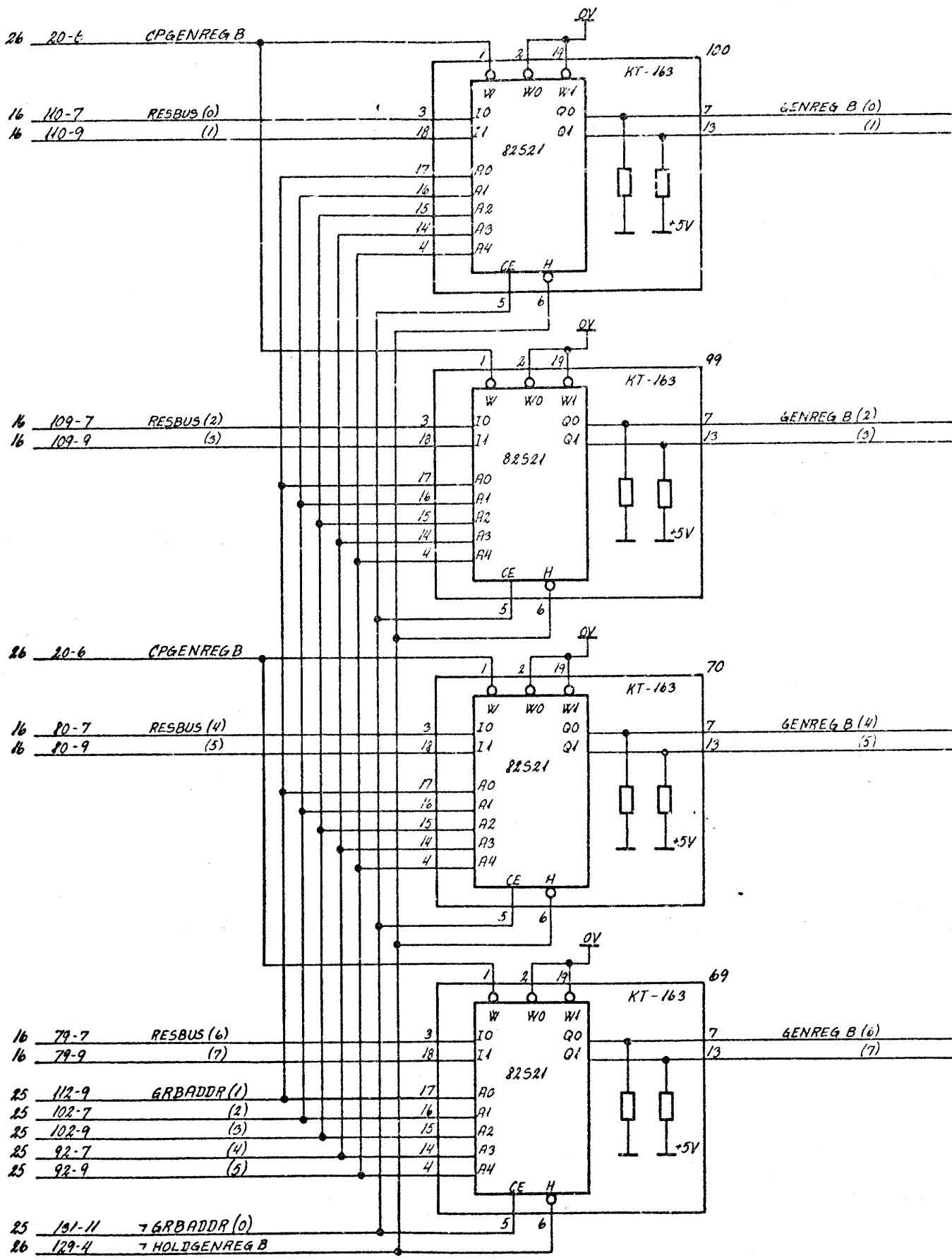


751029 APJ 731026 PDS

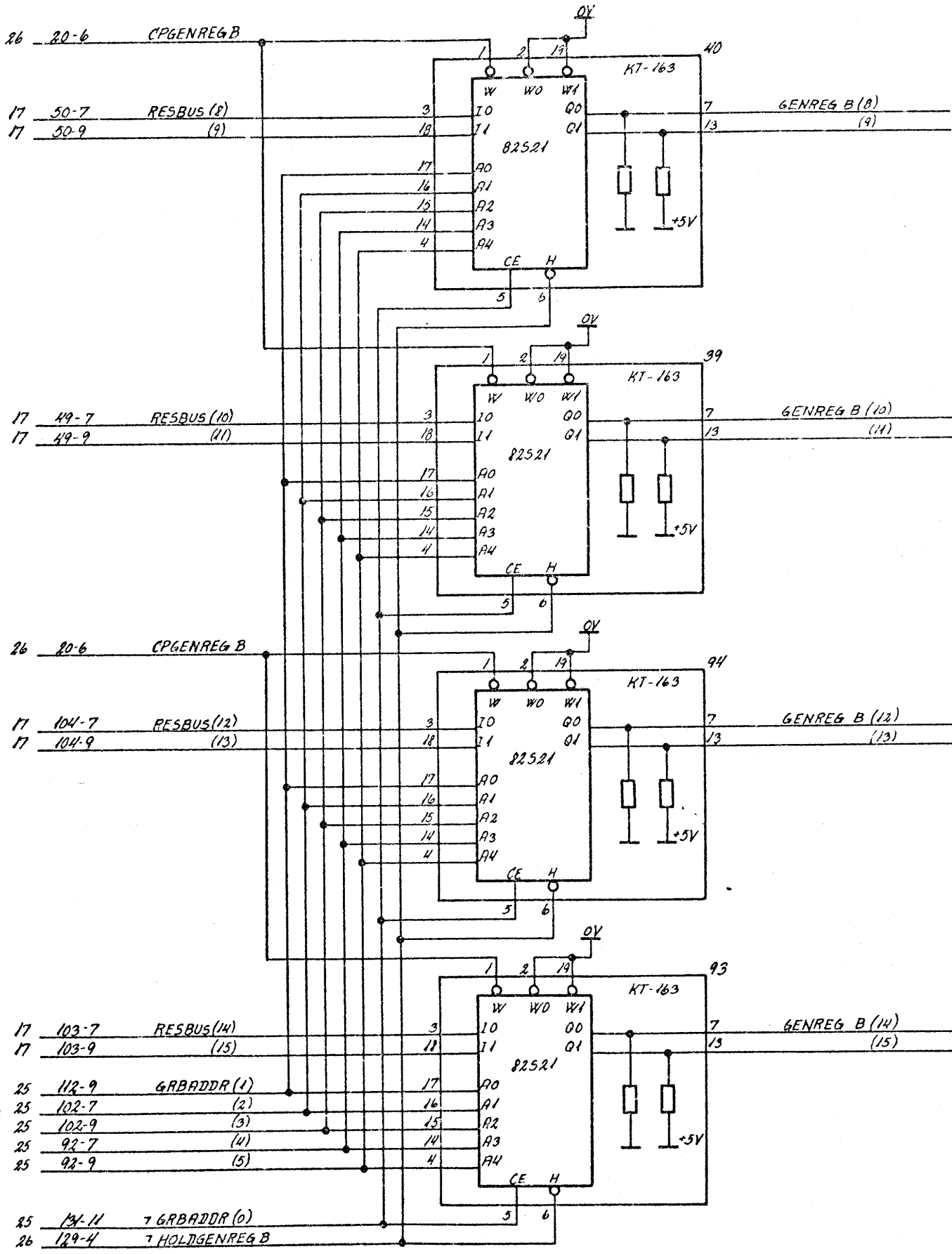
CPU 802
R11405

GENERAL REGISTERS A (8-15)





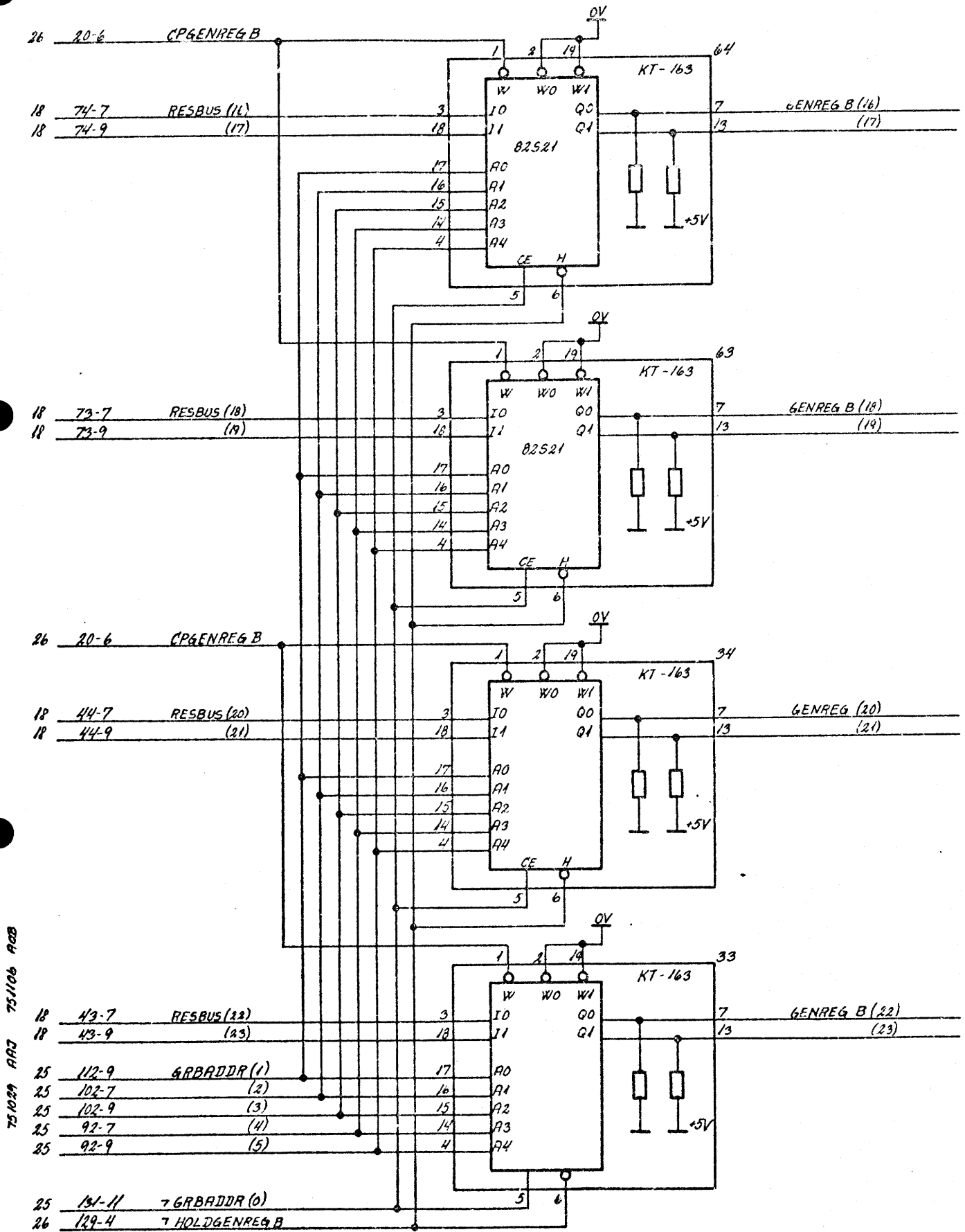
751029 AAJ 751106 AOB



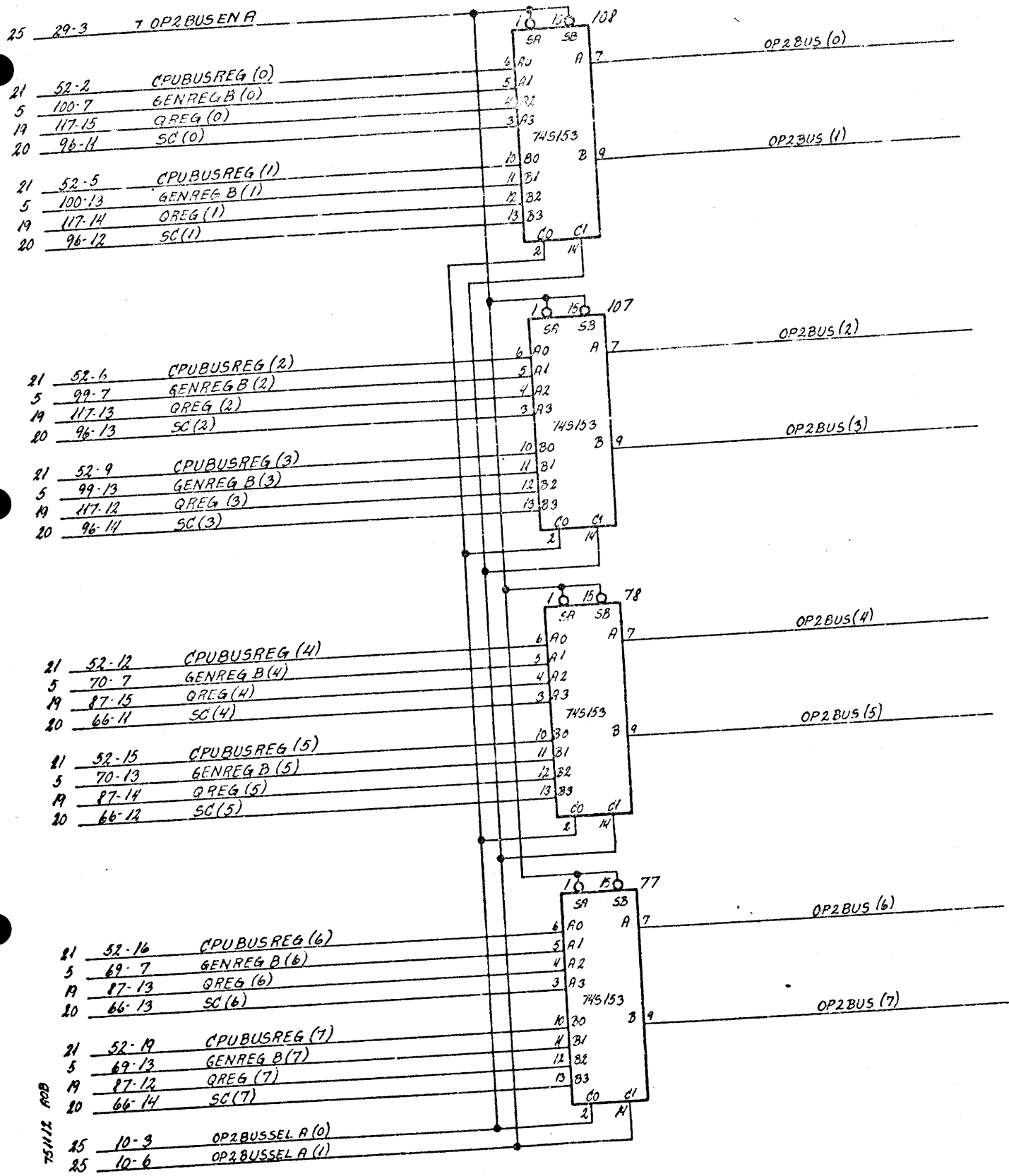
751029 AAJ 751103 AOB

CPU 802
RA1408

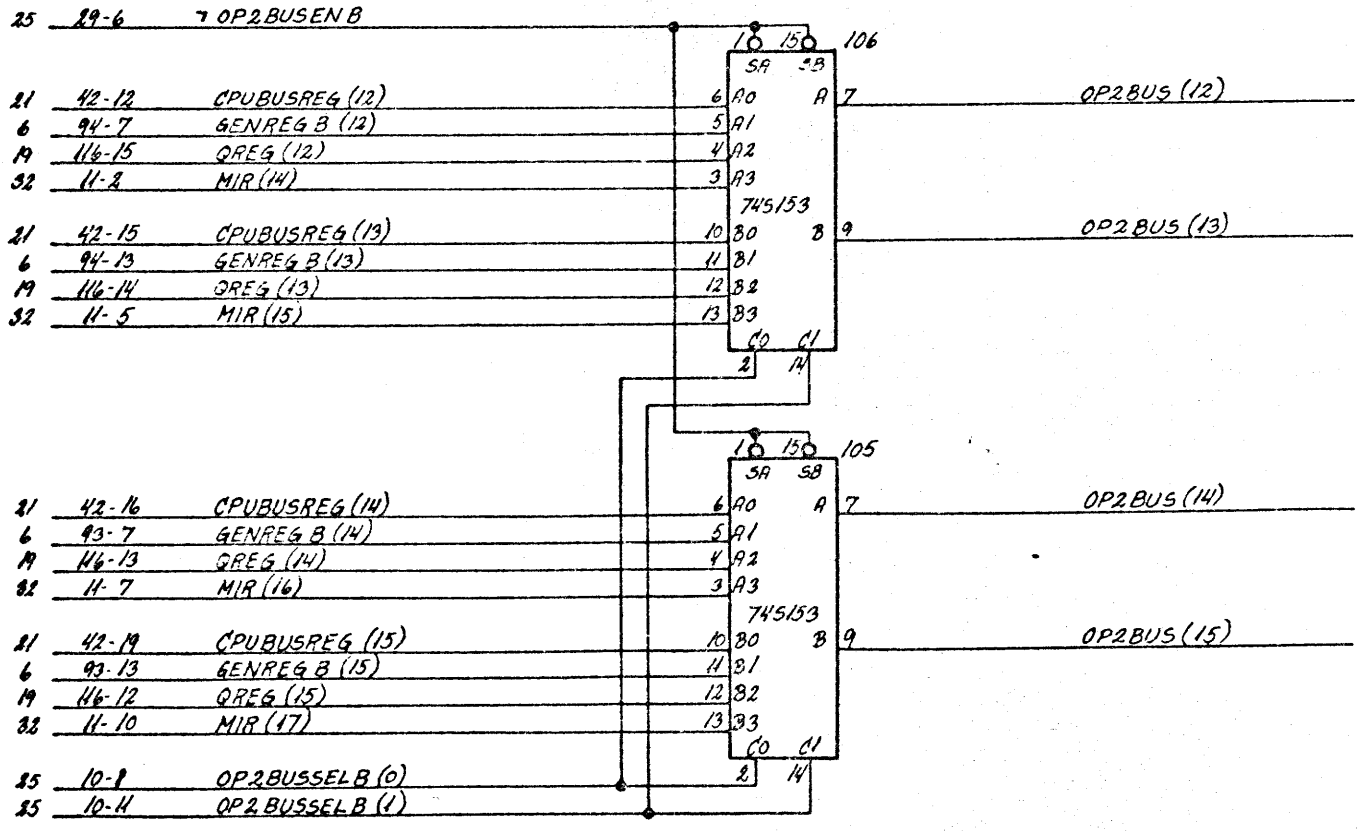
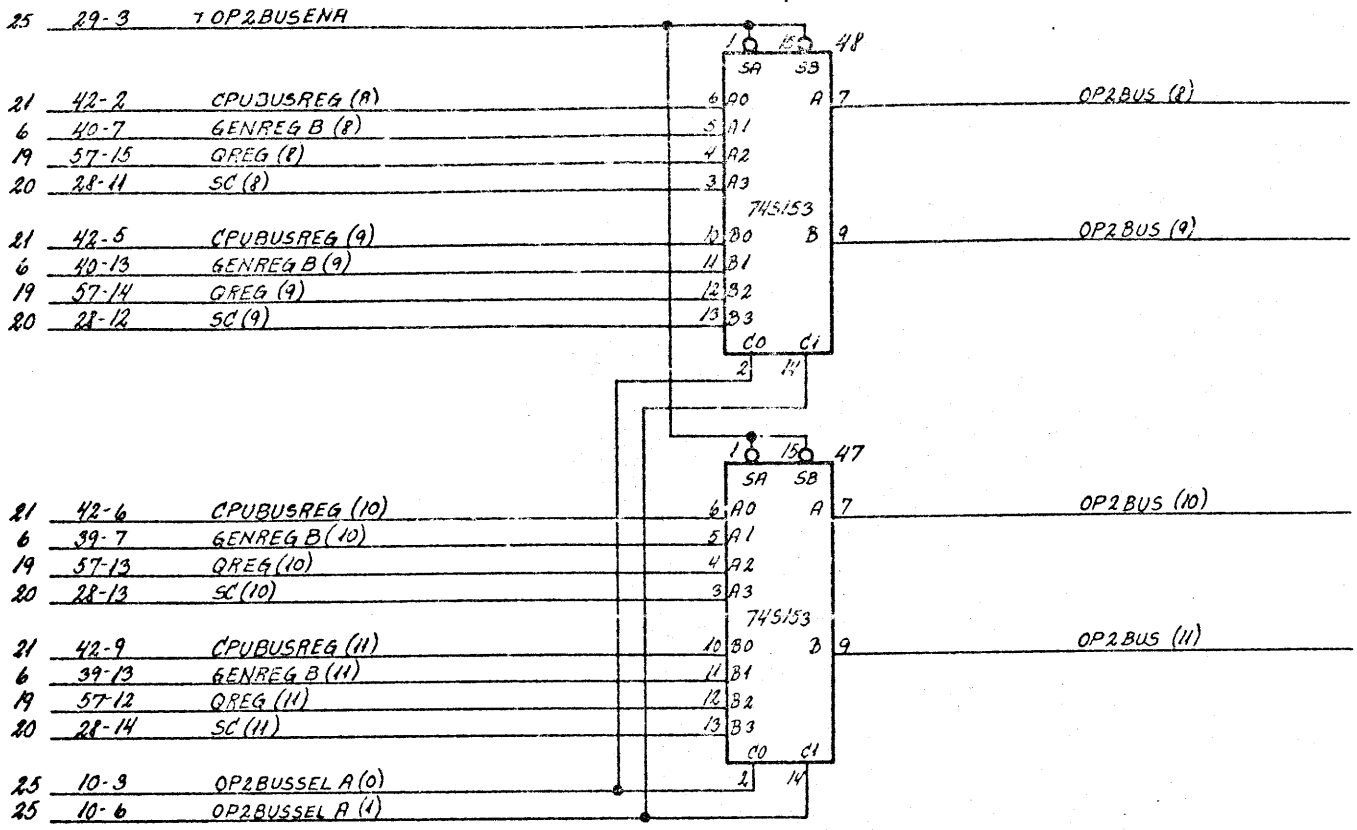
GENERAL REGISTERS B (8-15)



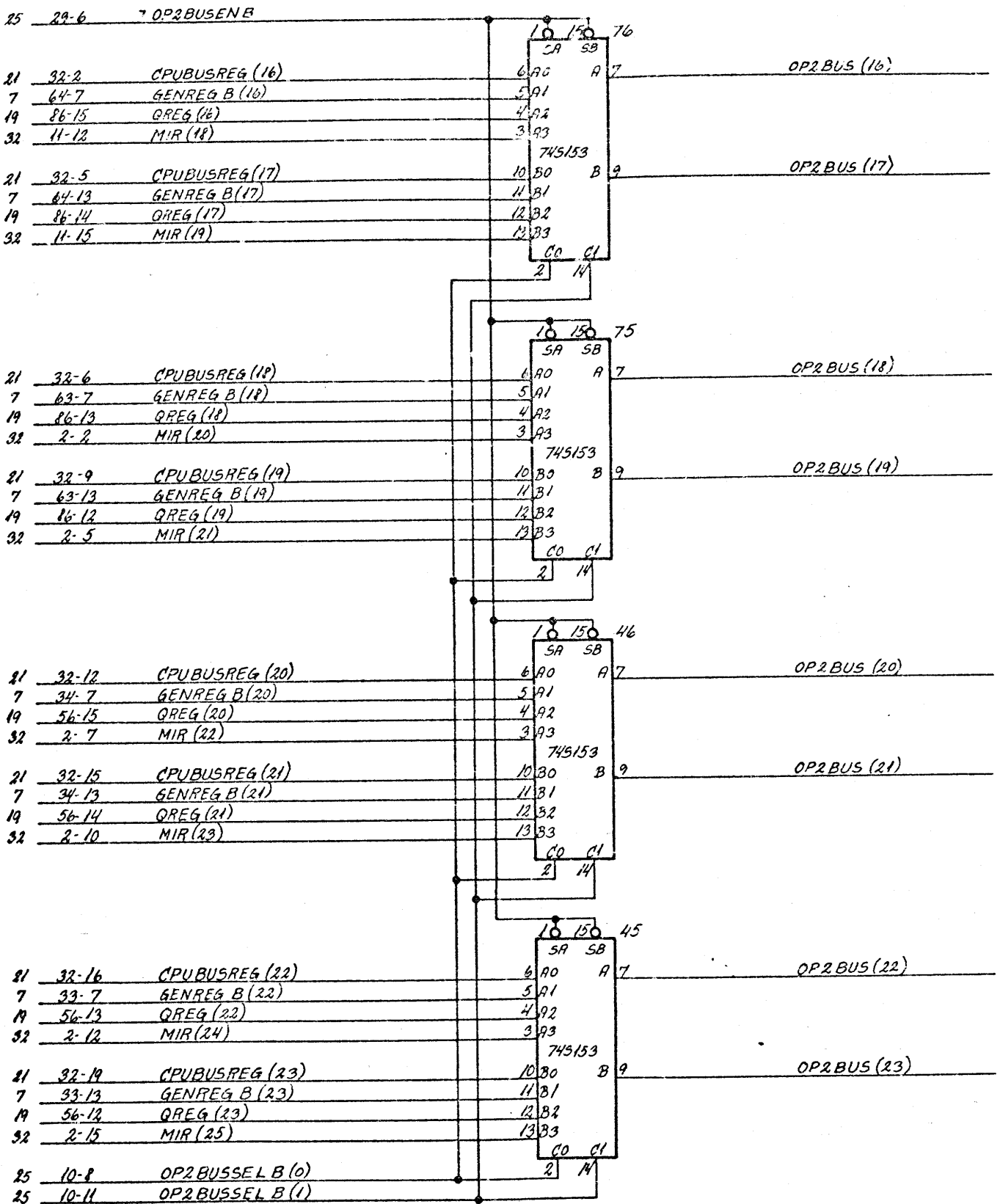
751029 AAJ 751106 AAB



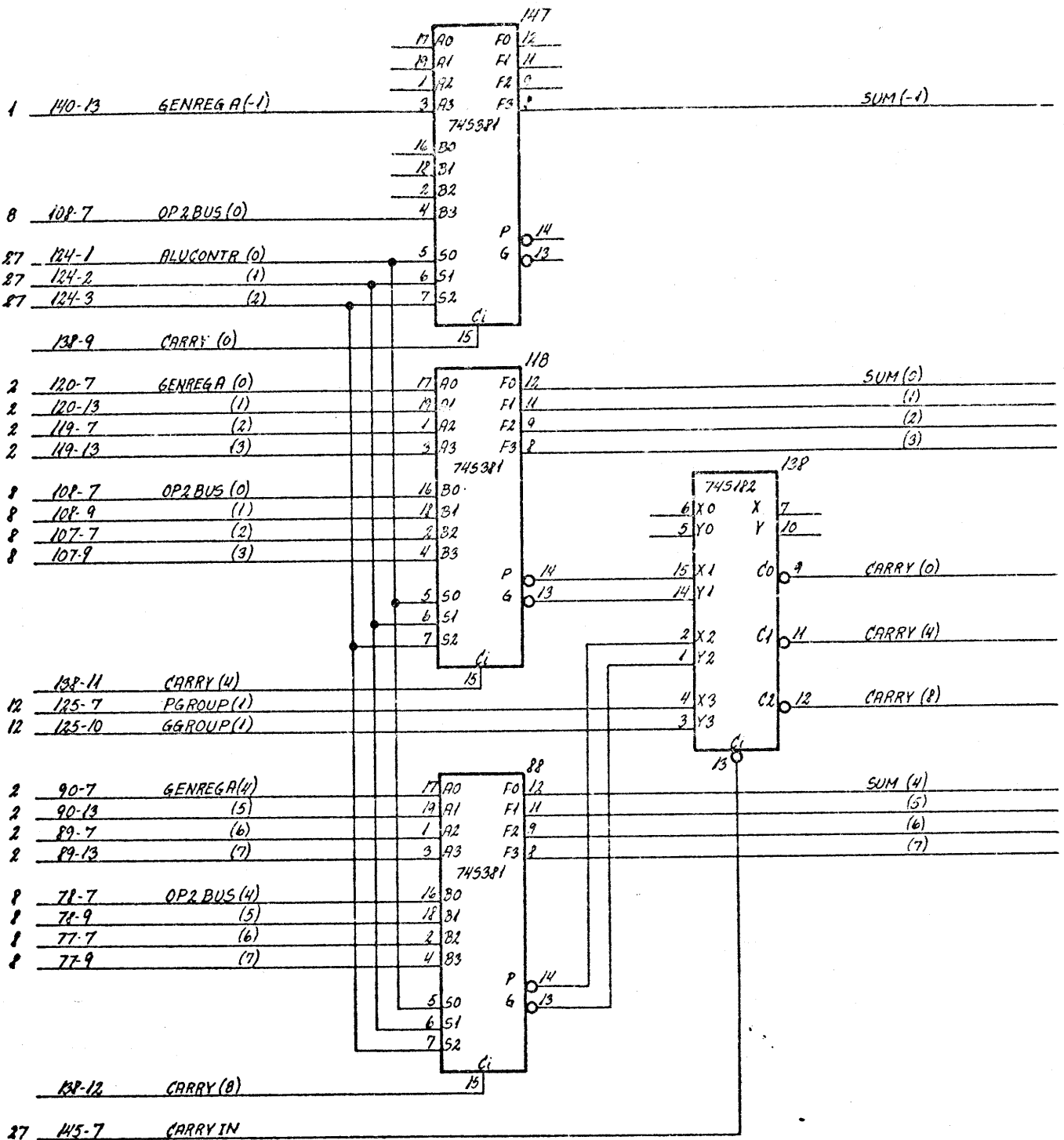
75112 A0B
75112 A07



75112 A08
75112 A07

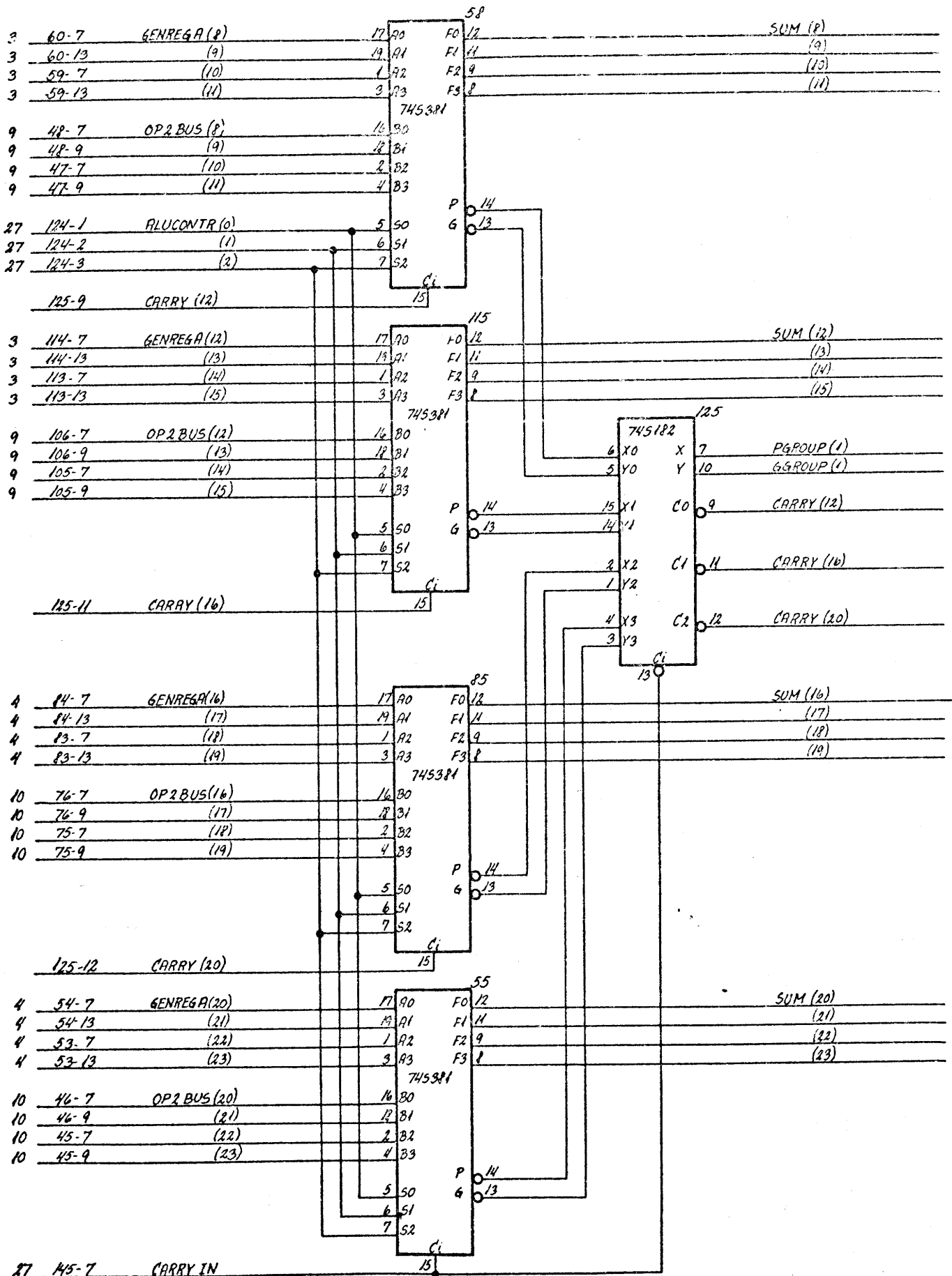


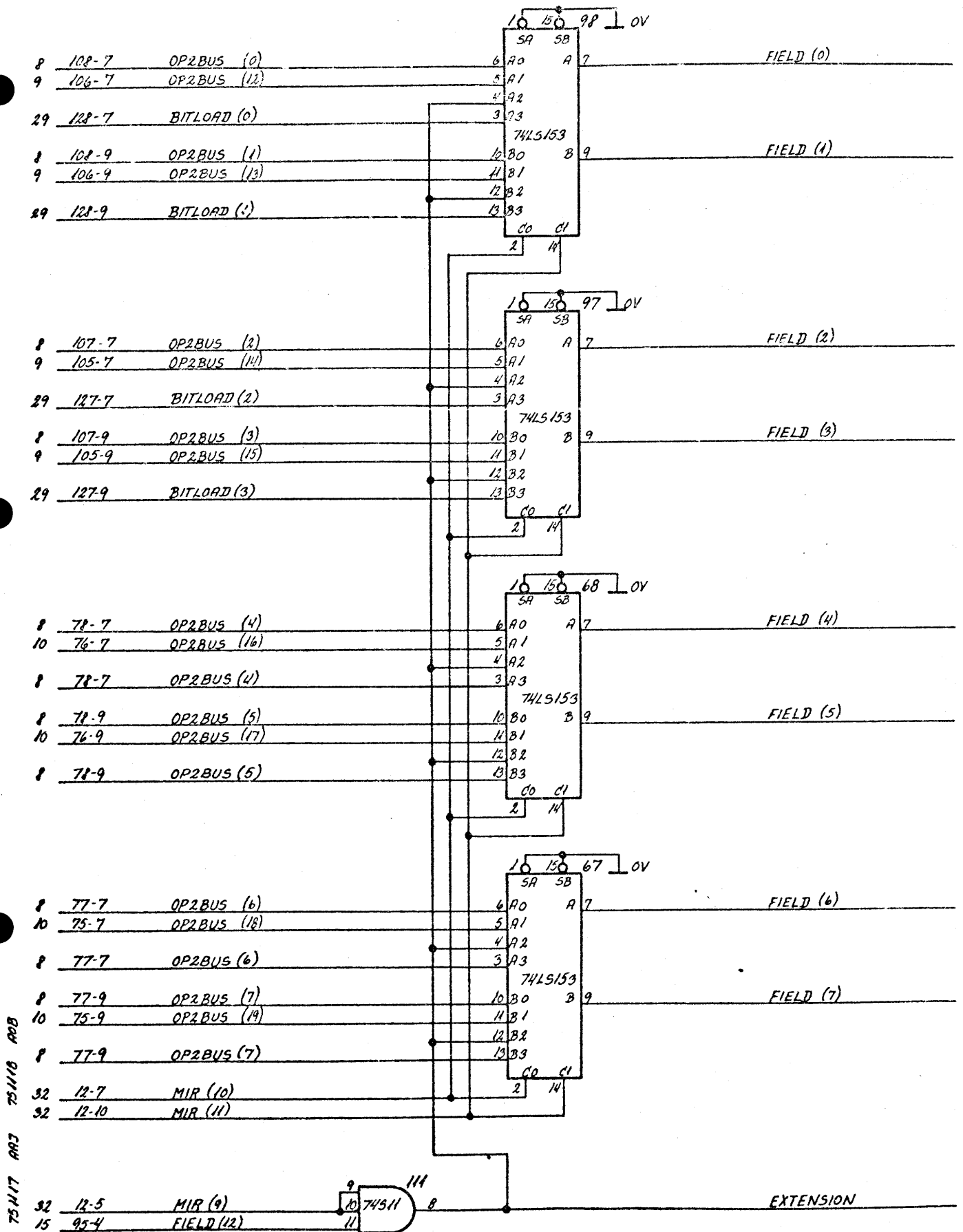
751119 A07 751229 A08

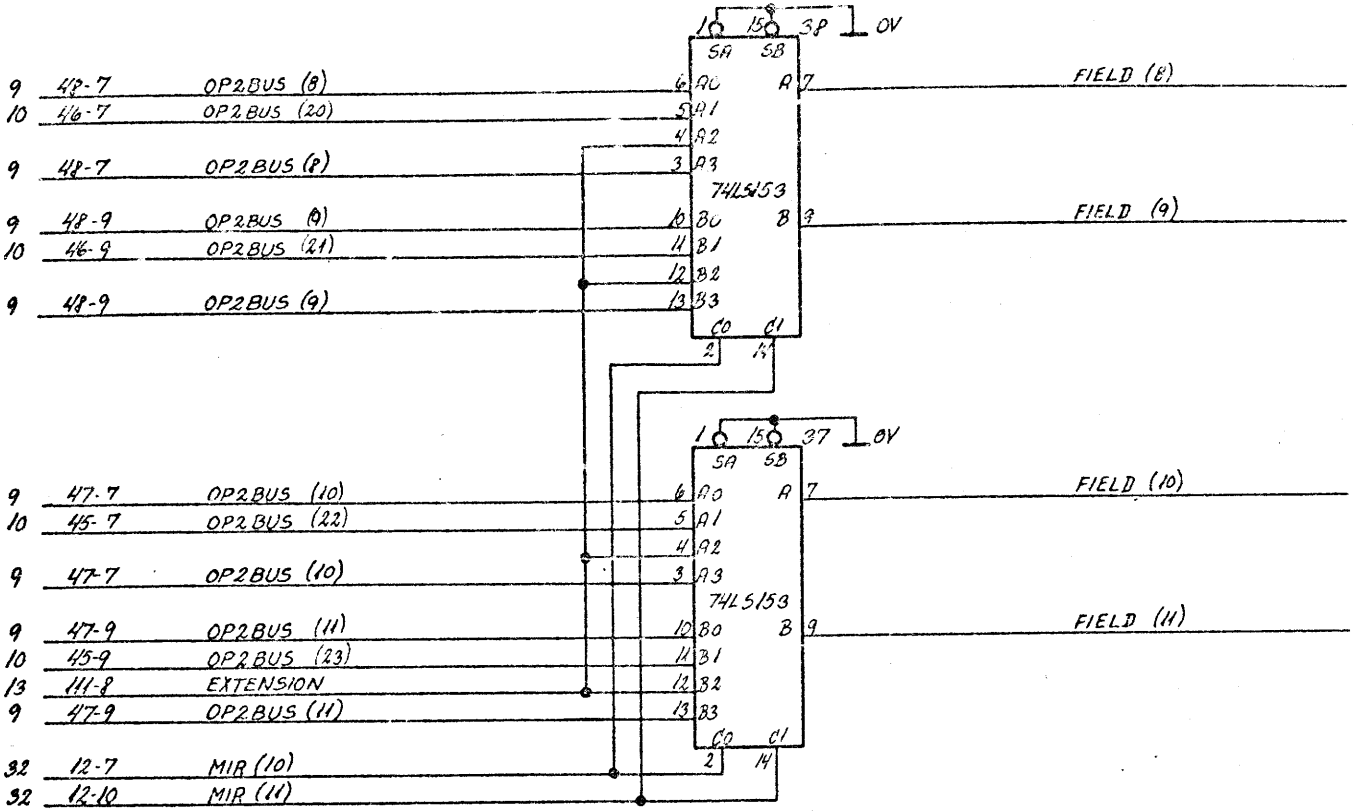


751090 AAJ 751106 AOB

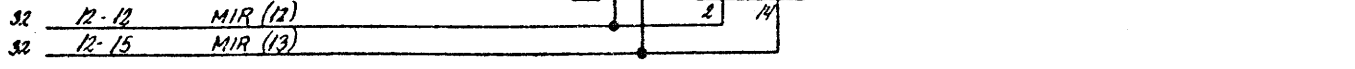
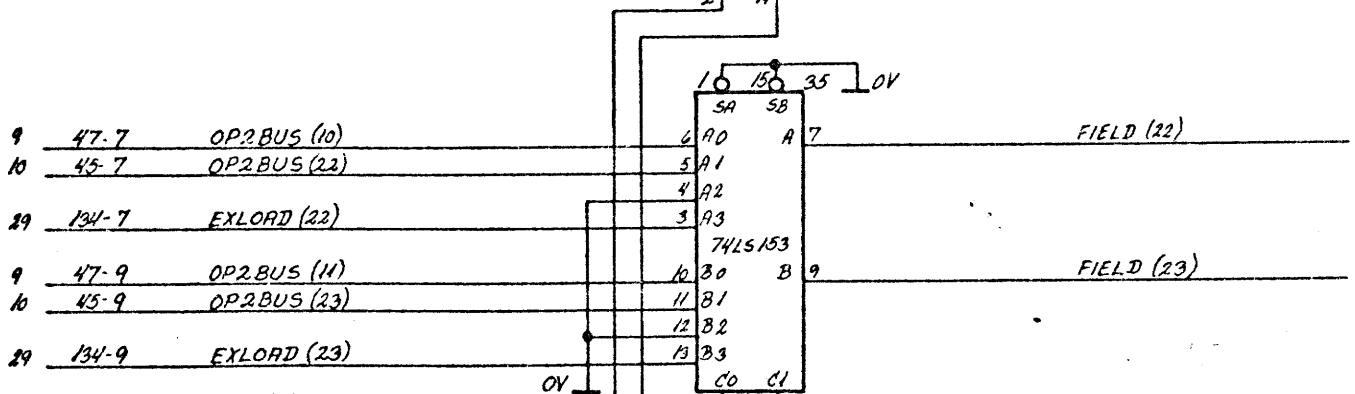
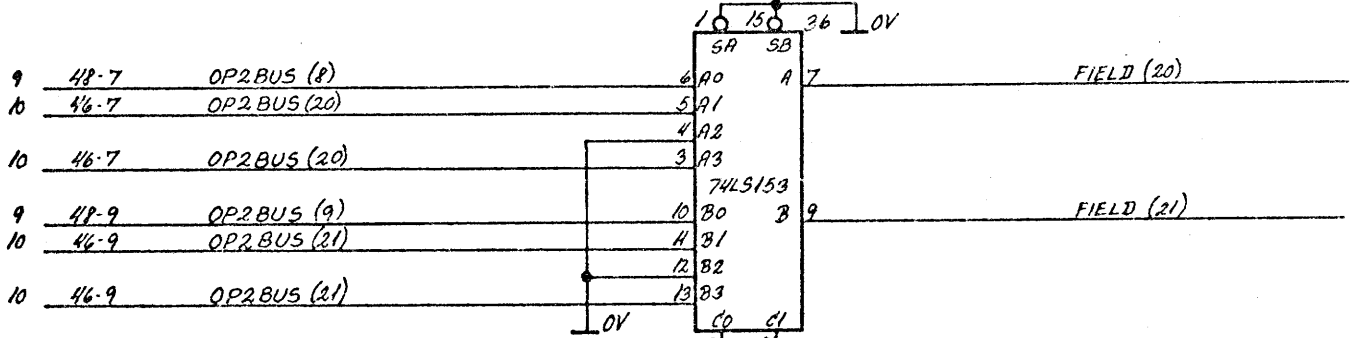
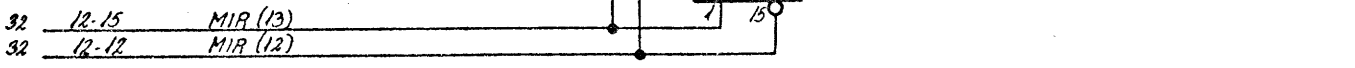
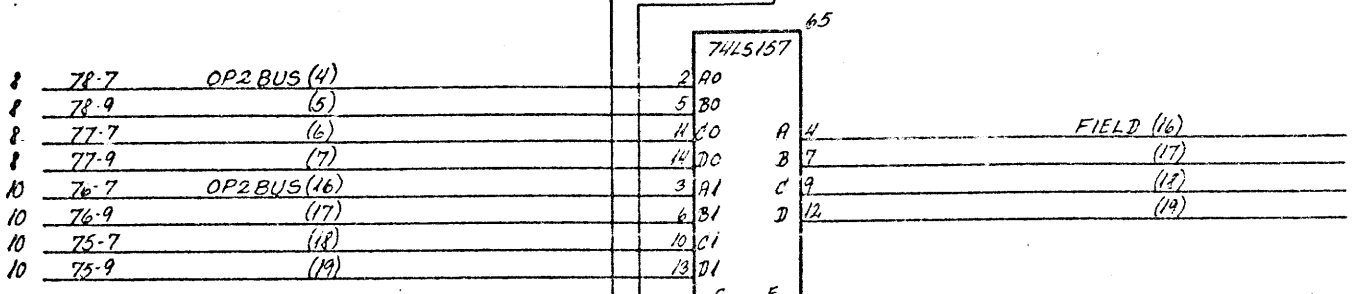
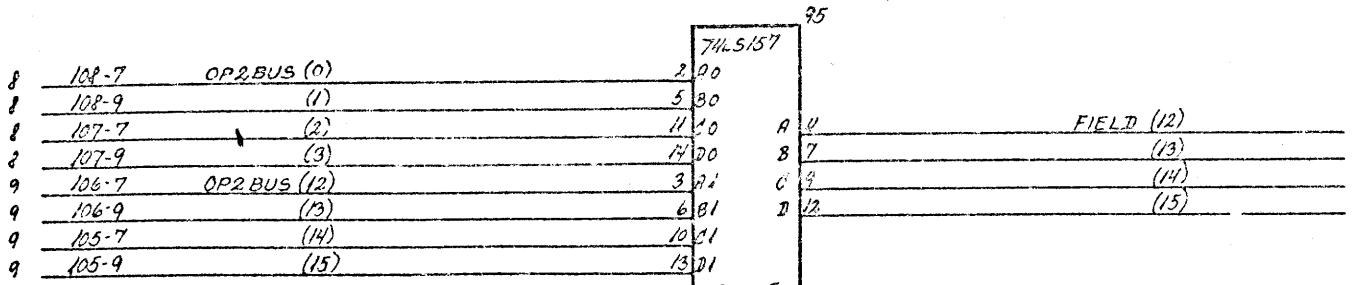
751030 RAJ 751106 ROB



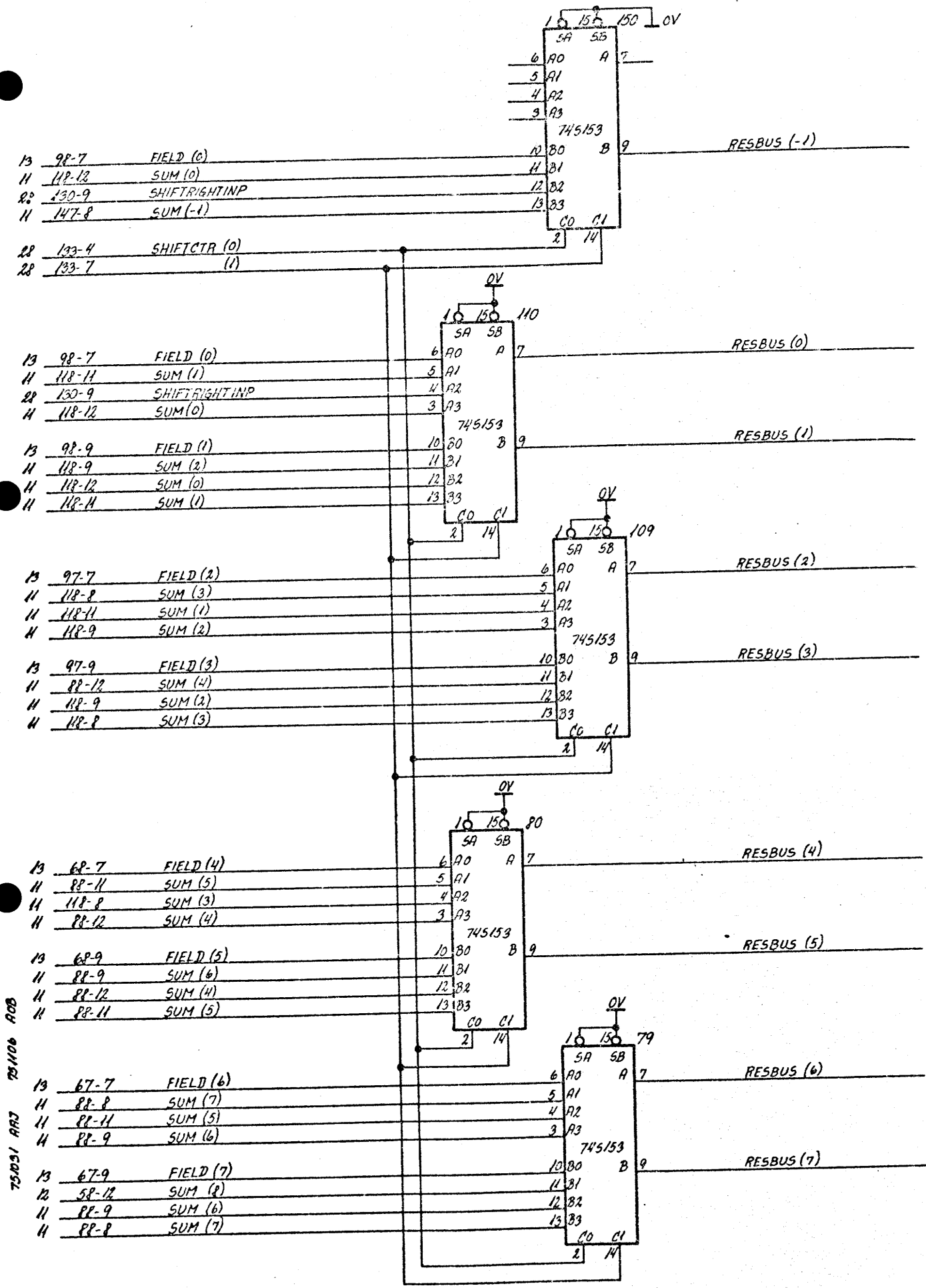




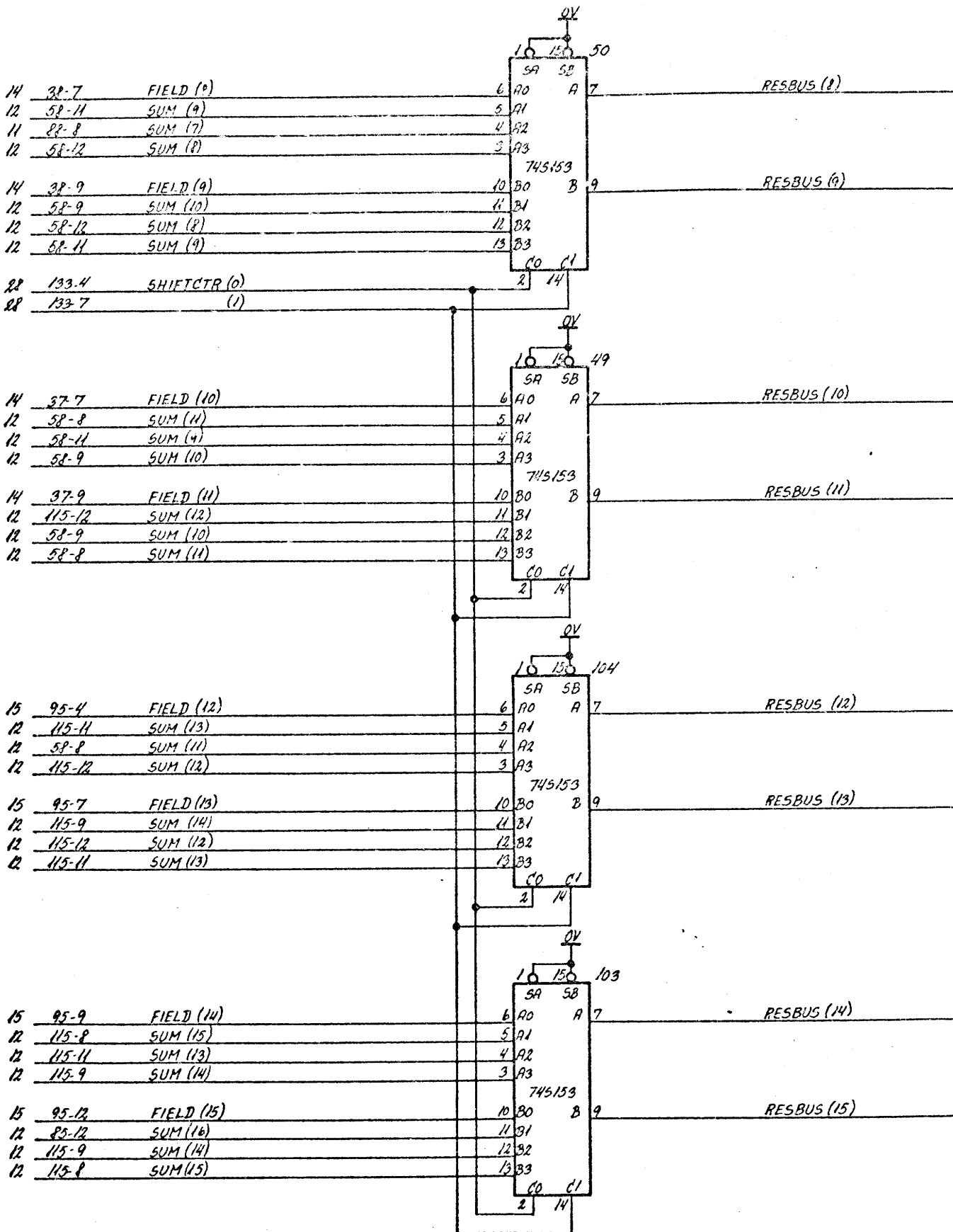
75N17 RA3 75N18 RD3



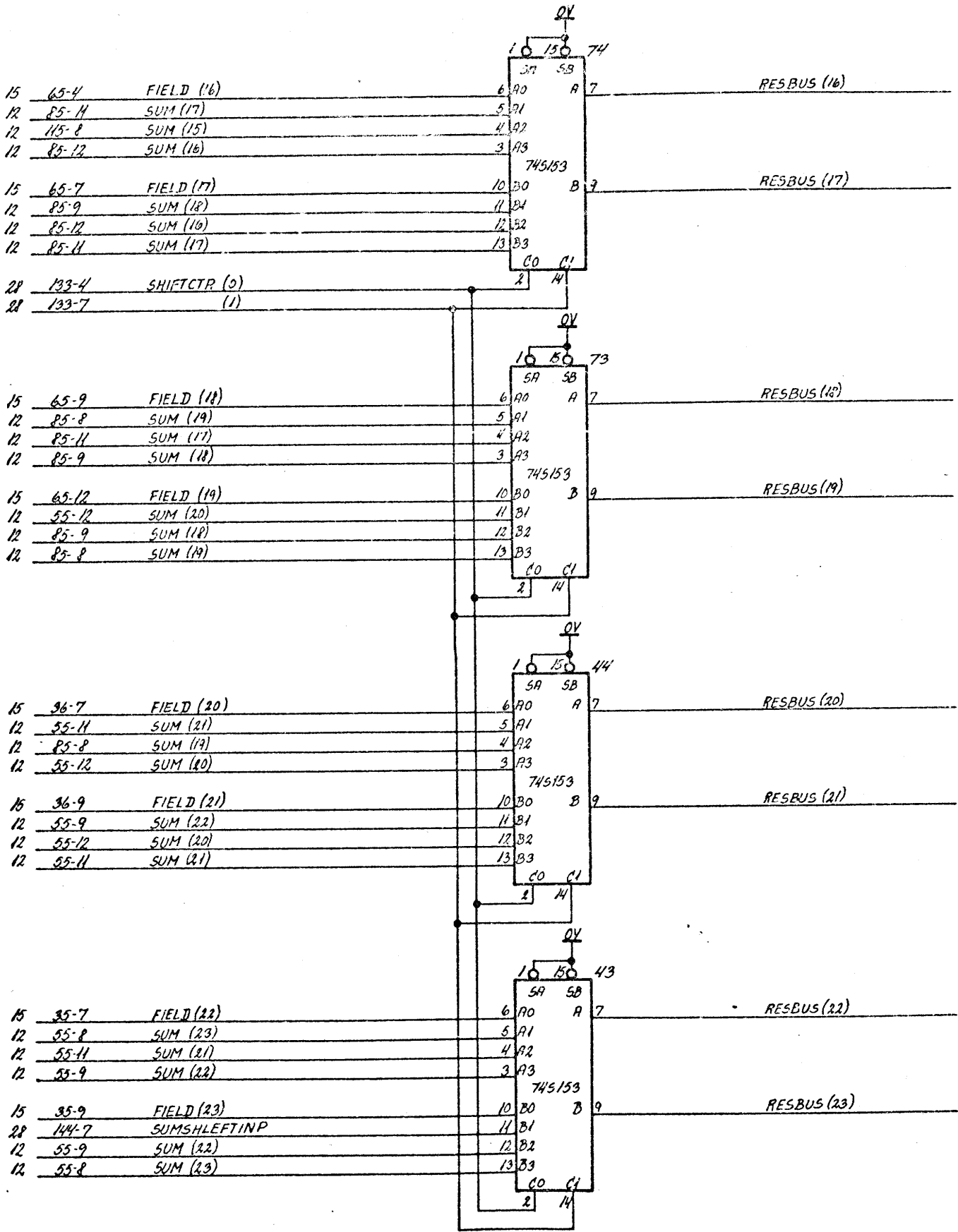
75119 AR3 760108 AR2



CPU 802
 R 11418
 SUM SHIFTER
 AND MULTIPLEXERS FOR RESULT BUS (-1:7)



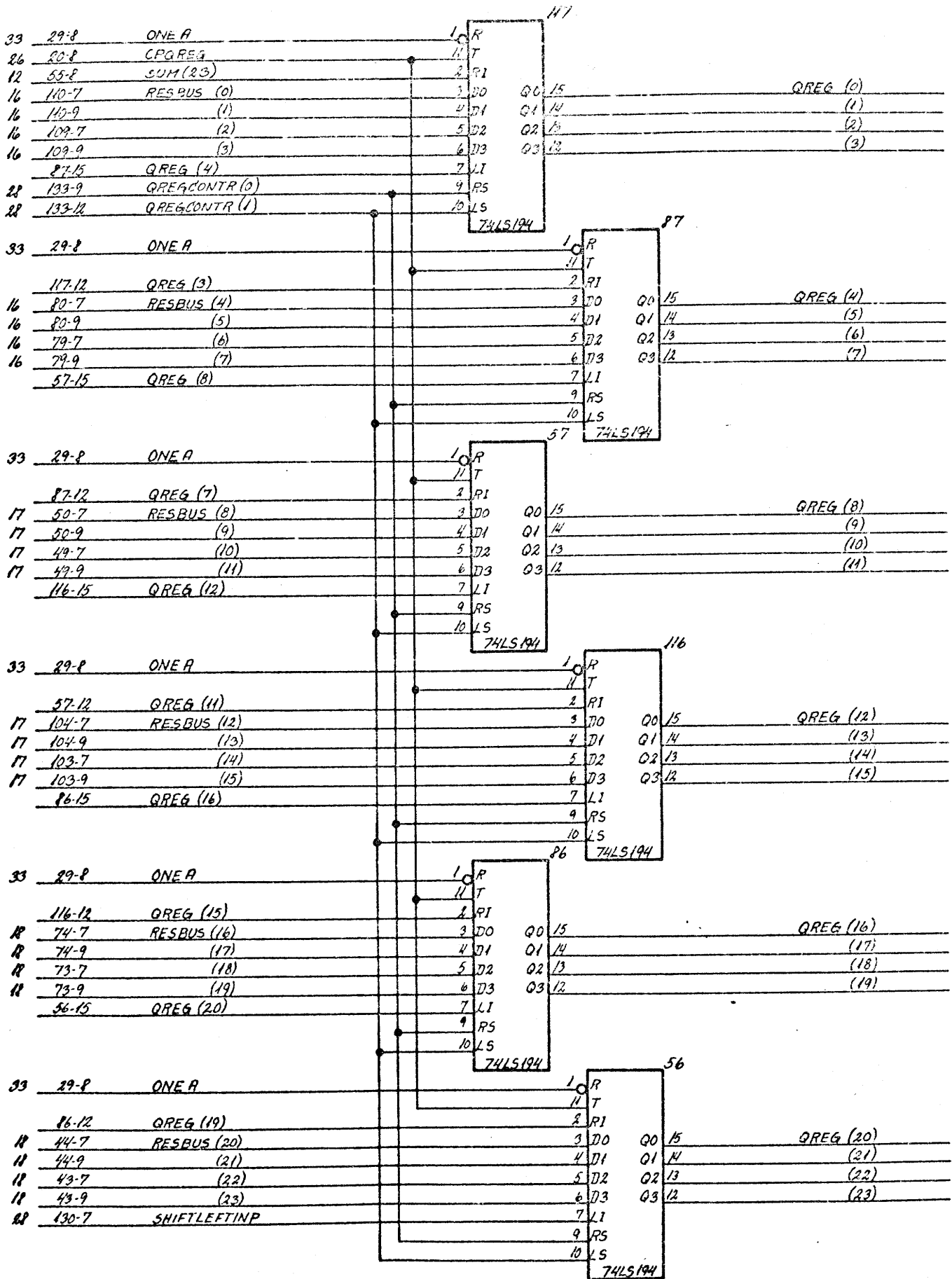
751091 AAJ 751106 ADB



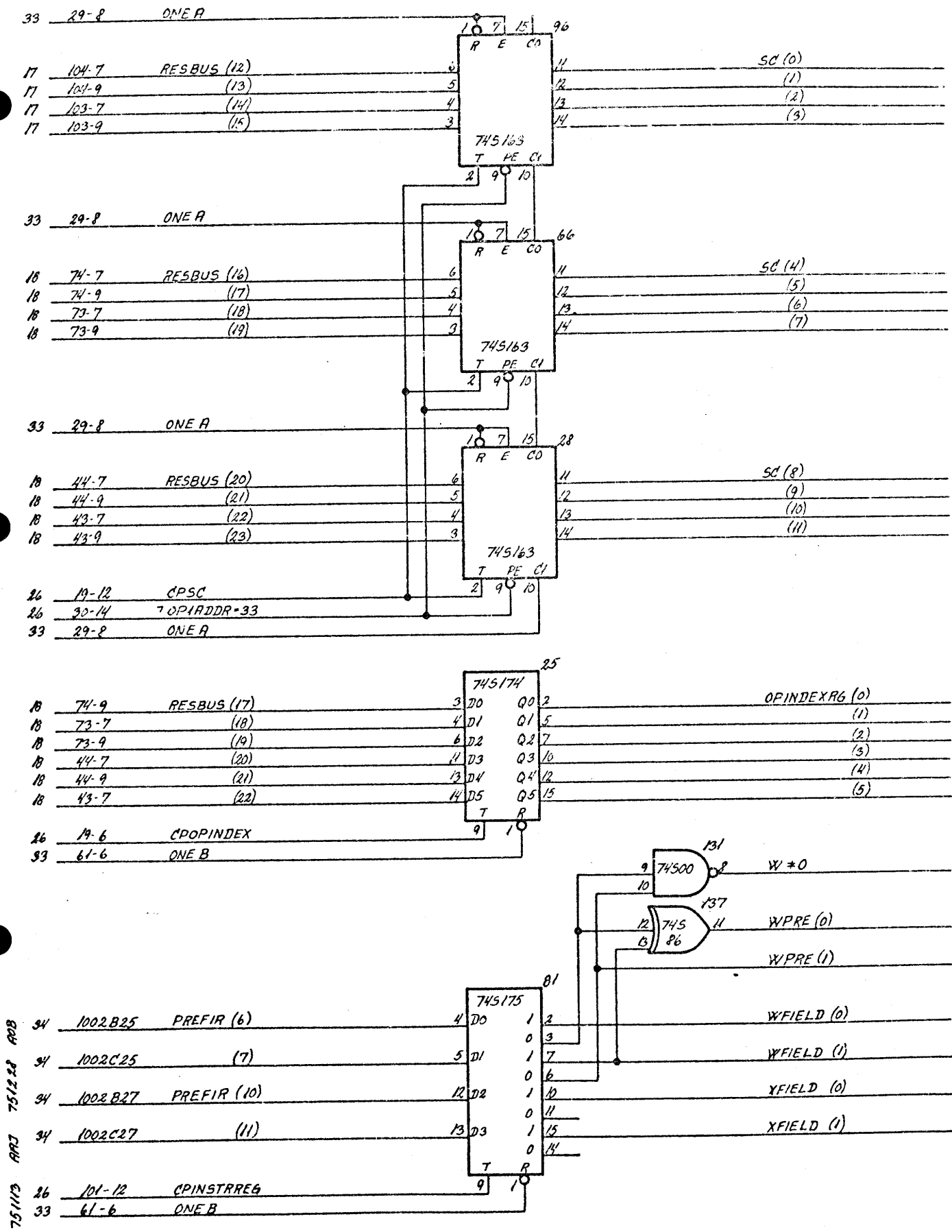
751031 ARJ 75106 AOB

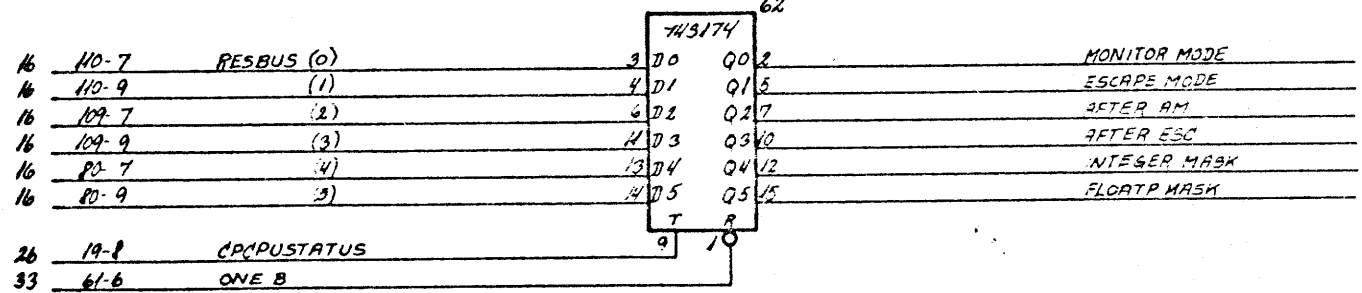
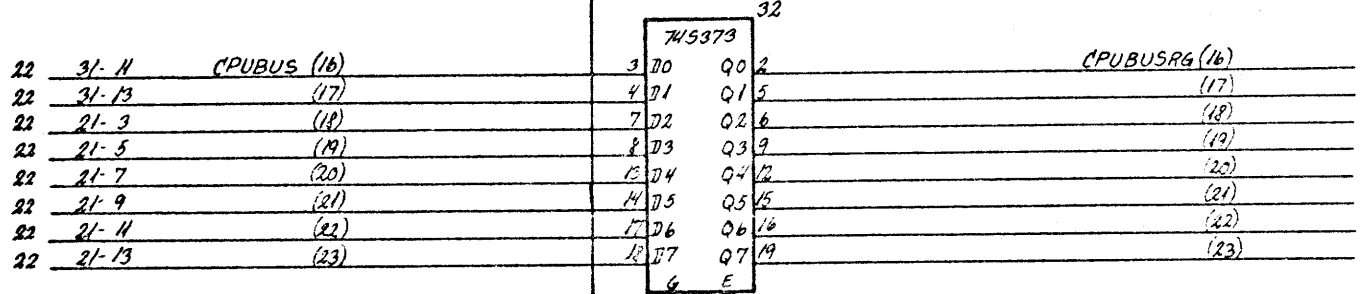
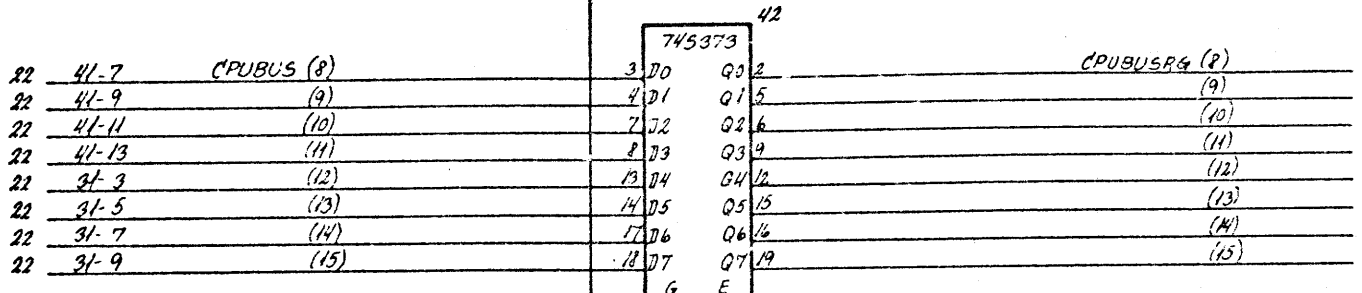
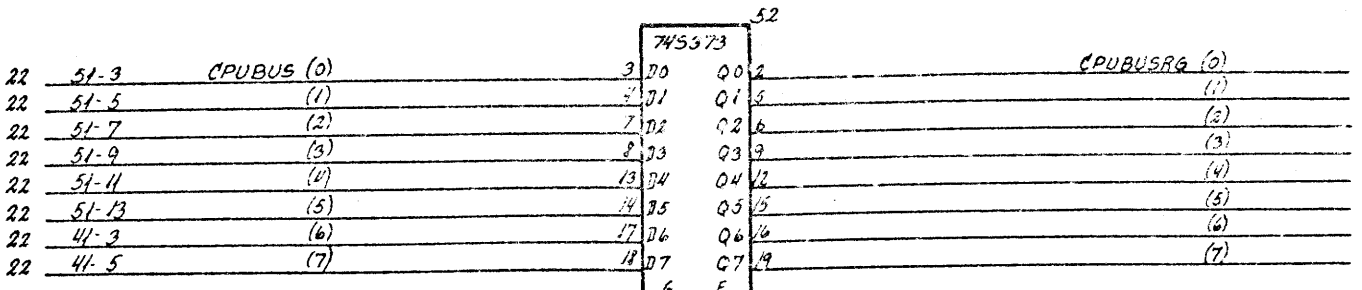
CPU802
R11420

SUM SHIFTER
AND MULTIPLEXERS FOR RESULT BUS (16-29)

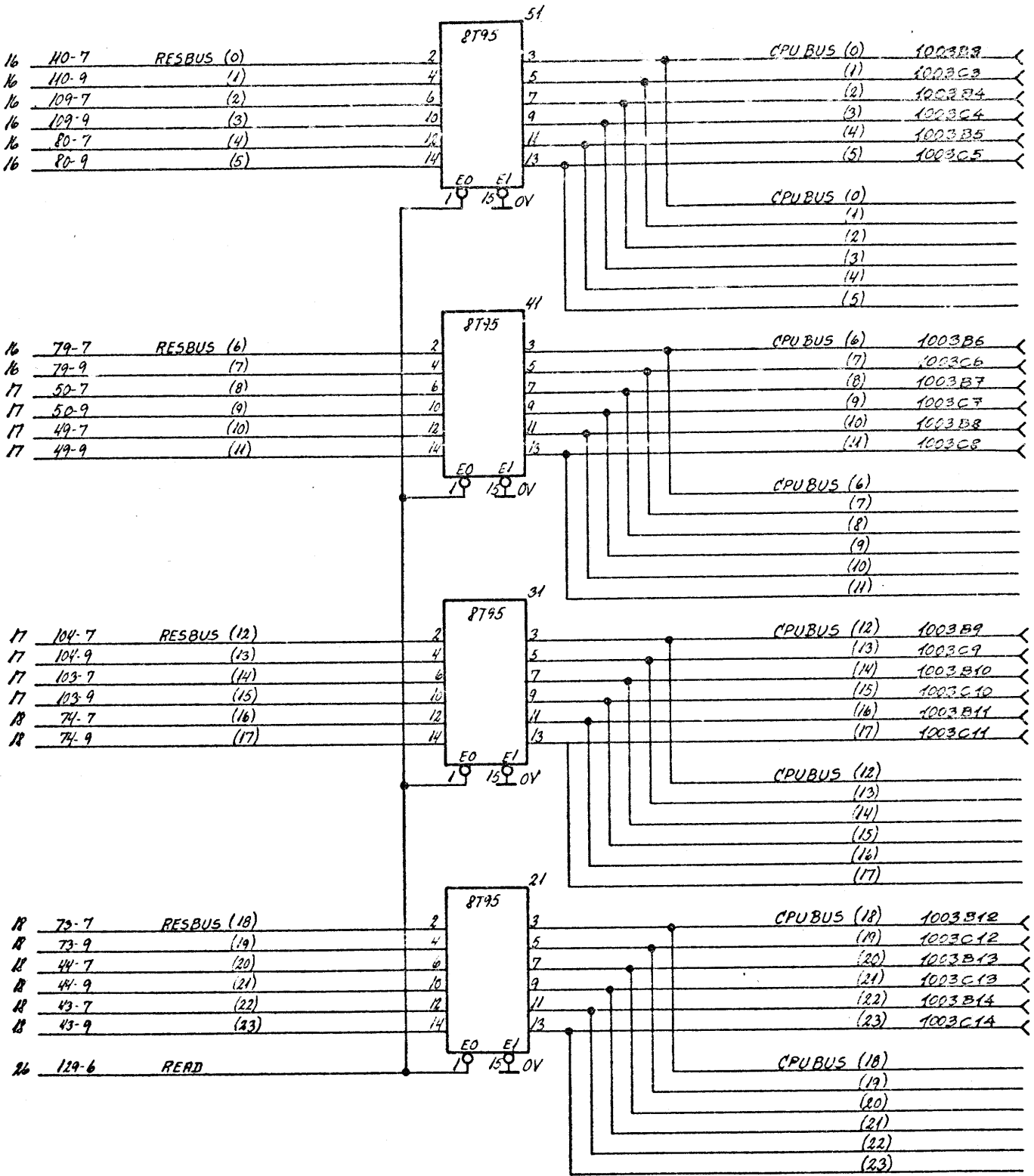


751030 RFD 751104 AOB

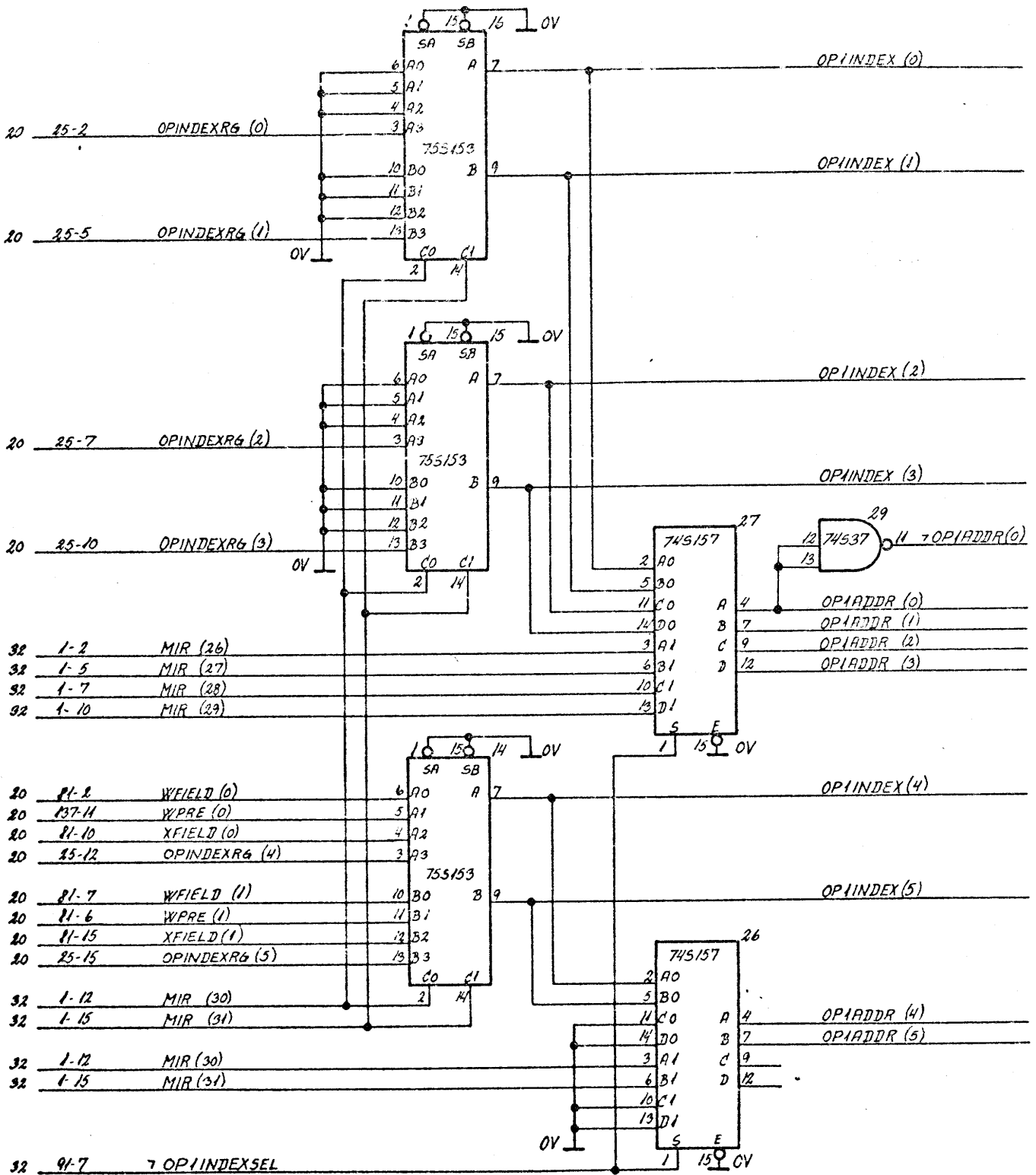




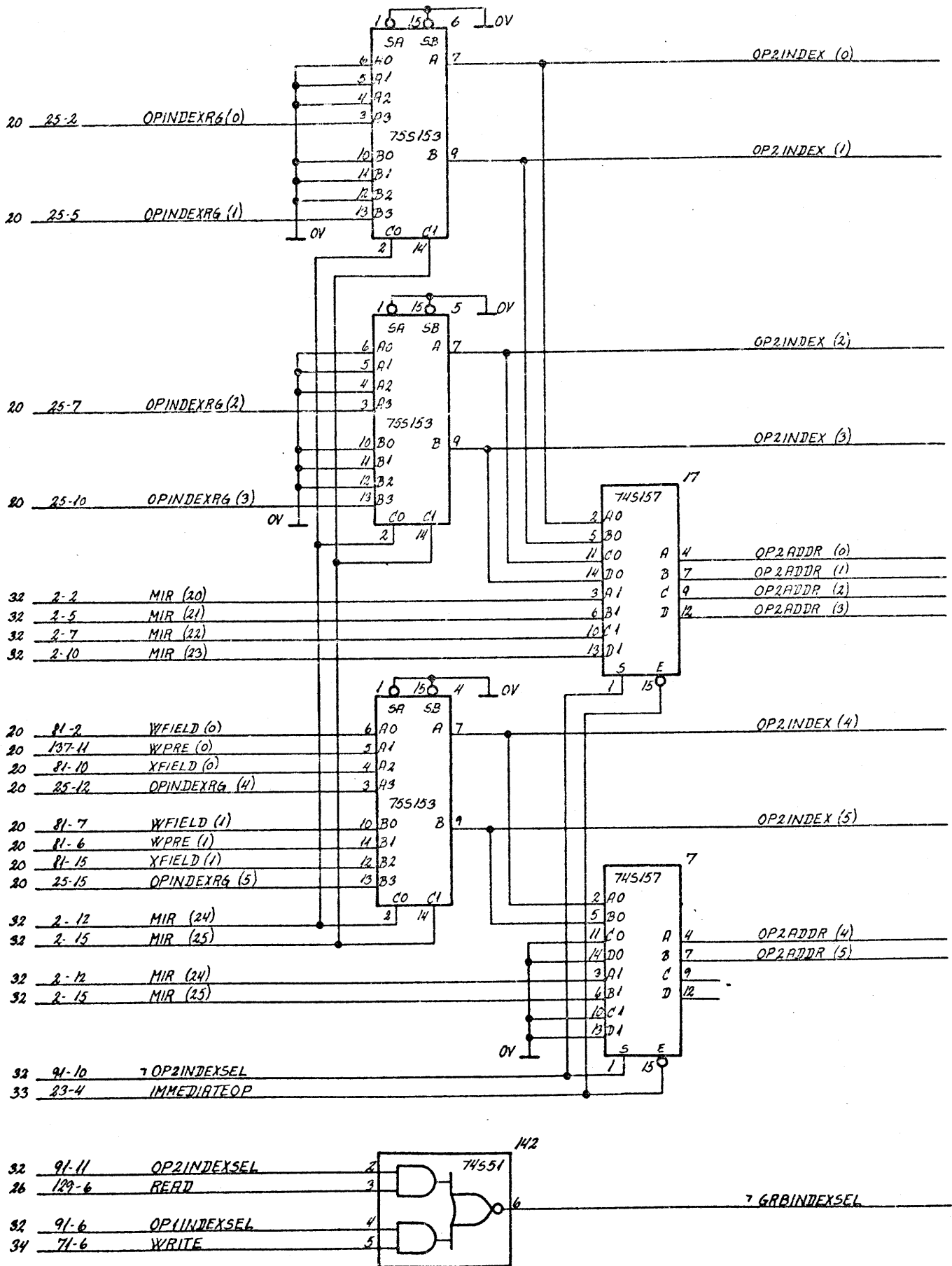
78118 AM3 75 AL31 A03



7541751 SW 4/1954

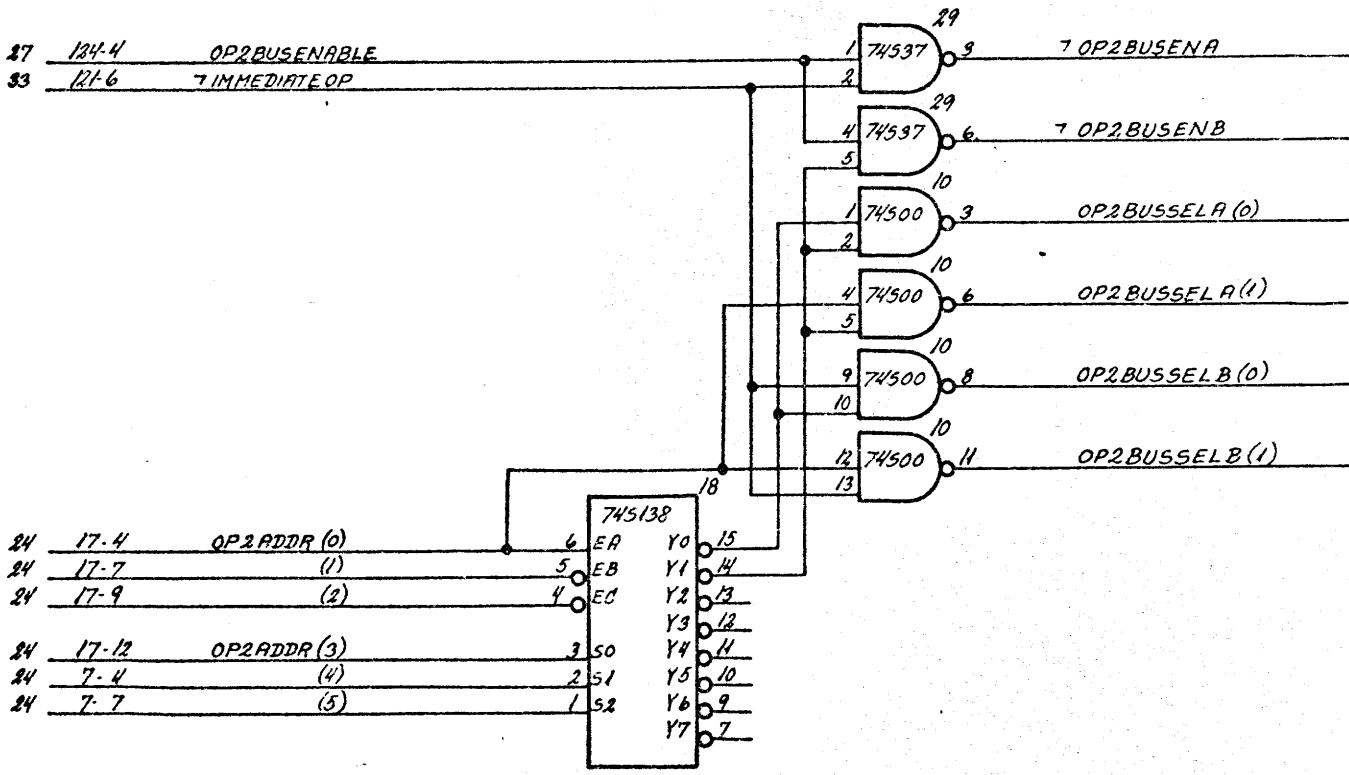
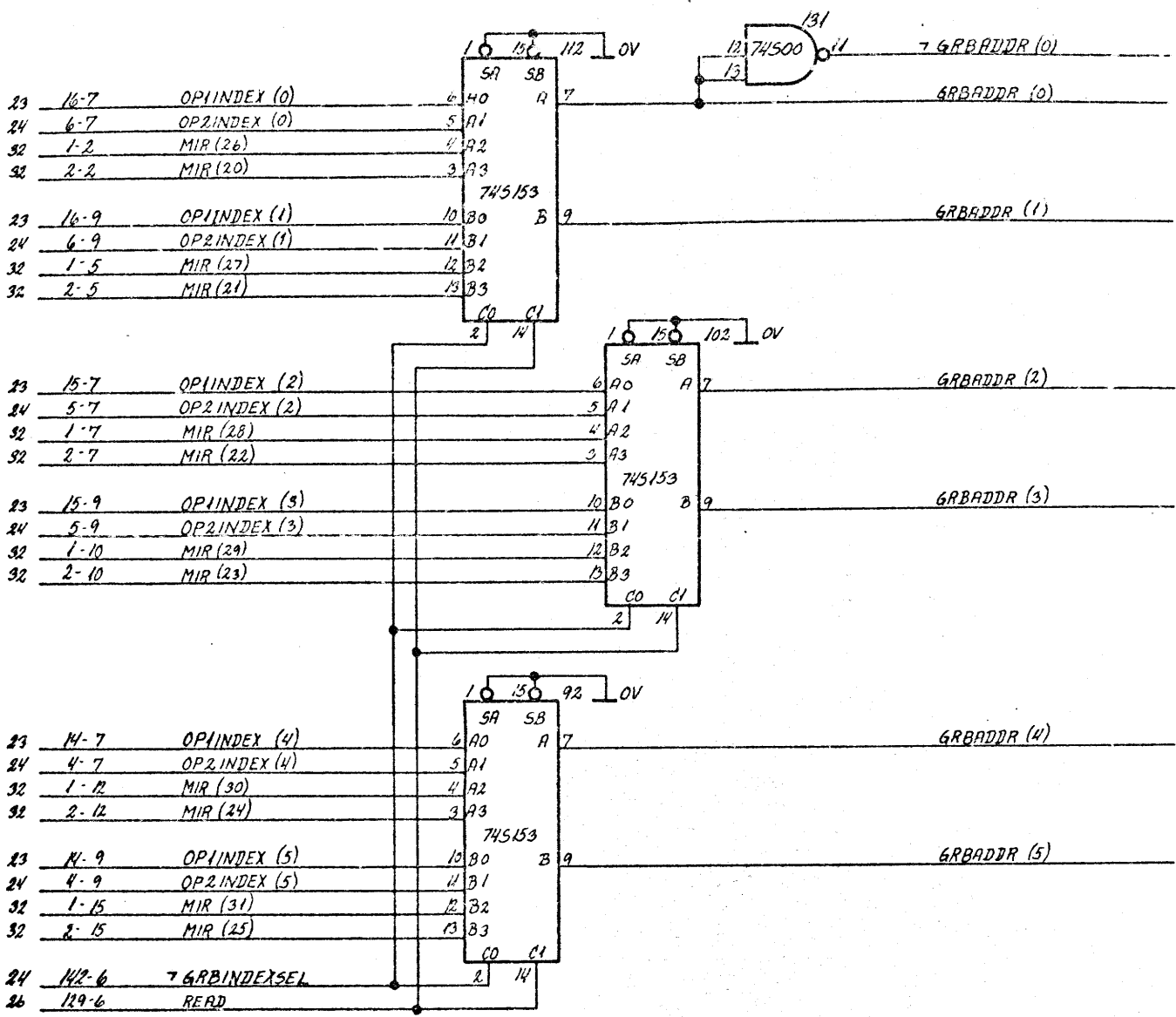


751106 ARR 751110 ROB

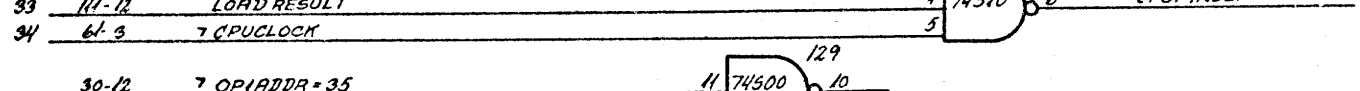
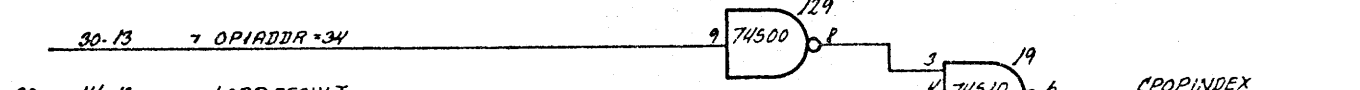
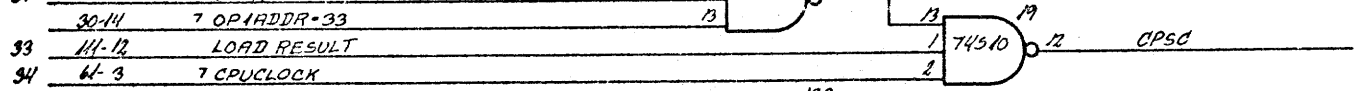
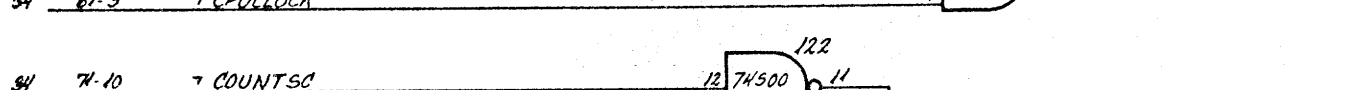
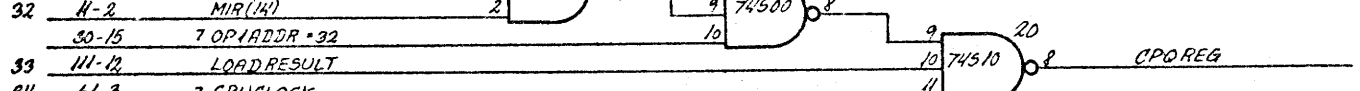
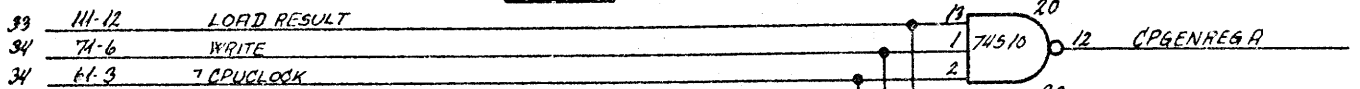
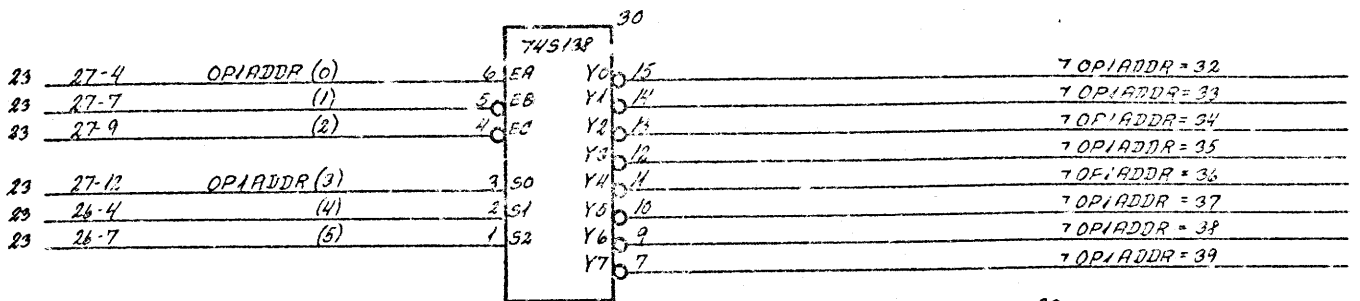


75110 ADB

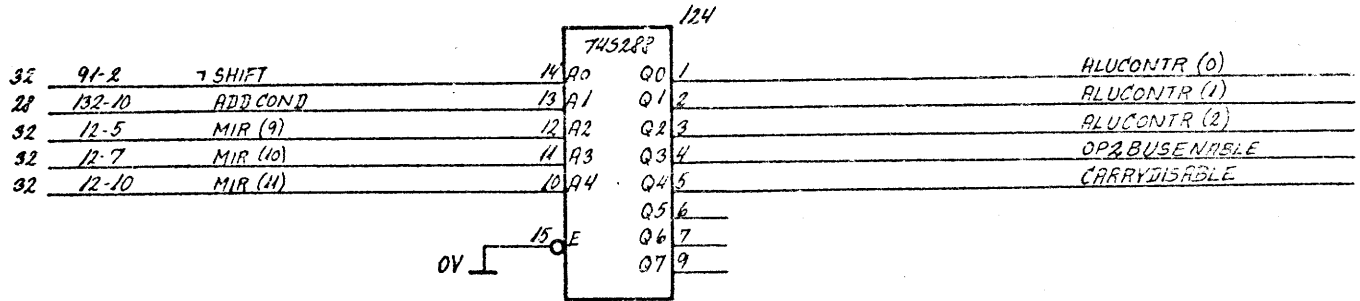
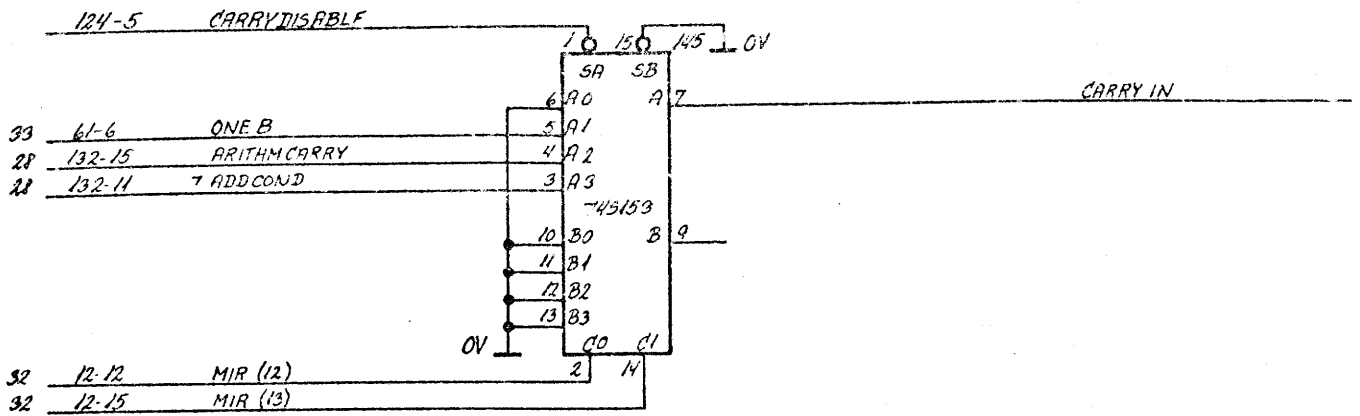
751106 AAD



TS1410 ASD
TS14107 ASD

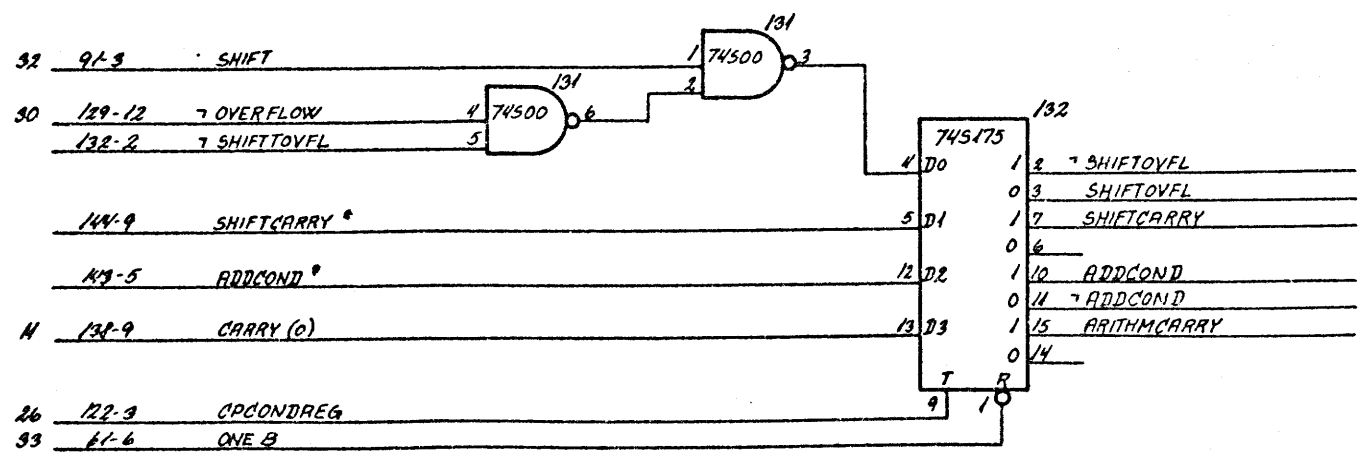
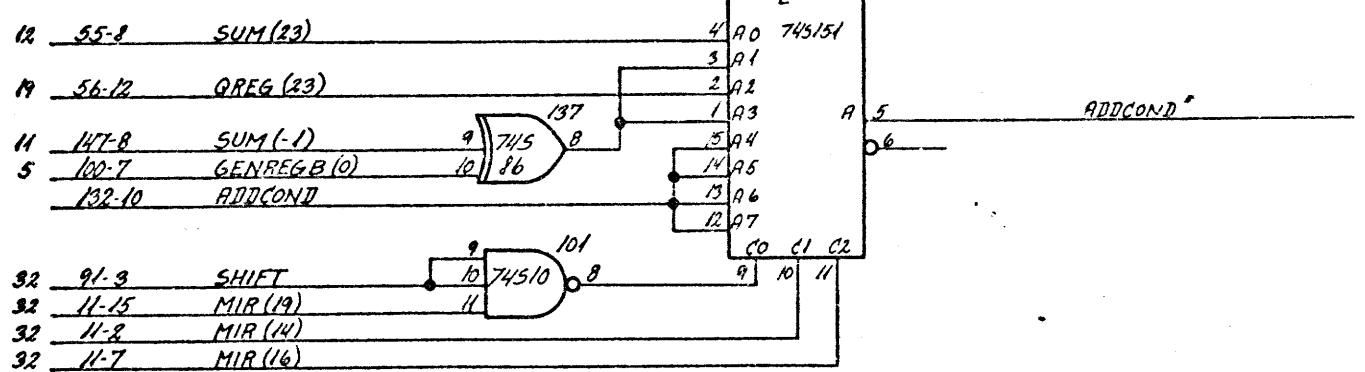
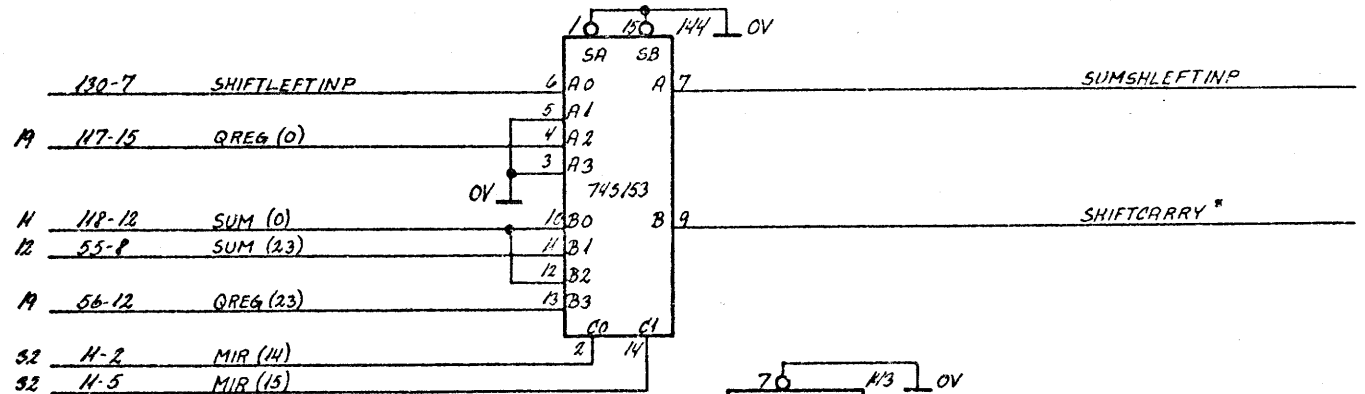
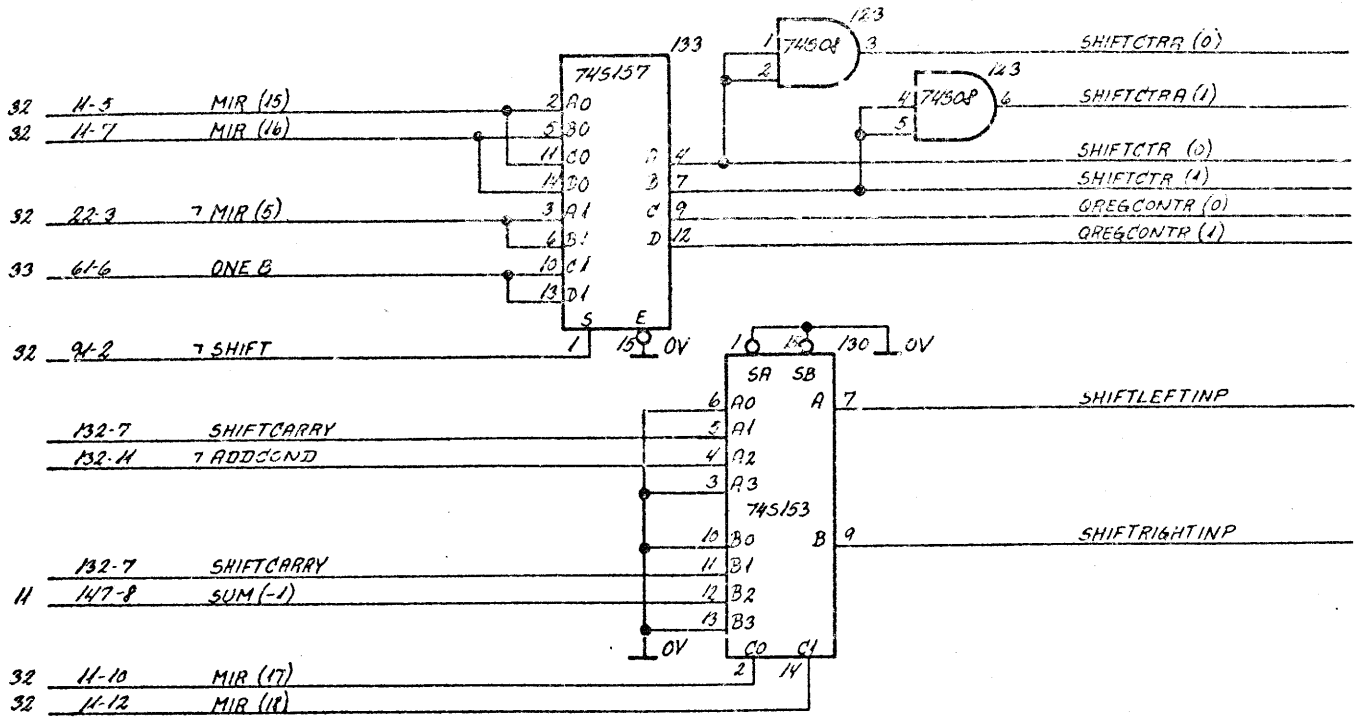


75114 AM3 760102 A05

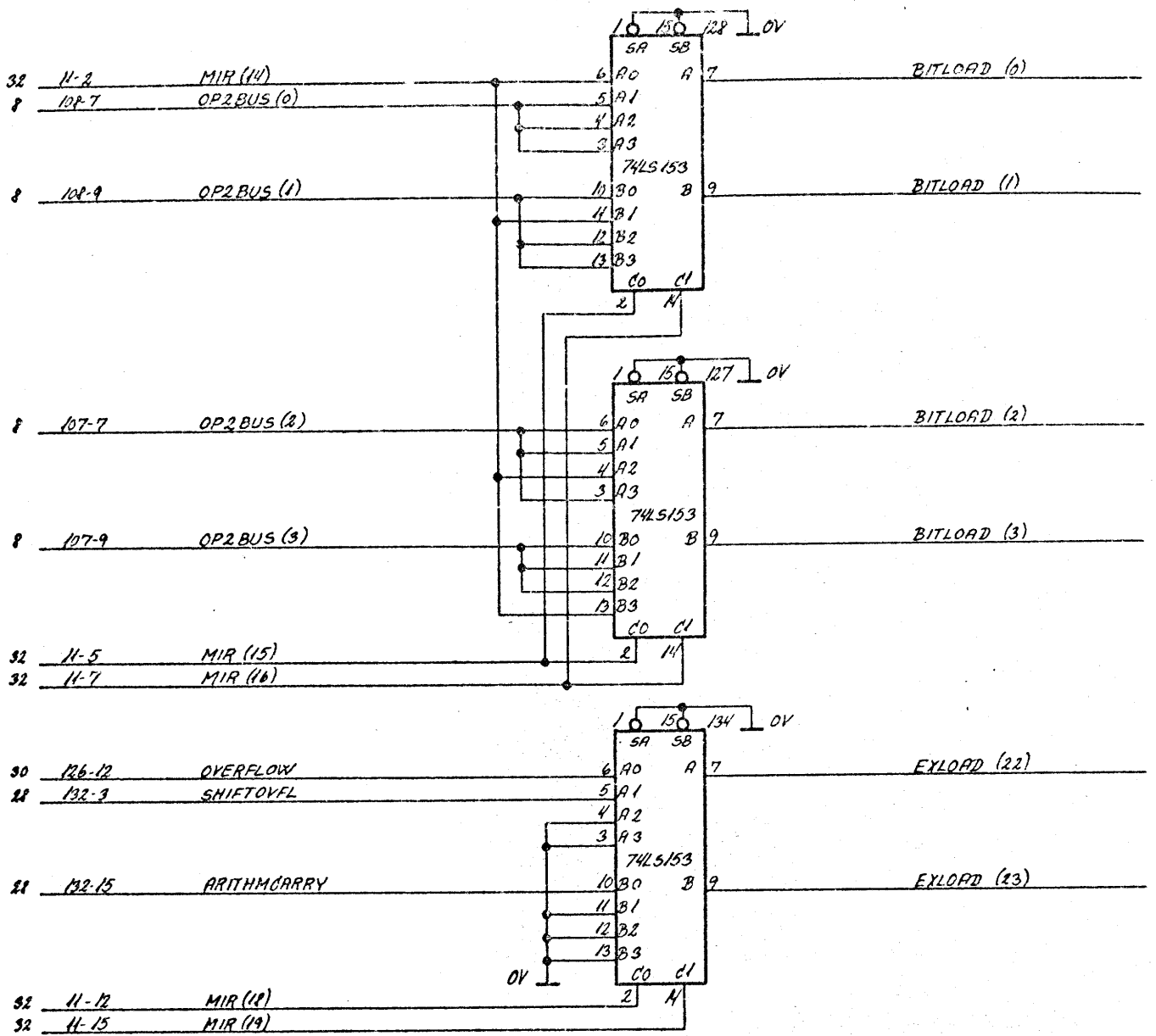


PROM ADDRESS			PROM OUTPUT		ALU OUTPUT
OCTAL	7 SHIFT ADD COND	MIR (9) MIR (10) MIR (11)	ALU CONTR (0) ALU CONTR (1) ALU CONTR (2)	OP2 BUSENABLE CARRYDISBLE	
0	00	000	110	00	OP1 + 0 + C
1	00	001	110	01	OP1 + 0
2	00	010	010	10	OP1 + 7OP2 + C
3	00	011	000	00	0
4	00	100	000	00	0
5	00	101	000	00	0
6	00	110	000	00	0
7	00	111	000	00	0
10	01	000	110	00	OP1 + 0 + C
11	01	001	110	10	OP1 + OP2 + C
12	01	010	110	10	OP1 + OP2 + C
13	01	011	000	00	0
14	01	100	000	00	0
15	01	101	000	00	0
16	01	110	000	00	0
17	01	111	000	00	0
20	10	000	000	10	0
21	10	001	100	10	7OP1 + OP2 + C
22	10	010	010	10	OP1 + 7OP2 + C
23	10	011	110	10	OP1 + OP2 + C
24	10	100	001	10	OP1 exor OP2
25	10	101	101	10	OP1 or OP2
26	10	110	011	10	OP1 and OP2
27	10	111	111	10	-1
30	11	000	000	10	0
31	11	001	100	10	7OP1 + OP2 + C
32	11	010	010	10	OP1 + 7OP2 + C
33	11	011	110	10	OP1 + OP2 + C
34	11	100	001	10	OP1 exor OP2
35	11	101	101	10	OP1 or OP2
36	11	110	011	10	OP1 and OP2
37	11	111	111	10	-1

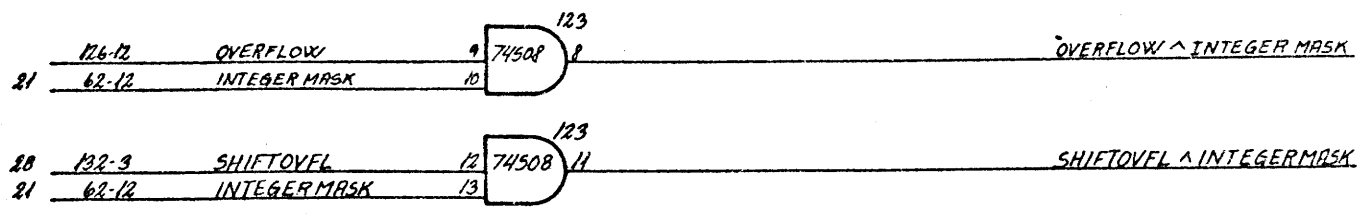
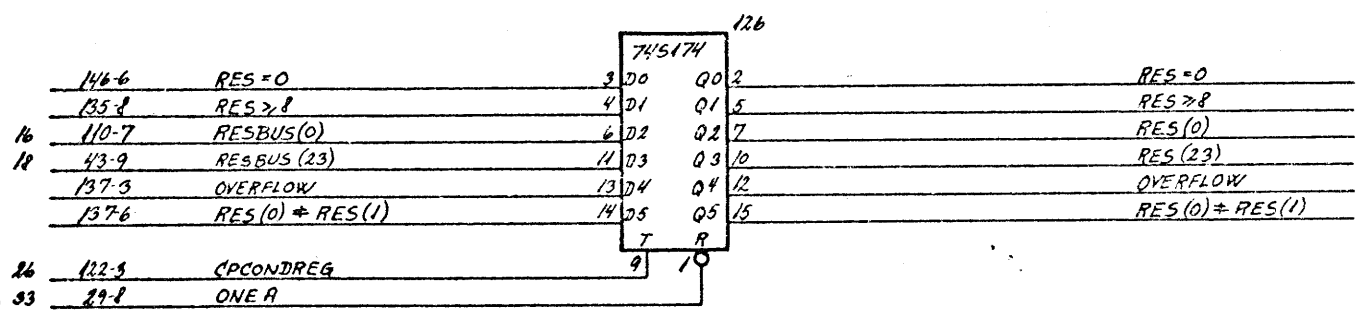
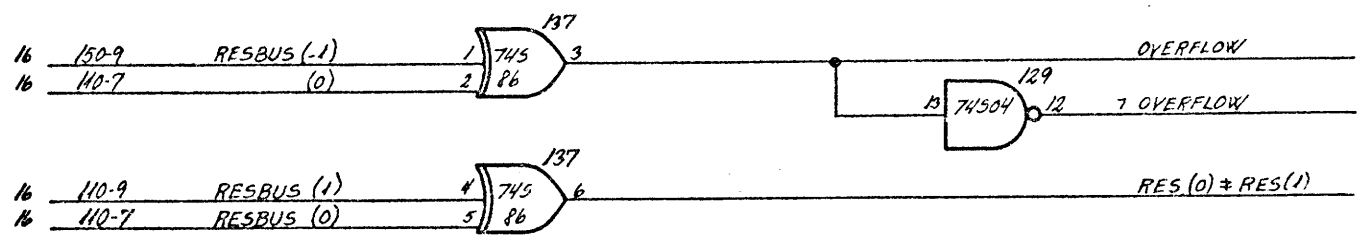
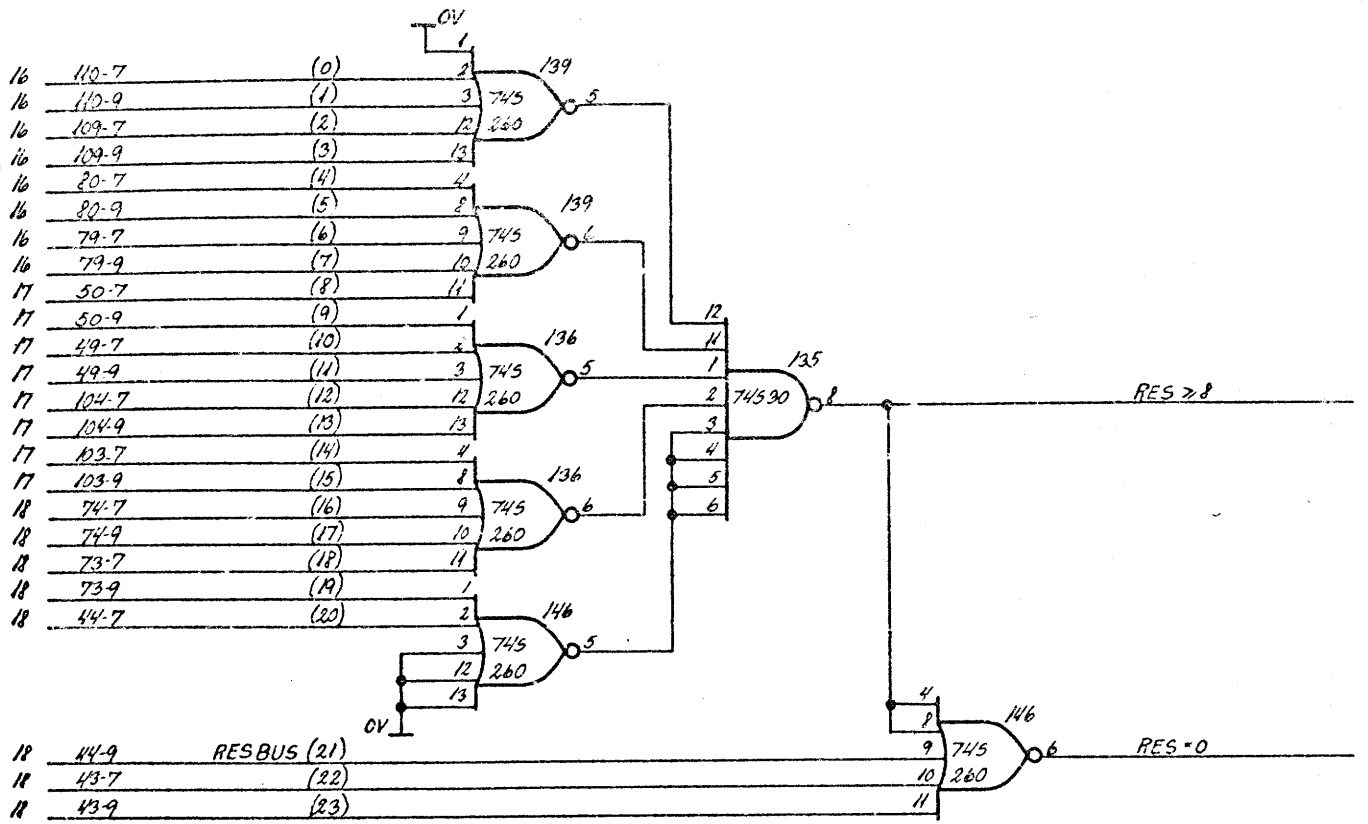
745153 AND 745222



75112 A08
75111 A07

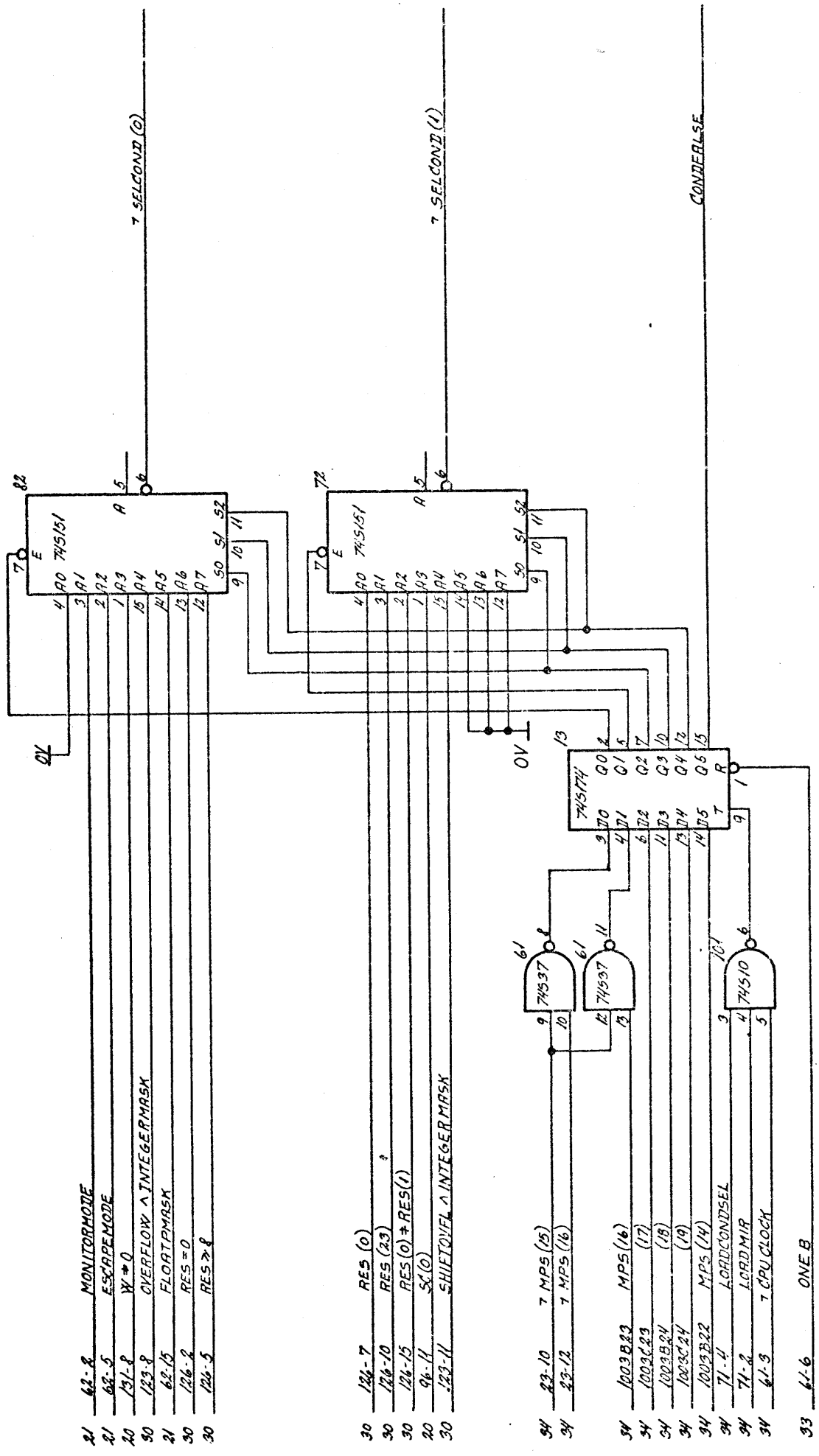


751119 RAO 760102 RAO

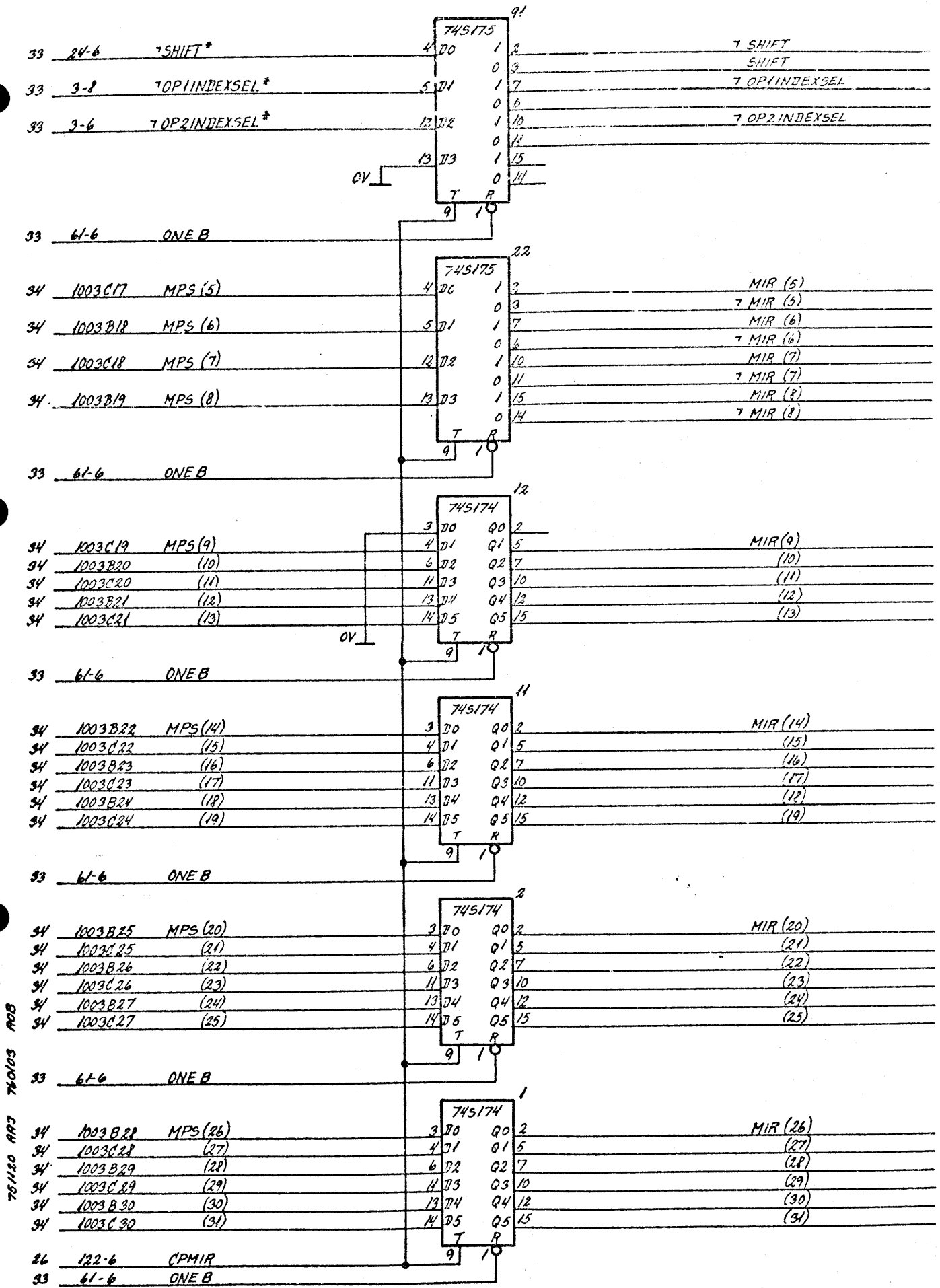


751120 A97 780102 A05

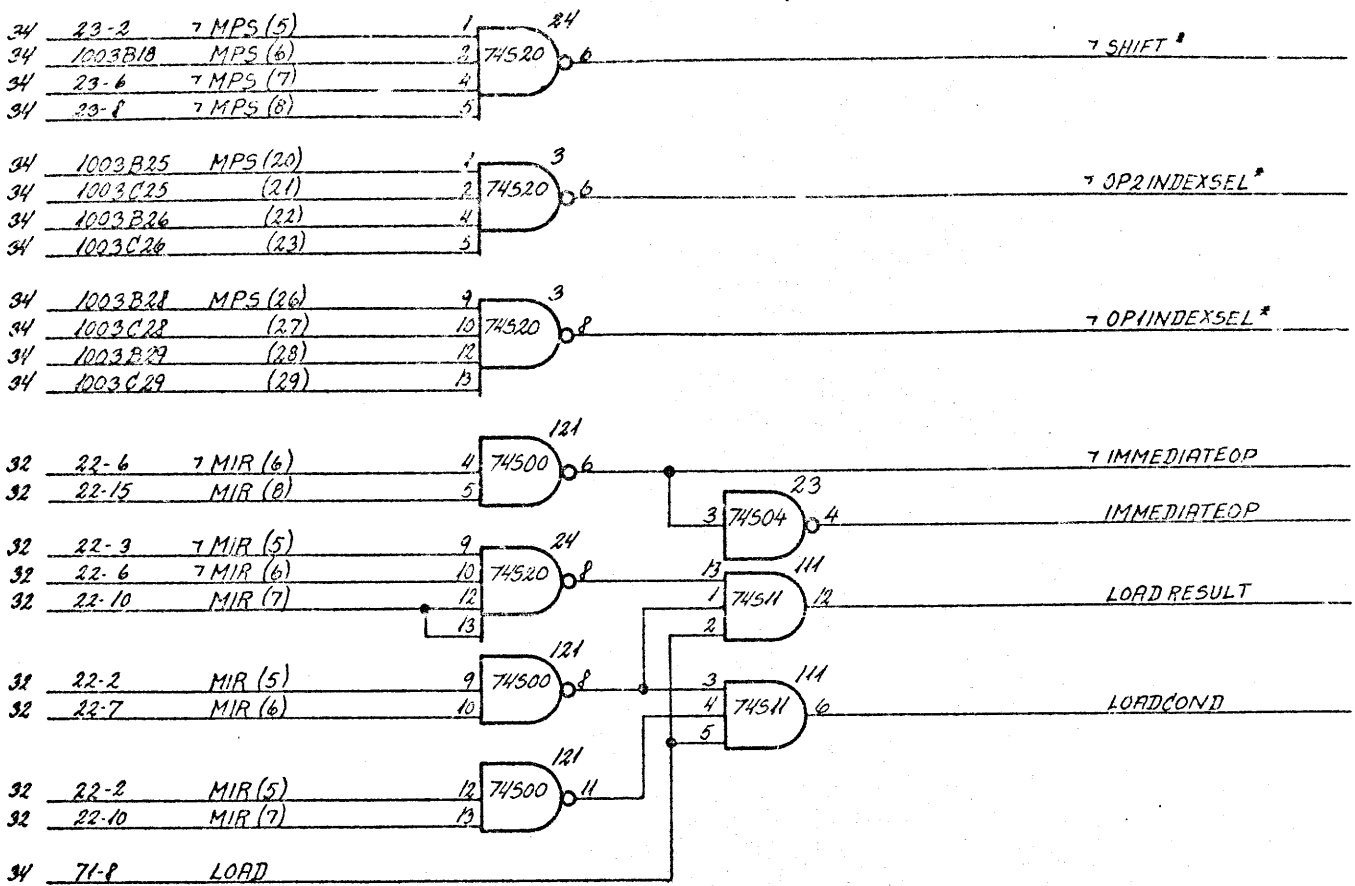
CPU002
R11433



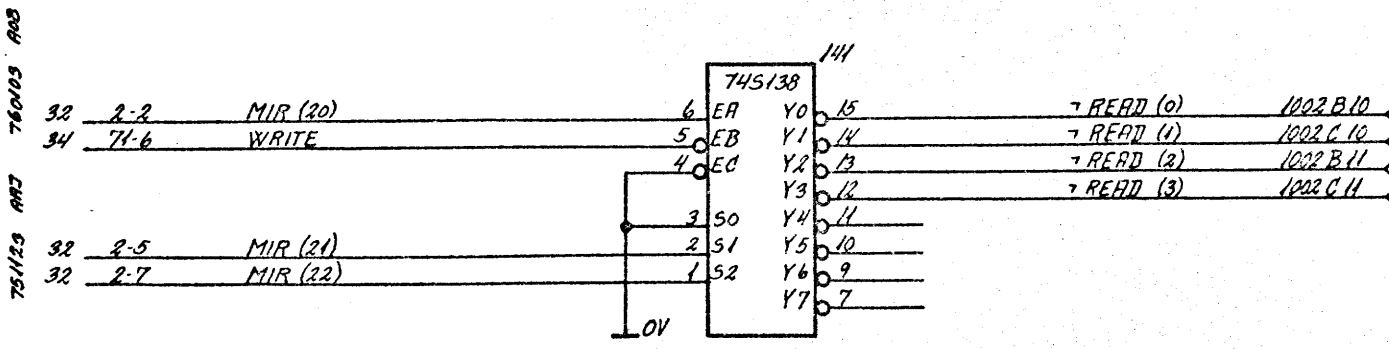
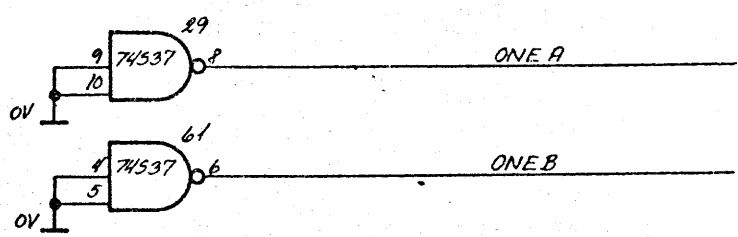
CONDITION SELECTOR

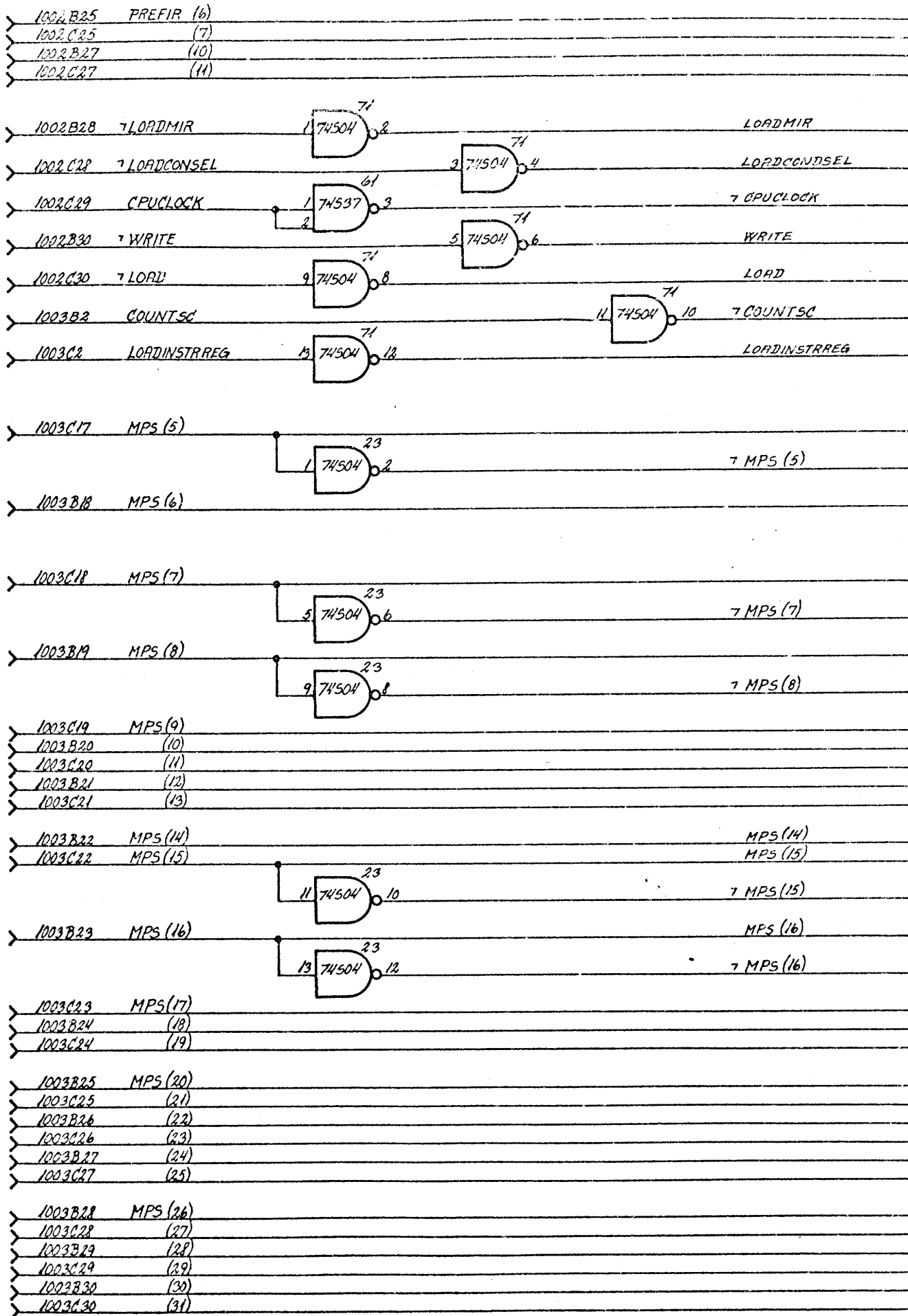


78120 MR3 780103 MR3



31	22-6	7 SELCOND (0)	1002 B 15
31	72-6	7 SELCOND (1)	1002 C 15
31	13-15	CONFALSE	1002 C 19
21	62-2	MONITORMODE	1002 B 20
21	62-5	ESCAPEMODE	1002 C 20
21	62-7	AFTER RM	1002 B 21
21	62-10	AFTER ESC	1002 C 21



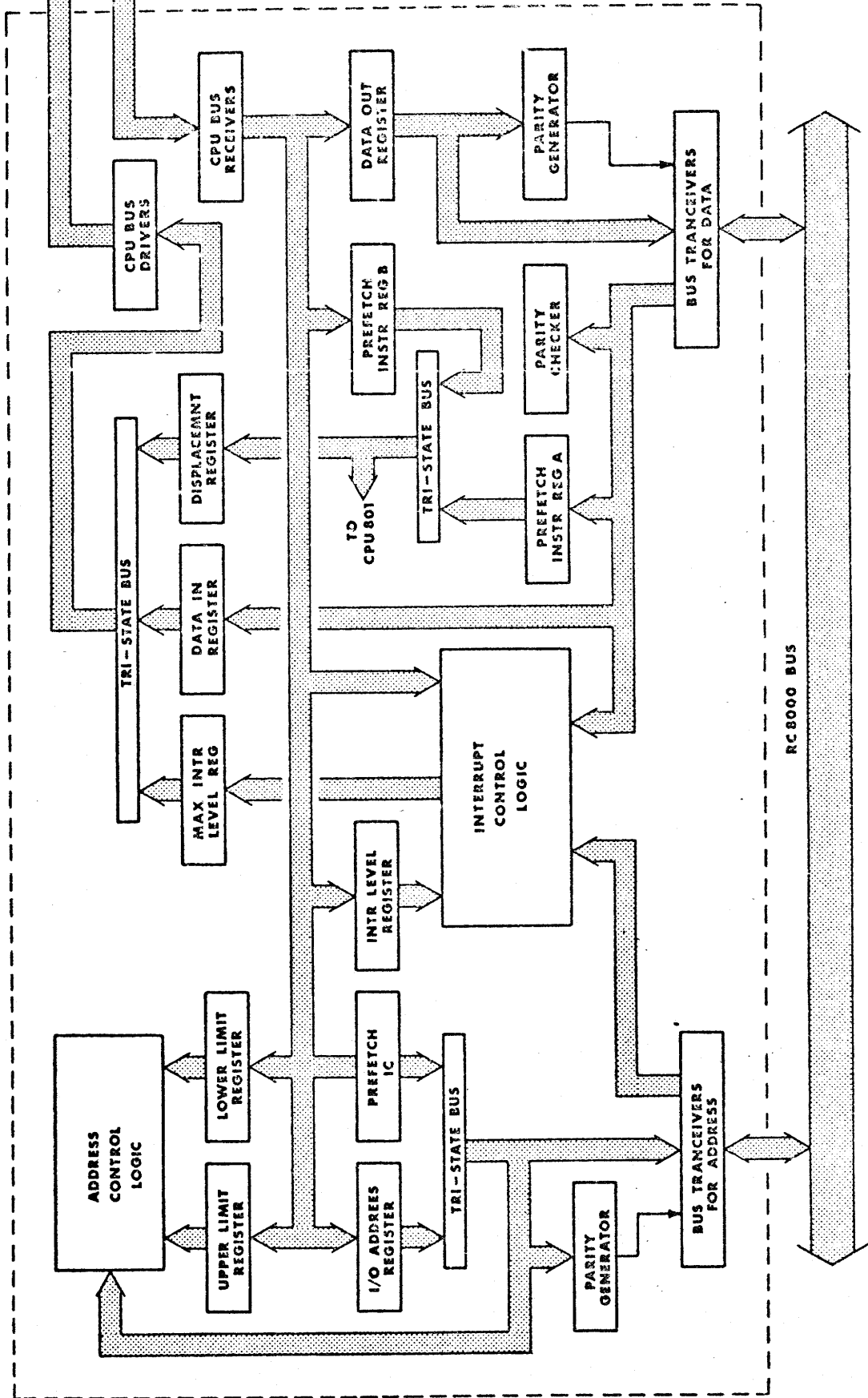


75121 ARJ 76005 AOB

A/S REC	Designed by	76110 AAJ	Drawn by	76110 AOB	Dwg. Office	Design Check	Replaces Dwg. No.	due to ECN	Reply	Dwg. No.
	CENTRALEN									

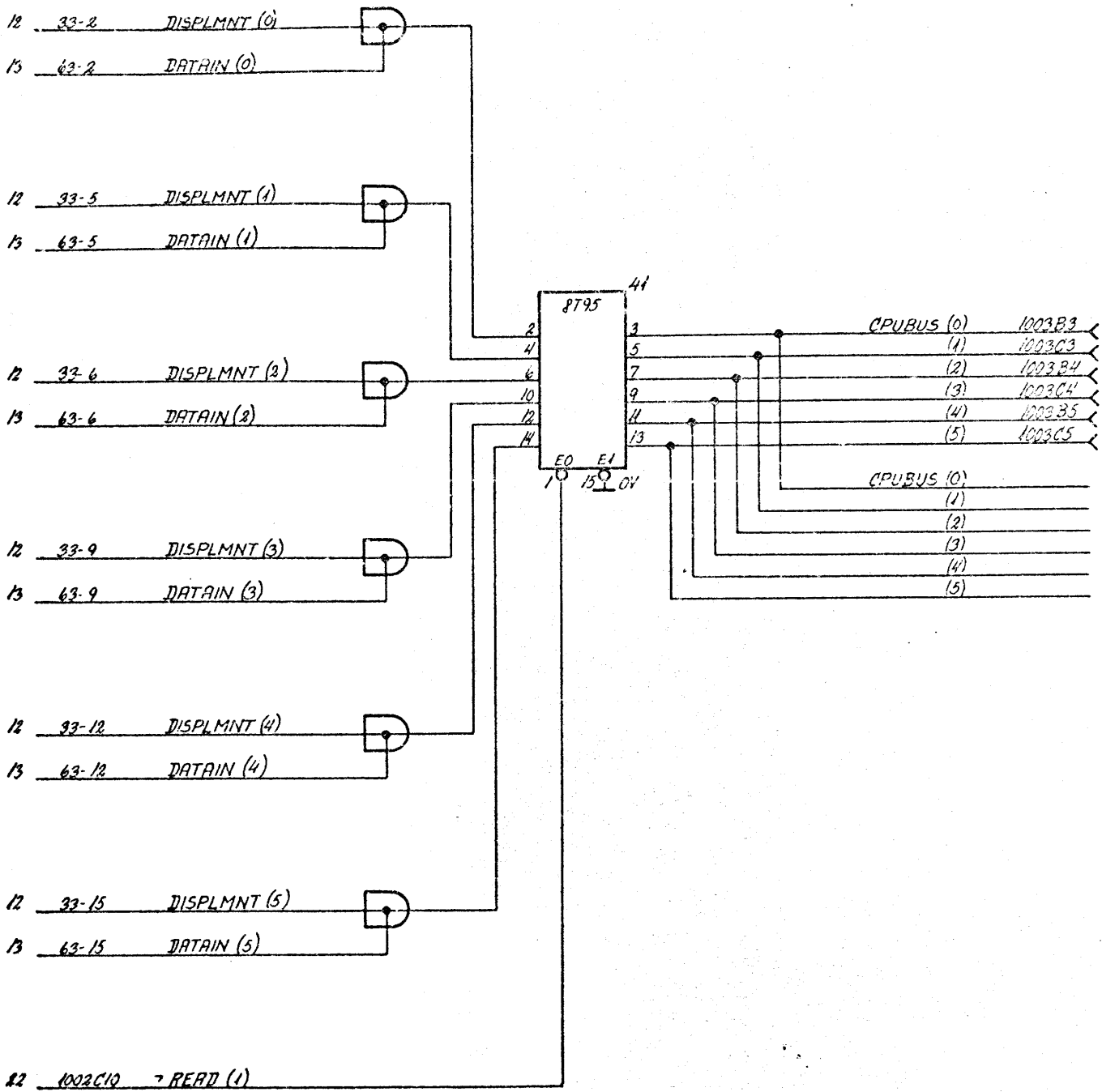
CPU BUS

CPU 803

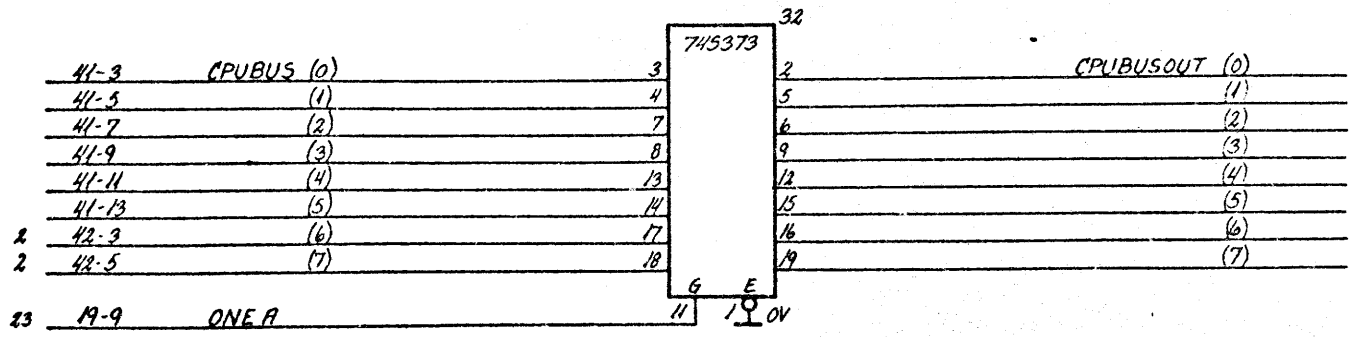


Unit
CPU 803
Dwg. No.
R11653

CPU 803 BLOCK DIAGRAM



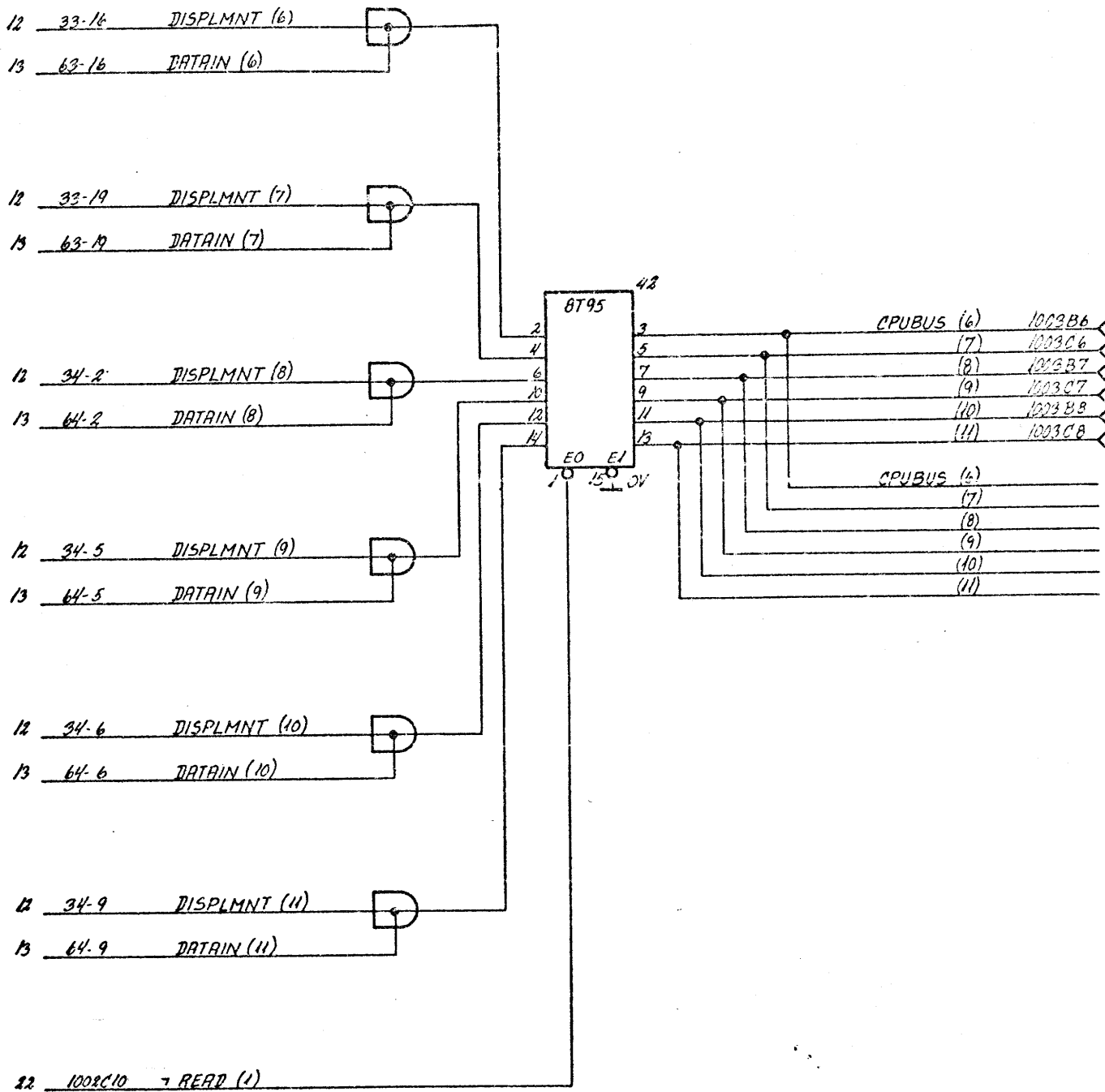
751210 ARZ 760305 AOB



CPU 803

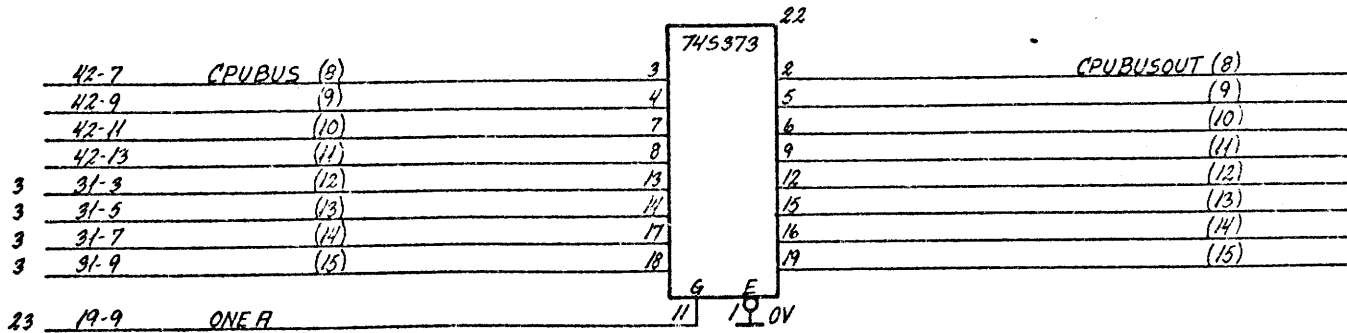
R11437

DRIVERS FOR CPUBUS (0-5)
AND RECEIVERS FOR CPUBUS (0-7)



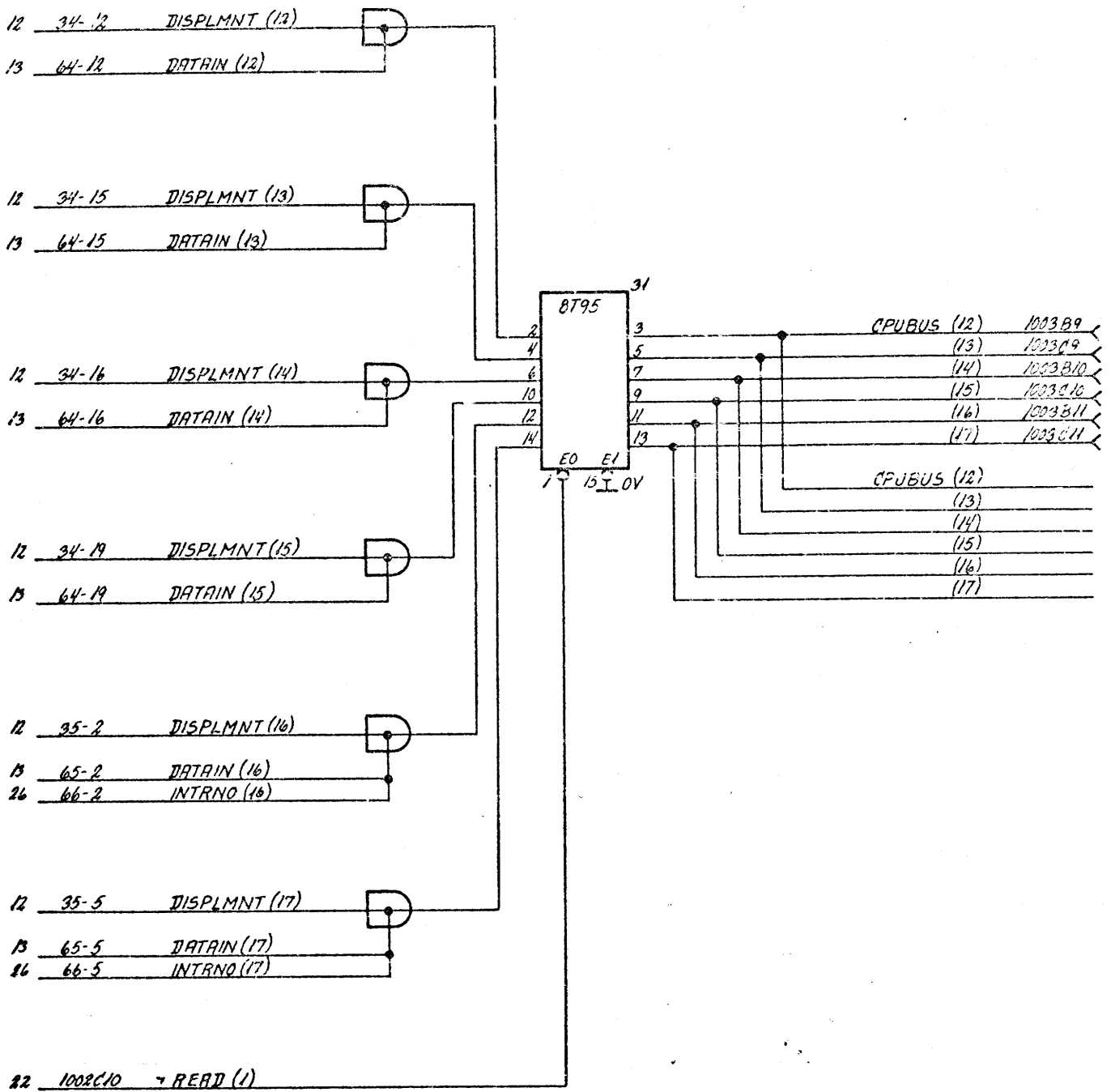
22 1003C10 → READ (1)

751210 RRJ 760305 ROB

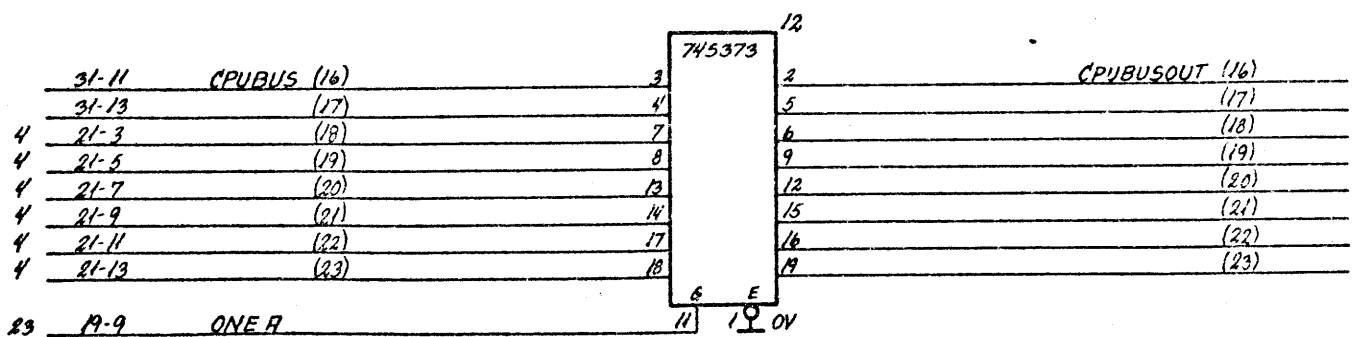


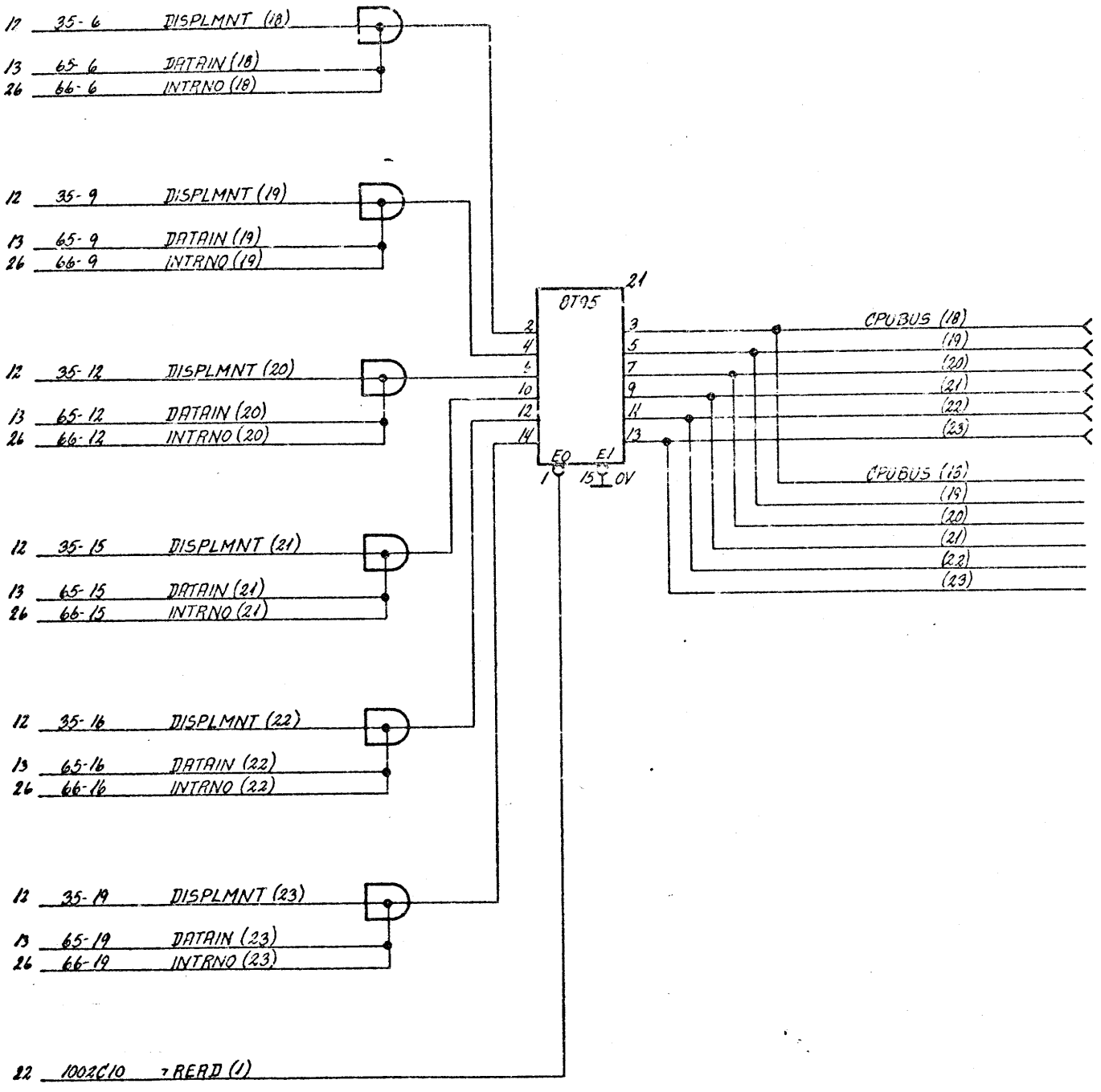
CPU 803
R4438

DRIVERS FOR CPUBUS (6:11)
AND RECEIVERS FOR CPUBUS (8:15)

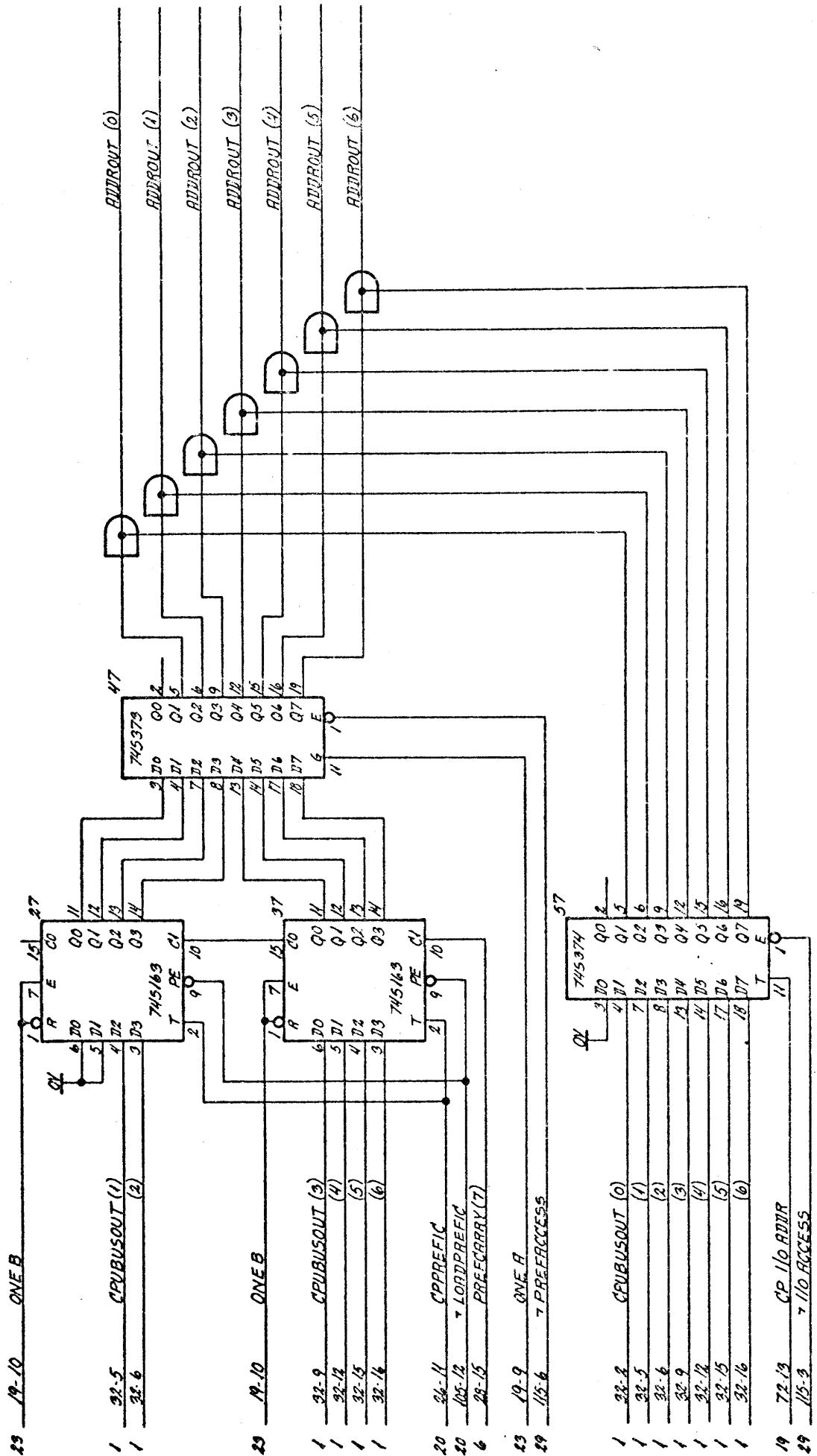


751810 REV 760305 A03





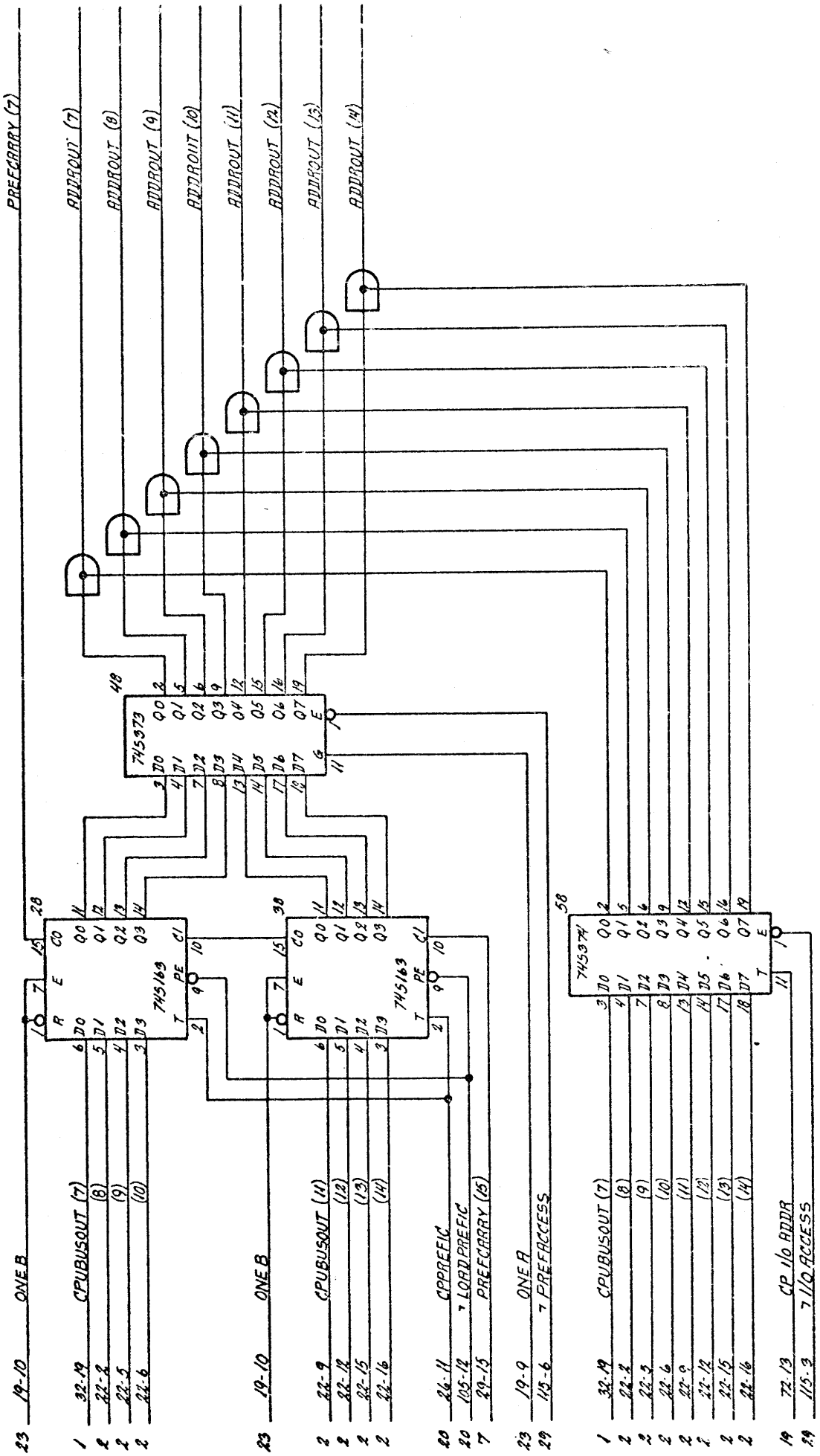
701210 RAF 760305 A0B



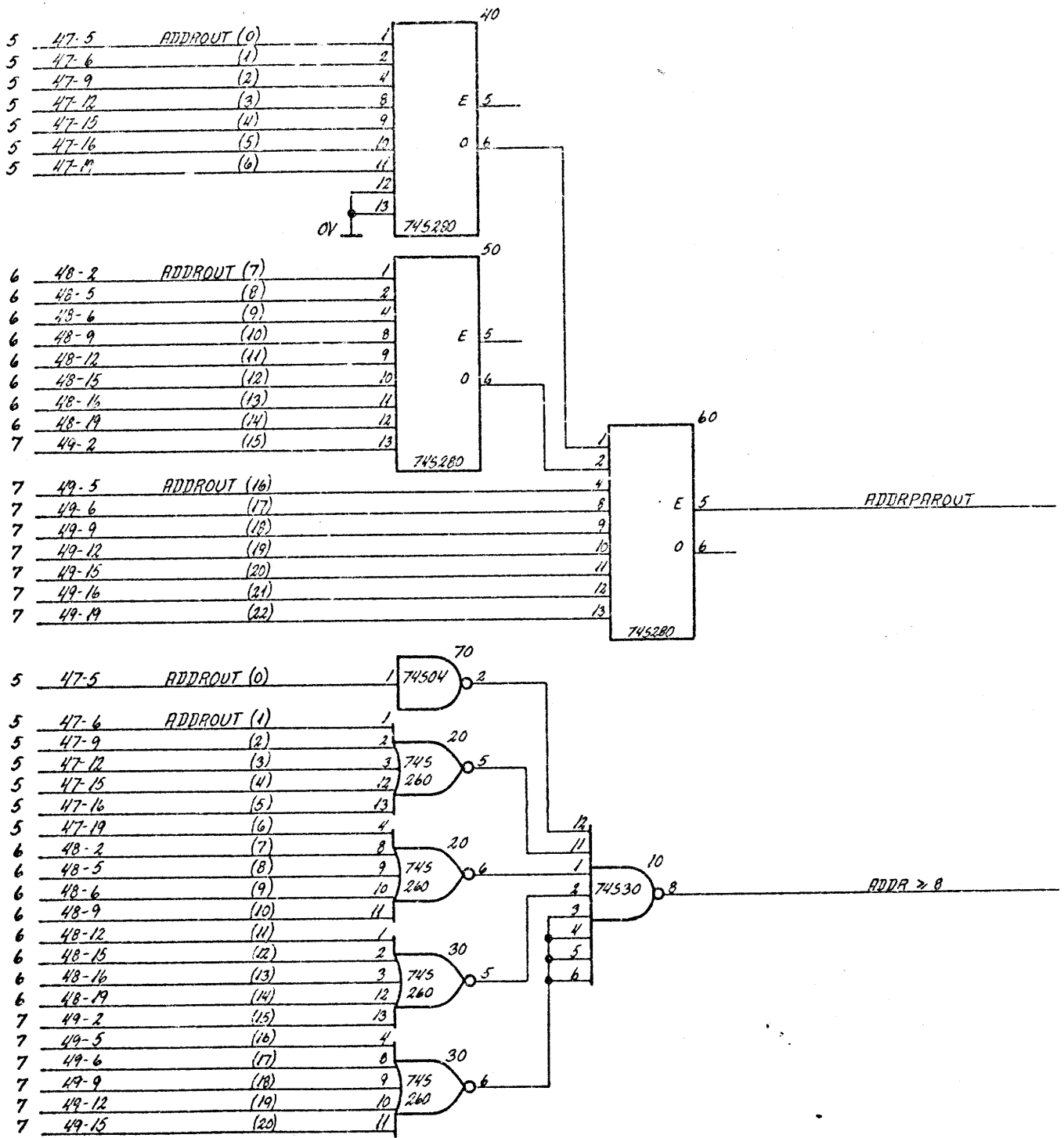
CPU 803
R11441

PREFETCH ADDRESS COUNTER
AND I/O ADDRESS REGISTER

CPU803
R 11442



PREFETCH ADDRESS COUNTER
AND I/O ADDRESS REGISTER



751211 RHJ 760901 RDB

760407 ARR 760407 ARR

67

		745374				
1	32-2	CPUBUSOUT (0)	3	D0	Q0 2	UPPERLIM (0)
1	32-5	(1)	4	D1	Q1 5	(1)
1	32-6	(2)	7	D2	Q2 6	(2)
1	32-9	(3)	8	D3	Q3 9	(3)
1	32-12	(4)	13	D4	Q4 12	(4)
1	32-15	(5)	14	D5	Q5 15	(5)
1	32-16	(6)	17	D6	Q6 16	(6)
1	32-19	(7)	18	D7	Q7 19	(7)
				T	E	
19	72-11	CPUPPERLIM	H	1	OV	

68

		745374				
2	22-2	CPUBUSOUT (8)	3	D0	Q0 2	UPPERLIM (8)
2	22-5	(9)	4	D1	Q1 5	(9)
2	22-6	(10)	7	D2	Q2 6	(10)
2	22-9	(11)	8	D3	Q3 9	(11)
2	22-12	(12)	13	D4	Q4 12	(12)
2	22-15	(13)	14	D5	Q5 15	(13)
2	22-16	(14)	17	D6	Q6 16	(14)
2	22-19	(15)	18	D7	Q7 19	(15)
				T	E	
19	72-11	CPUPPERLIM	H	1	OV	

69

		745374				
3	12-2	CPUBUSOUT (16)	3	D0	Q0 2	UPPERLIM (16)
3	12-5	(17)	4	D1	Q1 5	(17)
3	12-6	(18)	7	D2	Q2 6	(18)
3	12-9	(19)	8	D3	Q3 9	(19)
3	12-12	(20)	13	D4	Q4 12	(20)
3	12-15	(21)	14	D5	Q5 15	(21)
3	12-16	(22)	17	D6	Q6 16	(22)
3	12-19	(23)	18	D7	Q7 19	(23)
				T	E	
19	72-11	CPUPPERLIM	H	1	OV	

77

		745374				
1	32-2	CPUBUSOUT (0)	3	D0	Q0 2	LOWERLIM (0)
1	32-5	(1)	4	D1	Q1 5	(1)
1	32-6	(2)	7	D2	Q2 6	(2)
1	32-9	(3)	8	D3	Q3 9	(3)
1	32-12	(4)	13	D4	Q4 12	(4)
1	32-15	(5)	14	D5	Q5 15	(5)
1	32-16	(6)	17	D6	Q6 16	(6)
1	32-19	(7)	18	D7	Q7 19	(7)
				T	E	
19	72-10	CPLOWERLIM	H	1	OV	

78

		745374				
2	22-2	CPUBUSOUT (8)	3	D0	Q0 2	LOWERLIM (8)
2	22-5	(9)	4	D1	Q1 5	(9)
2	22-6	(10)	7	D2	Q2 6	(10)
2	22-9	(11)	8	D3	Q3 9	(11)
2	22-12	(12)	13	D4	Q4 12	(12)
2	22-15	(13)	14	D5	Q5 15	(13)
2	22-16	(14)	17	D6	Q6 16	(14)
2	22-19	(15)	18	D7	Q7 19	(15)
				T	E	
19	72-10	CPLOWERLIM	H	1	OV	

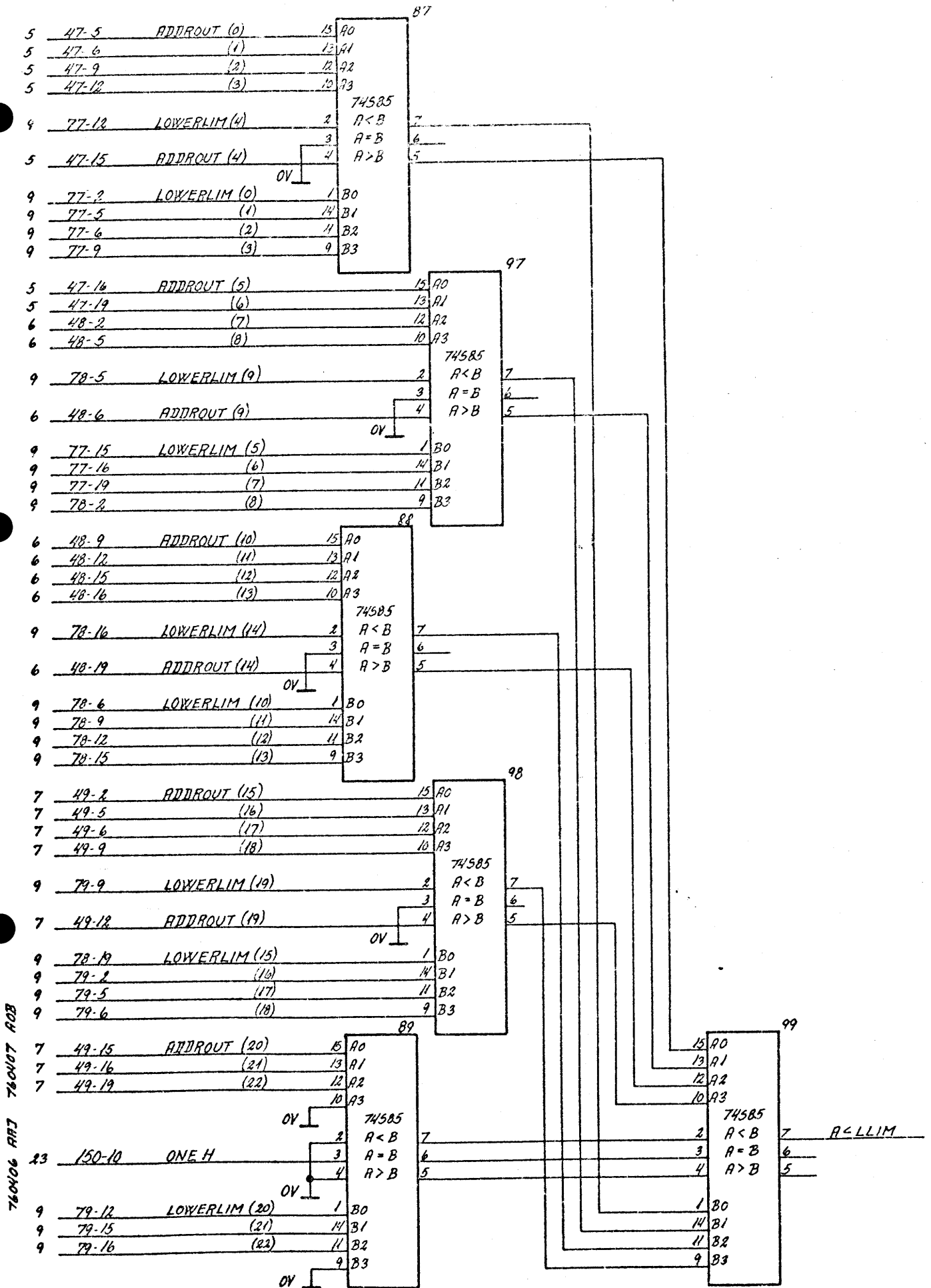
79

		745374				
3	12-2	CPUBUSOUT (16)	3	D0	Q0 2	LOWERLIM (16)
3	12-5	(17)	4	D1	Q1 5	(17)
3	12-6	(18)	7	D2	Q2 6	(18)
3	12-9	(19)	8	D3	Q3 9	(19)
3	12-12	(20)	13	D4	Q4 12	(20)
3	12-15	(21)	14	D5	Q5 15	(21)
3	12-16	(22)	17	D6	Q6 16	(22)
3	12-19	(23)	18	D7	Q7 19	(23)
				T	E	
19	72-10	CPLOWERLIM	H	1	OV	

CPU 803

R11445

UPPER AND LOWER LIMIT REGISTERS



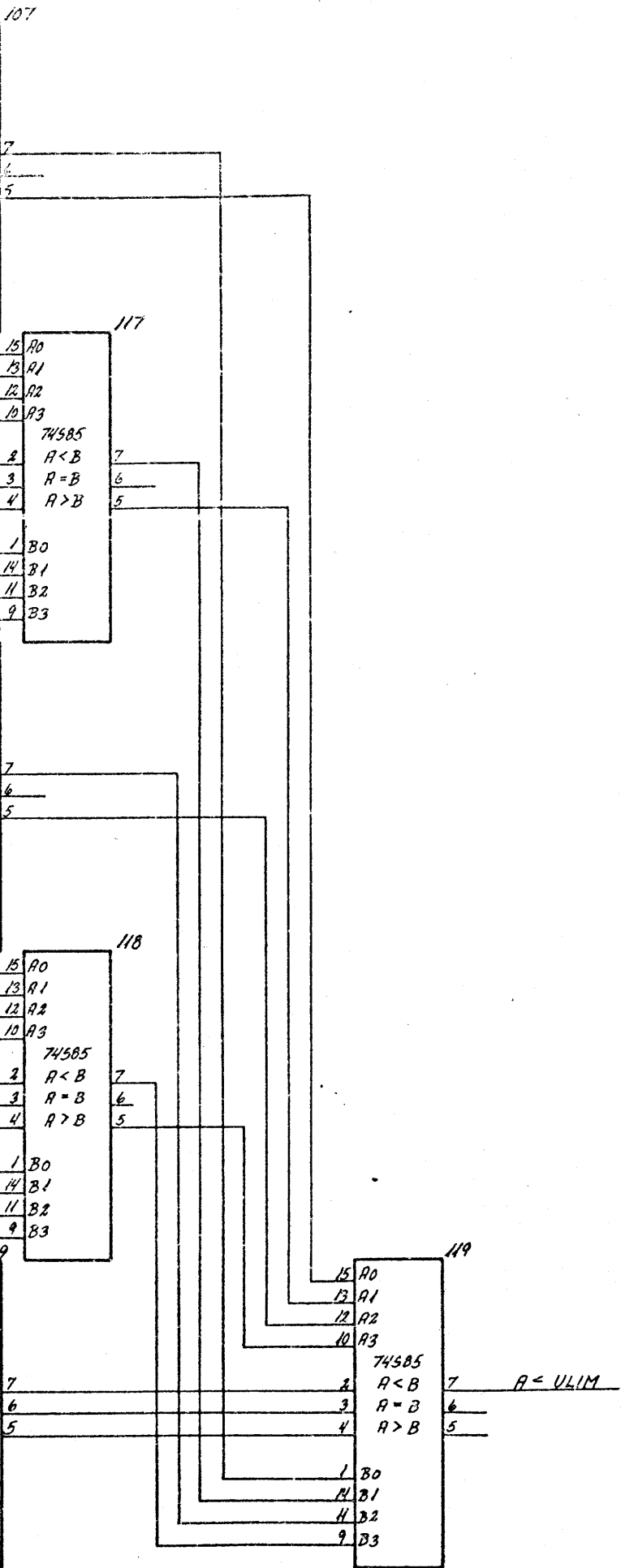
5	47-5	ADDRQUT (0)	15	A0
5	47-6	(1)	13	A1
5	47-9	(2)	12	A2
5	47-12	(3)	10	A3
				74585
9	67-12	UPPERLIM (4)	2	A < B
			3	A = B
			4	A > B
5	47-15	ADDRQUT (4)	15	A0
9	67-2	UPPERLIM (0)	1	B0
9	67-5	(1)	14	B1
9	67-6	(2)	11	B2
9	67-9	(3)	9	B3

5	47-16	ADDRQUT (5)	15	A0
5	47-19	(6)	13	A1
6	48-2	(7)	12	A2
6	48-5	(8)	10	A3
				74585
9	68-5	UPPERLIM (9)	2	A < B
			3	A = B
			4	A > B
6	48-6	ADDRQUT (9)	15	A0
9	67-15	UPPERLIM (5)	1	B0
9	67-16	(6)	14	B1
9	67-19	(7)	11	B2
9	68-2	(8)	9	B3

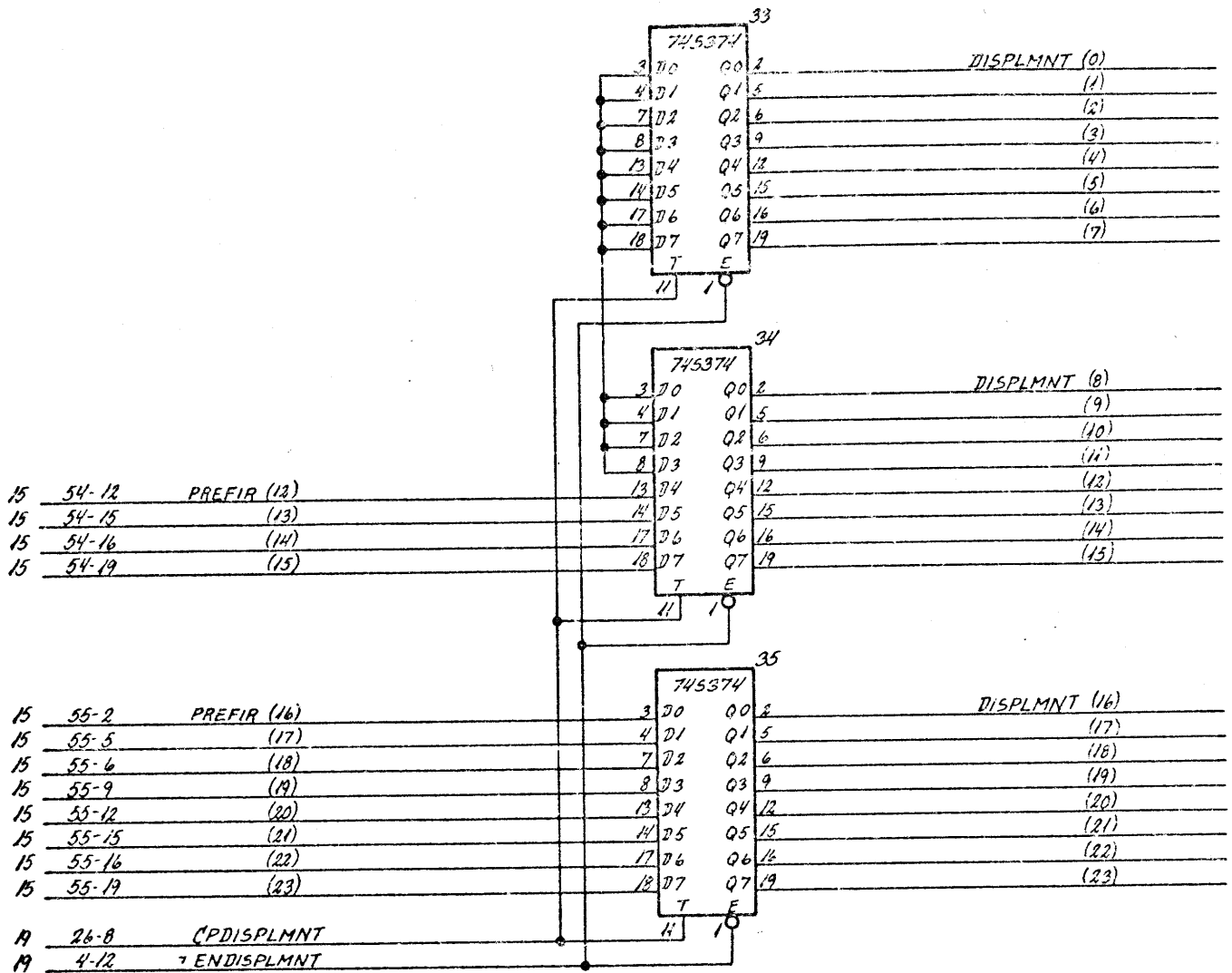
6	48-9	ADDRQUT (10)	15	A0
6	48-12	(11)	13	A1
6	48-15	(12)	12	A2
6	48-16	(13)	10	A3
				74585
9	68-16	UPPERLIM (14)	2	A < B
			3	A = B
			4	A > B
6	48-19	ADDRQUT (14)	15	A0
9	68-6	UPPERLIM (10)	1	B0
9	68-9	(11)	14	B1
9	68-12	(12)	11	B2
9	68-15	(13)	9	B3

7	49-2	ADDRQUT (15)	15	A0
7	49-5	(16)	13	A1
7	49-6	(17)	12	A2
7	49-9	(18)	10	A3
				74585
9	69-9	UPPERLIM (19)	2	A < B
			3	A = B
			4	A > B
7	49-12	ADDRQUT (19)	15	A0
9	68-19	UPPERLIM (15)	1	B0
9	69-2	(16)	14	B1
9	69-5	(17)	11	B2
9	69-6	(18)	9	B3

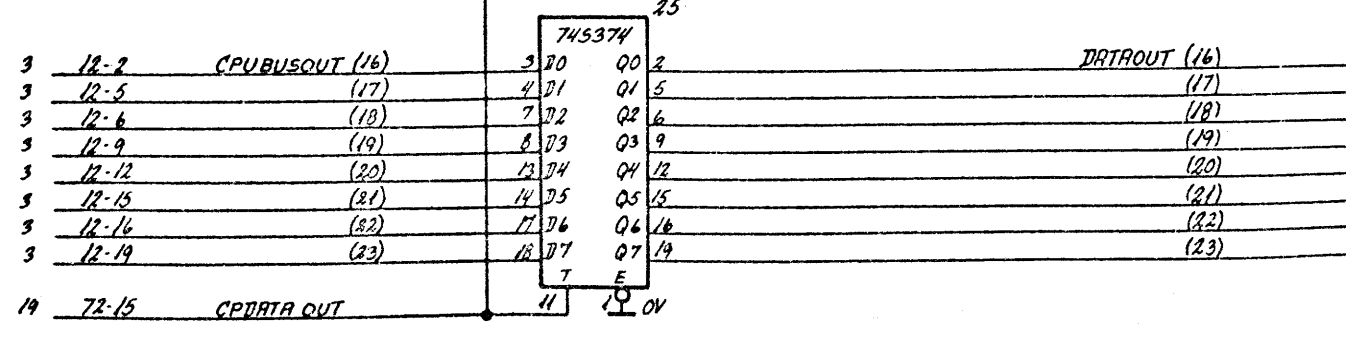
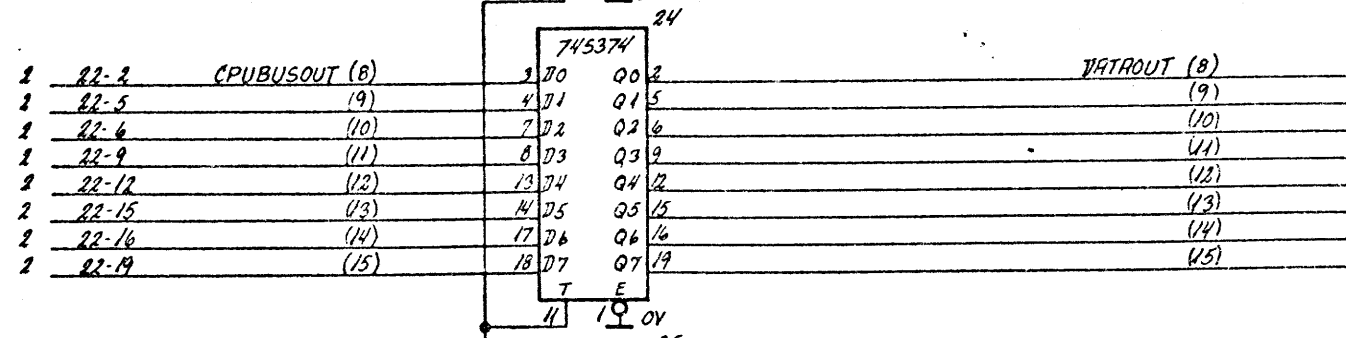
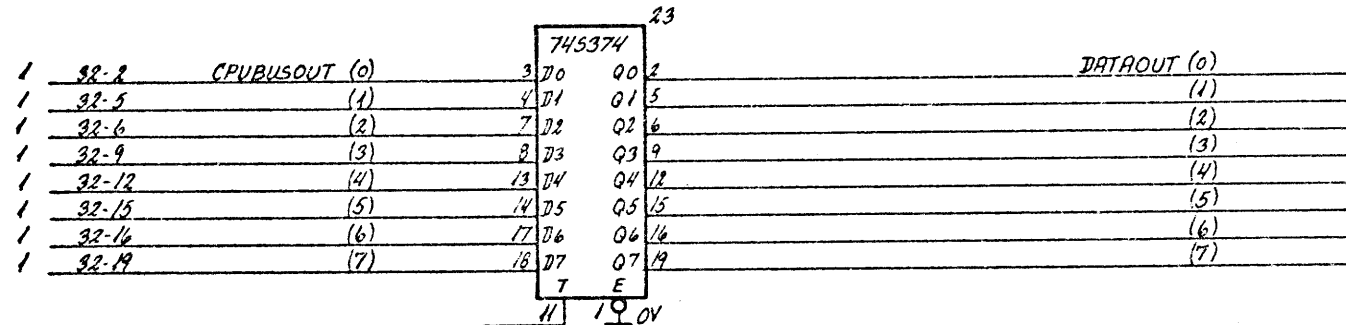
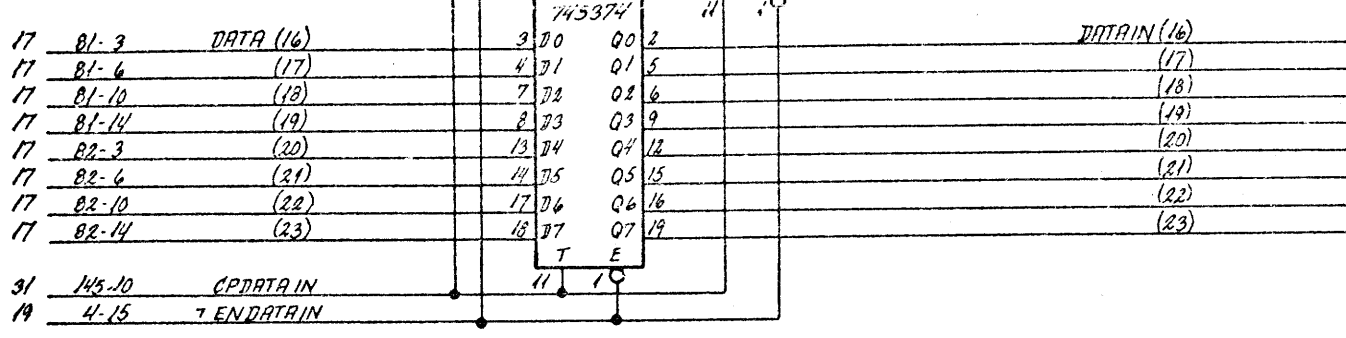
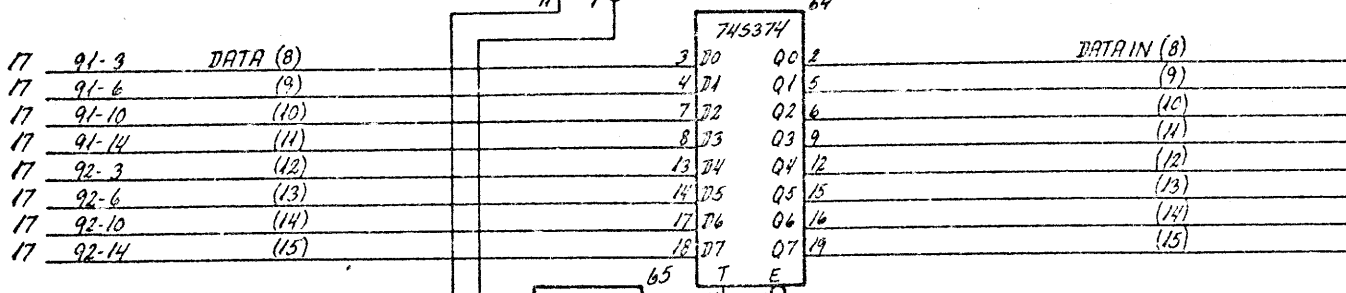
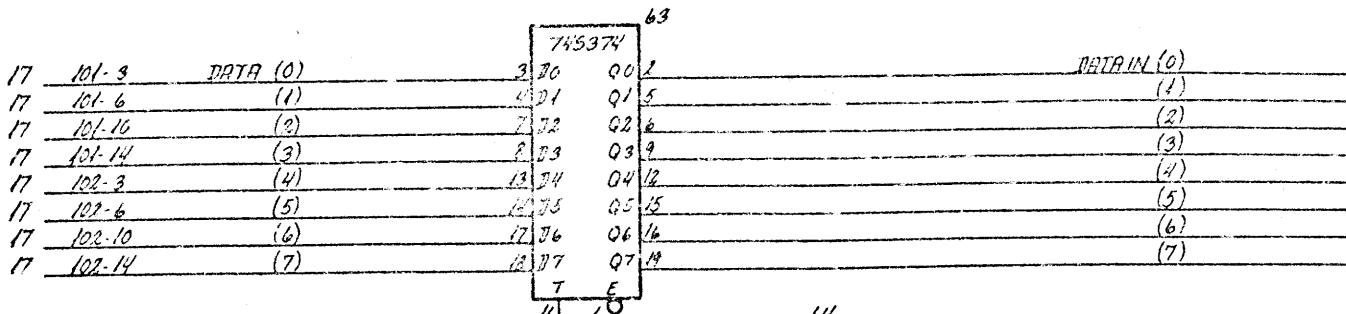
7	49-15	ADDRQUT (20)	15	A0
7	49-16	(21)	13	A1
7	49-19	(22)	12	A2
			10	A3
				74585
			2	A < B
			3	A = B
			4	A > B
25	150-10	ONE H		
9	69-12	UPPERLIM (20)	1	B0
9	69-15	(21)	14	B1
9	69-16	(22)	11	B2
			9	B3



760406 REF 760407 A0B



751219 REF 740308 RO3

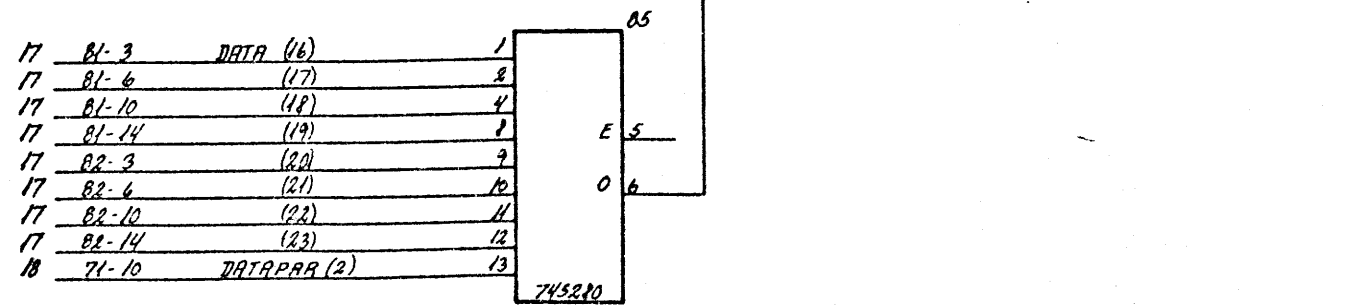
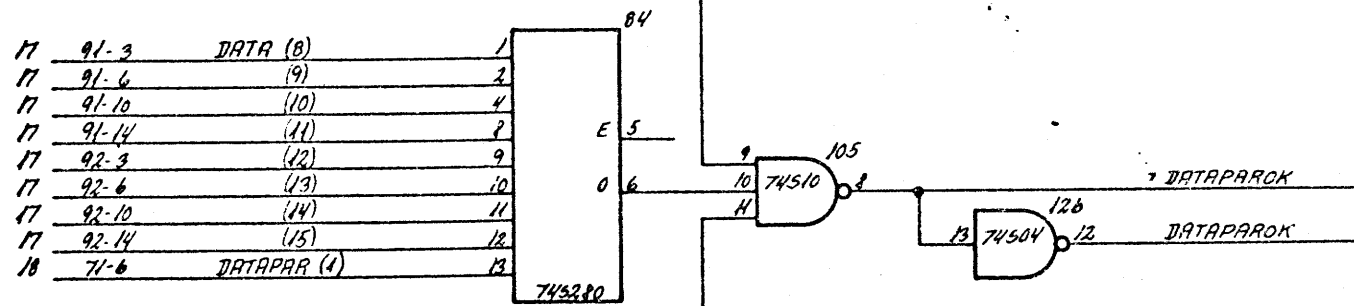
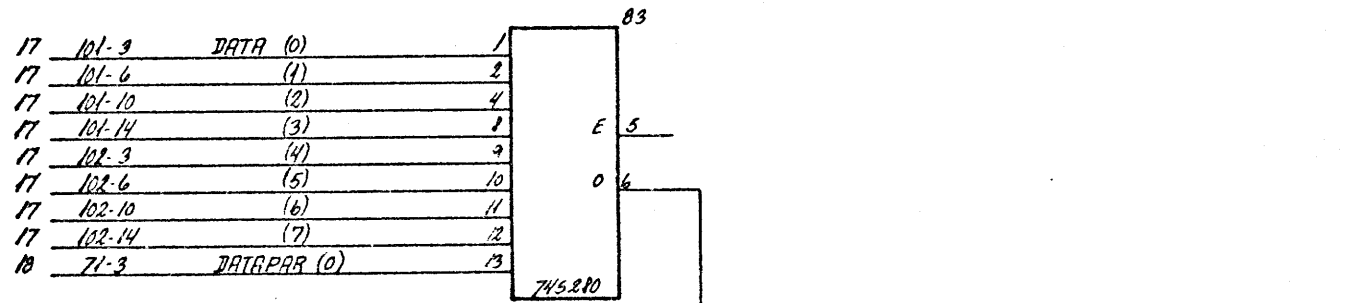
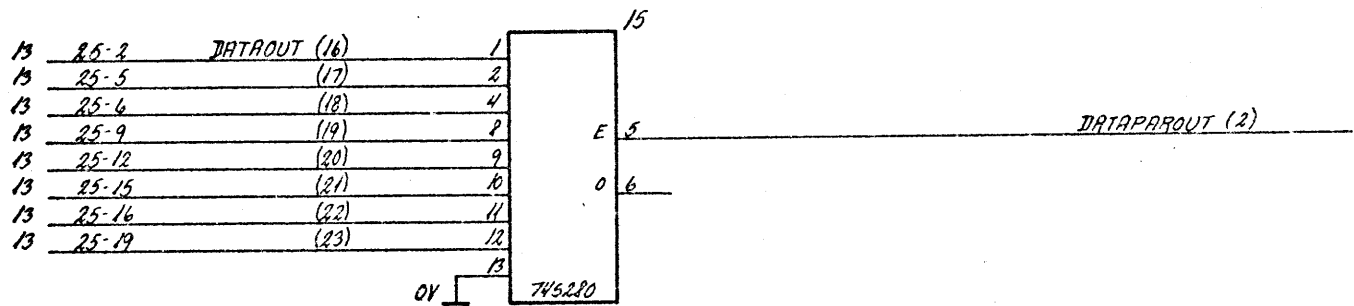
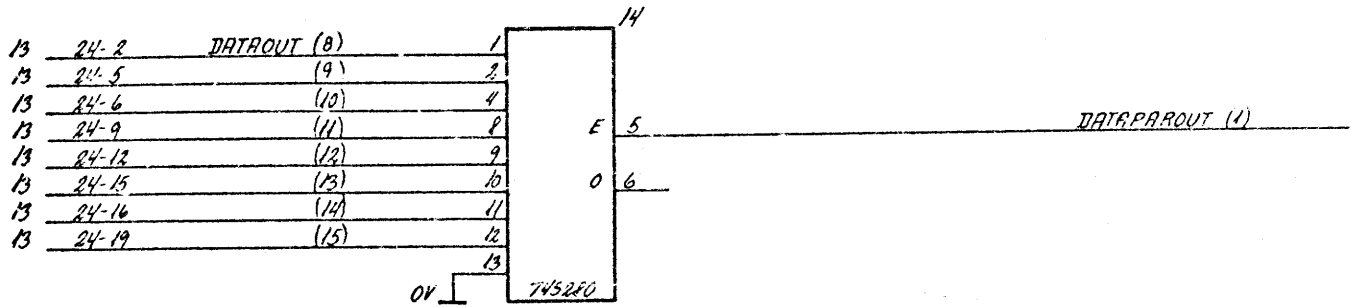
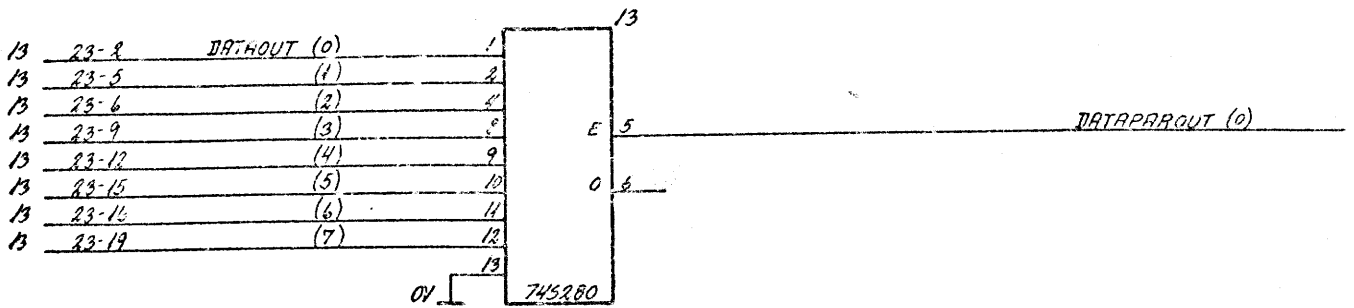


751210 RPT 760301 A03

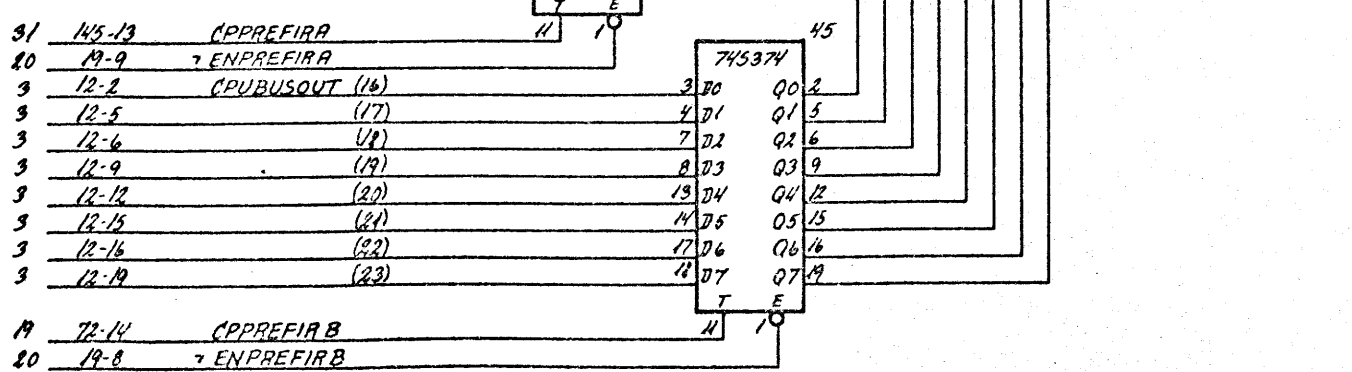
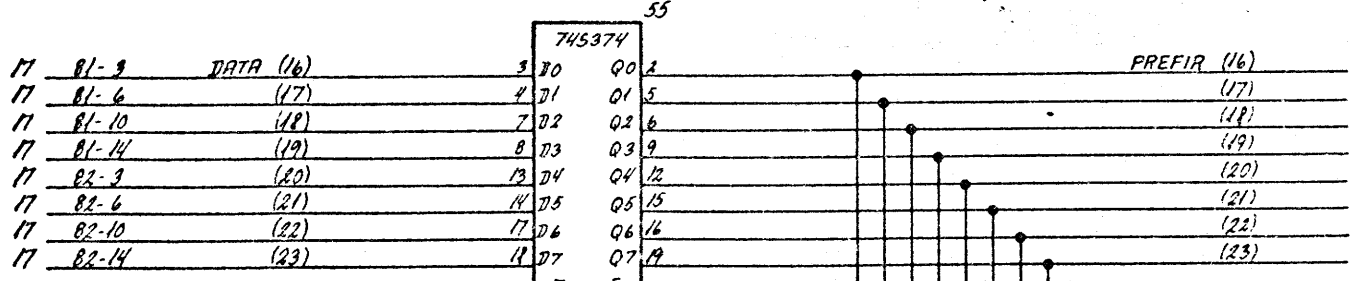
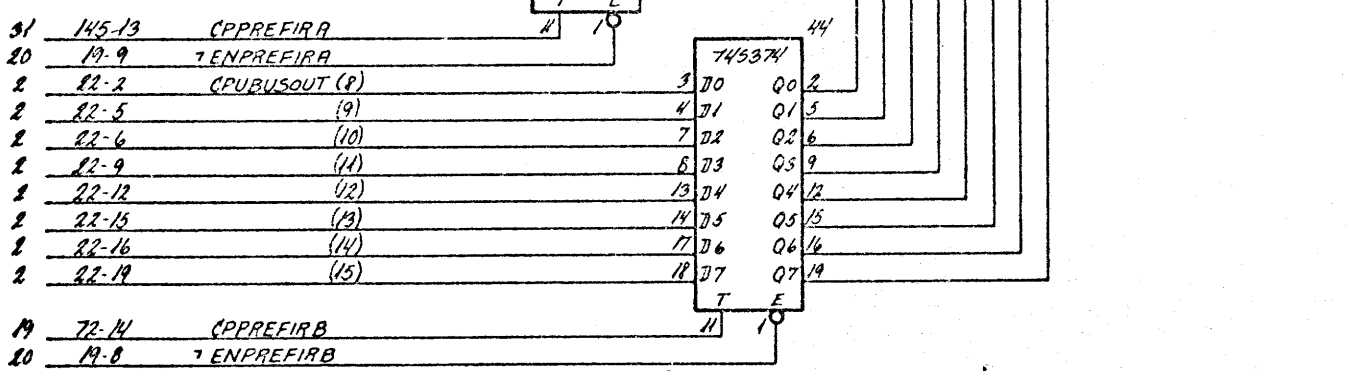
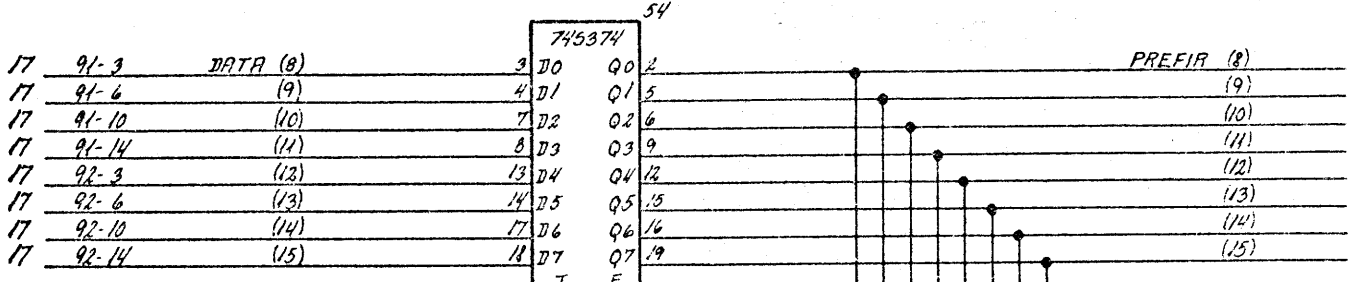
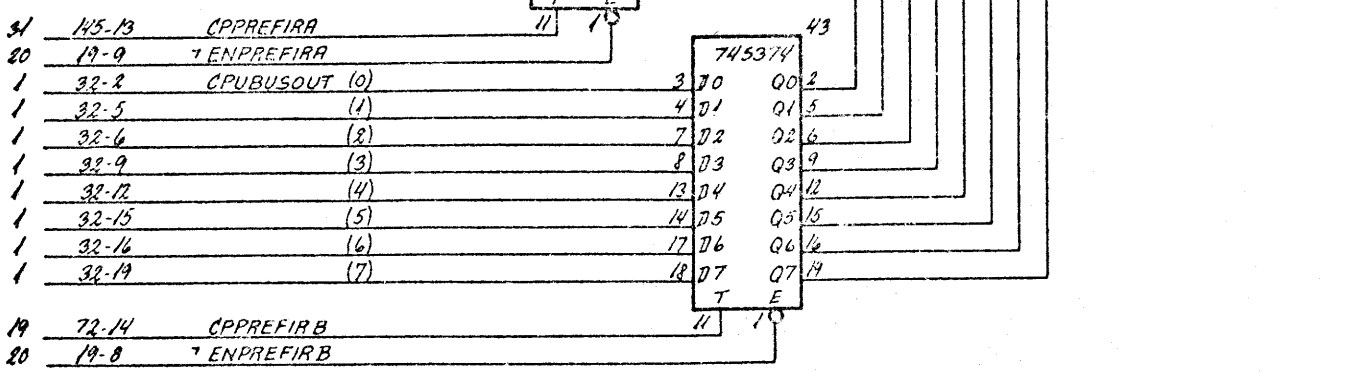
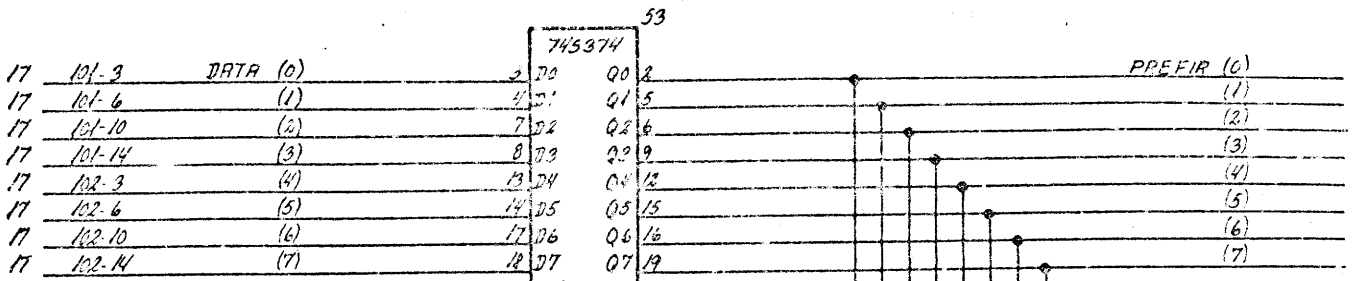
CPU803

R11449

I/O DATA-IN AND I/O DATA-OUT REGISTERS



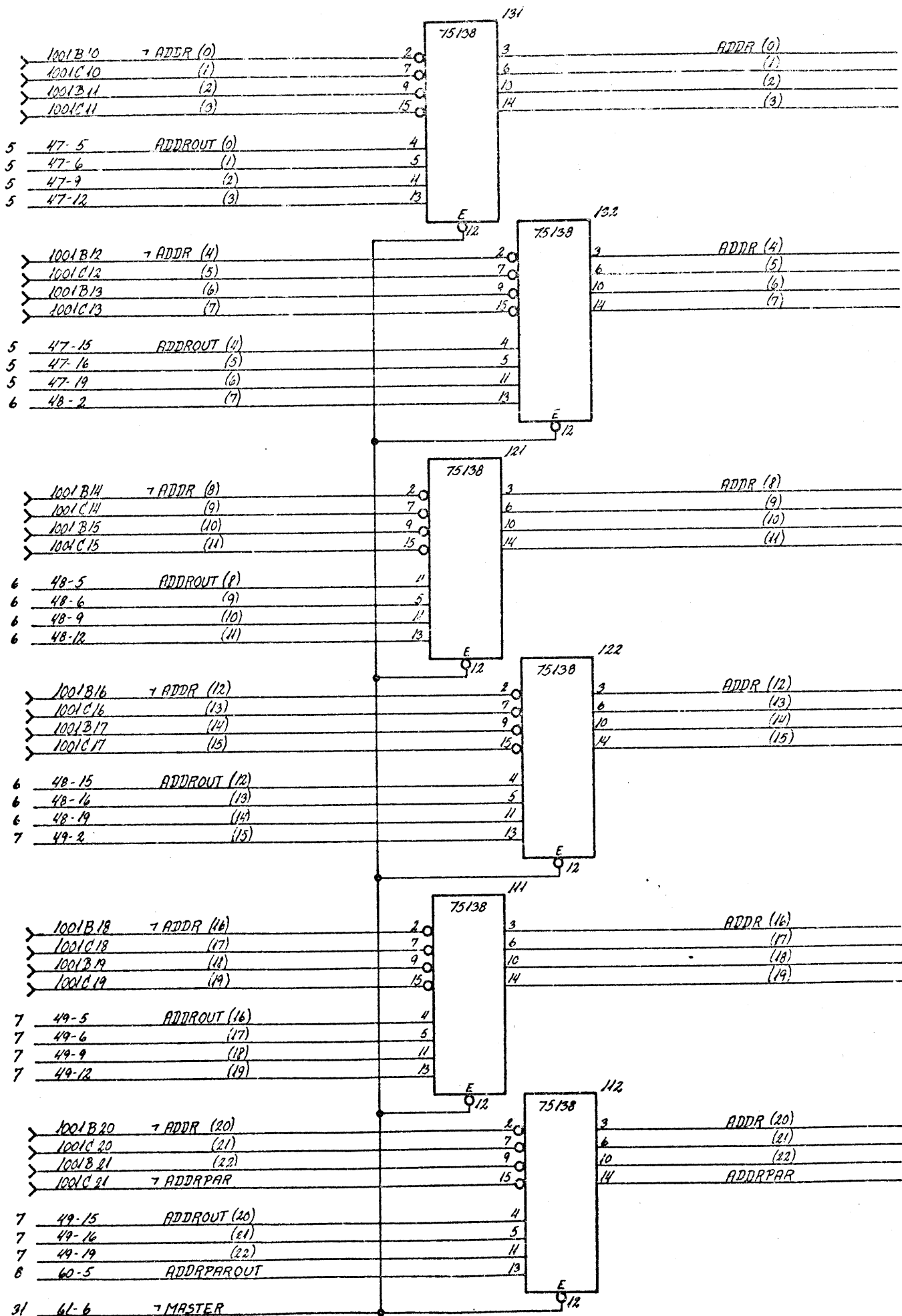
751210 ARR 76030P ROB



751219 MAR 760301 A03

CPU 803
R11451

PREFETCH INSTRUCTION REGISTERS

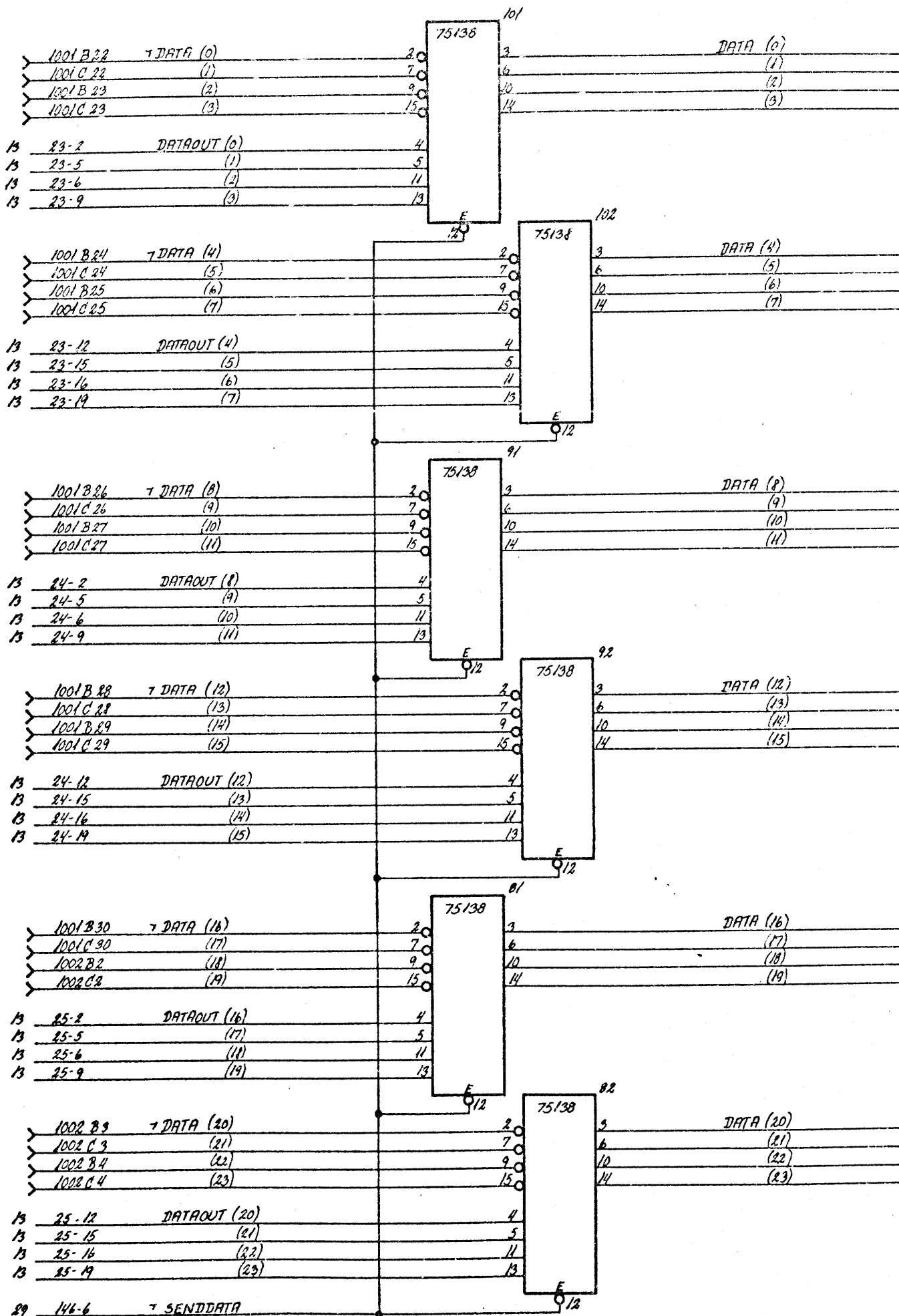


751215 ROE
751215 PAI

CPU 803

BUS TRANSCEIVER FOR ADDRESS

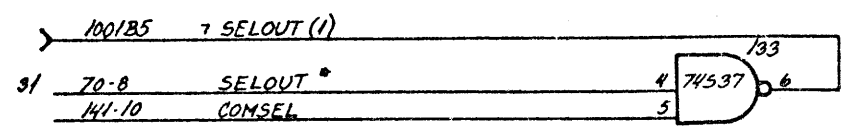
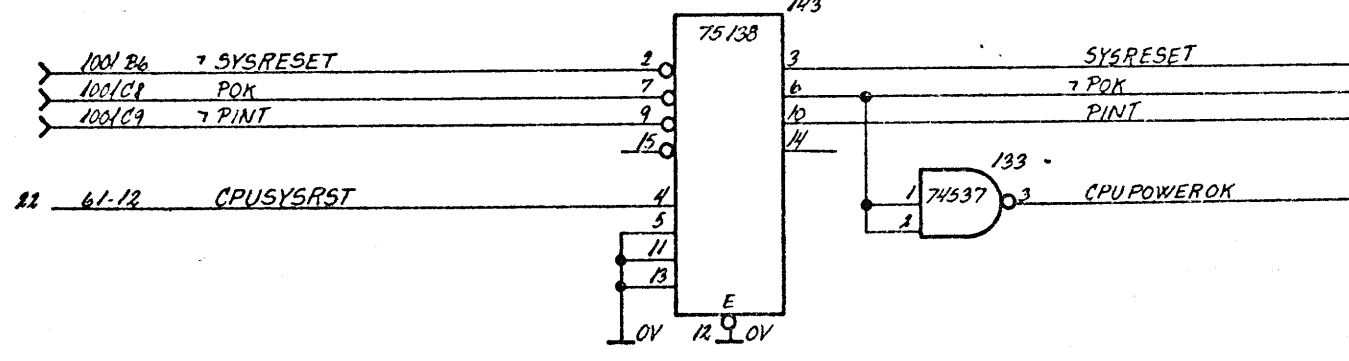
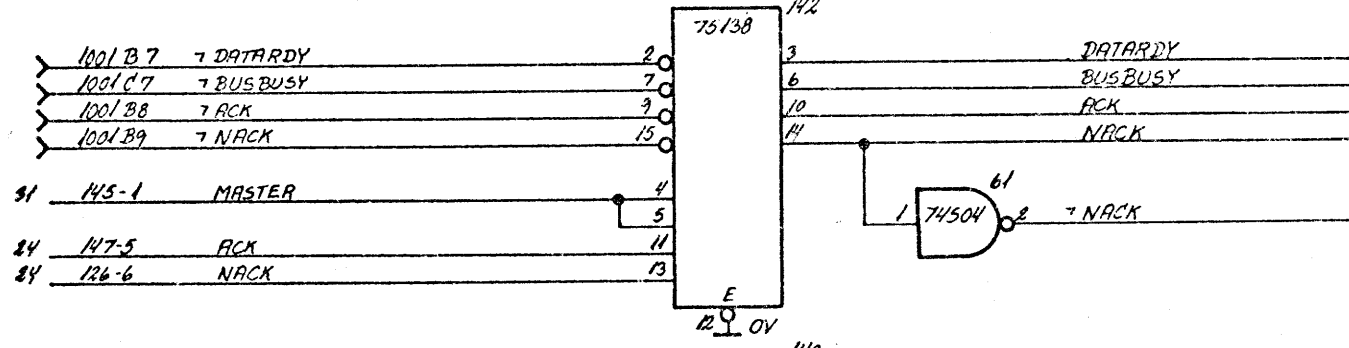
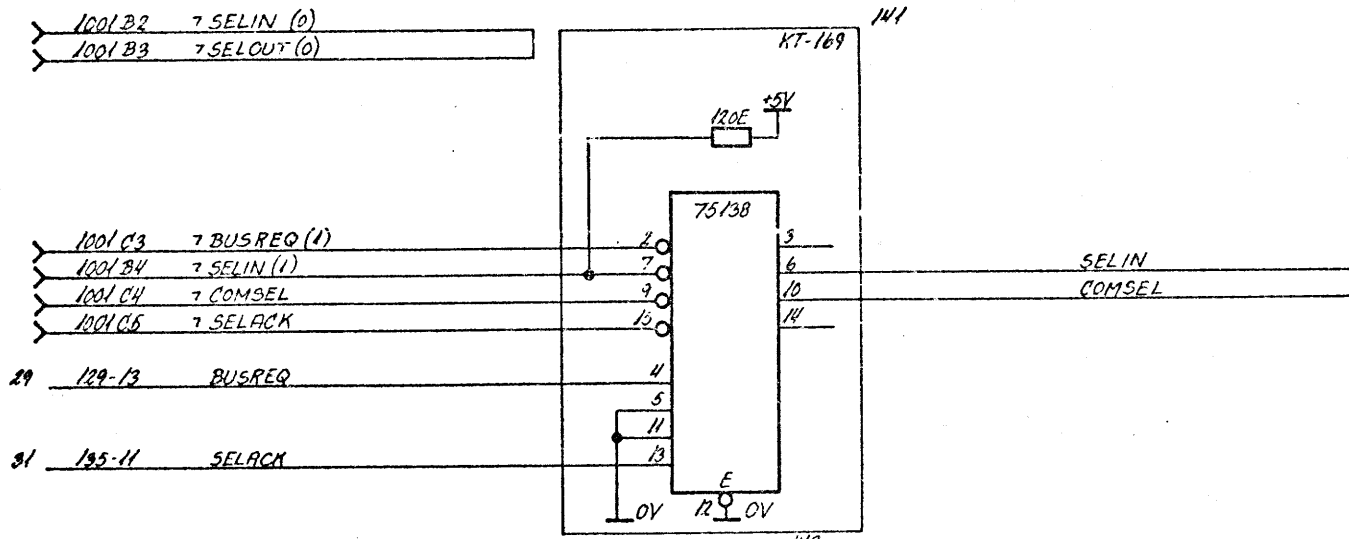
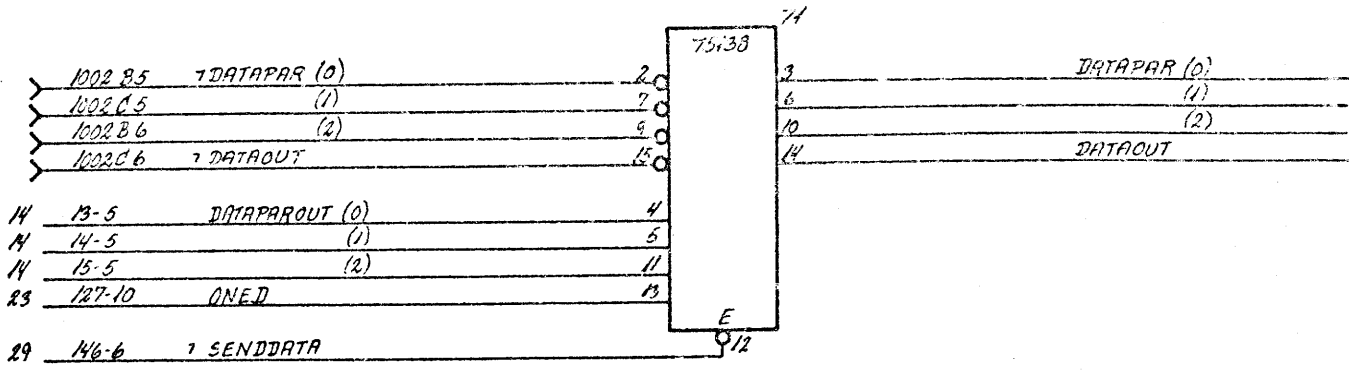
R11452



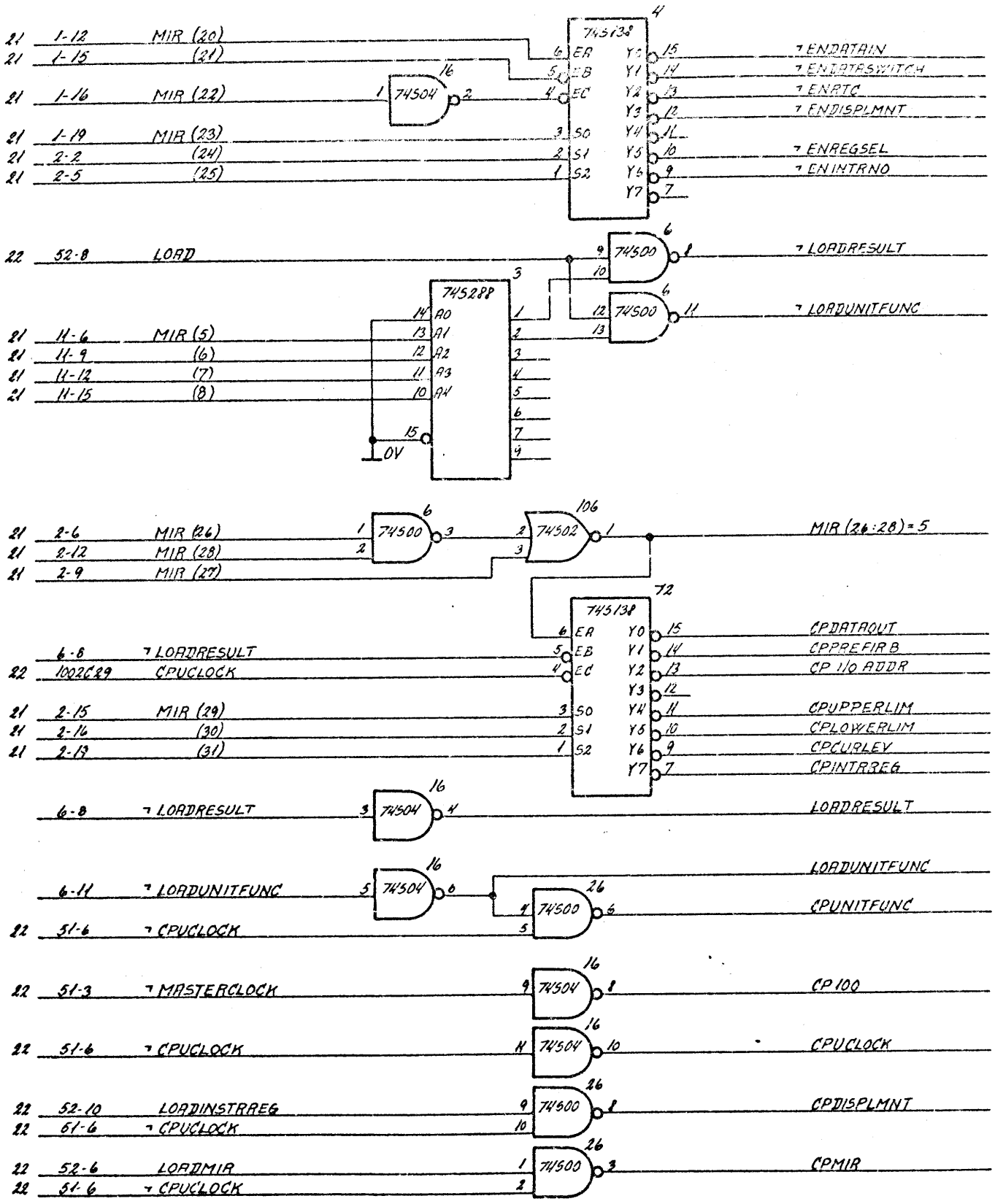
751215 A08
751215 A03

CPU 803
R11453

BUS TRANSCEIVERS FOR DATA



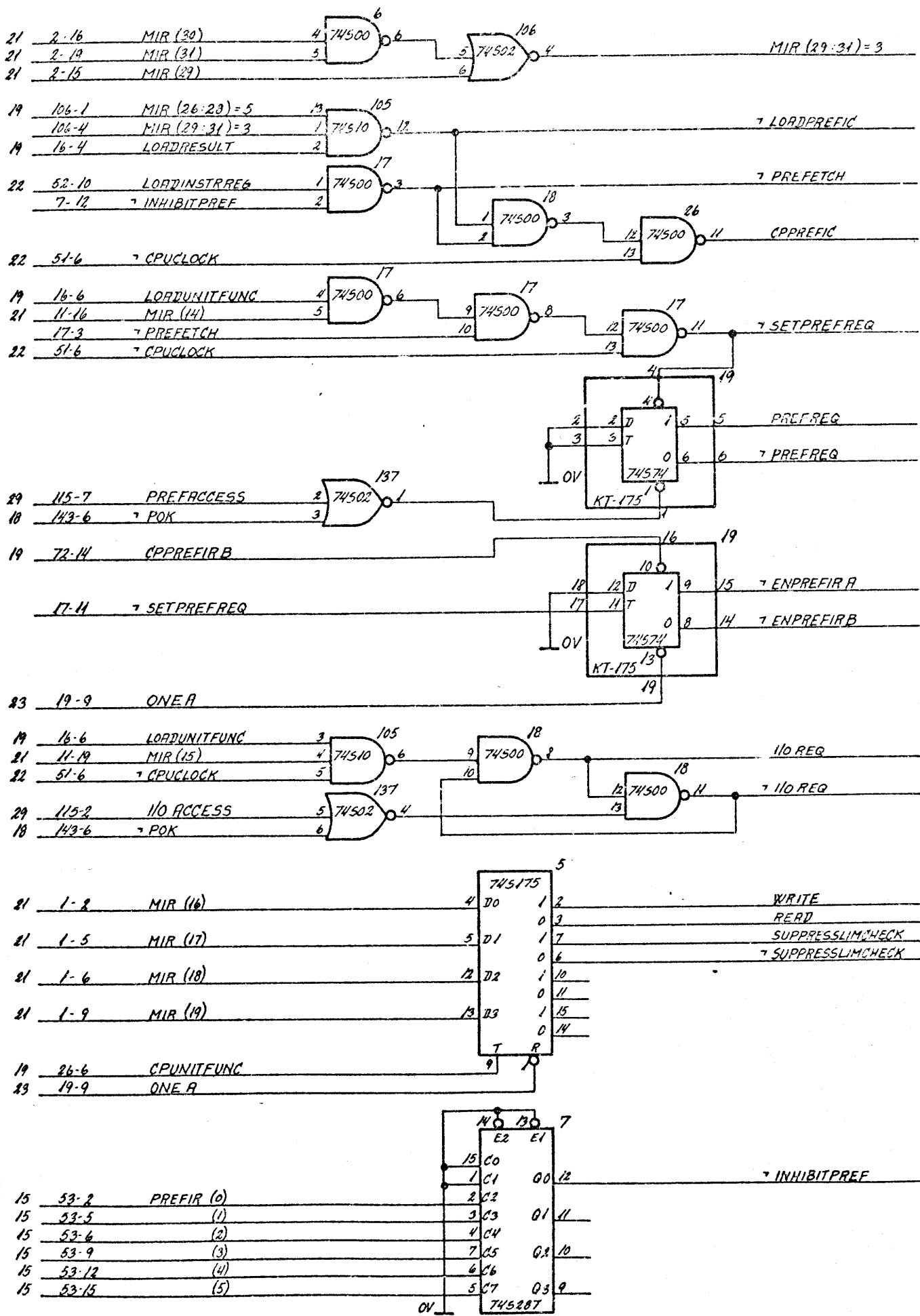
75129 897 75129 828

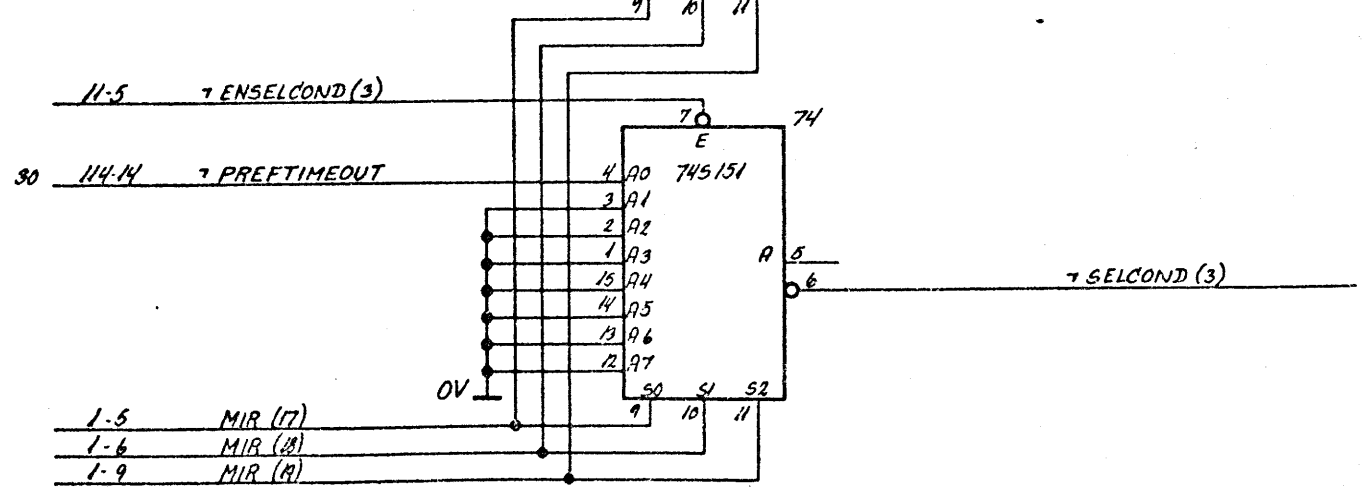
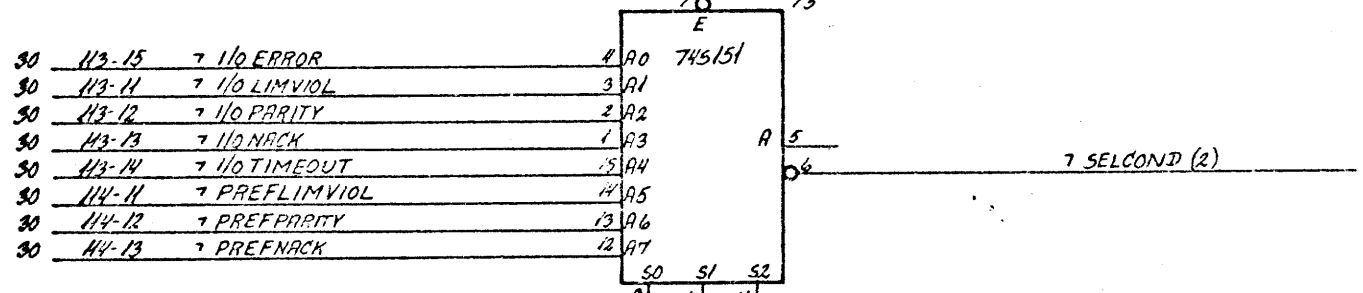
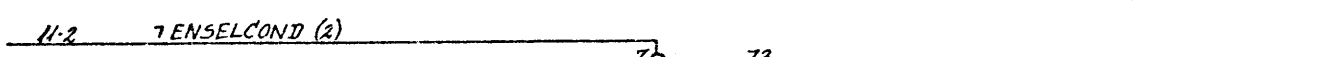
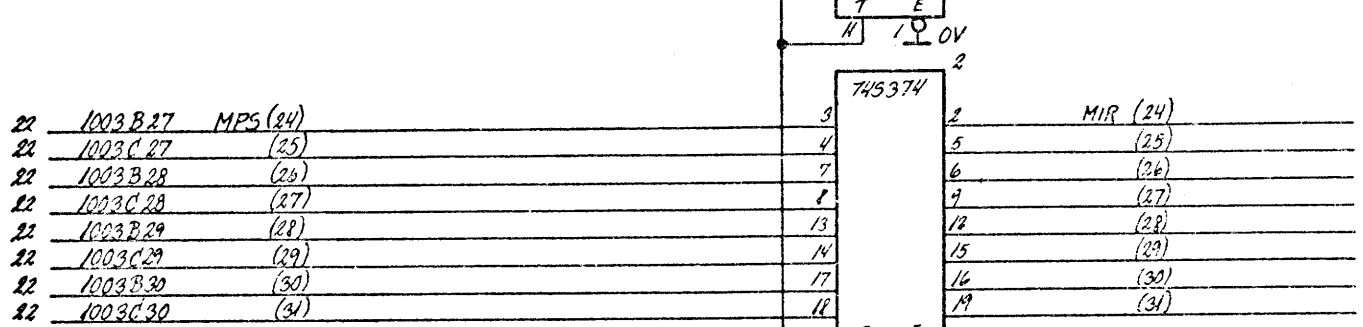
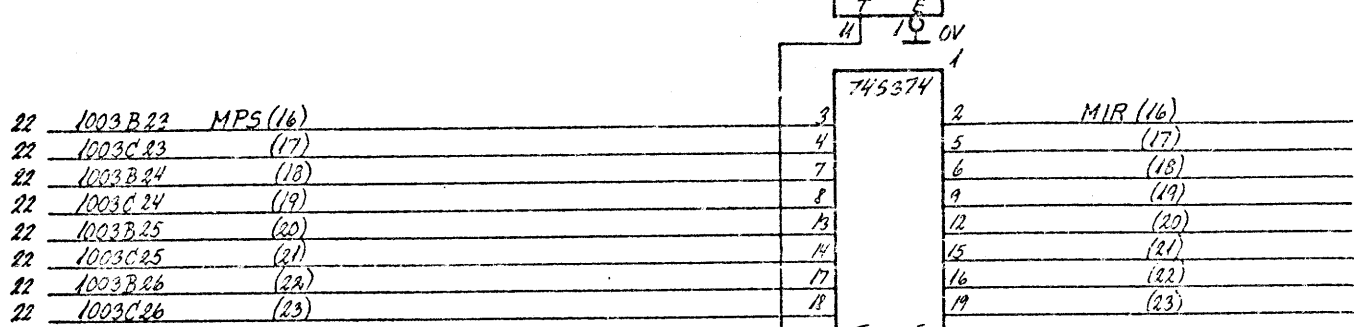
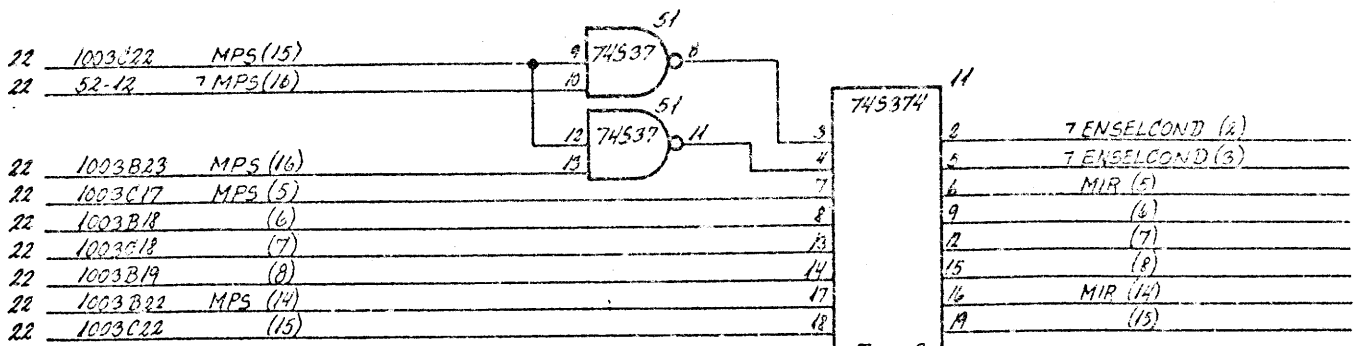


751221 REV 780310 R02

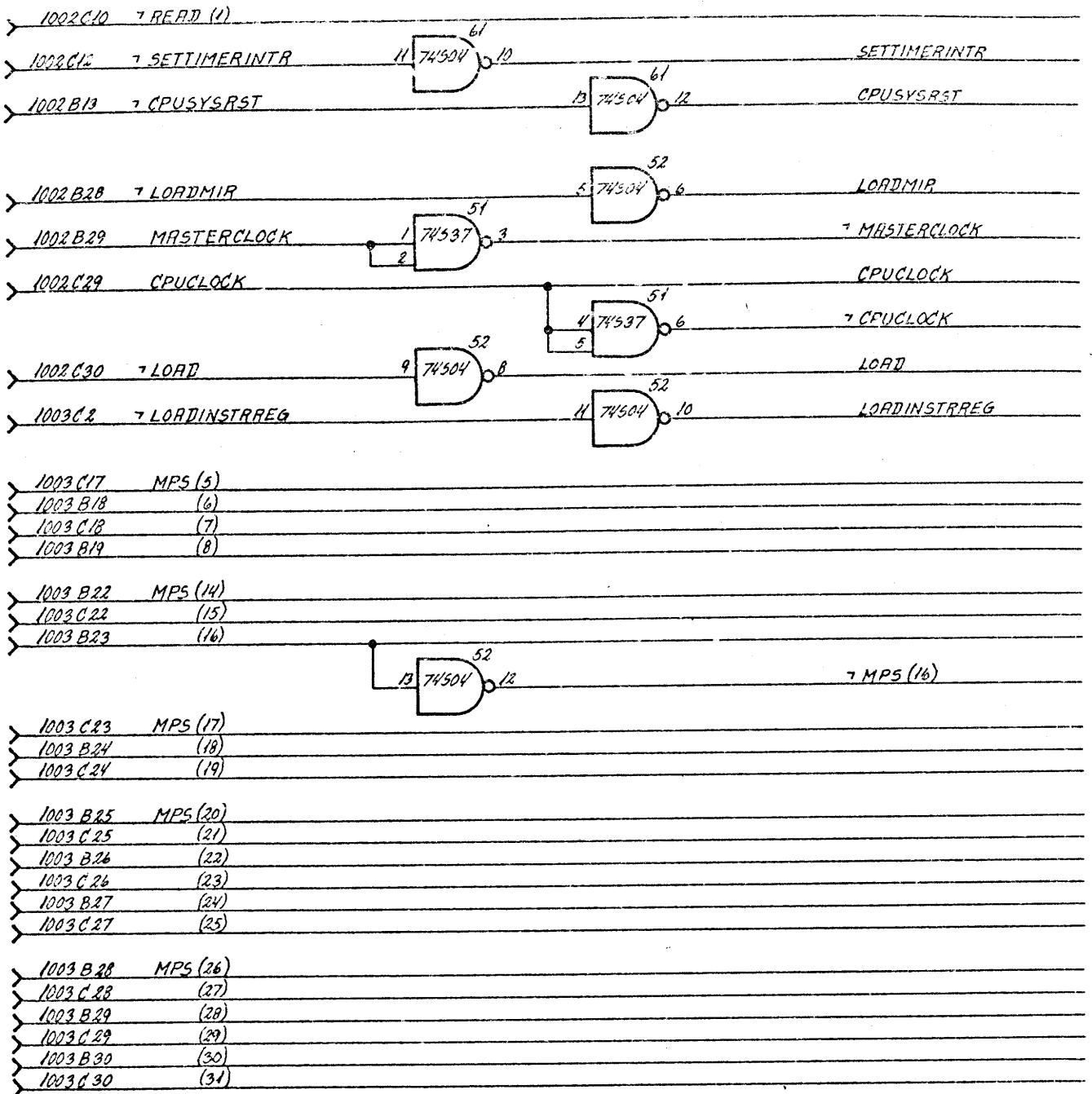
CPU003
R11455

SOURCE ADDRESS DECODING
AND REGISTER CLOCK CONTROL

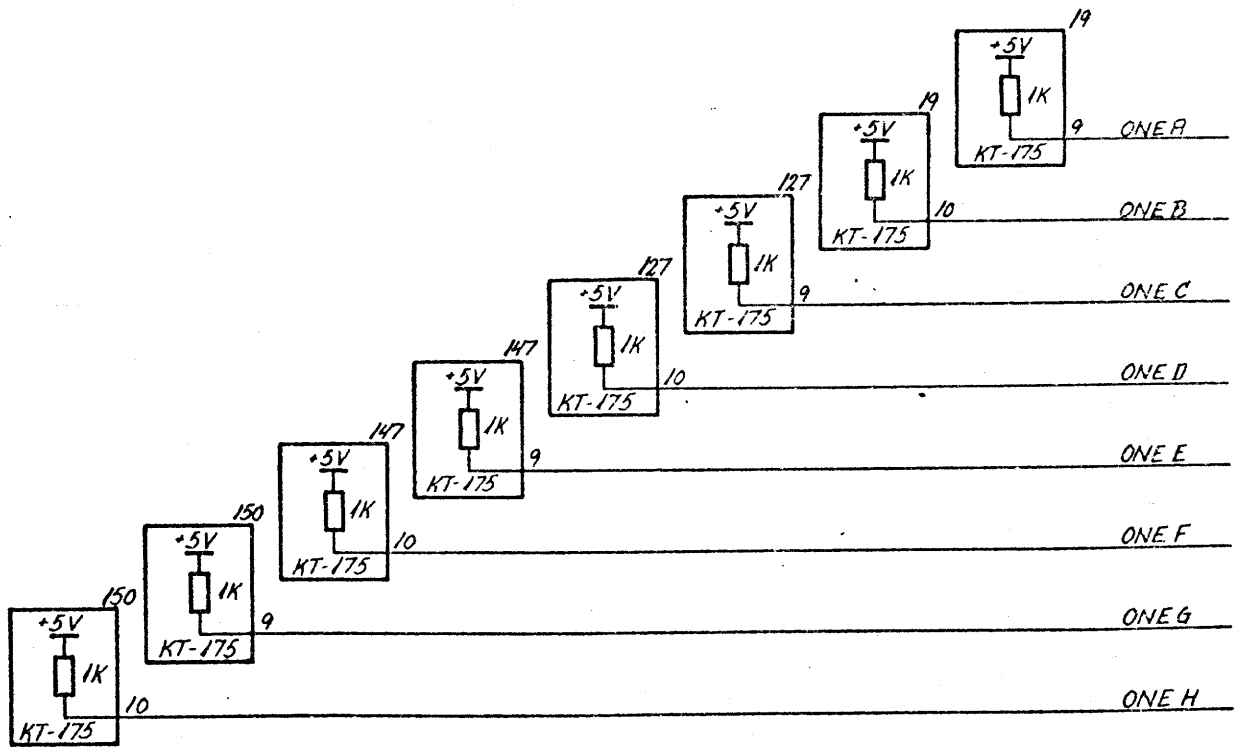
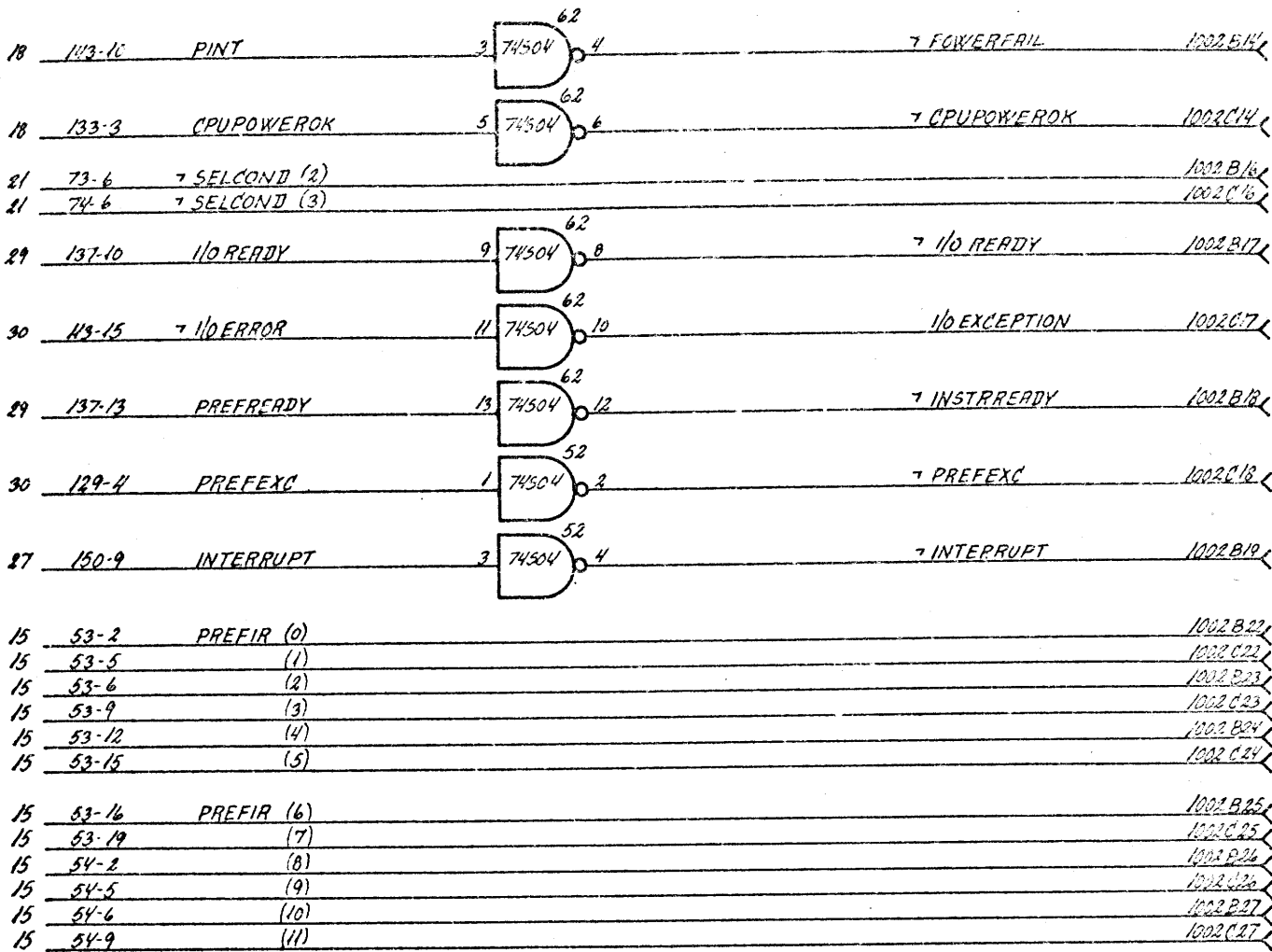




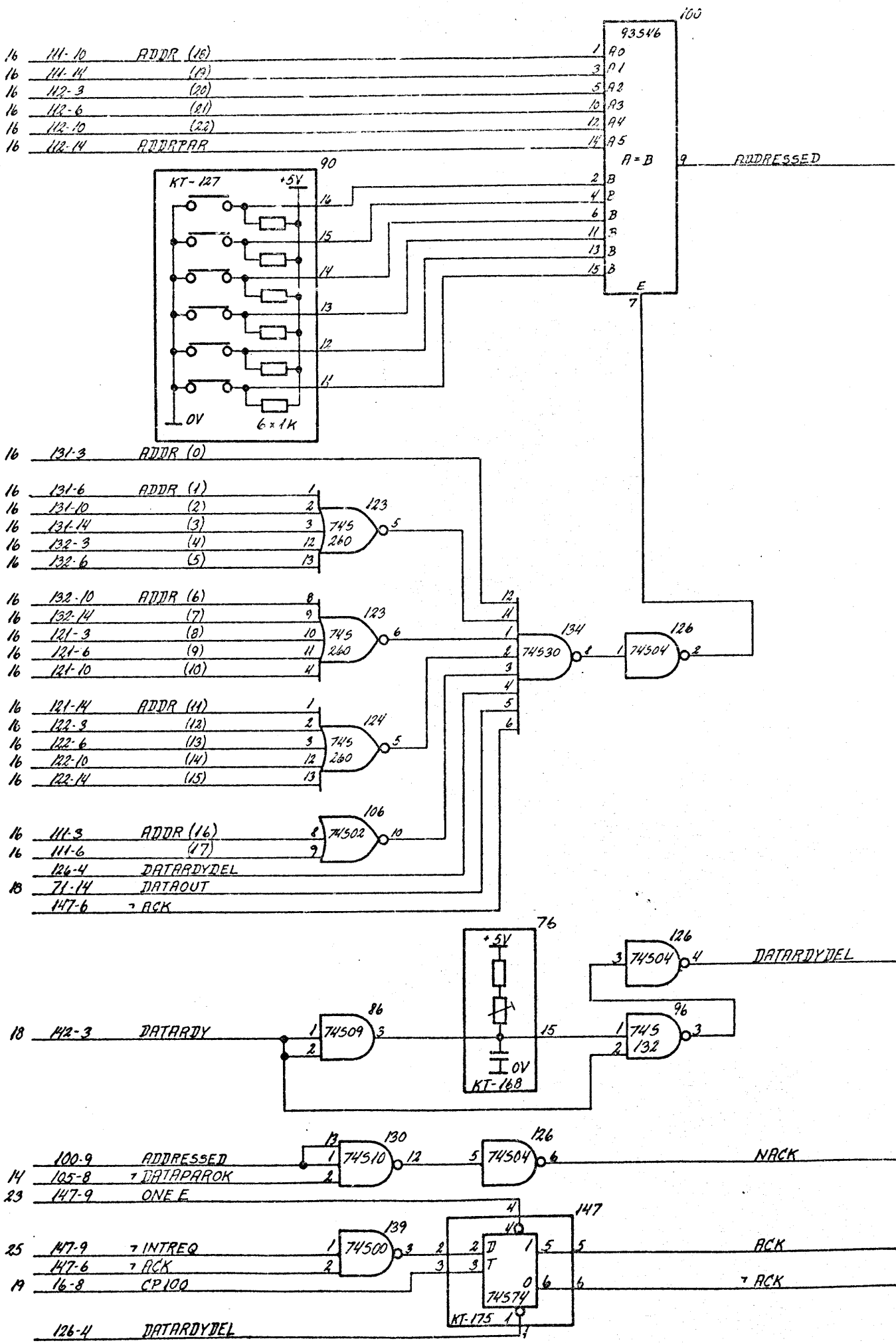
751219 ARJ 751219 ARB

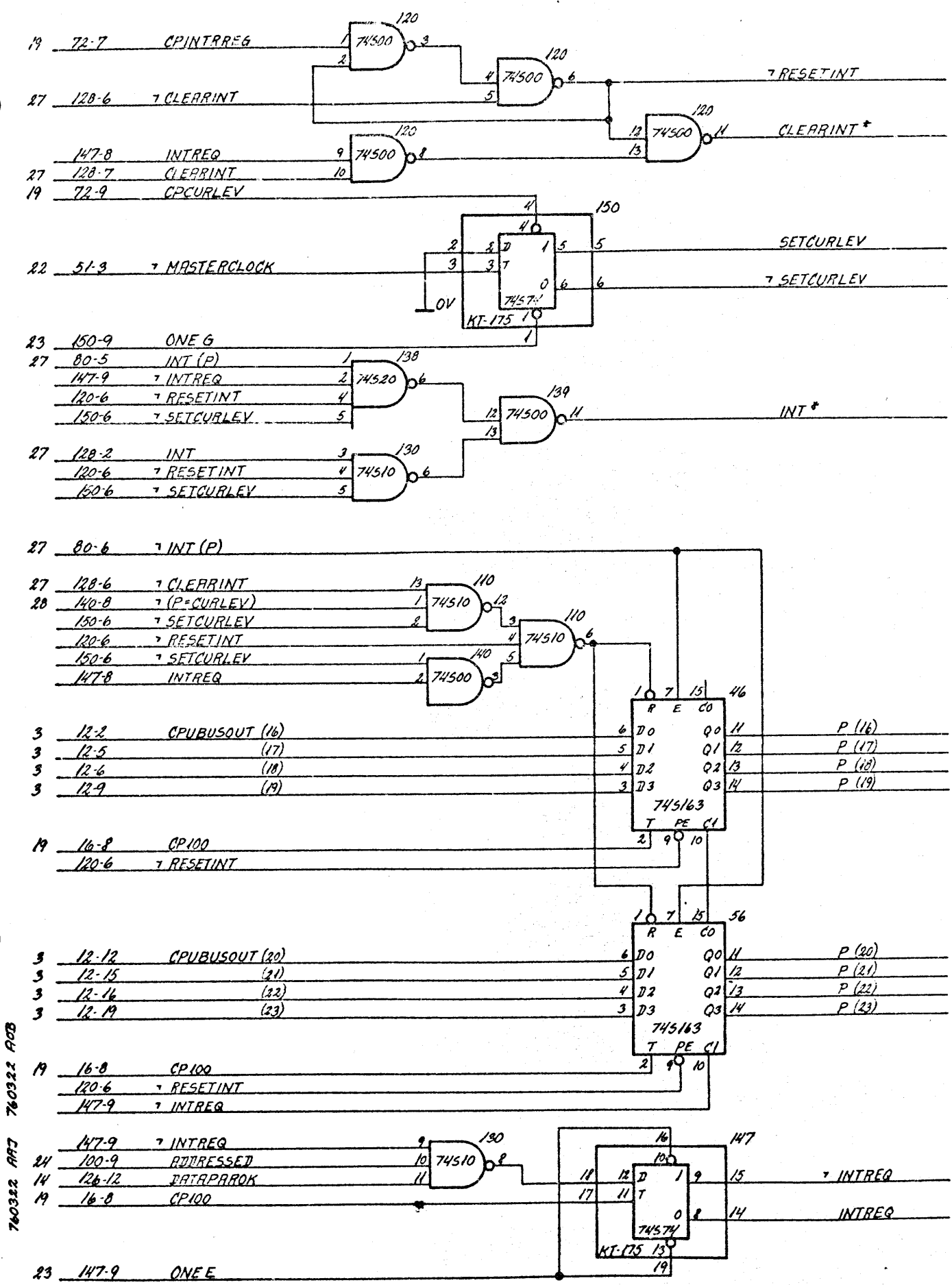


751223 RA7 740310 R03

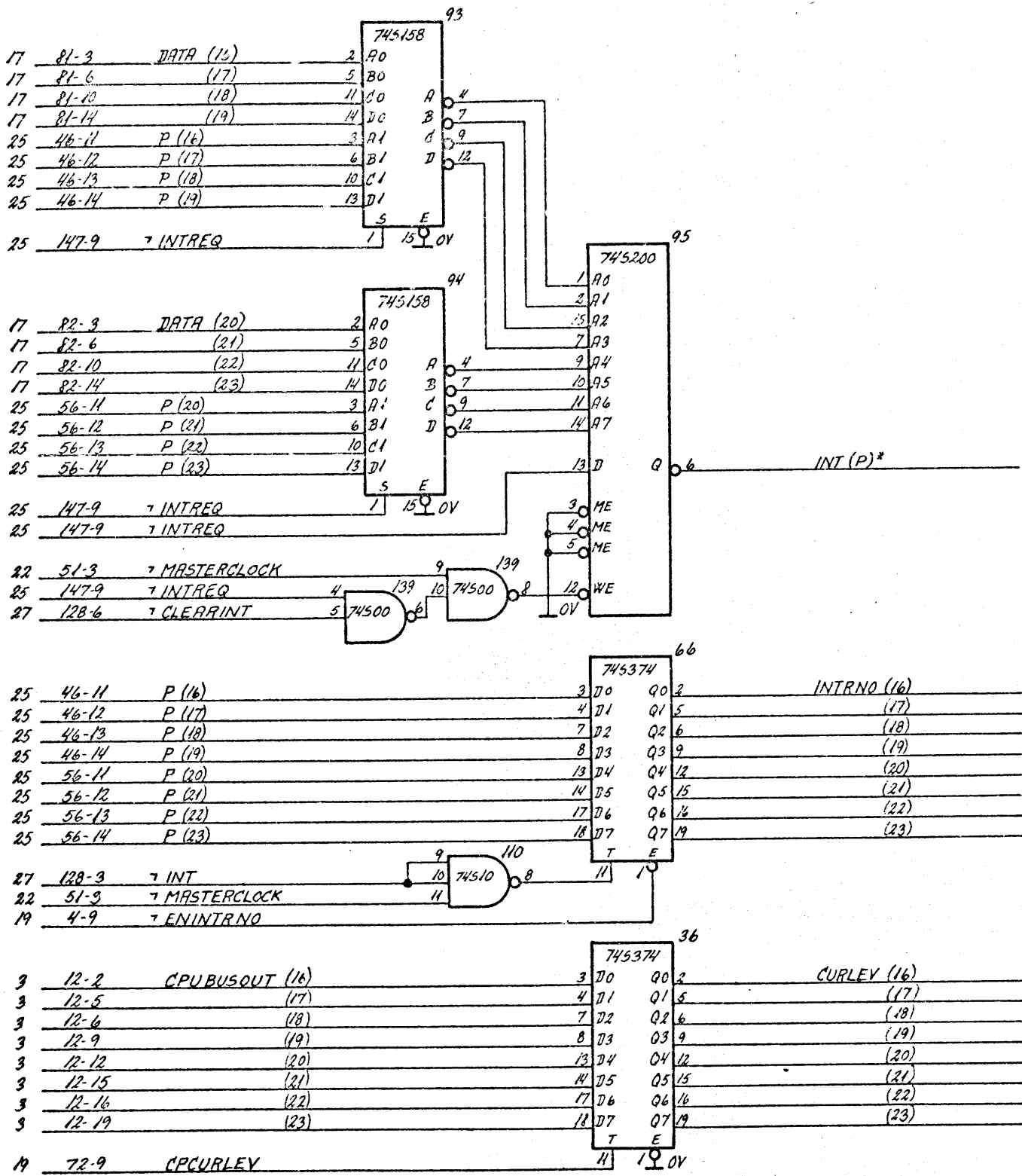


75123 ARJ 760310 AOB

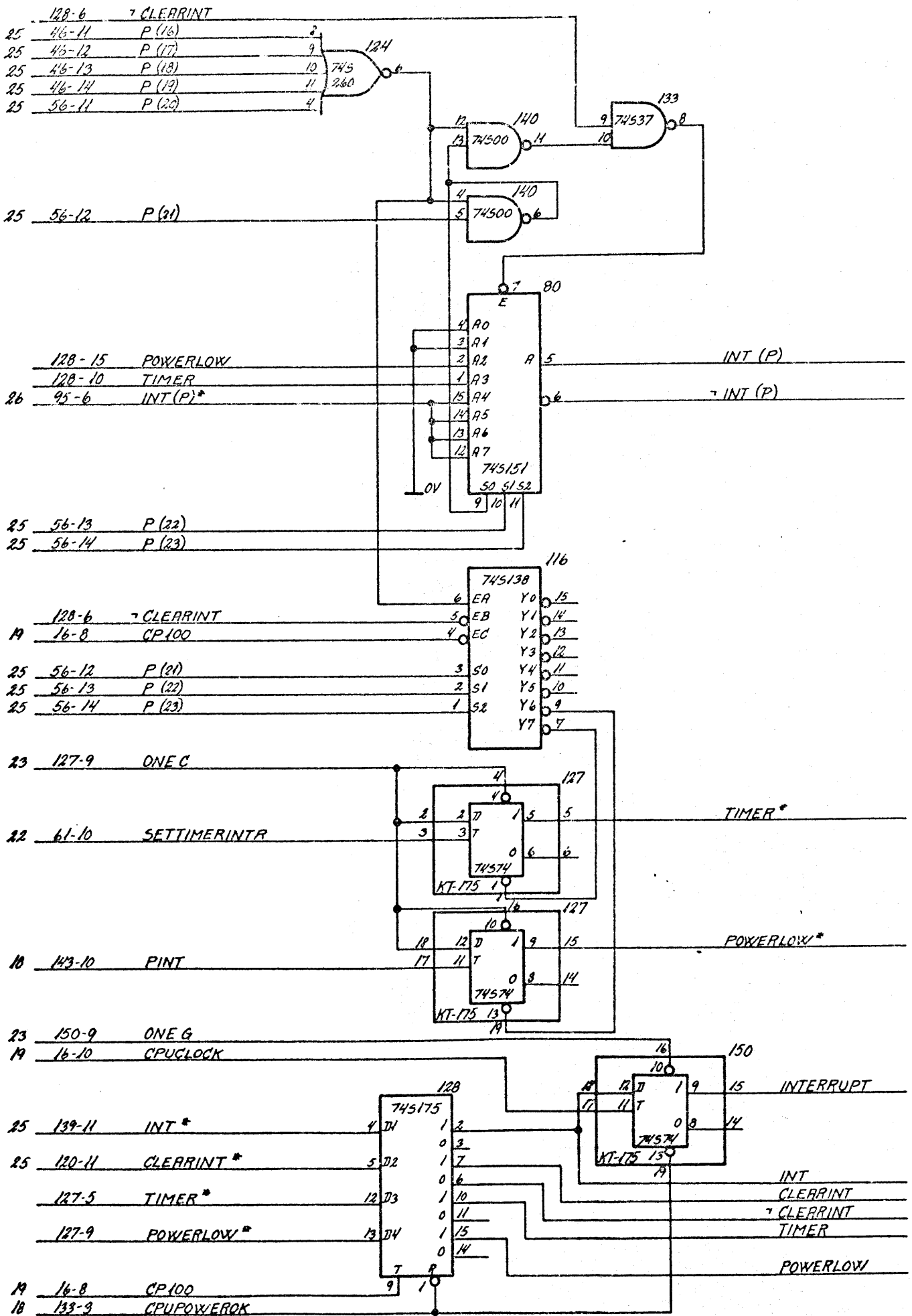




760322 A03
760322 A07



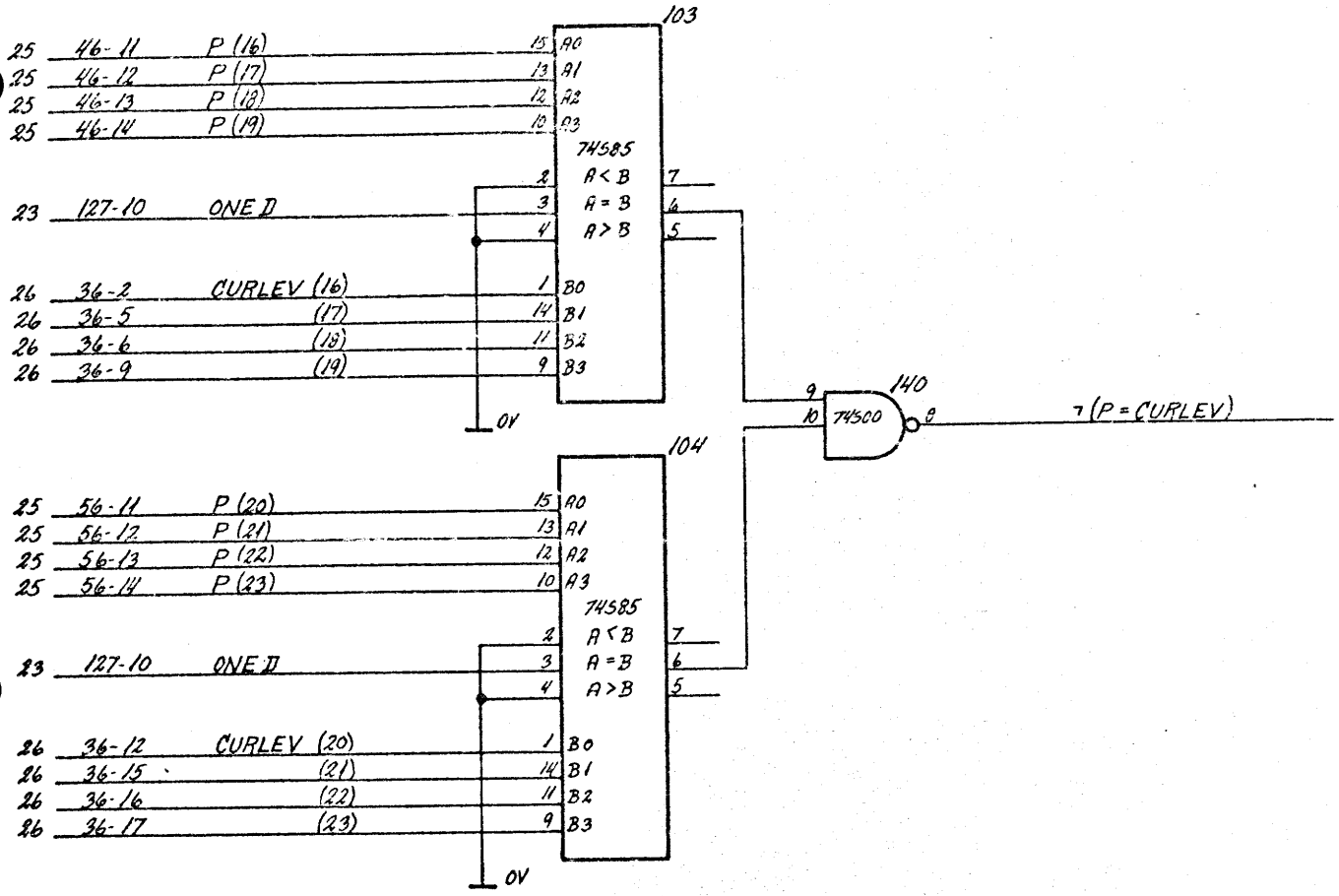
76.0322 RRT 76.0322 R03



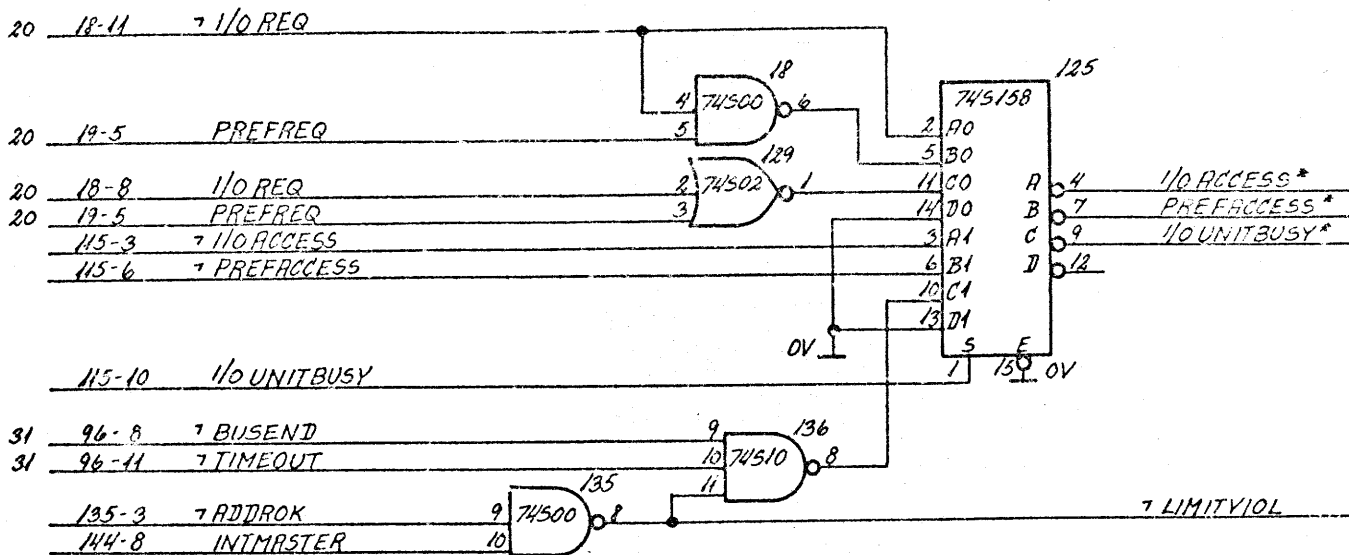
760322 ARJ 760322 ARB

CPU 803
R11463

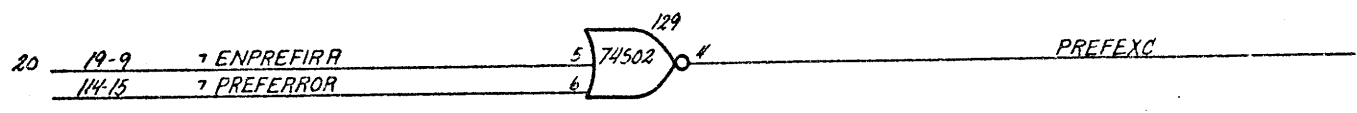
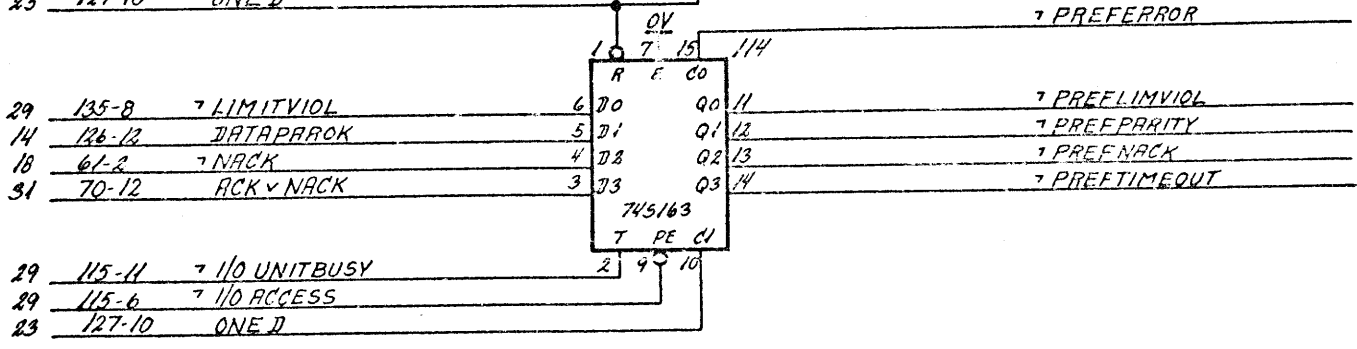
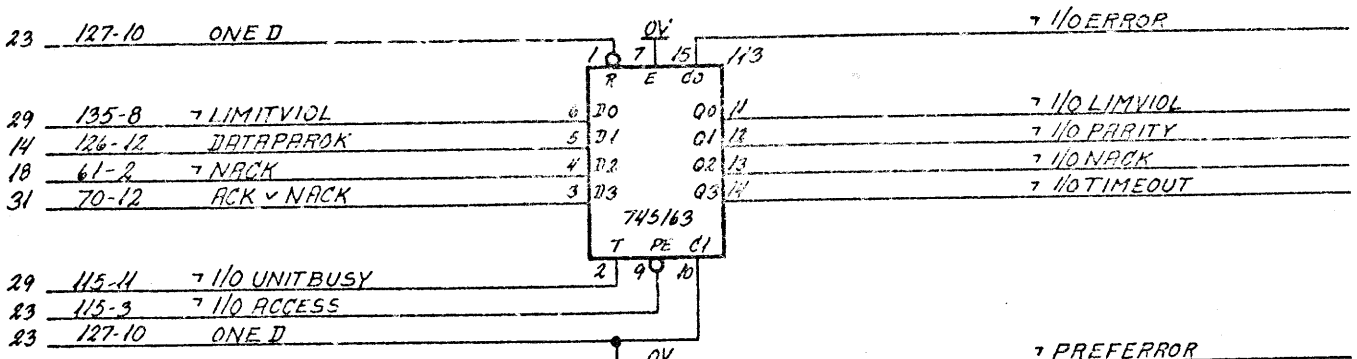
INTERRUPT CONTROL



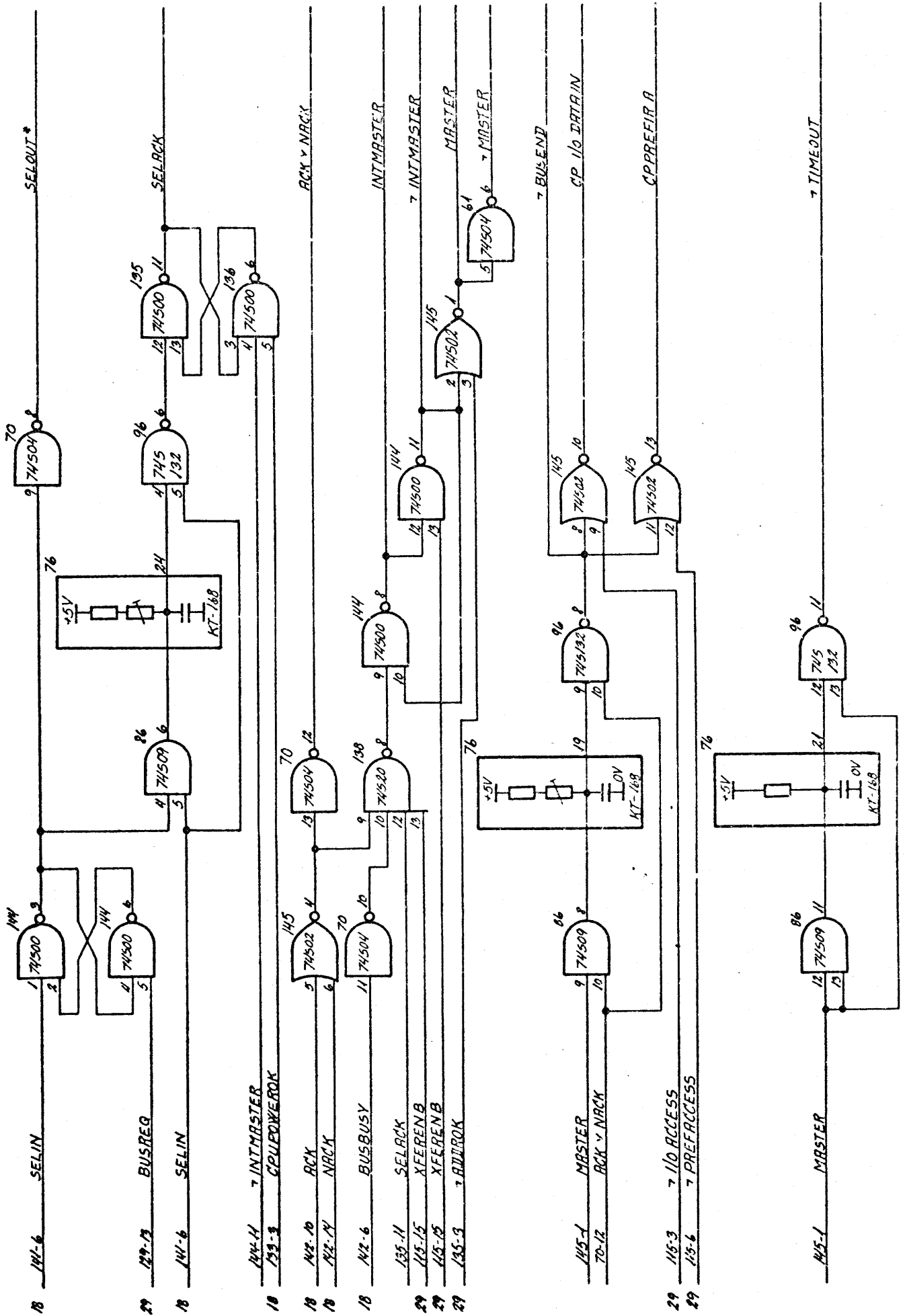
780410 R13 760V10 R03



760520 ARJ 760531 AOB



760322 RRT 760322 ROB



CPU803

R11467

BUS ACCESS CONTROL

A/S RE CENTRALEN

Designed by
76110 AAJ

Drawn by
76110 AOB

Dwg. Office

Design Check

Replaces Dwg. No.

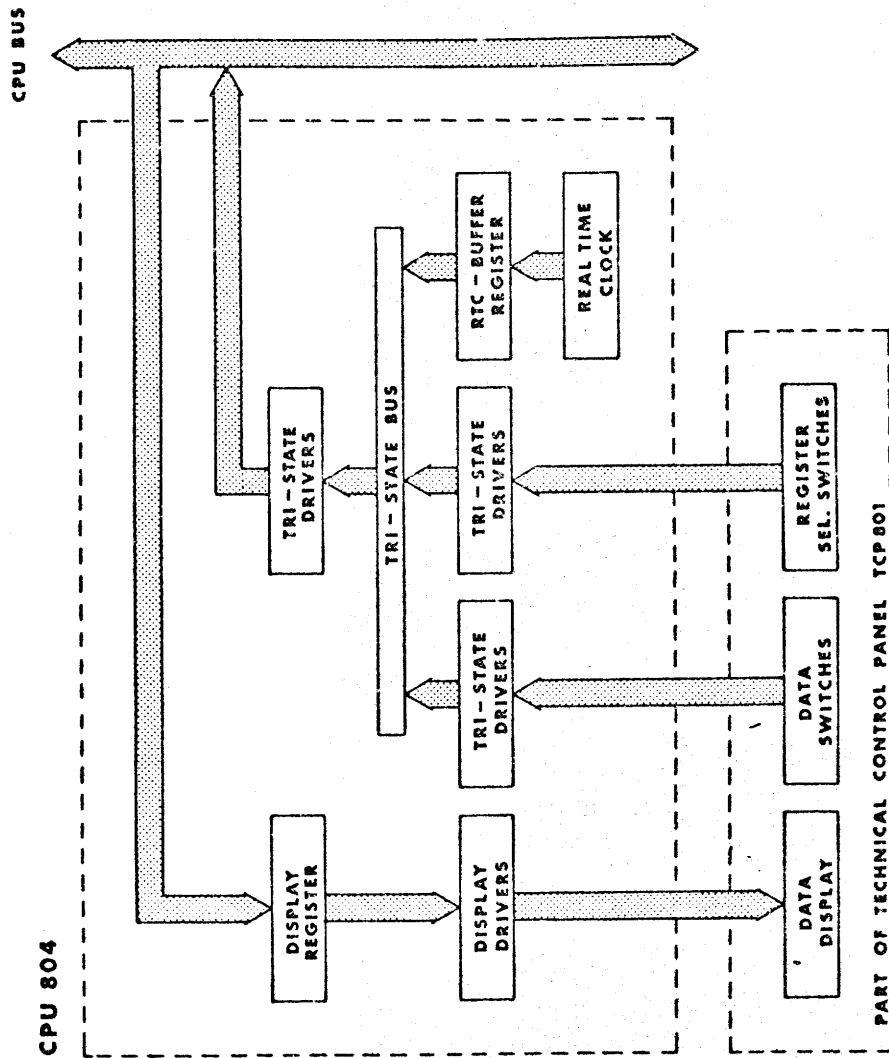
due to ECN

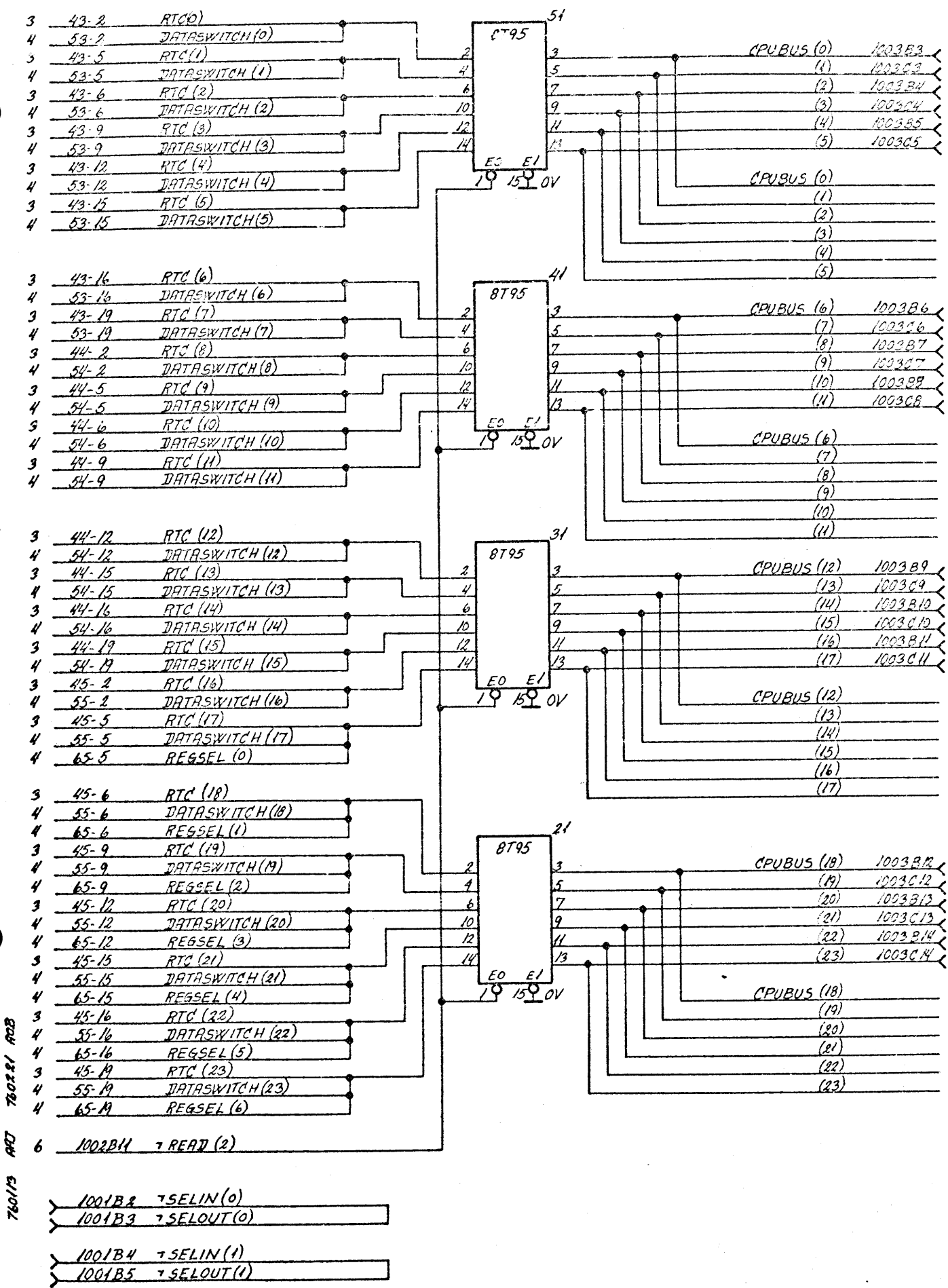
Replaces Dwg. No.

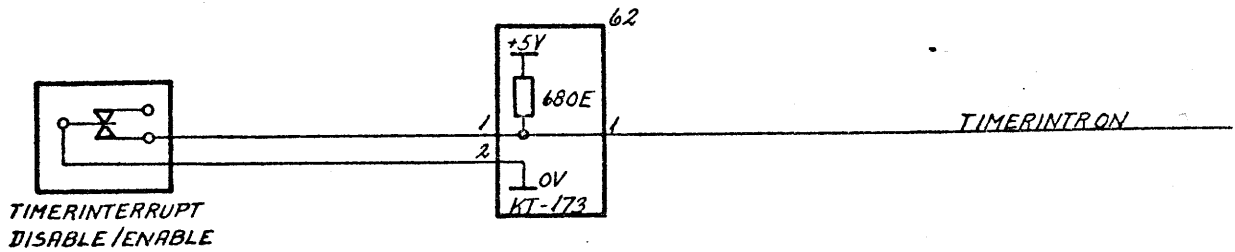
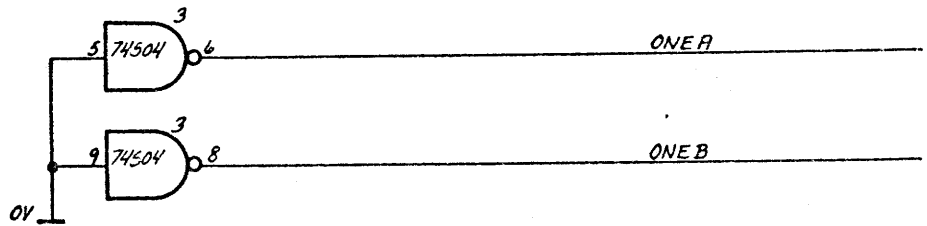
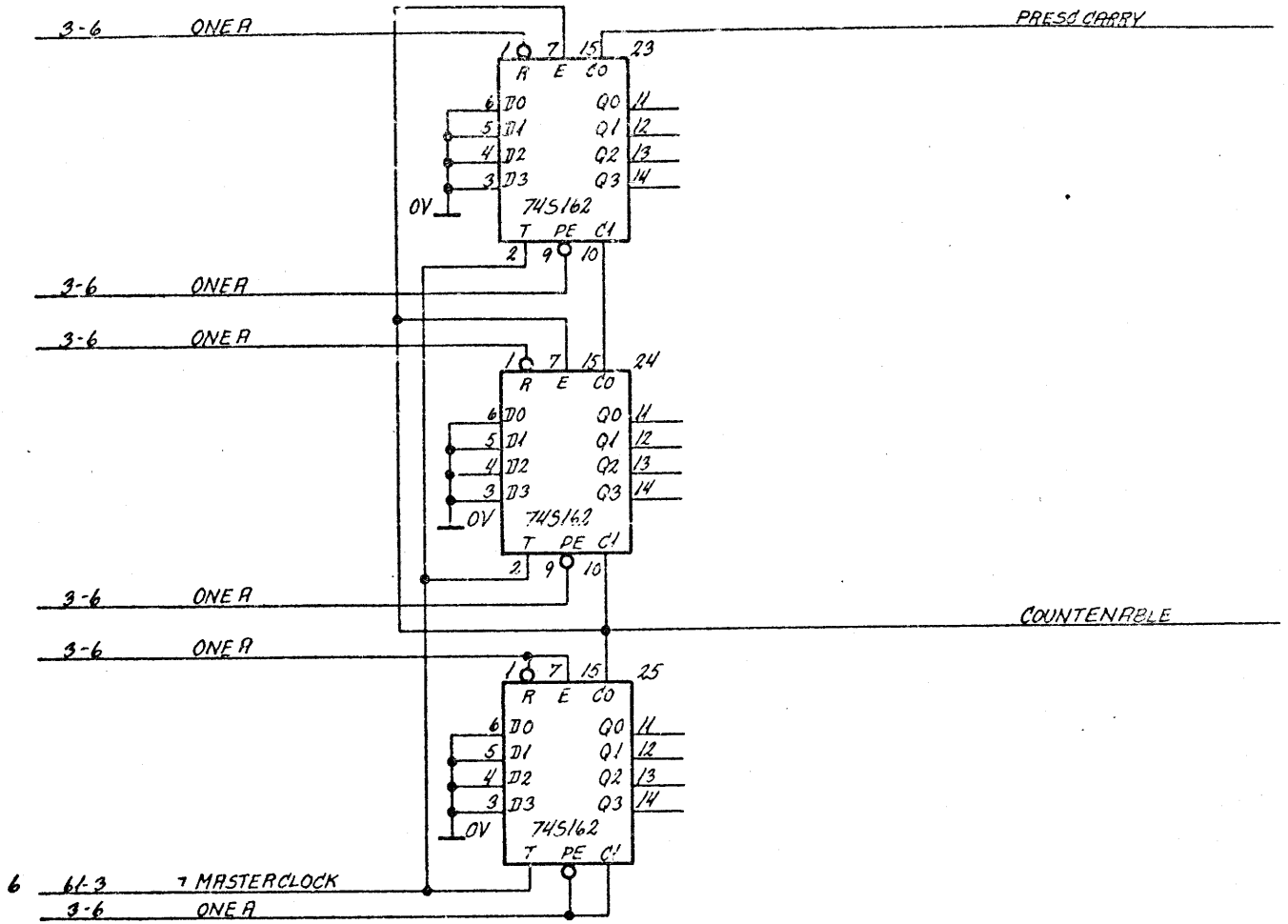
Unit
CPU 804

Dwg. No.
R11683

CPU 804 BLOCK DIAGRAM

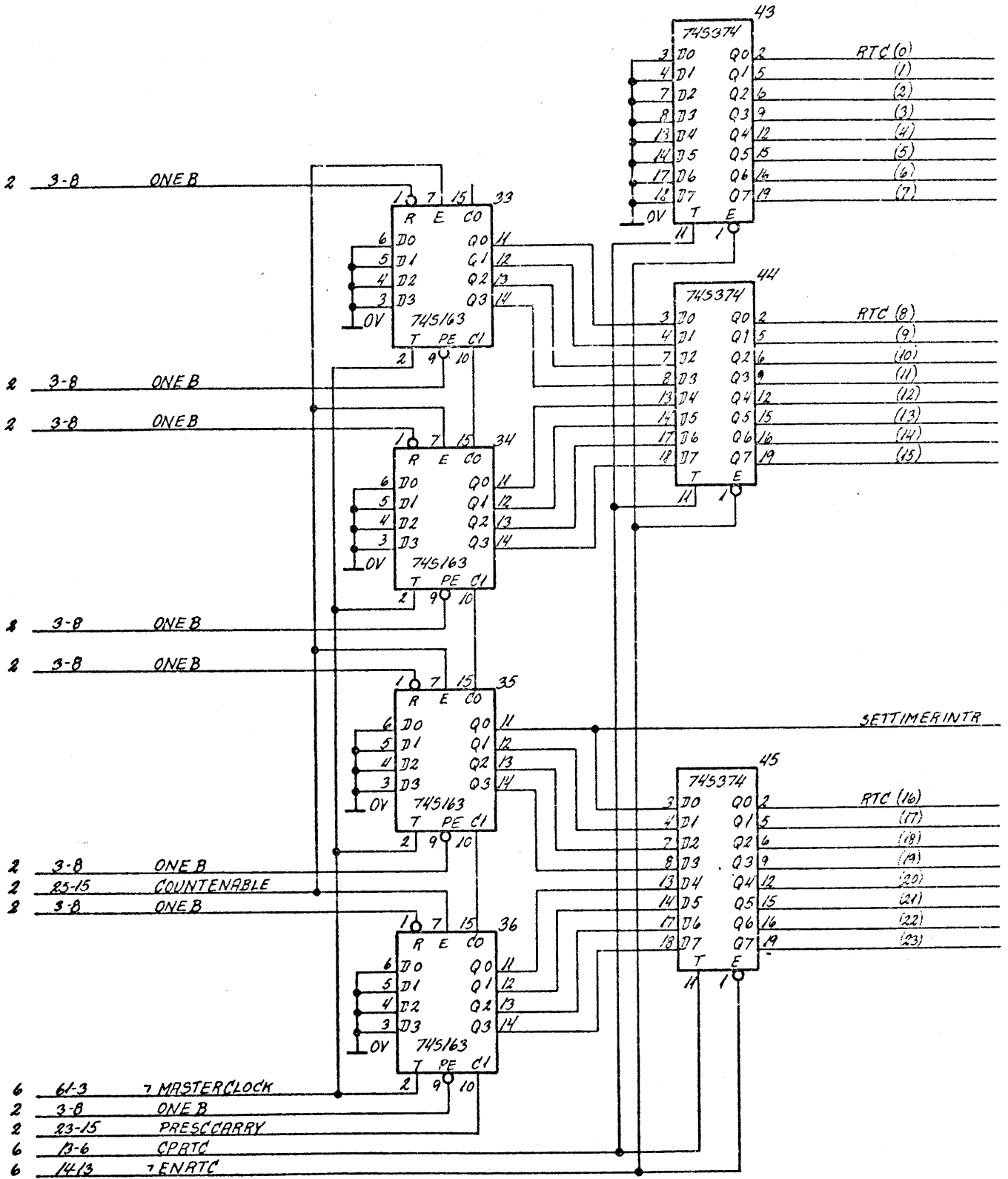


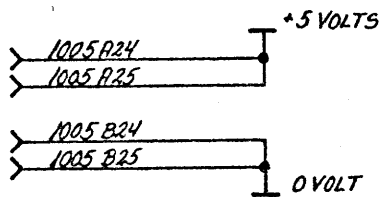
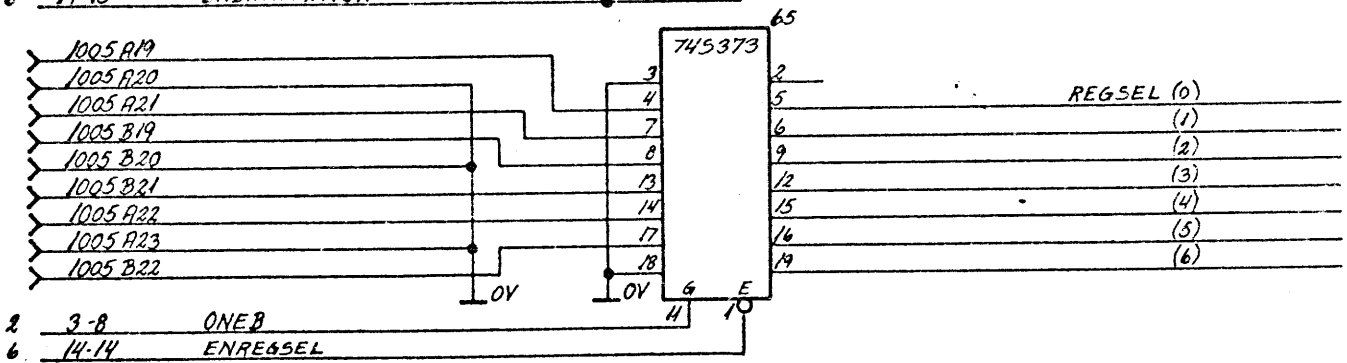
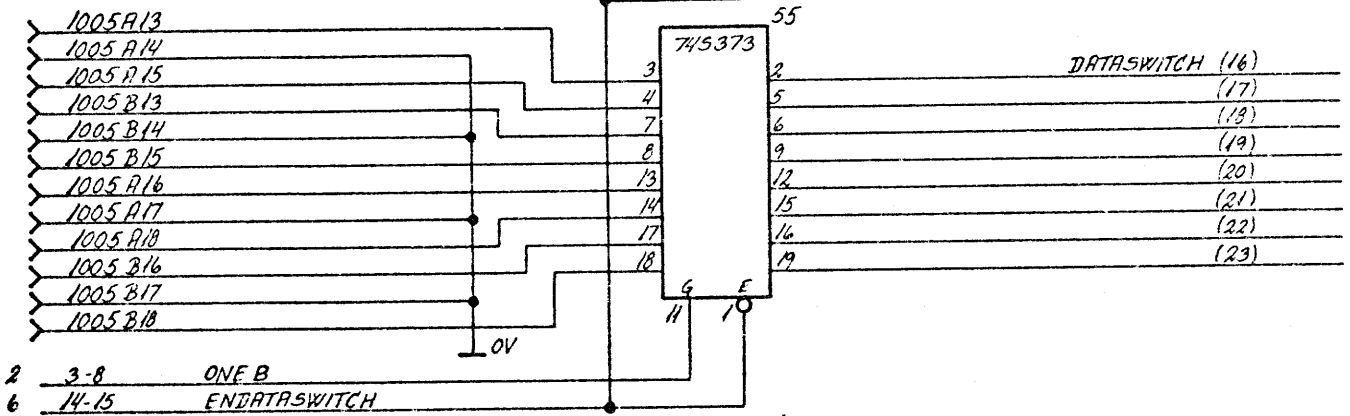
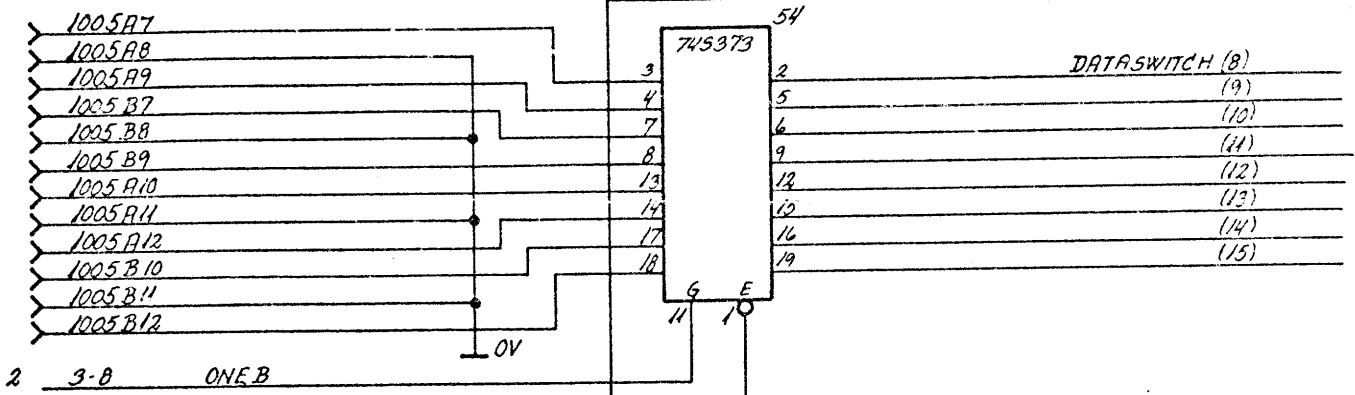
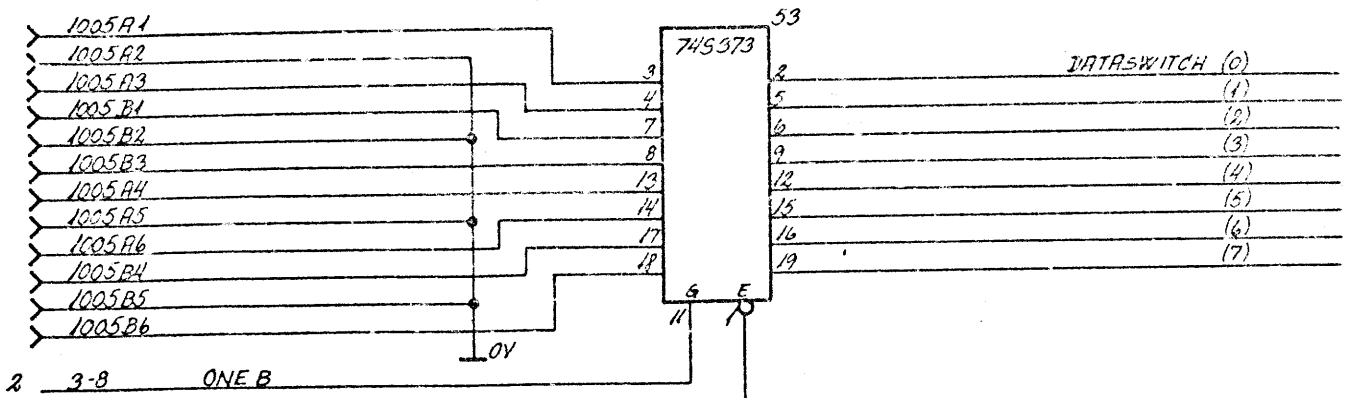




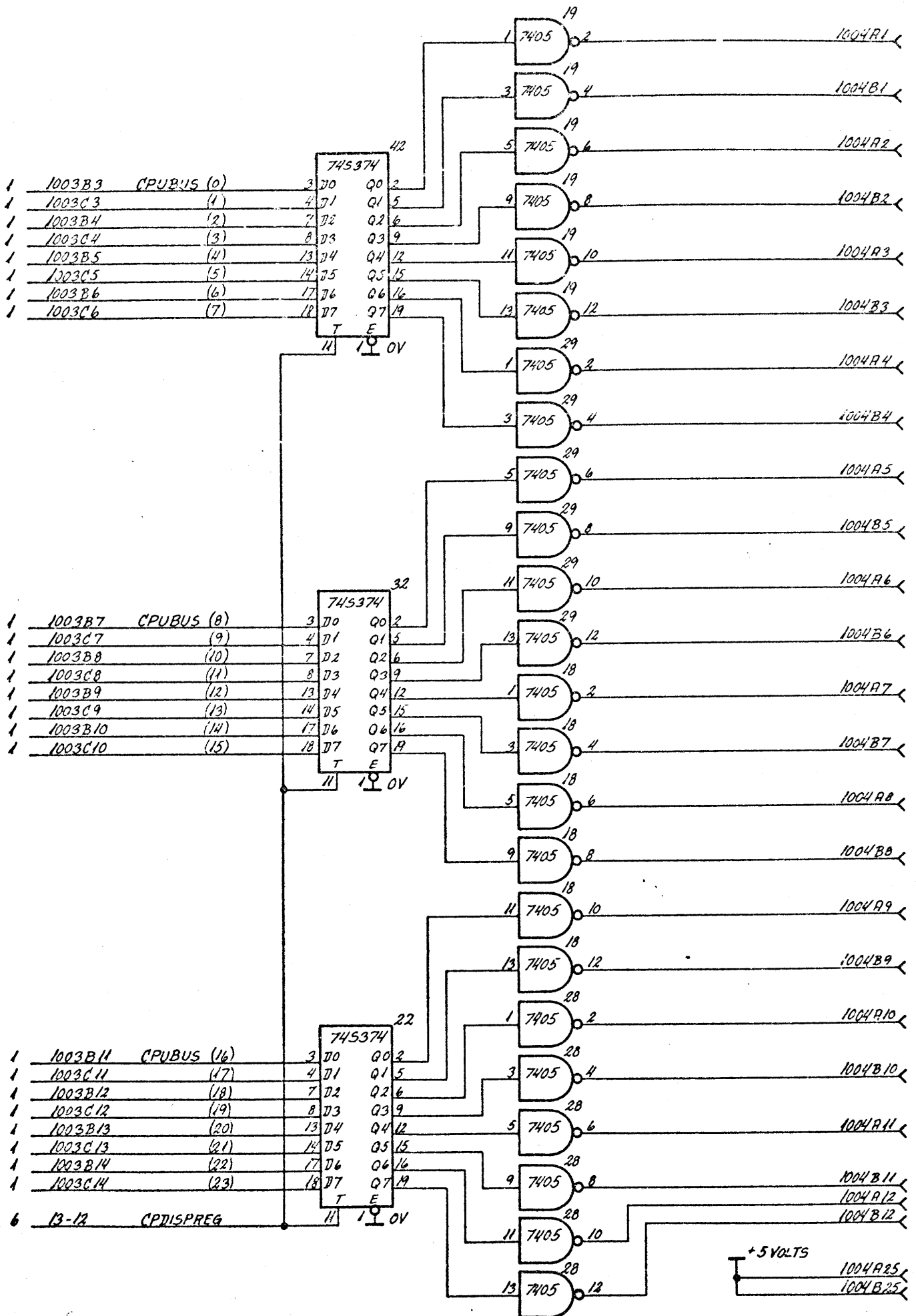
751126 RPS 76020 RO5

751126 RR7 740220 P08





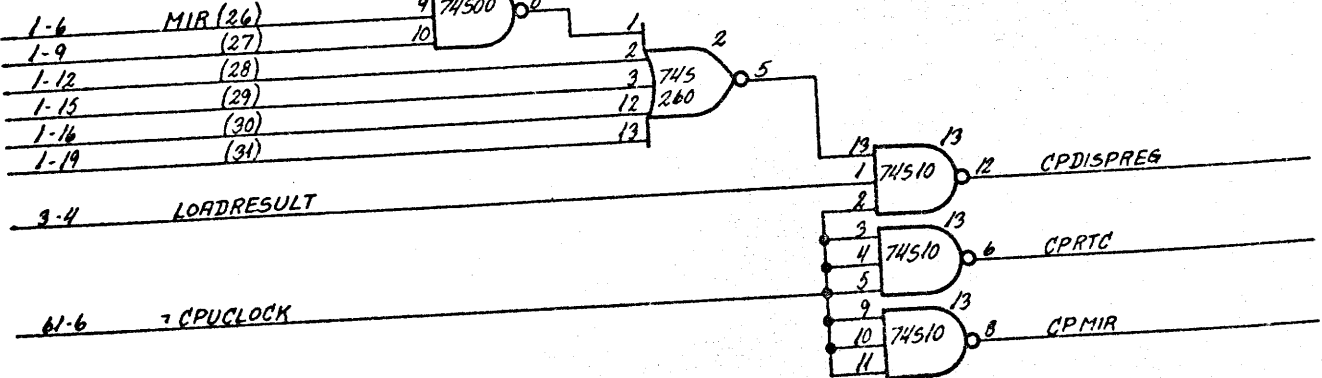
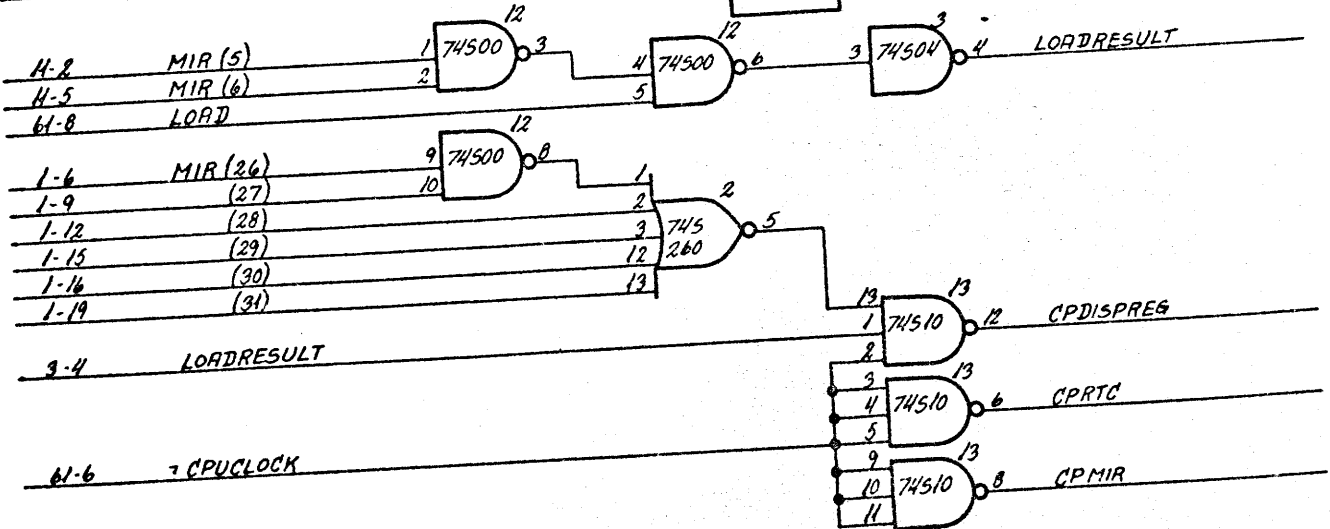
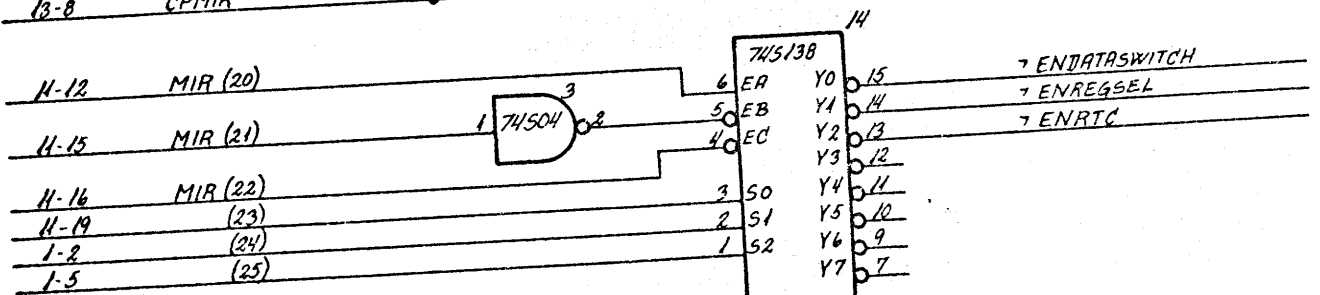
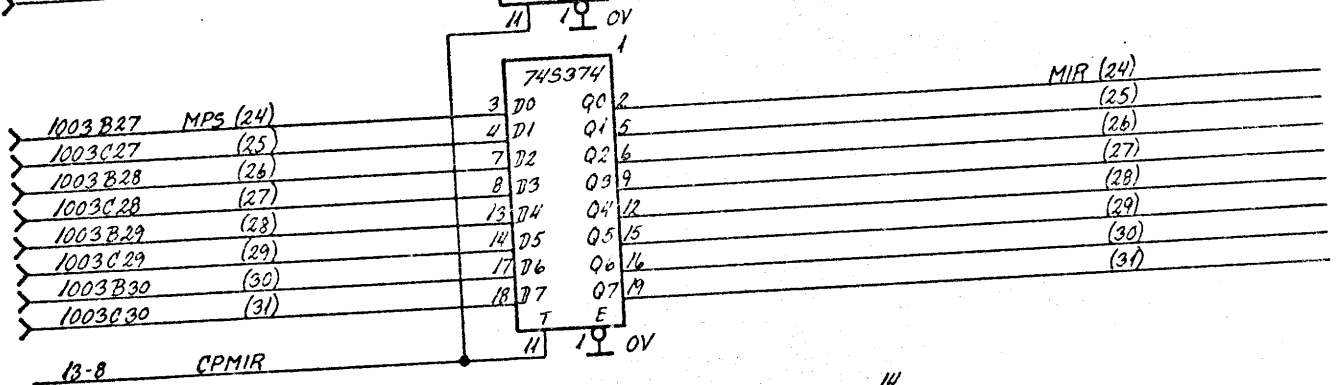
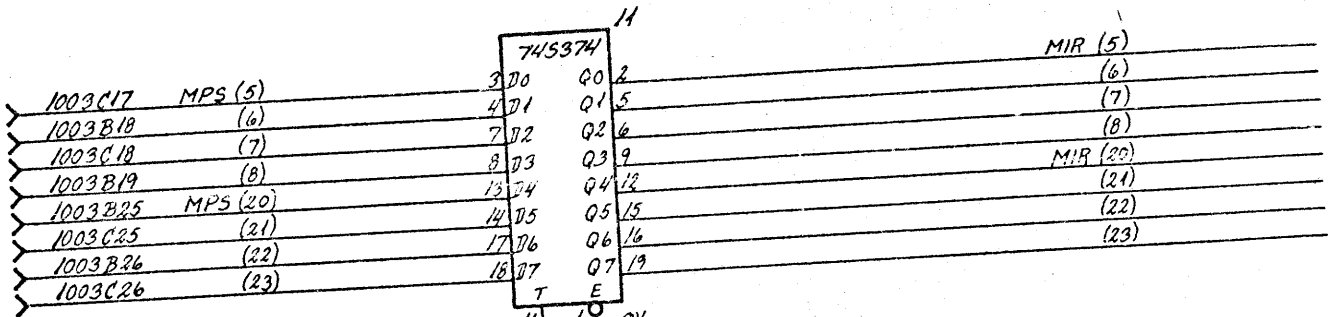
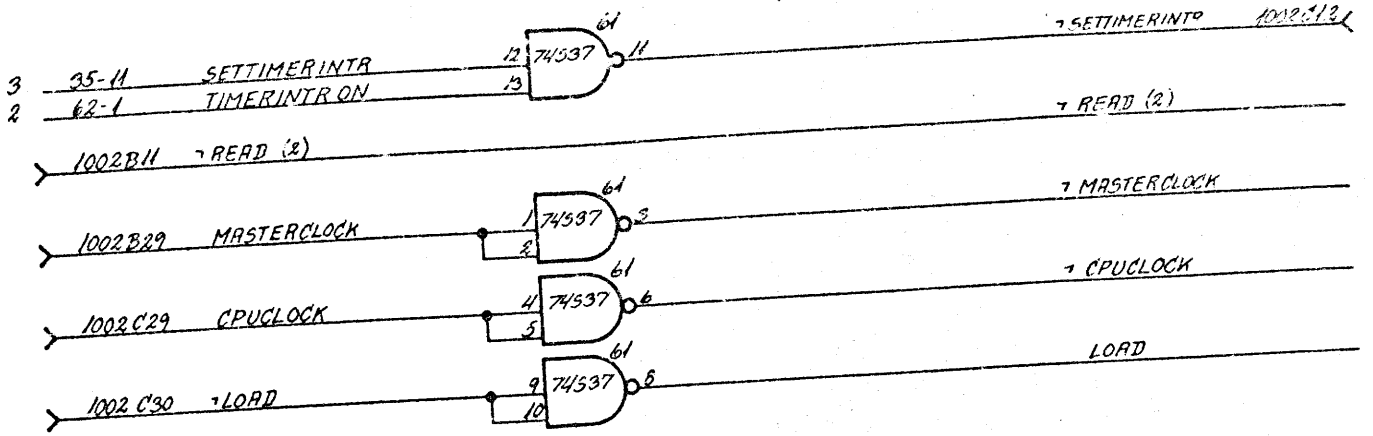
751211 AAJ 760220 AOB



751211 RAJ 760220 RO3

CPU 804
R11472

INTERFACE TO TECHNICAL CONTROL PANEL
DISPLAY REGISTER AND LAMP DRIVERS



760119 ARJ 760220 A08