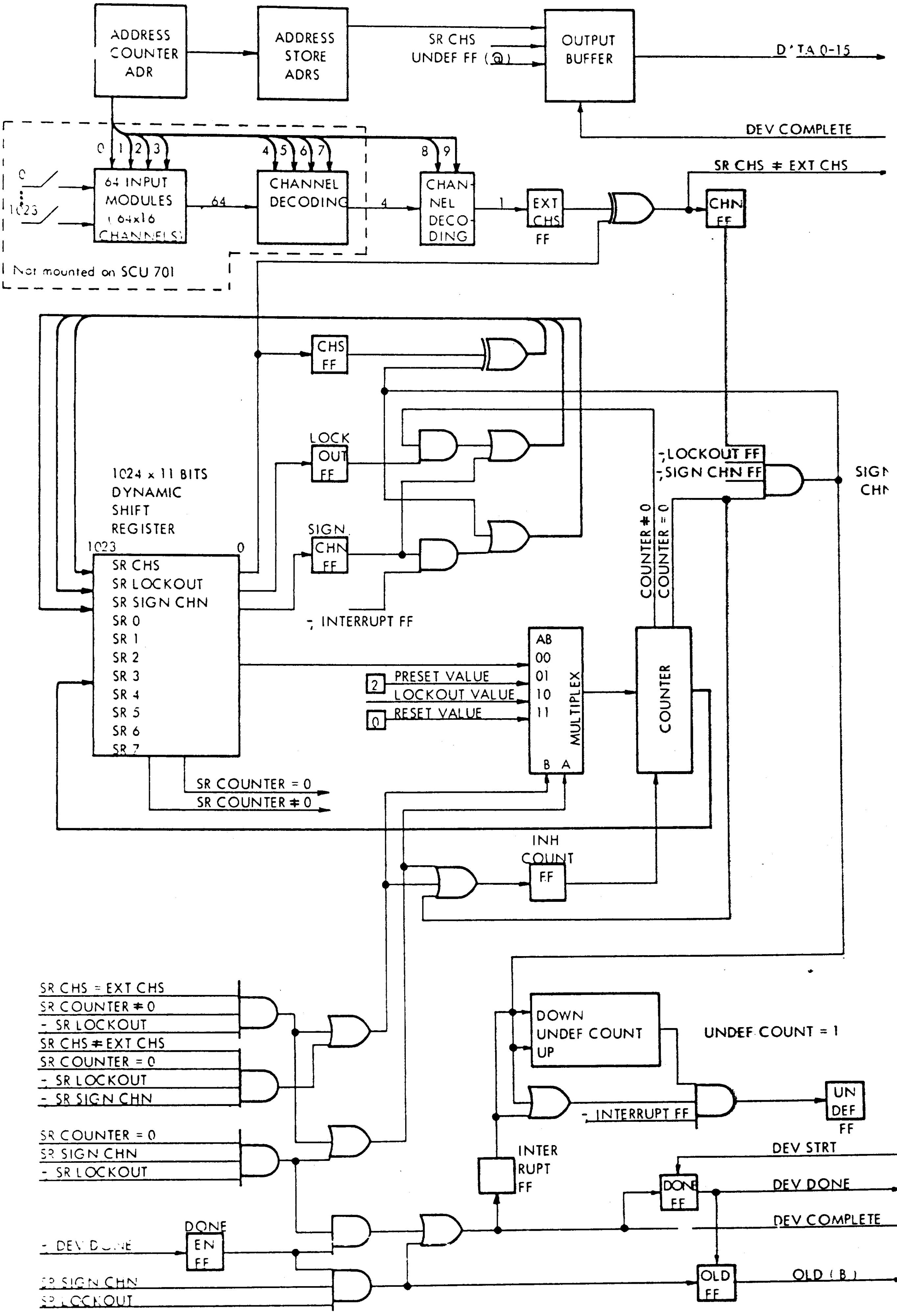
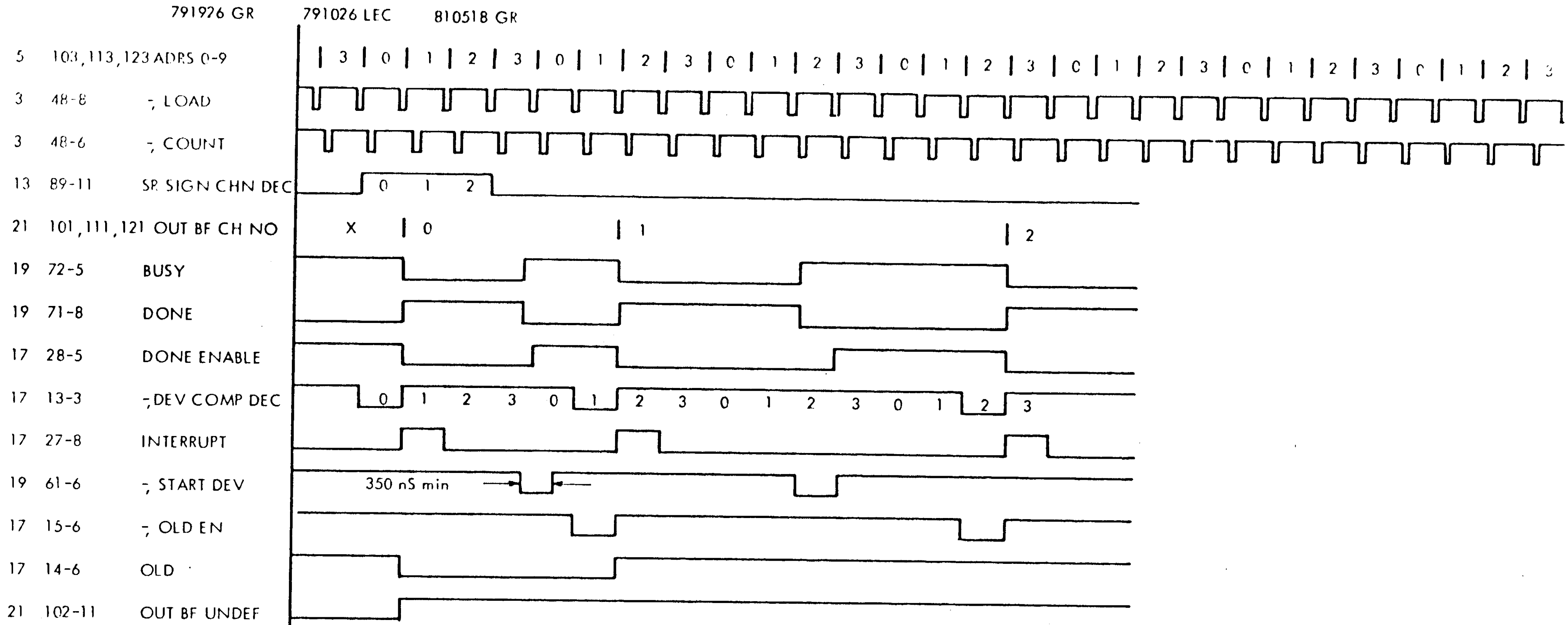


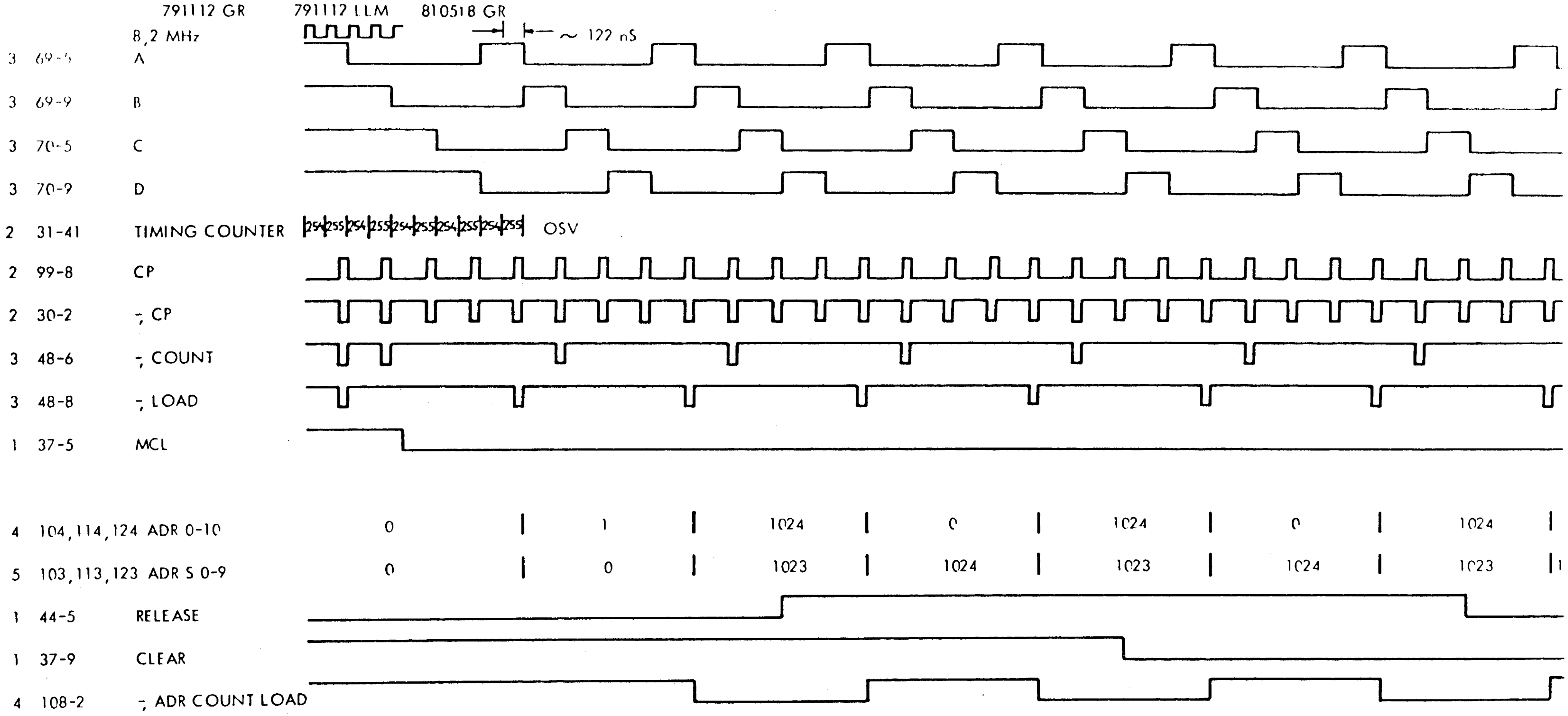
791113 GR 791113 LLM 810518 GR



SCU 701

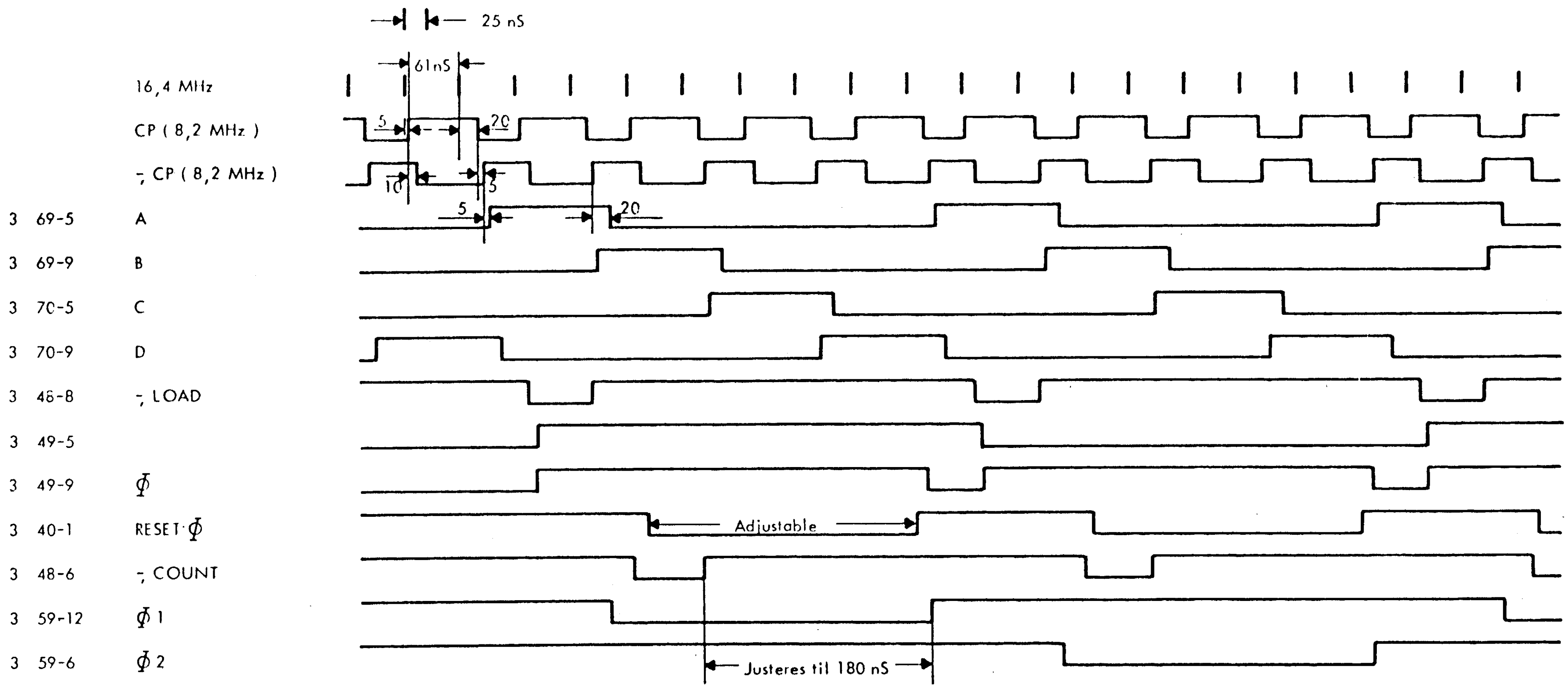
A 13797

Timing Chart



Timing Chart

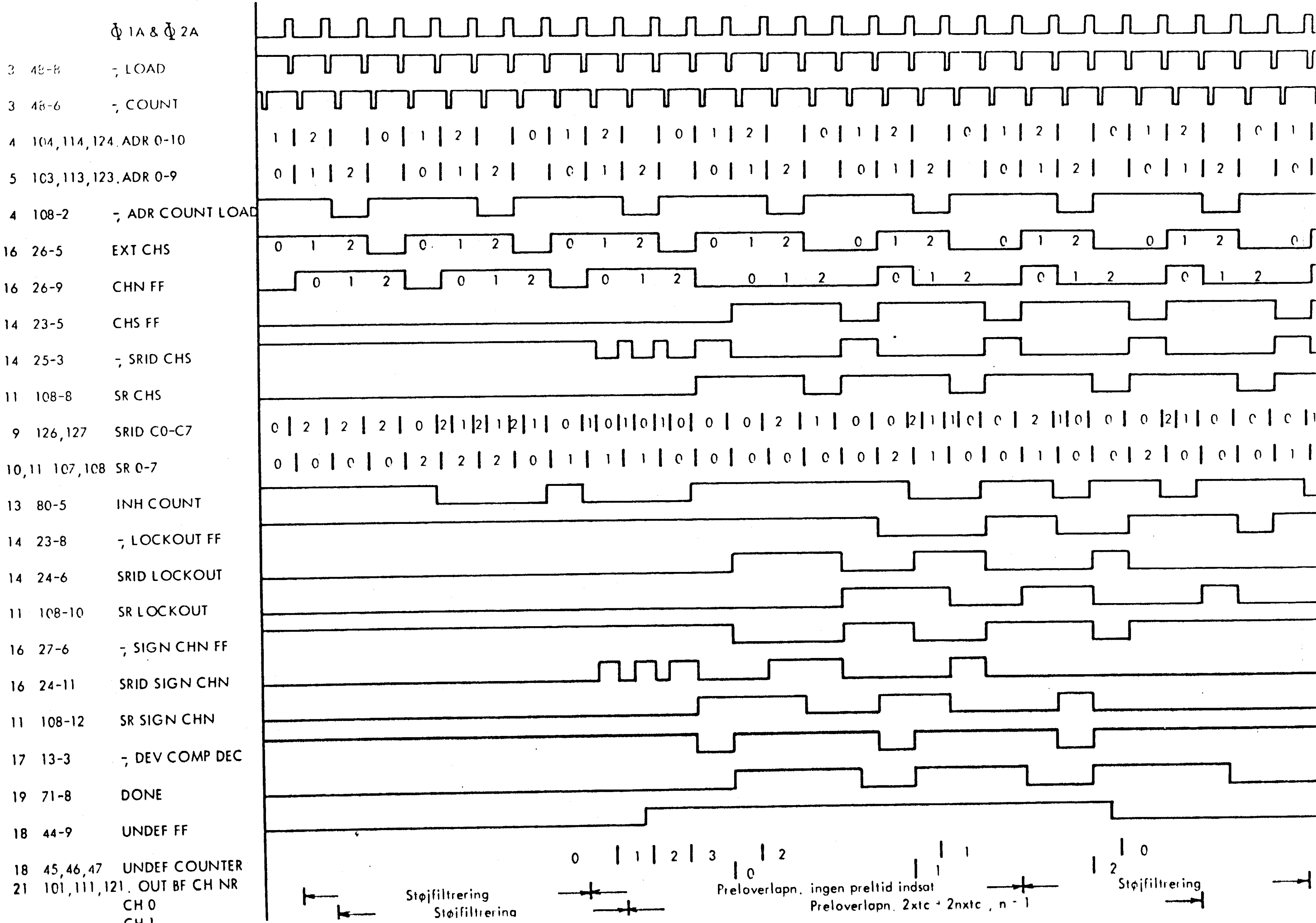
791113 GR 791113 LLM 810518 GR



SCU 701

A 13800

791112 GR 791112 LLM 810518 GR

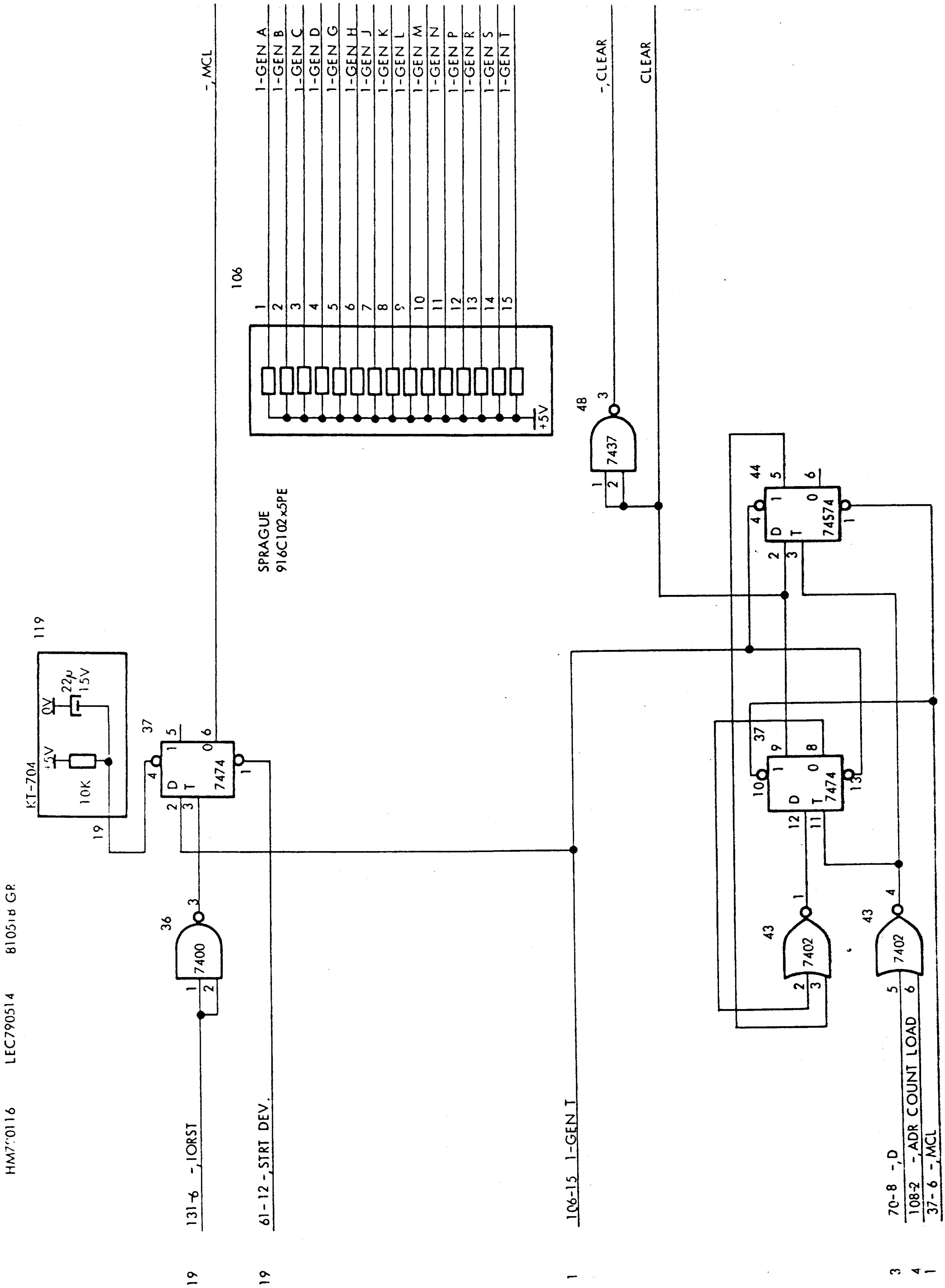


Timing Chart

TC 4

SIGNAL	DESTINATION	DESCRIPTION
CLEAR	p17	CLEAR pulse
₇ CLEAR	p13, p14, p16, p17, p18	₇ CLEAR pulse
₇ MCL	p1, p4, p15	₇ Master CLear
1 - GEN A		
1 - GEN B		
1 - GEN C		
1 - GEN D		
1 - GEN G		
1 - GEN H		
1 - GEN J		
1 - GEN K	p15, p18 p21	
1 - GEN L	p17	
1 - GEN M	p9, p13 p14, p16	
1 - GEN N	p4, p5	
1 - GEN P	p2	
1 - GEN R	p3	
1 - GEN S	p3	
1 - GEN T	p1	

Designed by 801110 GR
Drawn by 801110AMS
Dwg.
Check



SCU701

A 13774

START CIRCUITS

Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
CP	p3, p18	Clock Pulse CP $\leq$ 8,2 MHz.
¬ CP	p3	¬ Clock Pulse

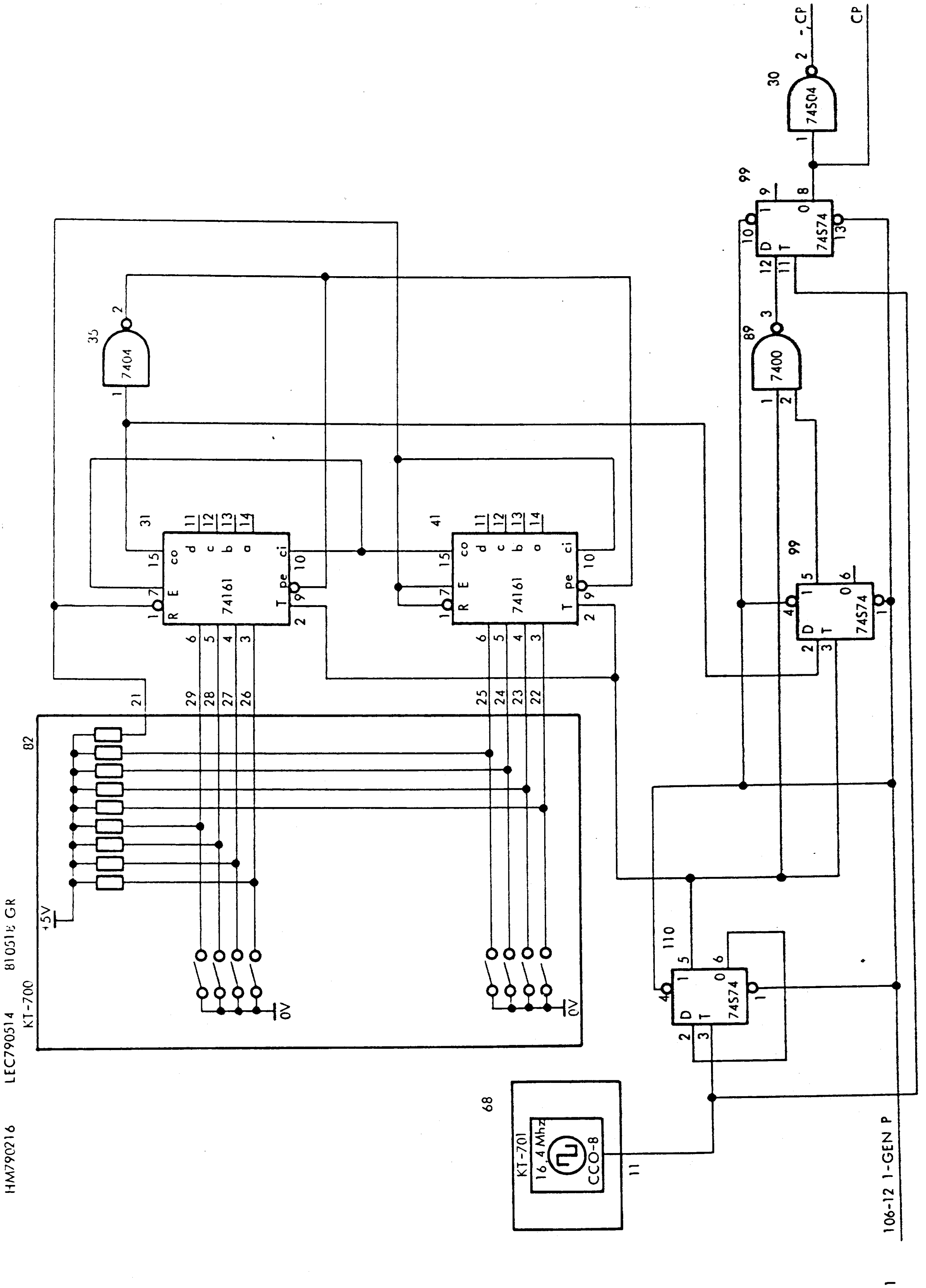
Designed by 801110 GR

Drawn by 801110 AMS

Dwg.

Check

Unit		
SCU 701		p2
Dwg. No. A25729	Signal List	



HM790216
LEC790514
KT-700
81051E GR
+5V
0V
7404
74161
74161
74S04
74S74
7400
74S74
74S74
KT-701
16.4 Mhz
CCO-8
106-12 1-GEN P
-CP
CP

SIGNAL	DESTINATION	DESCRIPTION
AØ1	p12, p15	APhase 1
AØ2	p12, p15	APhase 2
BØ1	p12	BPhase 1
BØ2	p12	BPhase 2
⁊ COUNT	p9	⁊ Count pulse
D	p18	4.th slep
⁊ D	p1	
LOAD	p13	LOAD pulse
⁊ LOAD	p4, p5 p9, p14 p15, p16 p17, p19 p21	⁊ LOAD pulse
A		1st slep
B		2d slep
C		3d slep

Designed by 801110 GR

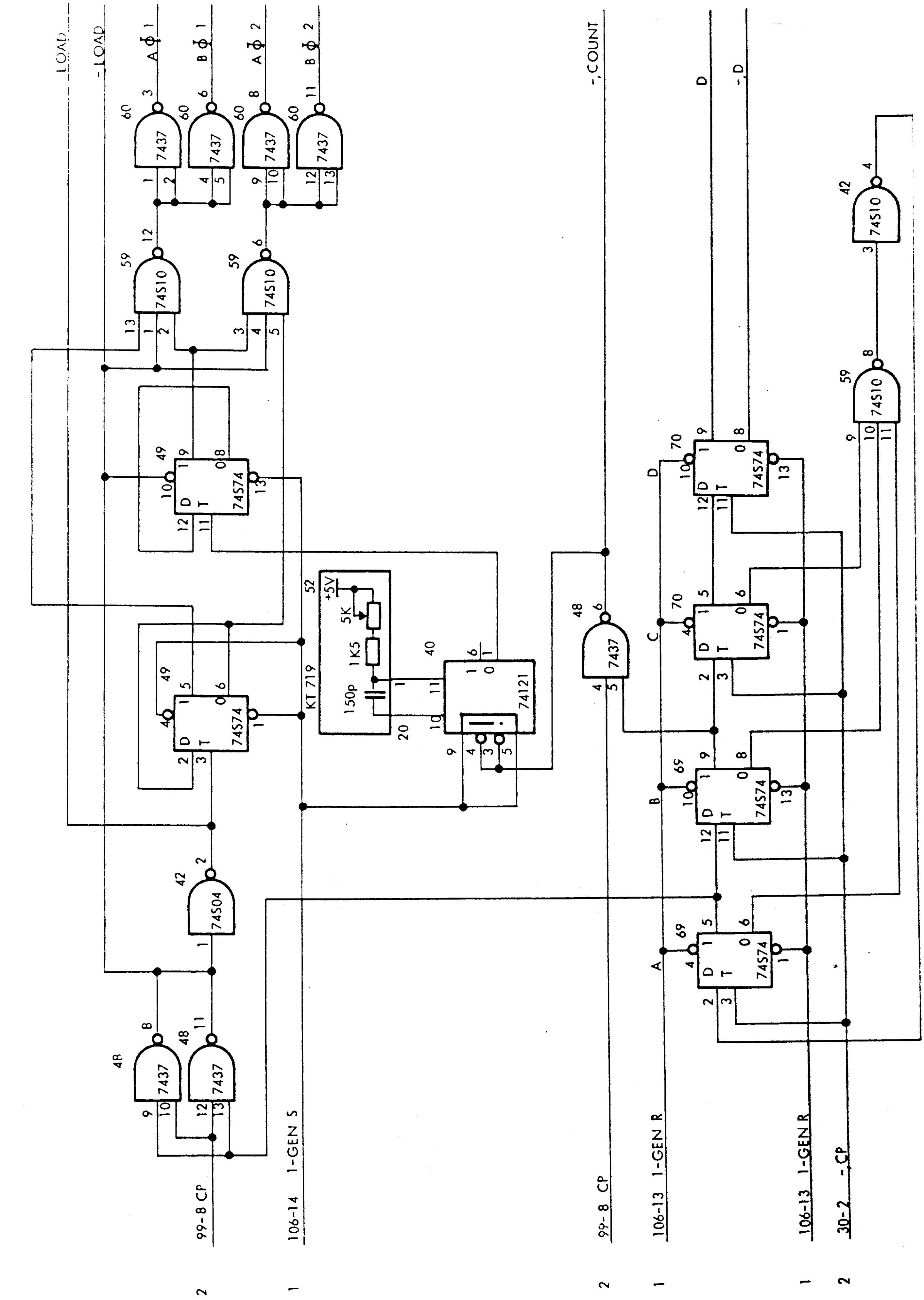
Drawn by 801110 AMS

Dwg

Check

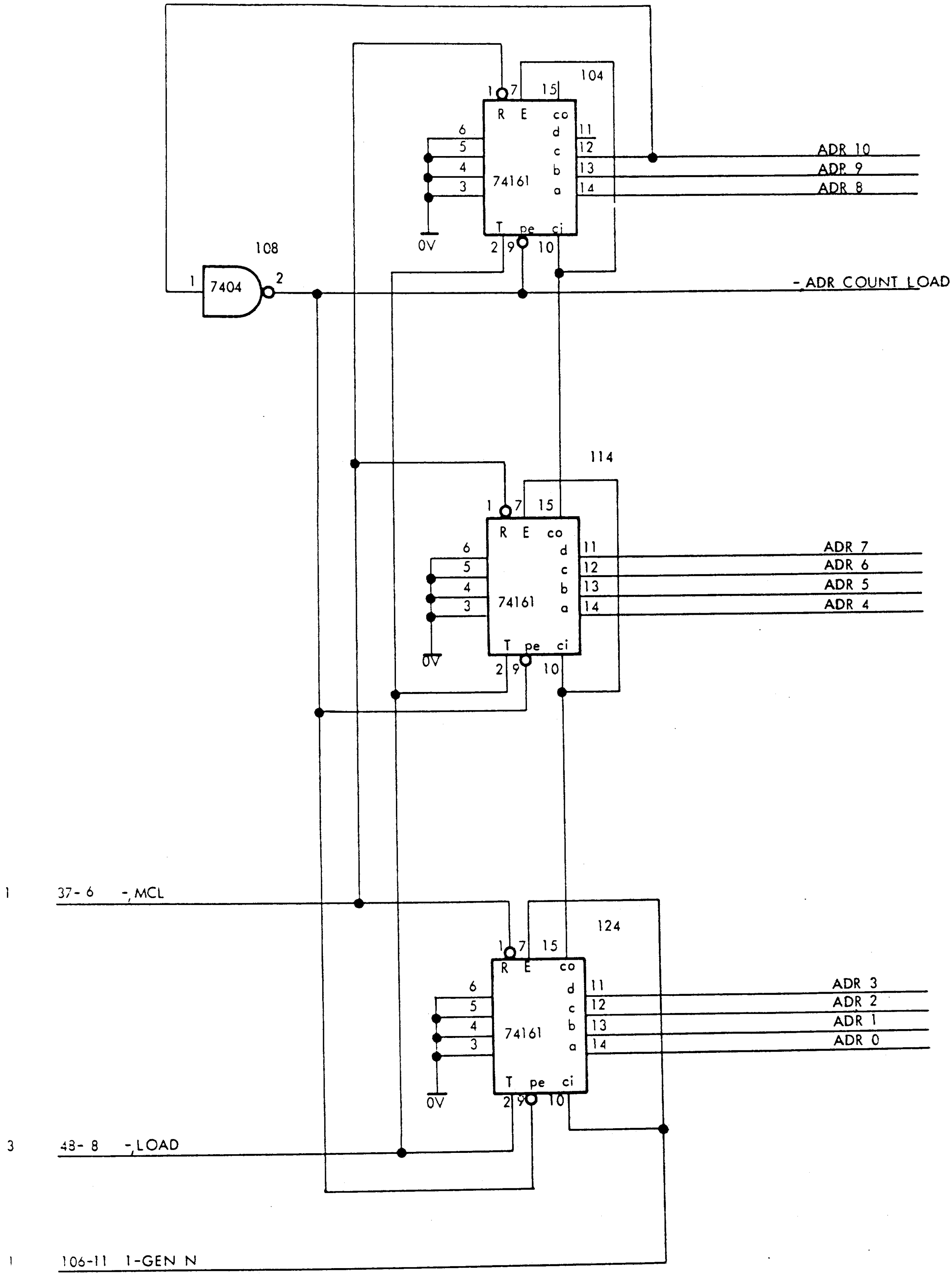
Unit SCU 701		p3
Dwg. No. A25730	Signal List	

HM790216 LEC790510 Rev 79..13 LLM 810518 GR



SIGNAL	DESTINATION	DESCRIPTION
ADR 0 - ADR 3	p5,p6, p7	ADdRess counter bit 0 - bit 10
ADR 4 - ADR 7	p5, p6 p7, p15	
ADR 8 - ADR 9	p5, p15	
ADR 10	p15	
¬ADR COUNT LOAD	p1, p15	¬ADdRess counter load pulse

Designed by 801110 GR
Drawn by 801110 AMS
Dwg
Check



H105 GR

LEC790510

HM790219

SIGNAL	DESTINATION	DESCRIPTION
ADRS 0 - 9	p21	store register for addresses 0 - 9

Designed by 801110 GR

Drawn by 801110 AMS

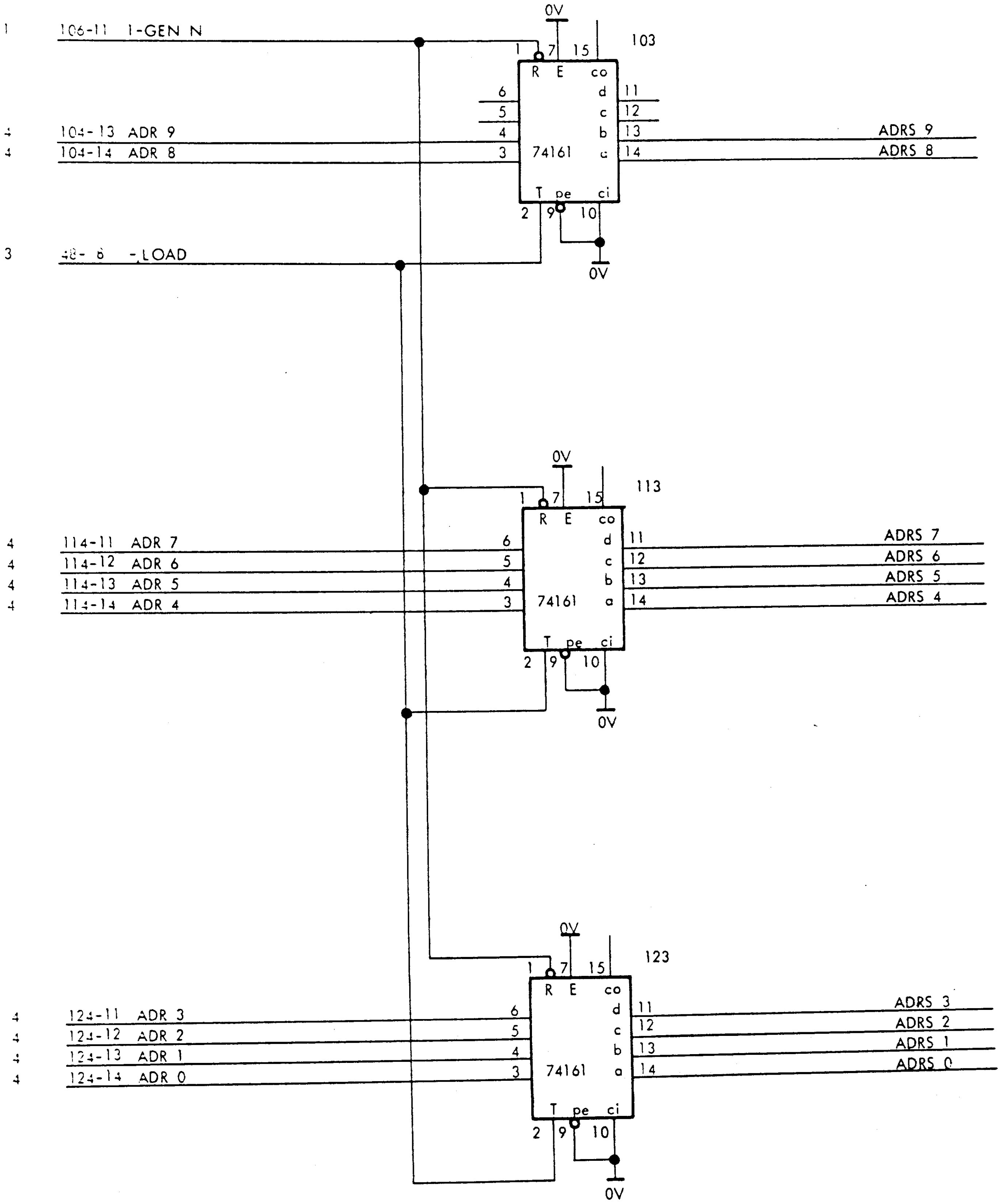
Dwg

Check

Unit SCU 701

Dwg. No. A25732

Signal List



810518 GR

LEC790509

HM790219

p.5

SCU701

ADRS REGISTER PART 2

A 13775

Circuit Diagram

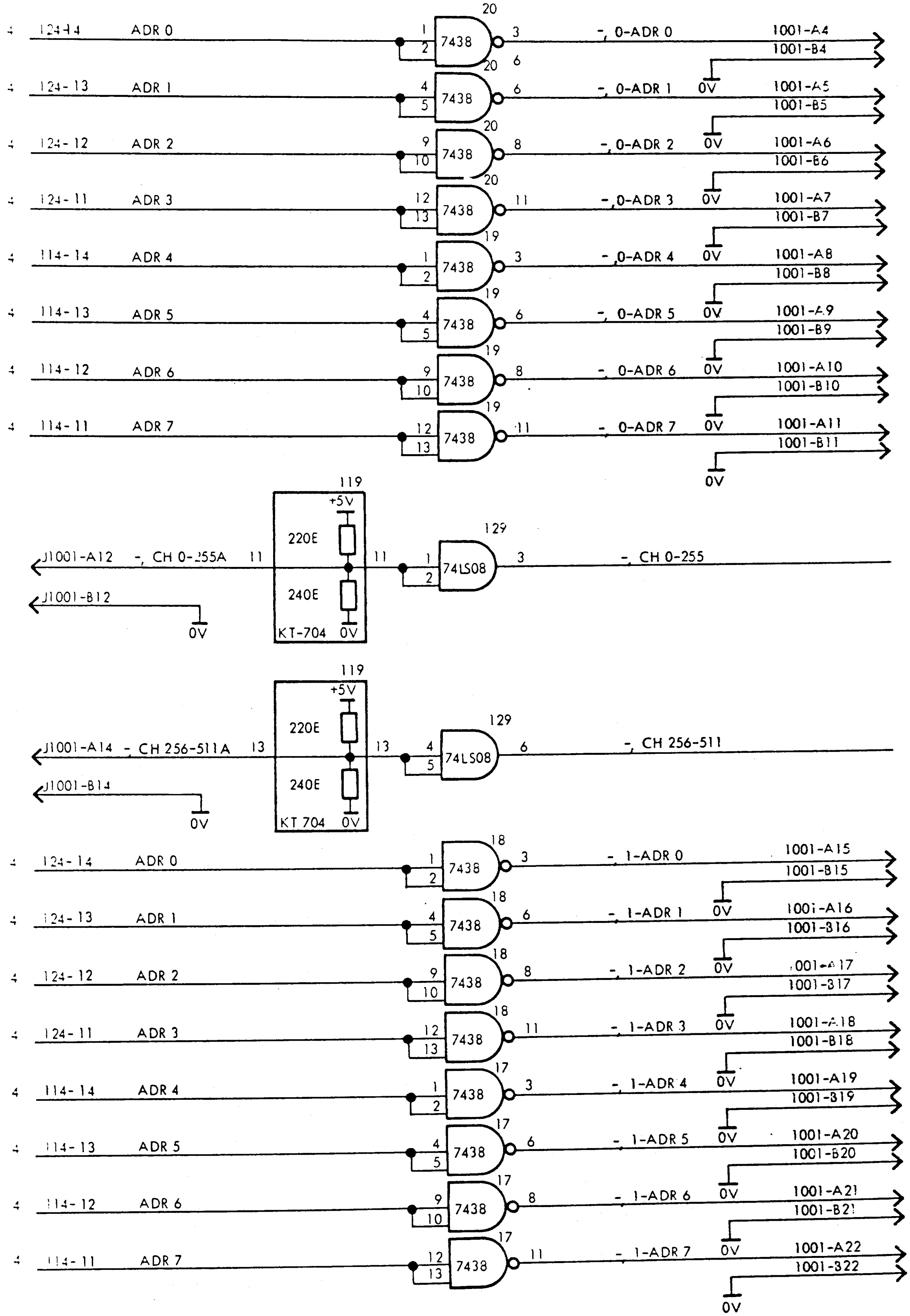
SIGNAL	DESTINATION	DESCRIPTION
¬CH 0 - 255	p15	¬CHannel 0 - 255
¬CH 256 - 511	p15	¬CHannel 256 - 511
¬CH 0 - 255 A	PLUG 1001	¬CHannel 0.- 255
¬CH 256 - 511	PLUG 1001	¬CHannel 256 - 511
¬0-ADR 0 - ¬0-ADR 7	PLUG 1001	¬ADdRess 0 - 7 for the channels 0 - 255
¬1-ADR 0 - ¬1-ADR 7	PLUG 1001	¬ADdRess 0 - 7 for the channels 256 - 511

Designed by 801110 GR
Drawn by 801110 AMS
Dwg. ...e Check

Unit SCU 701

Dwg. No. A25733

Signal List



790219 HM 790502 LEC 810518 GR

SCU 701

ADDRESS DRIVERS LEVEL 0 - 1

Circuit Diagram

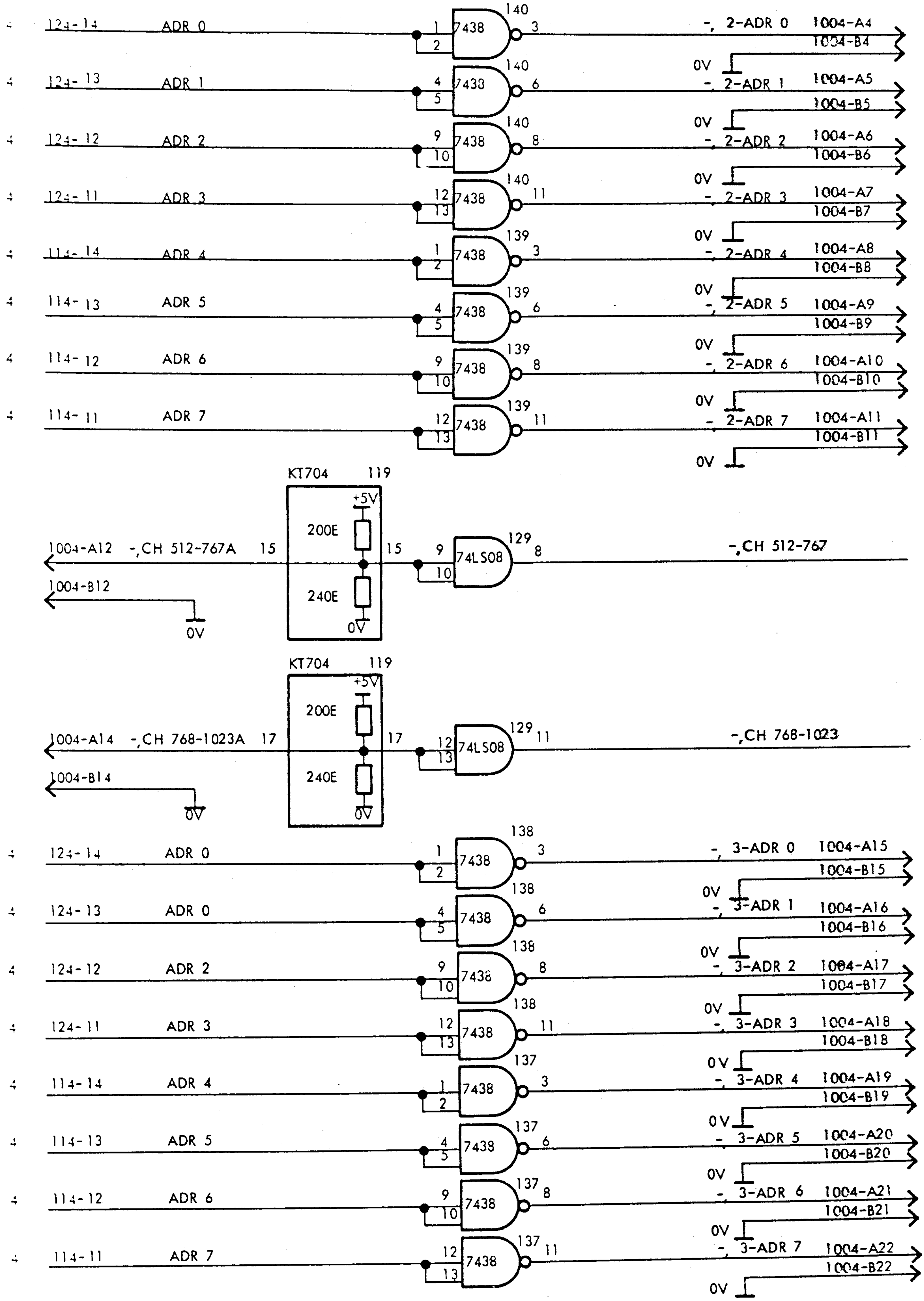
A13779

SIGNAL	DESTINATION	DESCRIPTION
¬ CH 512 - 767	p15	¬ CHannel 512 - 767
¬ CH 768 - 1023	p15	¬ CHannel 768 - 1023
¬ CH 512 - 767 A	PLUG 1004	¬ CHannel 512 - 767
¬ CH 768 - 1023 A	PLUG 1004	¬ CHannel 768 - 1023
¬ 2 - ADR 0 - ¬ 2-ADR 7	PLUG 1004	¬ ADRess 0 - 7 for the channels 512 - 767
¬ 3 - ADR 0 - ¬ 3-ADR 7	PLUG 1004	¬ ADRess 0 - 7 for the channels 768 - 1023

Designed by 801110 GR

Drawn by 801110 AMS

Dwg ... Check


124-14 ADR 0
124-13 ADR 1
124-12 ADR 2
124-11 ADR 3
114-14 ADR 4
114-13 ADR 5
114-12 ADR 6
114-11 ADR 7
7438
140
139
-, 2-ADR 0 1004-A4 1004-B4
-, 2-ADR 1 1004-A5 1004-B5
-, 2-ADR 2 1004-A6 1004-B6
-, 2-ADR 3 1004-A7 1004-B7
-, 2-ADR 4 1004-A8 1004-B8
-, 2-ADR 5 1004-A9 1004-B9
-, 2-ADR 6 1004-A10 1004-B10
-, 2-ADR 7 1004-A11 1004-B11
0V
KT704 119
+5V
200E
240E
1004-A12 -,CH 512-767A 15
1004-B12
74LS08 129
-,CH 512-767
1004-A14 -,CH 768-1023A 17
1004-B14
-,CH 768-1023
124-14 ADR 0
124-13 ADR 0
124-12 ADR 2
124-11 ADR 3
114-14 ADR 4
114-13 ADR 5
114-12 ADR 6
114-11 ADR 7
138
137
-, 3-ADR 0 1004-A15 1004-B15
-, 3-ADR 1 1004-A16 1004-B16
-, 3-ADR 2 1004-A17 1004-B17
-, 3-ADR 3 1004-A18 1004-B18
-, 3-ADR 4 1004-A19 1004-B19
-, 3-ADR 5 1004-A20 1004-B20
-, 3-ADR 6 1004-A21 1004-B21
-, 3-ADR 7 1004-A22 1004-B22
HM 790219 LEC 790509 810518 GR

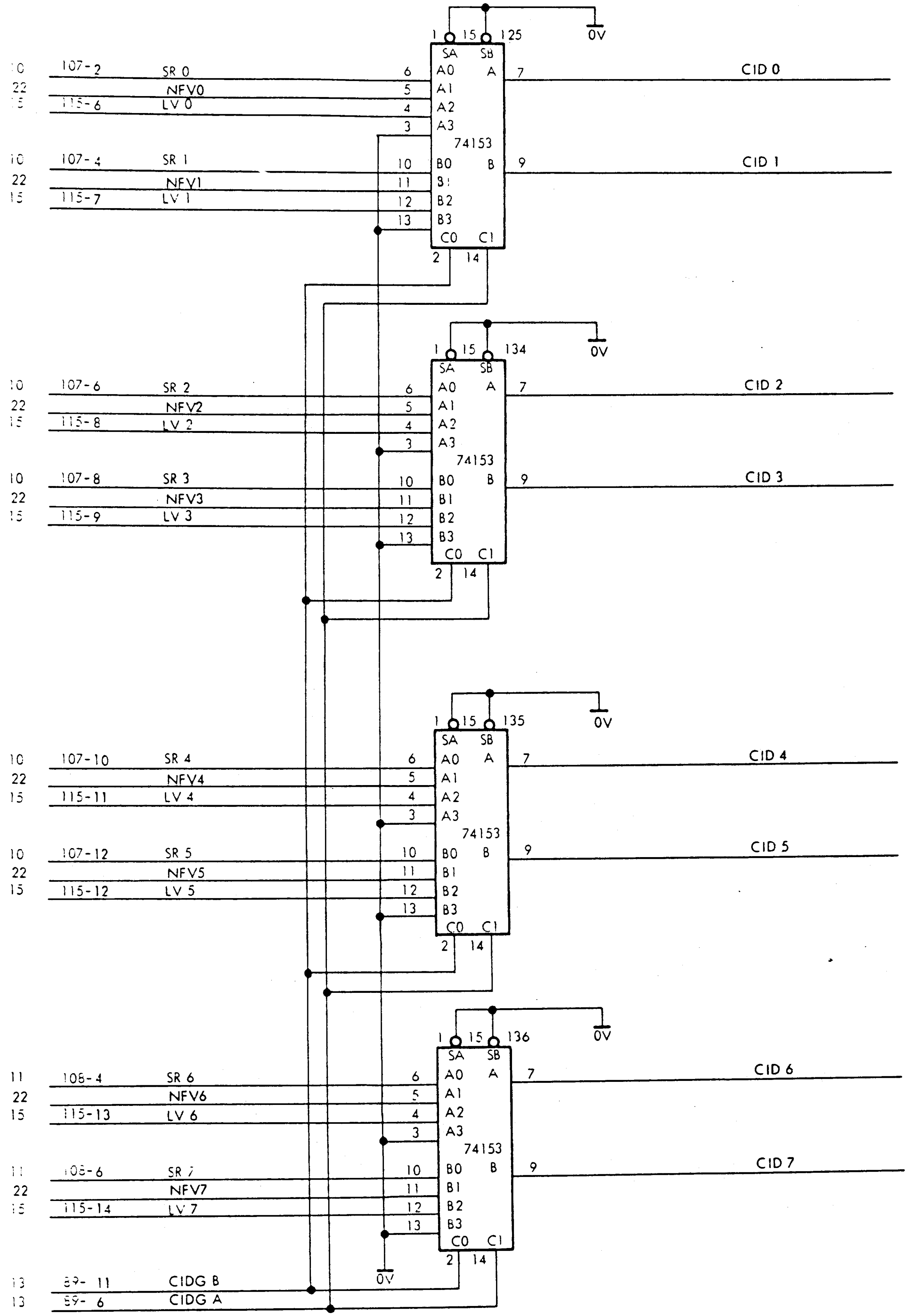
SIGNAL	DESTINATION	DESCRIPTION
CID 0 - CID 7	p9	Counter Input Data 0-7

Designed by 801110 GR

Drawn by 801110 AMS

Dwg ...e Check

Unit SCU 701		p8
Dwg. No. A25735	Signal List	



SCU 701

LOCKOUT COUNTER SELECTOR

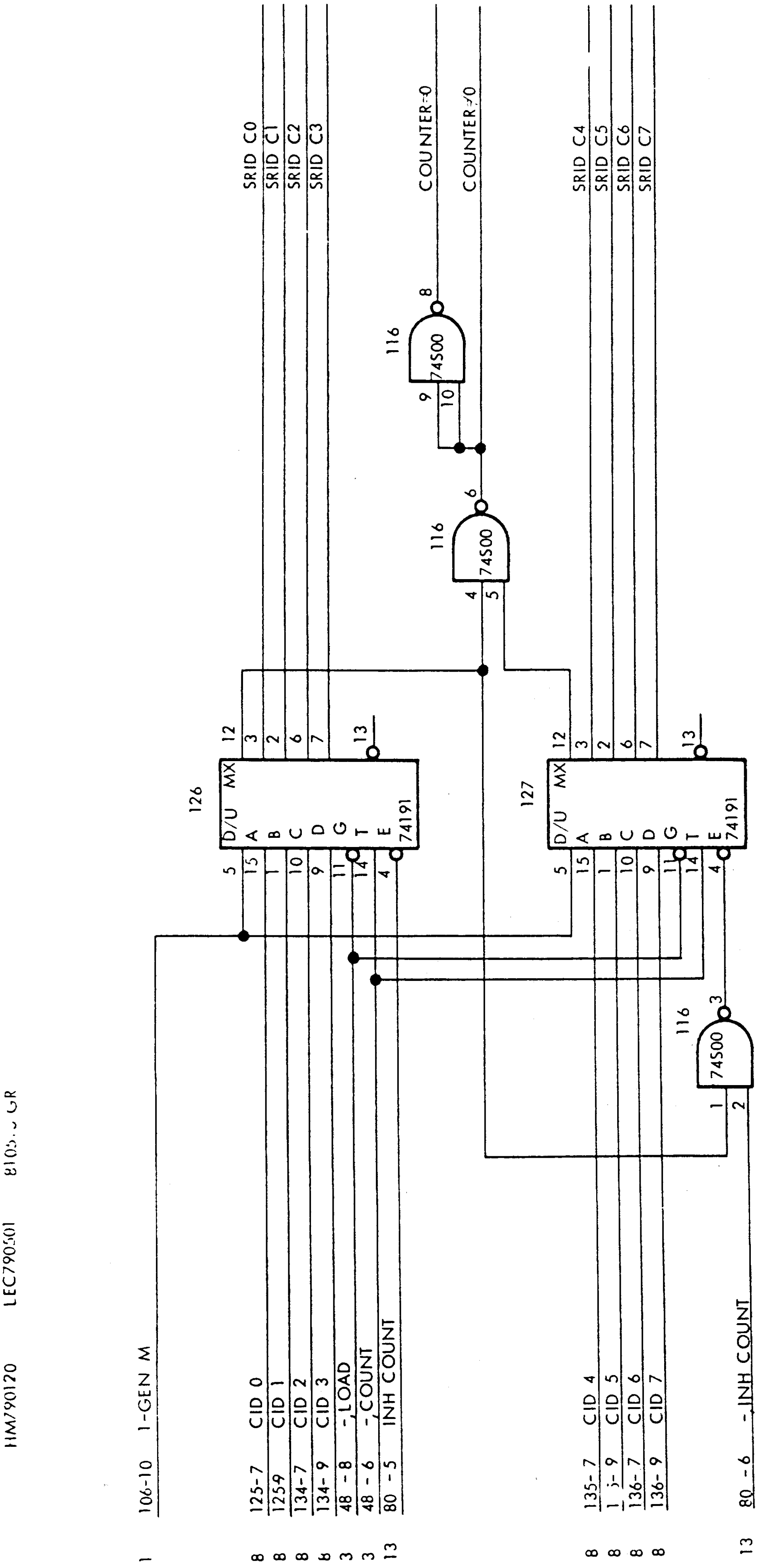
A 137-1

Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
COUNTER = 0	p16, p18	COUNTER = 0
COUNTER ≠ 0	p14	COUNTER ≠ 0
SRID C0 - SRID C5	p10	Shift Register Input Data C0 - C7

Designed by 801110 GR
Drawn by 801110 AMS
Dwg. Date Check

Unit SCU 701		p9
Dwg. No. A25736	Signal List	



A 13782

Circuit Diagram

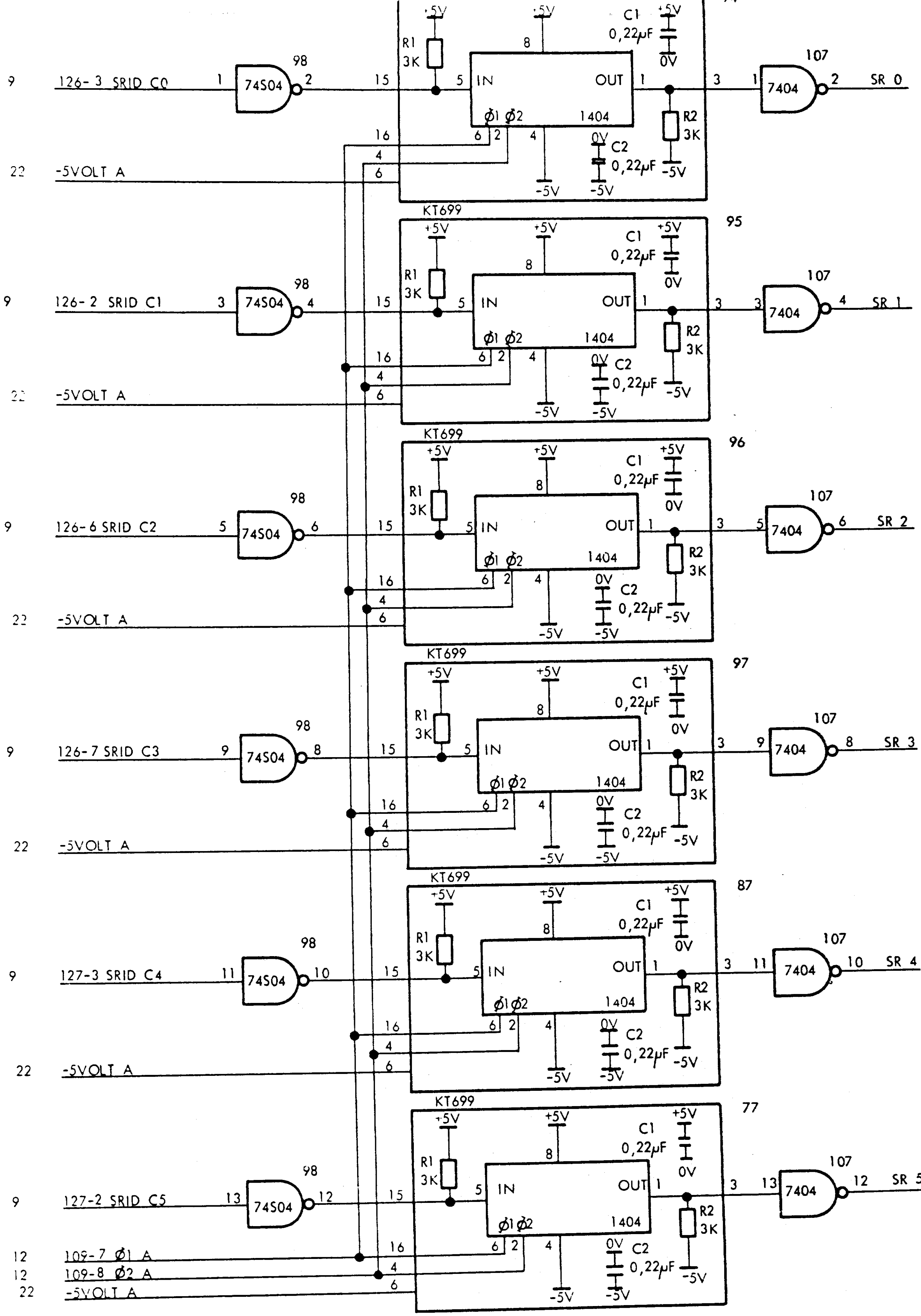
SIGNAL	DESTINATION	DESCRIPTION
SR 0 - SR 5	p12, p8	Shift Register bit 0 - 5

Designed by 801110 GR

Drawn by 801110 AMS

Dw[illegible]ice Check

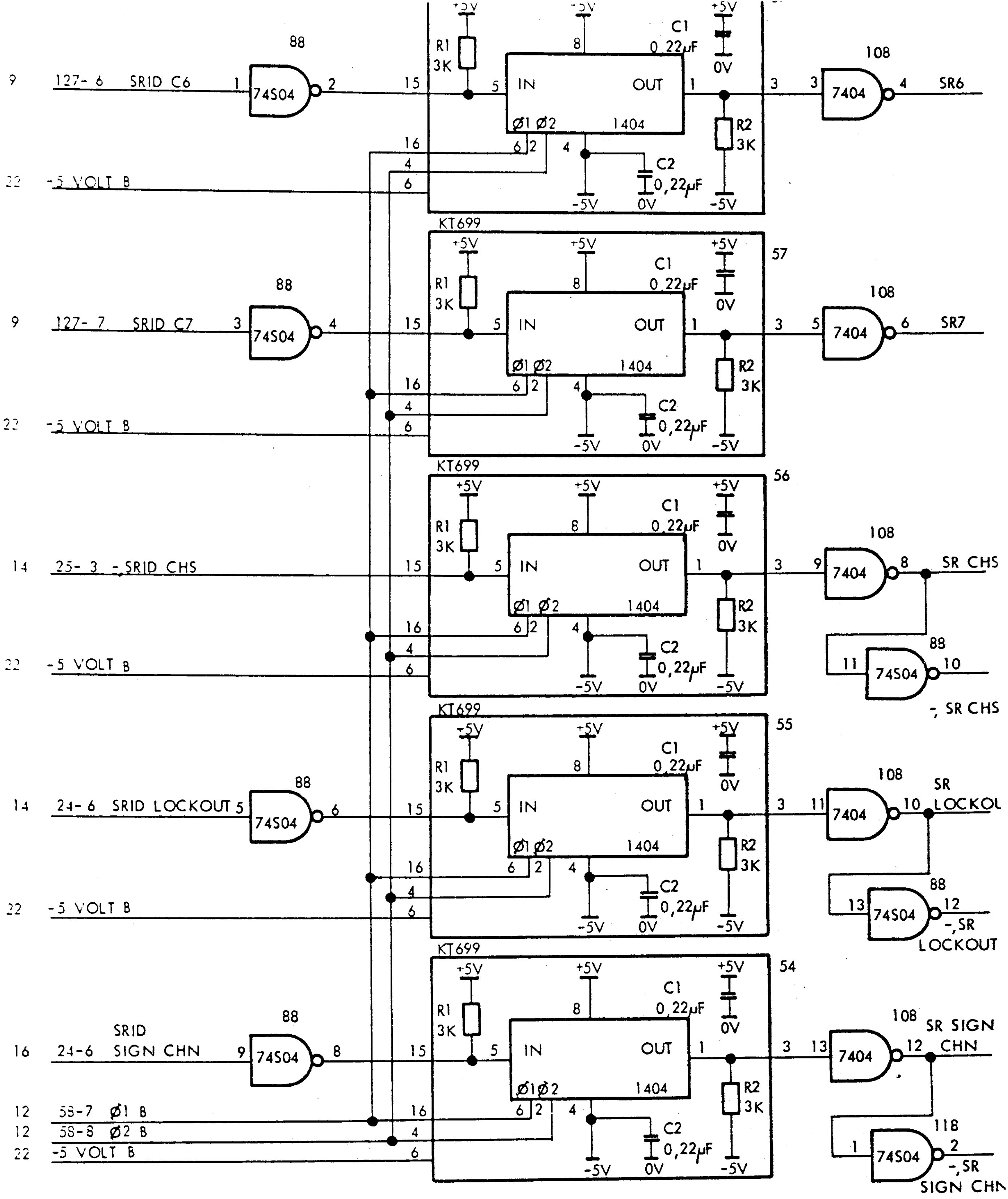
Unit SCU 701		p10
Dwg. No. A25737	Signal List	



HM790216 LEC790521 810518 GR

SIGNAL	DESTINATION	DESCRIPTION
SR 6 - SR 7	p12, p8	Shift Register bit 6-7
SR CHS	p14, p16 p21	Shift Register CHannel Status
¬SR CHS		¬Shift Register CHannel Status
SR LOCKOUT	p14,p17	Shift Register Lockout status
¬SR LOCKOUT	p13	¬ Shift Register Lockout status
SR SIGN CHN	p13, p16 p17,	Shift Register SIGNificant CHange Status
¬SR SIGN CHN	p13	¬Shift Register Significant Change Status

Designed by 801110 GR
Drawn by 801110 AMS
Dwg ...e Check

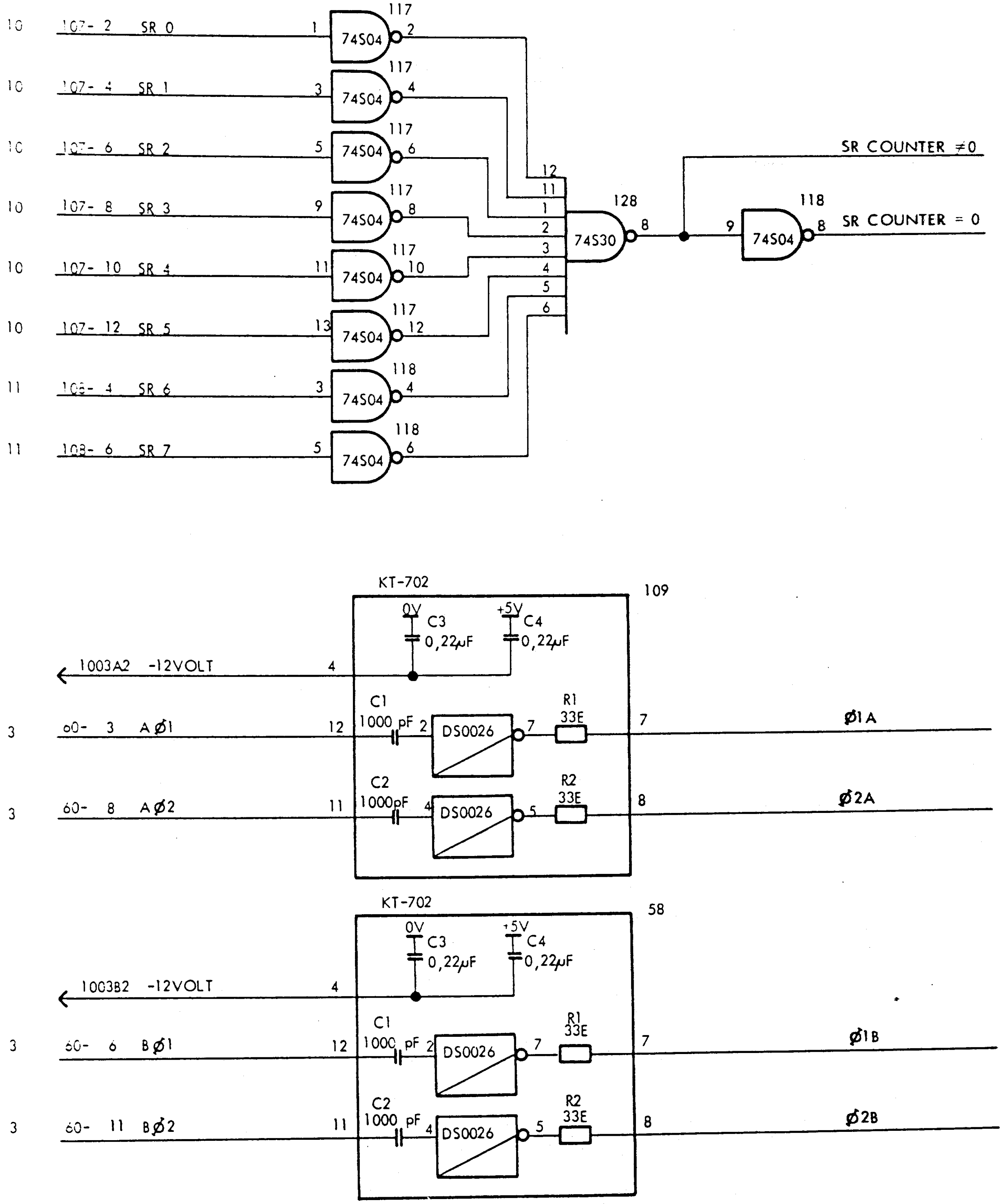


HM790216 LEC790522 810518 GR

SIGNAL	DESTINATION	DESCRIPTION
SR COUNTER = 0	p13	SR COUNTER = 0
SR COUNTER ≠ 0	p13	SR COUNTER ≠ 0
Ø 1 A	p10	Phase 1 A
Ø 2 A	p10	Phase 2 A
Ø 1 B	p11	Phase 1 B
Ø 2 B	p11	Phase 2 B
-12V	PLUG 1003	

Designed by	801110 GR	
Drawn by	801110 AMS	
Dwg		
e Check		

Unit SCU 701		p12
Dwg. No. A25739	Signal List	



810518 GR

LEC790521

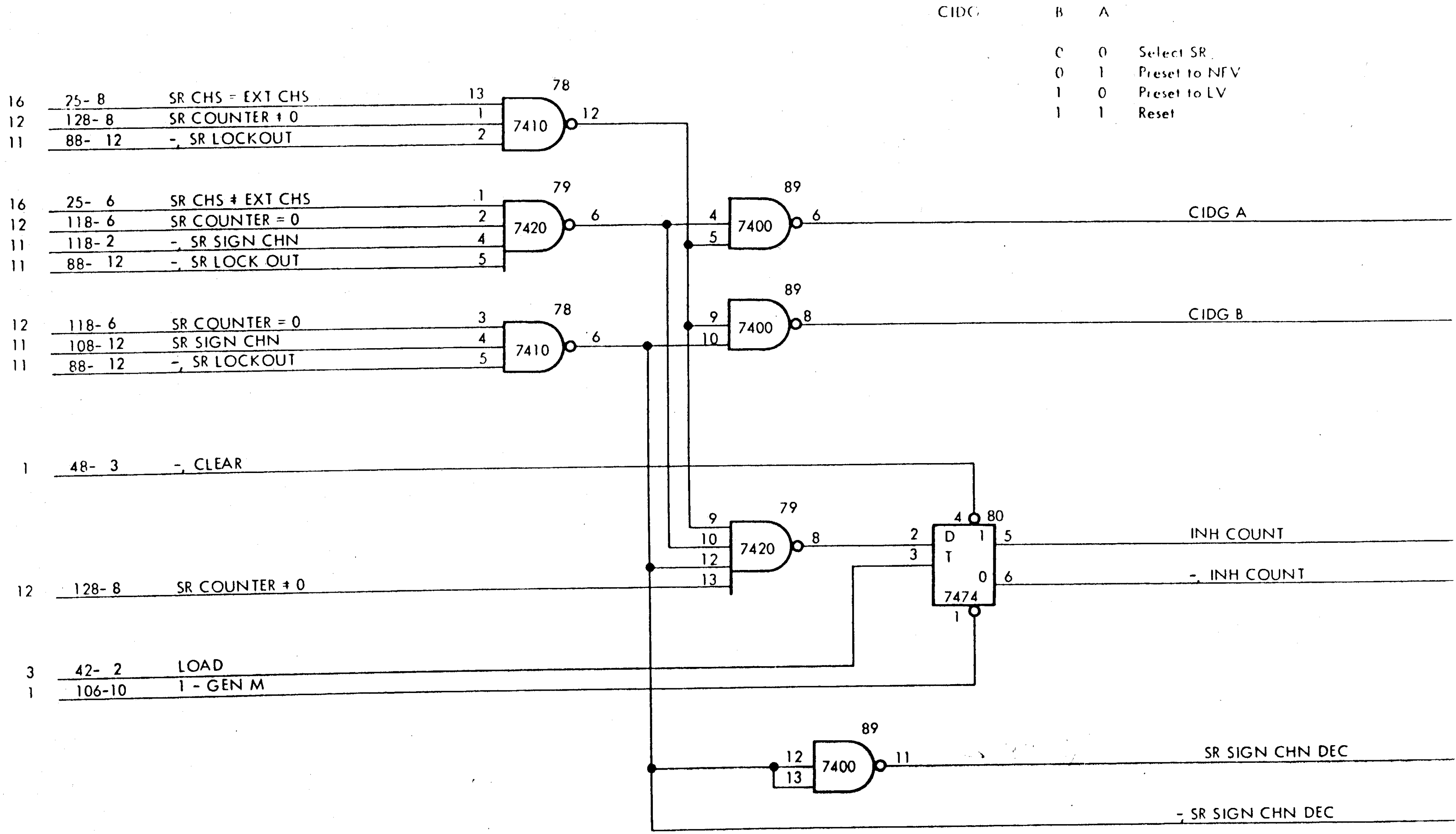
HM790216

SIGNAL	DESTINATION	DESCRIPTION
CIDG A	p8	Counter Inpit Data Gate pulse A
CIDG B	p8	Counter Input Data Gate pulse B
INH COUNT	p9	INHibit COUNT
SR SIGN CHN DEC	p17	Shift Register SIGnificant CHaNge DECoded
¬SR SIGN DEC		¬ Shift Register SIGnificant CHaNge DECoded

Designed by 801110 GR
Drawn by 801110 AMS
Dwg. ...ce Check

Unit SCU 701		p13
Dwg. No. A25740	Signal List	

70116 HM 790516 ABP Rev 791113 LLM 810518 GR



SIGNAL	DESTINATION	DESCRIPTION
¬ LOCKOUT FF	p16, p18	¬ LOCKOUT Flip Flop
SRID LOCKOUT	p11	Shift Register Input Data,LOCKOUT
¬ SRID CHS	p11	¬ Shift Register Input Data, Channel Status

Designed by 801110 GR

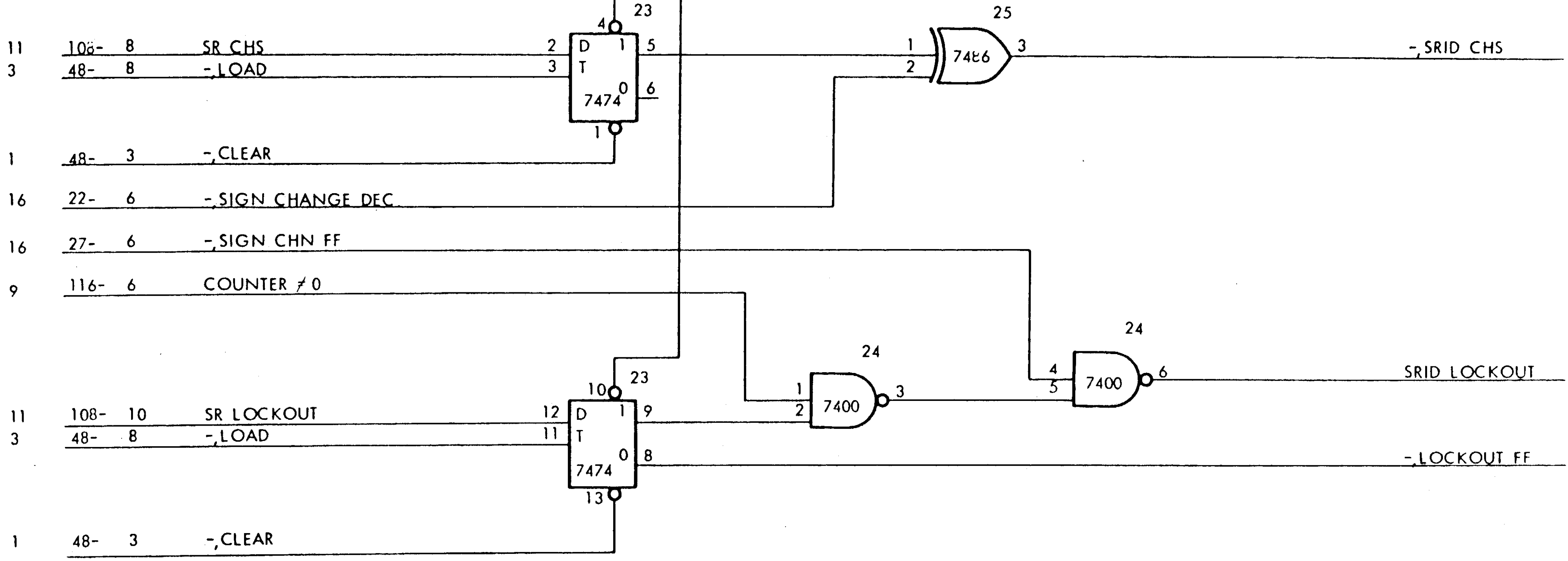
Drawn by 801110 AMS

Dwg ce Check

Unit SCU 701		p14
Dwg. No. A25741	Signal List	

HM790216 LEC790521 Rev. 791113 LLM 810518 GR

CHS FF	-, SIGN CHN DEC	-, SRID CHS
0	0	0
1	0	1
0	1	1
1	1	0



Lockout fjernes hvis : -, SIGN CHANGE FF & COUNTER = 0

Lockout føres igennem hvis : SIGN CHANGE FF ! COUNTER ≠ 0

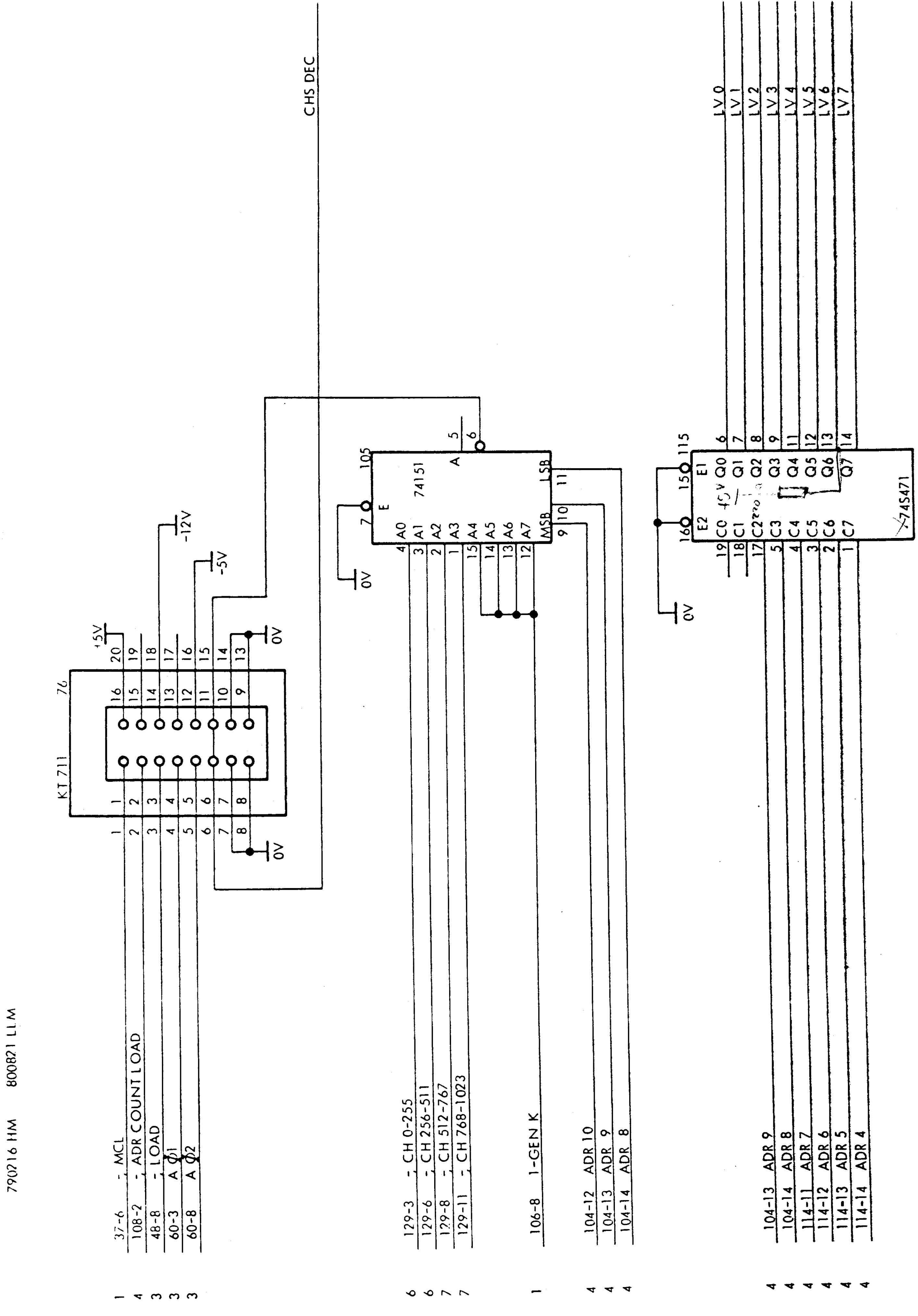
Lockout genereres hvis : SIGN CHANGE FF

SIGNAL	DESTINATION	DESCRIPTION
CHS DEC	p16	CHannel Status DECoded
LV 0 - LV 7	p8	Lockout Value bit 0 - bit 7

Designed by 801110 GR

Drawn by 801110 AMS

Dwg ... Check



CONTROL LOGIC PART 2

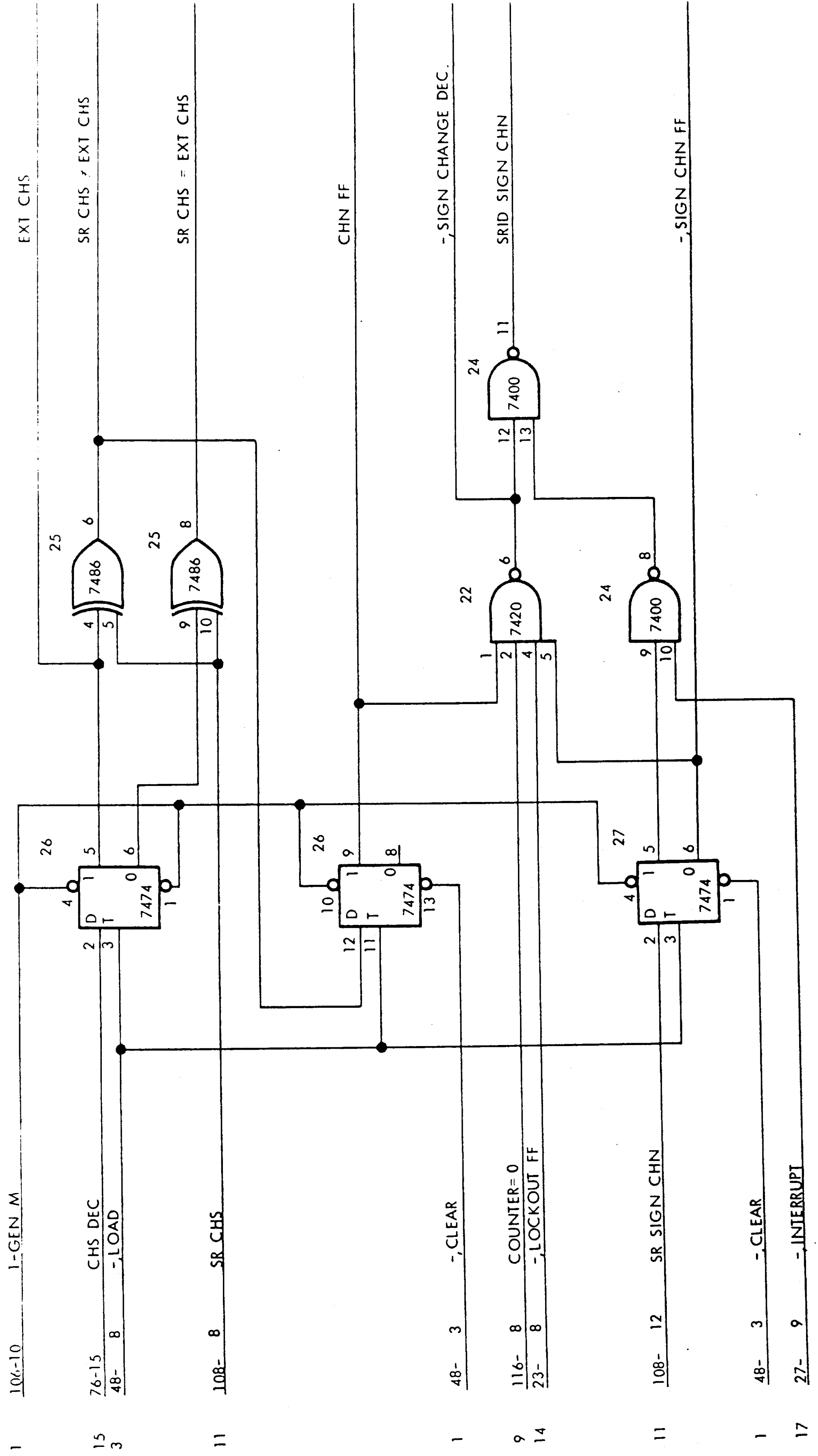
Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
CHN FF	p18	CHaNge Flip Flop
EXT CHS		EXTernal CHannel Status
SR CHS = EXT CHS	p13	Shift Register CHannel Status = External CHannel Status
SR CHS ≠ EXT CHS	p13	Shift Register CHannel Status ≠ EXTernal Channel Status.
SRID SIGN CHN	p11	Shift Register Input Data, SIGNificant CHaNge
¬SIGN CHANGE DEC	p14	¬ SIGNificant CHANGE DECoded
¬SIGN CHN FF	p18, p14	¬SIGNificant CHaNge Flip Flop

Designed by 801110 GR
Drawn by 801110 AMS
Dwg ... Check

Unit		
Unit SCU 701		p16
Dwg. No. A25743	Signal List	

HM790216 LEC790522 810518 GR



SIGN CHANGE fjernes hvis INTERRUPT
SIGN CHANGE føres igennem hvis -,INTERRUPT
SIGN CHANGE genereres hvis CHANGE FF & COUNTER = 0 & -,LOCKOUT FF & -,SIGN CHANGE FF

Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
DONE ENABLE		DONE ENABLE
¬ DEV COMP DEC	p19, p21	¬ DEVice COMPlete DECoded
INTERRUPT	p18	INTERRUPT
¬ INTERRUPT	p18, p16	¬ INTERRUPT
OLD	p21	OLD

Designed by 801110 GR

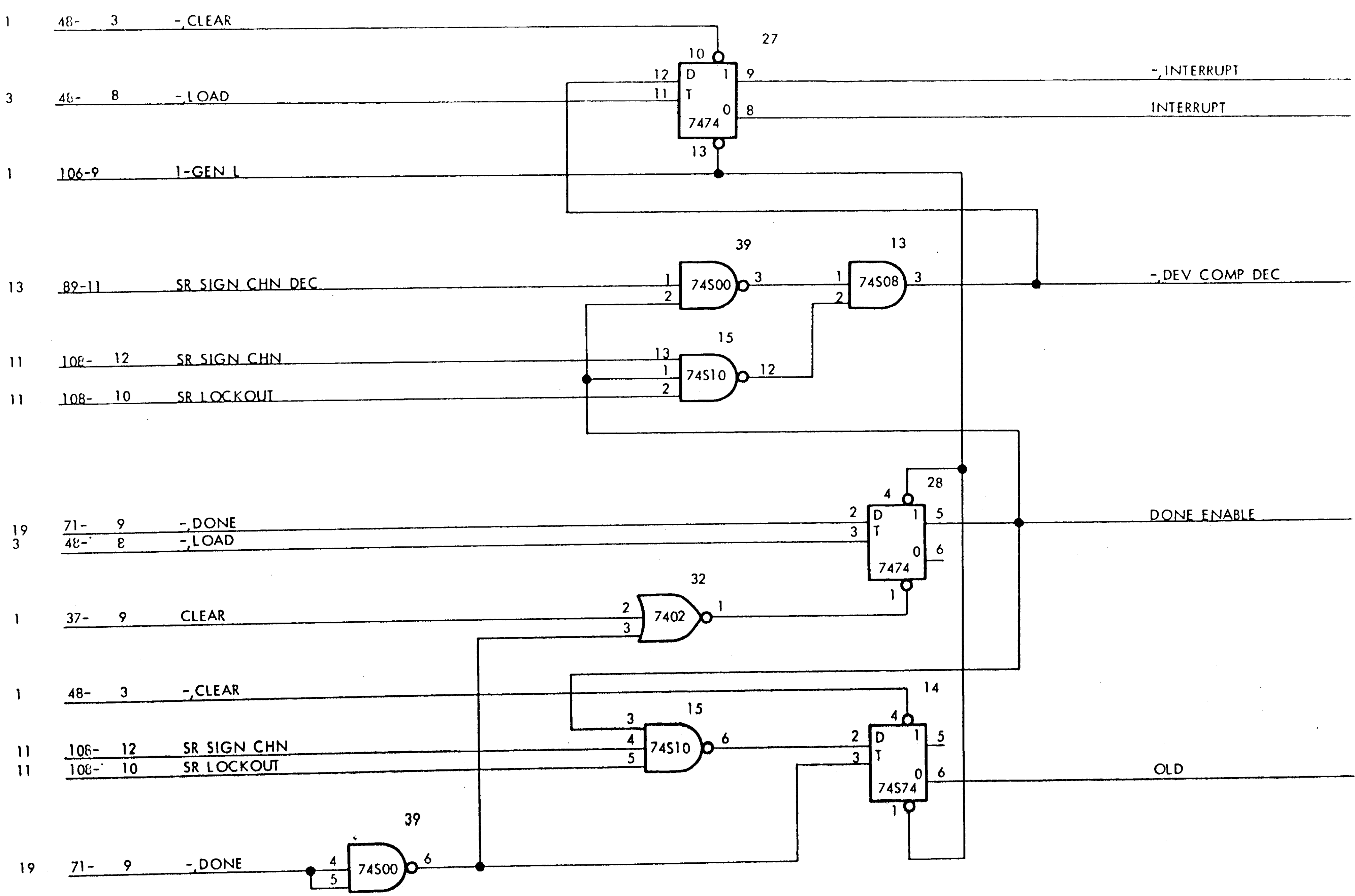
Drawn by 801110 AMS

Dwg ... e Check

Unit SCU 701

Dwg. No. A25744

Signal List


1 48- 3 -,CLEAR
3 48- 8 -,LOAD
1 106-9 1-GEN L
13 89-11 SR SIGN CHN DEC
11 108- 12 SR SIGN CHN
11 108- 10 SR LOCKOUT
19 71- 9 -,DONE
3 48- 8 -,LOAD
1 37- 9 CLEAR
1 48- 3 -,CLEAR
11 108- 12 SR SIGN CHN
11 108- 10 SR LOCKOUT
19 71- 9 -,DONE
27
7474
-,INTERRUPT
INTERRUPT
39
74S00
13
74S08
-,DEV COMP DEC
15
74S10
28
7474
DONE ENABLE
32
7402
14
74S74
OLD

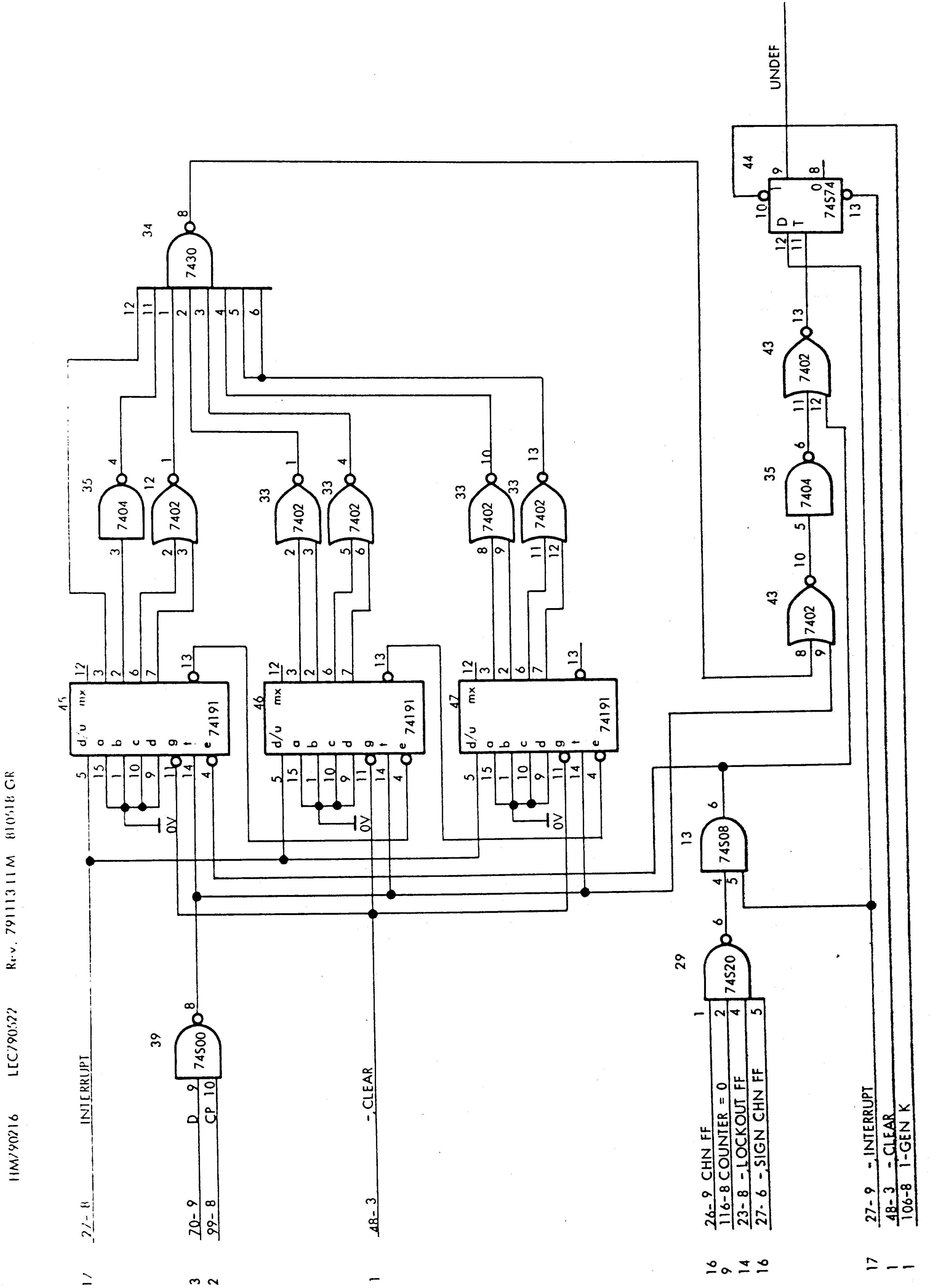
SIGNAL	DESTINATION	DESCRIPTION
UNDEF	p21	UNDEFined

Designed by 801110 GR

Drawn by 801110 AMS

Dwg Office Check

Unit SCU 701		p18
Dwg. No. A25745	SignalList	



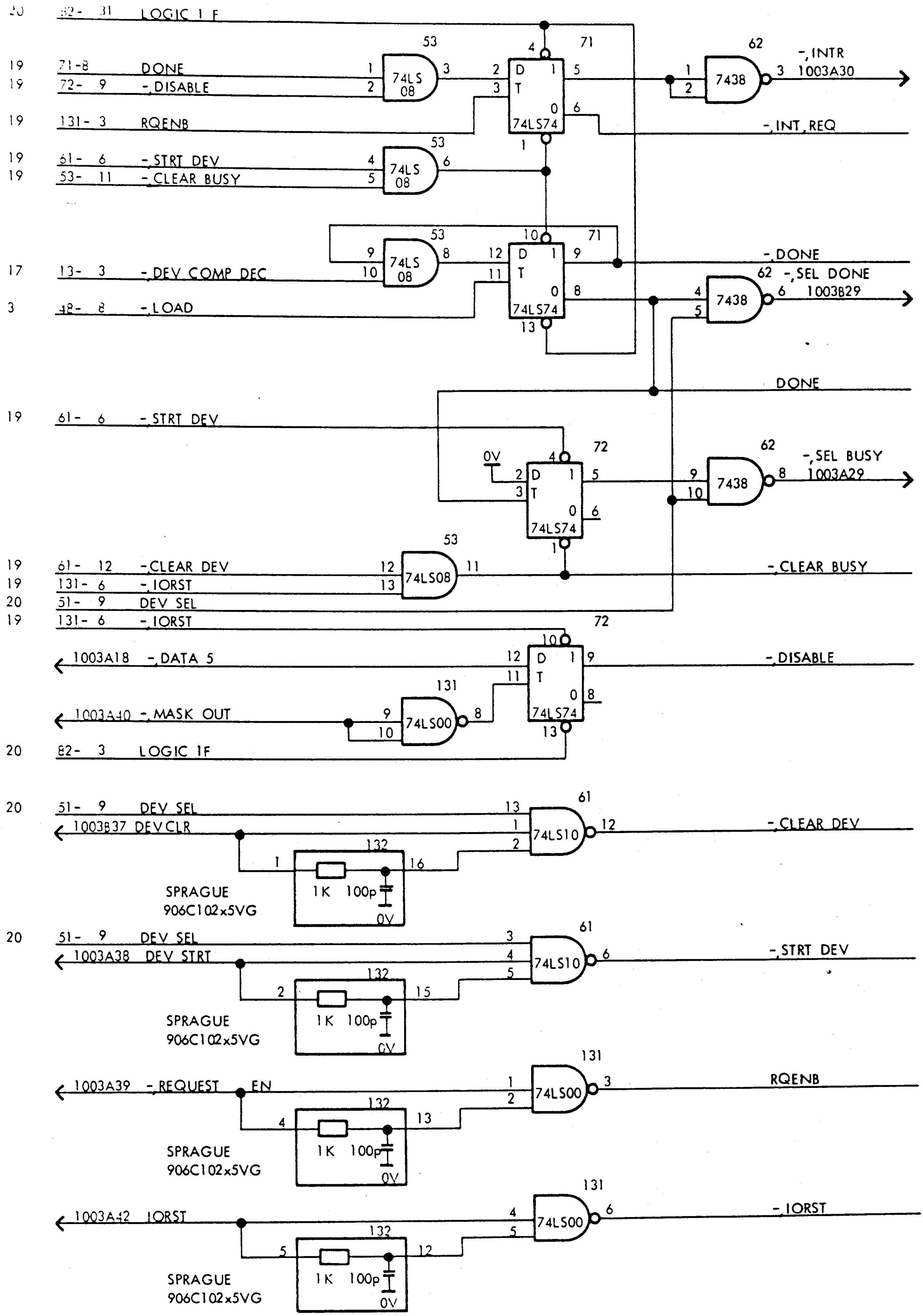
UNDEFINED COUNTER

Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
¬ CLEAR BUSY	p19	¬ CLEAR BUSY
¬ CLEAR DEV	p19	¬ CLEAR DEVice Flip Flop
DONE	p19	DONE
¬ DONE	p17	¬ DONE
¬ INTR	PLUG 1003	¬ INTeRrupt
¬INT REQ	p20	¬ INTeRrupt REQuest
¬ IORST	p1, p19	¬ IO ReSeT pulse
RQENB	p19	REQuest ENaBLE
¬ SEL BUSY	PLUG 1003	¬SELect BUSY
¬ SEL DONE	PLUG 1003	¬SELect DONE
¬STRT DEV	p1, p19	¬STaRT DEVice
¬ DATA 5	PLUG 1003	¬ DATA Bus 5
DEV CLR	PLUG 1003	DEVice CLeaR
DEV STRT	PLUG 1003	DEVice STaRT
IORST	PLUG 1003	IO ReSeT Pulse
¬ REQUEST EN	PLUG 1003	¬REQUEST ENable
¬ MASK OUT	PLUG 1003	¬ MASK OUT

Designed by 801110 GR
Drawn by 801110 AMS
Dwg ... e Check

Unit SCU 701
Dwg. No. A25746
Signal List
p19



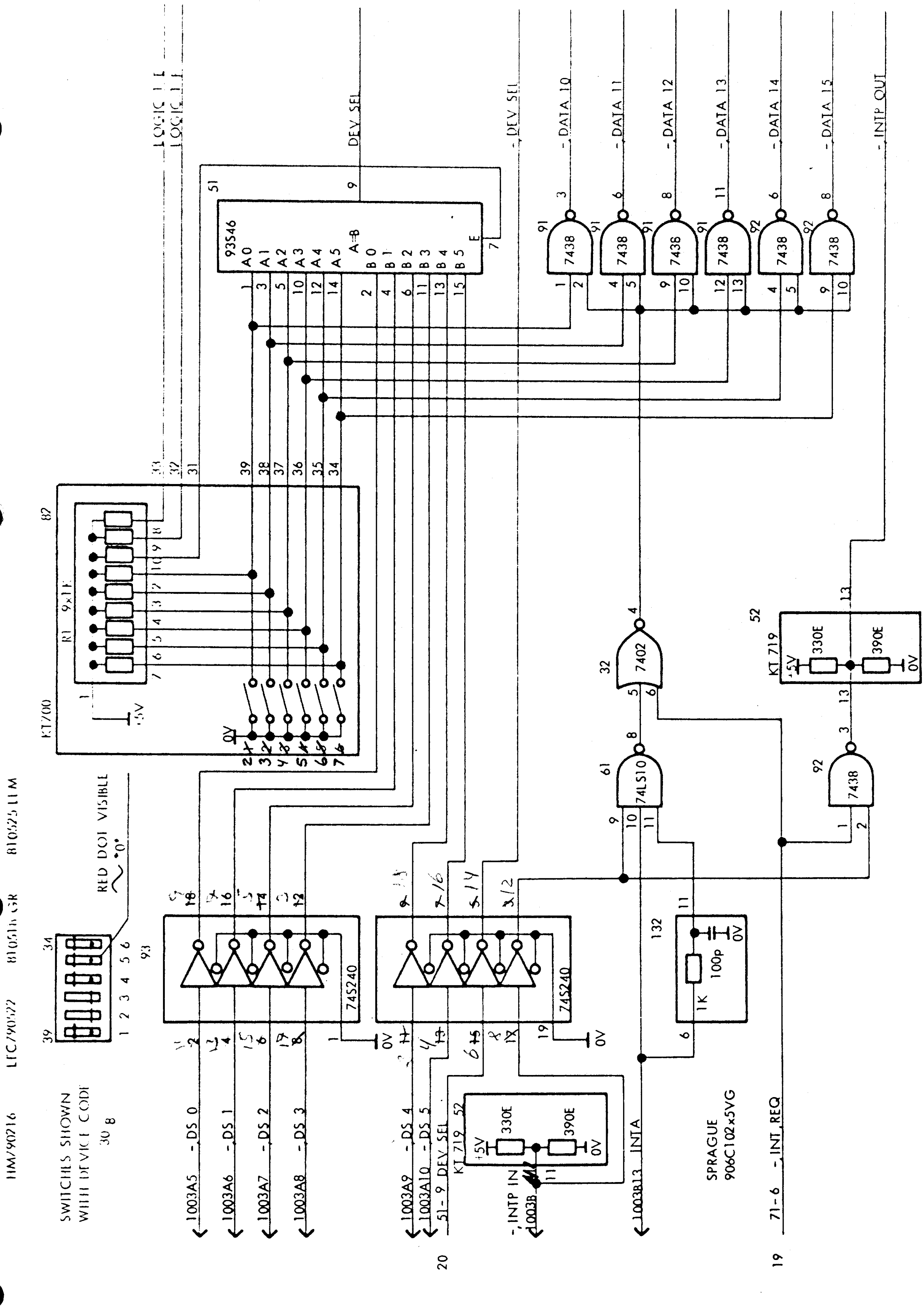
REV ..113 LLM 810518 GR

LEC790522

HM790216

SIGNAL	DESTINATION	DESCRIPTION
DEV SEL	p19, p20	DEVice SELect
¬ DEV SEL	p21	¬ DEVice SELect
¬ DATA 10 - ¬DATA 15	p21	¬ DARA Bus bit 10 - bit 15
¬DS 0 - ¬ DS 5	PLUG 1003	¬ Devise Select bit 0 - bit 5
INTA	PLUG 1003	INTerrupt Acknowledge
¬ INTP IN	PLUG 1003	INTerrupt Priority IN
¬ INTP OUT		¬ INTerrupt Priority OUT
LOGIC 1E		
LOGIC 1F	p19	

Designed by 801110 GR
Drawn by 801110 AMS
Dw... ce Check



SWITCHES SHOWN WITH DEVICE CODE 30 8
RED DOT VISIBLE "0"
93546
7438
7402
74LS10
74S240
KT 719
330E
390E
+5V
0V
1K
100p
SPRAGUE 906C102x5VG
- DEV SEL
- DATA 10
- DATA 11
- DATA 12
- DATA 13
- DATA 14
- DATA 15
- INTP OUT
1003A5 - DS 0
1003A6 - DS 1
1003A7 - DS 2
1003A8 - DS 3
1003A9 - DS 4
1003A10 - DS 5
51-9 DEV SEL
- INTP IN
1003B13 INTA
71-6 - INT REQ

SIGNAL	DESTINATION	DESCRIPTION
¬ DATA 0 - ¬ DATA 1	PLUG 1003	¬ DATA Bus bit 0 - bit 1
¬ DATA 5 - ¬ DATA 15	PLUG 1003	¬ DATA Bus bit 5 - bit 15
¬ DATI A	PLUG 1003	¬ DATa In A

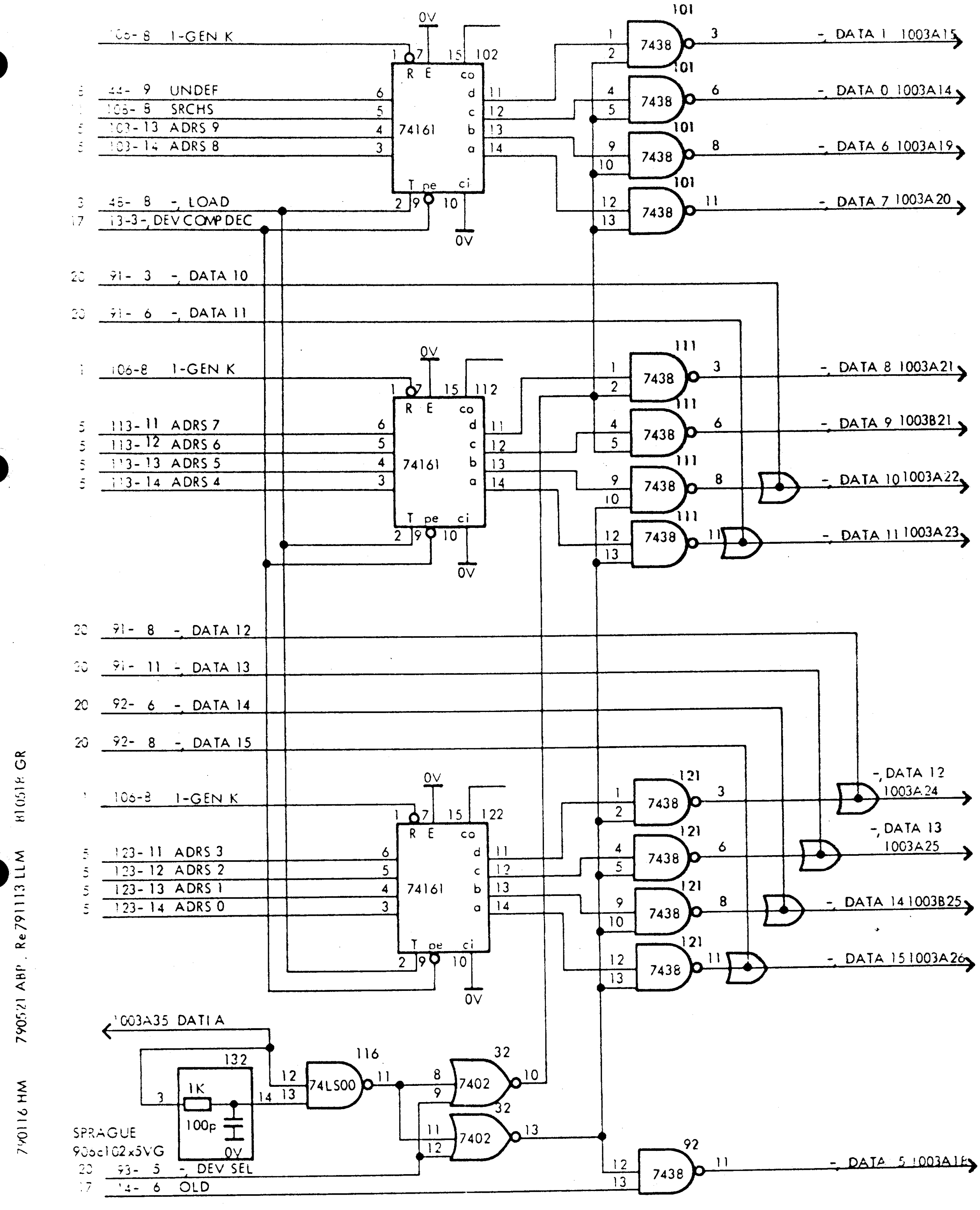
Designed by 801110 GR

Drawn by 801110 AMS

Dwg

.e Check

Unit SCU 701		p21
Dwg. No. A25748	Signal List	



106-8 1-GEN K
44-9 UNDEF
106-8 SRCHS
103-13 ADRS 9
103-14 ADRS 8
46-8 -, LOAD
13-3-, DEV COMP DEC
91-3 -, DATA 10
91-6 -, DATA 11
113-11 ADRS 7
113-12 ADRS 6
113-13 ADRS 5
113-14 ADRS 4
91-8 -, DATA 12
91-11 -, DATA 13
92-6 -, DATA 14
92-8 -, DATA 15
123-11 ADRS 3
123-12 ADRS 2
123-13 ADRS 1
123-14 ADRS 0
74161
7438
74LS00
7402
1003A35 DATI A
SPRAGUE
90sc102x5VG
1K
100p
0V
93-5 -, DEV SEL
14-6 OLD
-, DATA 1 1003A15
-, DATA 0 1003A14
-, DATA 6 1003A19
-, DATA 7 1003A20
-, DATA 8 1003A21
-, DATA 9 1003B21
-, DATA 10 1003A22
-, DATA 11 1003A23
-, DATA 12 1003A24
-, DATA 13 1003A25
-, DATA 14 1003B25
-, DATA 15 1003A26
-, DATA 5 1003A18
790116 HM 790521 ABP, Re 791113 LLM 810518 GR

SIGNAL	DESTINATION	DESCRIPTION
NFV 0 - NFV 7	p8	Noise Filtering Value bit 0 - bit 7
-5V A	p10	
-5V B	p11	
-12V	PLUG 1003	

Designed by 801110 GR

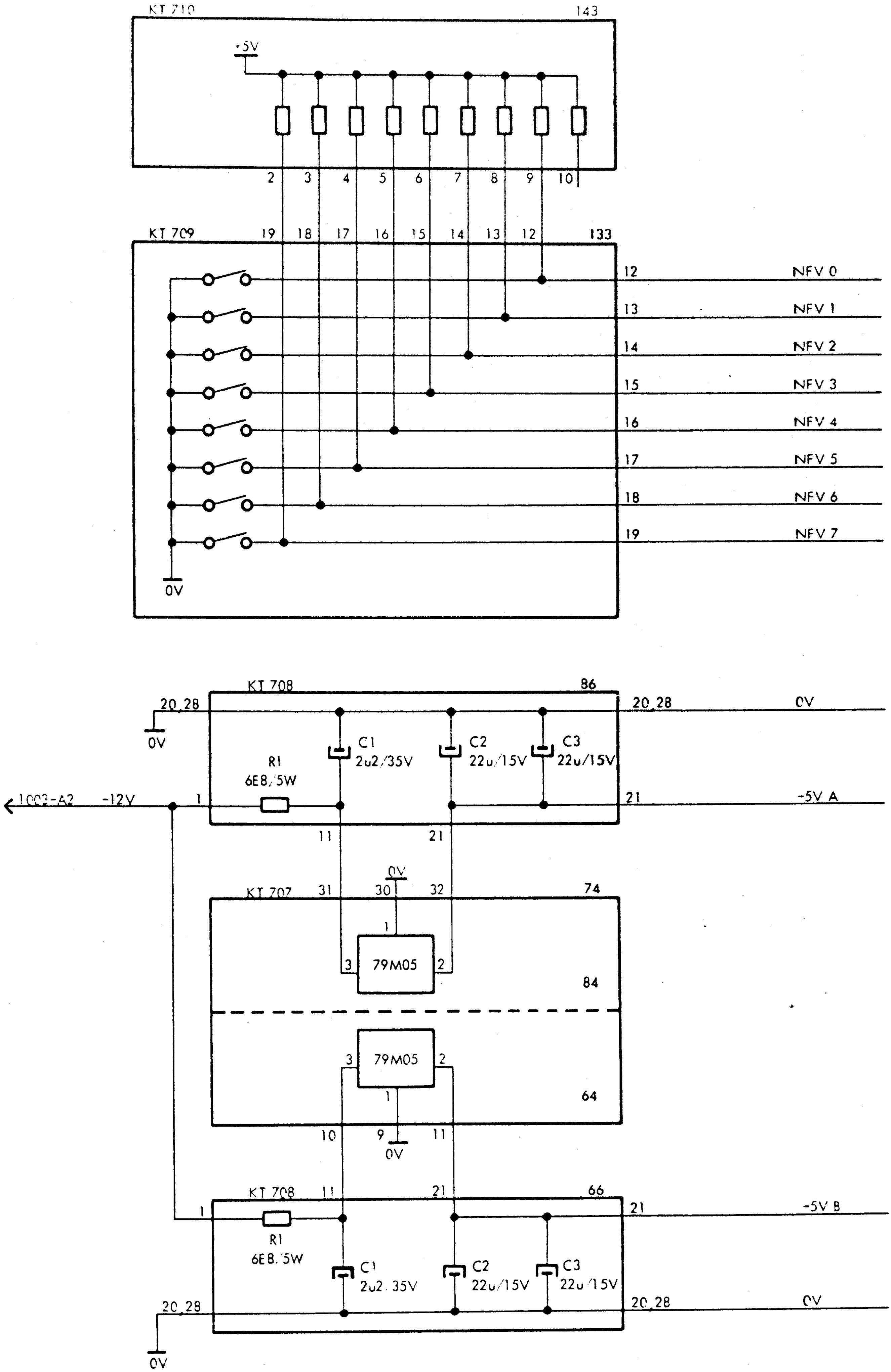
Drawn by 801110 AMS

Dwg ...e Check

Unit: SCU 701

Dwg. No. A25749

Signal List



790625 GR 791114 LLM 810518 GR

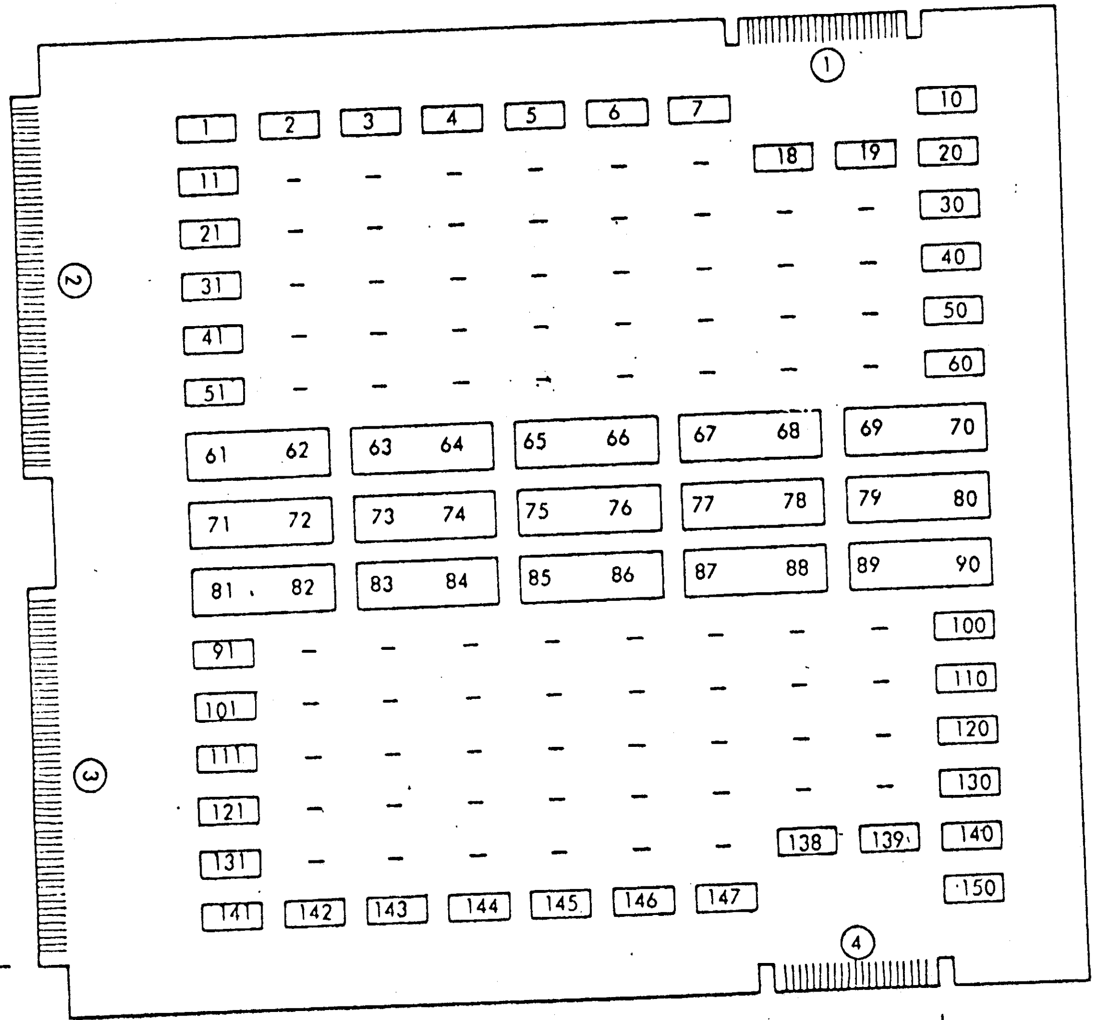
NOISE FILTERING VALUE SELECTOR
-5V POWER SUPPLY
Circuit Diagram

810518 GR

connector no. - pin no. and package position no.

(card viewed from componentside)

con. no.	pin no.	
1	B25 - - - -B1	comp.side
	A25 - - - -A1	solder side



con. no.	pin no.		pin no.	con. no.
2	A49- - - - - - - - - - - - - A1	comp.	B1 - - - - - - - - - - - - - B49	3
	B49- - - - - - - - - - - - - B1	solder	A1 - - - - - - - - - - - - - A49	

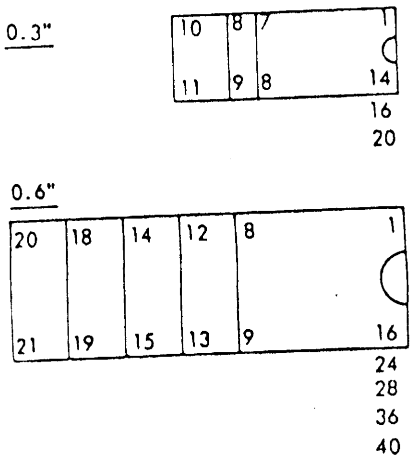
con. no.	pin no.	
4	A25 - - - A1	comp.side
	B25 - - - B1	solder side

SCU 701

package orientation
and pin no.

0.3"

0.6"



RC 2294
standardcard for
cassett -S 701

CONNECTOR : J 1001

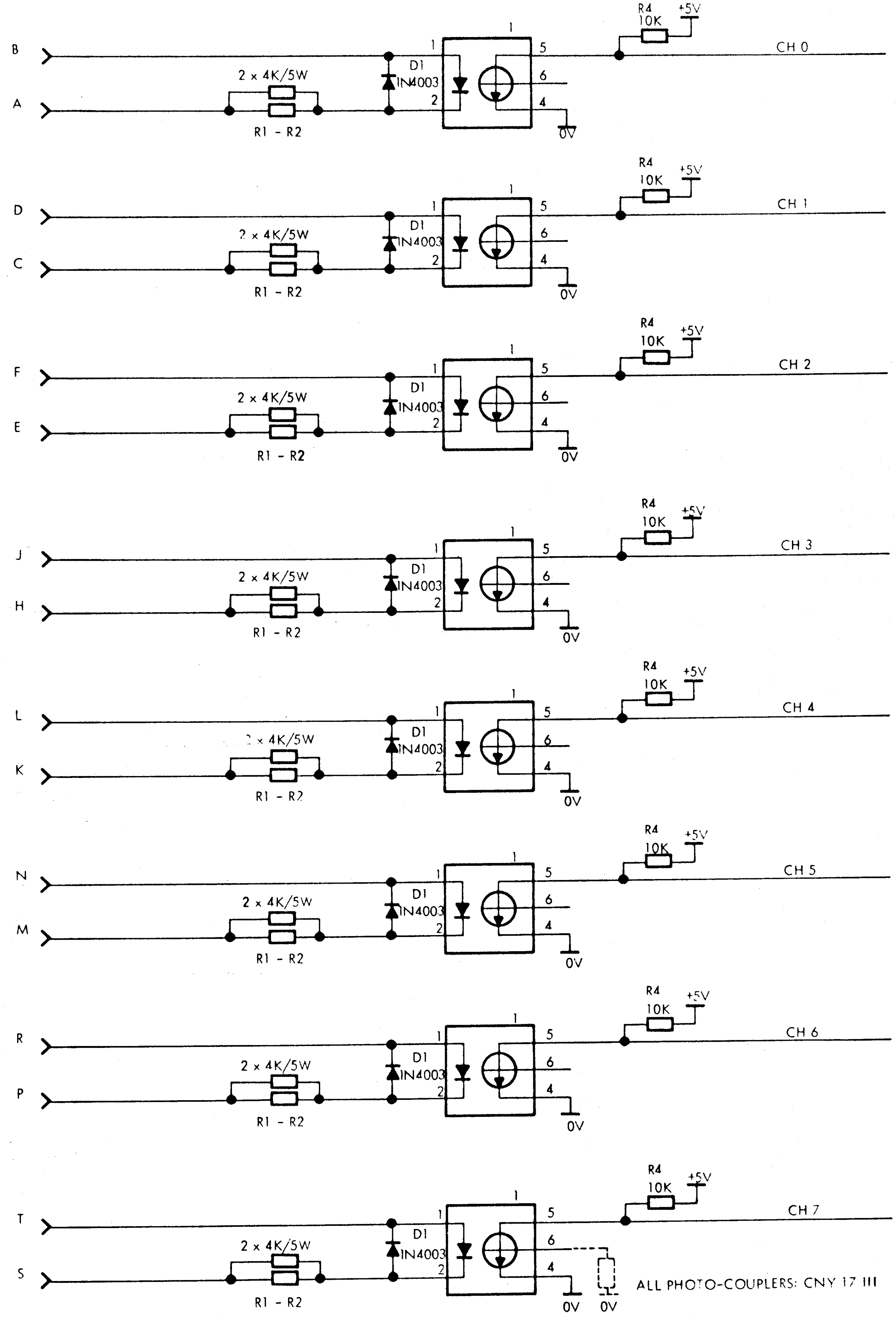
PLUG A	SIGNAL	PLUG B	SIGNAL
1	+ 5V DC	1	+ 5V DC
2	+ 5V DC	2	+ 5V DC
3	+ 5V DC	3	+ 5V DC
4	0 - ADR 0	4	0V
5	0 - ADR 1	5	0V
6	0 - ADR 2	6	0V
7	0 - ADR 3	7	0V
8	0 - ADR 4	8	0V
9	0 - ADR 5	9	0V
10	0 - ADR 6	10	0V
11	0 - ADR 7	11	0V
12	¬ CH 0 - 255 A	12	¬ CH 0 - 255 B
13	0V	13	0V
14	¬ CH 256 - 511 A	14	¬ CH 256 - 511 B
15	1 - ADR 0	15	0V
16	1 - ADR 1	16	0V
17	1 - ADR 2	17	0V
18	1 - ADR 3	18	0V
19	1 - ADR 4	19	0V
20	1 - ADR 5	20	0V
21	1 - ADR 6	21	0V
22	1 - ADR 7	22	0V
23	+ 5V DC	23	+ 5V DC
24	+ 5V DC	24	+ 5V DC
25	+ 5V DC	25	+ 5V DC

810518 GR

800904 GR 800904 LLM

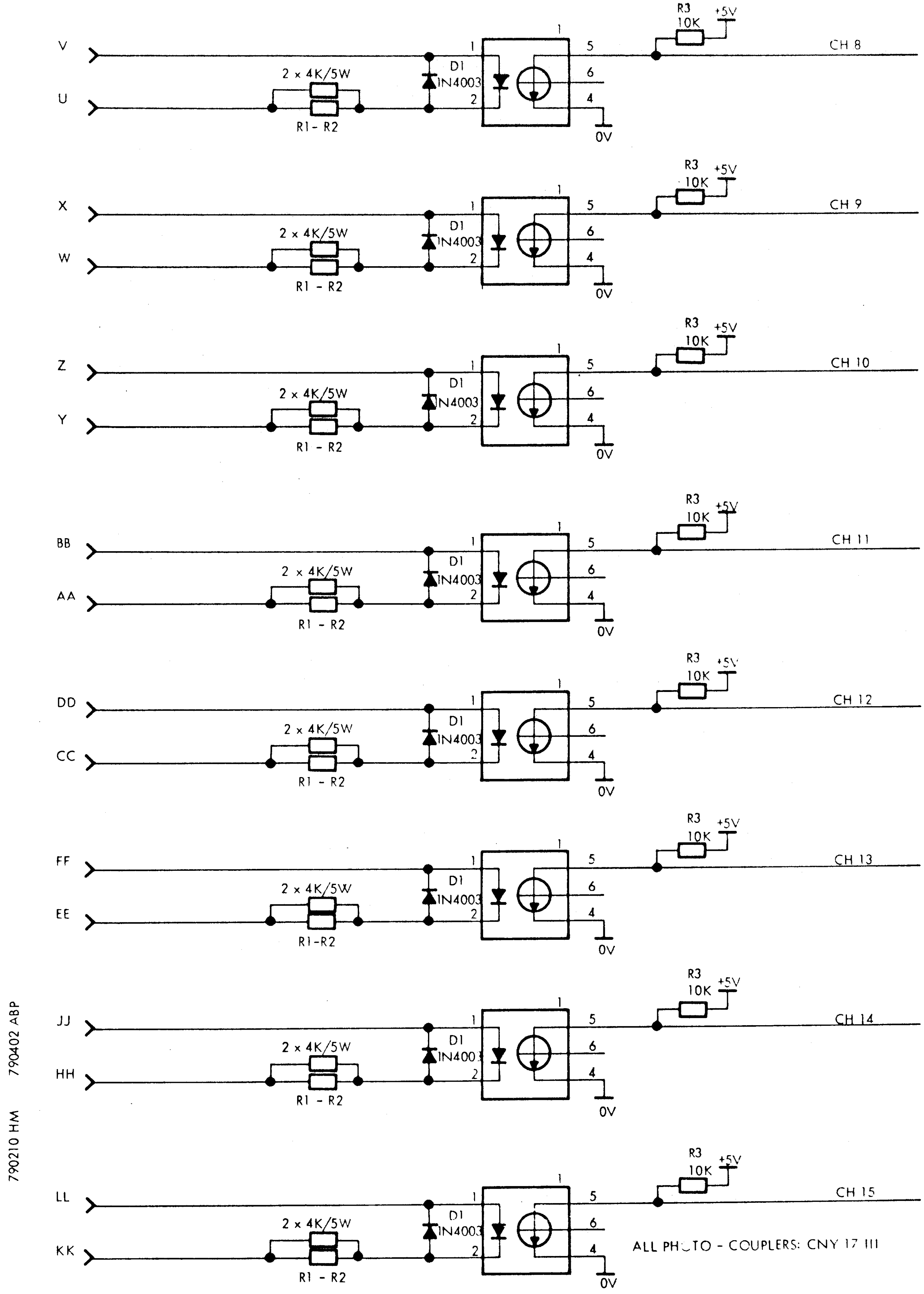
CONNECTOR : J 1004

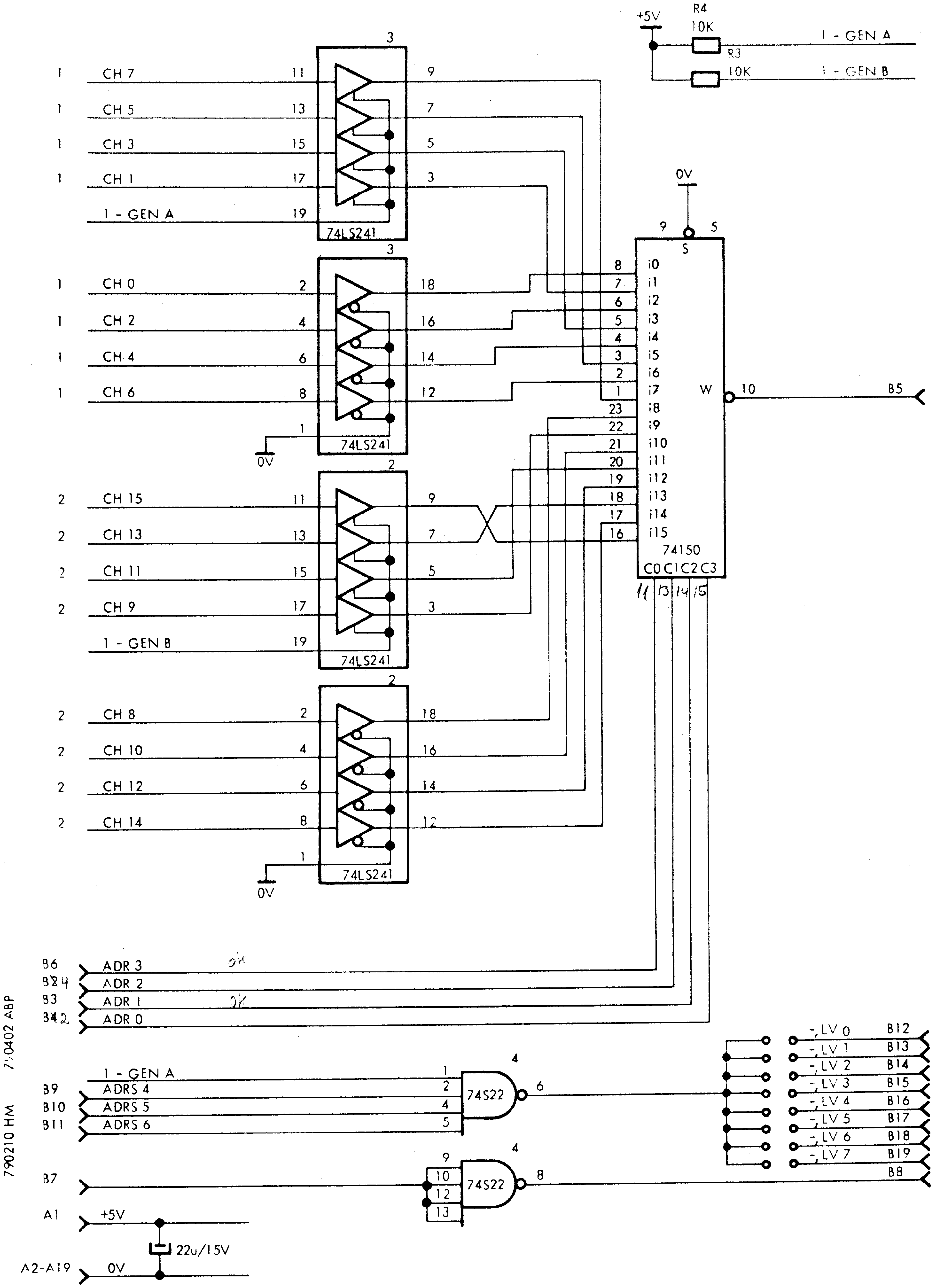
PLUG A	SIGNAL	PLUG B	SIGNAL
1	+ 5V DC	1	+ 5V DC
2	+ 5V DC	2	+ 5V DC
3	+ 5V DC	3	+ 5V DC
4	2 - ADR 0	4	0V
5	2 - ADR 1	5	0V
6	2 - ADR 2	6	0V
7	2 - ADR 3	7	0V
8	2 - ADR 4	8	0V
9	2 - ADR 5	9	0V
10	2 - ADR 6	10	0V
11	2 - ADR 7	11	0V
12	¬ CH 512 - 767 A	12	¬ CH 512 - 767 B
13	0V	13	0V
14	¬ CH 768 - 1023 A	14	¬ CH 768 - 1023 B
15	3 - ADR 0	15	0V
16	3 - ADR 1	16	0V
17	3 - ADR 2	17	0V
18	3 - ADR 3	18	0V
19	3 - ADR 4	19	0V
20	3 - ADR 5	20	0V
21	3 - ADR 6	21	0V
22	3 - ADR 7	22	0V
23	+5V DC	23	+ 5V DC
24	+ 5V DC	24	+ 5V DC
25	+ 5V DC	25	+ 5V DC



790402 ABP

790210 HM


V
U
2 x 4K/5W
R1 - R2
D1
1N4003
R3
10K
+5V
CH 8
0V
X
W
CH 9
Z
Y
CH 10
BB
AA
CH 11
DD
CC
CH 12
FF
EE
CH 13
JJ
HH
CH 14
LL
KK
CH 15
ALL PHOTO - COUPLERS: CNY 17 III
790402 ABP
790210 HM



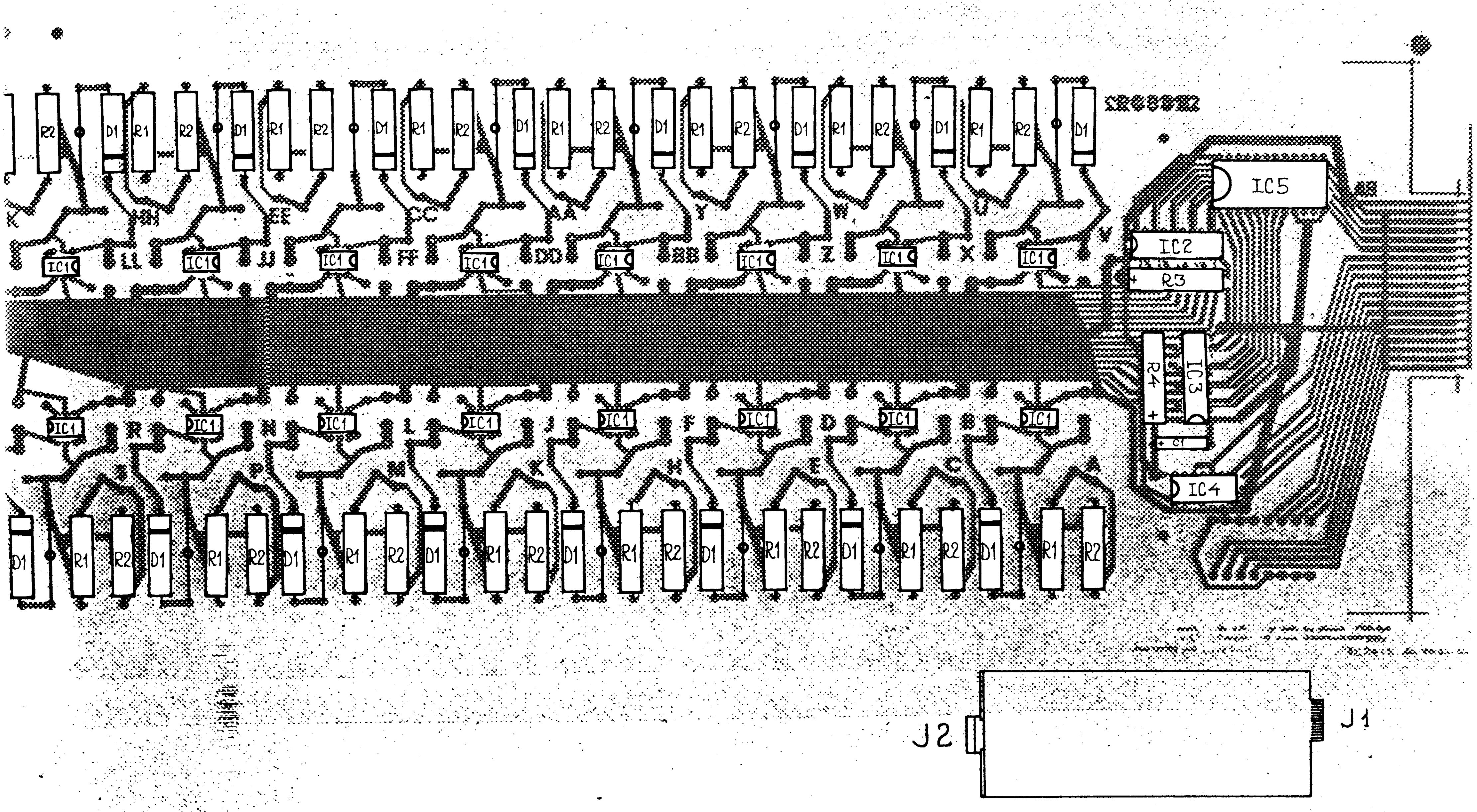
EIM 100

A13732

INPUT MODULE
CHANNEL MULTIPLEXER
Circuit Diagram

RC 3422-1
p. 3 of 3

790228 LLM   790315 ABP



A13628

PCB ASSEMBLY DRAWING RC 3422

EIM100

J 2

ELCO Varilock Receptacle, type 8016-038, code -

PIN	GEN ADR	SIGNAL NAME
A		CH 0 Return
B		CH 0
C		CH 1 Return
D		CH 1
E		CH 2 Return
F		CH 2
H		CH 3 Return
J		CH 3
K		CH 4 Return
L		CH 4
M		CH 5 Return
N		CH 5
P		CH 6 Return
R		CH 6
S		CH 7 Return
T		CH 7
U		CH 8 Return
V		CH 8
W		CH 9 Return
X		CH 9
Y		CH 10 Return
Z		CH 10
AA		CH 11 Return
BB		CH 11
CC		CH 12 Return
DD		CH 12
EE		CH 13 Return
FF		CH 13
HH		CH 14 Return
JJ		CH 14
KK		CH 15 Return
LL		CH 15
MM		
NN		
PP		
RR		
SS		
TT		

Replaced by Dwg. No. | due to ECN | Replaces Dwg. No. | Design Check | Dwg. Office Check | Drawn by 800923 LLM | Designed by 800923 GR

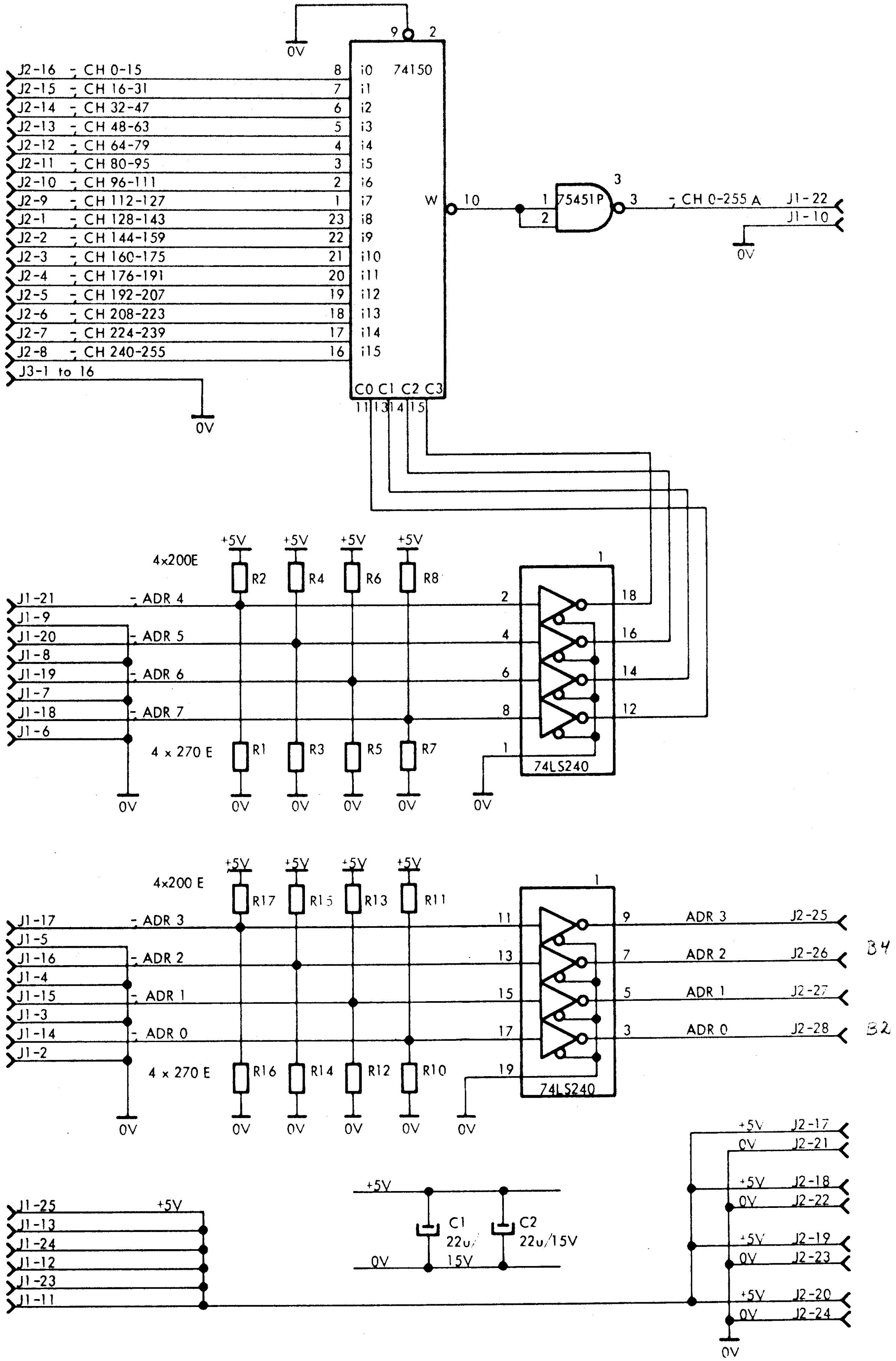
A/S REGNECENTRALEN RCSL: 52-AA95

Unit: EIM 100

Dwg. No.: A 25917

Jacklist

J 2



HM/NBL 800822 LLM REV. 810409 LLM

CHANNEL ADDRESS 0-3 AND
CHANNEL MULTIPLEXER
Circuit Diagram

J 1 ITT Cannon, type DB - 25 P		
PIN	GEN. ADR.	SIGNAL NAME
1		0V
2		0V
3		0V
4		0V
5		0V
6		0V
7		0V
8		0V
9		0V
10		0V
11		+ 5V
12		+ 5V
13		+ 5V
14		¬ ADR 0
15		¬ ADR 1
16		¬ ADR 2
17		¬ ADR 3
18		¬ ADR 7
19		¬ ADR 6
20		¬ ADR 5
21		¬ ADR 4
22		¬ CH 0 - 255 A
23		+ 5V
24		+ 5V
25		+ 5V

DBSL: 064

800904 GR 800905 LLM REV. 810409 LLM