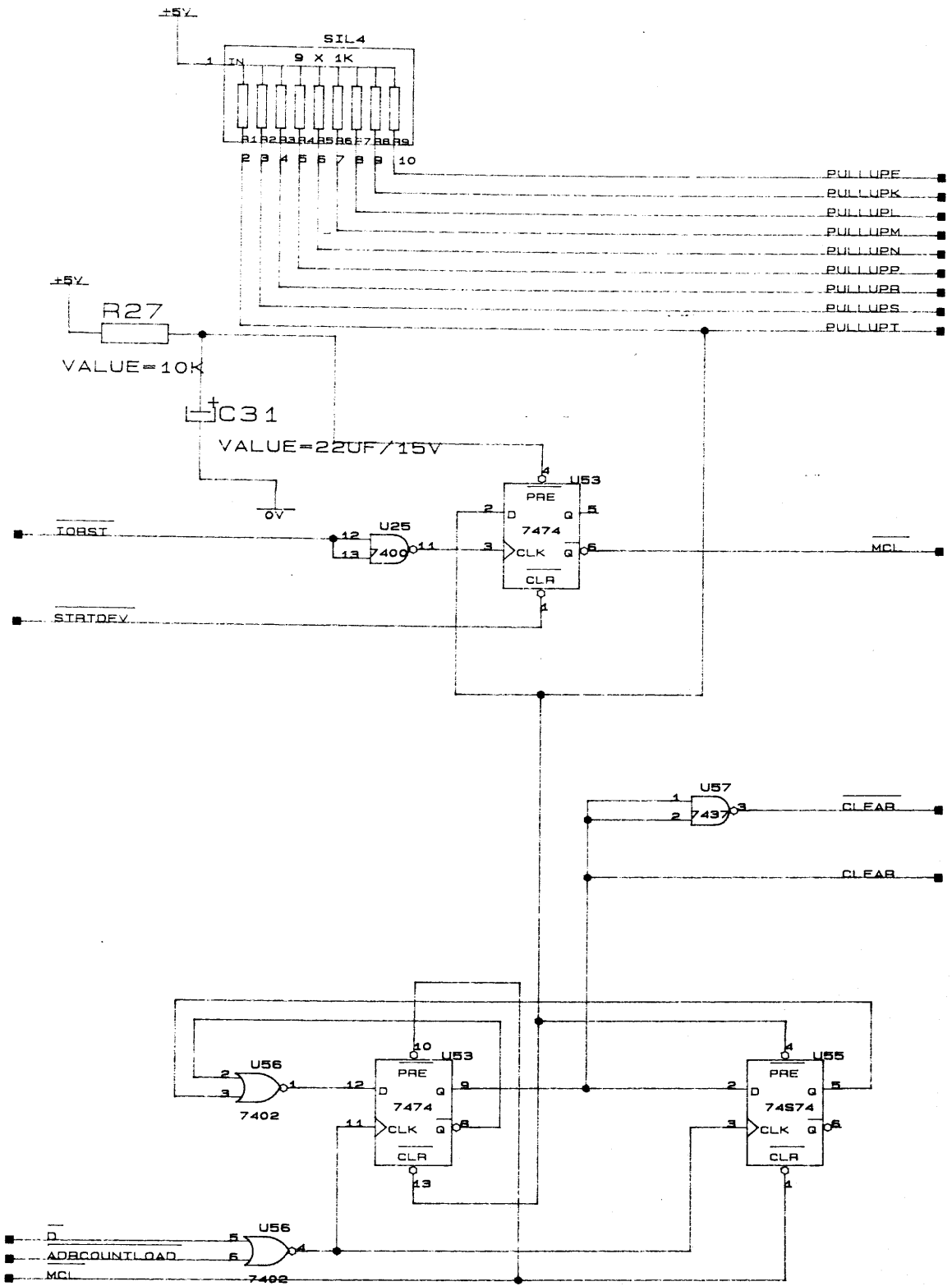
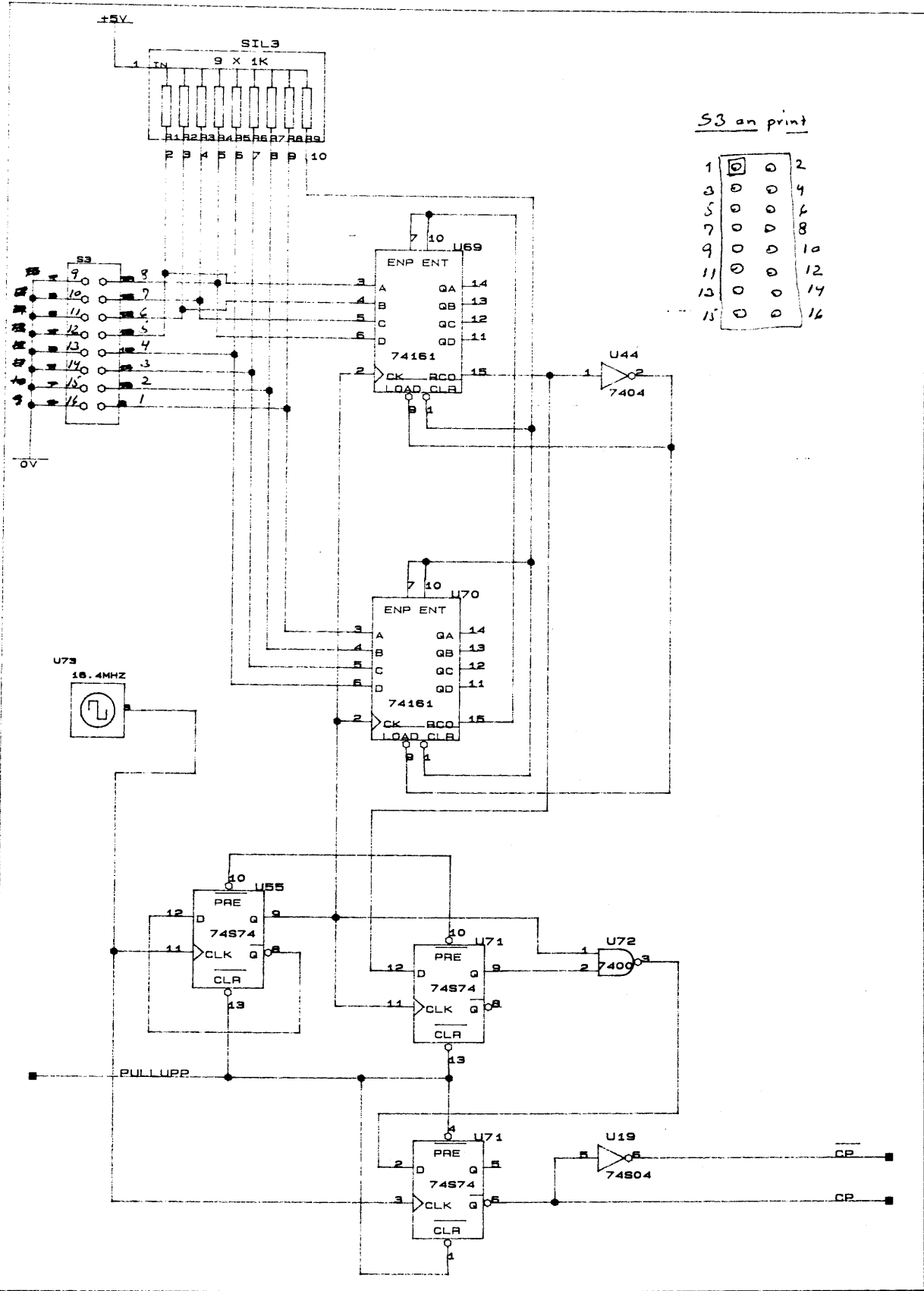


RC Computer



UNIT	DESIGN HM 790116	START CIRCUITS	PAGE
SCU702	DRAWN KNEH 4-2-1989_13: 37		1

RC Computer

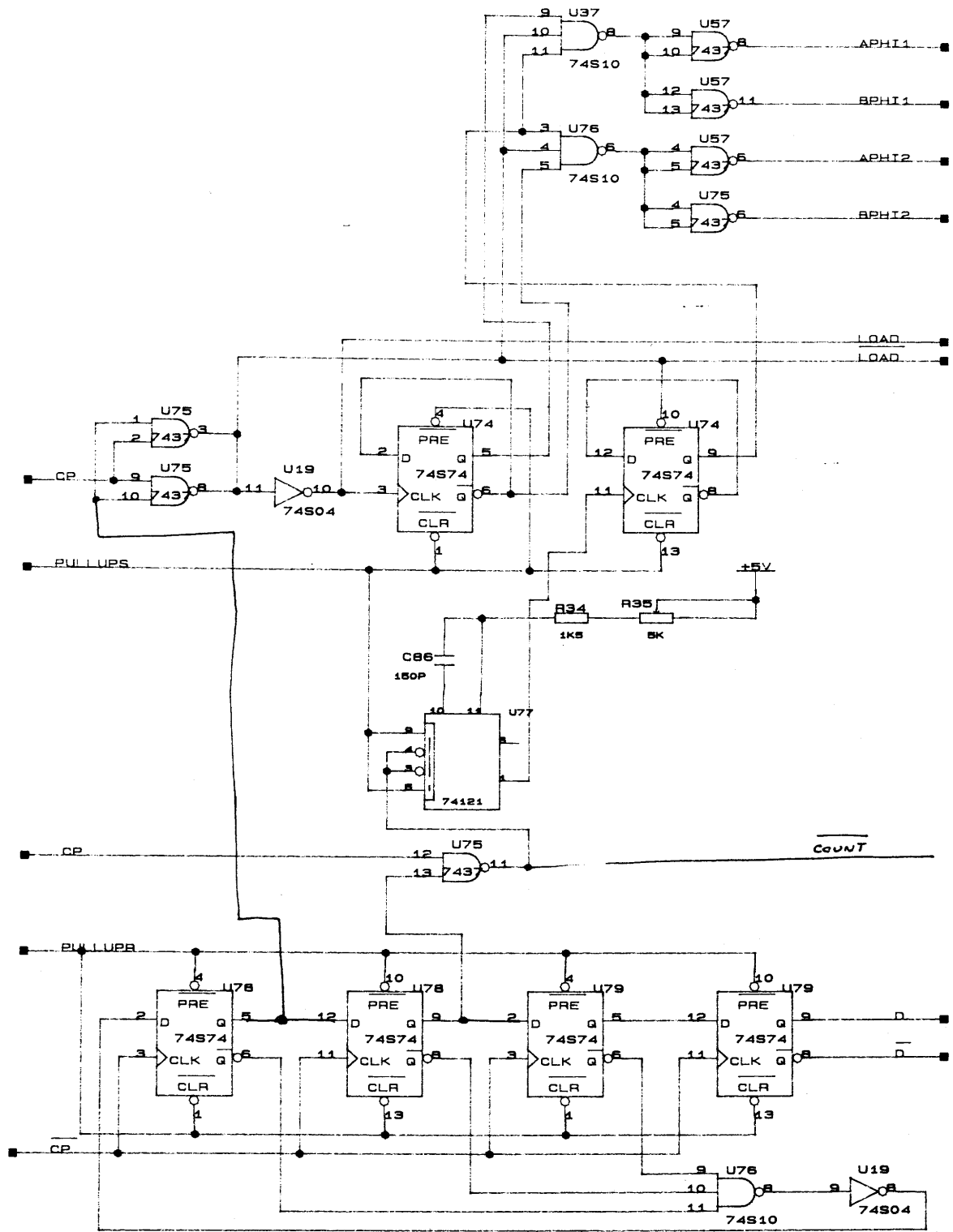


S3 on print

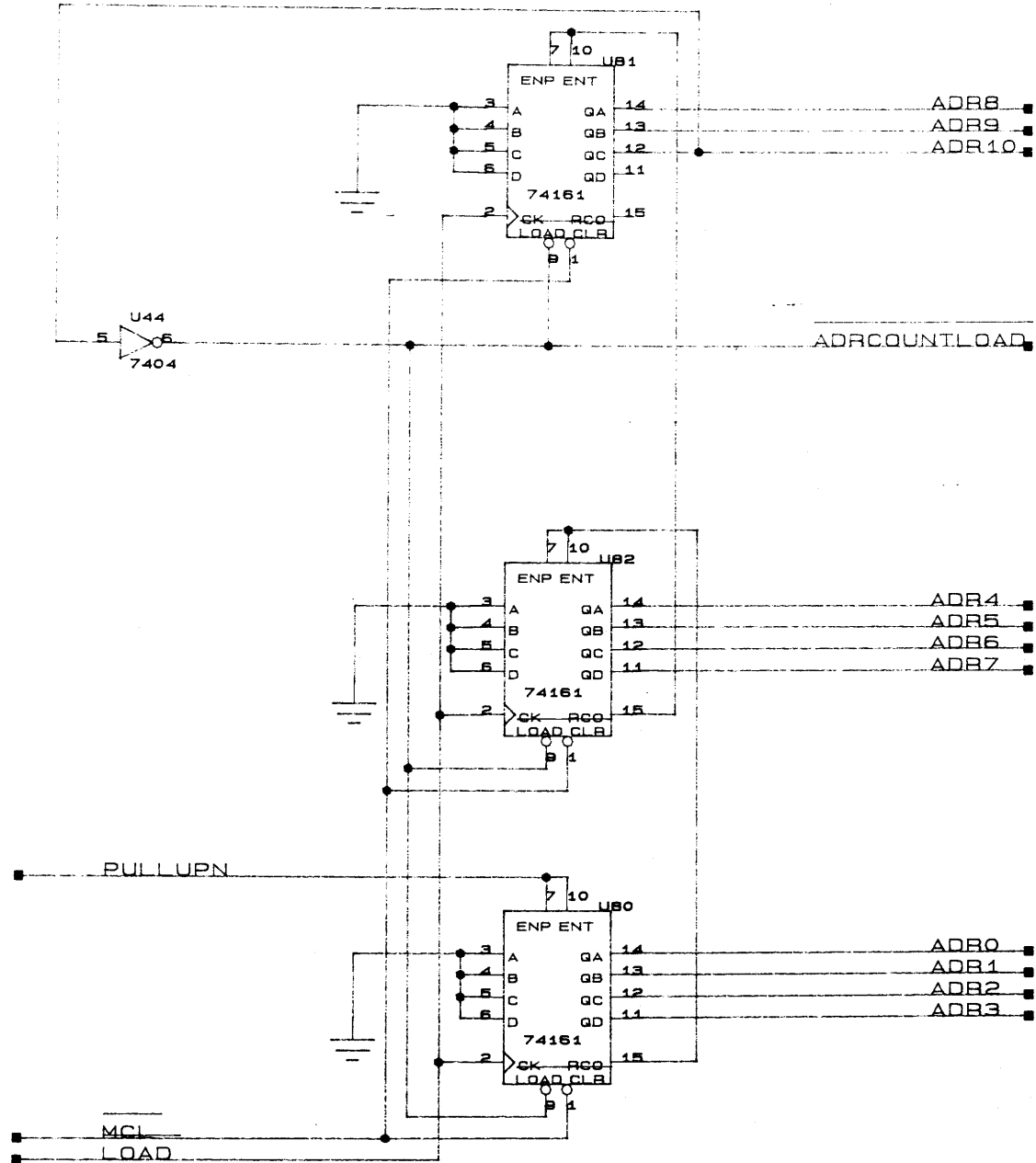
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3	0	0	4
5	0	0	6
7	0	0	8
9	0	0	10
11	0	0	12
13	0	0	14
15	0	0	16

UNIT	DESIGN	TIMING GENERATOR PART 1	PAGE
SCU702	790216 HM		
	DRAWN KNEH		
	4-2-1989_13: 37		2

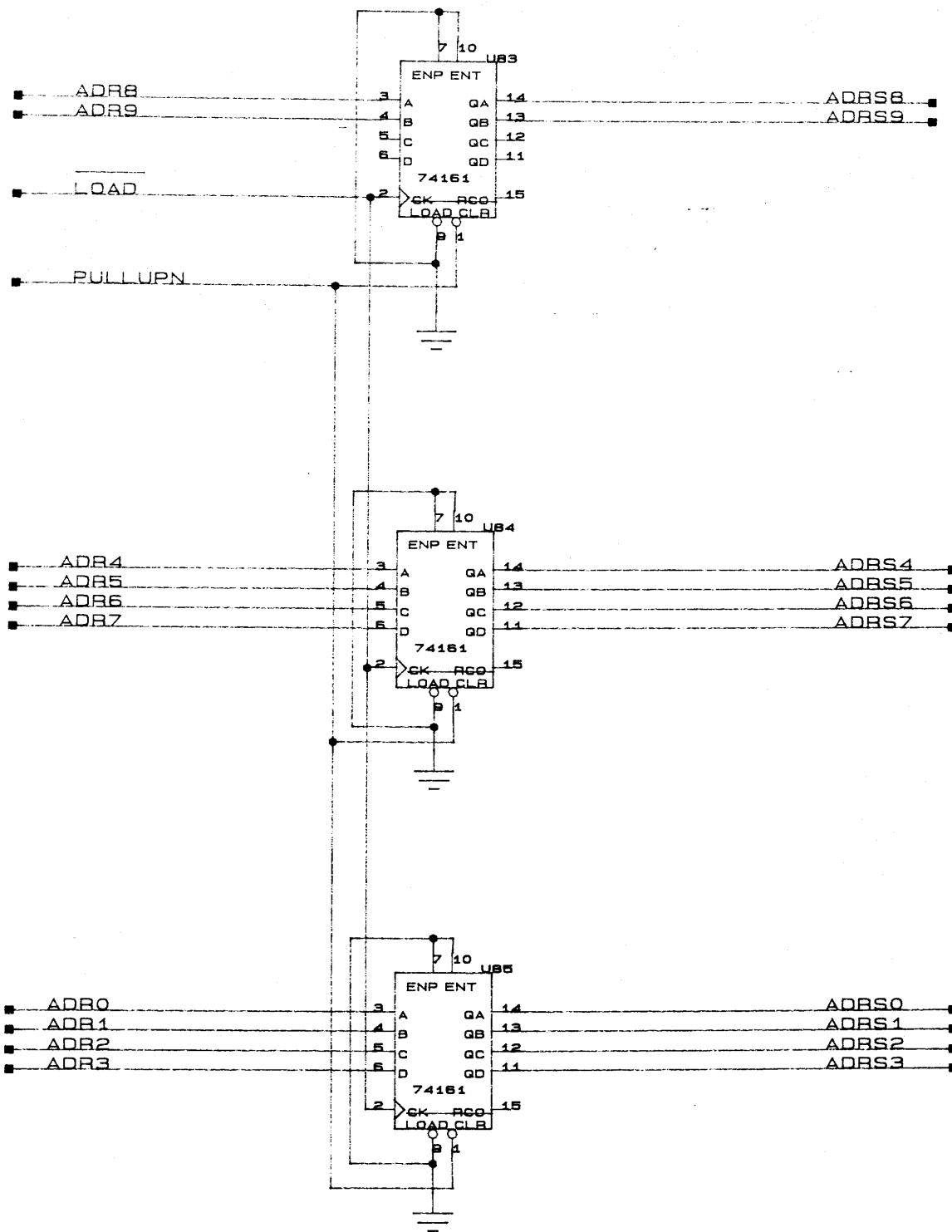
RC Computer



UNIT SCU702	DESIGN 790216 HM	TIMING GENERATOR PART 2	PAGE 3
	DRAWN KNEH 4-2-1989_13: 37		

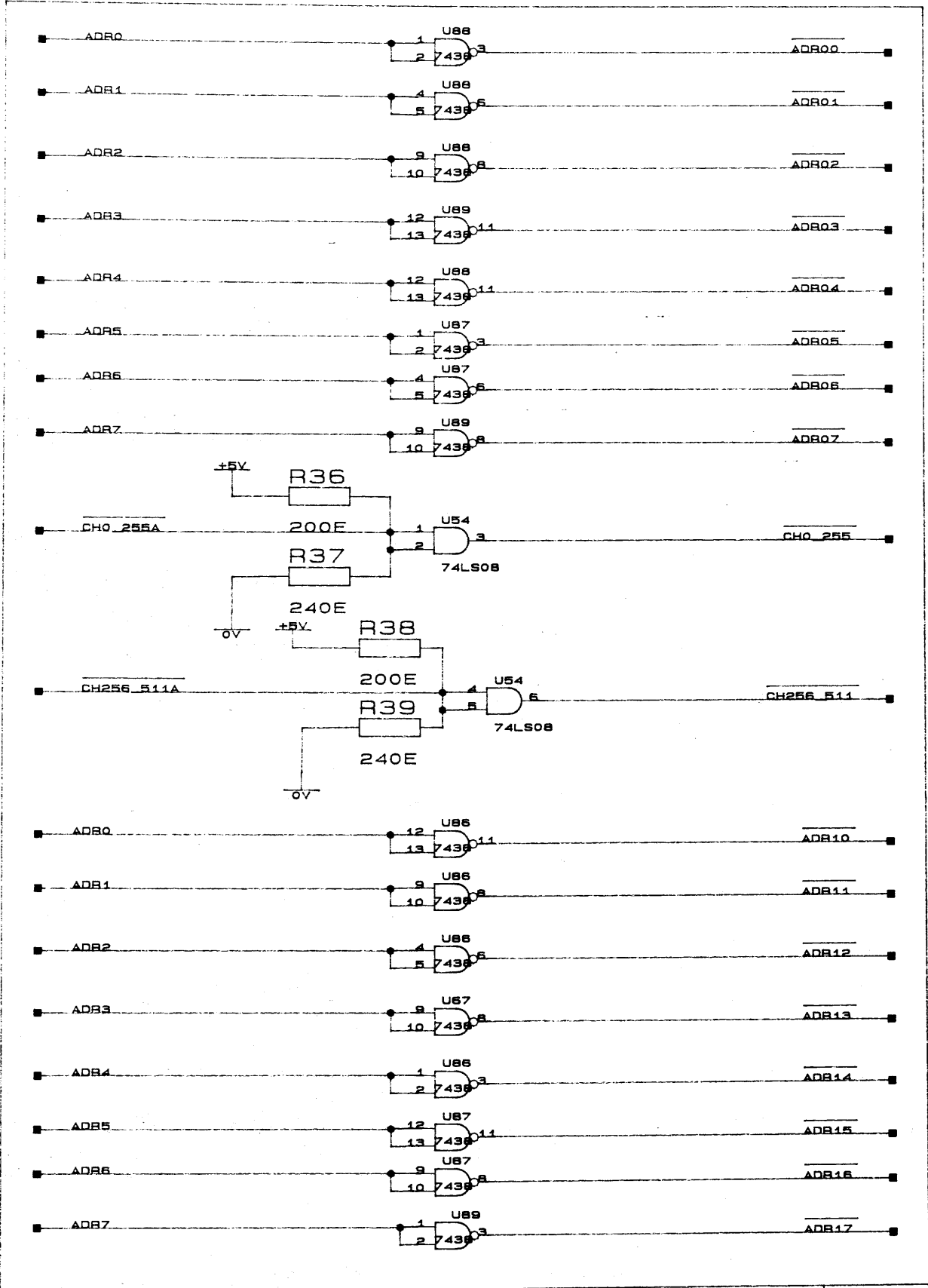


UNIT	DESIGN	ADR COUNTER PART 1	PAGE
SCU702	790219 HM		4
	DRAWN KNEH 4-2-1989_13: 37		



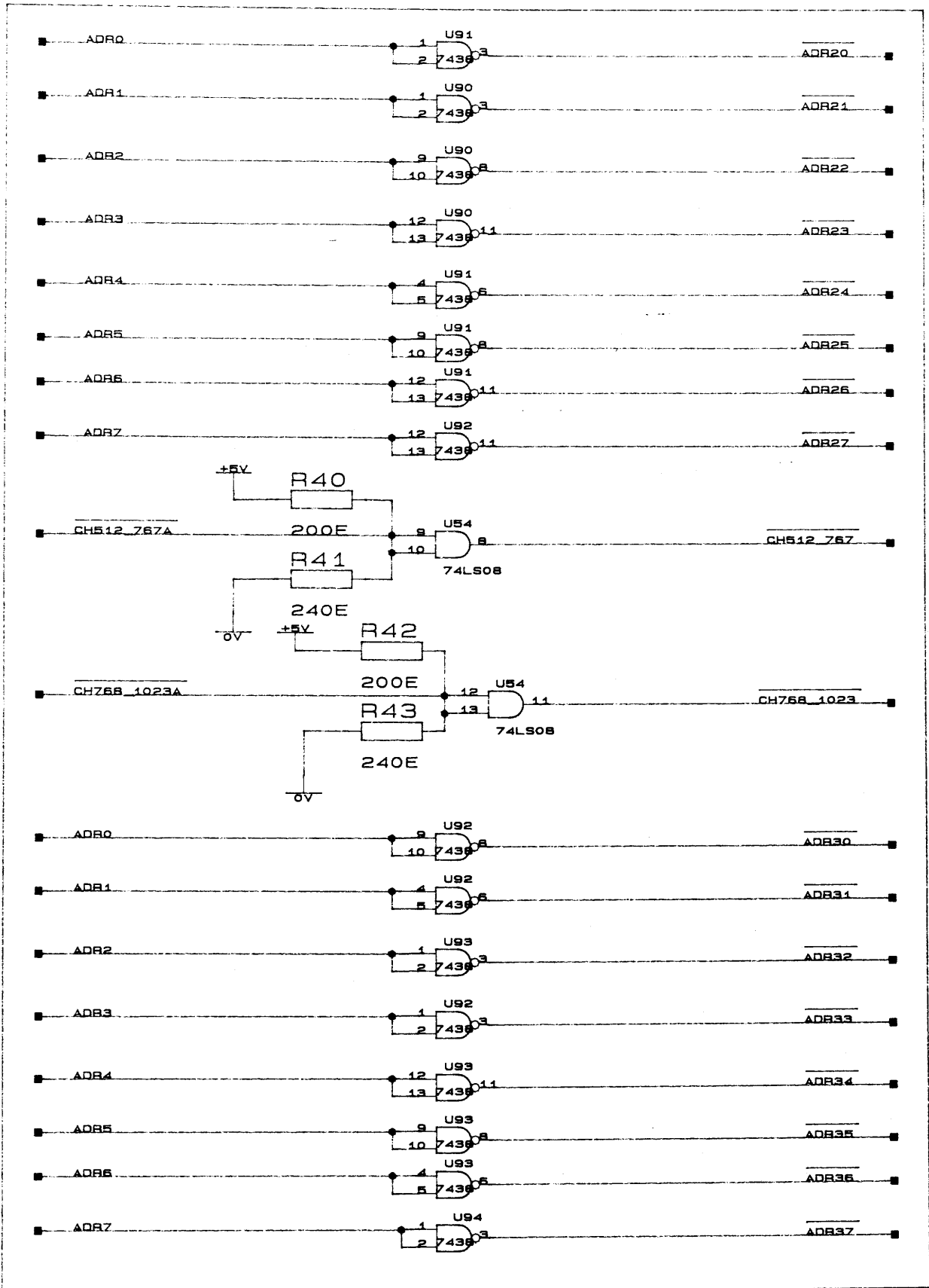
UNIT SCU702	DESIGN 790219 HM	ADRS REGISTER PART 2	PAGE
	DRAWN KNEH 4-2-1989_13: 37		5

RC Computer



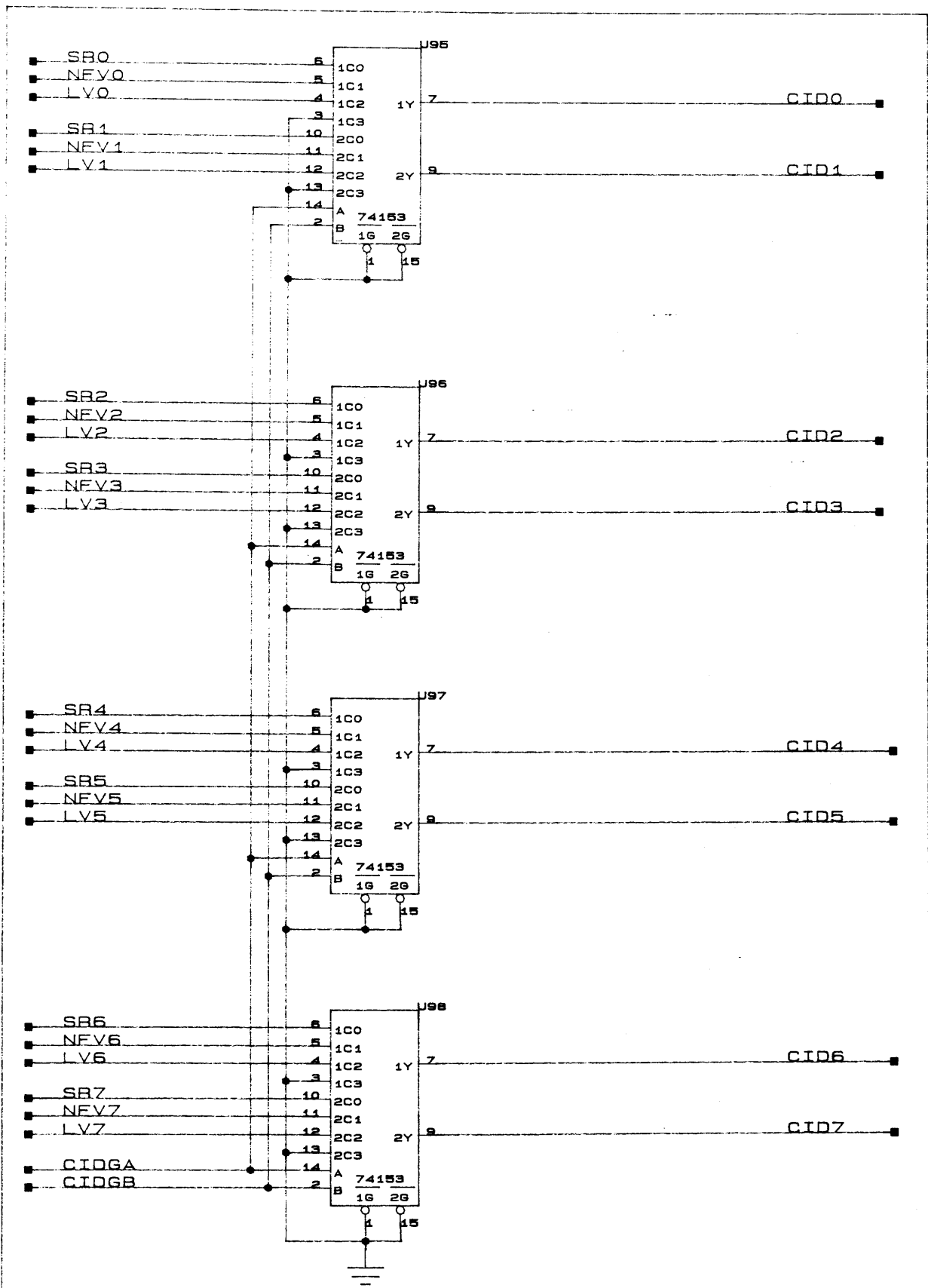
UNIT	DESIGN	ADDRESS DRIVERS LEVEL 0-1	PAGE 6
SCU702	790219		
	DRAWN KNEH 4-2-1989_13: 37		

RC Computer



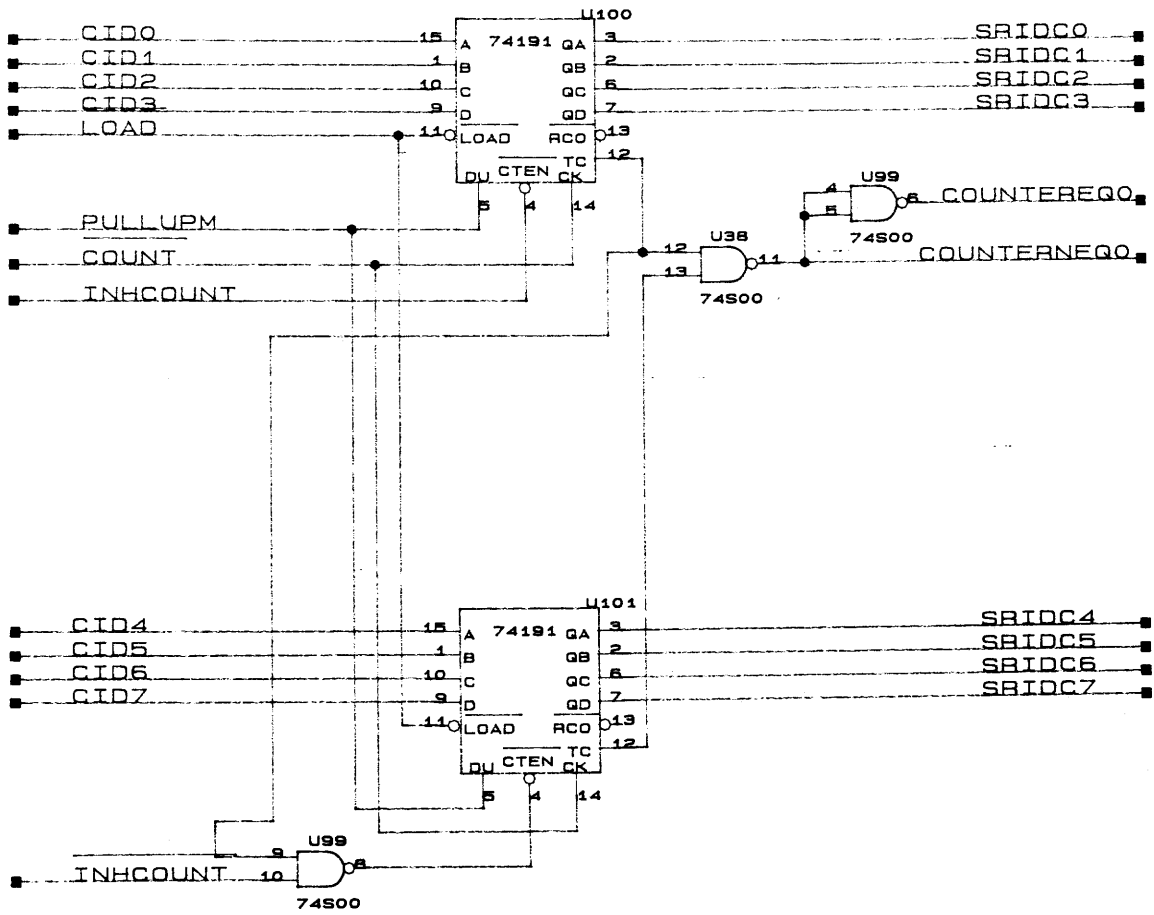
UNIT	DESIGN	ADDRESS DRIVERS LEVEL 2-3	PAGE
SCU702	790219		7
	DRAWN KNEH 4-2-1989_13: 37		

RC Computer

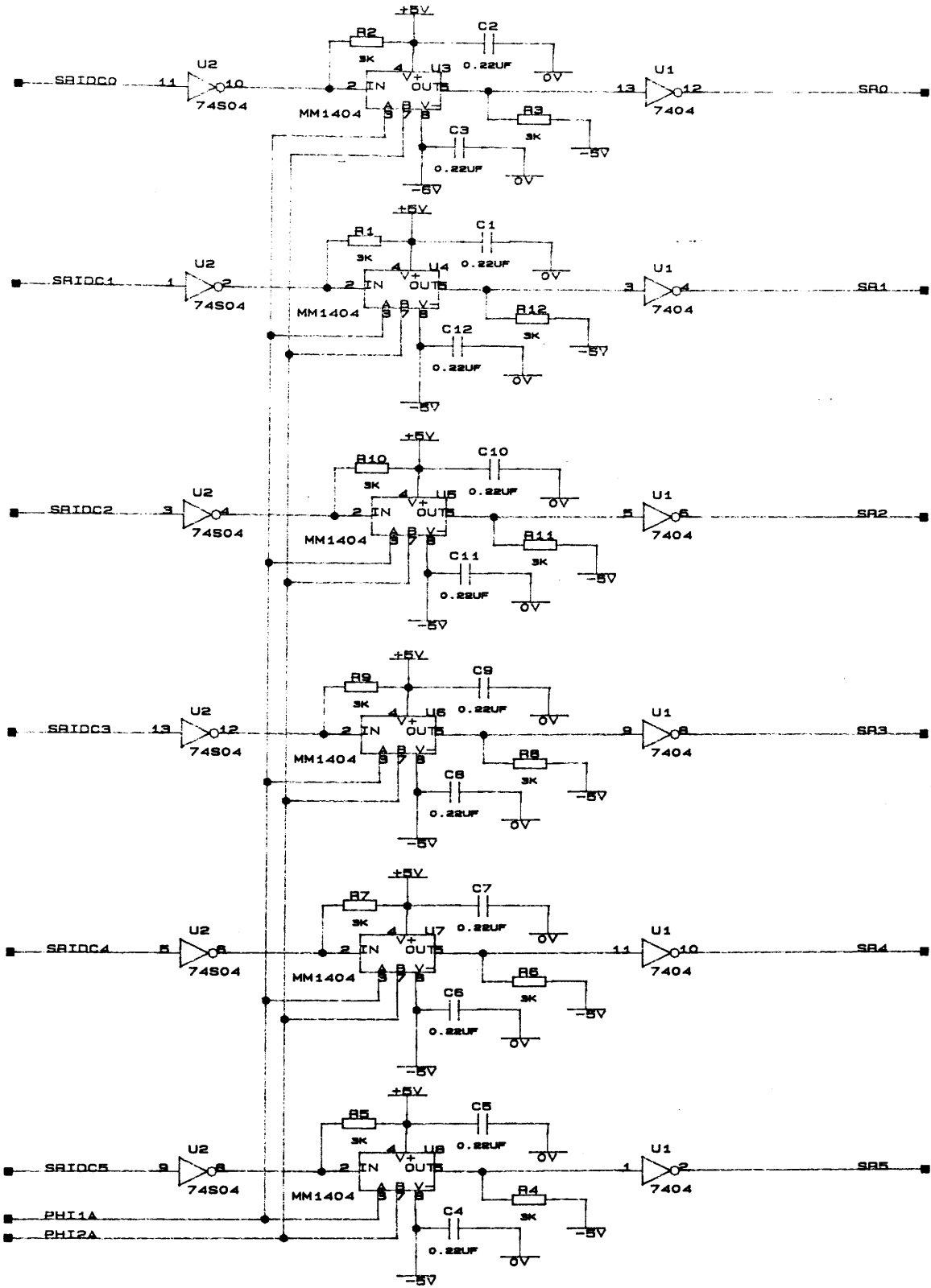


UNIT SCU702	DESIGN 790116 HM	LOCKOUT COUNTER SELECTOR	PAGE 8
	DRAWN KNEH 4-2-1989_13: 37		

RC Computer

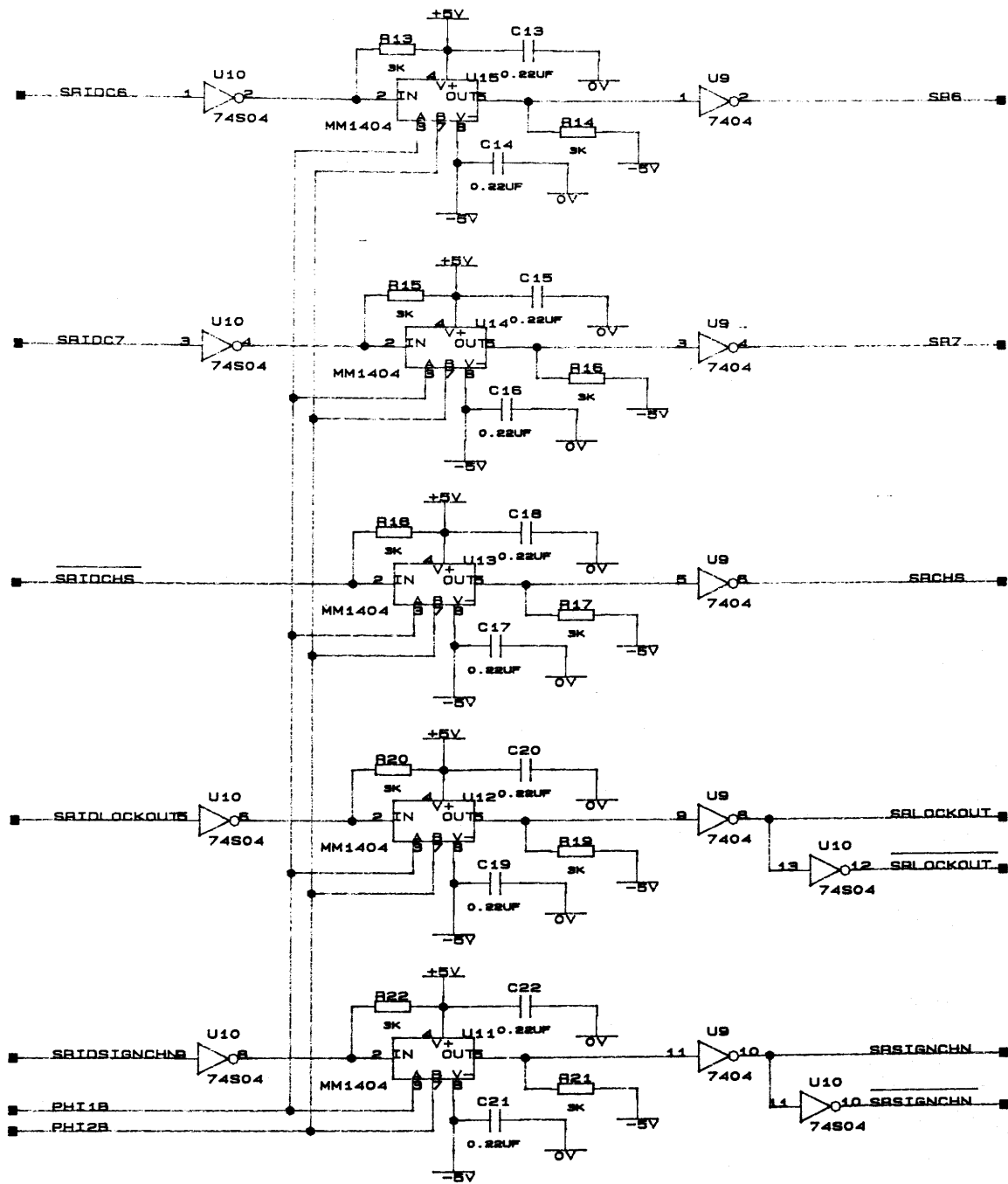


UNIT	DESIGN 790120 HM	LOCKOUT COUNTER PART 1	PAGE
SCU702	DRAWN KNEH		9
	4-2-1989_13: 37		



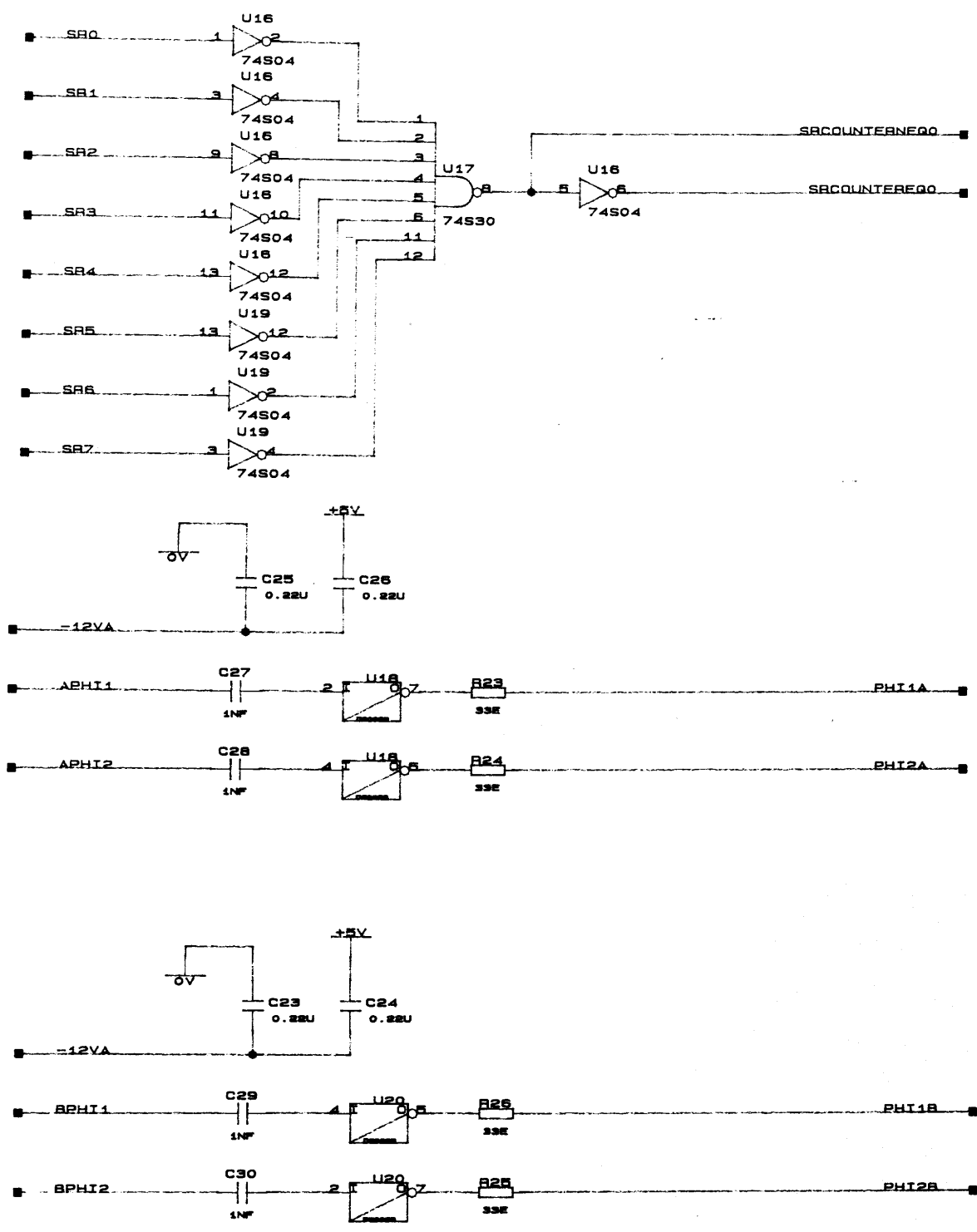
UNIT	DESIGN 790216 HM	SHIFT REGISTER SR (0: 5)	PAGE
SCU702	DRAWN KNEH		10
-2-1989_13: 37			

RC Computer



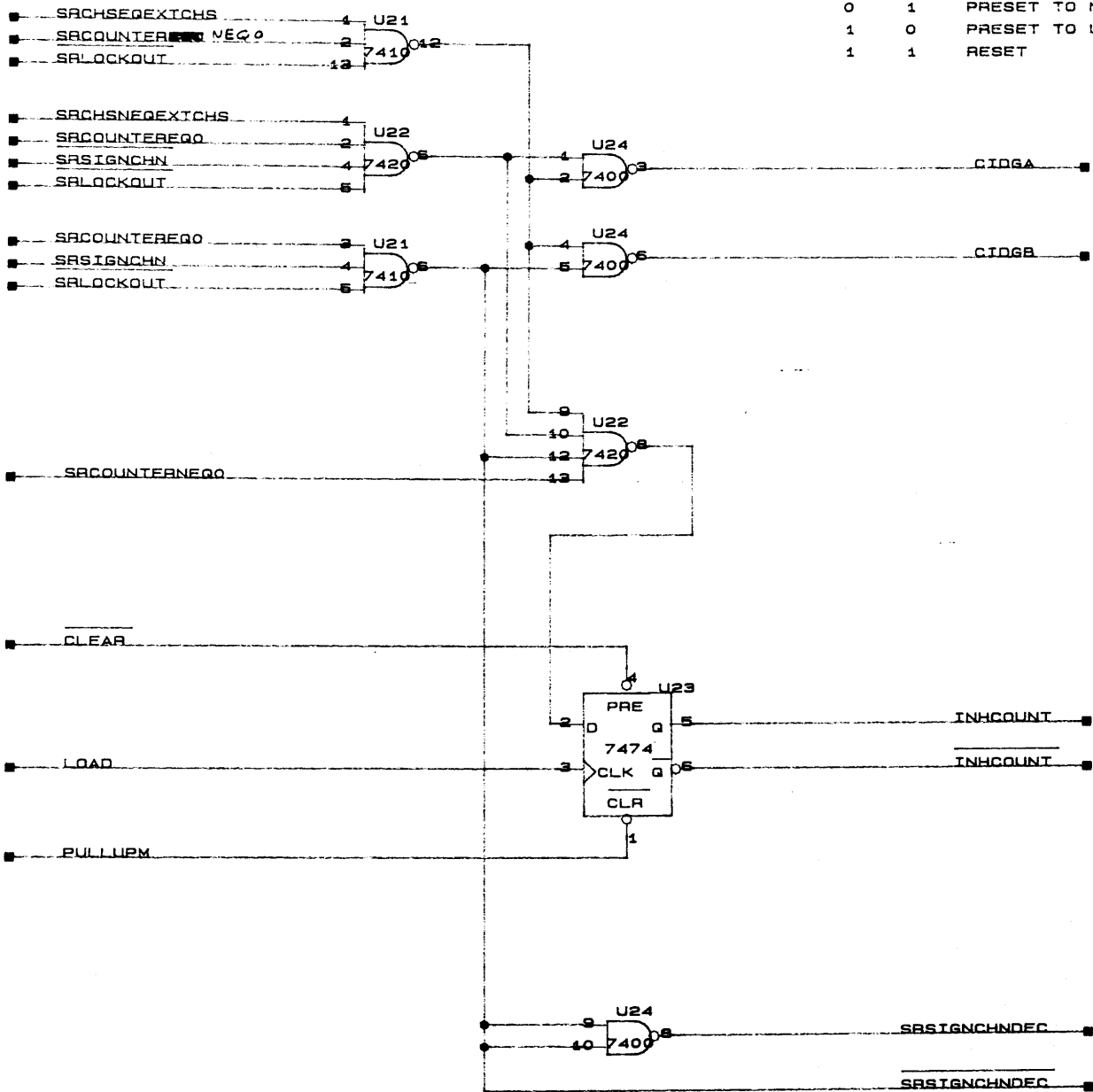
UNIT	DESIGN 790216 HM	SHIFT REGISTER (6: 10)	PAGE
SCU702	DRAWN KNEH		11
4-2-1989_13: 37			

RC Computer

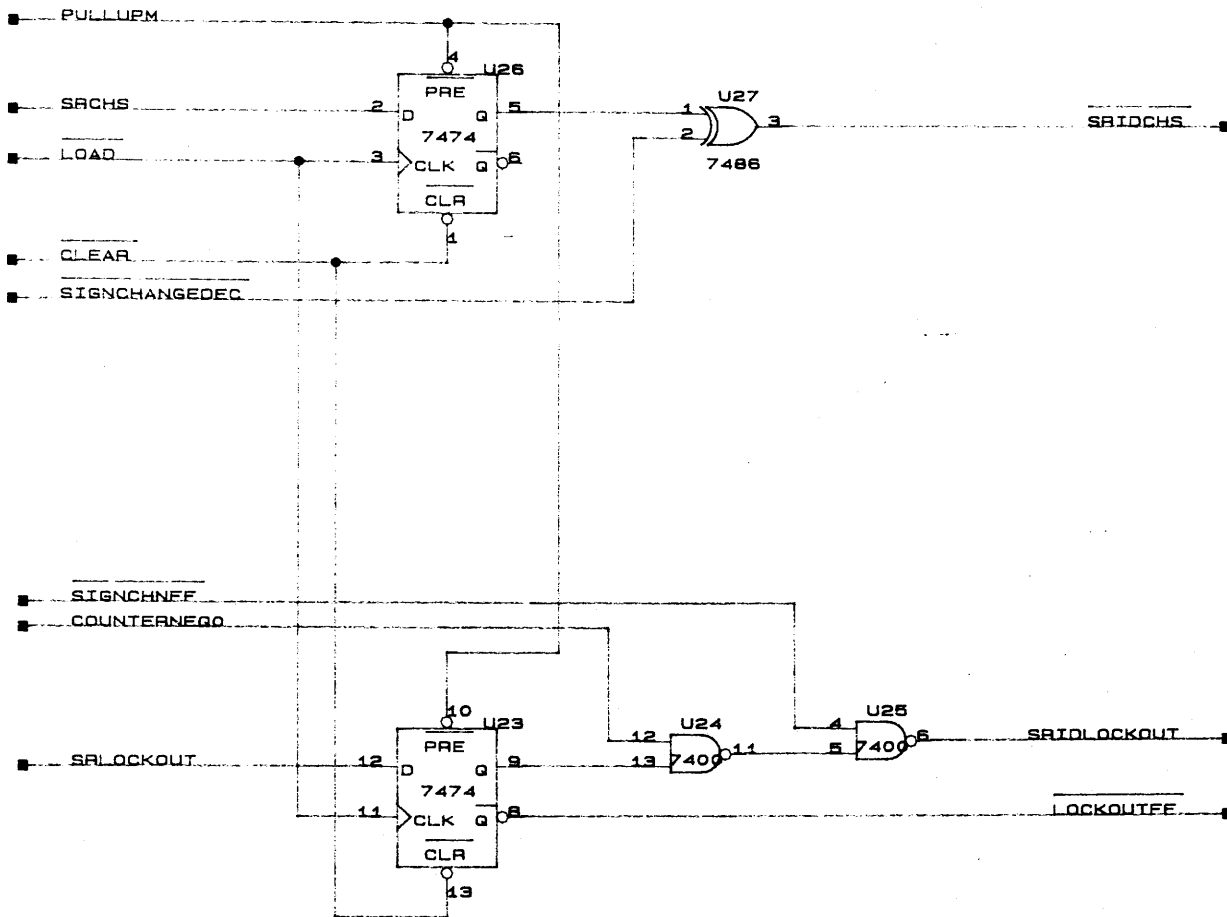


UNIT	DESIGN	SR CLOCK DRIVERS	PAGE 12
SCU702	790216 HM		
	DRAWN KNEH 4-2-1989_13: 37		

0	0	SELECT SR
0	1	PRESET TO NFV
1	0	PRESET TO LV
1	1	RESET



UNIT	DESIGN	CONTROL LOGIC 1A	PAGE
SCU702	790116 HM		13
	DRAWN KNEH 4-2-1989_13:37		

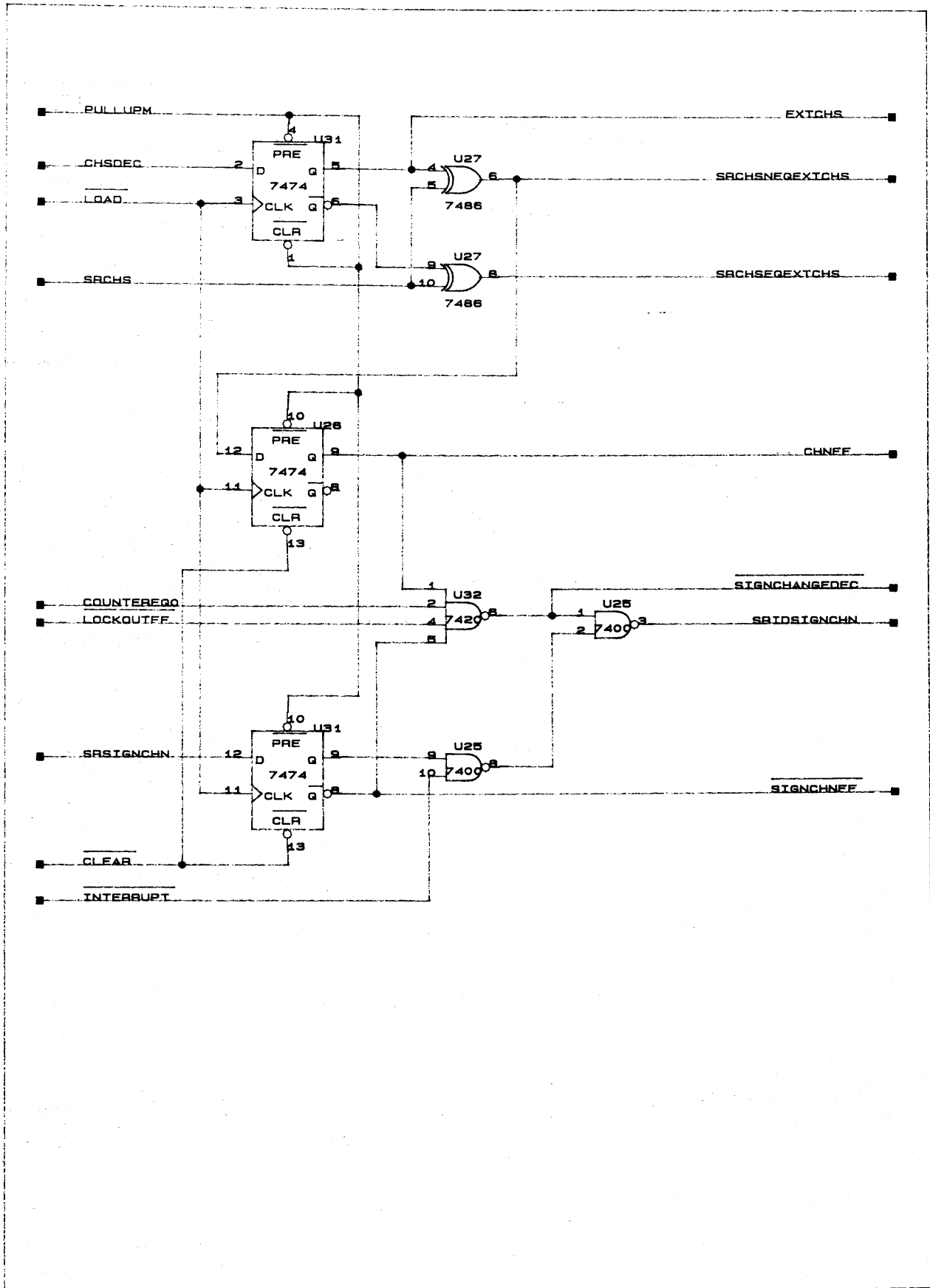


LOCKOUT FJERNES HVIS -, SIGNCHANGEFF & COUNTEREQO
 LOCKOUT PRES IGENNEM HVIS SIGNCHANGEFF I COUNTER<>0
 LOCKOUT GENERERES HVIS SIGNCHANGEFF

CHSFF -, SIGNCHNDEC -, SRIDCHS

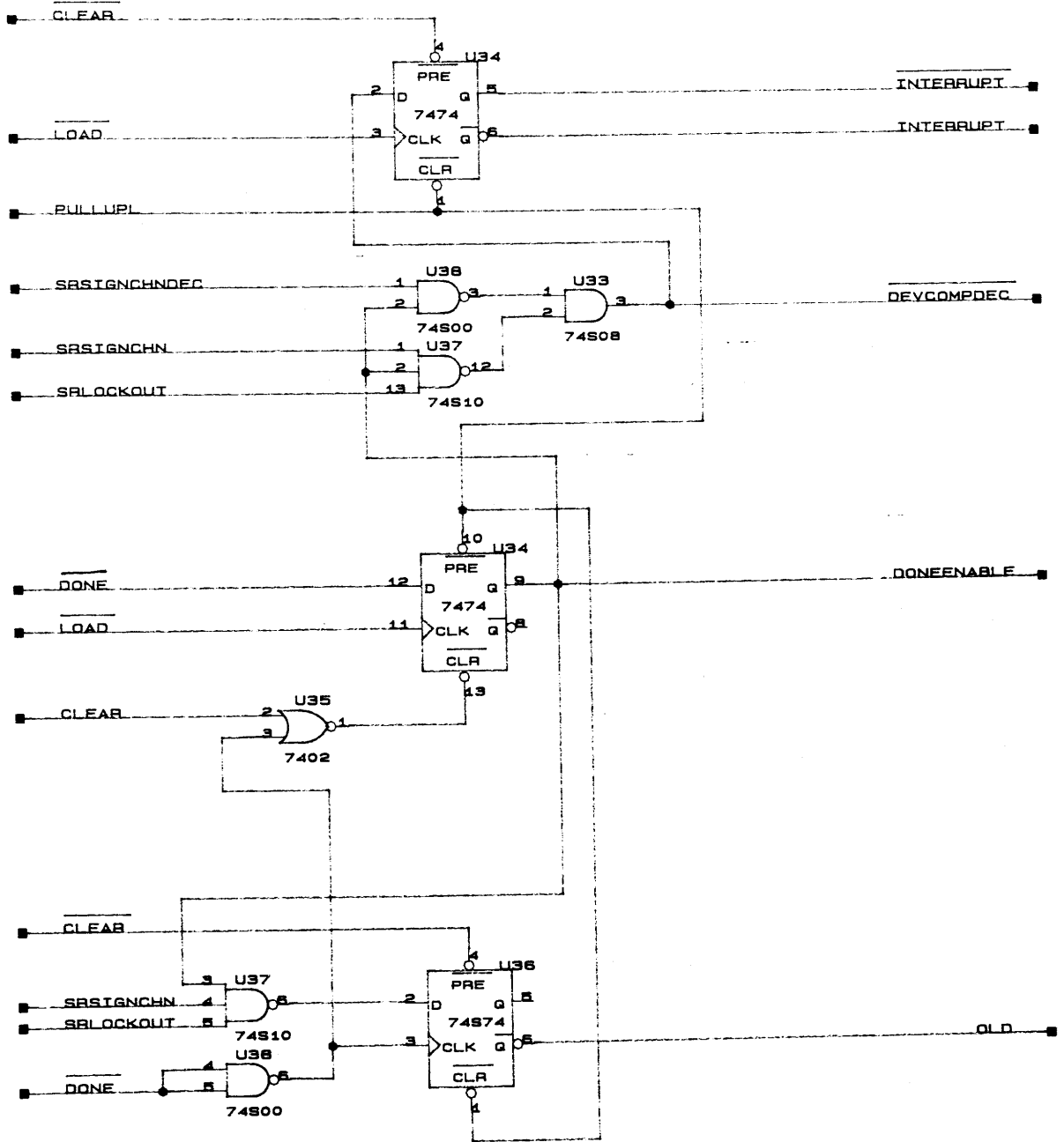
0	0	0
1	0	1
0	1	1
1	1	0

UNIT	DESIGN 790216 HM	CONTROL LOGIC 1B	PAGE
SCU702	DRAWN KNEH 4-2-1989_13: 37		14

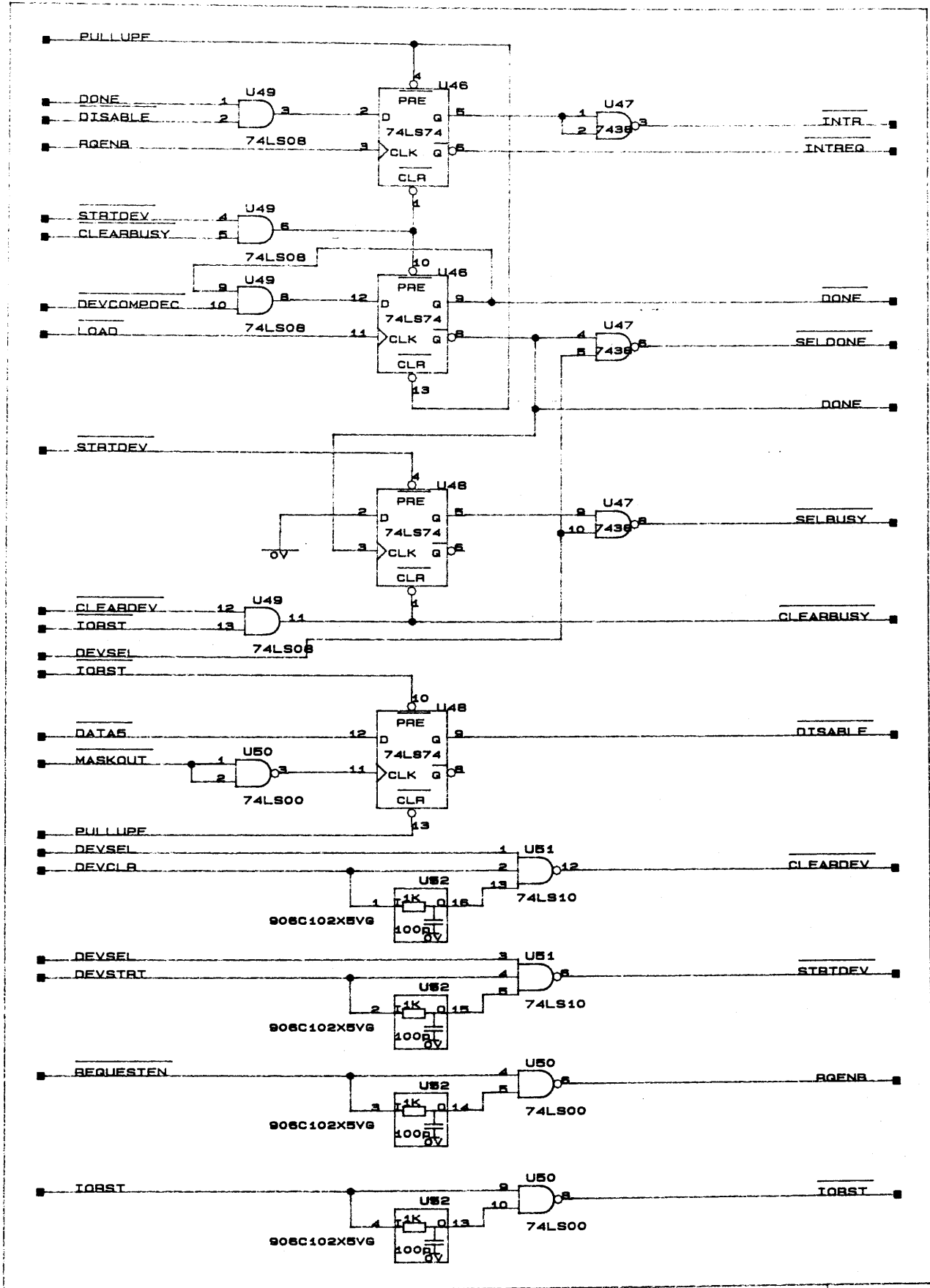


UNIT	DESIGN	CONTROL LOGIC PART 3	PAGE
SCU702	790216 HM		16
	DRAWN KNEH		
	4-2-1989_13: 37		

RC Computer



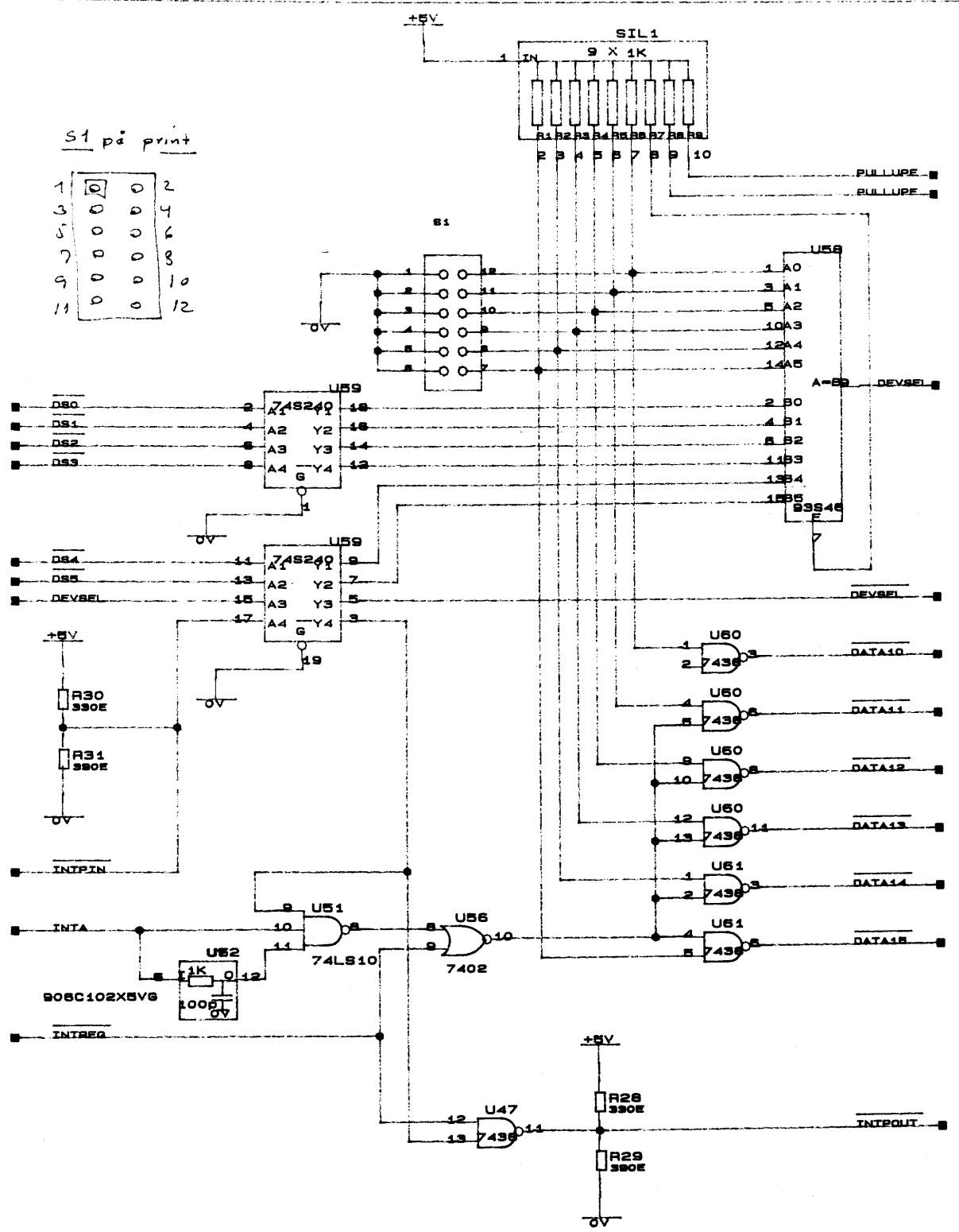
UNIT SCU702	DESIGN 790216 HM	CONTROL LOGIC PART 4	PAGE
	DRAWN KNEH 4-2-1989_13: 37		17



UNIT	DESIGN	CPU INTERFACE 1	PAGE
SCU702	790216 HM		19
	DRAWN KNEH 4-2-1989_13: 37		

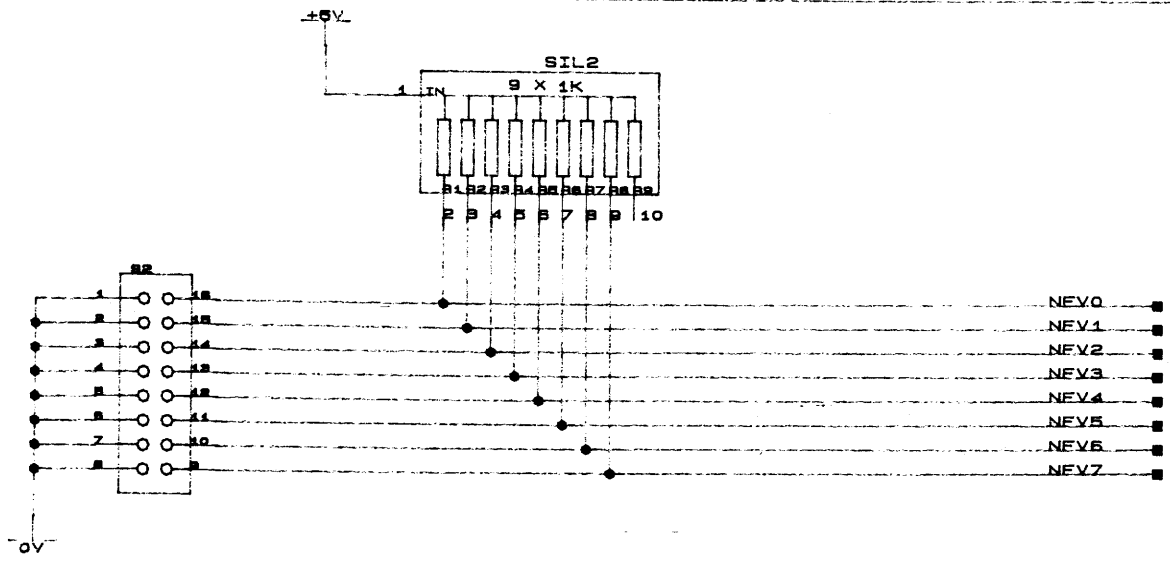
S1 pin print

1	0	2
3	0	4
5	0	6
7	0	8
9	0	10
11	0	12



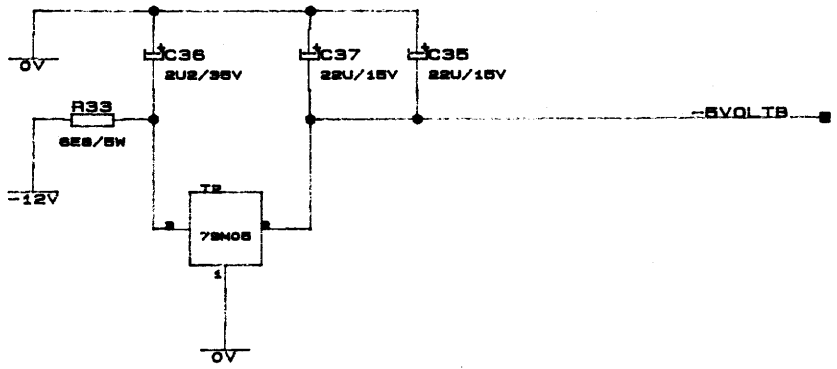
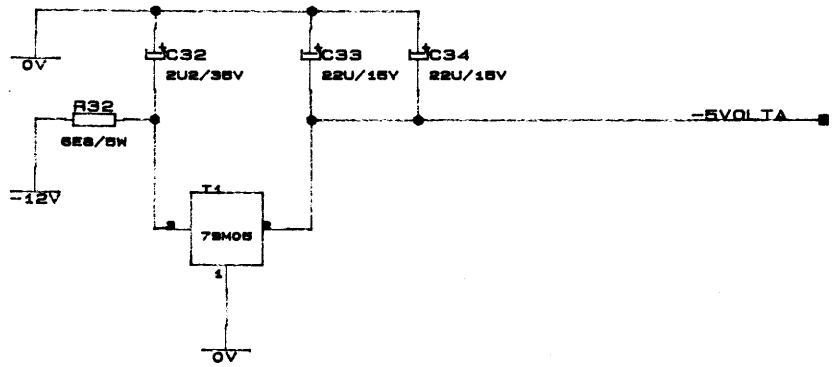
RC Computer

UNIT	DESIGN 790216 HM	CPU INTERFACE PART 2	PAGE 20
SCU702	DRAWN KNEH 4-2-1989_13:37		



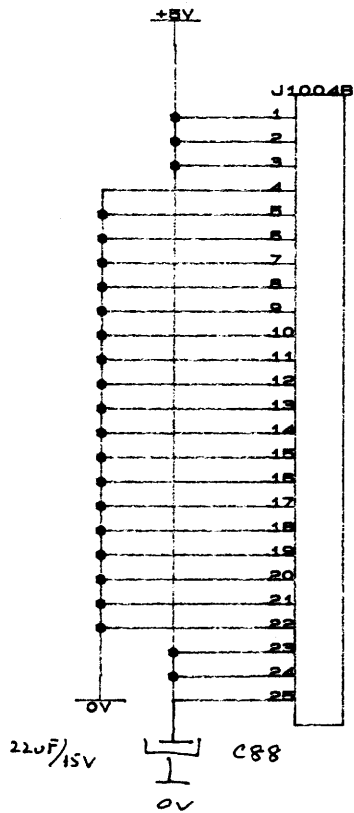
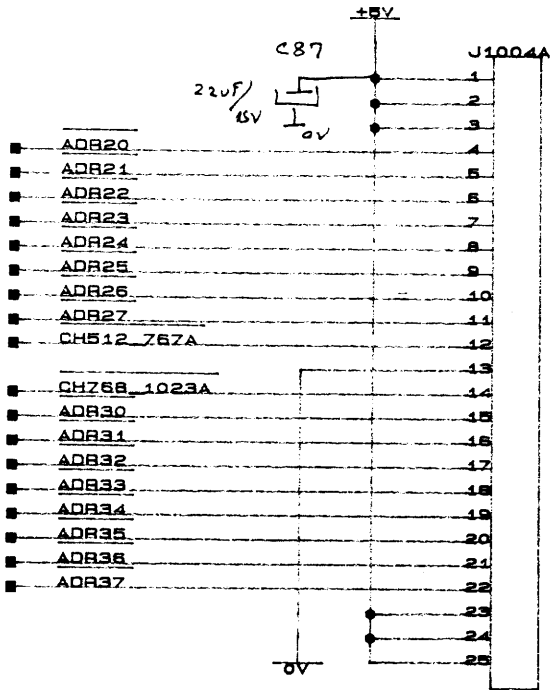
S2 on print

1	0	2
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5	0	6
7	0	8
9	0	10
11	0	12
13	0	14
15	0	16



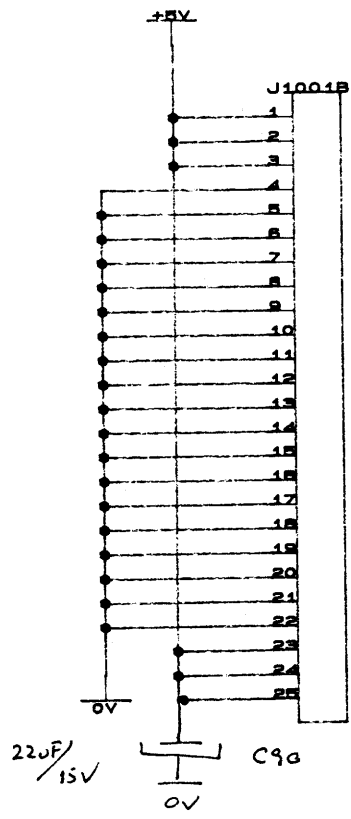
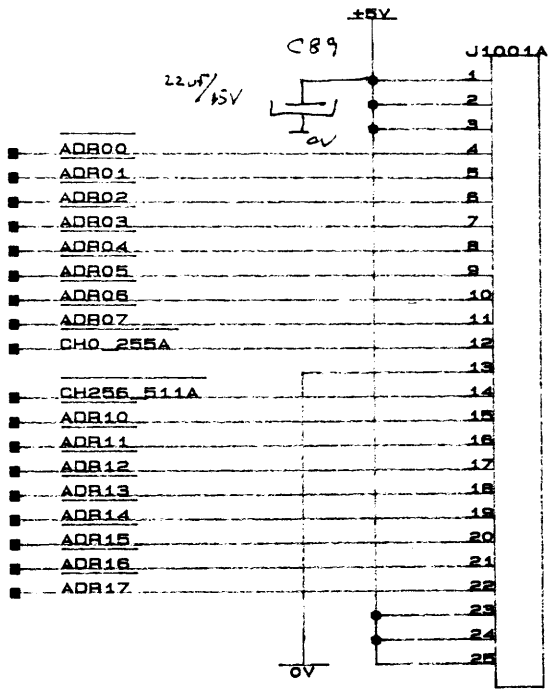
RC Computer

UNIT	DESIGN	NOISE FILTERING VALUE SELECTOR -5V POWER SUPPLY	PAGE 22
SCU702	790625 GR		
	DRAWN KNEH 4-2-1989_13: 37		



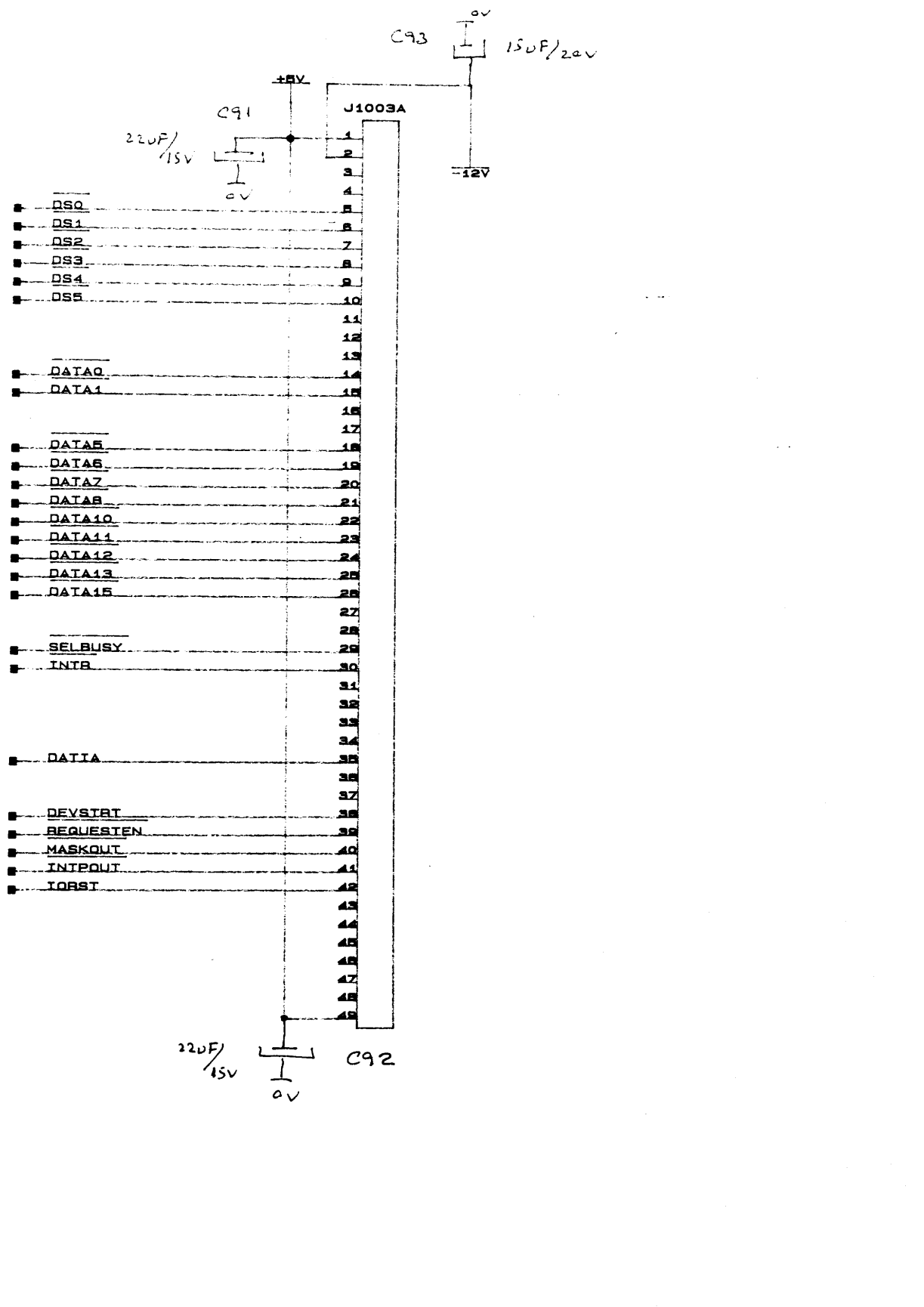
UNIT	DESIGN 890311 KNEH	CONNECTOR J1004	PAGE 23
SCU702	DRAWN KNEH 4-2-1989_13: 37		

RC Computer

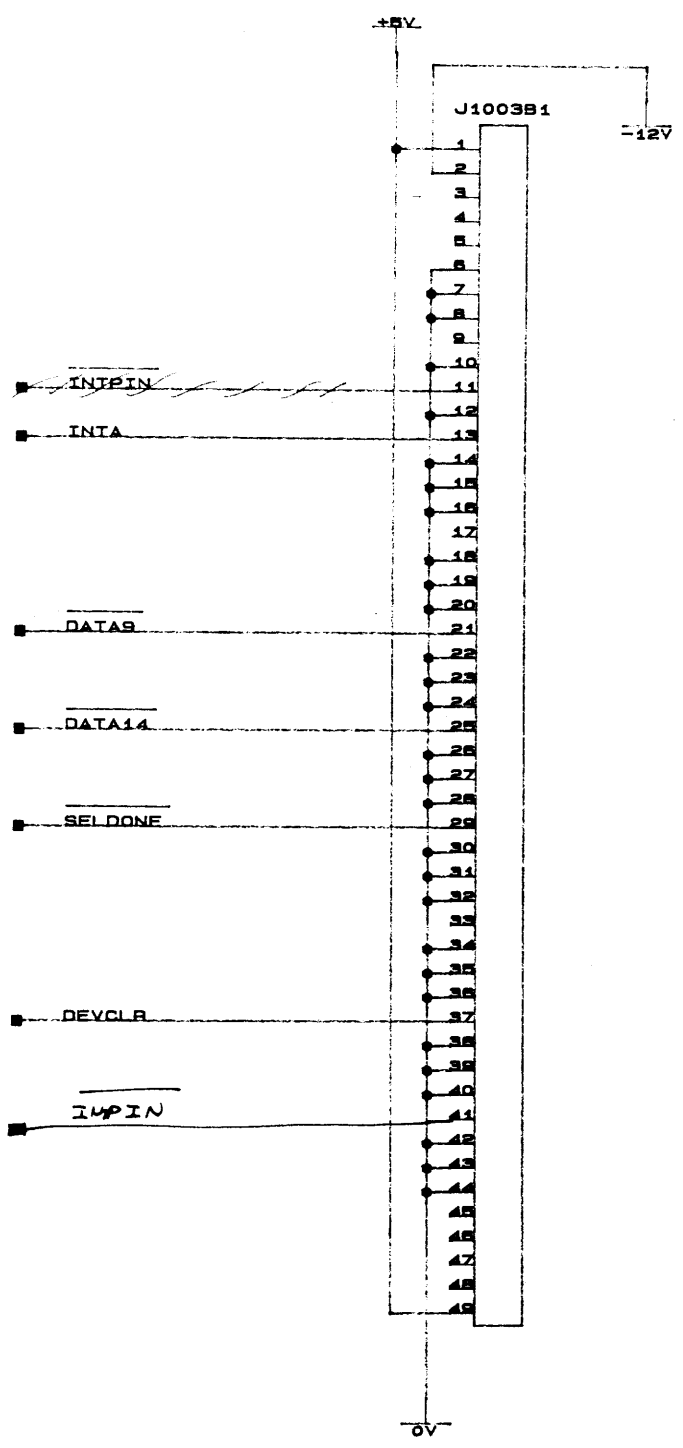


UNIT	DESIGN 890311 KNEH	CONNECTOR J1001	PAGE 24
SCU702	DRAWN KNEH 4-2-1989_13: 37		

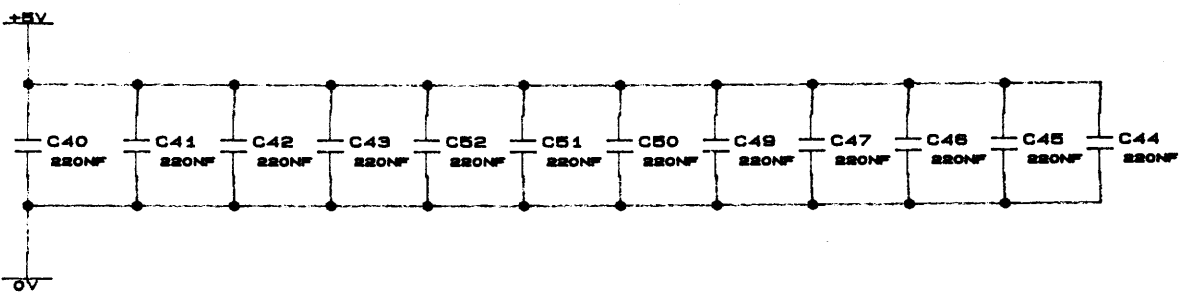
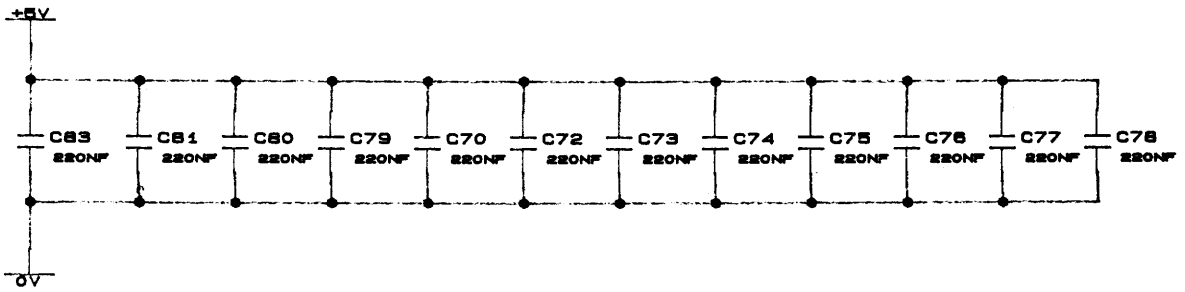
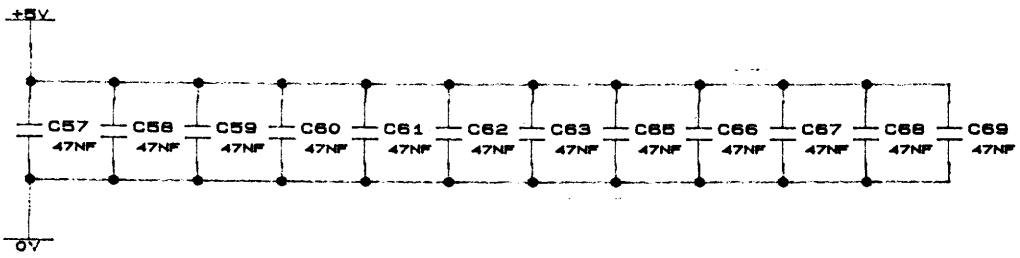
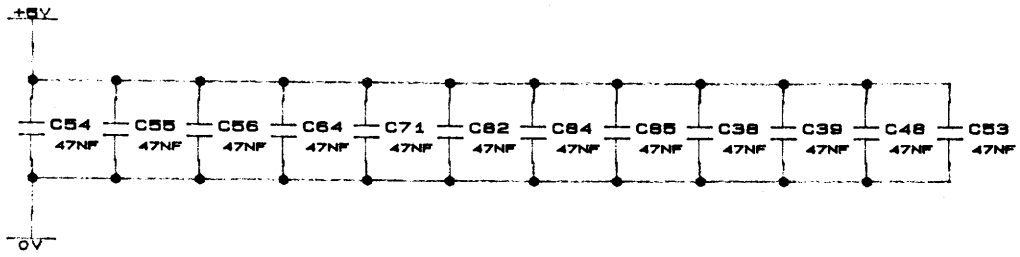
RC Computer



UNIT	DESIGN 890311 KNEH	CONNECTOR J1003A	PAGE 25
SCU702	DRAWN KNEH 4-2-1989_13: 37		

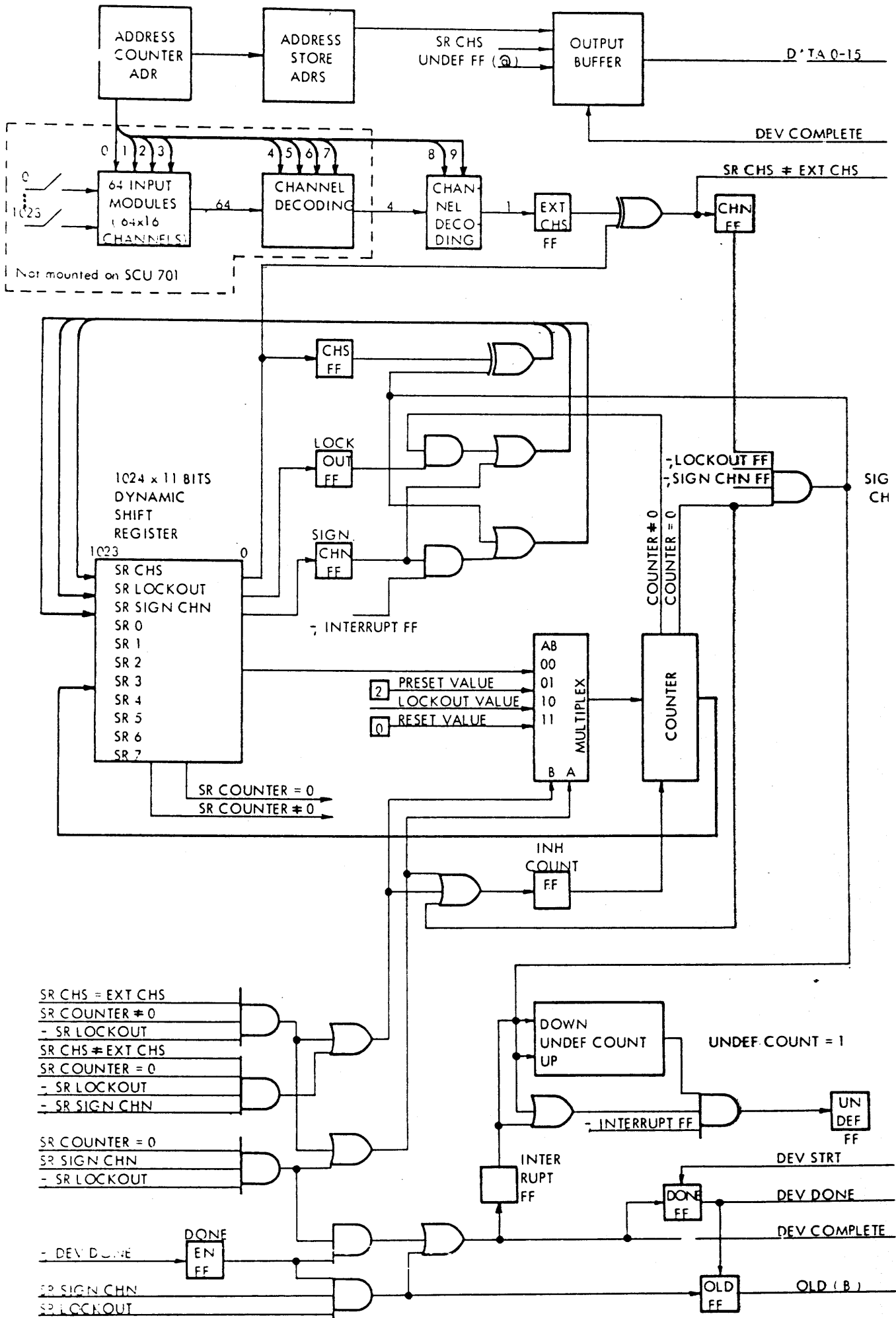


UNIT	DESIGN 890311 KNEH	CONNECTOR J1003B	PAGE 26
SCU702	DRAWN KNEH 4-2-1989_13: 37		



RC Computer

UNIT SCU702	DESIGN 890312 KNEH	+5V DECOUPLING CAPACITORS	PAGE 27
	DRAWN KNEH 4-2-1989_13: 37		



791113 GR 810518 GR 791113 LLM

791926 GR

791026 LEC 810518 GR

5 103, 113, 123 ADPS 0-9

3 48-8 ; LOAD

3 48-6 ; COUNT

13 89-11 SP. SIGN CHN DEC

21 101, 111, 121 OUT BF CH NO

19 72-5 BUSY

19 71-8 DONE

17 28-5 DONE ENABLE

17 13-3 ; DEV COMP DEC

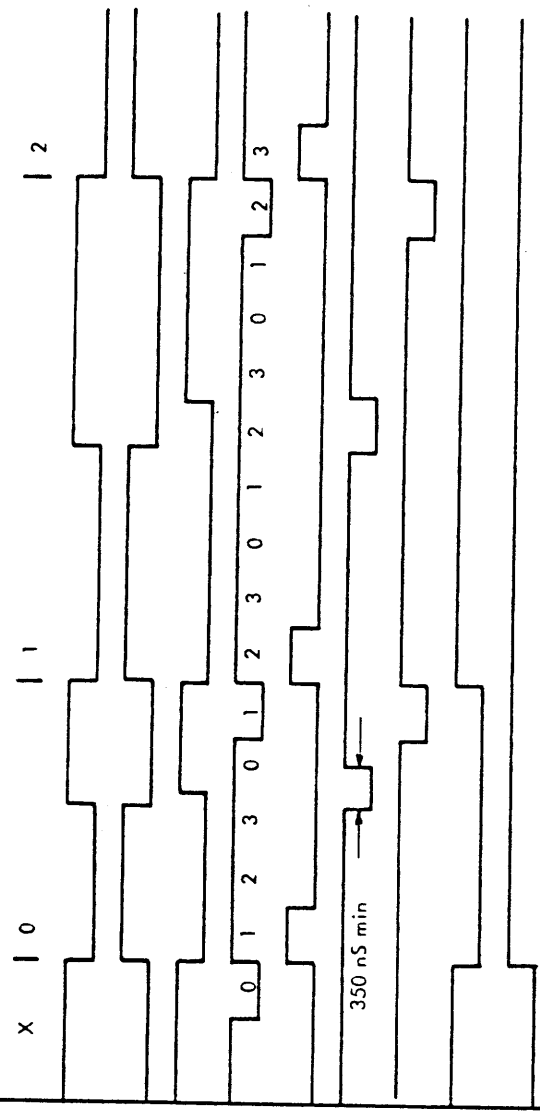
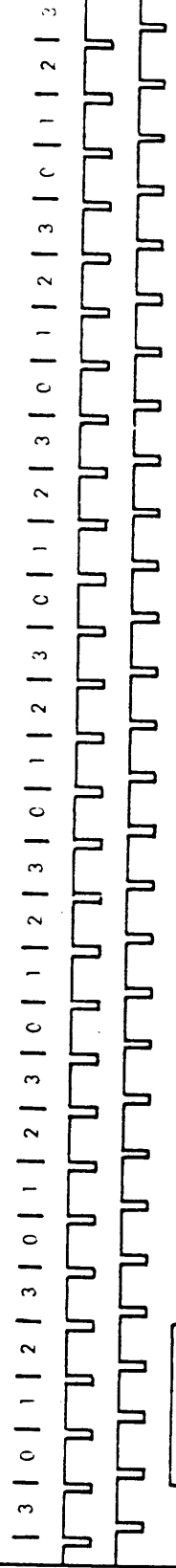
17 27-8 INTERRUPT

19 61-6 ; START DEV

17 15-6 ; OLD EN

17 14-6 OLD

21 102-11 OUT BF UNDEF



Timing Chart

791112 GR

810518 GR

8.2 MHz

τ ~ 122 ns

3 69-5

SCU TC1

4 13-9

3 69-9

3 70-5

3 70-9

2 31-41 TIMING COUNTER OSV

2 99-8 CP

2 30-2 ; CP

3 48-6 ; COUNT

3 48-8 ; LOAD

1 37-5 MCL

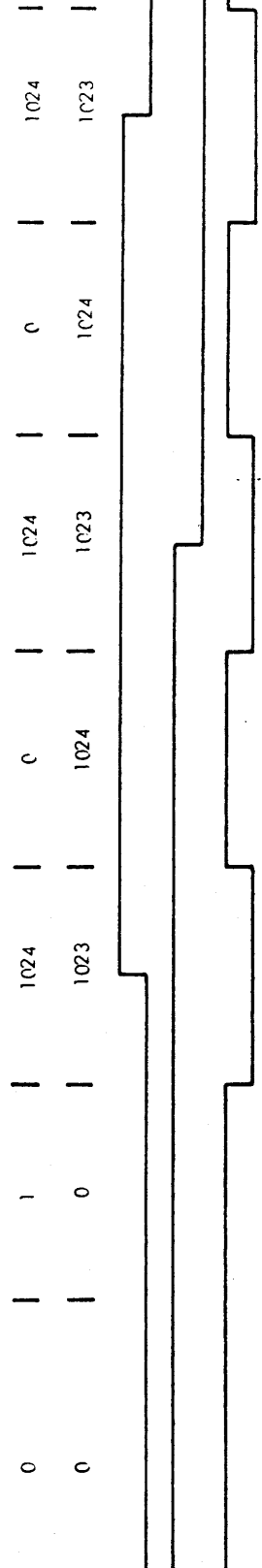
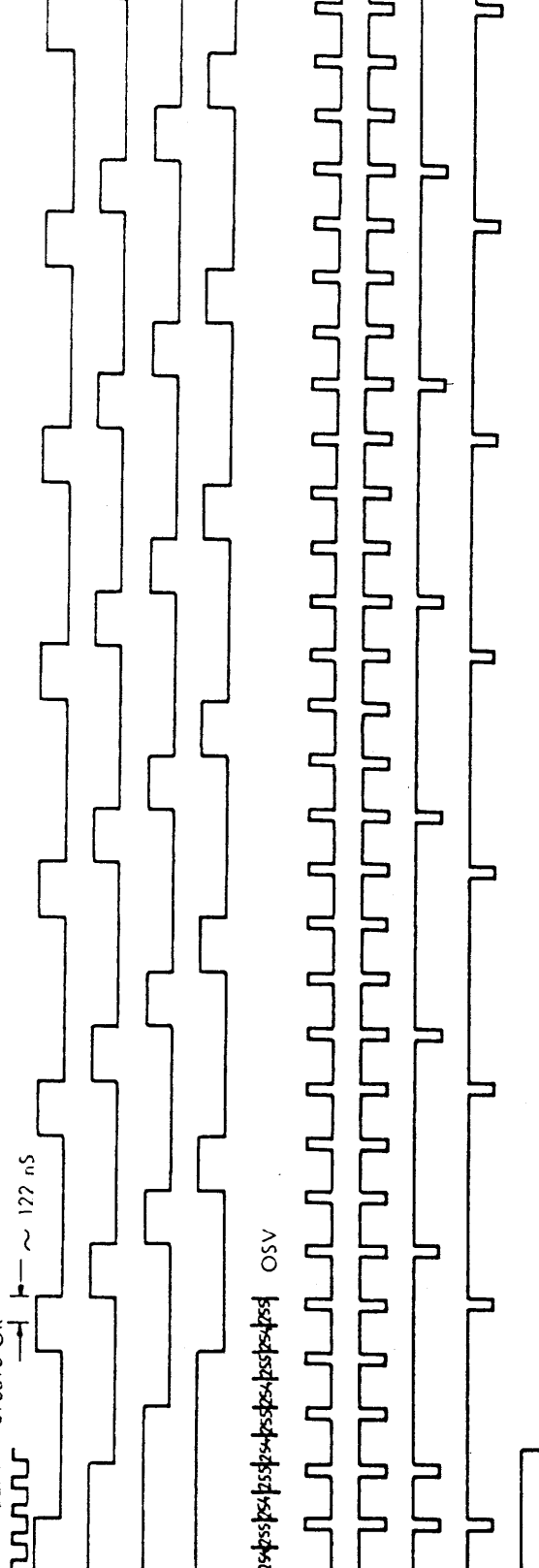
4 104, 114, 124 ADR 0-10

5 103, 113, 123 ADR 5 0-9

1 44-5 RELEASE

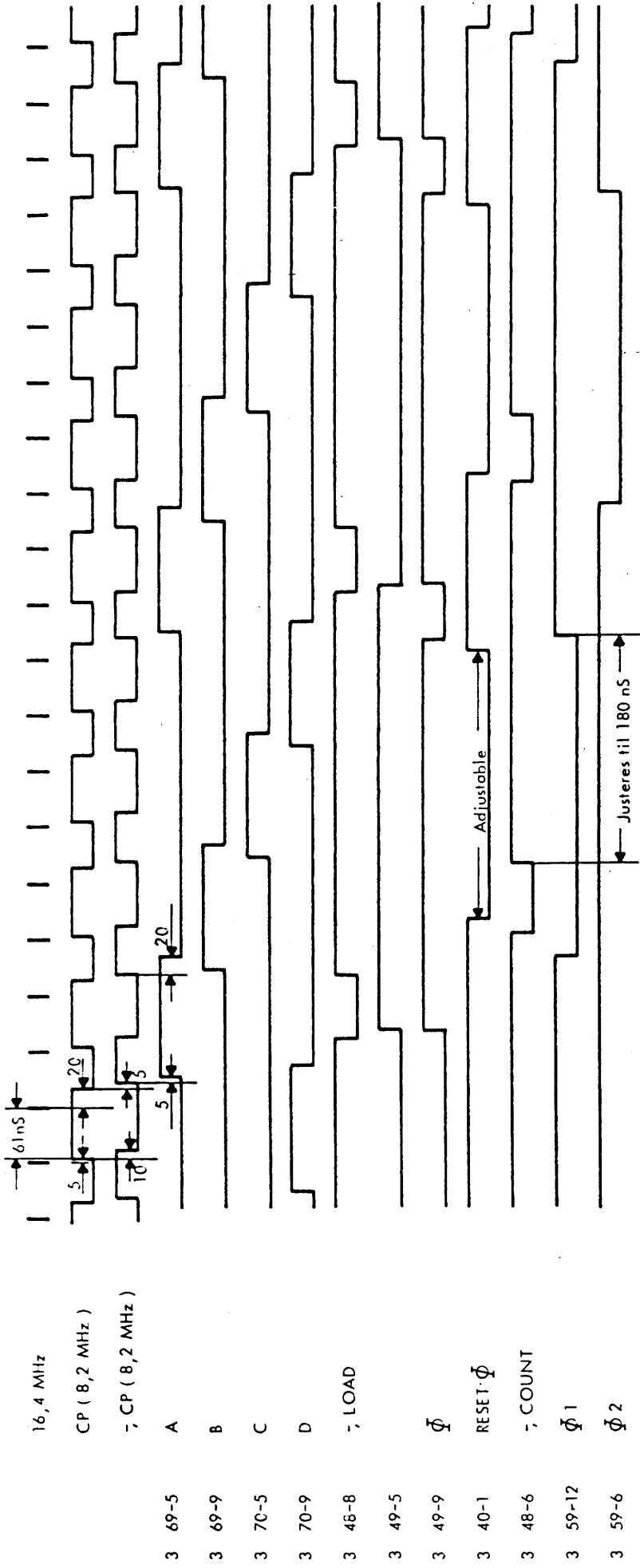
1 37-9 CLEAR

4 108-2 ; ADR COUNT LOAD

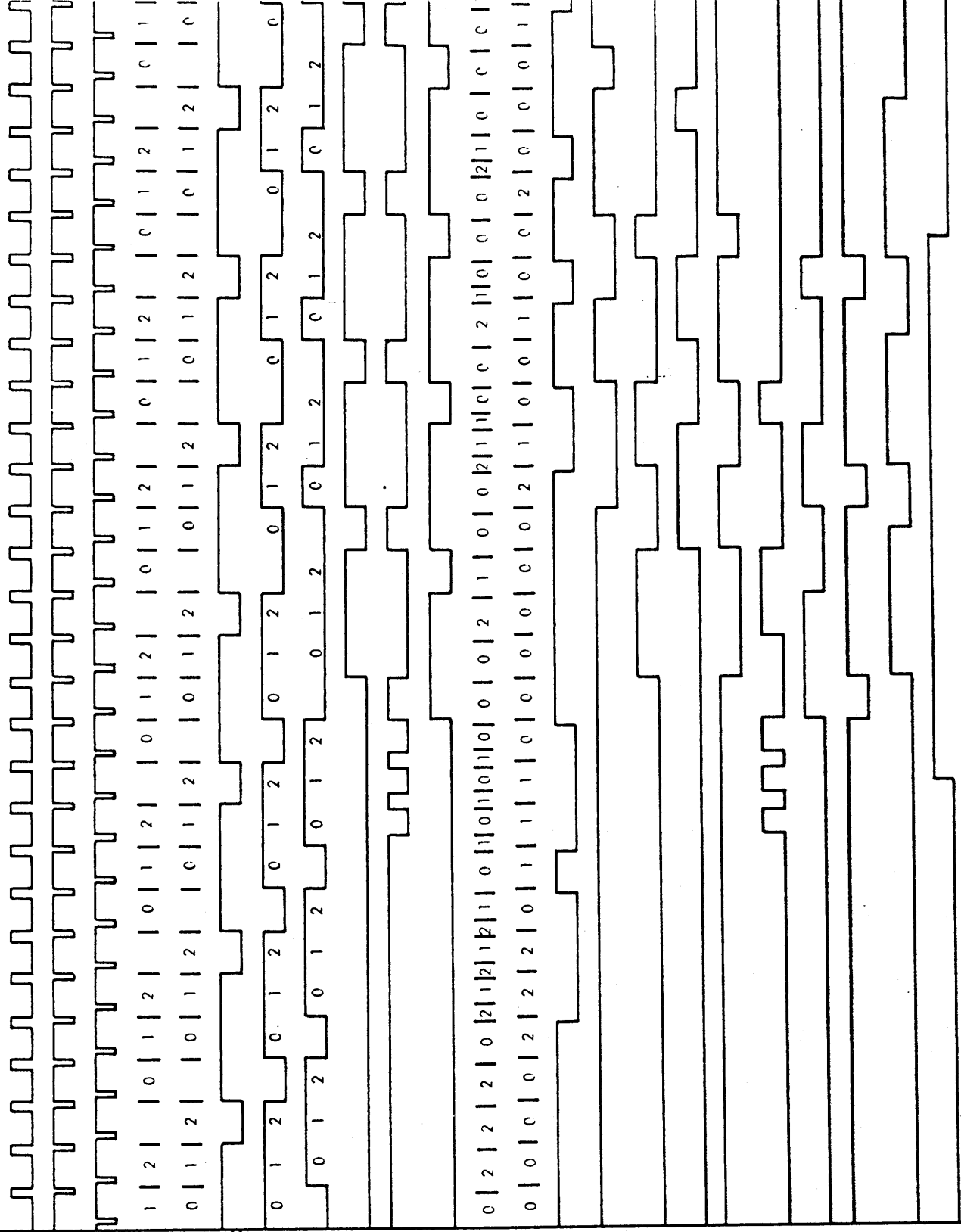


Timing Chart

25 nS



SCU 701
A 13800



- 2 48-8 ; LOAD
- 3 48-6 ; COUNT
- 4 104, 114, 124, ADR 0-10
- 5 103, 113, 123, ADR 0-9
- 4 108-2 ; ADR COUNT LOAD
- 16 26-5 EXT CHS
- 16 26-9 CHN FF
- 14 23-5 CHS FF
- 14 25-3 ; SRID CHS
- 11 108-8 SR CHS
- 9 126, 127 SRID C0-C7
- 10, 11 107, 108 SR 0-7
- 13 80-5 INH COUNT
- 14 23-8 ; LOCKOUT FF
- 14 24-6 SRID LOCKOUT
- 11 108-10 SR LOCKOUT
- 16 27-6 ; SIGN CHN FF
- 16 24-11 SRID SIGN CHN
- 11 108-12 SR SIGN CHN
- 17 13-3 ; DEV COMP DEC
- 19 71-8 DONE
- 18 44-9 UNDEF FF

- 18 45, 46, 47 UNDEF COUNTER
- 4 21 101, 111, 121, OUT BF CH NR
- CH 0

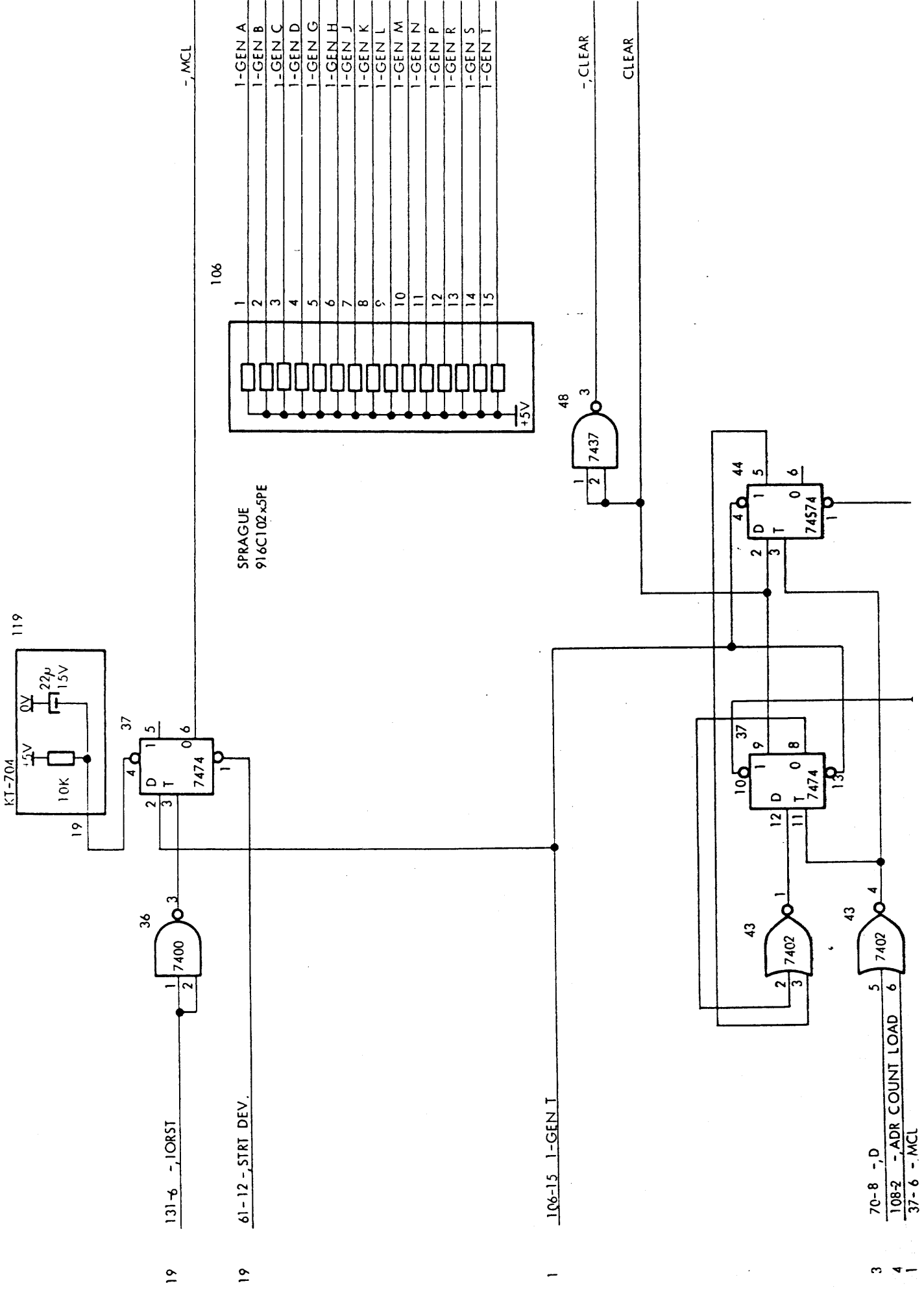
Timing Chart

Støjtfiltering
Preoverlapp, ingen preltid indsat
Støjtfiltering

SIGNAL	DESTINATION	DESCRIPTION
CLEAR	p17	CLEAR pulse
7 CLEAR	p13, p14, p16, p17, p18	7 CLEAR pulse
7 MCL	p1, p4, p15	7 Master CLear
1 - GEN A		
1 - GEN B		
1 - GEN C		
1 - GEN D		
1 - GEN G		
1 - GEN H		
1 - GEN J		
1 - GEN K	p15, p18 p21	
1 - GEN L	p17	
1 - GEN M	p9, p13 p14, p16	
1 - GEN N	p4, p5	
1 - GEN P	p2	
1 - GEN R	p3	
1 - GEN S	p3	
1 - GEN T	p1	

Designed by 801110 GR	Drawn by 801110AMS	Dwg. ce Check
--------------------------	-----------------------	------------------

Unit SCU 701		p1
Dwg. No. A25728	Signal List	



START CIRCUITS
Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
CP	p3, p18	Clock Pulse CP ≤ 8,2 MHz.
7 CP	p3	7 Clock Pulse

Designed by 801110 GR	Drawn by 801110 AMS	Dwg. <input type="checkbox"/> ce Check
--------------------------	------------------------	---

Unit SCU 701	<hr/> <hr/> <hr/>	<hr/> <hr/> <hr/>
Dwg. No. A25729	Signal List	

p2

SIGNAL	DESTINATION	DESCRIPTION
AØ1	p12, p15	APhase 1
AØ2	p12, p15	APhase 2
BØ1	p12	BPhase 1
BØ2	p12	BPhase 2
7 COUNT	p9	7 Count pulse
D	p18	4. th slep
7 D	p1	
LOAD	p13	LOAD pulse
7 LOAD	p4, p5 p9, p14 p15, p16 p17, p19 p21	7 LOAD pulse
A		1 st slep
B		2 ^d slep
C		3 ^d slep

Designed by	801110 GR
Drawn by	801110 AMS
Dwg. <input type="checkbox"/> Ice Check	

Unit SCU 701		p3
Dwg. No. A25730	Signal List	

SIGNAL

DESTINATION

DESCRIPTION

ADR 0 - ADR 3

p5,p6,
p7

ADdRes counter bit 0 - bit 10

ADR 4 - ADR 7

p5, p6
p7, p15

ADR 8 - ADR 9

p5, p15

ADR 10

p15

7ADR COUNT LOAD

p1, p15

7ADdRes counter load pulse

Designed by
801110 GR

Drawn by
801110 AMS

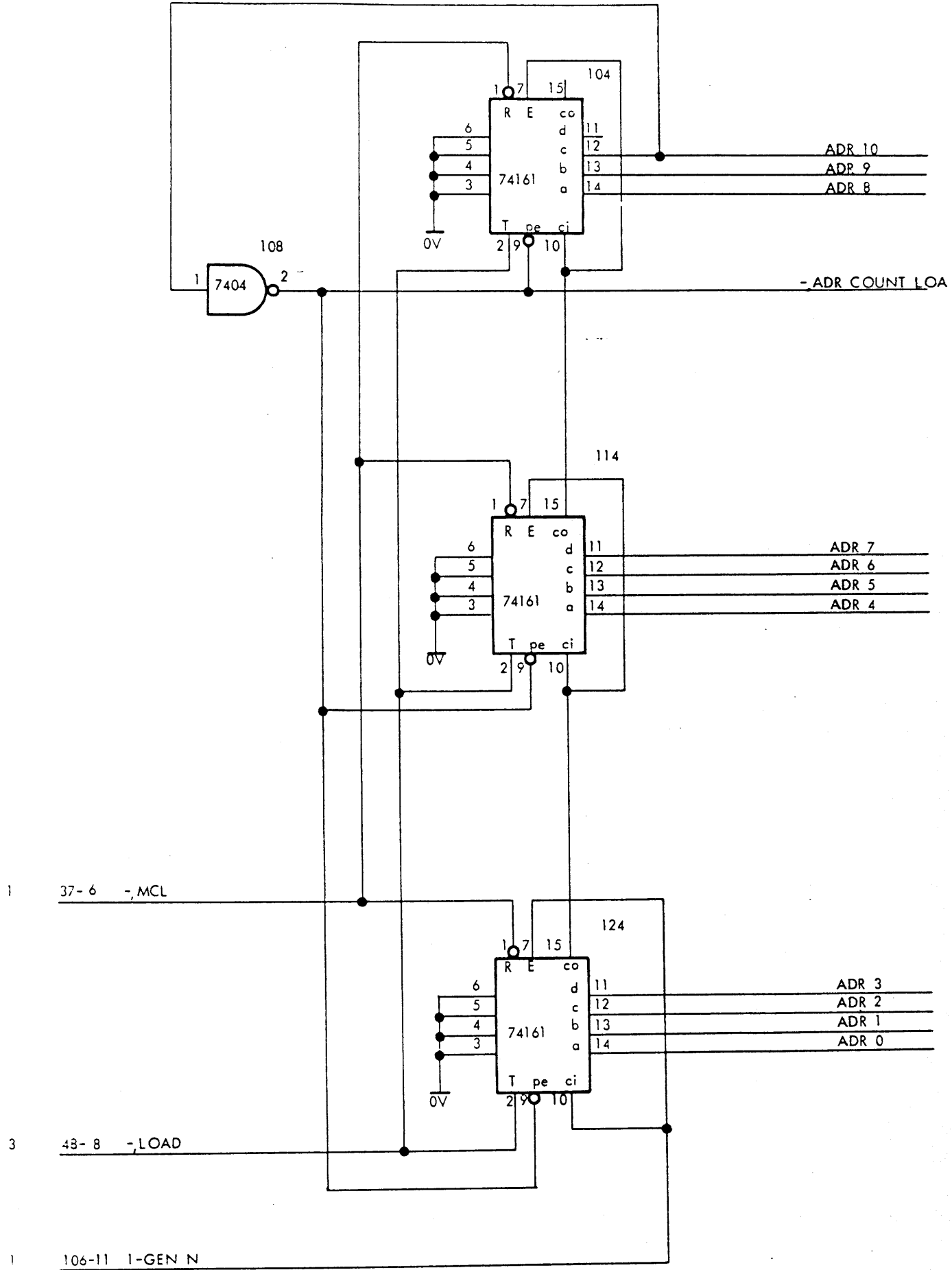
Dwg.
Ice Check

Unit
SCU 701

p4

Dwg. No.
A25731

Signal List



H1051R GR
LEC790510
H1M790219

SIGNAL

DESTINATION

DESCRIPTION

ADDRS 0 - 9

p21

store register for
addresses 0 - 9

Designed by 801110 GR	Drawn by 801110 AMS	Dwg. Office Check
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Unit

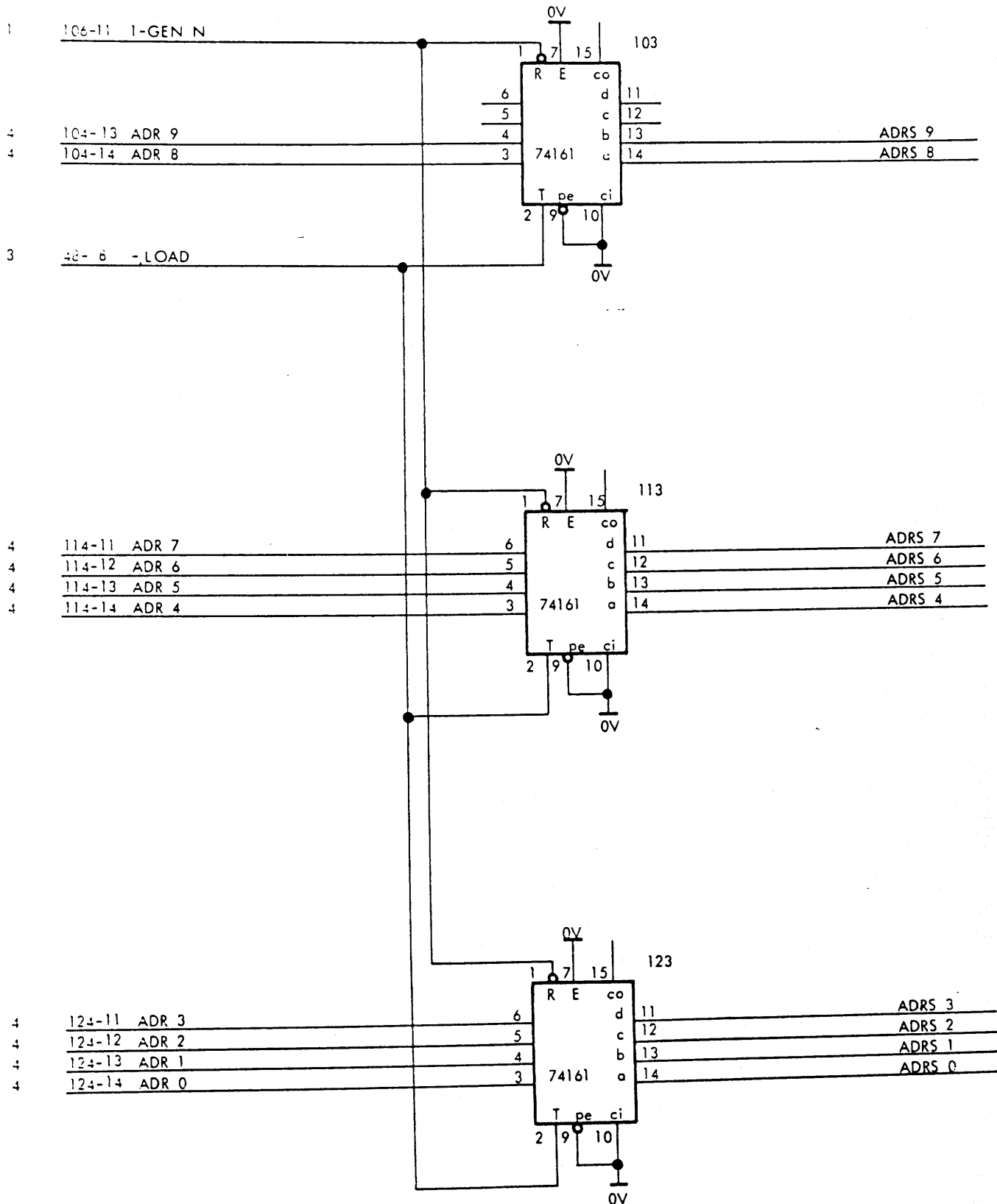
SCU 701

p5

Dwg. No.

A25732

Signal List



11M790219 LEC790509 H1051H GR

SCU701

A 13773

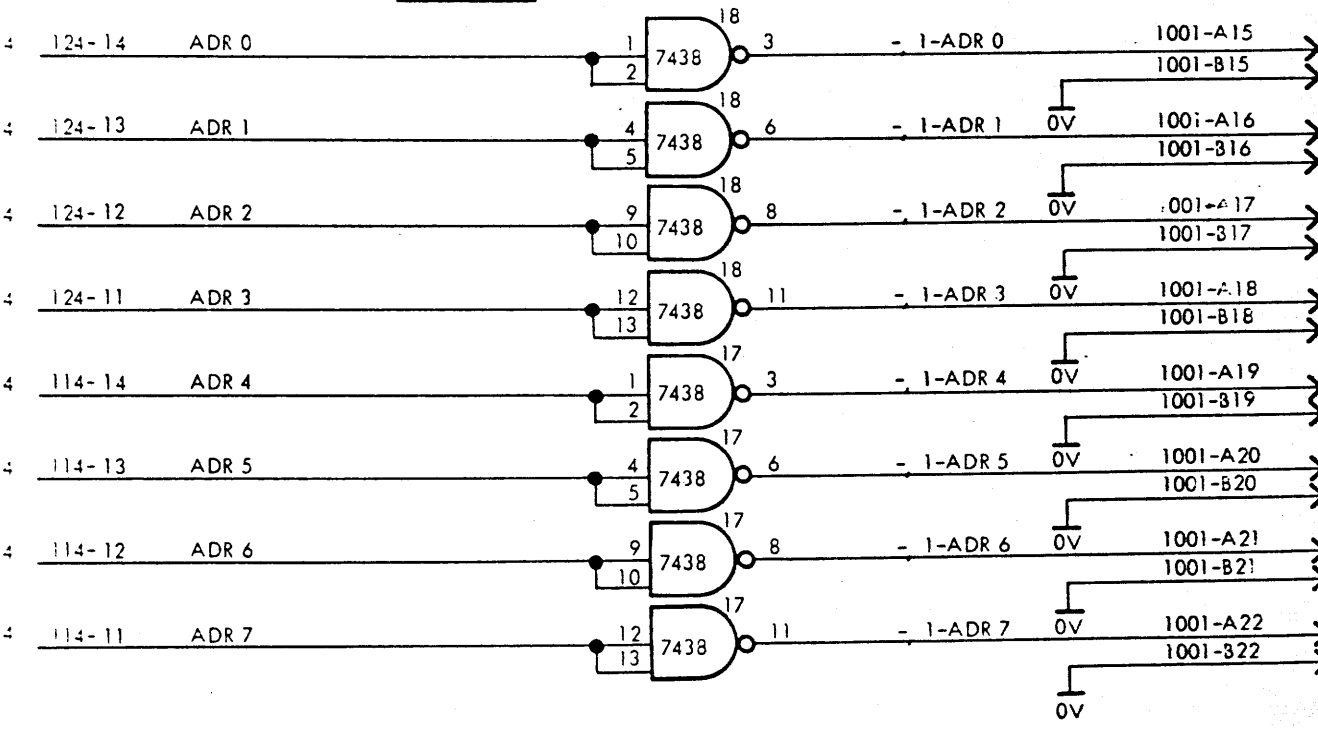
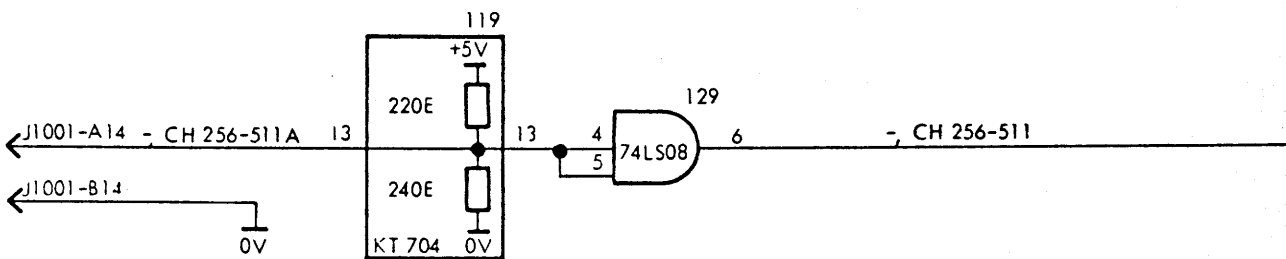
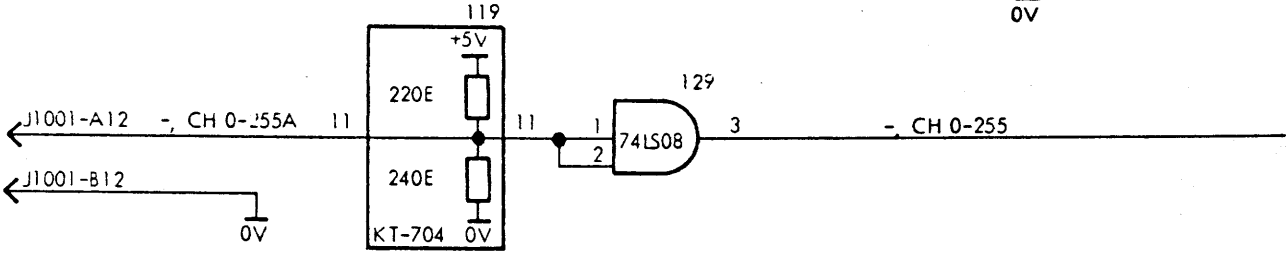
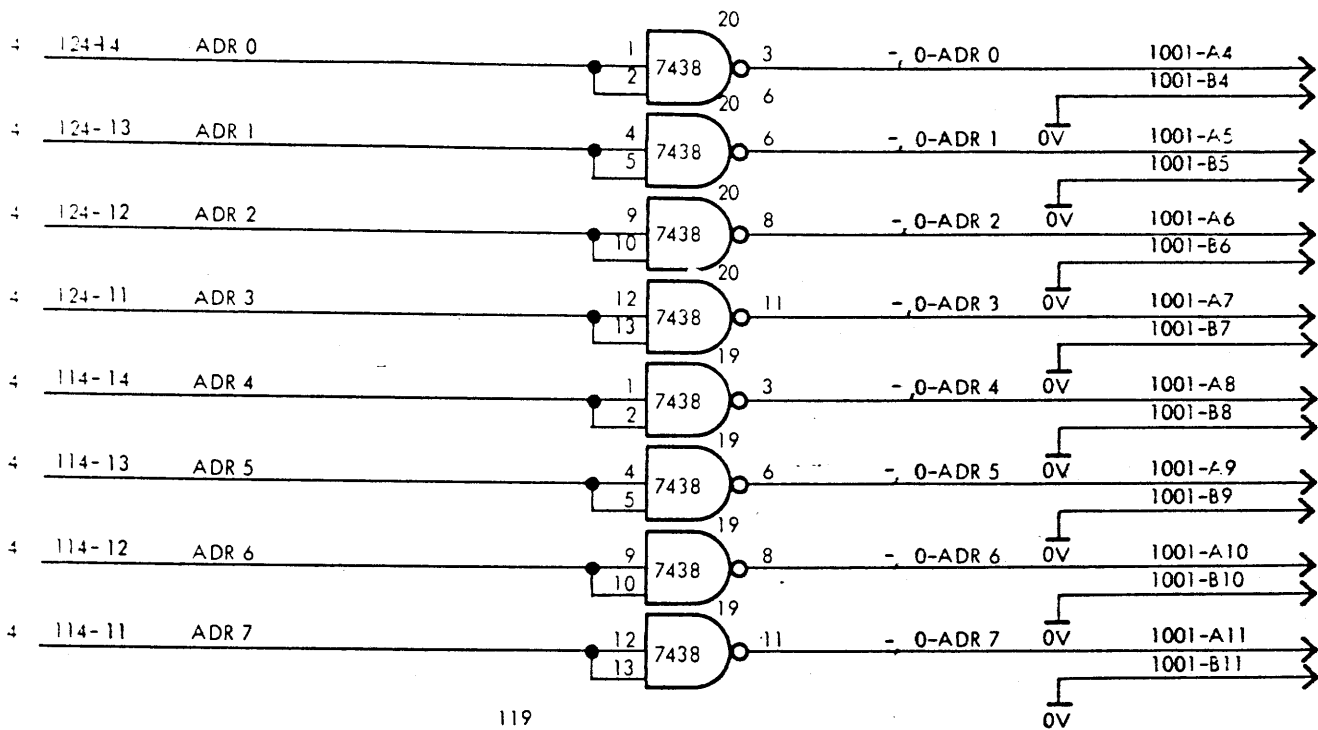
ADRS REGISTER PART 2

Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
7CH 0 - 255	p15	7CHannel 0 - 255
7CH 256 - 511	p15	7CHannel 256 - 511
7CH 0 - 255 A	PLUG 1001	7CHannel 0.- 255
7CH 256 - 511	PLUG 1001	7CHannel 256 - 511
70-ADR 0 - 70-ADR 7	PLUG 1001	7ADdRes 0 - 7 for the channels 0 - 255
71-ADR 0 - 71-ADR 7	PLUG 1001	7ADdRes 0 - 7 for the channels 256 - 511

Designed by 801110 GR	Drawn by 801110 AMS	Dwg e Check
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Unit SCU 701		p6
Dwg. No. A25733	Signal List	

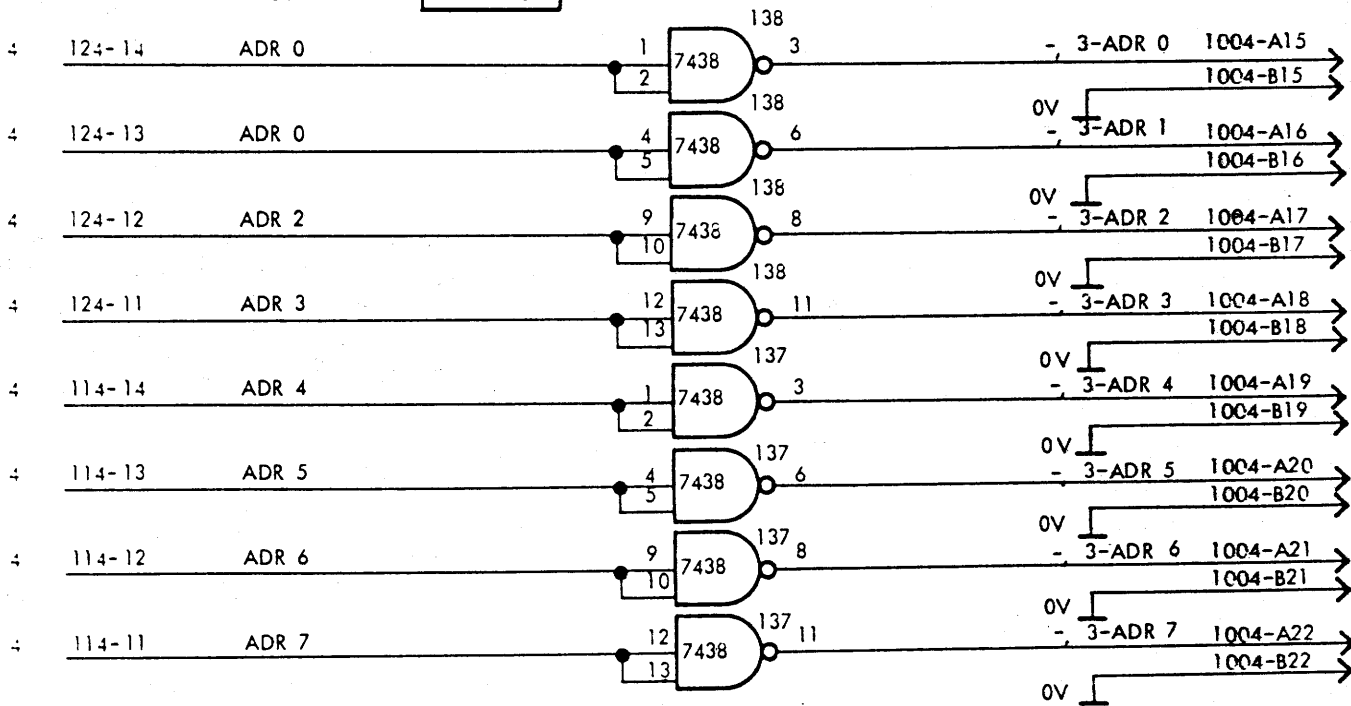
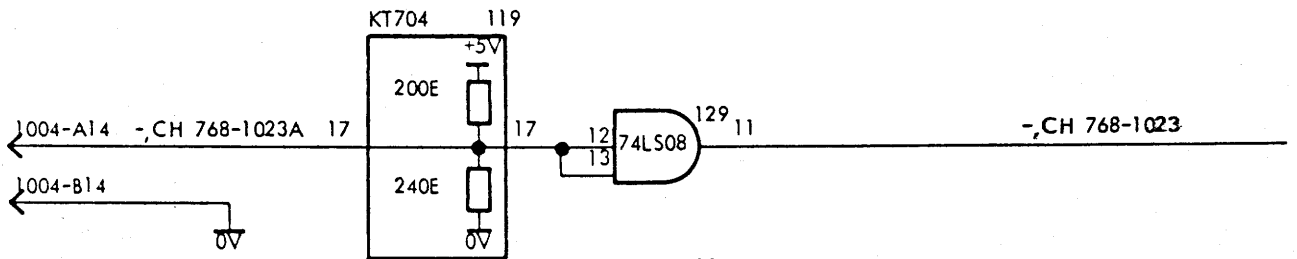
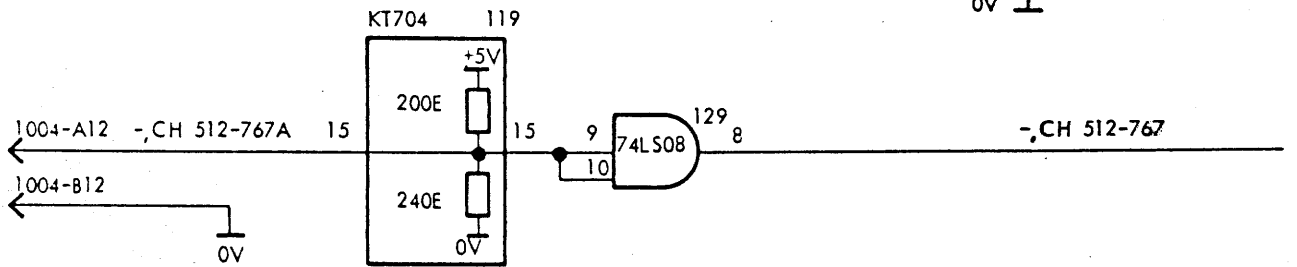
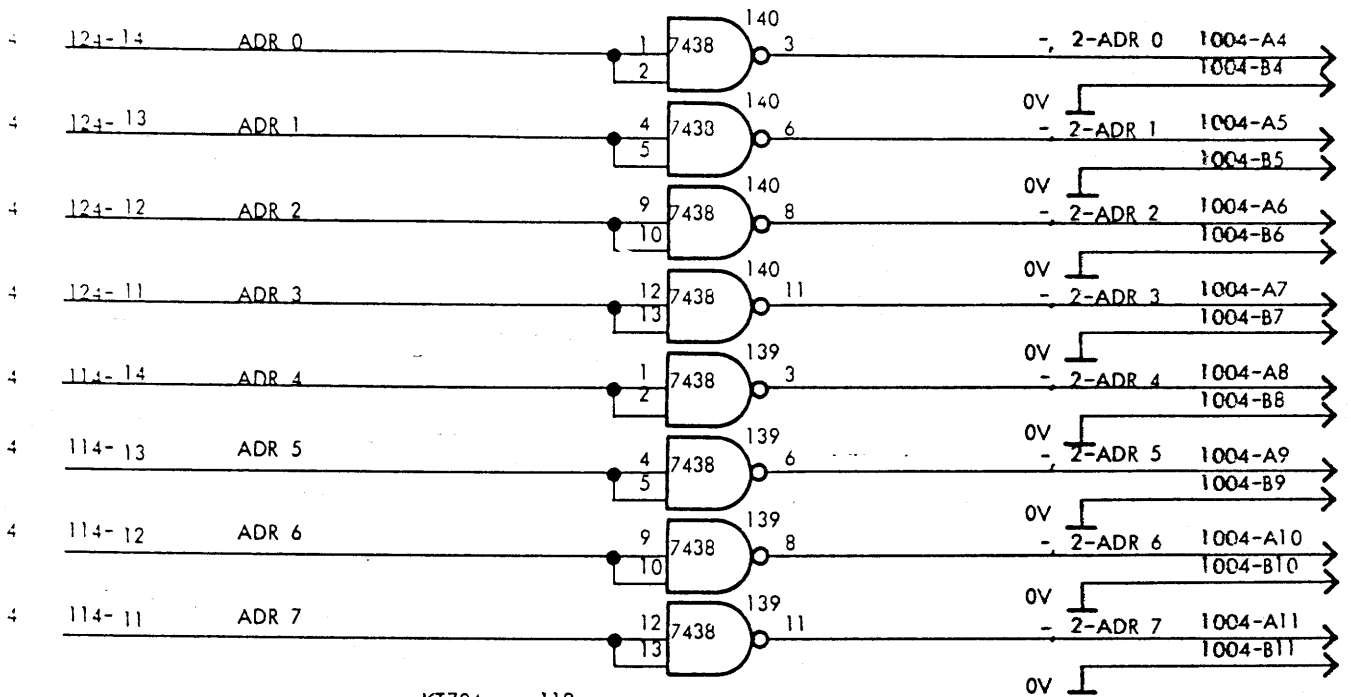


740219 HM 790502 LIC 810518 GR

SIGNAL	DESTINATION	DESCRIPTION
7 CH 512 - 767	p15	7 CHannel 512 - 767
7 CH 768 - 1023	p15	7 CHannel 768 - 1023
7 CH 512 - 767 A	PLUG 1004	7 CHannel 512 - 767
7 CH 768 - 1023 A	PLUG 1004	7 CHannel 768 - 1023
7 2 - ADR 0 - 7 2-ADR 7	PLUG 1004	7 ADResS 0 - 7 for the channels 512 - 767
7 3 - ADR 0 - 7 3-ADR 7	PLUG 1004	7 ADResS 0 - 7 for the channels 768 - 1023

Designed by 801110 GR	Drawn by 801110 AMS	Dwg. <input type="checkbox"/> Check
--------------------------	------------------------	--

Unit SCU 701		p7
Dwg. No. A25734	Signal List	



HM 790219 LEC 790509 R10518 GR

SIGNAL

DESTINATION

DESCRIPTION

CID 0 - CID 7

p9

Counter Input Data 0-7

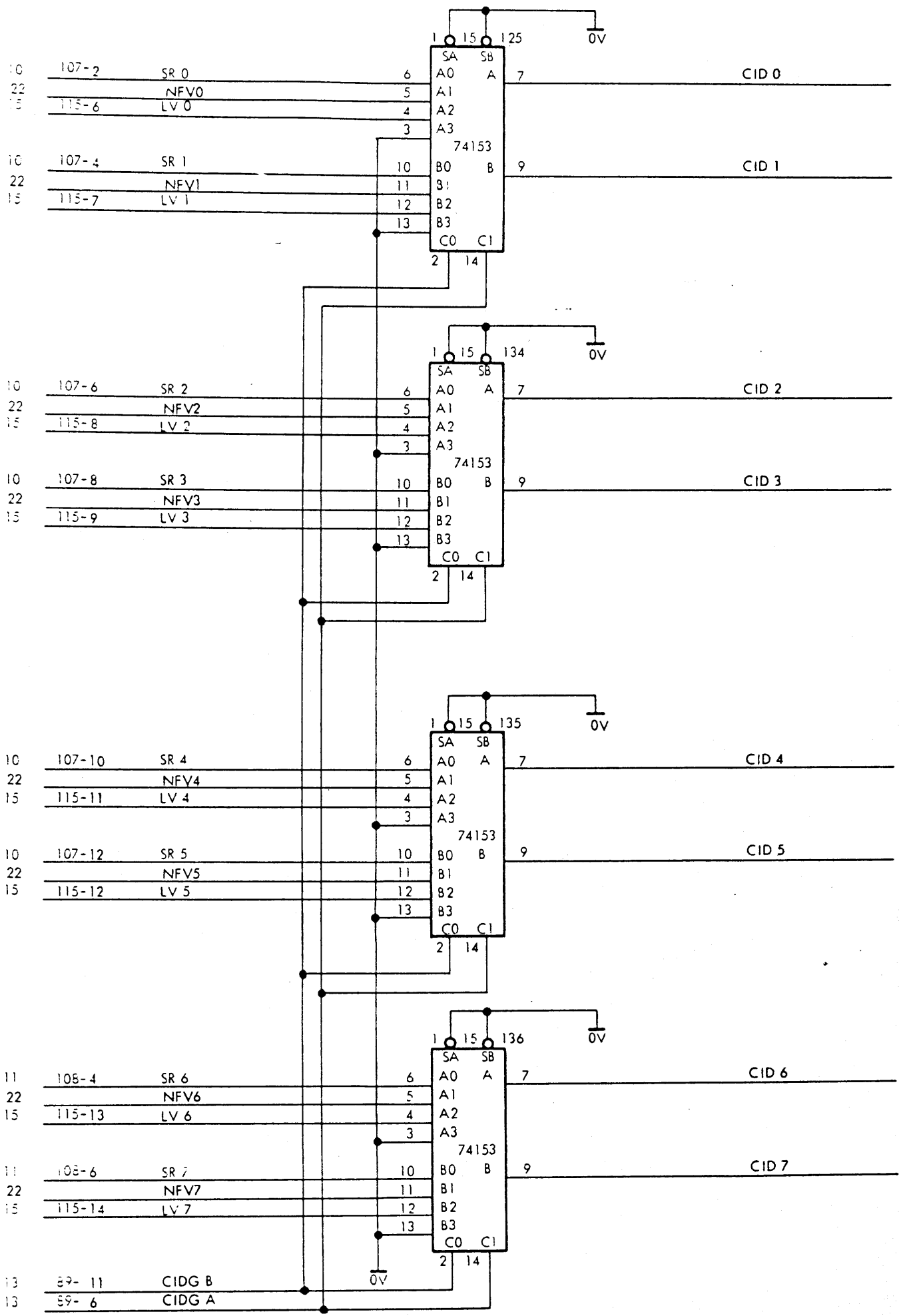
Designed by	801110 GR	Drawn by	801110 AMS	Dwg	Ice Check
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Unit
SCU 701

Dwg. No.
A25735

Signal List

p8



790116 HM 790502 LIC 81051 GR

SCU 70:

LOCKOUT COUNTER SELECTOR

A 137-1

Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
COUNTER = 0	p16, p18	COUNTER = 0
COUNTER ≠ 0	p14	COUNTER ≠ 0
.SRID C0 - SRID C5	p10	Shift Register Input Data C0 - C7

Designed by 801110 GR	Drawn by 801110 AMS	Dwg. Ice Check
--------------------------	------------------------	-------------------

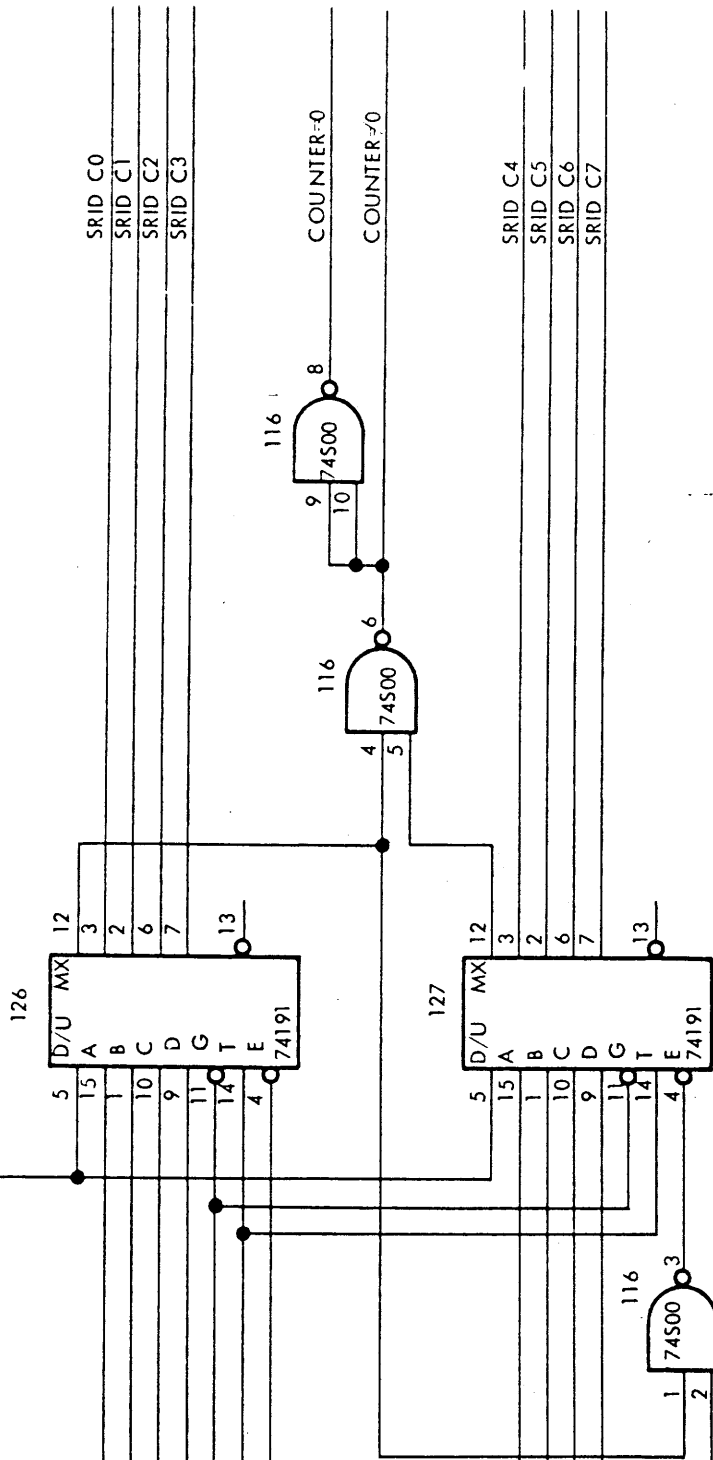
Unit SCU 701		p9
Dwg. No. A25736	Signal List	

1 106-10 1-GEN M

8 125-7 CID 0
 8 125-9 CID 1
 8 134-7 CID 2
 8 134-9 CID 3
 3 48-8 -LOAD
 3 48-6 -COUNT
 13 80-5 INH COUNT

8 135-7 CID 4
 8 135-9 CID 5
 8 136-7 CID 6
 8 136-9 CID 7

13 80-6 -INH COUNT

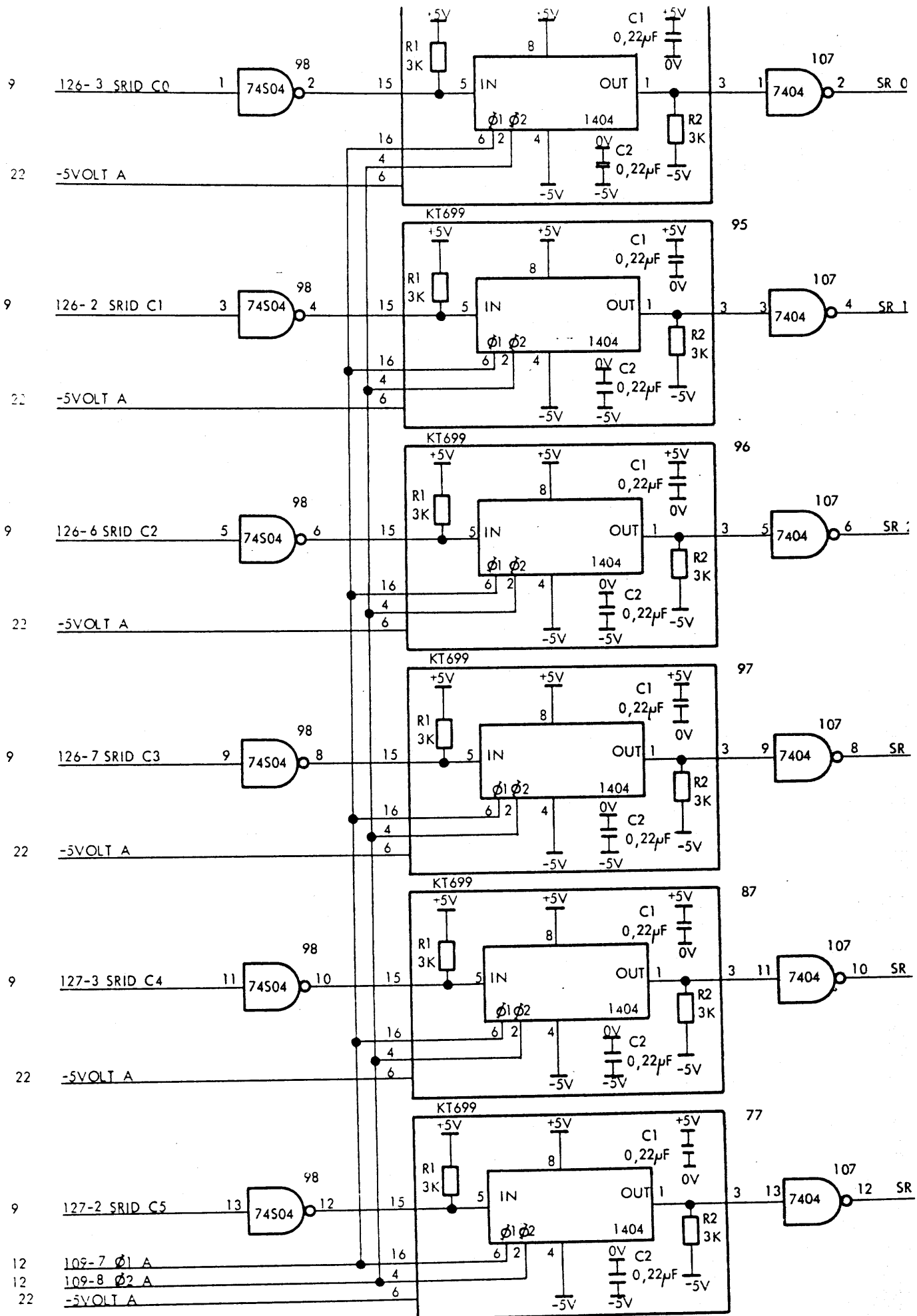


SIGNAL	DESTINATION	DESCRIPTION
SR 0 - SR 5	p12, p8	Shift Register bit 0 - 5

Designed by 801110 GR	Drawn by 801110 AMS	Dw lice Check
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bit SCU 701	<hr/> <hr/> <hr/>	p10
Dwg. No. A25737	Signal List	

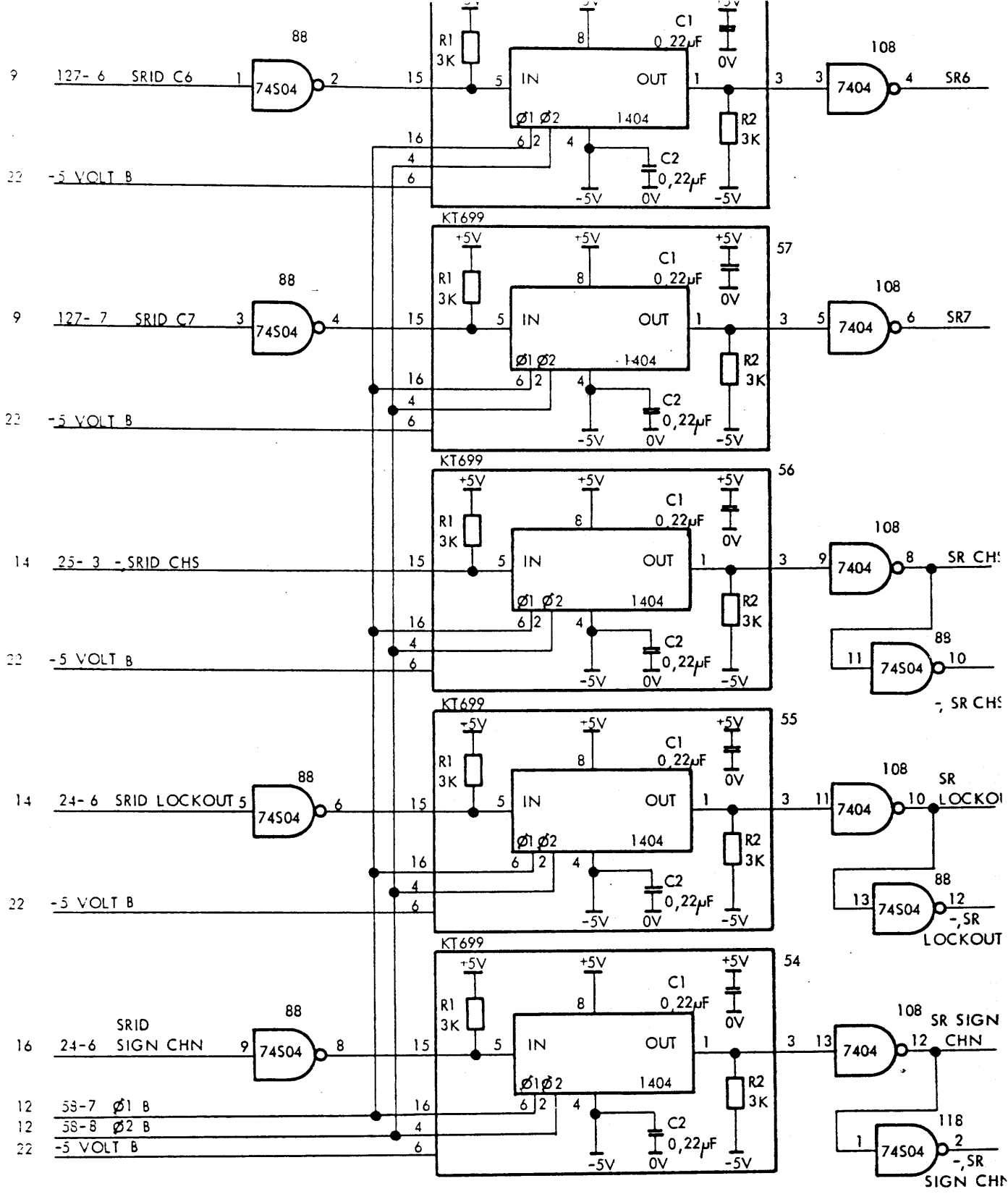
HM790216 LEC790521 810518 GR



SIGNAL	DESTINATION	DESCRIPTION
SR 6 - SR 7	p12, p8	Shift Register bit 6-7
SR CHS	p14, p16 p21	Shift Register CHannel Status
7SR CHS		7Shift Register CHannel Status
SR LOCKOUT	p14,p17	Shift Register Lockout status
7SR LOCKOUT	p13	7 Shift Register Lockout status
R SIGN CHN	p13, p16 p17,	Shift Register SIGNificant CHange Status
7SR SIGN CHN	p13	7Shift Register Significant Change Status

Designed by 801110 GR	Drawn by 801110 AMS	Dwg. ce Check
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Unit SCU 701		p11
Dwg. No. A25738	Signal List	

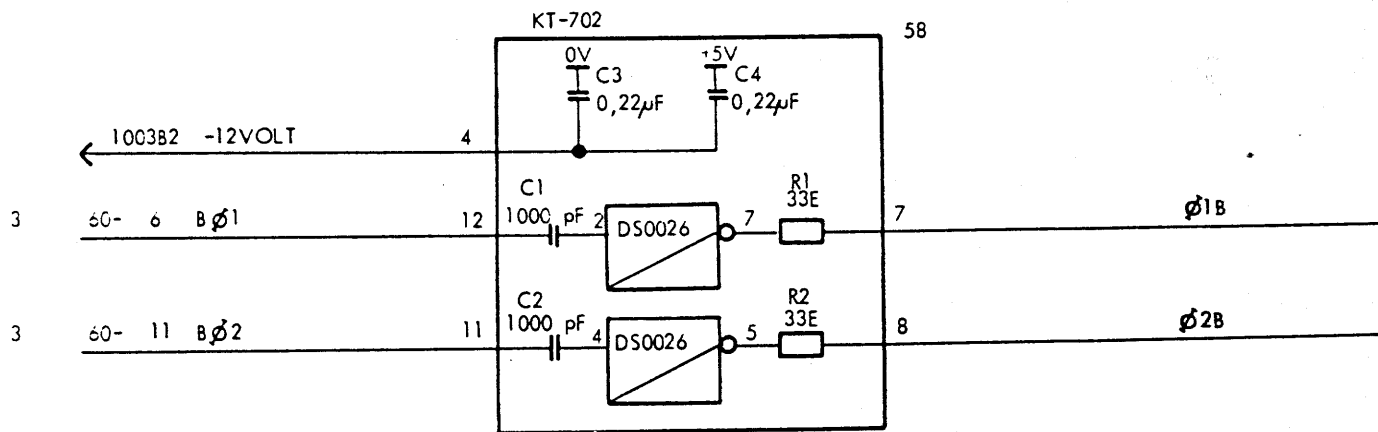
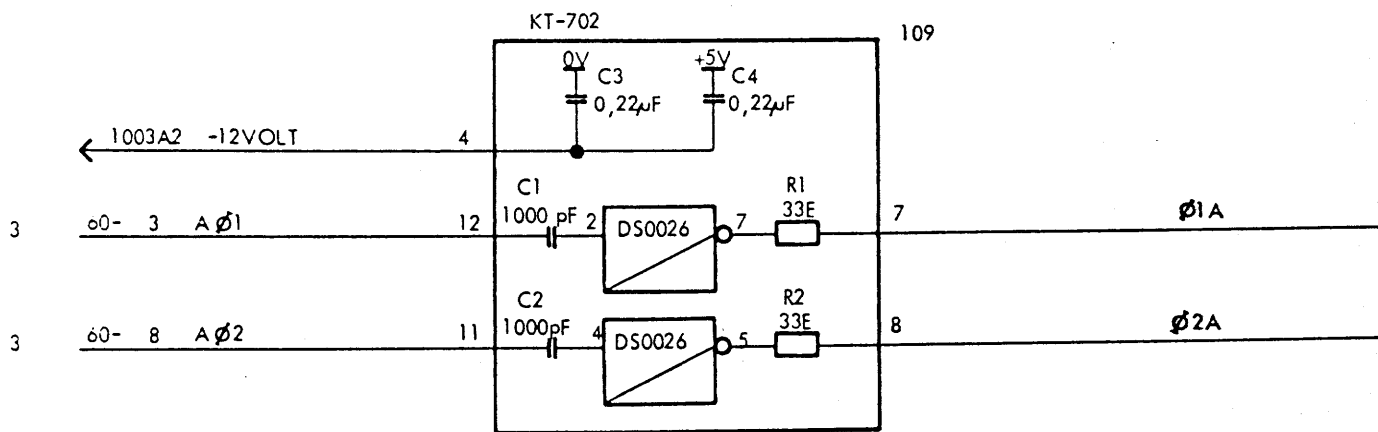
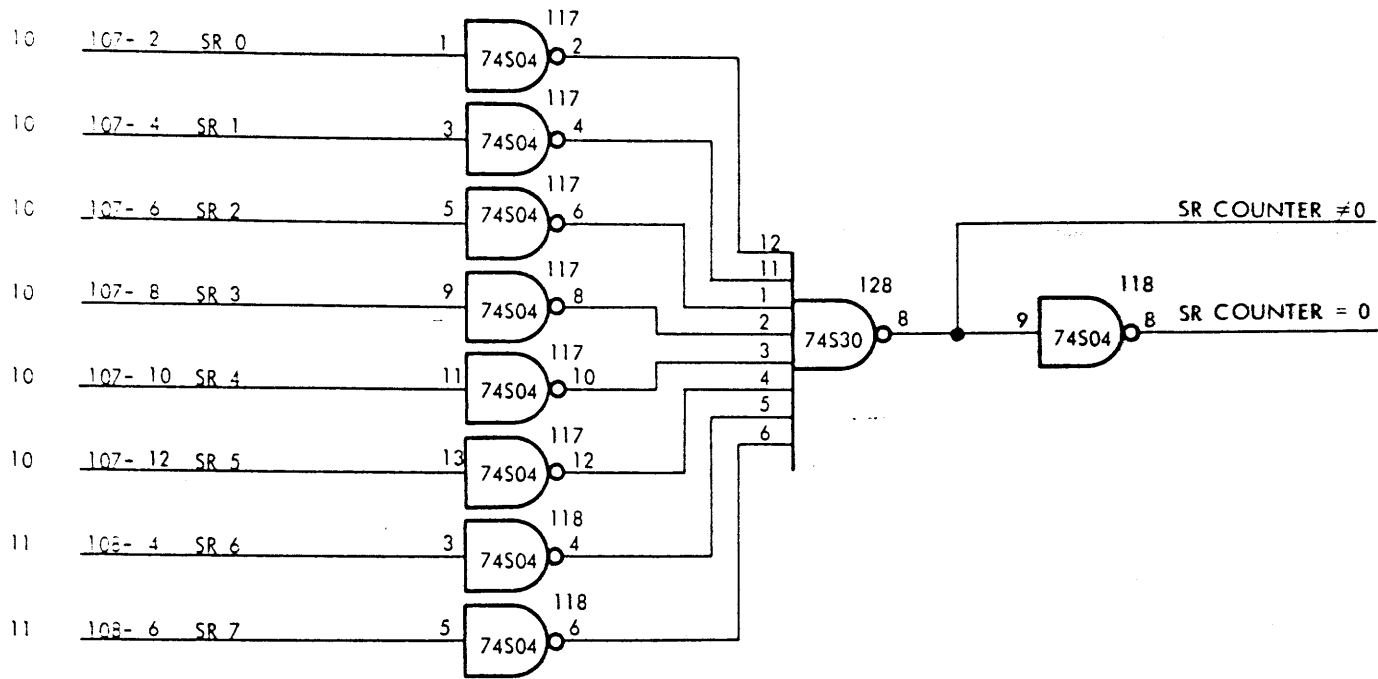


HM790216 LEC790527 R1051a CR

SIGNAL	DESTINATION	DESCRIPTION
SR COUNTER = 0	p13	SR COUNTER = 0
SR COUNTER ≠ 0	p13	SR COUNTER ≠ 0
Ø 1 A	p10	Phase 1 A
Ø 2 A	p10	Phase 2 A
Ø 1 B	p11	Phase 1 B
Ø 2 B	p11	Phase 2 B
-12V	PLUG 1003	

Designed by 801110 GR	Drawn by 801110 AMS	Dwg. <input type="checkbox"/> ce Check
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Unit SCU 701		p12
Dwg. No. A25739	Signal List	



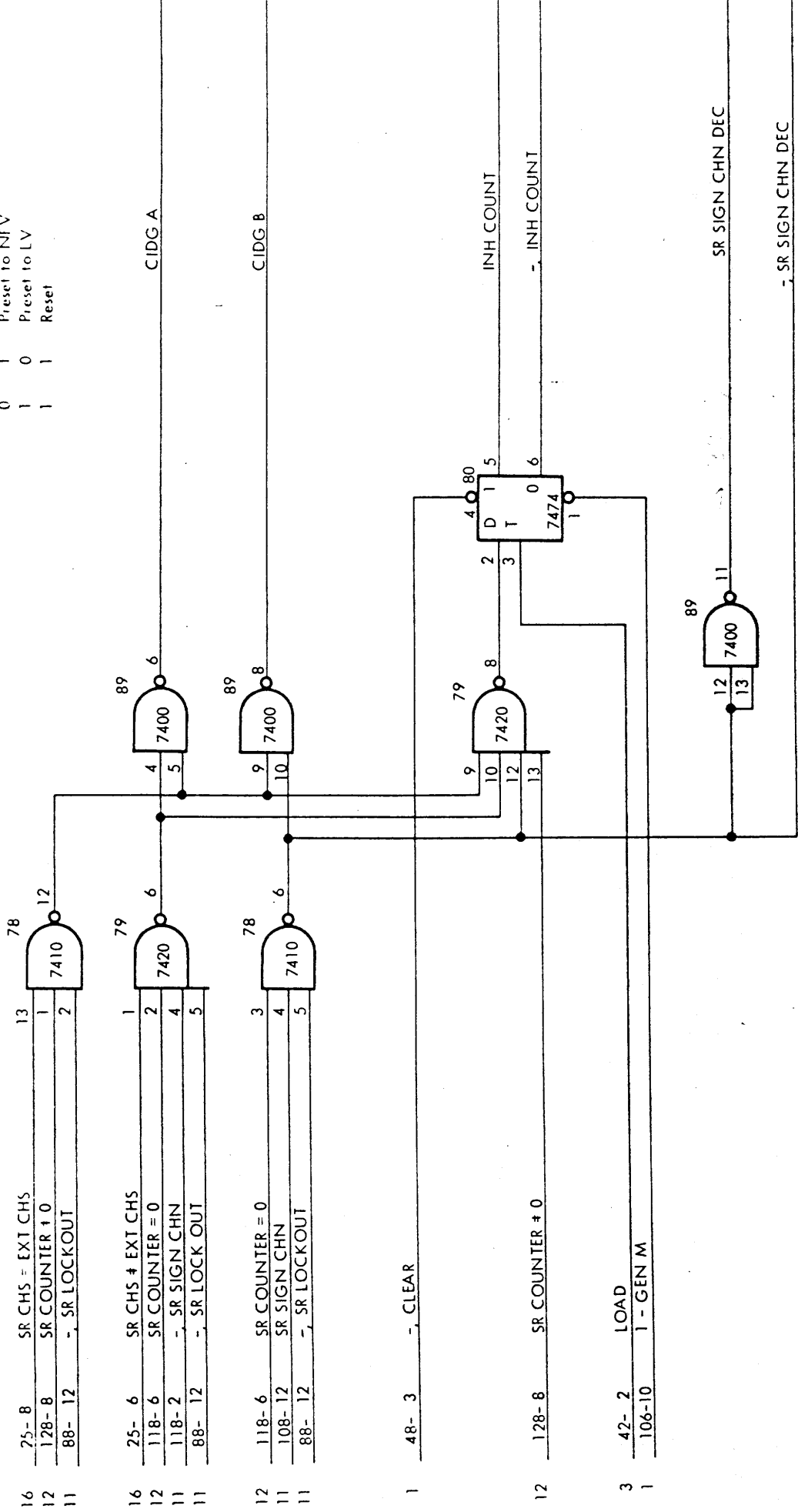
HM790216 LEC790521 810518 GR

SIGNAL	DESTINATION	DESCRIPTION
CIDG A	p8	Counter Inpit Data Gate pulse A
CIDG B	p8	Counter Input Data Gate pulse B
INH COUNT	p9	INHibit COUNT
SR SIGN CHN DEC	p17	Shift Register SIGNificant CHAnge DECoded
7SR SIGN DEC		7 Shift Register SIGNificant CHAnge DECoded

Designed by 801110 GR	Drawn by 801110 AMS	Dwg. Title Check
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Unit SCU 701		p13
Dwg. No. A25740	Signal List	

CIDG	B	A	
	C	0	Select SR
	0	1	Preset to NFV
	1	0	Preset to LV
	1	1	Reset



CONTROL LOGIC 1A
Circuit Diagram

SIGNAL

DESTINATION

DESCRIPTION

7 LOCKOUT FF

p16, p18

7 LOCKOUT Flip Flop

SRID LOCKOUT

p11

Shift Register Input Data, LOCKOUT

7 SRID CHS

p11

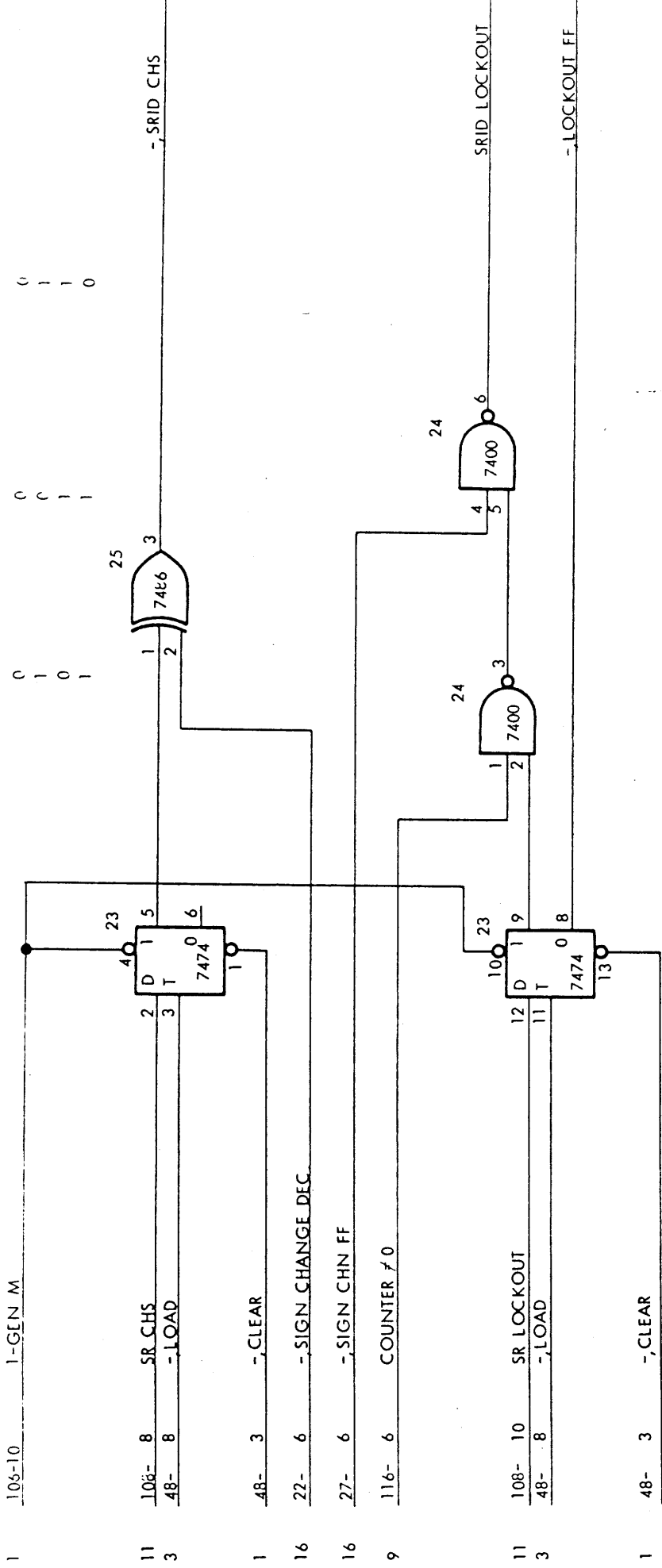
7 Shift Register Input Data,
Channel Status

Designed by 801110 GR	Drawn by 801110 AMS	Dwg. Ice Check
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SCU 701 Dwg. No. A25741	_____ _____ _____ Signal List	_____ p14 _____ _____
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SCU701
A 13767

CHS FF ; SIGN CHN DEC ; SRID CHS



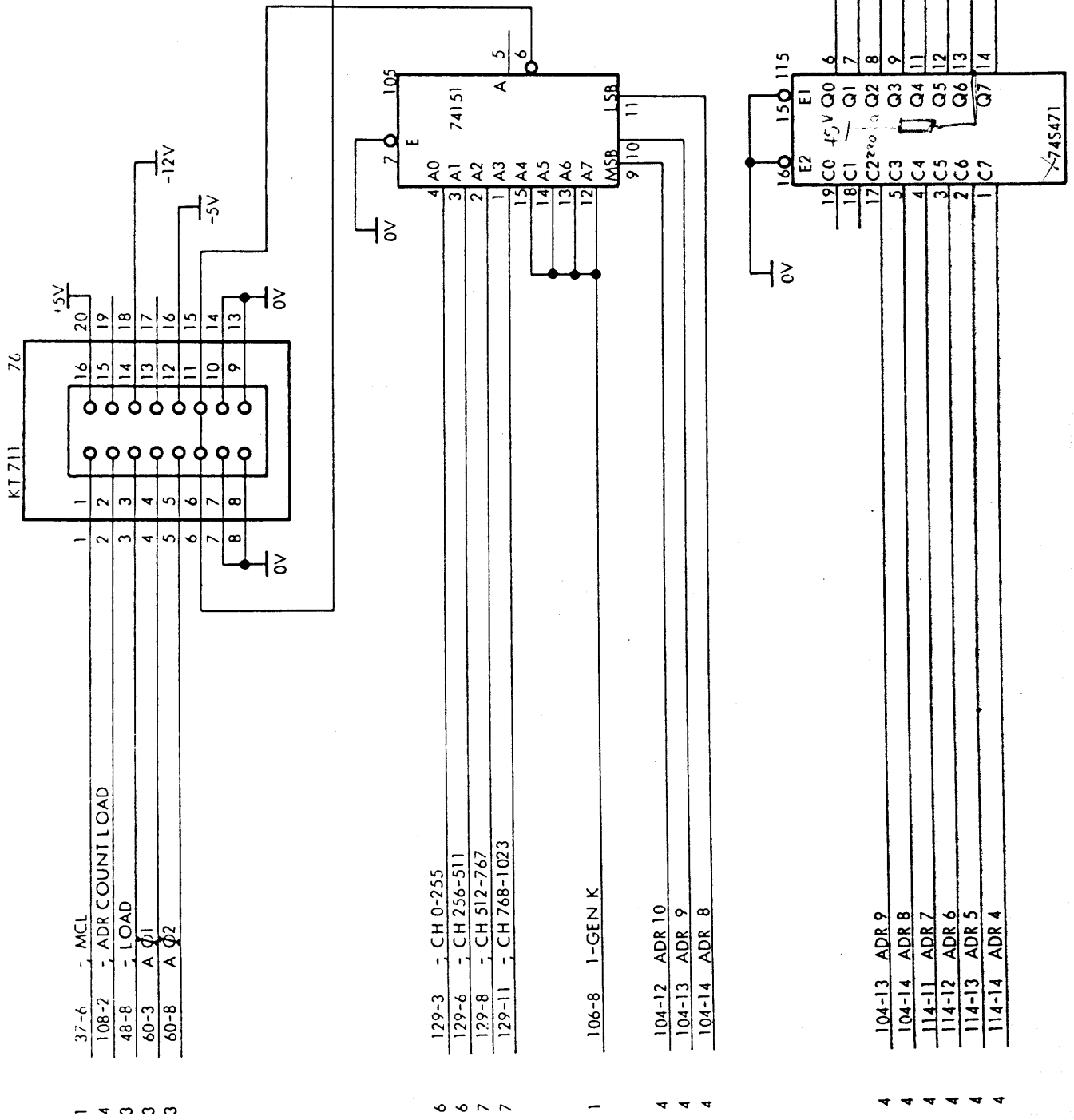
Lockout fjernes hvis : ; SIGN CHANGE FF & COUNTER = 0
 Lockout føres igennem hvis : SIGN CHANGE FF I COUNTER ≠ 0
 Lockout genereres hvis : SIGN CHANGE FF

CONTROL LOGIC 1B
Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
CHS DEC LV 0 - LV 7	p16 p8	CHannel Status DEcoded Lockout Value bit 0 - bit 7

Designed by	Drawn by	Dwg. <input type="checkbox"/> Check
801110 GR	801110 AMS	

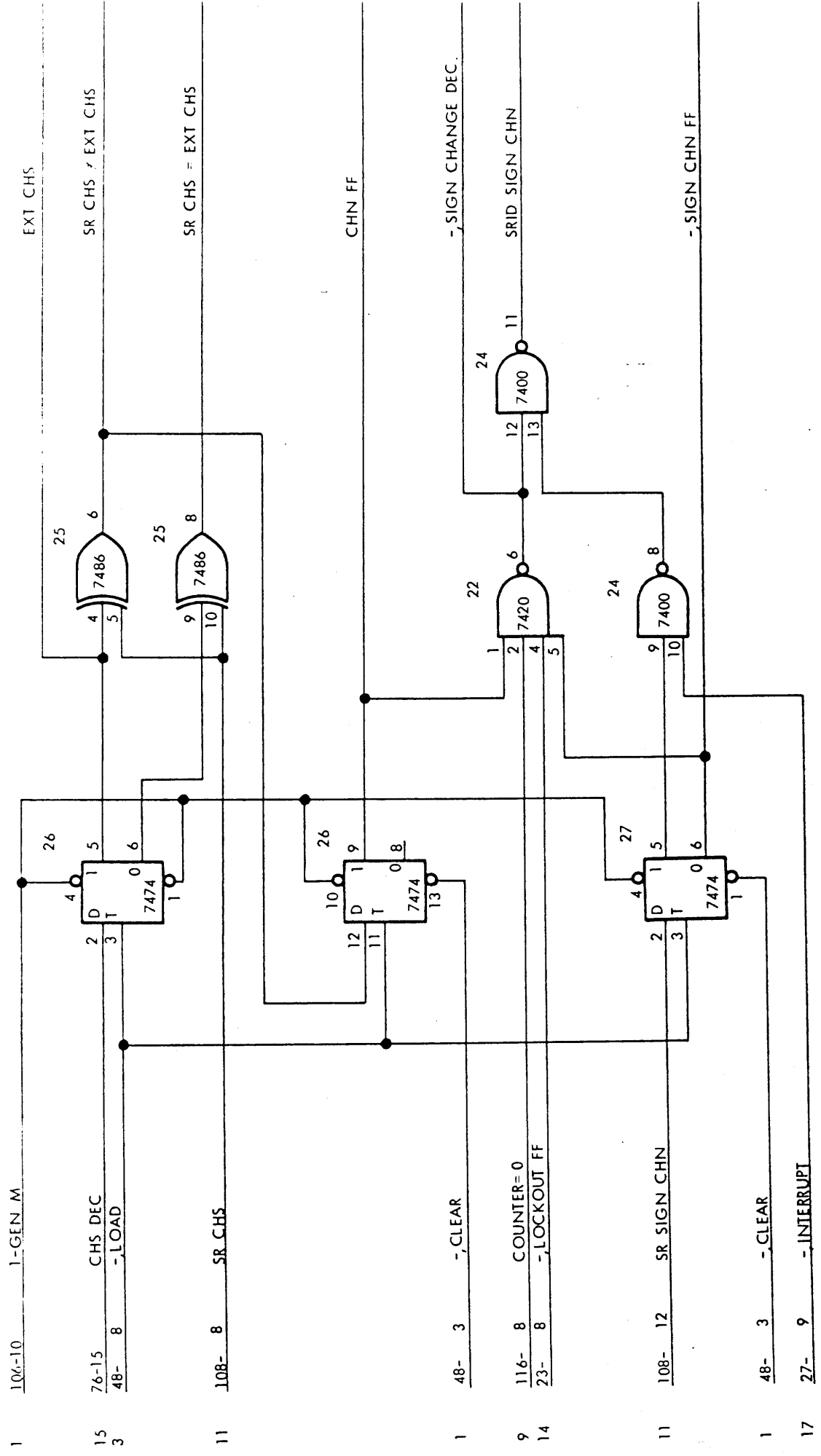
bit SCU 701	<hr/> <hr/> <hr/>	p15
Dwg. No. A25742	<hr/> <hr/> signal List	



SIGNAL	DESTINATION	DESCRIPTION
● CHN FF	p18	CHaNge Flip Flop
EXT CHS		EXTErnal CHannel Status
SR CHS = EXT CHS	p13	Shift Register CHannel Status = External Channel Status
SR CHS ≠ EXT CHS	p13	Shift Register CHannel Status ≠ EXTErnal Channel Status.
SRID SIGN CHN	p11	Shift Register Input Data, SIGNificant CHaNge
● 7SIGN CHANGE DEC	p14	7 SIGNificant CHANGE DECoded
7SIGN CHN FF	p18, p14	7SIGNificant CHaNge Flip Flop

Designed by 801110 GR	Drawn by 801110 AMS	Dwg Ice Check
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mit SCU 701	<hr/> <hr/>	p16
Dwg. No. A25743	Signal List	



SCU:01
A 13789

CONTROL LOGIC PART 3
Circuit Diagram

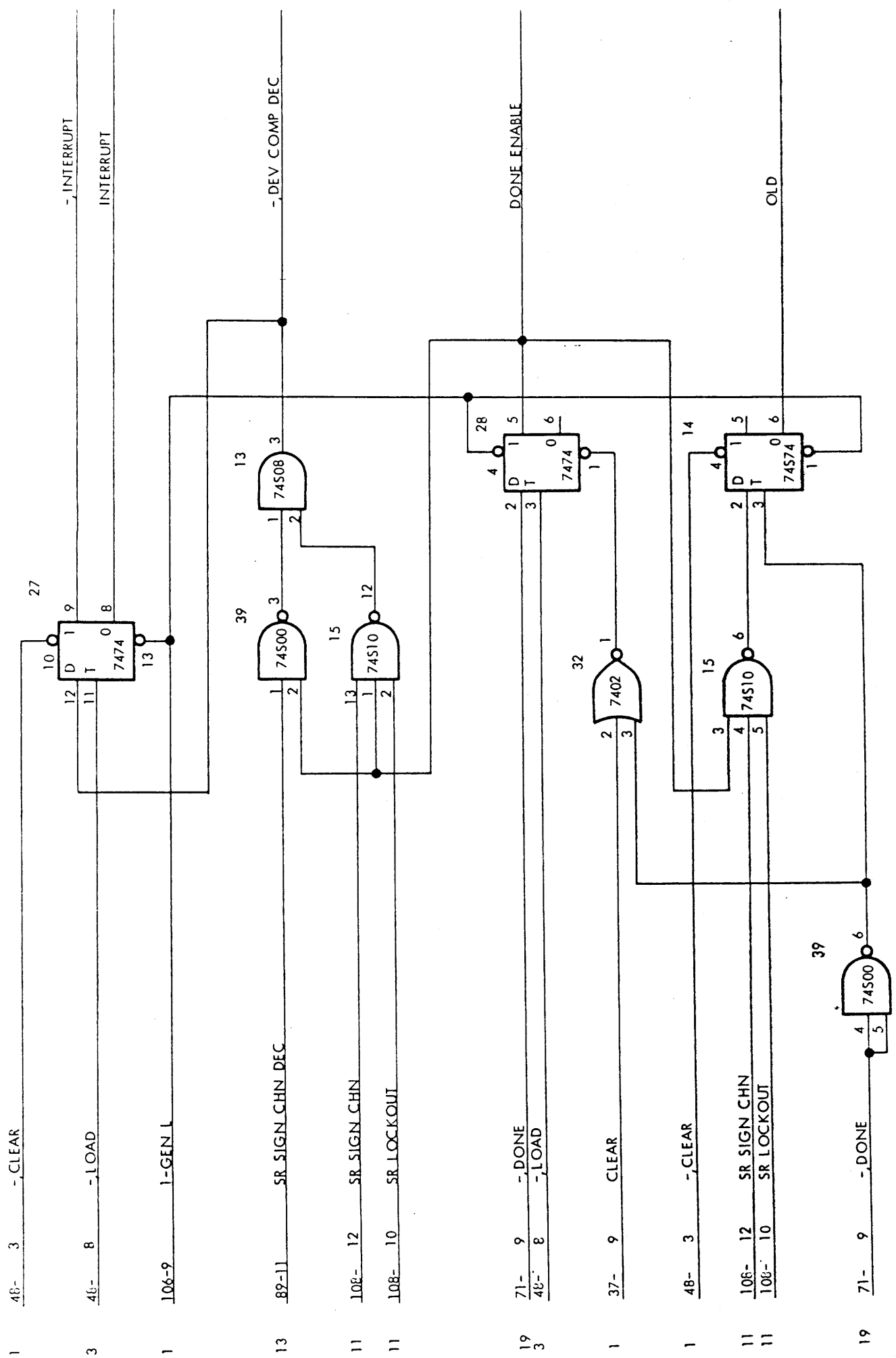
SIGN CHANGE fjernes hvis INTERRUPT
SIGN CHANGE føres igennem hvis -INTERRUPT
SIGN CHANGE genereres hvis CHANGE FF & COUNTER = 0 & -LOCKOUT FF & -SIGN CHANGE FF

SIGNAL	DESTINATION	DESCRIPTION
DONE ENABLE		DONE ENABLE
7 DEV COMP DEC	p19, p21	7 DEVIce COMpLeTE DECoded
INTERRUPT	p18	INTERRUPT
7 INTERRUPT	p18, p16	7 INTERRUPT
OLD	p21	OLD

Designed by 801110 GR	Drawn by 801110 AMS	Dwg. <input type="checkbox"/> ice Check
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Unit SCU 701		p17
Dwg. No. A25744	Signal List	

SCU701
A 13790



CONTROL LOGIC PART 4

Circuit Diagram

SIGNAL

DESTINATION

DESCRIPTION

UNDEF

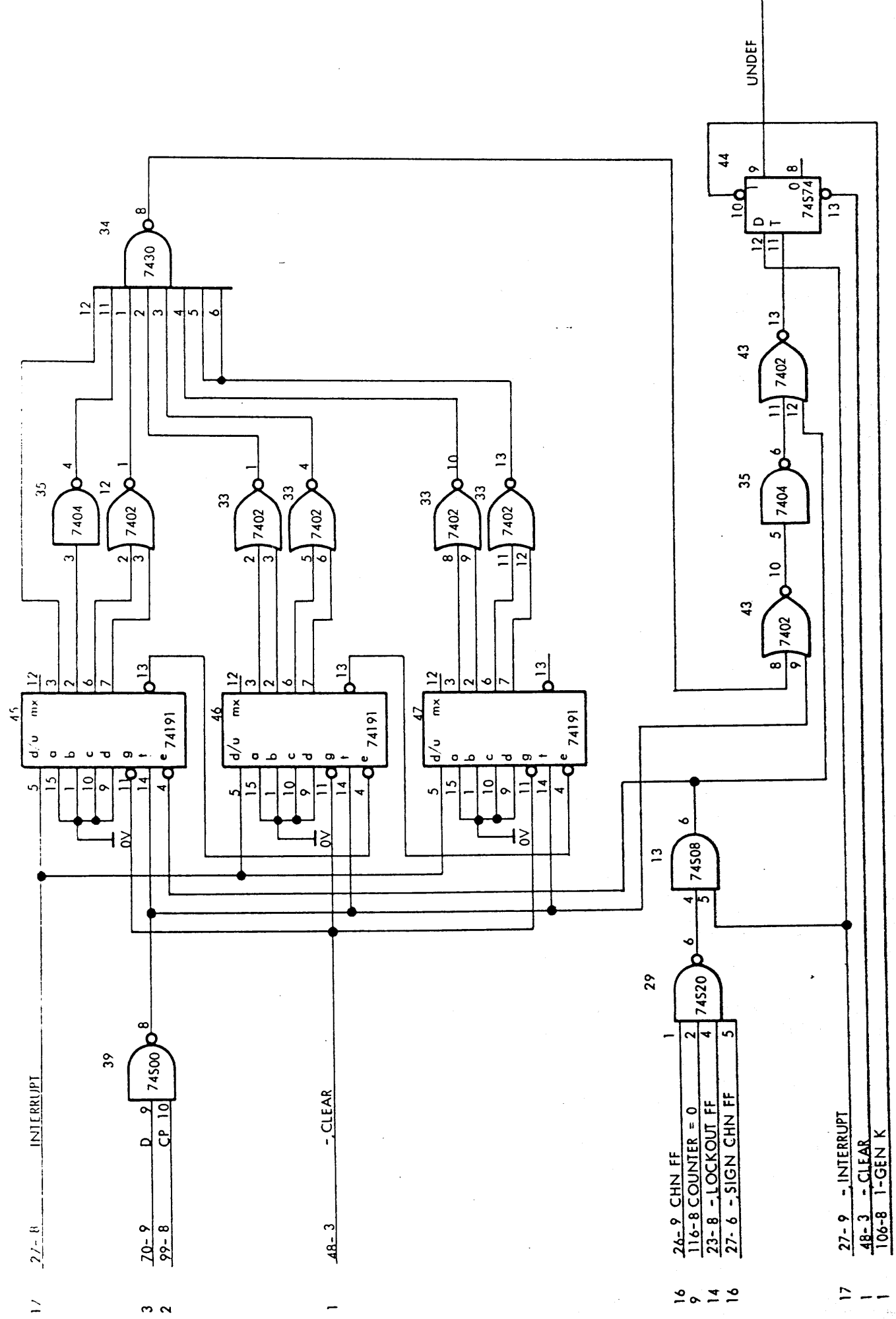
p21

UNDEFined

Designed by	801110 GR
Drawn by	801110 AMS
Dwg. <input type="checkbox"/> Ice Check	

it SCU 701		p18
Dwg. No. A25745	SignalList	

SCU701
A 13791



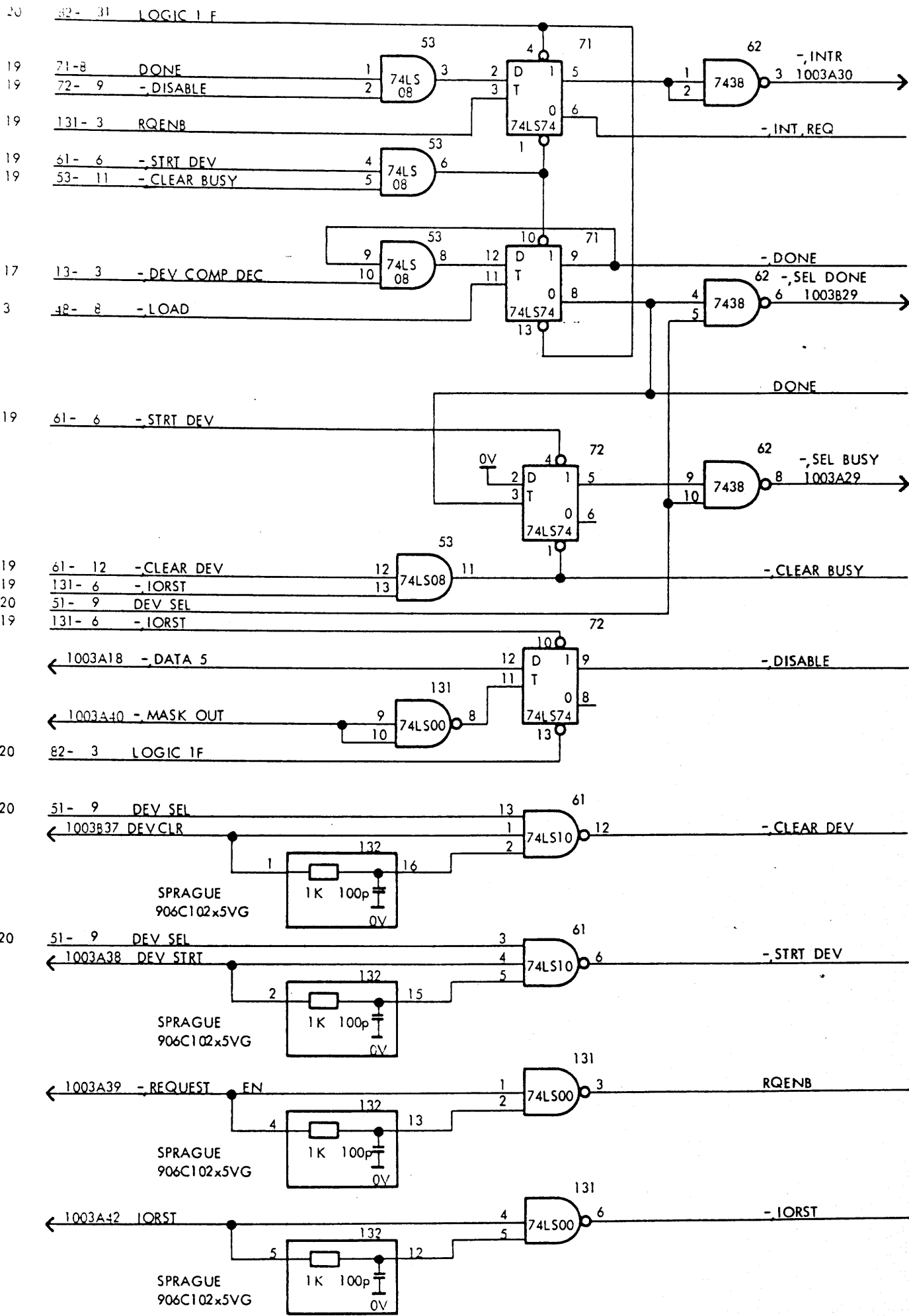
UNDEFINED COUNTER

Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
7 CLEAR BUSY	p19	7 CLEAR BUSY
7 CLEAR DEV	p19	7 CLEAR DEvIce Flip Flop
DONE	p19	DONE
7 DONE	p17	7 DONE
7 INTR	PLUG 1003	7 INTeRrupt
7INT REQ	p20	7 INTeRrupt REQuest
7 IORST	p1, p19	7 IO ReSeT pulse
RQENB	p19	REQuest ENABLE
7 SEL BUSY	PLUG 1003	7SELEct BUSY
7 SEL DONE	PLUG 1003	7SELEct DONE
7STRT DEV	p1, p19	7STaRT DEvIce
7 DATA 5	PLUG 1003	7 DATA Bus 5
DEV CLR	PLUG 1003	DEvIce CLeaR
DEV STRT	PLUG 1003	DEvIce STaRT
IORST	PLUG 1003	IO ReSeT Pulse
7 REQUEST EN	PLUG 1003	7REQUEST ENable
7 MASK OUT	PLUG 1003	7 MASK OUT

Designed by 801110 GR	Drawn by 801110 AMS	Dwg Ice Check
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bit SCU 701 Dwg. No. A25746	----- ----- Signal List	----- p19 -----
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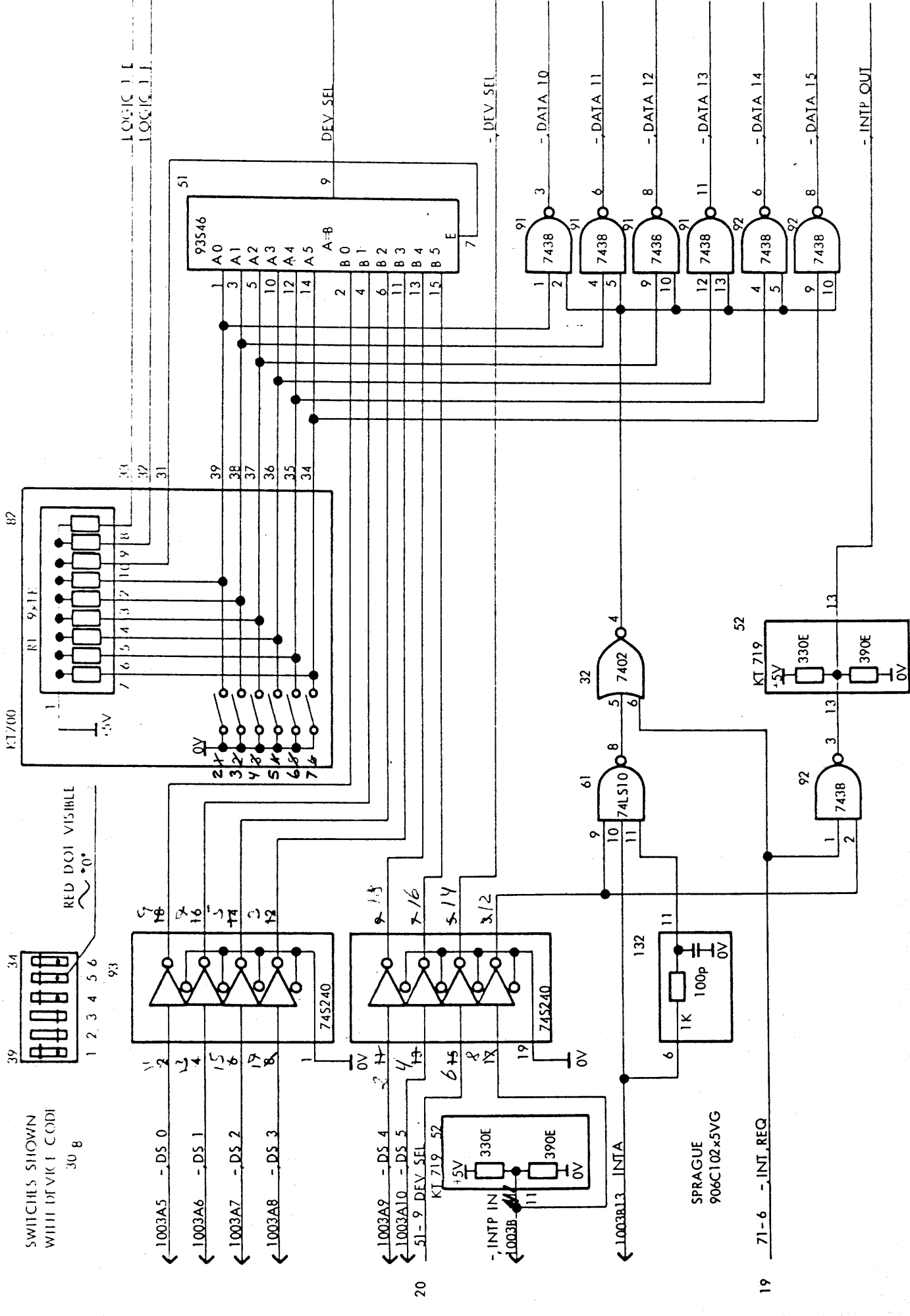


HM790216 LEC790522 REV 7/11/83 LLM 810518 GR

SIGNAL	DESTINATION	DESCRIPTION
DEV SEL	p19, p20	DEvIce SElect
7 DEV SEL	p21	7 DEvIce SElect
7 DATA 10 - 7DATA 15	p21	7 DARA Bus bit 10 - bit 15
7DS 0 - 7 DS 5	PLUG 1003	7 Devise Select bit 0 - bit 5
INTA	PLUG 1003	INTerrupt Acknowledge
7 INTP IN	PLUG 1003	INTerrupt Priority IN
7 INTP OUT		7 INTerrupt Priority OUT
LOGIC 1E		
LOGIC 1F	p19	

Designed by 801110 GR	Drawn by 801110 AMS	Dw. <input type="checkbox"/> lice Check
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it SCU 701		p20
Dwg. No. A25747	Signal List	



SIGNAL

DESTINATION

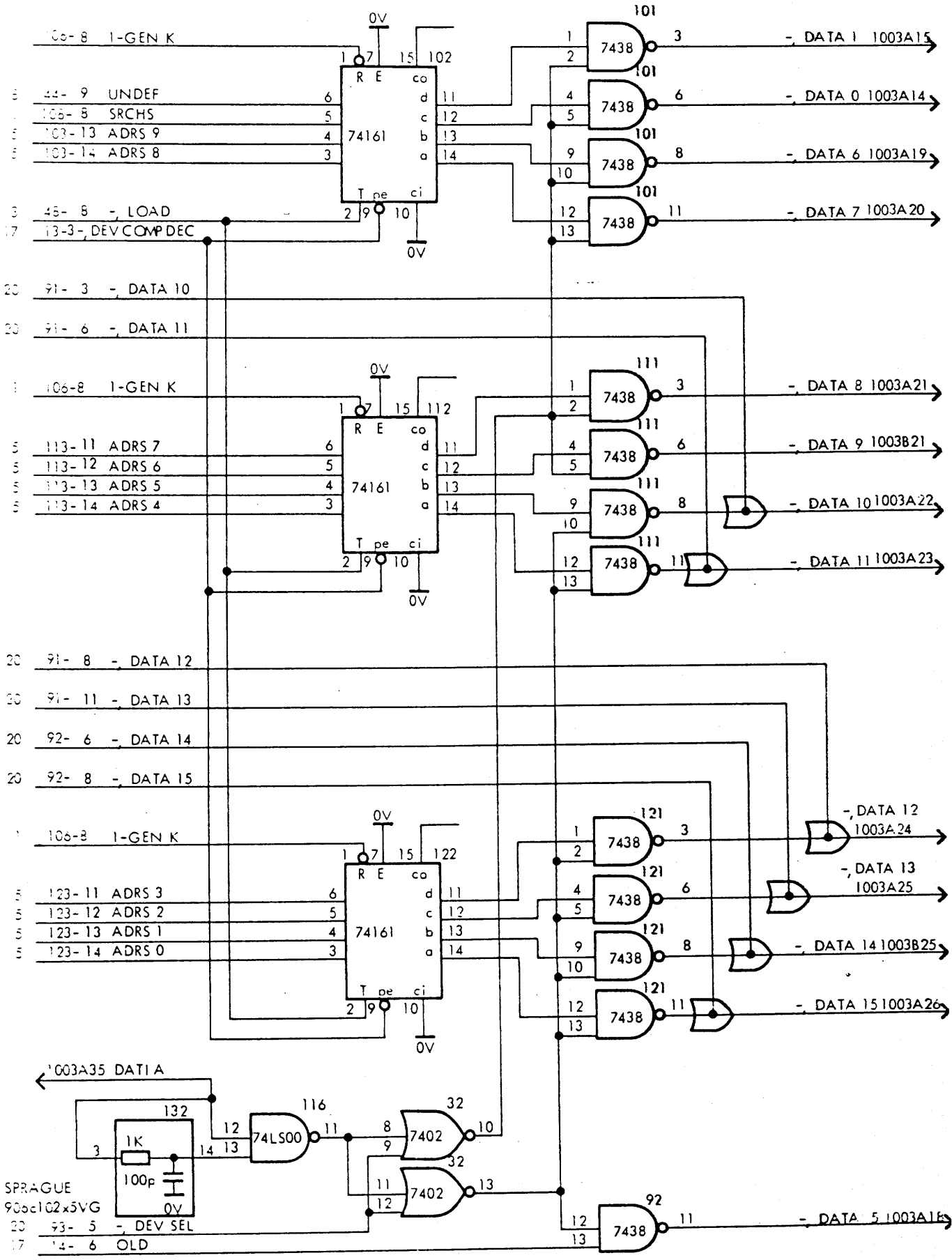
DESCRIPTION

● DATA 0 - 7 DATA 1	PLUG 1003	7 DATA Bus bit 0 - bit 1
7 DATA 5 - 7 DATA 15	PLUG 1003	7 DATA Bus bit 5 - bit 15
7 DATA A	PLUG-1003	7 DATA In A

Designed by 801110 GR	Drawn by 801110 AMS	Dwg. No. e Check
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Unit SCU 701		p21
Dwg. No. A25748	Signal List	

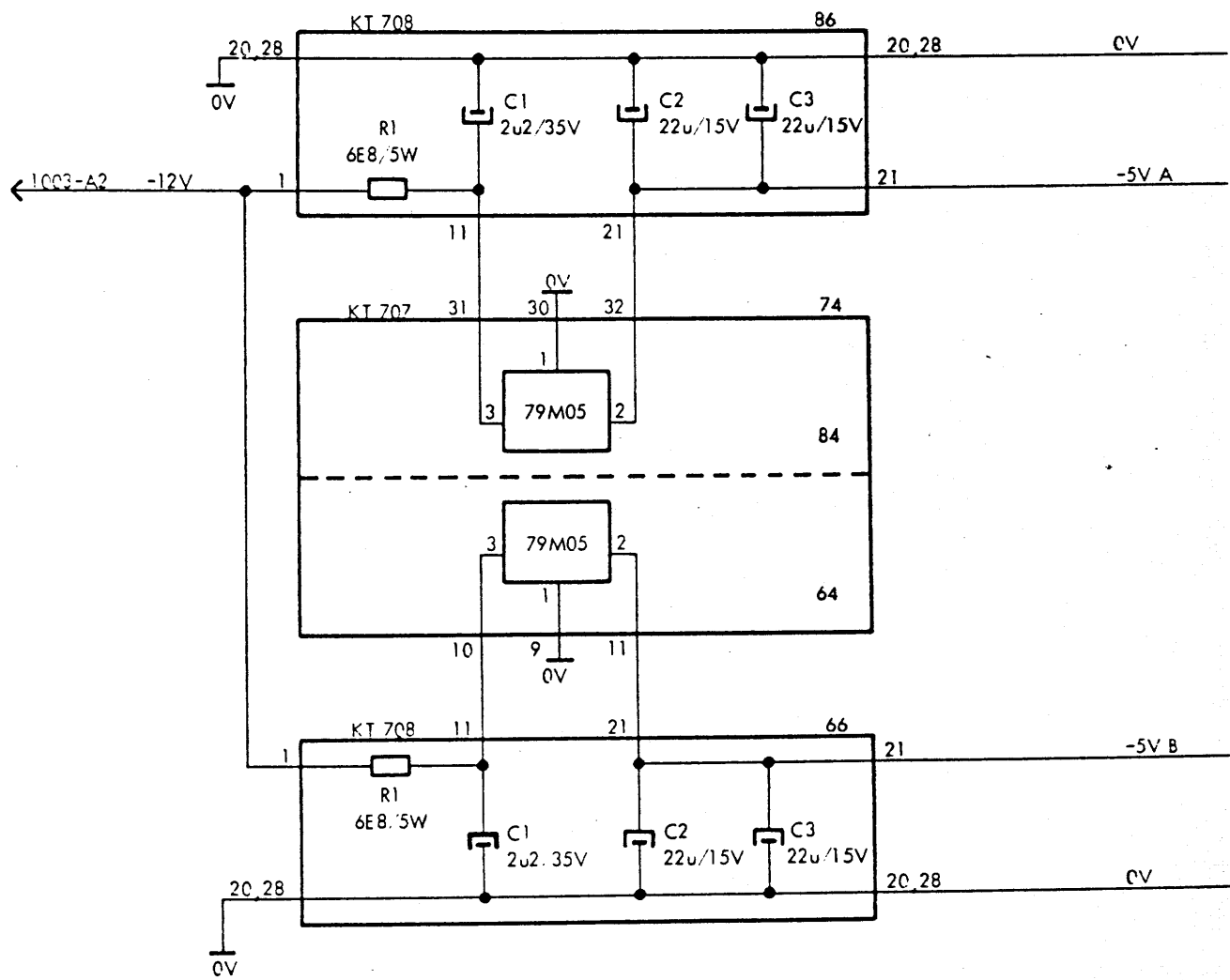
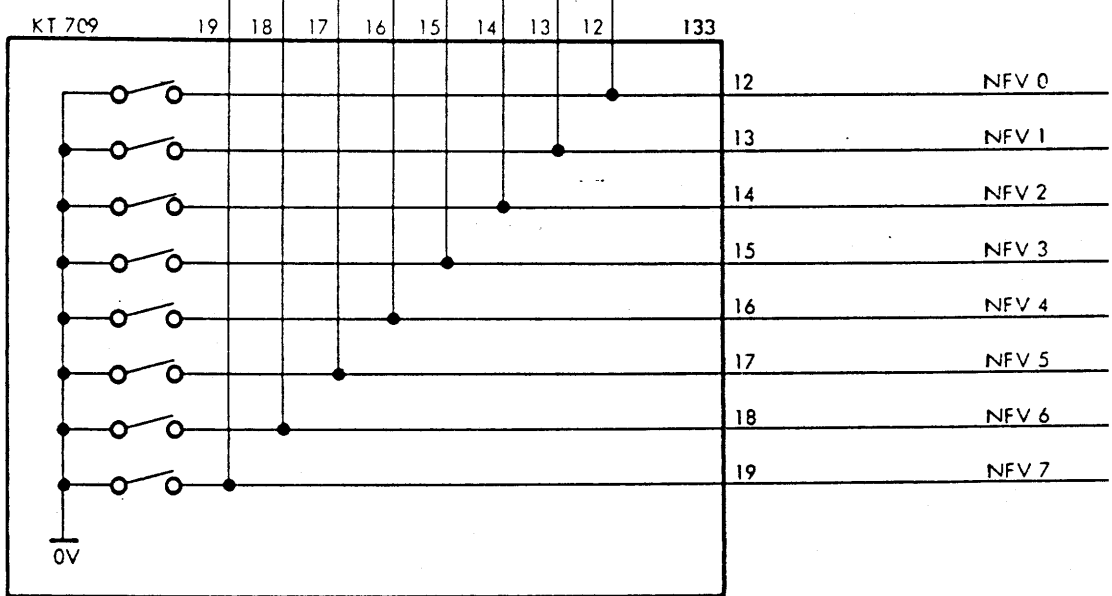
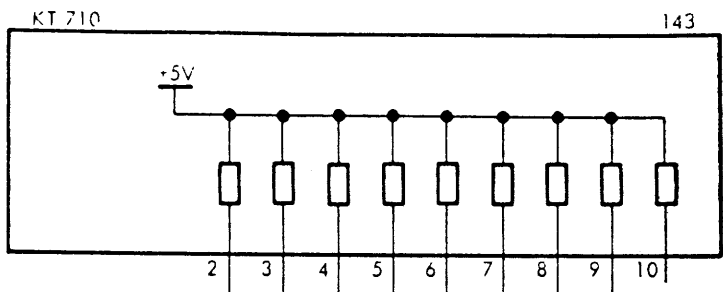
790521 ABP. Re791113 LLM R1051F GR 740116 HM



SIGNAL	DESTINATION	DESCRIPTION
NFV 0 - NFV 7	p8	Noise Filtering Value bit 0 - bit 7
-5V A	p10	
-5V B	p11	
-12V	PLUG 1003	

Designed by	801110 GR
Drawn by	801110 AMS
Dwg. Price Check	

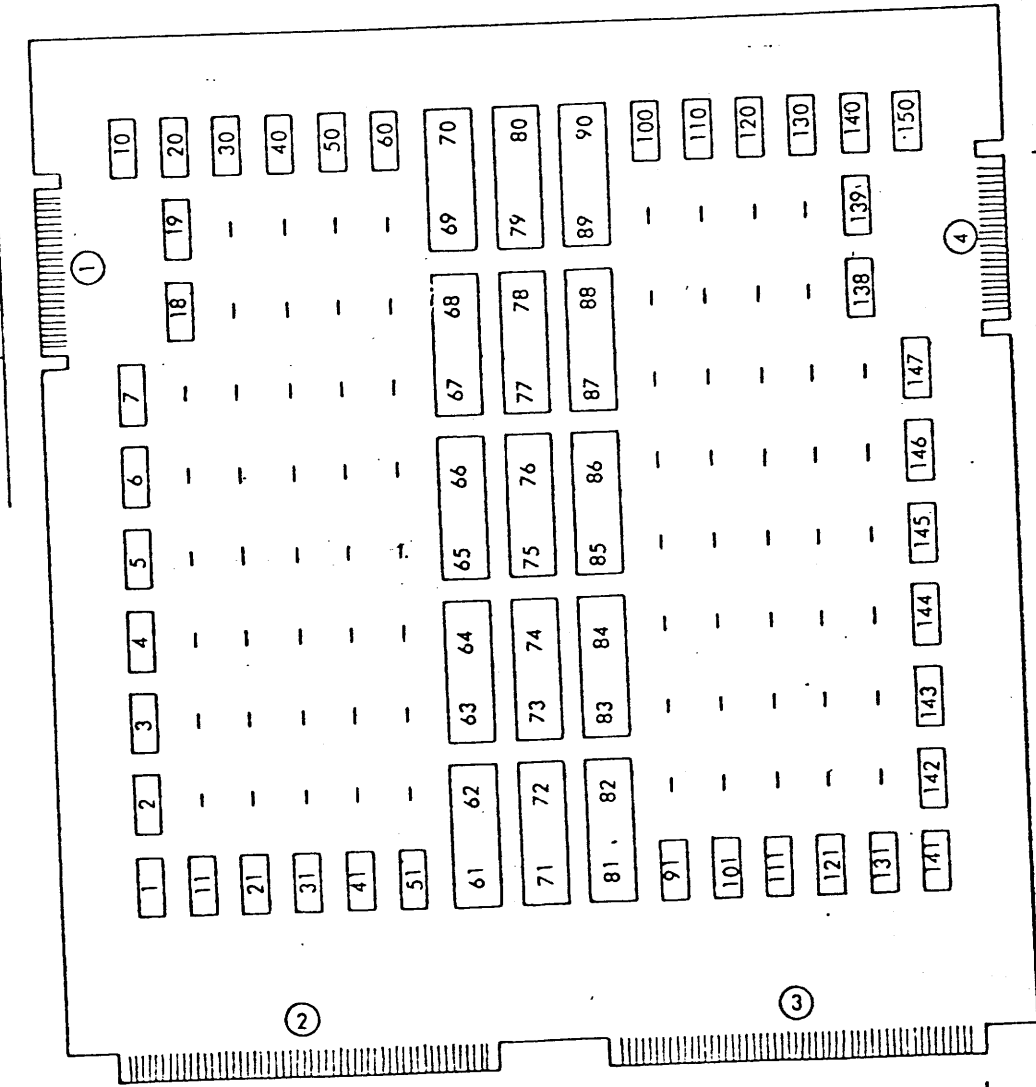
Title SCU 701	_____ _____ _____	p22
Dwg. No. A25749	Signal List	



790625 GR 791114 LLM 810518 GR

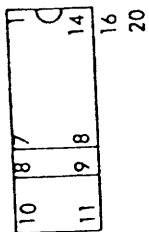
connector no. - pin no. and package position no.
(card viewed from component side)

con. no.	pin no.	comp. side
1	B25 - - - - - B1	comp. side
	A25 - - - - - A1	solder side

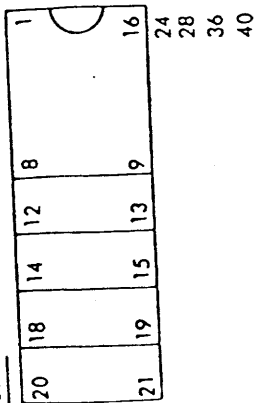


con. no.	pin no.	comp.	pin no.	con. no.
2	A49- - - - - A1	B1 - - - - - B49	3	
	B49- - - - - B1	A1 - - - - - A49		

package orientation
and pin no.



0.6"



Card Survey

CONNECTOR : J 1001

PLUG A	SIGNAL	PLUG B	SIGNAL
1	+ 5V DC	1	+ 5V DC
2	+ 5V DC	2	+ 5V DC
3	+ 5V DC	3	+ 5V DC
4	0 - ADR 0	4	0V
5	0 - ADR 1	5	0V
6	0 - ADR 2	6	0V
7	0 - ADR 3	7	0V
8	0 - ADR 4	8	0V
9	0 - ADR 5	9	0V
10	0 - ADR 6	10	0V
11	0 - ADR 7	11	0V
12	- CH 0 - 255 A	12	- CH 0 - 255 B
13	0V	13	0V
14	- CH 256 - 511 A	14	- CH 256 - 511 B
15	1 - ADR 0	15	0V
16	1 - ADR 1	16	0V
17	1 - ADR 2	17	0V
18	1 - ADR 3	18	0V
19	1 - ADR 4	19	0V
20	1 - ADR 5	20	0V
21	1 - ADR 6	21	0V
22	1 - ADR 7	22	0V
23	+ 5V DC	23	+ 5V DC
24	+ 5V DC	24	+ 5V DC
25	+ 5V DC	25	+ 5V DC

810518 GR

CONNECTOR : J 1004

PLUG A	SIGNAL	PLUG B	SIGNAL
1	+ 5V DC	1	+ 5V DC
2	+ 5V DC	2	+ 5V DC
3	+ 5V DC	3	+ 5V DC
4	2 - ADR 0	4	0V
5	2 - ADR 1	5	0V
6	2 - ADR 2	6	0V
7	2 - ADR 3	7	0V
8	2 - ADR 4	8	0V
9	2 - ADR 5	9	0V
10	2 - ADR 6	10	0V
11	2 - ADR 7	11	0V
12	- CH 512 - 767 A	12	- CH 512 - 767 B
13	0V	13	0V
14	- CH 768 - 1023 A	14	- CH 768 - 1023 B
15	3 - ADR 0	15	0V
16	3 - ADR 1	16	0V
17	3 - ADR 2	17	0V
18	3 - ADR 3	18	0V
19	3 - ADR 4	19	0V
20	3 - ADR 5	20	0V
21	3 - ADR 6	21	0V
22	3 - ADR 7	22	0V
23	+5V DC	23	+ 5V DC
24	+ 5V DC	24	+ 5V DC
25	+ 5V DC	25	+ 5V DC

800904 GR 800904 LLM