MANUAL NO. G I

TECHNICAL MANUAL

FOR THE

GIER

VOL. 4

A/S REGNECENTRALEN
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Technical Manual of GIER
Vol. IV
Descriptions of GIER

A/S REGNECENTRALEN

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Ed.: J. Routh Sørensen
A/S Regnecentralen, Rialto
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Technical Manual of GIER, Vol. IV. Descriptions of GIER

Contents

1. Introduction

The purpose of this text is to give an introduction to the technical description of GIER which implies the logical blockdiagrams, the circuitdiagrams and the wiringplans. A general knowledge of transistorized pulse- and digitalcircuits, computersystems and GIER-machine-language is taken for granted (see refs. 1,2 and 3). The mainprinciples for the machinestructure and the pulsecircuits are described in two articles which are included in this volume (refs 4 and 5).

Besides this the volume contains a list defining the logical symbols used, a text for each logical blockdiagram, specifications for bigger subunits (typewriter, tapepunch, etc.) and datasheets for transistors and diodes.

Ref. 1. A Manual of GIER-programming,
Chr. Gram, Regnecentralen 1963.

Ref. 2. Digital Rechenanlagen,
A.P. Speiser, Springer Verlag, Berlin 1961
(Pages 48-106, 283-308, 332-355 and 372-416)

Ref. 3. Design of Transistorized Circuits for Digital Computers,
Abraham I Pressman,
John F. Rider Publisher, New York 1951
(Capters 1-6 and 11)

Ref. 4. GIER
H. Isaksson and B. Scarøe Petersen
Ingeniøren, Internat.ed., Vol 5 no. 4,
København, December 1961.

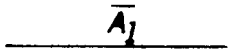
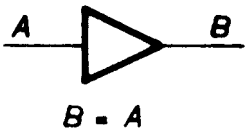
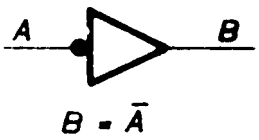
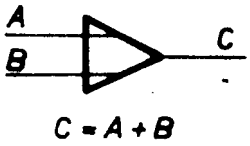
Ref. 5. GIER - A Danish Computer of Medium Size
C. Gram and others,
IEEE Transac. EC-12, No. 5, December 1963.

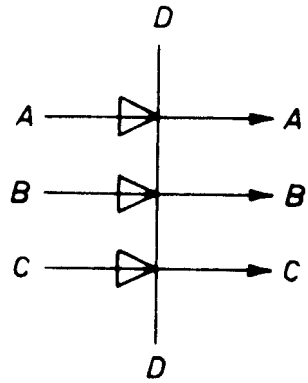
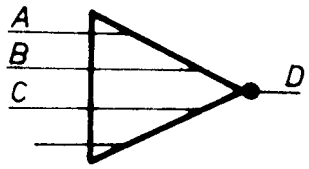
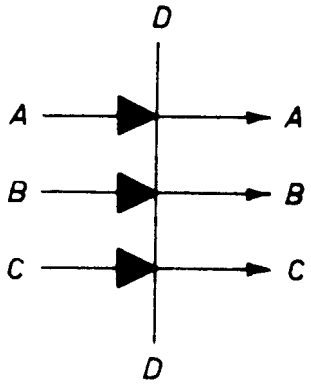
Symbols and Signs

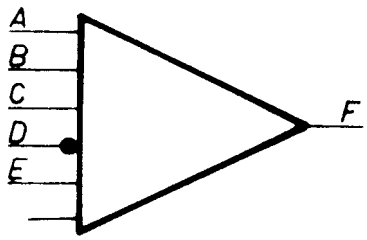
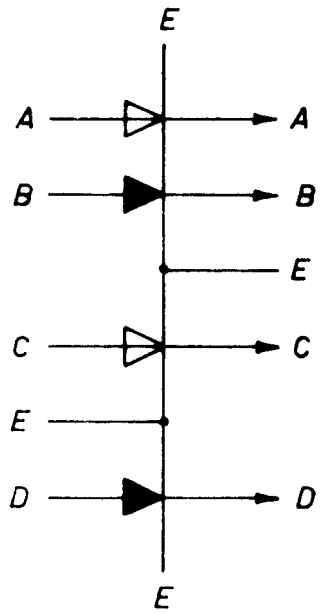
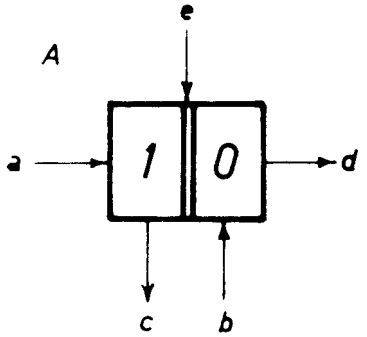
Some twenty-six logical symbols, used in describing the circuits, are explained in the following table. The next seven pages, containing this table, are numbered internally, at the bottom of each page, from 1 to 7.

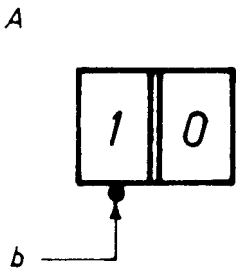
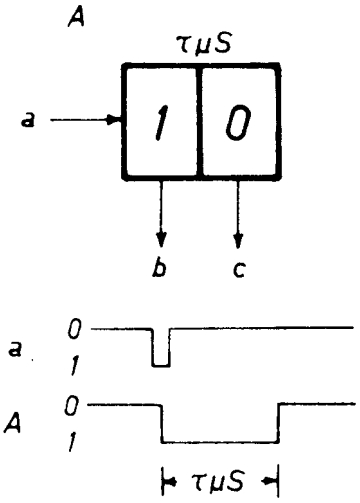
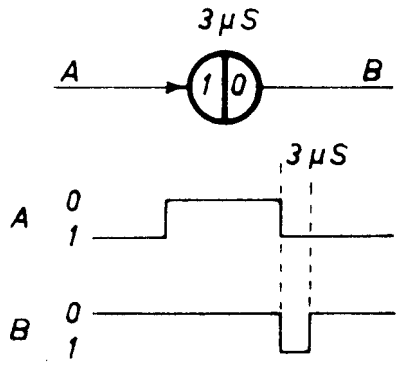
In order to facilitate a natural association between block diagram and circuit, some of the signal names bear a mnemonic relationship to the logical representation: thus, if a wire carries the logical variable A in low representation, meaning that the most negative level corresponds to logical ' 1 ' (negative logic), this is indicated by A_l in the diagram; similarly, A_h means that the ' 1 ' value of the variable is represented by the high voltage level, i.e. the most positive level (positive logic).

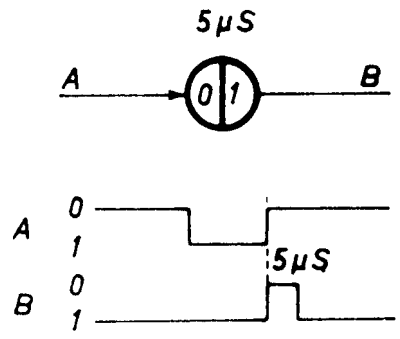
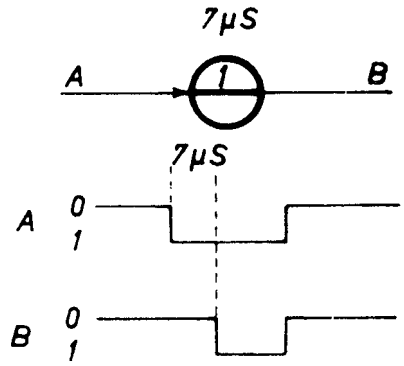
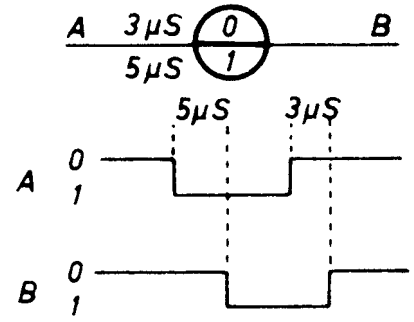
While the block diagrams represent the circuits as accurately as possible, primary emphasis has been placed on making the logical diagrams easy to understand; for this reason then, a circuit element may not necessarily correspond to a logical block or a logical block to a circuit, so that a connection between two inverter outputs, for example, may be described as an OR-gate outside of the dotted box that indicates the limits of the circuit card.

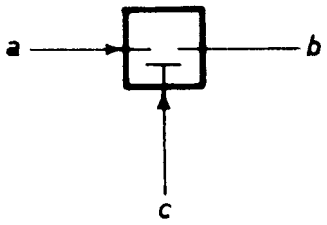
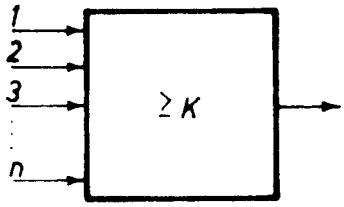
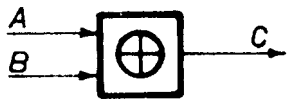
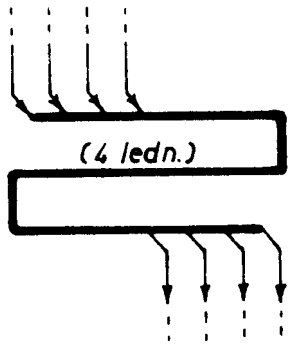
	Symbol	Description
1		Signalname, here: "A - inverted" in the circuit realized so that logical "1" corresponds to most negative level.
2		Signal path, the arrow shows the direction of the signaltransmission
3		Signal path with fan out.
4		Inverting input. The dot may be used in connection with any in- or output to a symbol
5		Amplifier or the like with no logical function
6		Inverter
7		Or - circuit.

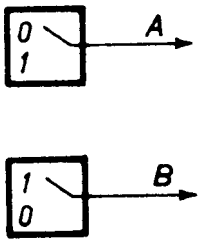
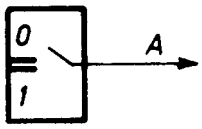
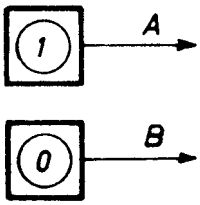
Symbol	Description
7a  $D = A + B + C$	Or - circuit Specially usefull in large systems f.ex. as encoding circuit
8  $D = \overline{A + B + C}$	Or - circuit with inverting output. Not controlled input - terminals are considered as not - exsisting
9  $C = A \cdot B = AB$	And - circuit
9a  $D = A \cdot B \cdot C$	And - circuit Specially usefull in large systems f.ex as decoding circuit.

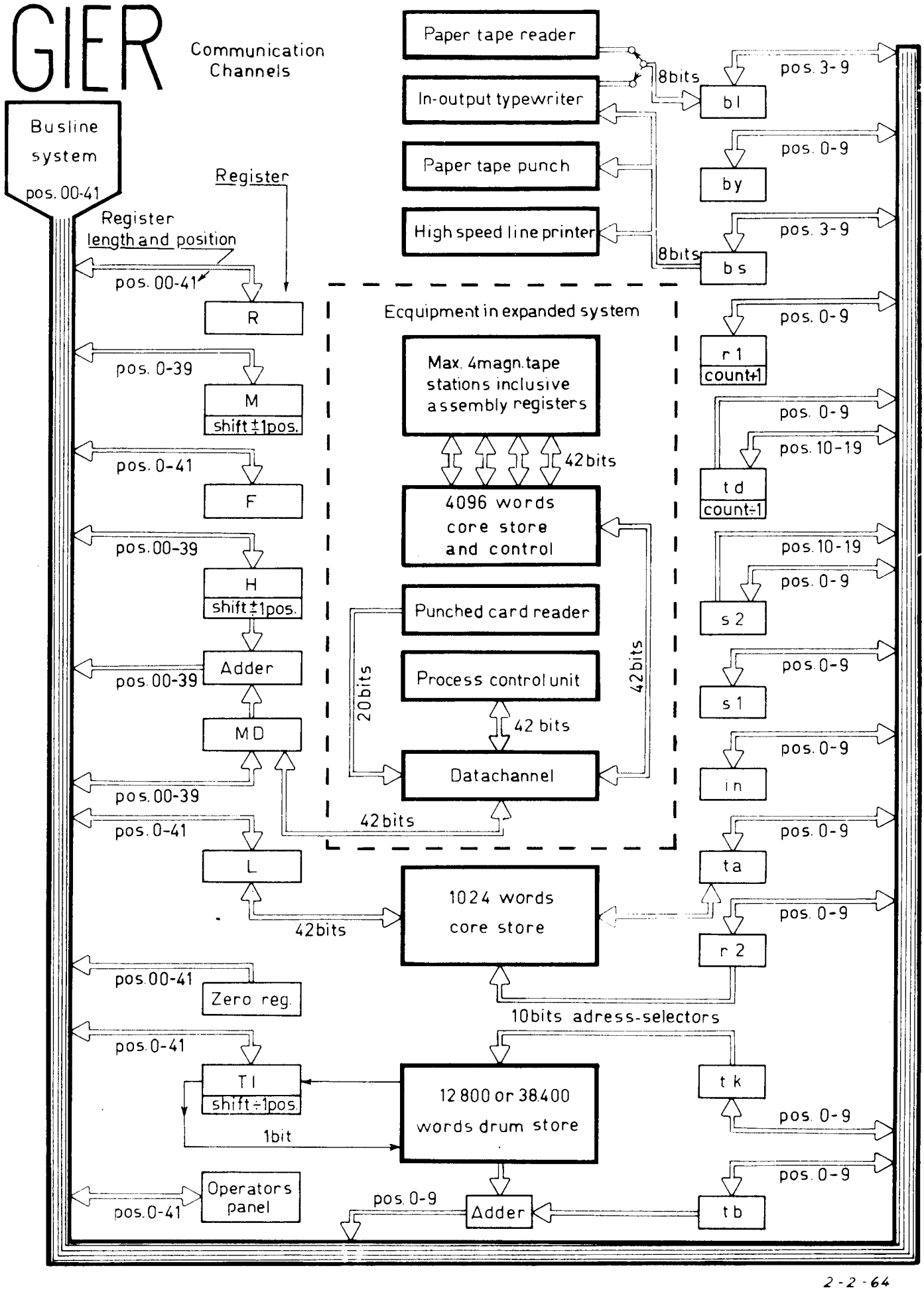
Symbol	Description
1C  $F = A \cdot B \cdot C \cdot \bar{D} \cdot E = ABC\bar{D}E$	And - circuit with one inverting input. Not controlled input - terminals are considered as not - exsisting
10a  $E = (A + C) \cdot B \cdot D$	Combined and - or - circuit Specially usefull in large systems f.ax. as busline circuit
11  	Flip - flop, 1-bit store for the variable A. Input - signals that are "0" do not influence the flip-flop. If an input to the "1" - side (a) becomes logical "1", then the variable A will be set to "1". If an input to the "0" - side (b) becomes "1", then the variable $\bar{A}$ is set "1", which means that A becomes a "0". Output-signals from the "1" - side (c) are equal to A, and from the "0" - side (d) equal to $\bar{A}$. Shift of the inputsignal upon terminal e from "0" to "1" will change the value of A (from "1" to "0" or from "0" to "1").

Symbol	Description
12 	Flip - flop with inverting input.
13 	Monostable multivibrator, 1-bit store for the variable A. Statically A is "0". If an input to the "1" - side (a) becomes "1" for a short time, then the variable A is set to "1" and stays "1" for a limited time. The time may be noted at the figure. Outputsignals from the "1" - side (b) are equal to A, and from the "0" - side (c) equal to $\overline{A}$.
14 	Circuit for differentiation. Input indicated by means of an arrow. Outputsignal is statically equal to the value noted in the output side, in this case "0". At the input side is the inverse value noted, here "1". When the input changes its value to the one noted at the input then the output signal becomes equal to the inputsignal for a limited time. The time may be noted next to the symbol

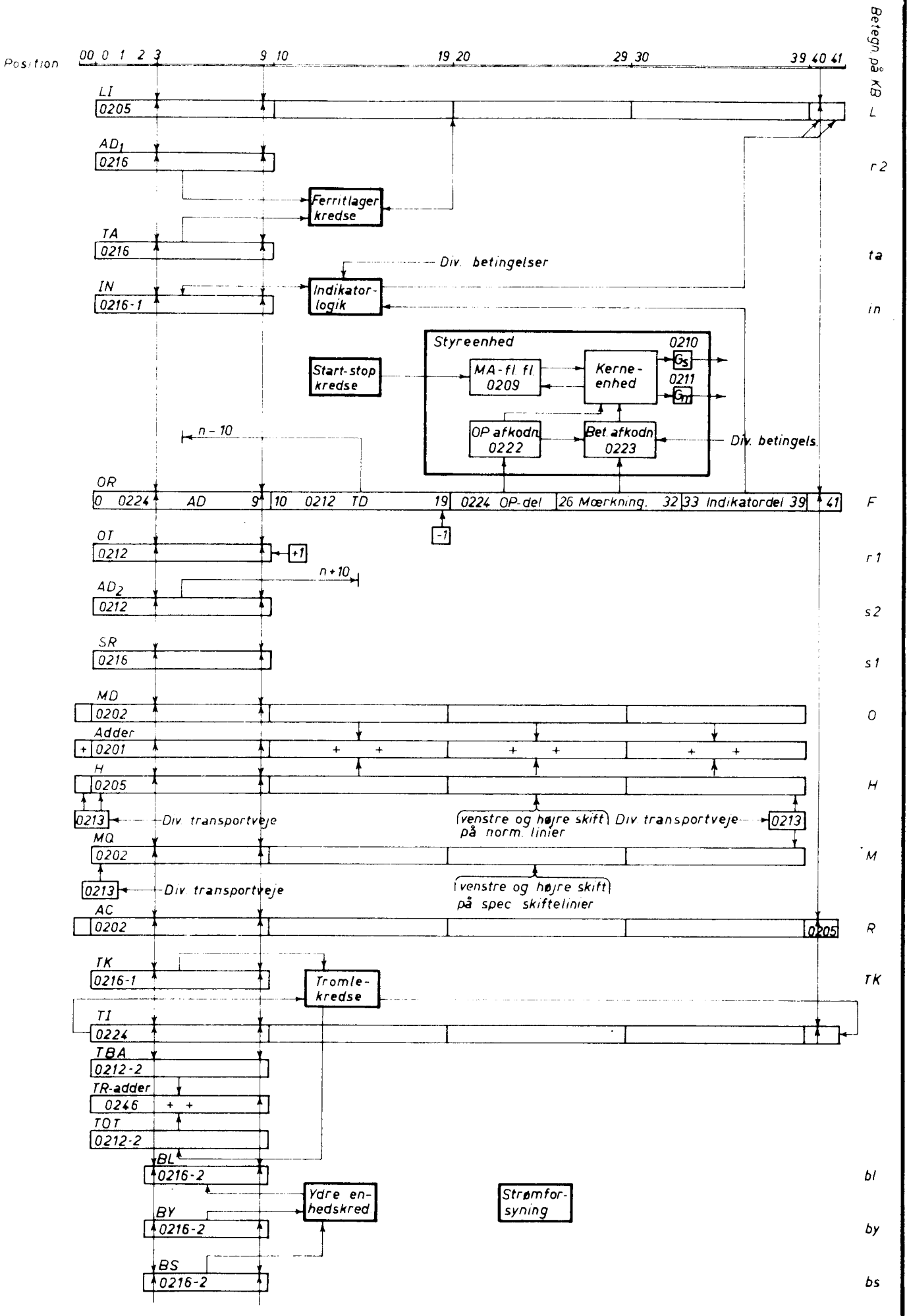
Symbol	Description
15 	Circuit for differentiation as above. The output signal is statically a "1". When the inputsignal changes from "1" to "0" the outputsignal will become a "0" for a limited time.
16 	Circuit for delaying signals. Inputside indicated by means of an arrow. Outputsignal is statically equal to the inputsignal. When the inputsignal changes from "0" to "1" then the outputsignal will remain "0" for a limited time, that is to say the value indicated in the circle (here "1") is delayed. A change of the inputsignal from "1" to "0" is transferred to the output without delay.
17 	Circuit for delaying signals as above. Both "0" and "1" are delayed by an amount of time as indicated next to the "0" - and "1" - side respectively
18 	Oscillator
19 	Oscillator generating square - waves

Symbol	Description
20 	Switch circuit with in - and out-put terminals a and b and control - input c. When the signal to the control-input c is "1" then the outputsignal b will be identical to the inputsignal. When the signal to the controlinput c is "0" the signalpath from a to b is broken, that is outputwire b is not controlled. The input to which the wire b is connected should in this case be considered as not - existing compare symbols 8 and 10.
21 	Majority circuit. The output is "1" if and only if at least K of the inputsignals are "1".
22  $C = A \oplus B = A \cdot \bar{B} + \bar{A} \cdot B$	Half - adder modulo 2.
23 	Fan - in and fan - out of signal - paths.

Symbol	Description
24  	Mechanically activated functions, f.ex. pushbuttons, with only one stable position. Outputsignal A is "0" in the stable position and "1" in the activated position. Outputsignal B is "1" in the stable position and "0" in the activated position.
25  	Mechanically activated function, f.ex. toggle switch, with two stable positions. Outputsignal A is "0" or "1" depending upon the state of the switch
26  	Signal sources for steady signals. Outputsignal A is always "1" Outputsignal B is always "0"


GIER
Communication Channels
Busline system pos. 00-41
Register
Register length and position
pos. 00-41
R
pos. 0-39
M
shift ±1pos.
pos. 0-41
F
pos. 00-39
H
shift ±1pos.
Adder
pos. 00-39
MD
pos. 00-39
pos. 0-41
L
42bits
pos. 00-41
Zero reg.
pos. 0-41
T I
shift ÷1pos.
1bit
Operators panel
pos. 0-41
Paper tape reader
In-output typewriter
Paper tape punch
High speed line printer
8bits
8bits
b l
by
b s
Ecquipment in expanded system
Max. 4magn. tape stations inclusive assembly registers
42bits
4096 words core store and control
Punched card reader
20bits
Process control unit
42 bits
Datachannel
42bits
42bits
1024 words core store
12 800 or 38.400 words drum store
pos. 0-9
Adder
r 1
count+1
t d
count÷1
s 2
s 1
in
ta
r 2
10bits adress-selectors
t k
t b
pos. 3-9
pos. 0-9
pos. 10-19
pos. 0-9
pos. 10-19
pos. 0-9
pos. 0-9
pos. 0-9
pos. 0-9
pos. 0-9
pos. 0-9
pos. 0-9
pos. 3-9
pos. 0-9
pos. 0-9

2-2-64



REGNECENTRALEN Dansk Institut for Matematikmaskiner	Udvikl.			BLOKSKEMA OVER REGISTRE	GIER
	Ajour	20-6-63 PTN			1.1

4. Start-stop circuits

The clockpulses from the 450 KHz oscillator are distributed to different parts of the machine controlled by signals from the pushbuttons on the operators panel.

There are in priciple 3 different output-clockpulses:

1. KPA and KP.A which drives the microaddress flip-flops and gates in the control unit during normal operation.

2. KPB and KP.B which drives the special microaddress flip-flops and gates in the control unit during a drumtransfer function.

3. Display and 'zero to all lines' which drives the register-display-system that is active when the machine is stopped.

Besides this there are some special pulses (Sp-adder, SpH and SpMQ) which controls the shortterm-memories in the outputs of the adder and the registers H and MQ.

The distribution of clockpulses is controlled by means of the flip-flops VAC and VAB.

The flip-flop VAT is only one when the special testmicroprograms are activated by means of the switch in the central processor.

When VAC = 1 the outputgates for the display-system are enabled.
When VAC = 0 the machine is running and gate 5 on card 249 is enabled.
If VAB = 0 gate 5 will send outputpulses and KPA and KP.A will be active. If VAB = 1 gate 5 will be closed and gate 7 open so that KPB and KP.B will be active.

It is seen that if VAC = 1 and VAB = 1 gate 7 will still be active while display is inactive. This means that a drum transfer may be finished after VAC has been set to 1.

The primary clockpulse is interrupted in the following situations: after execution of microoperation Gmstep (1 clockpulse is removed), when VAC or VAB are changing or when pushbuttons are activated.
The logic around VAB is syncronizing the drumoperations and the clock-pulse, and makes sure that a core-memory cycle is not interrupted by the drum.

5. Core Store

The timing-circuits for the core-store are controlled by means of 6 flip-flops (cards 221) one for each type of core-store function as seen from the microprogram. These signals are coded together to a central start-signal: Start FL which will originate a number of pulses spaced in time, (nul KL, LPX primær, LPY, etc.). The timing is shown in the block-diagram.

The decoding is working as concidence-gates via the memory-wiring. The 10-bits address, selected from either TA or AD_1 on cards 206, is split up so that pos. 0,1,2 selects one out of 8 groups of wires in the X-side of the top of the core stock, while bits pos. 8,9 selects one out of 4 wires af the mentioned actual group in the X-side of the button of the core stock. In the same manner pos. 5,6,7 and pos. 3,6 select one Y-wire.

The gates on cards 203-1 are symmetrical allowing both the read and write currents to pass the same circuits, while the gates on cards 207 have separated circuits for the read and the write currents.

6. Drumstore.

Main principles of control.

Transfer of information between the drumstore and the core store is divided up in a drum-synchronous serialtransfer between the drum and the buffer-register TI and a GIER-synchronous paralleltransfer between TI and the core store. The drumsynchronous transfer is performed by the drumcircuits simultaneous with the execution of instructions not concerning the drum. The corestorageadress to or from which the drumtransfer shall be done, is also calculated by the drumcircuits simultaneous with normal operations. At the moment when the drumcircuits are ready for the parallel transport the execution of simultaneous operations is interrupted for about 26 μS while the paralleltransfer to or from the core store is going on. This is done by a special microprogram which is activated by means of a special set of 8 microaddresses, MAB 1-8, and a special clockpulse, KPB. The time-interval between the 4o interruptions during a channel transfer is about 5oo μS.

Channel selection.

Selection of the channel to or from which a transfer is wanted is done by execution of the operation VK by which the channel number modulo 512 is transferred to the register TK. Any channel-transferoperation is normally executed on condition that an existing channel has been selected. If a transfer to a nonexisting channel is executed (no. 32o-511 or 832 - 1o23) the drumcircuits will be occupied the normal time (about 21 ms). After this the situation is unchanged in the store. If a transfer from a nonexisting channel is executed the corresponding cells in the core-store will be set to zero and the computer will not finish the LK-operation untill the pushbutton "annul. of the TR-paritet" is activated.

The 32o channels in the drumstore are mechanically represented by 32o read-writeheads, which are individually wired to 4o plugs (A2-A11, B2-B11, C2-C11 and D2-D11), but electrically they are separated in 2o groups each containing 16 channels. The read-write heads are decoded from the TK-register. Bits 1-5 (numbers according to the buswire no.) are decoded to an X-value: 1 out of 2o possible (12 are not used) and bits 6-9 are decoded to an Y-value: 1 out of 16 possible. These X- and

Y-values are defining the selected track, and this last part of the decoding is performed by means of the diodes placed in the plugs sitting upon the drum. This part of the decoding in only active during the execution of the operations LK or SK.

Changing of the contents of the TK-register during a channel-transfer is impossible due to the signal "block Gm TK" from card 2o5-4.

Locking for writing.

Some of the drumtracks may be locked for writing. The locking can be done in two levels. The first level comprises normally track no. o-31.. This lock is manually operated and is accessible to the user. It is possible to expand this locking to comprise up to 5 groups of 16 tracks by connecting the X-group in the decoding to one of the spare-inputs upon card 2oo-4. For instance a connection between the pins C3-2o-15 and C5-21-12 will expand the lockingarea to tracks o-47.

The second level of locking comprises normally only track no. 0, and is not accessible to the user. Unlocking can be done by removing the short circuit pin upon card 2oo-4. This locking may also be expanded so that it comprises up to 16 tracks, no. o-15, by connecting the appropriate Y-group in the decoding to C3-24-1N.

The execution of an SK-instruction where the selected track has been locked will be finished without writing during 9 µsec. for the basic-operation plus the normal executiontime for the modifications.

Clocktracks.

The drum is equipped with 3 clocktracks and associated readamplifiers. Clocktrack no. I contains one mark for detecting word no. 0, track no. II a marking for each of the 4o words, and track III a marking for each bit in all words.

Transfers to and from the drum.

The microprograms for the druminstructions LK and SK begin with the micro•peration "Gm sæt TL" which will read the value of the signal TR" into the flip-flop TL upon card no. 266. If TL becomes 1 it means that the drumcircuits are unoccupied (TL means "Tromle ledig" or "drum ready"), and the microprogram will proceed with starting the drumcircuits by means of the microoperation "Gm start TR", which will set one of the flip-flops upon the card 264 dependent on whether it is a write-or a read-operation. This flip-flop will remain set during the drumaccess and will select the correct microprogram to be executed at the interruptions when words are transferred to or from the core store. The syncronizing signal to the start-stop circuits SL ("skriv-læs" means ready for write to or read from core memory)is derived from this flip-flop and clockpulse II. The delay of 12 μsec. upon card 261 is nescessary due to the parity check (see later).

As the drum acces is initiated non-syncronous to the drum, the serial transfer of information from the drum to the TI-register may start in the middle of a word, so that the first word transferred to the corestore is not correct. The drumacces is therefore always transferring 41 words so that the first word in the acces is beeing transferred 2 times where the last one is always correct. The counting of the number of words transferred is done by means of the counting register TKT. This register is cleared (set to zero) at the beginning of a drumaccess (and when a parityfault occurs in a word). When the contents of TKT is 41, the drumacces is finished by resetting the flip-flop upon the card 264.

If a SK-instruction is initiated during the word-time of word no. 39, the 41'st counting pulse to TKT will finish the drumaccess just before the second and correct writing of word no. 39 occurs. To prevent this, an extra clearing of TKT is being executed just before word no. 0 is written the first time in the above mentioned situation.

Addresscalculation.

The resultant address of a LK or SK-instruction is transferred to the TBA-register. The TOT-register always contains the word no. of the word thas has just passed the read/writehead. The sum of TBA and TOT is calculated by means of the drumadder. This number is the corememoryaddress to where the word from the drum shall be transferred at the storing-interruption during execution of a LK-instruction. In case of the SK-instruction this sum from the drumadder has to be increased by one to give the address in the corememory wherefrom to fetch the word that shall be written upon the drum. This is done by setting the carryinput of the lowest position of the adder to the value 1. When word no. 0 is to be transferred the contents of TOT must be -1 this value is set into TOT during wordtime 39.

The contents of register TBA cannot be seen from the display in the operators panel, but by means of a DM 160 lampcard placed in A1-23.

During the B-microprograms which executes the transfers between the corestore and the drumstore the output from the drumadder is transferred to the TA-register and the inputs to the addressdecoding of the core store are connected to TA instead of AD1. This shift of them decoding is done by means of a flip-flop upon the card 266.

Wordtransfer.

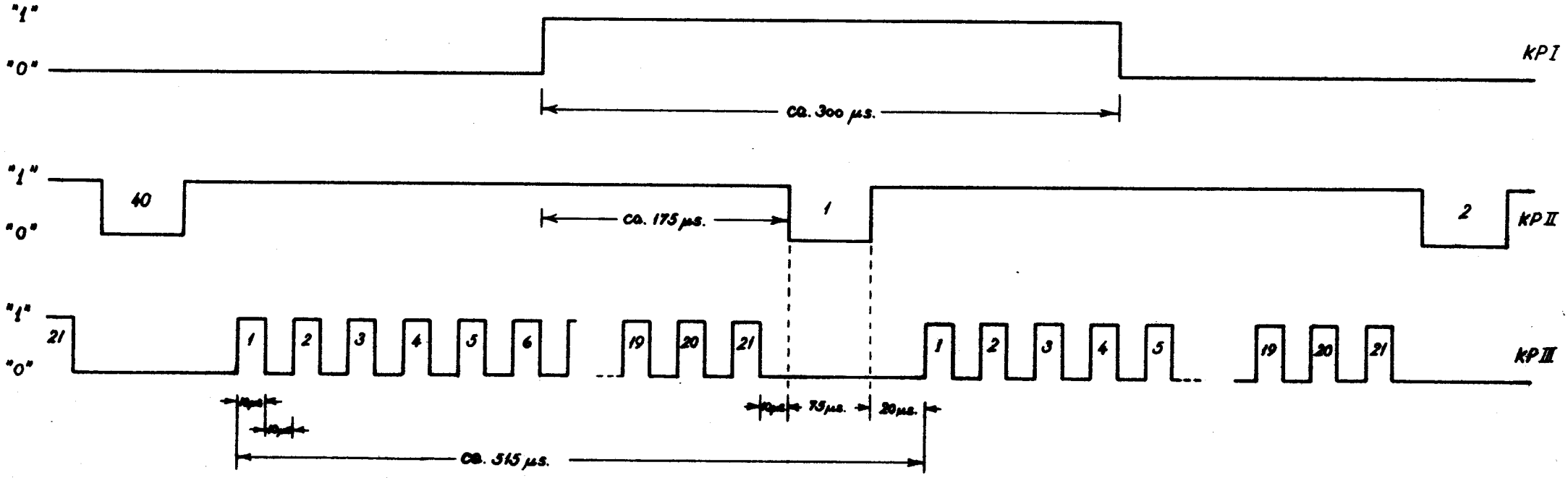
The serialtransfer between the drum and the bufferregister TI is performed one bit at a time, the contents of TI beeing shifted one position to the left for every bittime. During writing upon the drum the signal for controlling the write amplifier is taken from TI-position 0 while during reading the output from the readamplifier is connected to TI-position 41. The shiftpulse for TI is derived from clockpulse III and II, the shifts being performed at the times where the value of clockpulse III is changing from 1 to 0 and from 0 to 1 and where clock-pulse II changes from 1 to 0. The principle of writing that is used is called NRZ, non-return-to-zero, because the current in the writehead is always running one or the other way. It is shifting at the beginning of words, at every bit = 1 in the words and after the finish of a word if the number of 1's was even.

The signal from the read amplifier is setting a flip-flop which again steers another flip-flop strobed by a signal derived from the clock-pulses. After this the shifting begins in a flip-flop called TI-pos.42. The last bit that is read in a word-time is the paritybit, which remains in TI-pos. 42 during the succeeding paralleltransfer to the corestore. At the shifting-in into TI of the next word from the drum, the proceeding word is shifted out through TI-0 and is lost.

Paritycontrol.

The paritycheck at reading claims that every word including paritybit contains an odd number of ones. The "ones"are counted by means of a flip-flop upon card 263. At the end of a word-time this flip-flop must contain a 0 indicating correct parity , at the beginning it contains 1. If this is not so the signal SL will via the logik cause a resetting of register TKT and the transfer will start from the beginning. If the fault continues the tracktransfer will never finish, unless the operator cancel the paritycheck by means of the switch "Annul.tr.paritet" (The red lamp will light when the check is inactive). Operating the "Reset"-button will as usual stop every action.

Simultaneously with the resetting of TKT because of parityfault another flip-flop upon the card 263 will be set, and later it will be reset when TKT = 41. This flip-flop will light the lamp at the operatorspanel called "Tromlefejl" indicating error in the drum. Because of the non-syncronous start of reading from the drum, the first word read is often with parityfault. To prevent the lamp from lighting for this reason, there is a delay between the flip-flop and the lamp.



GIER drumcircuits

Clockpulses I, II and III

1. Peripheral Unit Circuits

Note

In publishing this English version of 'Description of Peripheral Units Circuits', it has seemed advisable to include a list of the new English designations on the Display Panels and word lists for the designations employed on the various flow charts and block diagrams, retained herein with Danish text. Accordingly, a brief word list, containing the Danish terminology and English equivalents, follows each flow chart. A similar word list is given for each block diagram. These block diagrams are however inserted in Vol. I of GIER Technical Manual. The list of Display Panel designations is inserted after Contents.

The gap in page numbers between 7-2a and 7-11 is due to the fact that these pages have been inserted as chapter 2 of this volume.

20 June 1965/ HAZ.

Contents

Display Panel Designations

Note: The following English abbreviations and terms have been suggested to replace the present Danish designations on the Display and Auxiliary Display Panels of the GIER Computer.

DANISH	ENGLISH	MEANING
Manøvrebord	Display Panel	
YE	PD	Peripheral Device
SF	PS	Power Supply
TO	VO	Void Operation
TR	DP	Drum Parity
L	TP	Tape Parity
INDIKATOR	INDICATOR	
KLAR	IDLE	
FEJL	FAULT	
ADRESSEDEL	ADDRESS	
TÆLLEDEL	INCREMENT	
GRUNDOPERATION	BASIC OPERATION	
NORMAL: START/STOP	START/STOP	
HØJTALER	LOUDSPEAKER	
MIKROTEMPI: START/STOP	STEP/RESET	
Hjælpemanøvrebord	Auxiliary Display Panel	
Klar	Idle	
YE	PD	Peripheral Device
Str. læs. par. fejl	PT Parity	Paper Tape Parity
Tromlefejl	Drum Parity	
TO fejl	Void Op.	Void Operation
HP spærret	HP Inhibited	
i-løkke	Addr. Looping	Address Looping

All other designations on these two Panels remain unchanged.

A Short Description of the Peripherals

The GIER computer is equipped with a paper tape reader, a punch for 8-track tapes, and an input/output typewriter.

Since an LY (LY=les ydre=read peripheral) operation and an SY (SY= skriv ydre=write peripheral) operation respectively cause the input and the output of only one character or row of holes, both input and output take place one character or row of holes at a time.

These basic peripheral devices are connected to the computer via 10-bit registers in the buffer. The typewriter is an exception to this however, since punching a key takes much longer than the time required by the computer itself to place data from the typewriter in the AC register directly from the buslines.

The registers in the buffer utilize only the 8 least significant positions (pos. 2-9), plus pos. 0 in the bl register.

The connection of the individual peripherals is controlled by the BY register.

Peripheral Selection

Selection of the peripheral device is achieved with the VY (VY=velg ydre-select peripheral) operation (OP 51). As may be seen from the flow chart for the VY operation, the modified address is placed in the BY register with the increment part of the instruction as a mask, where the postitons with one-bits in the increment part of the operation are not changed.

If the operation has no increment number, this is regarded as zero, and the entire modified address is placed in the BY register.

In the BY register, positions 3-6 are reserved for selection of output devices and positions 7-9 for selection of input devices.

Input devices are

tape reader,
typewriter, and
card reader.

Output devices are

typewriter,
punch, and
line printer.

In addition, a group of 16 buttons on the Auxiliary Display Panel makes it possible to activate one or more output devices simultaneously through manual selection. The arrangement of these manual selection buttons is shown on the next page.

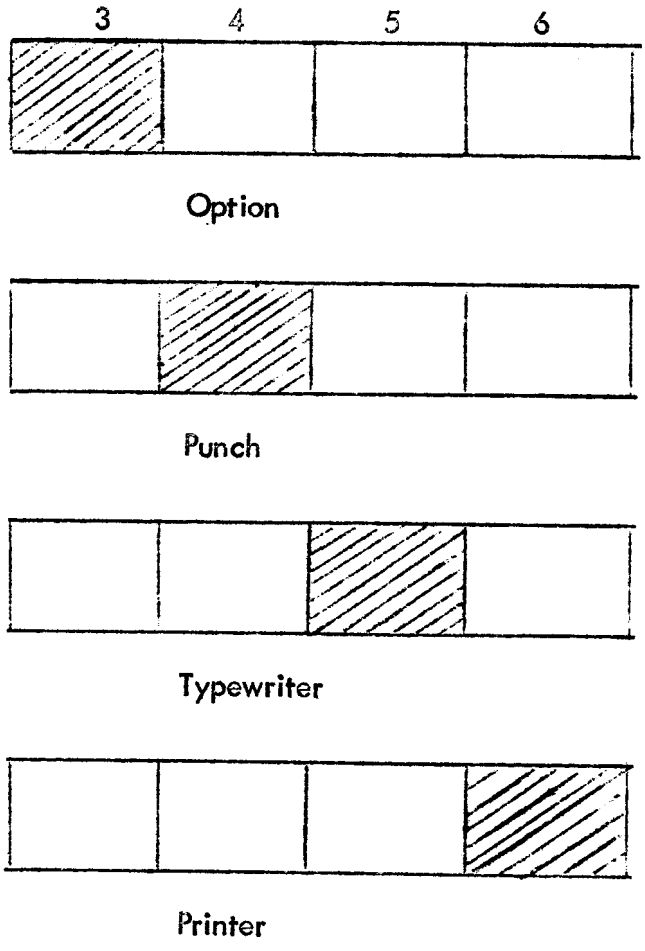
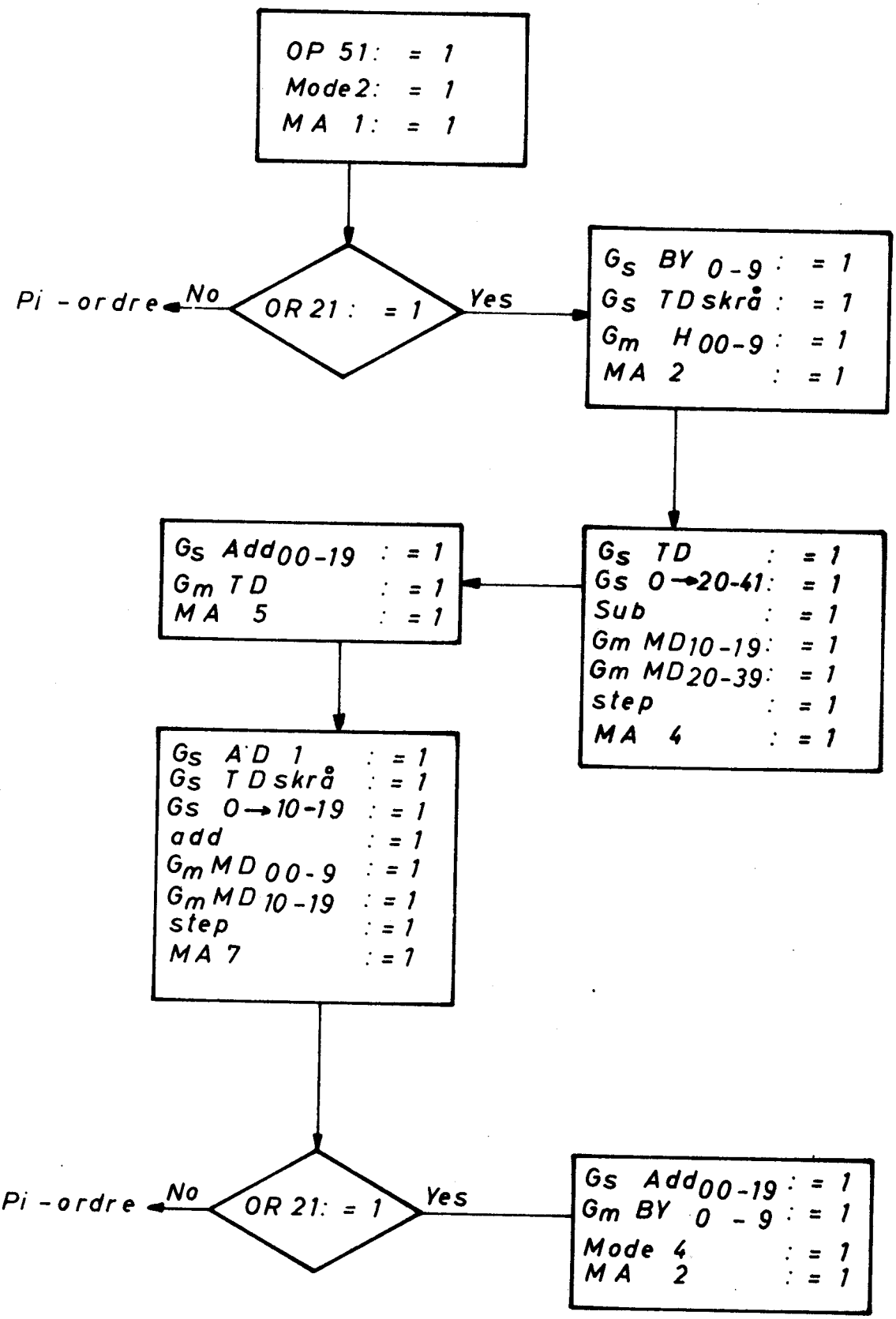


Illustration of the Arrangement of the Manual Selection Buttons on the Auxiliary Display Panel

The appropriate peripheral device(s) is selected according to which position(s) in the BY register is set and which button(s), corresponding to this position, is depressed.

VY-ordrens Flow-card



VY-ordrens Flow-card

Pi - ordre

TD skrå

Flow Chart for the VY Operation

Pi - operation

TD cross

Input via Peripheral

The GIER Computer operates with a clock cycle of approximately 450 kHz (2.2μsec.), and therefore cannot be employed in direct conjunction with peripheral devices, since the latter are engaged in input/output that involves differing lengths of time, e.g.:

typewriter	ca.	100 milliseconds,
tape reader	ca.	0.5 - 2 milliseconds, or
punch	ca.	8 milliseconds.

Accordingly, the computer must receive indication from the peripheral that the latter is 'ready' to respond to instructions for input/output or that it is 'busy' with input/output.

A sense-busy signal, micro-operation Gmj, is therefore included in the built-in microprograms for input/output , which if the computer receives the 'busy' signal from a peripheral, causes the former to wait until the 'ready' signal, j klar, is received, which then allows the computer to proceed in the microprogram.

The LY operation (OP 59) is employed for input via peripheral to the computer. As may be seen from the flow chart for the LY operation, three conditions, are involved, viz.:

condition 1 : $BY\ 8 \cdot \overline{BY\ 9} := 1$,

condition 2 : $BY\ 8 \cdot \overline{BY\ 9} + \overline{BY\ 8} \cdot BY\ 9 := 1$, and

condition 3 : $jLY := 1$.

Condition 1 distinguishes between card reader selection or tape reader and typewriter selection.

Condition 2 distinguishes between tape reader selection or typewriter selection, so that selection is now possible among all three devices.

As may also be seen, selection is achieved via positions 7-9 of the BY register in the following fashion:

BY 8	BY 9	
0	0	tape reader selection,
0	1	typewriter selection,
1	0	card reader selection, and
1	1	tape reader input without parity stop.

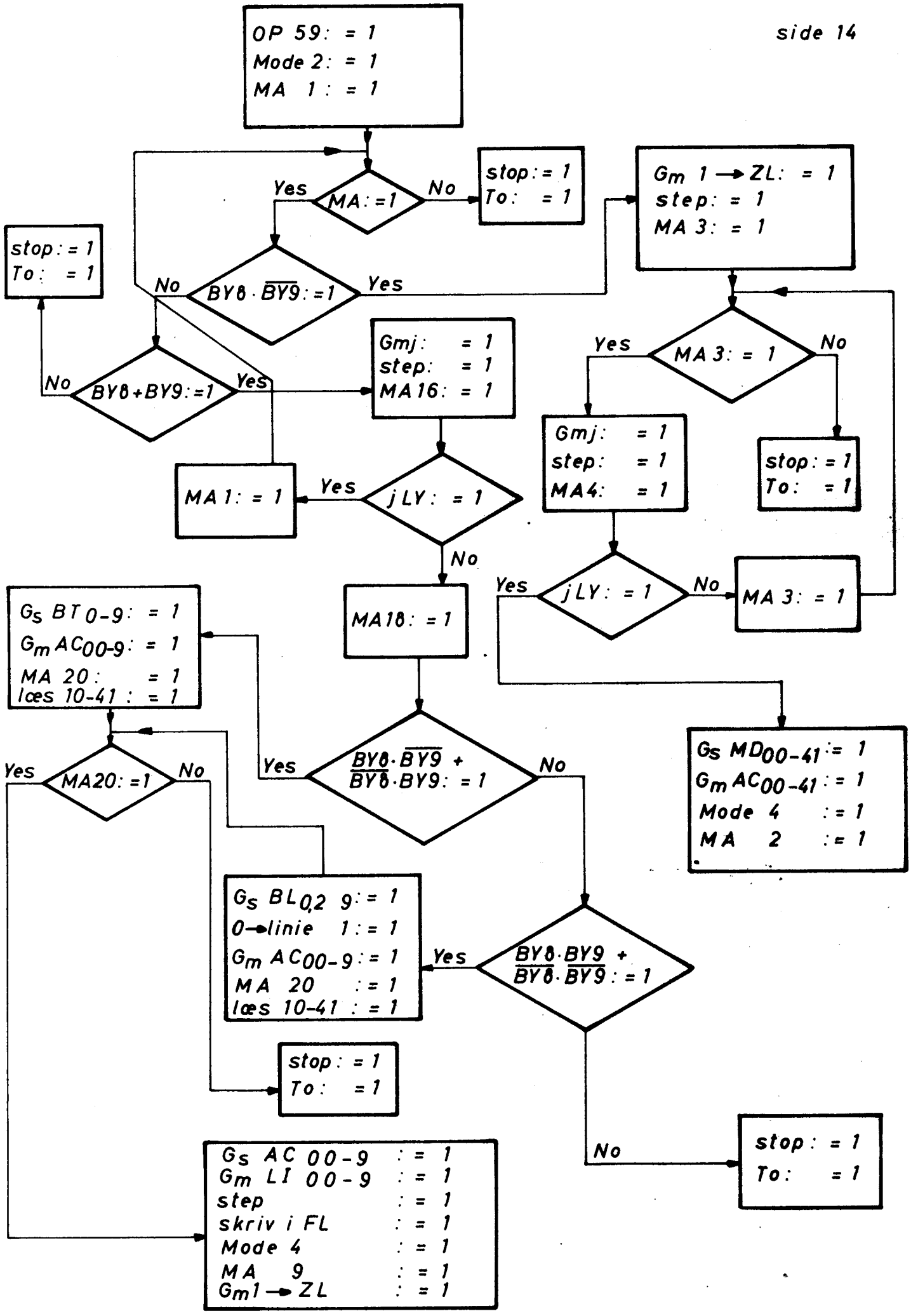
Condition 3 distinguishes between 'busy' and 'not busy', received from the peripheral, in the following manner:

¡LY := 1	peripheral 'busy' with input, or
$\overline{¡LY}$:= 1	peripheral 'not busy' with input.

As may be further seen from the flow chart for the LY operation, if the computer receives ¡LY := 1, it jumps back to MA 1 and begins to send the sense-busy signal, micro-operation Gmj, continuing until $\overline{¡LY}$:= 1 is received.

Additional information on input is contained in subsequent sections, viz. Tape Reader Input and Typewriter Input.

LY - ordrens flowcard



LY-ordrens flowcard

læs 10-41

linie 1

skriv i FL

Flow Chart for the LY Operation

read 10-41

line 1

write in FL

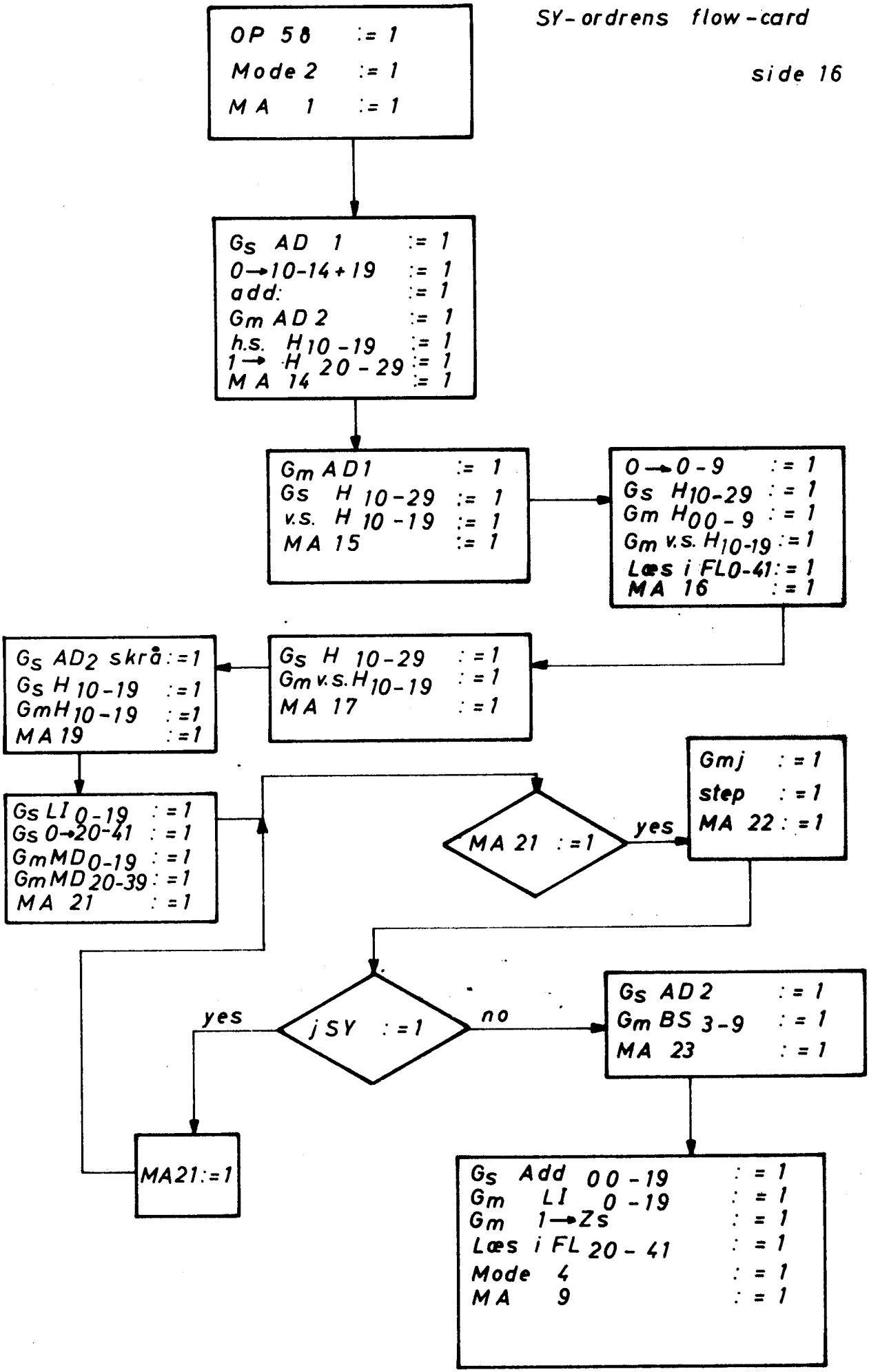
Output via Peripheral

Output via peripheral is achieved by means of the SY operation (OP 58). As may be seen from the flow chart for the SY operation, the seven least significiant positions of the modified address are transferred to positions 3-9 in the BS register.

If the typewriter is selected, the character that corresponds to the contents of the BS register is now written. If the contents of the BS register, however, are such that there is no corresponding character on the typewriter, then this operation merely causes the transfer of the address to the BS register, after which the computer contimues -- without write-out on the typewriter -- with the next operation. The same time is required for writing both existent and non-existent characters.

At least ca. 100 milliseconds must follow such a character, before the next SY operation can be executed, i.e. not until the computer has received the j klar signal from the typewriter.

LOWER CASE (selected by means of the SY 58 operation) causes the write-out of all succeeding characters in lower case, until the SY 60 operation for UPPER CASE is executed, after which all succeeding characters are output in upper case -- this applies however only to output on the typewriter.


OP 58 := 1
Mode 2 := 1
MA 1 := 1
Gs AD 1 := 1
0→10-14+19 := 1
add: := 1
Gm AD 2 := 1
h.s. H10-19 := 1
1→ H 20-29 := 1
MA 14 := 1
Gm AD1 := 1
Gs H 10-29 := 1
v.s. H 10-19 := 1
MA 15 := 1
0→0-9 := 1
Gs H10-29 := 1
Gm H00-9 := 1
Gm v.s. H10-19 := 1
Læs i FL0-41 := 1
MA 16 := 1
Gs H 10-29 := 1
Gm v.s. H10-19 := 1
MA 17 := 1
Gs AD2 skrå := 1
Gs H 10-19 := 1
GmH10-19 := 1
MA 19 := 1
Gs LI 0-19 := 1
Gs 0→20-41 := 1
GmMD0-19 := 1
GmMD20-39 := 1
MA 21 := 1
MA 21 := 1
yes
Gmj := 1
step := 1
MA 22 := 1
jSY := 1
yes
no
Gs AD2 := 1
Gm BS 3-9 := 1
MA 23 := 1
MA21 := 1
Gs Add 00-19 := 1
Gm LI 0-19 := 1
Gm 1→Zs := 1
Læs i FL 20-41 := 1
Mode 4 := 1
MA 9 := 1

SY-ordrens flow-card	Flow Chart for the SY Operation
h.s.	right shift
v.s.	left shift
læs i FL 0-41	read in FL 0-41
skrå	cross

Tape Reader Input

The condition for tape reader input is $BY\ 8 \cdot BY\ 9 + \overline{BY\ 8 \cdot BY\ 9} := 1$. When a tape has been placed in the reader, the first character on the tape must be placed in the BL register.

This is done in the following manner: when the push-button for one-hole drive is pressed, the signal is fed via KB 8-B to the Schmitt on printed circuit card 244. Here, the 1-character signal from the Schmitt trigger is fed to card 216 A-1, where it sets the ZL flip-flop (ZL := 1). The 1-character signal also resets the PFS flip-flop (PFS :=0) on card 261-1.

The signal from the ZL flip-flop is fed to three cards: first a monostable flip-flop with a pulse duration of 100 μsec. is started on card 202-25; then DISPLAY on card 200-10 is inhibited; and, finally, the YE indicator is illumined on the Display and the Auxiliary Display Panels via 200-37 and KB 6 and KB 12.

The monostable flip-flop that sends the 100 μsec. pulse serves two purposes: it sends the start signal to the reader and resets the BL register, so that the latter is ready to receive information from the reader. This reset is necessary, because information input from the reader to the BL register completely bypasses the transfer lines.

The start signal is fed to the reader via KB 8-S from 202-25. When the reader has been started, information from the 1 to 5 or 1 to 8 tracks is fed to the input of the amplifiers on card 200-2. The output of the amplifiers on 200-2 overrides the one collector on the BL flip-flop.

The outputs are also fed to card 251, where the entire card forms a half-adder. The parity check is performed here, and the half-adder indicates 1 := parity error in the presence of an even number of holes.

If BY 8 and BY 9 = 0.0 and all holes are present, it is desirable to suppress the parity error found. This is achieved by feeding the inverted signal from the AND-gate on card 200-2, which indicates all holes present, and the signal from 251, which indicates parity error, to the AND-gate that sets the PFS flip-flop.

if BY 8 and BY 9 := 1, input is desirable from the reader without parity check; for this reason, an additional AND-gate is inserted between the above-mentioned AND-gate and the PFS flip-flop, with the following inputs:

$\overline{\text{BY 8}}$:= 1 ,
Gs-BL := 1 , and
parity := 1 .

From this it may be seen that if BY 8 := 1 , $\overline{\text{BY 8}}$:= 0 and the parity signal := 1 will stop at this point.

When the reader has read a character, it sends a j klar pulse via KB 8-M to 200-2. The j klar signal is amplified and fed to 272-1, where it starts a monostable flip-flop with a pulse duration of 10 μsec. The pulse resets the ZL flip-flop on 216A-1.

The first character has now been placed in the BL register, and the reader is ready to receive new instructions regarding input.

Tape reader input is continued by means of the LY operation (OP 59). BY decoding on card 222-7 is utilized here, where the static signal $\overline{BY\ 8}$:= 1 and $\overline{BY\ 9}$:= 1 decodes the reader for input with parity check.

The signal is fed to card 216A-1, where along with Gm 1-ZL it forms inputs to an AND-gate that sets the ZL flip-flop.

As may be seen from the flow chart for the LY operation, Gmj is sent at Mode 2, MA 1. Gmj inputs the position, i.e. set or reset, of the ZL flip-flop to the jLY flip-flop, which is incorporated as a condition in the next microstep (jLY := 1 being the condition for peripheral busy with input).

Here it is assumed that ZL is reset at the beginning of the LY operation. The Gmj pulse will, accordingly, input 0 to the jLY flip-flop, so that jLY := 0. The computer then jumps to MA 18 and so forth, but just prior to the jump to Mode 4, Gm 1-ZL is sent. The ZL flip-flop is then set and remains set.

If, however, it is assumed that the computer immediately afterwards jumps into a new LY operation, it will send a new Gmj pulse and, as mentioned above, the position of ZL (0 or 1) will be input; but because of Gm 1-ZL, ZL := 1 and the jLY flip-flop is hereby set. The computer jumps back and forth between MA 1 and MA 16 in the LY operation now, continuously sending Gmj.

Since tape reader input requires ca. 0.5 - 2 milliseconds, the computer may continue to send Gmj for a considerable length of time. When the reader has read a character, it sends j klar to 200-2. This signal starts a monostable flip-flop. This pulse of ca. 10 μsec. resets the ZL flip-flop, and the computer can reset the jLY flip-flop at the next Gmj. The computer is then able to proceed in the microprogram.

When the computer jumps to Mode 4, Gm 1-ZL is sent, and this process continues until there are no more characters to be read from the tape.

If a parity error occurs when BY 8 := 1 and BY 9 := 1, the PFS flip-flop is set. This in turn sets the STOP flip-flop and the computer is stopped.

The PFS indicator is illumined at the same time on both the Display and Auxiliary Display Panels.

If BY 8 := 1 and BY 9 := 1, the parity check output is suppressed, as mentioned earlier, but the parity is transferred to line 0, because BY 8 := 1, Gs-BL := 1, and parity := 1 form inputs to an AND-gate that sets line 0 (line 0 := 1). The information about the parity error is then input to the AC register (cf. microprogram).

Blokdiagram for læsning fra strimmellæser	Block Diagram for Tape Reader Input
blok display	inhibit display
tænd YE lampen	light YE indicator
YE-lamper	YE indicators
1 huls-fremføring	one-hole drive
tegn	character
kør frem til næste tegn	forward to next character
strimmellæser	tape reader
nulstil.	reset
x-felt	matrix
klar	ready
linie	line
til paritetsfejllampe	to parity error indicator
1 af 8 pos	one of eight positions
nulstilling af BL	reset of BL

Typewriter Input

If it is assumed that BY 9 := 1, then typewriter input is selected. The decoding of the typewriter keyboard takes place on card 222-7, where BY 8 and BY 9 decode typewriter input.

The static signal is sent to 216A-1, where along with ¡ tastatur, ' ¡ keyboard,' it forms inputs to an AND-gate. The signal from the latter, along with the Gmj signal, forms inputs to a new AND-gate that is connected to an internal line on the card. Since this internal line contains a logical 1, the ¡LY flip-flop is set by the first Gmj sent from the microprogram.

The computer stops now at the ¡LY := 1 condition and jumps back and forth between MA 1 and MA 16. At the same time, the static tastatur valgt, 'keyboard selected', signal is fed to card 200-37, where along with the condition for the LY operation it forms inputs to an AND-gate, which illumines the YE indicator on both the Display and the Auxiliary Display Panels and the keyboard indicator on the typewriter.

In this state, the computer waits for typewriter input. When a key on the typewriter is punched, the following occurs: the signal from the key punched is fed to one of the three 273-cards, where diode conversion, i.e. conversion to binary representation, of the key. takes place. The table on pages 26 and 27 that shows the correspondance between numerical values and typographical symbols. The conversion is fed to 200-15, where the outputs are BT 4 - BT 9. Note that CR has a special output, BT 3.

As may be seen from the block diagram, there is no buffer register between the computer and the typewriter, since the time for punching a key far exceeds the time the computer requires for placing the information in the AC register from the lines.

A Schmitt trigger on card 200-15 is activated the moment the information is clear of the diode logic on the 273-cards. The output signal from the Schmitt trigger sets the ZT flip-flop and resets the ¡LY flip-flop on the next Gmj signal from the microprogram.

Correspondance between Numerical Values and Typograhical Symbols

NUMERICAL VALUE	BINARY REPRESENTATION	LOWER CASE	UPPER CASE
0	0000000		space
1	0000001	1	V
2	0000010	2	×
3	0000011	3	/
4	0000100	4	=
5	0000101	5	;
6	0000110	6	[
7	0000111	7	]
8	0001000	8	(
9	0001001	9	)
10	0001010		unused
11	0001011		stop code
12	0001100		end code
13	0001101	å	Å
14	0001110	-	|
15	0001111		unused
16	0010000	0	^
17	0010001	<	>
18	0010010	s	S
19	0010011	t	T
20	0010100	u	U
21	0010101	v	V
22	0010110	w	W
23	0010111	x	X
24	0011000	y	Y
25	0011001	z	Z
26	0011010		unused
27	0011011	,	10
28	0011100		unused
29	0011101		red ribbon
30	0011110		tabulator
31	0011111		punch off
32	0100000	-	+
33	0100001	j	J
34	0100010	k	K

NUMERICAL VALUE	BINARY REPRESENTATION	LOWER CASE	UPPER CASE
35	0100011	l	L
36	0100100	m	M
37	0100101	n	N
38	0100110	o	O
39	0100111	p	P
40	0101000	q	Q
41	0101001	r	R
42	0101010		unused
43	0101011	ϕ	Φ
44	0101100		punch on
45	0101101		unused
46	0101110		unused
47	0101111		unused
48	0110000	æ	Æ
49	0110001	a	A
50	0110010	b	B
51	0110011	c	C
52	0110100	d	D
53	0110101	e	E
54	0110110	f	F
55	0110111	g	G
56	0111000	h	H
57	0111001	i	I
58	0111010		lower case
59	0111011	.	:
60	0111100		upper case
61	0111101		unused
62	0111110		black ribbon
63	0111111		tape feed
64	1000000		carriage return

Blokdiagram for skrivemaskine input	Block Diagram for Typewriter Input
skrivemaskine	typewriter
tastatur	keyboard
linie	line
x-felt	matrix
tasta. valgt	keyboard selected
bet. fra LY-ordre	condition from LY operation
klar kontakt	ready contact
tastaturlampe	keyboard indicator
YE lampe i kontrolbord	YE indicator on Display Panel
YE lampe i HP-bord	YE indicator on Auxiliary Display Panel

The computer can then proceed in the microprogram and sends Gs-tastatur 'Gs-keyboard', to 212-2 -- seven positions in all -- as well as a Gm AC 00-9. After this, the information is in the AC register.

When the ZT flip-flop on 202-7 is set, the ZT signal is fed further to 202-19, from there to KB 9-D, and still further to 216-4; here, the signal waits for the next Gmj, when the jSY flip-flop is set.

Setting the jSY flip-flop makes it impossible for the computer tp proceed in an SY operation immediately following an LY operation, before the ZT flip-flop is reset and klar, 'ready', is received from the typewriter.

When the LY operation causes a jump, the condition disappears from 200-37 and the typewriter and YE indicators are then extinguished.

When the key has fallen back into place on the typewriter from the platen, a klar contact is activated, sending klar back to the computer via S4-24 to 272-2. Here, a monostable flip-flop is activated for 60 milliseconds. This signal resets the ZT flip-flop, after which the typewriter is ready to receive new input instructions.

Punch Output

The condition for punch output is determined by the SY operation and by setting the Manual Selection buttons on the Auxiliary Display Panel, so that the punch is selected in accordance with positions 3-6 of the BY register. The static signal is sent via KB 12 and 13 to 202-19, where it then waits.

If these conditions are present, the microprogram sends Gm 1-Zs via 200-37 and KB 9-A to 202-19, prior to the jump to Mode 4. The ZP flip-flop is hereby set, causing linie for jS, 'line for jS', to be set (linie for jS := 1), whereupon the jSY flip-flop is set on the next Gmj sent by the microprogram. Setting the jSY flip-flop causes the YE indicators on the Display and the Auxiliary Display Panels to be illumined via 200-37 and KB 6 and 12.

The ZP flip-flop also causes the reset signal to be fed to card 269, where a monostable flip-flop with a pulse duration of 6.5 milliseconds is started. On the leading edge of this signal, a new monostable flip-flop is started on the same card. The motor relay of the punch was also activated on the leading edge.

The monostable flip-flops are required to bring the punch up to maximum operating speed, before punching a character on the tape. When this speed has been attained, in virtue of the monostable delay, the start signal is sent via KB 11-a1 to card 269, where it forms, along with ZP := 1 and the amplified signal := ZP* as well as the last monostable signal from card 269, inputs to an AND-gate, the outputs of which are $\overline{\text{START}}$. This signal overrides the one collector on the FB flip-flop, so that FB := 1.

The FB signal now advances the tape, so that it is clear of the row of holes just punched, and sets the GP flip-flop.

A short time later, the punch sends the klar, 'ready', signal, which is fed via KB 11-a3 and 200-13 to 202-4, where it overrides the one collector on the GP flip-flop, so that GP := 0. The BL flip-flop is hereby reset by the GpF signal, and the gate pulse, BLs, is sent to 202-4, where it forms, along with GP, GP' to 214-6, thus giving the signal to the punch in accordance with the contents of the BS register.

After punching, the punch sends a STOP signal via KB 11-a2 and 200-13 to card 202-4, where the FB flip-flop is overridden on the collector, so that FB := 0. The tape is hereby locked by the signal via 270 and KB 11-a8.

The blank strimmel or 'blank tape' signal is sent by means of manual operation of the start switch on the punch. The BL flip-flop is hereby set, inhibiting the gate for GP', and the punch advances the tape without the contents of the BS register being punched. (Tape feed is, of course, punched).

The information from the BS register (placed in the register by means of the microprogram of the SY operation) is fed via 200-10 and KB 9 to 200-11, where the signals are inverted again and then fed to 214-6 and 251-1.

Card 251-1 consists of a series of half-adders that determine whether the contents of the BS register are even or odd with respect to binary 1. If the number of 1's is even, the output assumes a negative value, which is in accordance with having a hole punched in track 5.

Blokdiagram over skrivning med perforator	Block Diagram for Punch Output
perforator	paper tape punch
klar	ready
blank strimmel	blank tape
motor relæ	motor relay
HP-bord	Auxiliary Display Panel
x-felt	matrix
YE-lampe	YE indicator

Typewriter Output

The condition for typewriter output is determined by the SY operation and by setting the Manual Selection buttons on the Auxiliary Display Panel, in such a way that the typewriter is selected as output device in accordance with the contents of the BY register. The signal is sent via KB 12 and 13 to 202-19, where it waits.

If these conditions are present, the microprogram sends Gm 1-Zs, before the jump to Mode 4, via 200-37 and KB 9-A to 202-19, where the ZS flip-flop is set, causing linie for jS ('line for jS') to be set, whereby the jSY flip-flop is set on the next Gmj from the microprogram. Setting the jSY flip-flop causes the YE indicators to be illumined on both the Display and the Auxiliary Display Panels via 200-37 and KB 6 and 12.

In accordance with the SY operation, the information to be written out is sent to the seven least significant positions of the BS register (pos. 3-9), after which a purely static decoding of these seven positions takes place, as the static signals are fed to the decoding cards (203-3 and 203-4). These cards divide the BS register into two halves, with positions 4-6 in the one half and positions 7-9 in the other. Card 203-3 (positions 4-6) forms the control card for positions 7-9, since the ST* condition for write-out is placed on card 203-3.

The St* condition is a function of the position (set or reset) of the ZS flip-flop, since ZS := 1 (due to Gm 1-Zs) is fed to a monostable flip-flop on card 272-2, which has a pulse duration of ca. 3 milliseconds. The static signal of the Zs flip-flop is hereby delayed 3 milliseconds. On the trailing edge of this pulse, a new monostable flip-flop is activated, with a pulse duration of 42 milliseconds. This pulse is called St*. The inverted St* signal keeps linie for jS set (linie for jS := 1) as long as the decoding pulse, St* := 42 mS, is present. With the help of St*, the decoding of the BS register is fed to the 271-cards, which form the drive section for the typewriter.

When the typewriter has written the character on the paper, or possibly on the platen, it sends a klar ('ready') signal via S4-24 to 272-2, where the signal starts a monostable flip-flop with a pulse duration of 60 milliseconds. The ZS flip-flop is reset on the trailing edge of this signal. The 60 milliseconds are necessary, since the maximum operating speed of the typewriter is ca. 12 char./sec.

If it is assumed that the contents of the BS register do not correspond to any character on the typewriter in binary representation (cf. table on pages 7-26 and 27), then the output of the drive section is fed to klar af ubrugte tegn, 'ready from unutilized characters', which resets the ZS flip-flop, so that the computer can proceed in the microprogram after waiting ca. 45 milliseconds.

The typewriter contains speciel keys, such as Upper Case and Lower Case, and the computer includes a special Upper/lower Case flip-flop, by means of which the typewriter is locked in the case desired, until other declaration is made. If two Upper or Lower Cases follow immediately after each other, the computer does not wait very long, since the KLAR flip-flop from Upper and Lower Case sends klar af ubrugte tegn for reset of the ZS flip-flop.

Other special keys are Black and Red Ribbon Shift, with a special input for reset of the ZS flip-flop, since they activate the monostable flip-flop with a pulse duration of 60 milliseconds that resets the ZS flip-flop on the trailing edge of the pulse.

If it is assumed that the next operation is an LY operation, the computer cannot execute it, before the jLY flip-flop (which was set on Gmj from the SY operation) has been reset, which must be done first by pressing a key on the keyboard. This cannot, however, be done, until the typewriter is finished writing what was desired from the SY operation.

Blokdiagram skrivning på skrivemaskine	Block Diagram for Typewriter Output
afkodning	decoding
skrivemaskine tastatur	typewriter keyboard
klar signal	ready signal
sort farvebånd	black ribbon
klar til	ready to
linie	line
ubr. tegn	unused character
sort ind	black in
fra afkodning	from decoding
rød ind	red in
HP-bord	Auxiliary Display Panel
YE-lampe	YE indicator

Line Printer Output

Line printer output proceeds along the same lines as punch output. Information from the BS register is fed statically to the line printer via 200-10 and KB 9 as well as 200-11 and KB 14.

The ZA signal to the line printer originates, when the Manual Selection buttons on the Auxiliary Display Panel are set, in accordance with the contents of the BY register, in such a way that the line printer is selected.

The static signal is fed via KB 12 and KB 13 to 200-25, where it forms along with Gm 1-Zs inputs to an AND-gate, the output of which is ZA. This signal is fed via KB 14 to the line printer.

The line printer sends Z0 via KB 14 to 202-19. The inverted signal controls the line called linie for jS, ' line for jS ', which sets the jSY flip-flop on the next Gmj from the SY operation, whereupon the YE indicators on both the Display and the Auxiliary Display Panels are illumined.

These indicators are extinguished again, when the jSY flip-flop is reset, either by RESET or on the next Gmj, which inputs 0 from linie for jS.

Blokdiagram for skrivning på Anelex

Anelex

YE-lampe i KB-bord

YE-lampe i HP-bord

HP-bord

Block Diagram for Line Printer Output

line printer

YE indicator on Display Panel

YE indicator on Auxiliary Display Panel

Auxiliary Display Panel

8. Indicator circuits

The indicator operation is defined by means of the bits OR 33 and OR 34 in the following manner:

OR 33	OR 34	Name		Description
0	0	B_0	I	Storing in indicator
0	1	B_1	M	Marking of cell
1	0	B_2	N	Conditioning of instruction
1	1	B_3	L	- - -

It will be seen that each operation has two names. The names B_0-B_3 are only used in the technical papers. The decoding of the indicator-operation is done by the 'I -afk' on the card 222-2.

The indicator address is defined by means of the bits OR35 - OR39. The first 3 bits are decoded by means of the 'IA-afk' on the cards 222-1 in the following manner:

OR 35	OR 36	OR 37	Name	Description
0	0	0	N	Zerokombination
0	0	1	K	Push buttons on control panel
0	1	0	W or Z	Zero status of the R-gister
0	1	1	O	Overflow
1	0	0	T	Sign
1	0	1	P	Marking bits
1	1	0	Q	- -
1	1	1	R	- -

The two last bits of the address are used in the following manner:

OR 38	OR 39	Name
0	0	Zerokombination
1	0	A
0	1	B
1	1	C

The Indicator-register IN consists of 12 flip-flops with the names:
OA, OB, TA, TB, PA, PB, QA, QB, RA, RB, KA and KB.
The 10 first are connected to the busline-system and are placed upon the circuit cards 216-1. KA and KB can only be set manually from the control panel and are placed upon the card 200-5.

The specific functions of the indicator-logic are described in full detail in 'A Manual of GIER Programming', vol 1, page 90-95.

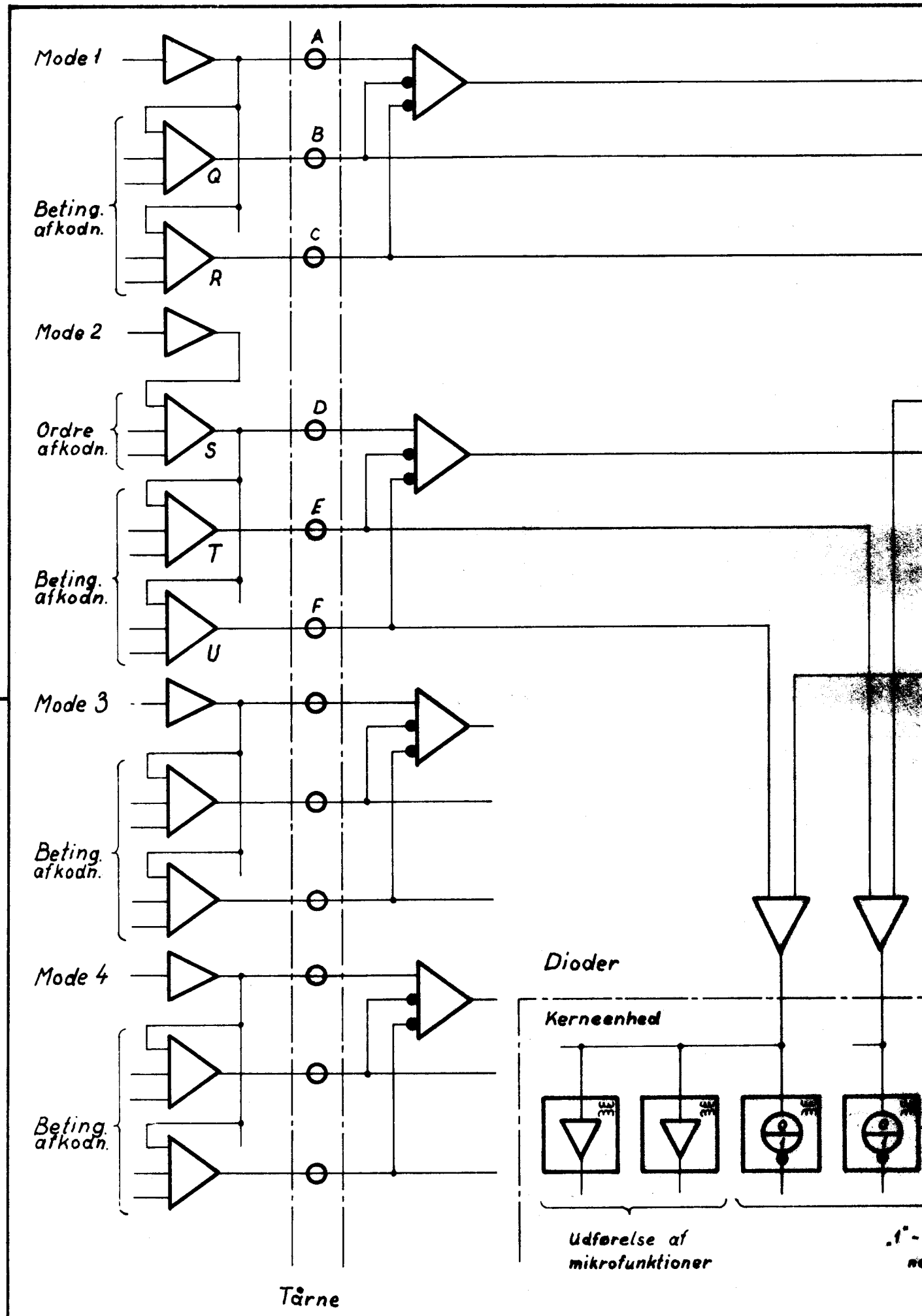
Conditioning of an instruction by means of indicatoroperations N or L is performed by a group of logic circuits which gives the outputsignal B.
If B = 1 the condition is fulfilled and the instruction will be executed.
This logic is placed upon the cards 233 and 200-9. The Boolean expression for B can be written in this way:

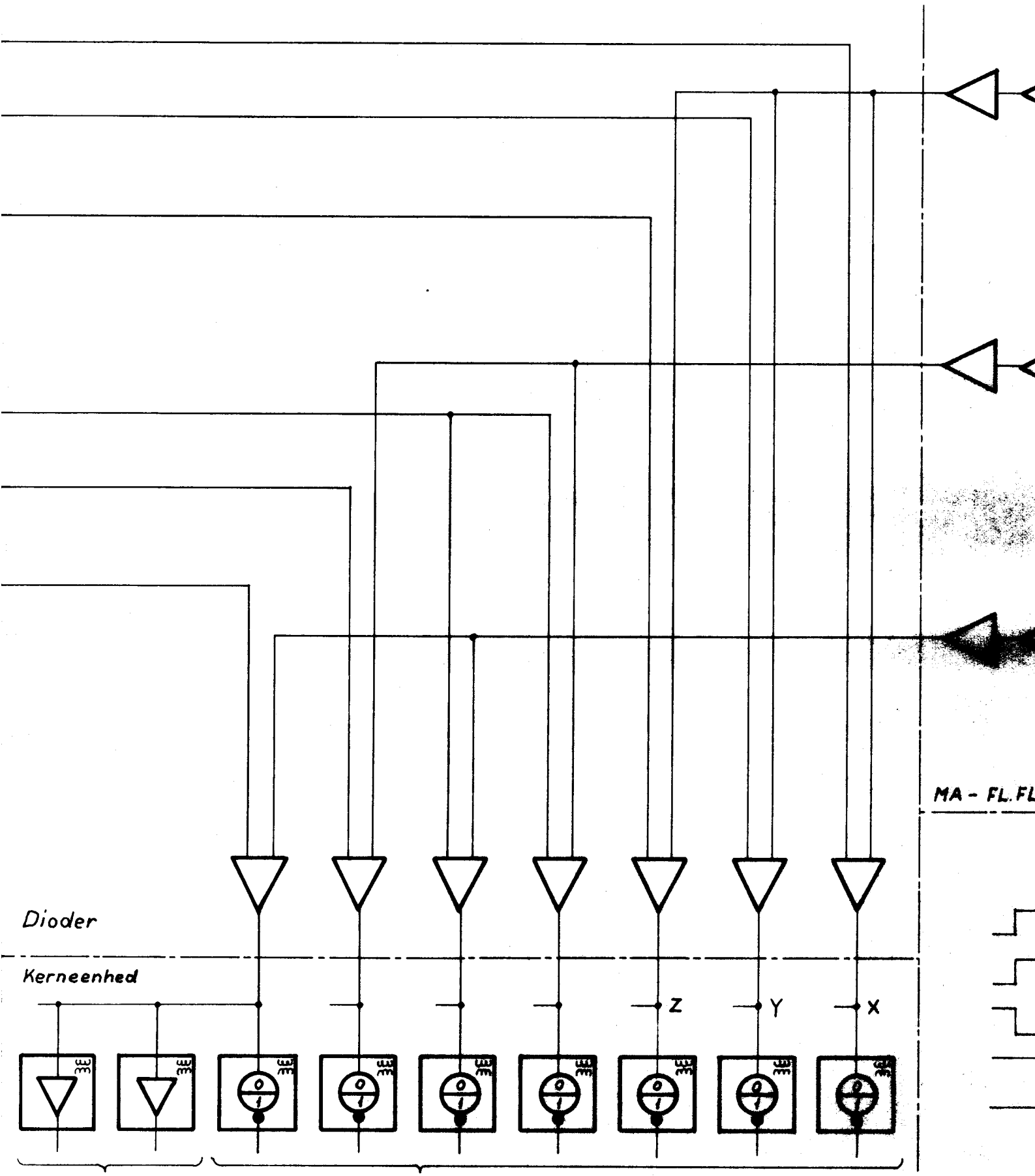
$$
\begin{aligned}
B = \quad & (\overline{N} + \overline{B}_3 \cdot \overline{H}_{40} + B_3 \cdot H_{40} + \overline{OR}_{38})(\overline{N} + \overline{B}_3 \cdot \overline{H}_{41} + B_3 \cdot H_{41} + \overline{OR}_{39}) \cdot \\
& (\overline{K} + \overline{B}_3 \cdot \overline{K}_A + B_3 \cdot K_A + \overline{OR}_{38})(\overline{K} + \overline{B}_3 \cdot \overline{K}_B + B_3 \cdot K_B + \overline{OR}_{39}) \cdot \\
& (\overline{W} + \overline{B}_3 \cdot \overline{O}_A + B_3 \cdot O_A + \overline{OR}_{38})(\overline{W} + \overline{B}_3 \cdot \overline{O}_B + B_3 \cdot O_B + \overline{OR}_{39}) \cdot \\
& (\overline{W} + \overline{B}_3 \cdot \overline{w} + B_3 \cdot w + OR_{38} + OR_{39}) \cdot \\
& (\overline{O} + \overline{B}_3 \cdot \overline{O}_A + B_3 \cdot O_A + \overline{OR}_{38})(\overline{O} + \overline{B}_3 \cdot \overline{O}_B + B_3 \cdot O_B + \overline{OR}_{39}) \cdot \\
& (\overline{O} + \overline{B}_3 \cdot \text{overflow in AC} + B_3 \cdot \text{overflow in AC} + OR_{38} + OR_{39}) \cdot \\
& (\overline{T} + \overline{B}_3 \cdot \overline{T}_A + B_3 \cdot T_A + \overline{OR}_{38})(\overline{T} + \overline{B}_3 \cdot \overline{T}_B + B_3 \cdot T_B + \overline{OR}_{39}) \cdot \\
& (\overline{T} + \overline{B}_3 \cdot \overline{AC}_{00} + B_3 \cdot AC_{00} \cdot OR_{38} + OR_{39}) \cdot \\
& (\overline{P} + \overline{B}_3 \cdot \overline{P}_A + B_3 \cdot P_A + \overline{OR}_{38})(\overline{P} + \overline{B}_3 \cdot \overline{P}_B + B_3 \cdot P_B + \overline{OR}_{39}) \cdot \\
& (\overline{Q} + \overline{B}_3 \cdot \overline{Q}_A + B_3 \cdot Q_A + \overline{OR}_{38})(\overline{Q} + \overline{B}_3 \cdot \overline{Q}_B + B_3 \cdot Q_B + \overline{OR}_{39}) \cdot \\
& (\overline{R} + \overline{B}_3 \cdot \overline{R}_A + B_3 \cdot R_A + \overline{OR}_{38})(\overline{R} + \overline{B}_3 \cdot \overline{R}_B + B_3 \cdot R_B + \overline{OR}_{39}) \cdot
\end{aligned}
$$

In the case that indicatoroperation L is used then we have B 3 = 1. For operation N we have B 3 = 0 in the expression. By selecting an address f.ex. P, we have P = 1 and $\overline{P} = 0$. This means that only the paranthes containing $\overline{P}$ is interesting, because all other addresses N, K, W, O, T, Q and R = 0 that is $\overline{N}$, $\overline{K}$, $\overline{W}$, ... $\overline{R}$ = 1 so that all the rest of the parantheses are equal to 1. The expression simplifies in this case

For B 3 = 1 to $B = (PA + \overrightarrow{OR}_{38}) (PB + \overline{OR}_{39})$ and

for B 2 = 1 to $B = (\overline{PA} + \overline{OR}_{38}) (\overline{PB} + \overline{OR}_{39})$.


Mode 1
A
B
Q
Beting. afkodn.
C
R
Mode 2
Ordre afkodn.
D
S
E
T
Beting. afkodn.
F
U
Mode 3
Beting. afkodn.
Mode 4
Beting. afkodn.
Dioder
Kerneenhed
Udførelse af mikrofunktioner
Tårne



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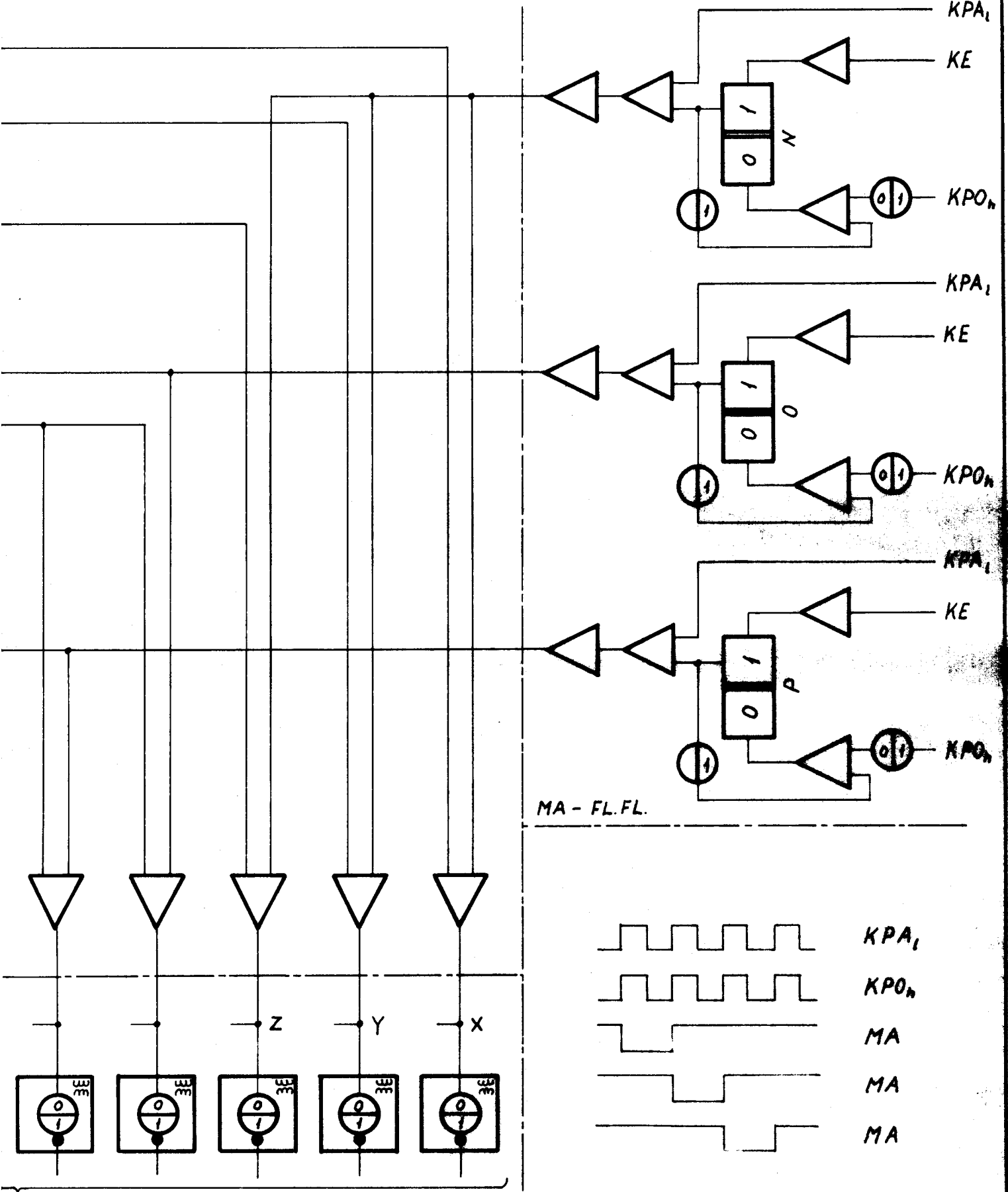

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A/S REGNE CENTRALEN	drawn by	K.F.	GIER Styreenhed Princip - diagram	pages	page
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The Control Unit Circuit

The GIER computer contains 64 instructions or macro-operations, which are executed by means of built-in micro-operations. The execution of a macro-operation takes place in four stages or modes: each macro-operation executed goes through Mode 1, Mode 2, and Mode 4; Mode 3, an extension of Mode 2, is used mainly in operations with floating point arithmetic.

Each macro-operation has its own microprogram, comprising Mode 1 (the same for all operations), Mode 2 (special for each individual operation), and Modes 3 and 4 (the same for all operations). Address modification is carried out in Mode 1, the actual microprogram, corresponding to the given macro-operation, in Modes 2 and 3, and indicator operations in Mode 4. Mode 5 constitutes a special microprogram, used in connection with the HELP system, and is described separately.

A microprogram is executed in time steps with a clock frequency of ca. 450 KHz. At each step a micro-operation, consisting of combinations of built-in microfunctions, is executed. For a given core in a built-in fixed wired store (also referred to as KE) there is a given microfunction that is executed, when that core is activated. Roughly 185 different microfunctions are included in the computer. Micro-address flip-flops, numbered 1-24, correspond to these steps. At a given step, one of the microfunctions will always be selection of the next step (MA flip-flop), which is not necessarily the nearest lower or higher number. A core is activated by voltage coincidence between an MA flip-flop and a decoding for selection of the microprogram.

Conditions may be introduced for any micro-operation: if a certain condition is present, a micro-operation corresponding to it will be executed; if not present, a different one will be executed. With the exception of substitution instructions, the microprogram for a macro-operation is ended by selection of MA flip-flop 1 and Mode 1, and this, accordingly, is the state at the outset, when a new macro-operation is to be carried out.

The control unit in the computer comprises a built-in fixed wired store (KE), 24 MA flip-flops, and a total of about 700 diodes (one for each micro-operation) for decoding of selection of the microprogram and the micro-operation. All decodings end on solder terminals, of which there are some 300.

Clock pulses, the fixed wire store, MA flip-flops, diodes, terminals, and gates for decoding of registers and mode flip-flops are shown on the Principle Diagram. Clock pulses KPA_l and KPO_h, which are identical, constitute the normal clock pulse in the computer. An MA flip-flop is set (selected) as a function of the KE signal, which is the differentiated and inverted output from an activated core in the fixed wired store. An MA flip-flop is reset by the differentiated clock pulse KPO_h. Mode flip-flops are set as a function of an activated core, and are reset by the next mode flip-flop.

At a given step during the execution of Mode 1 of a macro-operation, MA flip-flop N is selected. If decoding indicates that condition Q is present, terminal B is selected; if condition R is present, terminal C is selected; if neither of these conditions is present,

terminal A is selected. Decoding and diode logic are so arranged that only one terminal (A, B, or C) is selected, never two or more at one time; the logical inversion in the diode logic, moreover, gives condition terminals, e.g. B and C, priority over operation terminals, e.g. A. When clock pulse KPA_1 is logical "1" and MA flip-flop N and either terminal A, B, or C are selected, then a number of cores (microfunctions), corresponding to this given micro-operation, will be activated.

It may be seen that with the same MA flip-flop selected, but in accordance with which terminal a condition is present for, different cores will be activated, corresponding to the execution of different micro-operations. Logically, this may be expressed as follows:

$$\text{micro-operation } X = (KPA_1 \cdot \text{MA flip-flop N}) \cdot (A \cdot \overline{B} \cdot \overline{C}),$$

from which it may be seen that in order to have the micro-operation that corresponds to terminal A executed, terminals B and C must be logical "0" (not selected). The decoding logic makes it impossible for conditions Q and R to be present at the same time.

With respect to time, the control unit is governed by the clock pulses. The microfunctions are executed on the leading edge of KPA_1. The next MA flip-flop is set on the trailing edge of KPA_1, as a consequence of the differentiation and inversion of the output on the cores that select the next MA flip-flop; at the same time, the previous flip-flop is reset by KPO_h. Two MA flip-flops are therefore not selected simultaneously. As shown on the drawing, an MA flip-flop is set in a clock period.

At the end of Mode 1 (address modification), the Mode 2 flip-flop and MA flip-flop 1 are set. Setting the Mode 2 flip-flop provides the condition for the decoding of the macro-operation (S), and terminal D is then selected, if conditions T and U are not present.

As shown on the drawing, one terminal can in principle be connected to more than one MA flip-flop, and one MA flip-flop to more than one terminal.

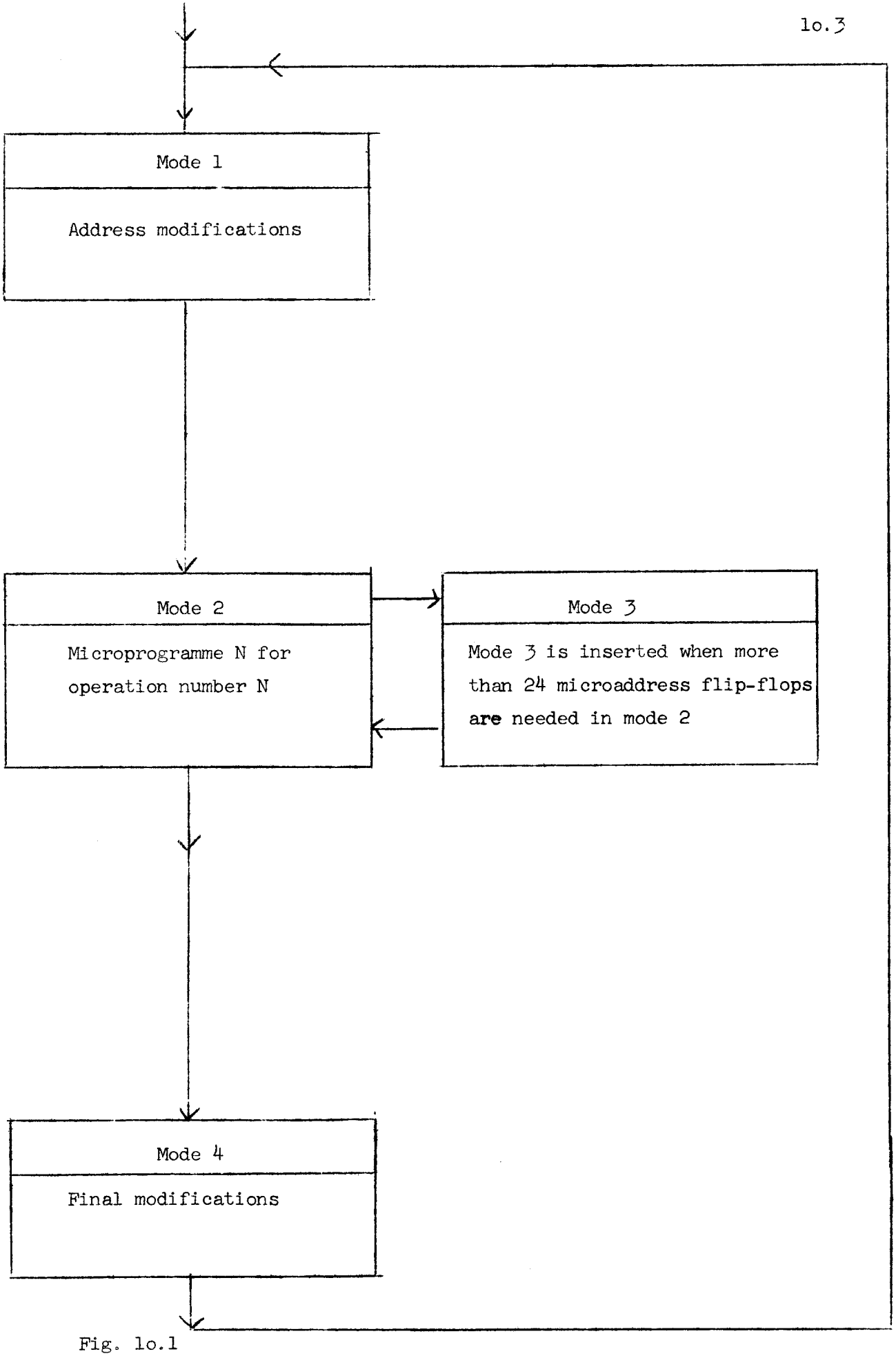


Fig. lo.1

General principle of the sequence of microprogrammes at the execution of one operation.

MODE 5

The HP button is used to interrupt the program being run and to activate the program stored on track 0. This interruption is made in such a way that it is possible to re-establish the situation before interruption by means of programming. The exact function of the HP button is described in Christian Gram: A Manual of GIER Programming, Volume 2, Section 13.2.1.

By pressing the HP button, a Schmitt trigger is activated that gives the signal 1-HP. The HP flip-flop is set, if the condition for the following AND-gate is present, namely that:

1. Mode 5 is not set, and
2. BY0•VAC is not "1".

The first condition prevents HP from being set again, while Mode 5 is being executed. The second condition applies in the following: if BY0 is set and the Mode 5 flip-flop is to be activated without using the RESET button, this is only possible by resetting BY0 from the Display Panel; if the HP flip-flop is set and the BY0•VAC circuit is not intact, the Mode 5 flip-flop is activated the moment BY0 is reset, and the Mode 5 microprogram is executed with line 0 overridden to 0.

With BY0•VAC intact, the HP flip-flop is reset by VAC, and 1-HP is inhibited, until BY0 is reset.

Now it is only possible to activate the Mode 5 flip-flop by pressing the HP button again.

If the computer is stopped in Mode 1, MA 1, and if BY0 is reset, setting HP causes Mode 5 to be set.

If the computer is in operation, the state, where Mode 1 = "1" and MA 1 = "1", must be present; this only happens on the completion of one operation and before the start of the next.

Since the VAC condition is not present, only the differentation circuit on 209-2 is open to Mode 1; otherwise Mode 5 might be activated at a point, when the first microstep in the next operation was executed before the setting of the Mode 5 flip-flop had been able to reset the Mode 1 flip-flop.

When Mode 5 is set, Mode 1 and HP are reset and 1-HP is inhibited. Operation terminals 231 and 232 for the Mode 5 microprogram have now been selected from output C6-7-5. By means of the amplifier on C6-3, access is given to condition terminals 115 and 128.

At the same time, the Mode 5 signal is sent via an amplifier on C6-4 to the start-stop circuits and the computer is started.

During the Mode 5 microprogram, setting the b flip-flop causes output of core store cells 0-39 to drum track 38, while resetting the b flip-flop causes input of drum track 0 to core store cells 0-39; in addition, 0T is set equal to 1.

Finally, the Mode 1 and MA 1 flip-flops are set. A signal that resets Mode 5 is hereby sent via the amplifier on 209-5.

If NORMAL STOP (STOP) on the Display Panel is manually activated now, the computer is stopped here and track 0 is stored in core store cells 0-39.

If STOP is not activated, the computer proceeds and executes the operation in cell 1.

In order to execute the Mode 5 microprogram step by step, the following must be done:

1. reset,
2. set the test switch to Test 3 or 4,
3. press the HP button,
4. press MIKROTEMPI STOP (RESET), and
5. set the test switch to Normal Run.

The computer is now in Mode 5, MA 1, and the microprogram can be executed step by step.

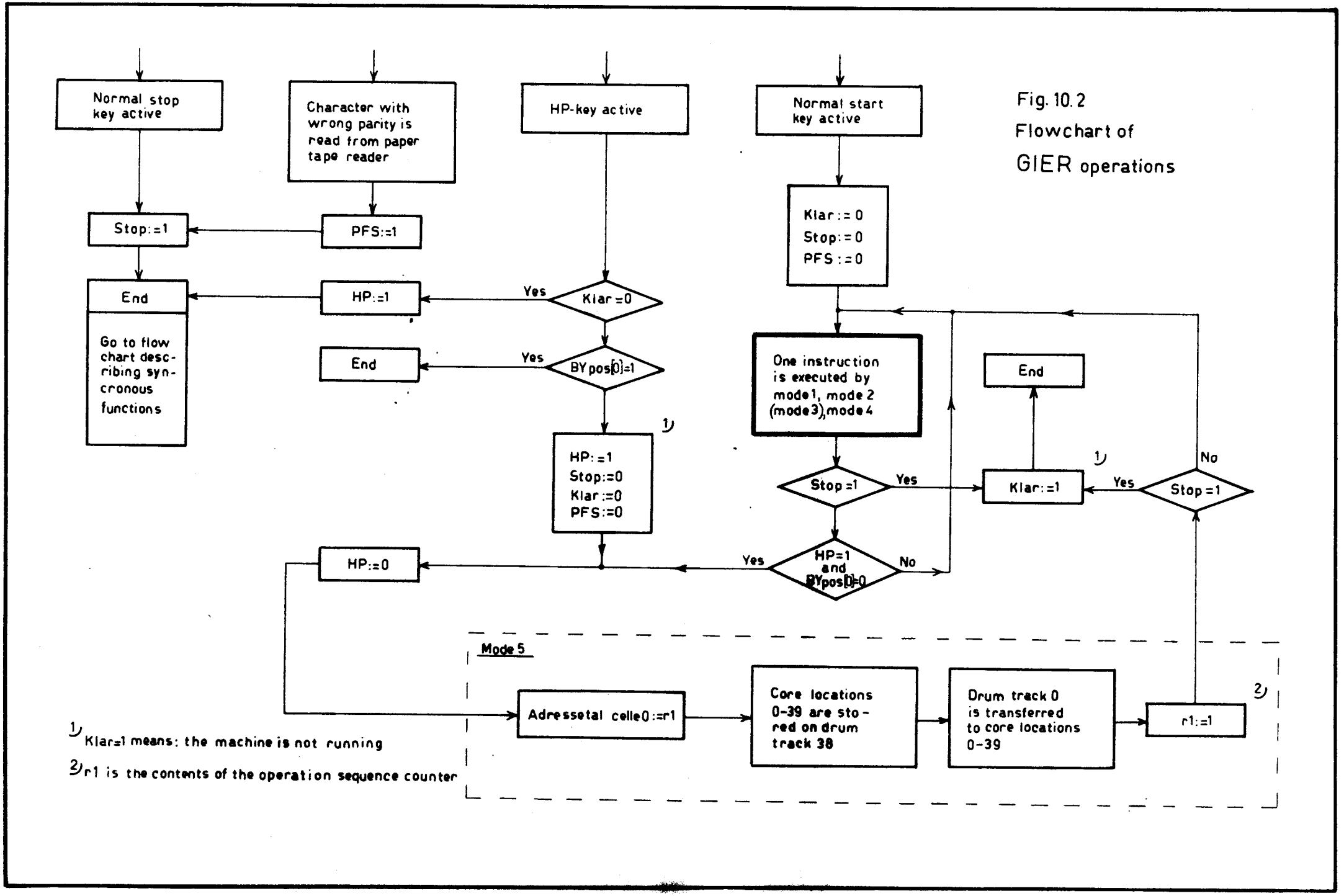
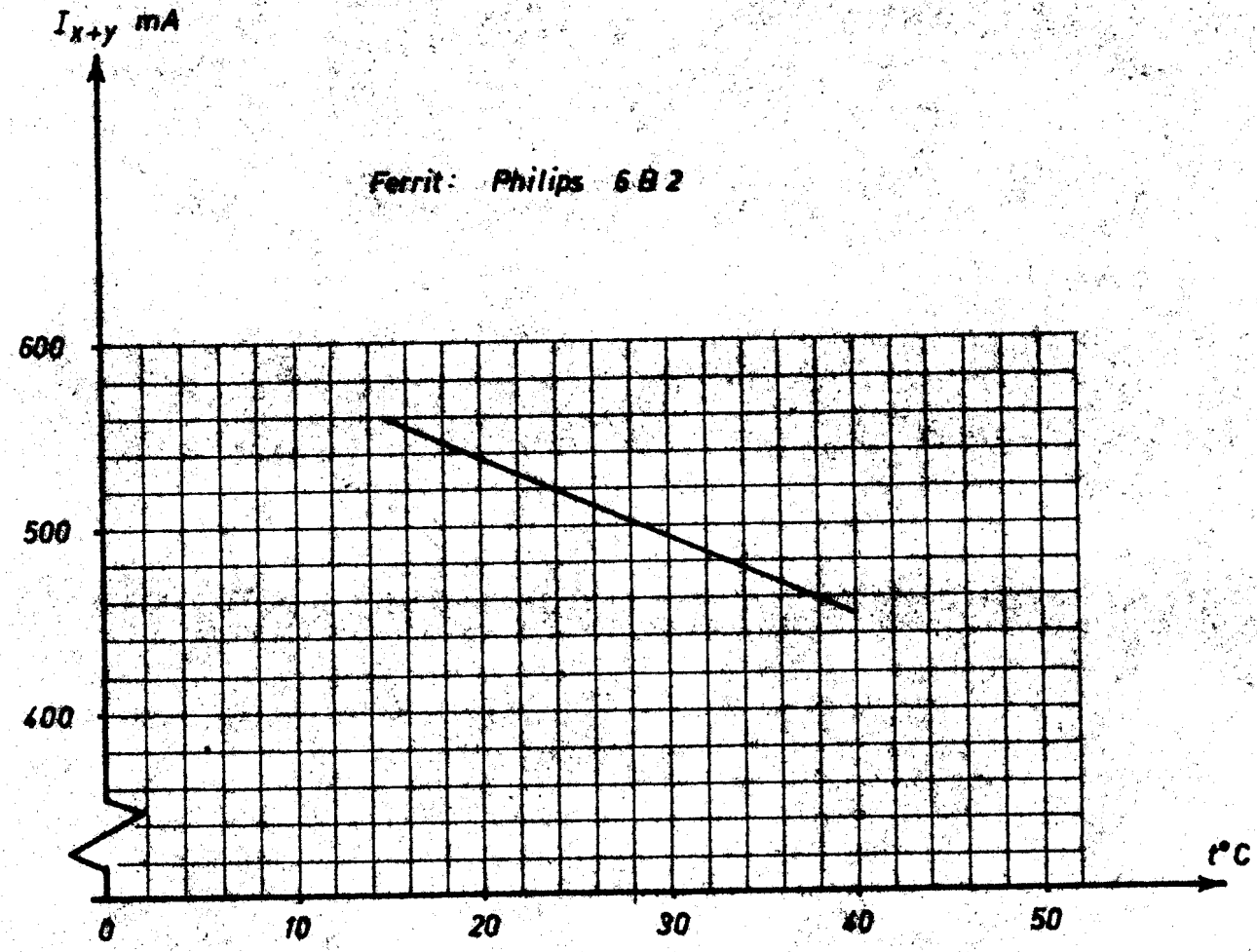


Fig. 10.2
Flowchart of
GIER operations



Drivstrøm til GIER ferritlager som funktion af temp.

REGNECENTRALEN Dansk Institut for Matematikmaskiner	Tegnet	1-11-63 PT.N.		FERRITLAGER	GIER
	Kontrol				
	Godk.				