Internal use only

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Title:

CPU752 Technical Manual
RC750 CPU-Board.

RCSL Nr. 46-F 0089

A/S REGNECENTRALEN
af 1979

Keywords:

CPU752, Technical Manual, 80186, 82730.

Abstract:

This manual contains the technical description of CPU752. CPU752 is used in RC750.

(82 printed pages)

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RCSL Nr. 46-F 0087

The block diagram, shown on page 4, intends to give a generel overview of the CPU.

The individual functional blocks are marked with references to relevant pagenumbers in the logic diagram.

The lefthand pages are thought as comments and explanation of the logic diagrams presented on the righthand pages.

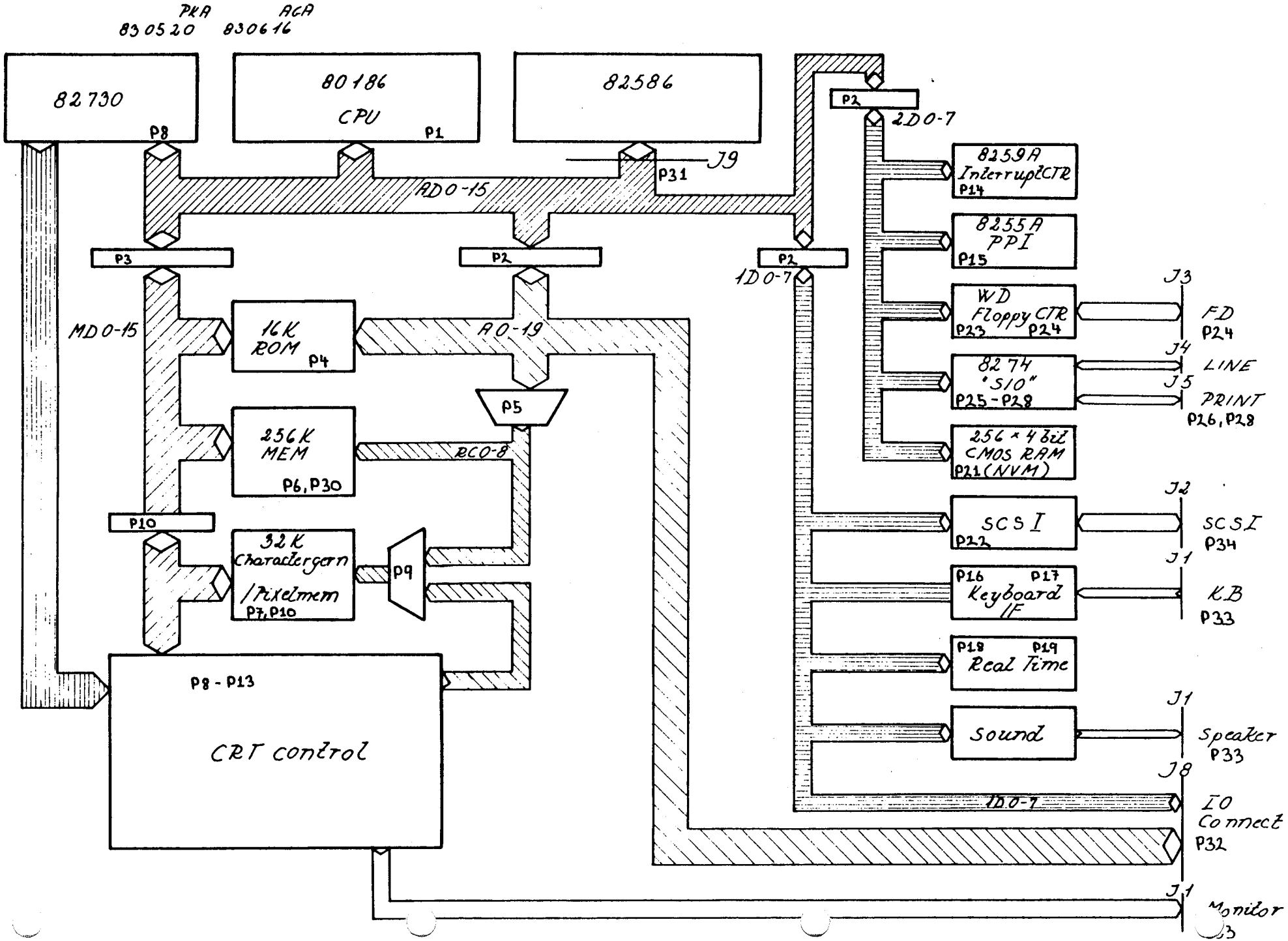
The following FCO's are included in the logic diagram:

19-017	19-018	19-020
19-021	19-028	19-029
19-030	19-031	19-032

Whenever a logic diagram page is changed by an FCO, this will be noted on the relevant page.

Please be sure to update your diagram according to later FCO's.

Block Diagram



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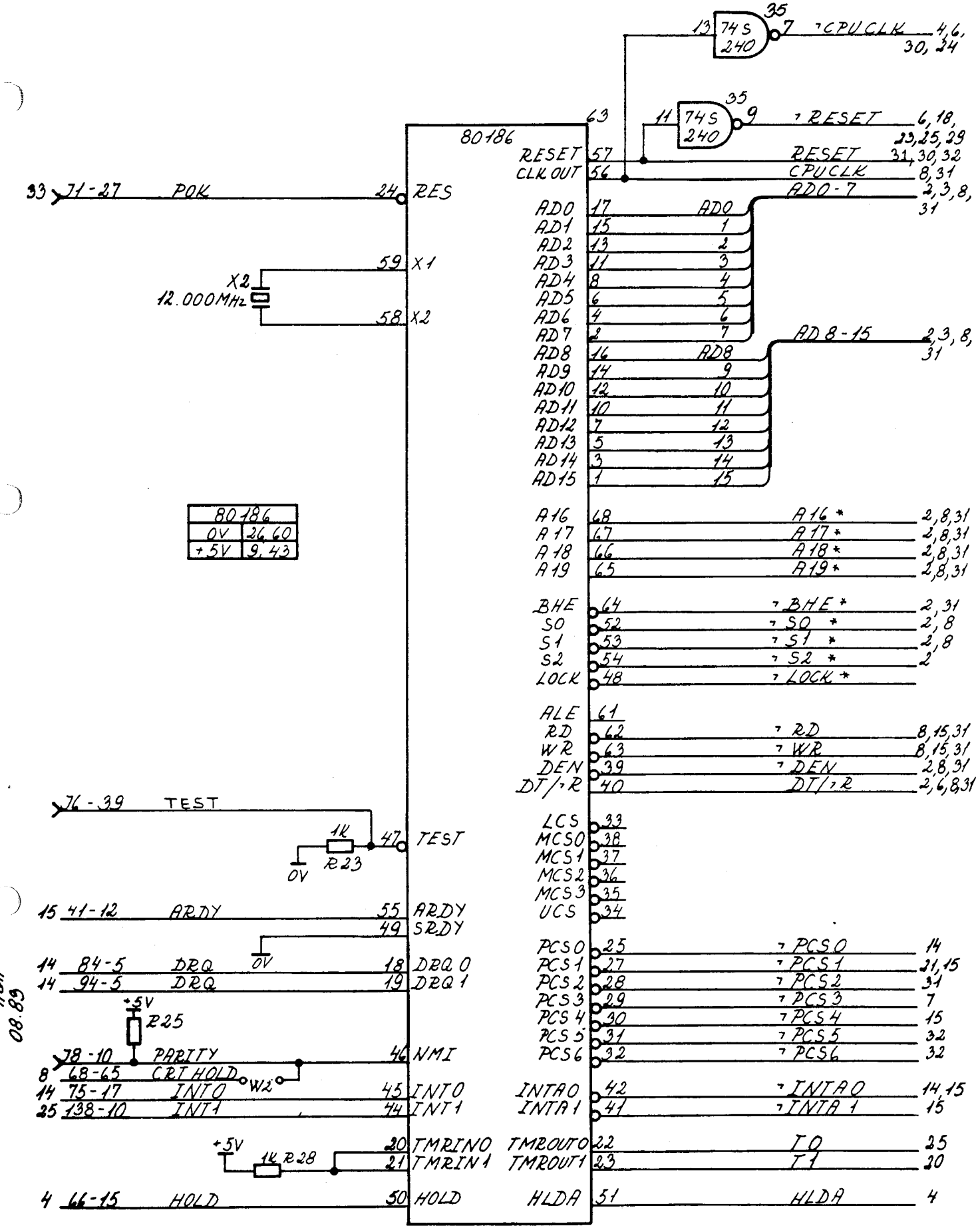
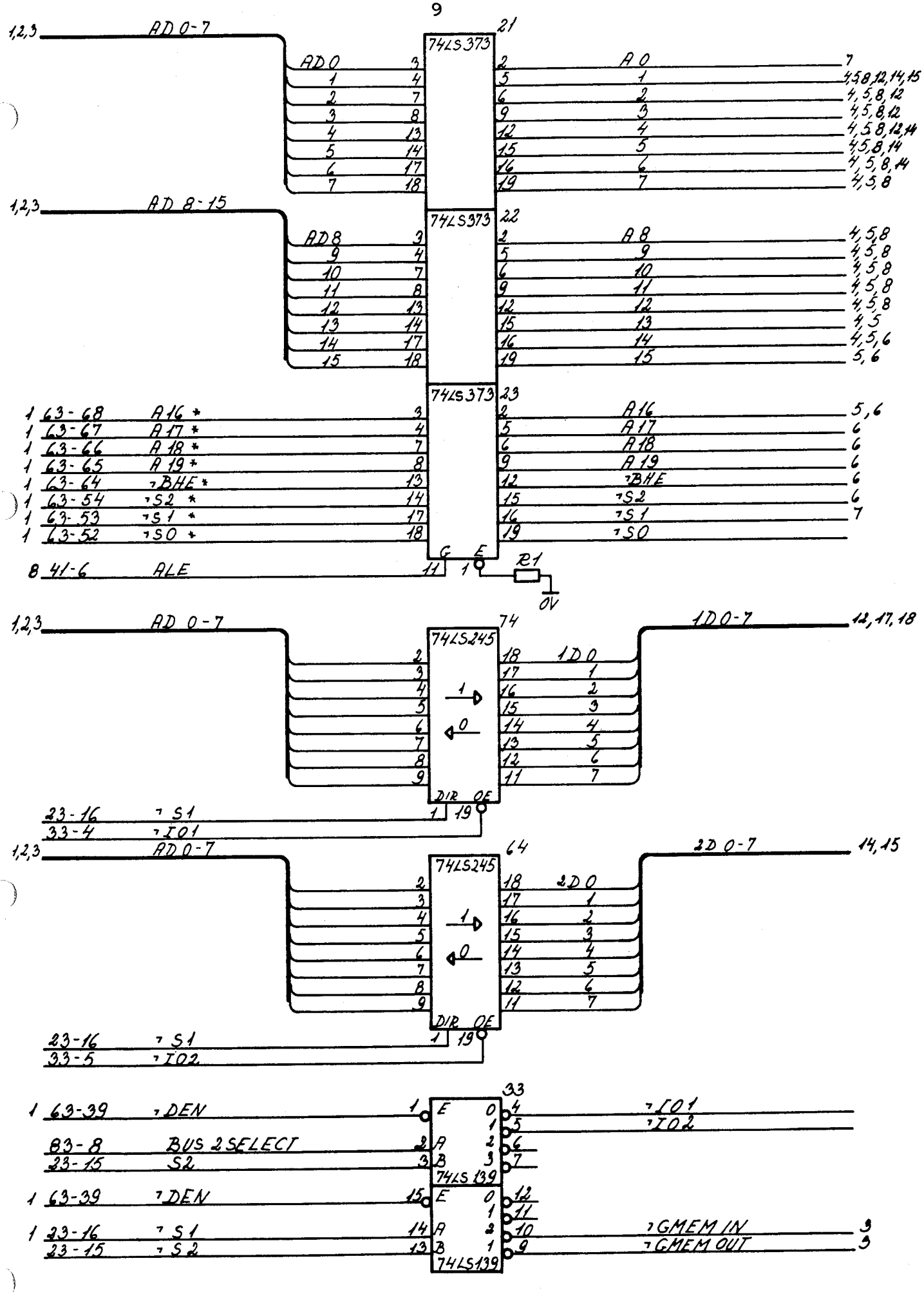
Signal	Description
AD 0-15	Multiplexed Address/Databus common for the coprocessors. AD0 is least and AD15 most significant.
ALE	Address Latch Enable Signifies a valid address on the AD bus.
CPU CLK	Timing signal for parts running synchronously with the CPU.
RESET	True when the CPU is being reset.
A 16-19	The four most significant addressbits.
-BHE	Byte High Enable low when data is transferred on D 8-15.
-S0-2	Bus status signals indicating the kind of bus cycle being performed:

-S2	-S1	-S0	Bus cycle
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

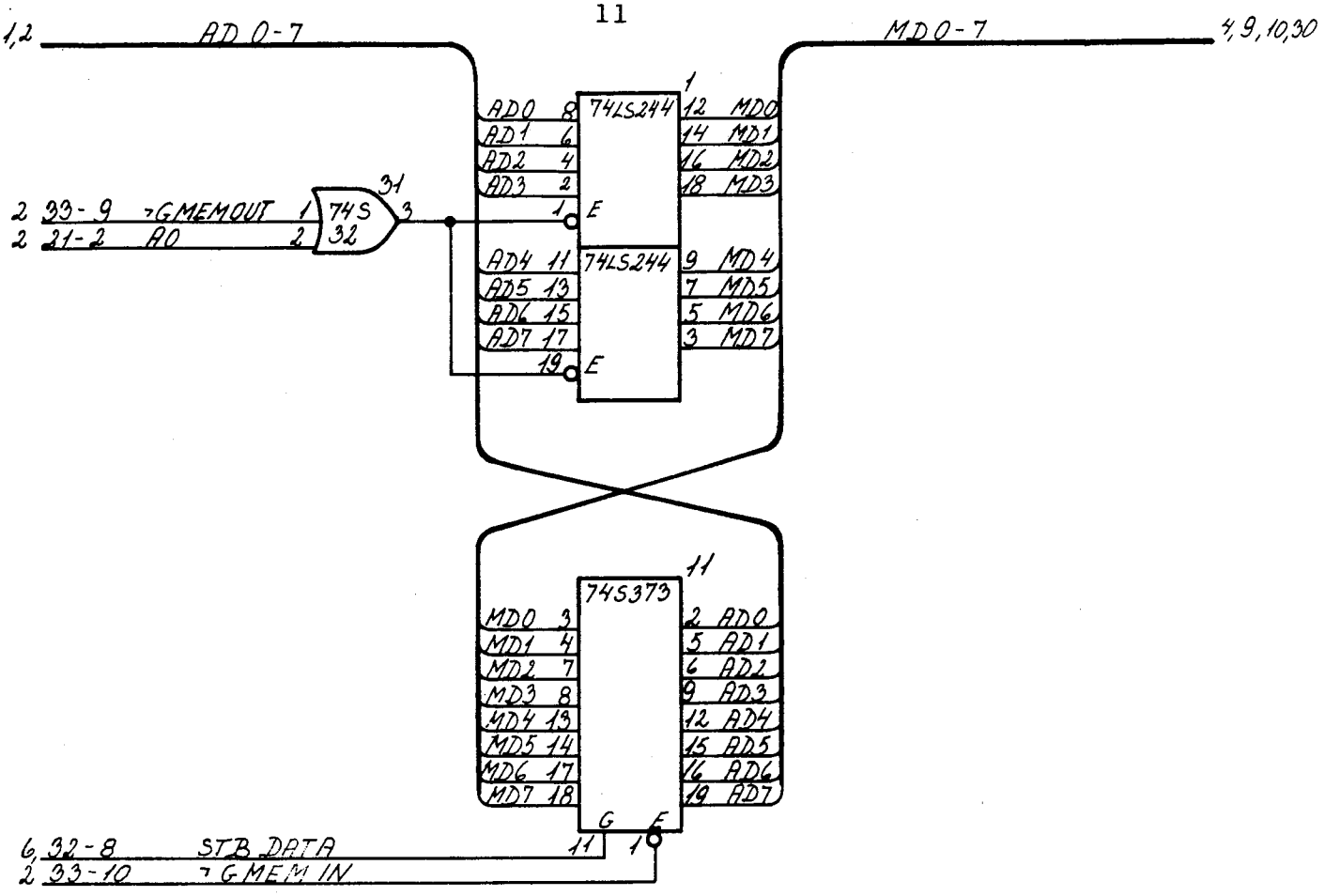
-RD, -WR	Read and Writestrobes.
-DEN, DT/-R	Data enable, Direction Transmit/not Receive. Used to controle Databuffers.
-PCS 0-6	Peripheral Chip Select outputs.
-INTA 0-1	Interrupt acknowledge.
T 0-1	Timer outputs.
HLDA	Hold acknowledge.

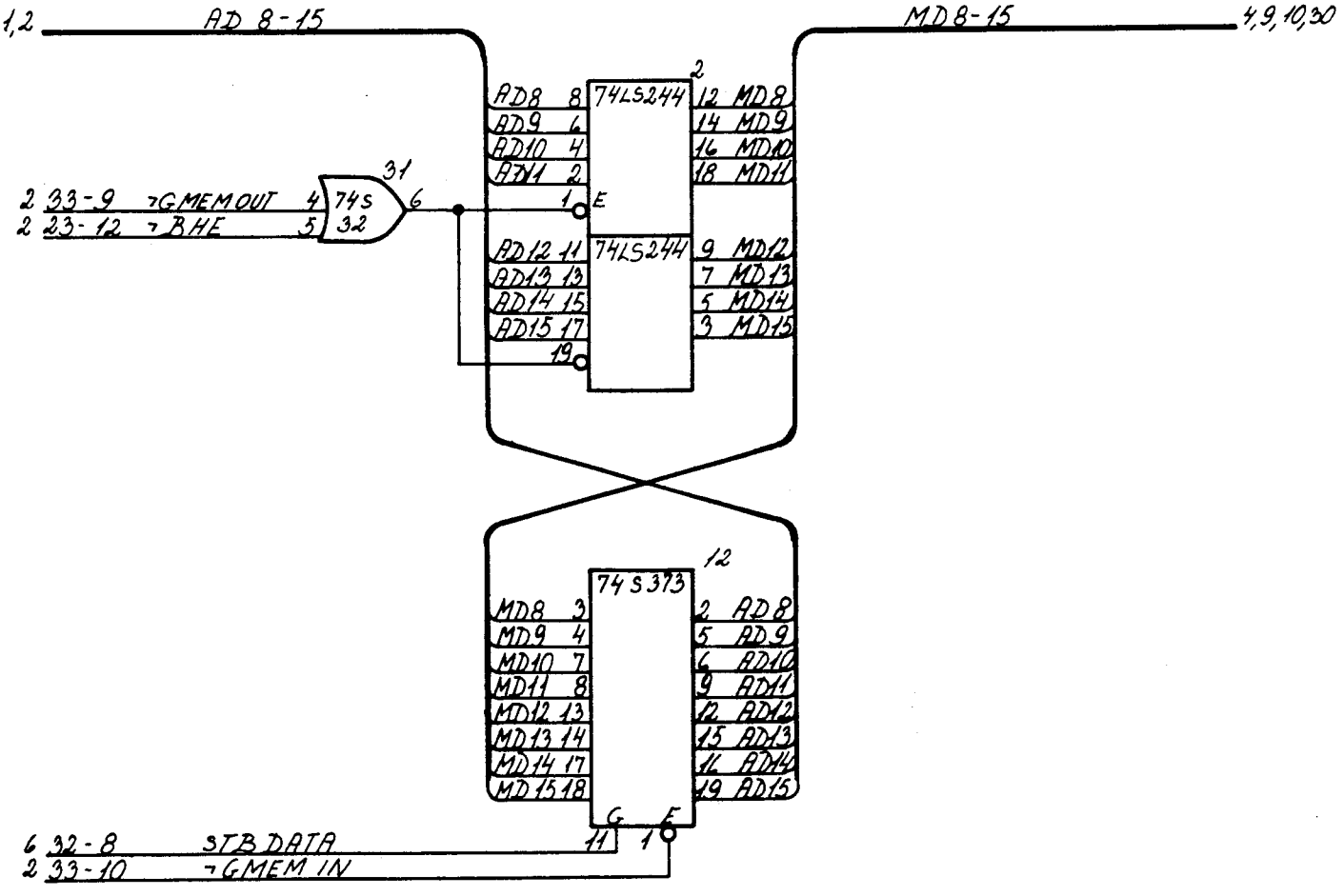

74S 240
CPUCLK
RESET
80186
RESET
CLKOUT
POK
RES
X1
X2
12.000MHz
ADO-7
AD8-15
A16 *
A17 *
A18 *
A19 *
BHE *
S0 *
S1 *
S2 *
LOCK *
RD
WR
DEN
DT/R
TEST
1K
R23
ARDY
SRDY
DRQ 0
DRQ 1
R25
PARITY
CRT HOLD
W2
NMI
INT0
INT1
R28
TMRIN0
TMRIN1
HOLD
HLDA
LCS
MCS0
MCS1
MCS2
MCS3
UCS
PCS0
PCS1
PCS2
PCS3
PCS4
PCS5
PCS6
INTA0
INTA1
TMROUT0
TMROUT1
T0
T1
80186
0V 26,60
+5V 9,43

Signal	Description
AD 0-19	Memory or I/O address for the current buscycle.
-BHE	Byte High Enable: latched version of the signal on the CPU.
-S 0-2	Bus status: latched versions of the signals on the CPU.
1 D 0-7	Databus used for transfer to or from peripherals having TTL bus interface.
2 D 0-7	Databus used for transfer to or from peripherals having MOS bus interface.
-GMEM IN/OUT	Gate memory data in/out: Controls for memory bus buffers.


1,2,3 AD 0-7
74LS373 21
AD0 A0
1,2,3 AD 8-15
74LS373 22
AD8 A8
74LS373 23
1 63-68 A16 *
1 63-67 A17 *
1 63-66 A18 *
1 63-65 A19 *
1 63-64 ¬BHE *
1 63-54 ¬S2 *
1 63-53 ¬S1 *
1 63-52 ¬S0 *
A16 A17 A18 A19 ¬BHE ¬S2 ¬S1 ¬S0
8 41-6 ALE
G E
R1
0V
1,2,3 AD 0-7
74LS245 74
1D0
1D0-7
DIR OE
23-16 ¬S1
33-4 ¬IO1
1,2,3 AD 0-7
74LS245 64
2D0
2D0-7
DIR OE
23-16 ¬S1
33-5 ¬IO2
33
1 63-39 ¬DEN
B3-8 BUS 2 SELECT
23-15 S2
74LS139
1 63-39 ¬DEN
1 23-16 ¬S1
23-15 ¬S2
¬IO1
¬IO2
¬GMEM IN
¬GMEM OUT

Signal	Description
MD 0-15	Memory databus connected to Main memory, Pixel memory and Read Only memory.

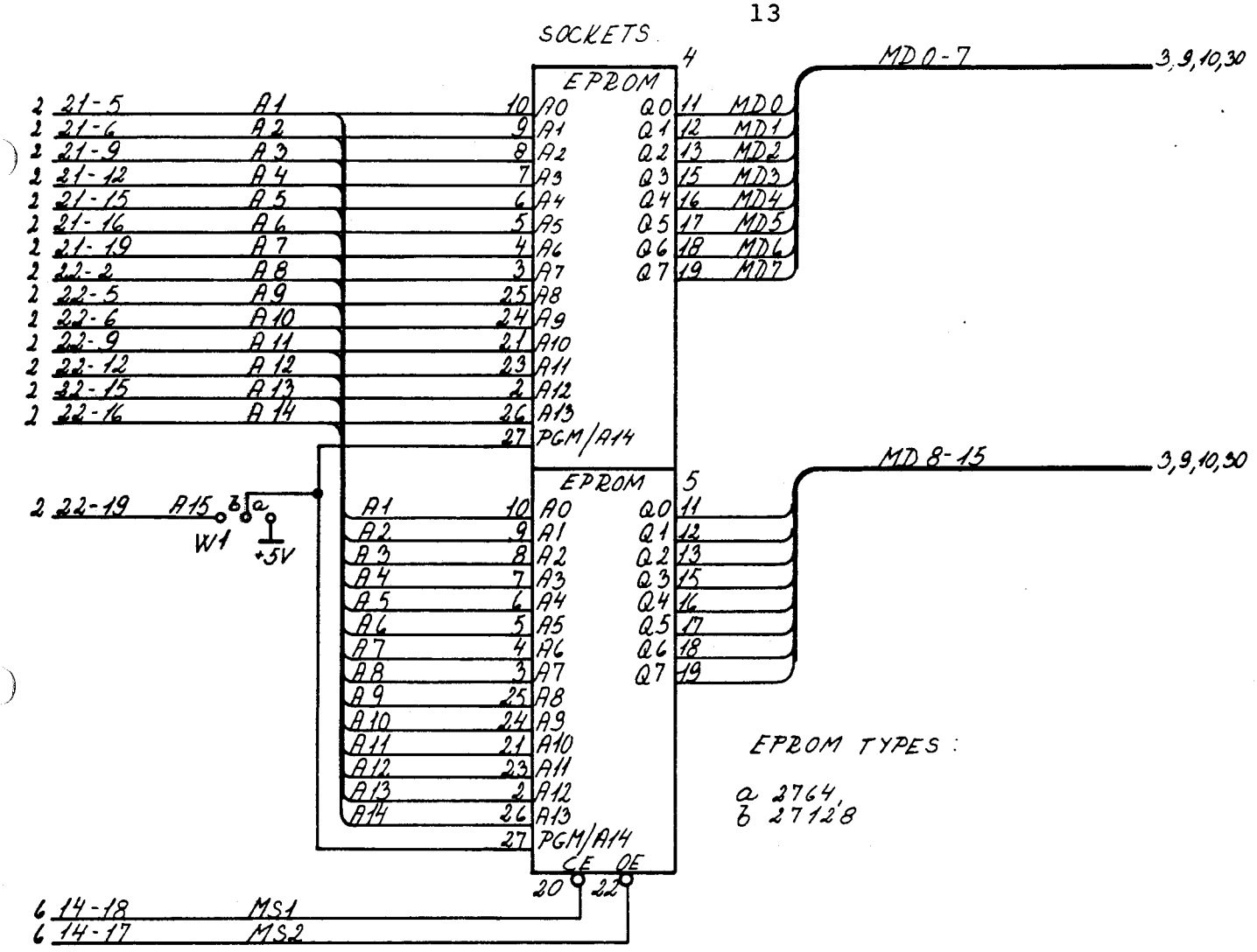

1,2
AD 0-7
MD 0-7
4,9,10,30
74LS244
74S373
74S
32
2 33-9 ¬GMEMOUT
2 21-2 A0
6,32-8 STB DATA
2 33-10 ¬GMEM IN

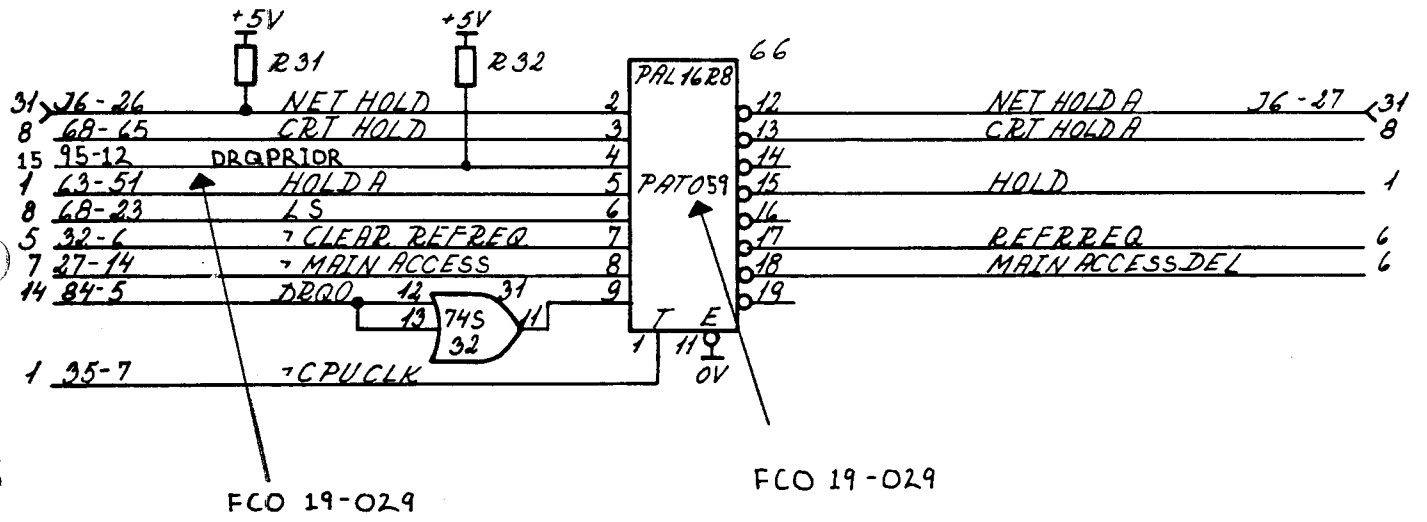

1,2
AD 8-15
MD 8-15
4,9,10,30
74LS244
74S373
74S
32
2 33-9 ¬GMEMOUT
2 23-12 ¬BHE
6,32-8 STB DATA
2 33-10 ¬GMEM IN

AGA 08.83

Signal	Description
MD 0-15	Memory databus.
NET HOLDA	Coprocessor hold acknowledge.
CRT HOLDA	CRT controller hold acknowledge.
HOLD	Hold request to CPU.
DRQPRIOR	Changes the DMA-priority with respect to CRT and LAN.

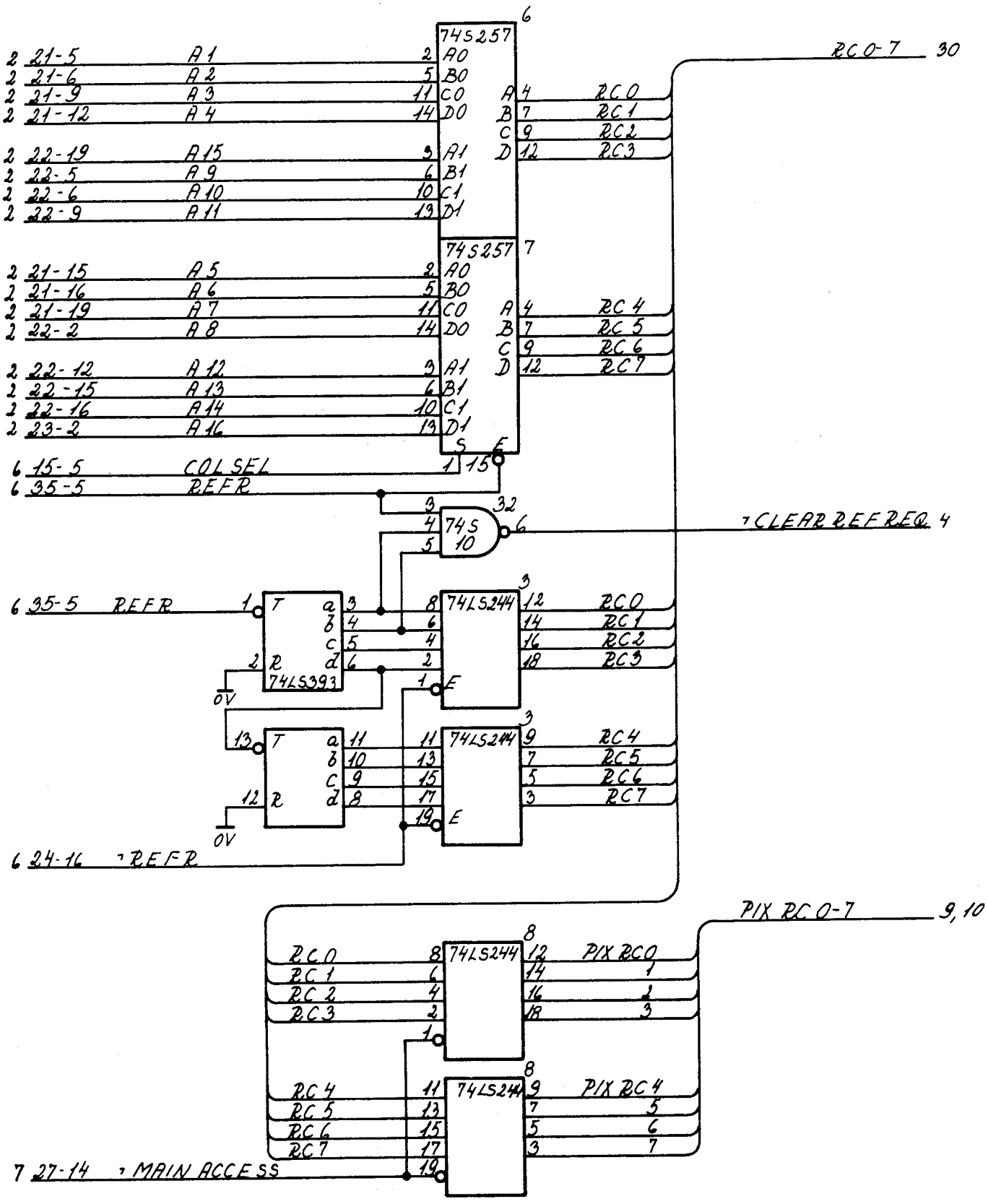
```
PAL16R8                                   PAL DESIGN SPECIFIKATION
PAT059                                    PKA 840329
BUS ARBITOR

CPUCK /NETH CRTH DRQPRIOR HLDA LS /CLREF /MACC DRQ GND
/E NETA CRTA /DRQD HOLD /NETAD REFRQ /MACCD /MACCDD VCC

/NETA   := /NETH + /HLDA + CRTA + DRQD + /HOLD
/CRTA   := /CRTH + /HLDA + NETH*/CRTA + NETA + DRQD + /HOLD
/HOLD   := /NETH*/CRTH + /HOLD*DRQ*/DRQPRIOR + /HOLD*DRQD +
           NETAD*/NETH + /NETAD*DRQD*/CRTH
/REFRQ  := /LS
MACCD   := MACC*/MACCD*/MACCDD
MACCDD  := MACCD
DRQD    := NETA*DRQ*/DRQPRIOR + CRTA*DRQ*/DRQPRIOR +
           DRQD*DRQ*/DRQPRIOR + /HOLD*HLDA + DRQD*HLDA
NETAD   := NETA + NETAD*DRQD
DESCRIPTION:
```


SOCKETS
EPROM 4
EPROM 5
MD 0-7
MD 8-15
3,9,10,30
2 21-5 A1
2 21-6 A2
2 21-9 A3
2 21-12 A4
2 21-15 A5
2 21-16 A6
2 21-19 A7
2 22-2 A8
2 22-5 A9
2 22-6 A10
2 22-9 A11
2 22-12 A12
2 22-15 A13
2 22-16 A14
2 22-19 A15
W1
+5V
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 PGM/A14
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7
CE OE
20 22
6 14-18 MS1
6 14-17 MS2
EPROM TYPES :
a 2764,
b 27128


+5V
R31
R32
66
PAL16R8
PAT059
31 J6-26 NET HOLD
8 G8-G5 CRT HOLD
15 95-12 DRQPRIOR
1 G3-51 HOLD A
8 G8-23 LS
5 32-6 ¬CLEAR REFREQ
7 27-14 ¬MAIN ACCESS
14 84-5 DRQO
1 35-7 ¬CPUCLK
74S 32
NET HOLD A J6-27 31
CRT HOLD A 8
HOLD 1
REFRREQ 6
MAIN ACCESS DEL 6
0V
FCO 19-029
FCO 19-029

AGA 83.10.27

Signal	Description
RC 0-75	Row and Column address multiplexed for addressing of the main memory consisting of DRAM's.
CLEAR REFREQ	This signal is active when the fourth refresh cycle in each refresh burst is being executed, indicating the end of the burst.
PIX RC 0-7	Row and Column address multiplexed for addressing of the pixel memory.



CPU 752

ADDRESSMULTIPLEXERS FOR
ROW/COLOUMN SELECTION & REFRESH ADDRESS COUNTER

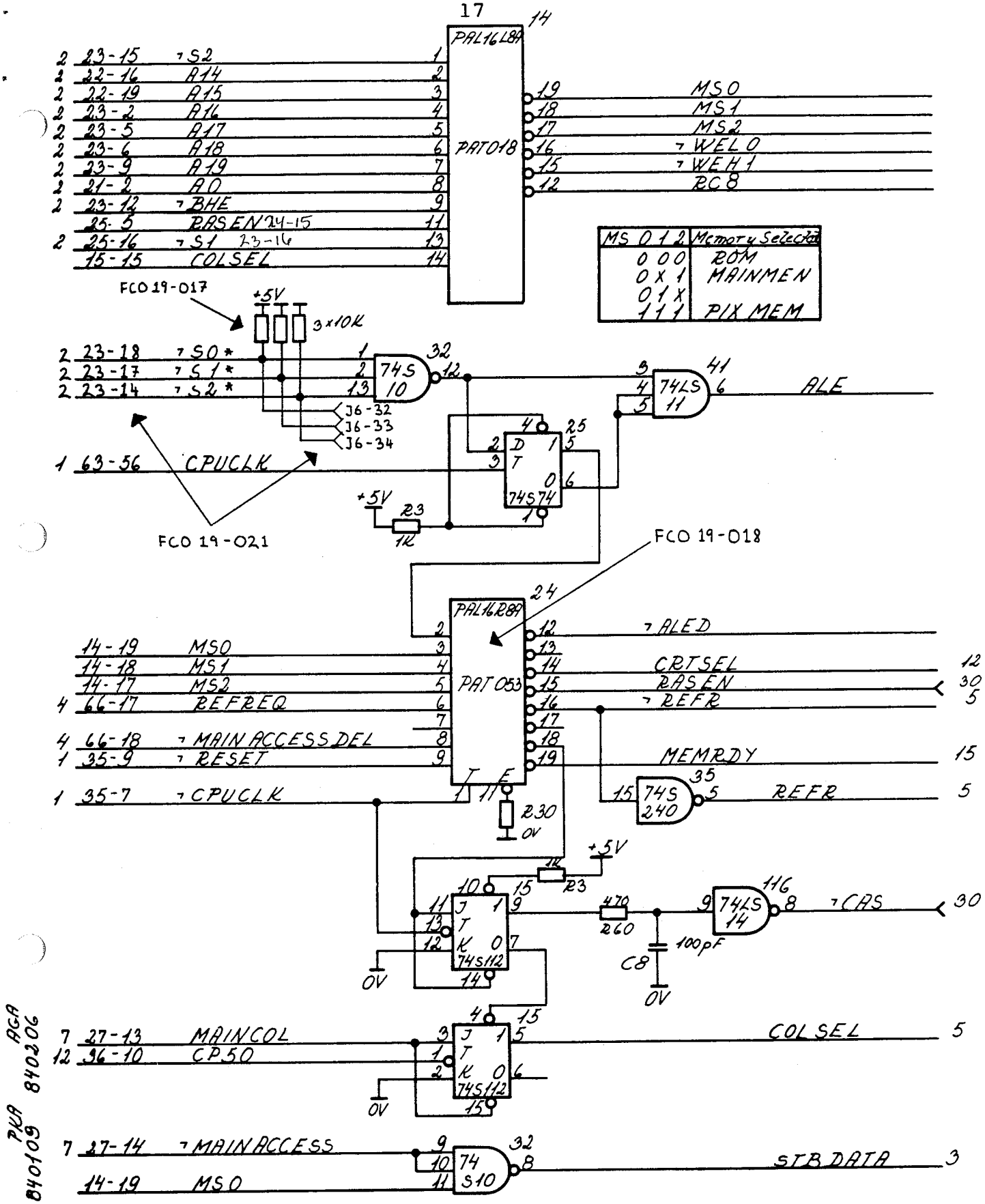
5

Signal	Description
MS 0-2	Memory selection code
WE LO/HI	Write enable for low and high byte
/RC8	A18 and A19 multiplexed

```
PAL16L8                          PAL DESIGN SPECIFIKATION
PAT0018                           PKA 830719
      MEMADDR. DECODER RC750

/S2 A14 A15 A16 A17 A18 A19 A0 /BHE GND
RASEN RC8 /S1 COLSEL /WEHI /WELO
MS2 MS1 MS0 VCC

IF(VCC)    /MS0 = /A19+/A18+/A17+/A16+A15+S2
IF(VCC)    /MS1 = A19*A18*A17*A16*A15+
                  /A19*/A18*/A17+S2
IF(VCC)    /MS2 = A19*A18*A17*A16*A15+
                  /A19*/A18*A17+S2
IF(VCC)    WELO = /S2*/S1*/A0
IF(VCC)    WEHI = /S2*/S1*BHE
IF(VCC)    /RC8 = /COLSEL*/A18+COLSEL*/A19

DESCRIPTION:
```

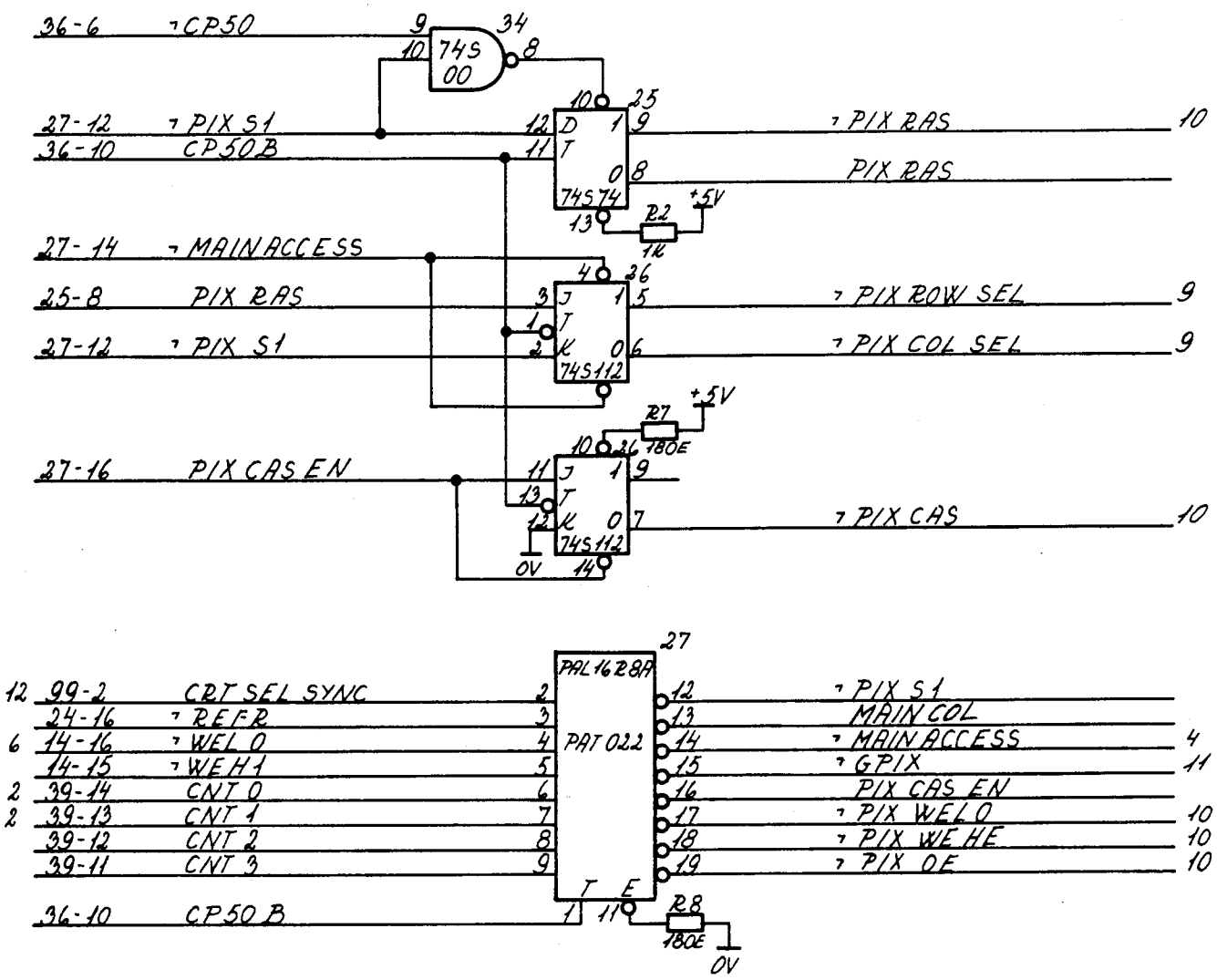
```
PAL16R8A                    PAL DESIGN SPECIFIKATION
PAT053 (PAT020 REPLACEMENT)     PKA 840201
    MAIN MEMORY CONTROLLER

CPUCLK ALE MS0 MS1 MS2 REFREQ NC /MAINACC /RESET GND
/OE /ALED MAINM CRTSEL RASEN /REFR /CAS COLSEL MRDY VCC

ALED    := ALE

/MAINM  := CAS + MAINACC
         + /MAINM*MRDY*/ALE*/REFREQ + /MAINM*MRDY*ALED*/REFREQ
         + /MAINM* MS0*/REFREQ + /MAINM*/MS1*/MS2*/REFREQ
         + /MAINM*RASEN

/CRTSEL := MAINACC + RESET
         + /CRTSEL*MRDY*/ALE*/REFREQ + /CRTSEL*MRDY*ALED*/REFREQ
         + /CRTSEL*/MS0*/REFREQ + /CRTSEL*RASEN
         + /CRTSEL*REFREQ*/REFR

/RASEN  := CAS + MAINACC
         + /RASEN*MRDY*/ALE*/REFREQ + /RASEN*MRDY*ALED*/REFREQ
         + /RASEN*/MS0*/MS1*/MS2*/REFREQ + /RASEN*REFREQ*/REFR


REFR    := REFR*/MAINACC*/RESET
         + REFREQ*/RASEN*/MAINM*/CRTSEL*/MAINACC

/COLSEL := CAS + /COLSEL*MRDY*/ALE + /COLSEL*MRDY*ALED
         + /COLSEL*/MS0*/MS1*/MS2 + /COLSEL*MS0
         + /COLSEL*RASEN + /COLSEL*REFREQ
         + /COLSEL*REFR

CAS     := /CAS*RASEN*/REFR*/CRTSEL*MS2
         + /CAS*RASEN*/REFR*/CRTSEL*MS1
         + RESET
/MRDY   :=  ALE*/ALED*REFR*MS1 + ALE*/ALED*REFREQ*MS1
         +  ALE*/ALED*REFR*MS2 + ALE*/ALED*REFREQ*MS2
         +  ALE*/ALED*MS0
         + /MRDY*REFR + /MRDY*REFREQ + /MRDY*MS0*/MAINACC

DESCRIPTION:
```

CRTSEL	Access to pixel memory
RASEN	Enable Row Address Selection
REFR	Refresh cycle in progress
COLSEL	Control signal to address mux
STBDATA	Load datalatches with MB0-15


PAL16L8A
14
PAT018
2 23-15 ¬S2
2 22-16 A14
2 22-19 A15
2 23-2 A16
2 23-5 A17
2 23-6 A18
2 23-9 A19
2 21-2 A0
2 23-12 ¬BHE
25-5 RASEN 24-15
2 25-16 ¬S1 23-16
15-15 COLSEL
19 MS0
18 MS1
17 MS2
16 ¬WEL 0
15 ¬WEH 1
12 RC8
MS 0 1 2 | Memory Selected
0 0 0 ROM
0 X 1 MAINMEN
0 1 X
1 1 1 PIX MEM
FCO 19-017
+5V
3x10K
2 23-18 ¬S0*
2 23-17 ¬S1*
2 23-14 ¬S2*
74S 10
32
J6-32
J6-33
J6-34
41
74LS 11
ALE
25
D T 0
74S74
1 63-56 CPUCLK
+5V
23
1K
FCO 19-021
FCO 19-018
24
PAL16R8A
PAT053
14-19 MS0
14-18 MS1
14-17 MS2
4 66-17 REFREQ
4 66-18 ¬MAIN ACCESS DEL
1 35-9 ¬RESET
1 35-7 ¬CPUCLK
¬ALED
CRTSEL
RASEN
¬REFR
MEMRDY
12
30
5
15
35
74S 240
REFR
5
R30
0V
+5V
1K
R23
10
15
J T K 0
74S112
11
13
12
7
14
0V
470
R60
116
74LS 14
¬CAS
30
100pF
C8
0V
4
15
MAINCOL
CP50
COLSEL
5
7 27-13
12 36-10
0V
7 27-14 ¬MAIN ACCESS
14-19 MS0
74 S10
32
STB DATA
3
PCA 840206
PKA 840109

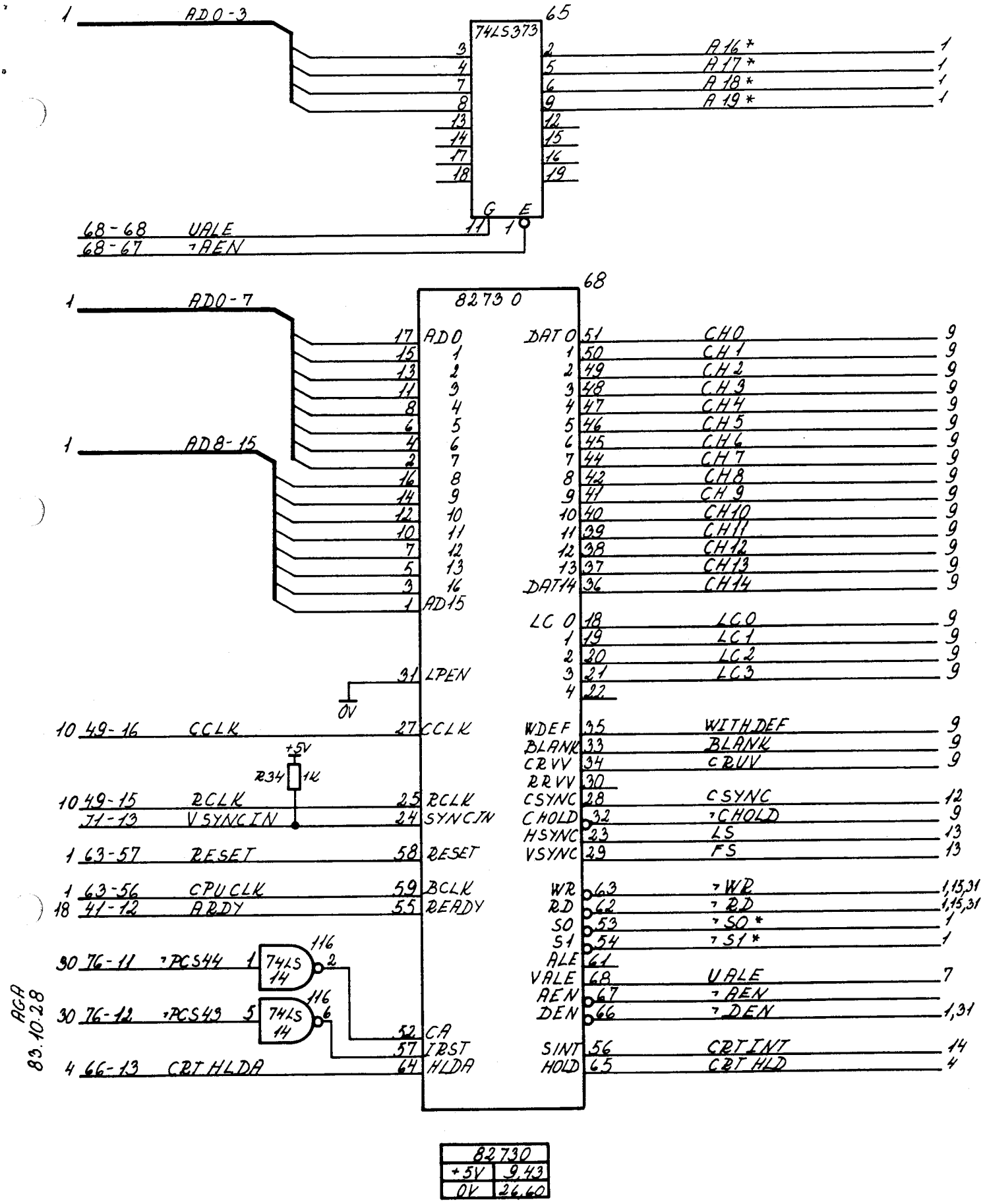
Signal	Description
PIXRAS	RAS signal to Pixel memory
/PIXROWSEL	Selection signals to address multiplexer
/PIXCOLSEL	for addresses generated by 82730. Both inactive when a mainaccess is in progress, as main memory controller supplies multiplexed address.
PIXCAS	CAS signal to Pixel memory
PIX S1	Pixel memory cycle in progress
MAINCOL	Address multiplex control signal during main access.
MAINACCESS	Main system (CPU or coprocessor) is accessing the Pixel memory.
GPIX	Connects the PIX memory data bus to the Main memory data bus.
PIXWELO/HI	Write enable LO and HI for the pix memory
PIXOE	Output enable to pix memory chips.

```
PAL16R8A                    PAL DESIGN SPECIFIKATION
PAT022                       PKA 830721
         PIXEL MEMORY CONTROLLER

CP50 CRTSEL /REFR /WELO /WEHI CNT0 CNT1
CNT2 CNT3 GND /E /PIXS1 MAINCOL /MAINACC
/GPIX PIXCASEN /PIXWELO /PIXWEHI
/PIXOE VCC

PIXS1     := CNT0*/CNT1*/CNT2*/CNT3*CRTSEL +
             CNT0*/CNT1*/CNT2*CNT3 +
             PIXS1*/CNT0 +
             PIXS1*/CNT2
MAINACC   := CNT0*/CNT1*/CNT2*/CNT3*CRTSEL +
             MAINACC*/CNT1 +
             MAINACC*/CNT2
GPIX      := CNT0*/CNT1*/CNT2*/CNT3*CRTSEL*/REFR +
             GPIX*/CNT0 +
             GPIX*/CNT1 +
             GPIX*/CNT2
/PIXCASEN:= /GPIX*/CNT3 +
             /CNT2*/CNT1 +
             /CNT2*/CNT0 +
             CNT0*CNT1*CNT2
PIXWELO   := WELO*MAINACC*/REFR
PIXWEHI   := WEHI*MAINACC*/REFR
PIXOE     := CNT3 + MAINACC*/PIXWELO*/PIXWEHI*/WELO*/WEHI
/MAINCOL:= /MAINACC + CNT0*CNT1*CNT2

DESCRIPTION:
```


36-6 ¬CP50
74S 00
27-12 ¬PIX S1
36-10 CP50B
74S74
¬PIX RAS
PIX RAS
R2 1K
+5V
27-14 ¬MAIN ACCESS
25-8 PIX RAS
27-12 ¬PIX S1
74S112
¬PIX ROW SEL
¬PIX COL SEL
R7 180E
27-16 PIX CAS EN
0V
¬PIX CAS
PAL16R8A
PAT 022
99-2 CRT SEL SYNC
24-16 ¬REFR
14-16 ¬WEL0
14-15 ¬WEH1
39-14 CNT 0
39-13 CNT 1
39-12 CNT 2
39-11 CNT 3
36-10 CP50B
¬PIX S1
MAIN COL
¬MAIN ACCESS
¬GPIX
PIX CAS EN
¬PIX WEL0
¬PIX WE HE
¬PIX OE
R8 180E
0V

AGA
83.10.28

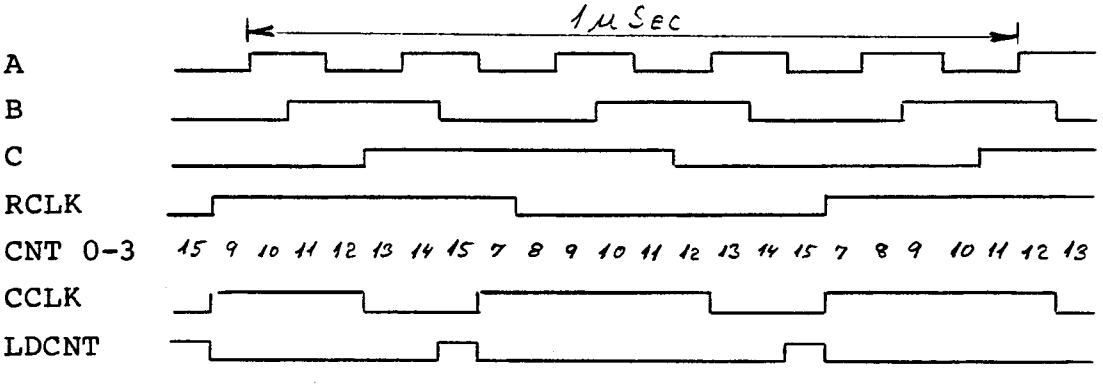
Signal	Description
A16-19*	Most Significant addressbits generated by 74LS373 which is loaded from the Processor bus on UALE (Upper Address Latch Enable) time.
CH 0-14	Value of next displayed character clocked out of 82730 on CCLK.
LC 0-3	Video Line Count bits indication video line no within one row.
BLANK	Next character shall not be displayed
CRVV	Next character shall be displayed in reverse video.
CSYNC	True during retrace for syncronizing CCLK to RCLK.
CHOLD	When active the CCLK is stopped.
LS	Line sync
FS	Frame sync
-WR	
-RD	Bus controls
-S0*	For the coprocessor bus
-S1*	
CRTALE	
UALE	Upper Address Latch Enable
CRT INT	Interrupt signal (IR3)
CRT HLD	Coprocessor bushold request.

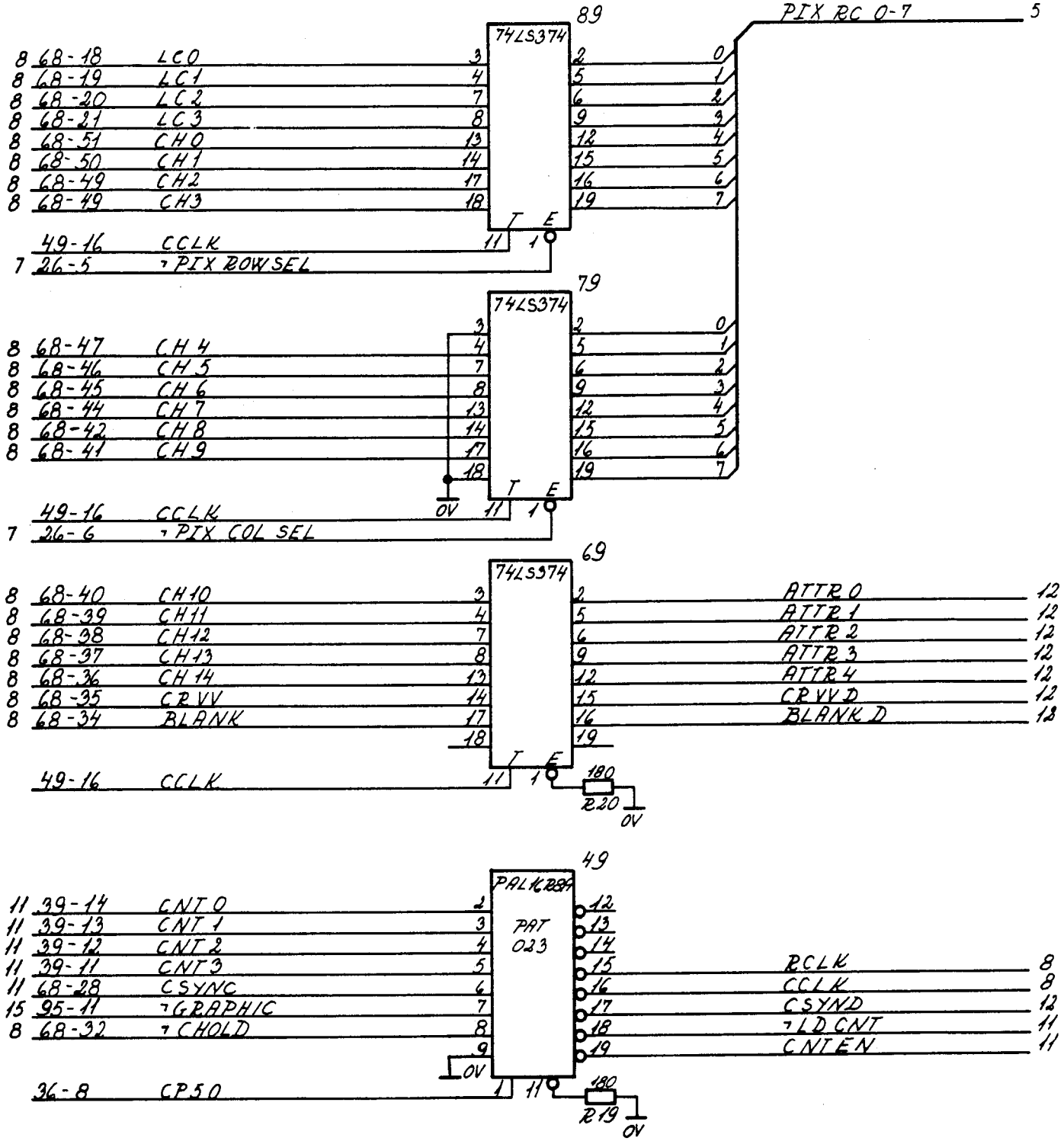

74LS373
ADO-3
A16*
A17*
A18*
A19*
68-68 UALE
68-67 ¬AEN
8273 0
ADO-7
AD8-15
DAT 0
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
CH9
CH10
CH11
CH12
CH13
DAT14
CH14
LC 0
LC0
LC1
LC2
LC3
LPEN
CCLK
+5V
R34 1K
RCLK
VSYNCIN
RESET
CPUCLK
ARDY
¬PCS44
¬PCS43
74LS 14
CA
IRST
CRT HLDA
HLDA
WDEF
WITH.DEF
BLANK
CRVV
RRVV
CSYNC
¬CHOLD
LS
FS
WR
RD
SO
S1
ALE
VALE
AEN
DEN
SINT
HOLD
CRT INT
CRT HLD
82730
+5V 9.43
0V 26.60

AGA 83.10.28

Signal	Description
PIXRC 0-7	Pipelined and multiplexed characterbits and videoline count bits for read into the pixel memory.
ATTR 0-4	Pipelined version of character bits 10-14
CRVVD, BLANKD	Pipelined versions of CRUV and BLANK

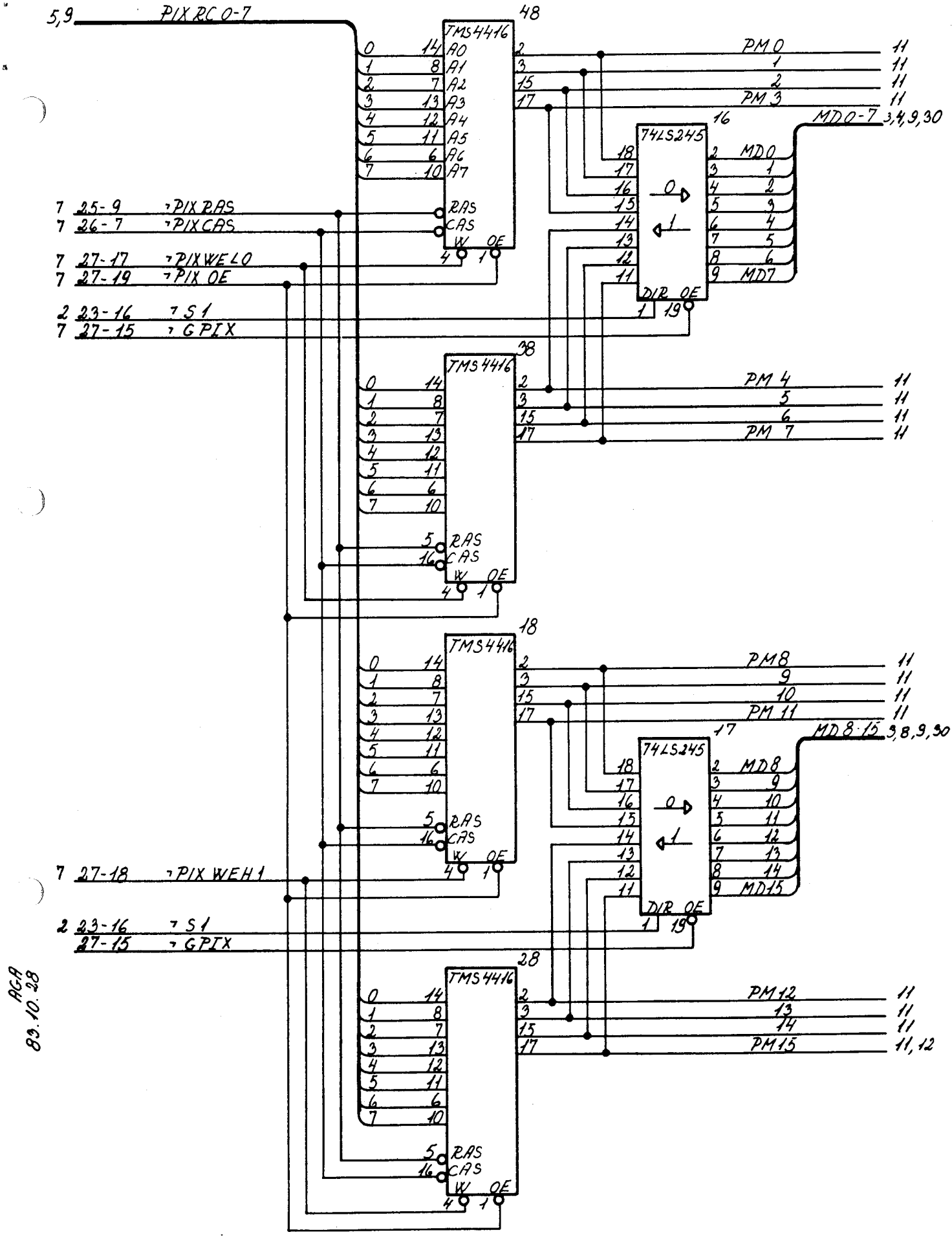
```
PAL16R8A                          PAL DESIGN SPECIFICATION
PAT023                              PKA 830921
                    CRT CLOCK CONTROL

CP50 CNT0 CNT1 CNT2 CNT3 CSYNC /GRAPH /CHOLD NC GND
/OE /A /B /C RCLK CCLK CSYND /LDCNT CNTEN VCC

A       := /B*/C*/RCLK
         +  B* C*/RCLK
         + /B* C* RCLK
         +  B*/C* RCLK

B       :=  A*/C*/RCLK
         +  A* C* RCLK
         + /A* B

C       := /A* B*/RCLK
         +  C*/RCLK
         +  C*/B
         +  C* A

/RCLK   := /A*/B*/C
         + /RCLK* A
         + /RCLK* B
         + /RCLK*/C

/CCLK   :=  CCLK* CNT3* CNT2*/CNT1*/CNT0*/CHOLD
         + /CCLK*/CNT1
         + /CCLK*/CNT0

/CSYND  := /CSYNC
         + /CSYND* RCLK
         + /CSYND*/C
         + /CSYND* B

/CNTEN  := CSYND* CNT1* CNT2* CNT3* B
         + CSYND* CNT1* CNT2* CNT3*/C
         + CSYND* CNT1* CNT2* CNT3* RCLK
         + CCLK * CNT1* CNT2* CNT3* B
         + CCLK * CNT1* CNT2* CNT3*/C
         + CCLK * CNT1* CNT2* CNT3* RCLK

LDCNT   := /LDCNT* CNT1* CNT2* CNT3*/CSYND*/GRAPH*/CCLK

DESCRIPTION:
```




89
74LS374
8 68-18 LC0
8 68-19 LC1
8 68-20 LC2
8 68-21 LC3
8 68-51 CH0
8 68-50 CH1
8 68-49 CH2
8 68-49 CH3
49-16 CCLK
7 26-5 ¬PIX ROWSEL
PIX RC 0-7 5
79
74LS374
8 68-47 CH4
8 68-46 CH5
8 68-45 CH6
8 68-44 CH7
8 68-42 CH8
8 68-41 CH9
0V
49-16 CCLK
7 26-6 ¬PIX COL SEL
69
74LS374
8 68-40 CH10
8 68-39 CH11
8 68-38 CH12
8 68-37 CH13
8 68-36 CH14
8 68-35 CRVV
8 68-34 BLANK
49-16 CCLK
180
R20
0V
ATTR 0 12
ATTR 1 12
ATTR 2 12
ATTR 3 12
ATTR 4 12
CRVVD 12
BLANKD 12
49
PALK82A
PAT
023
11 39-14 CNT0
11 39-13 CNT1
11 39-12 CNT2
11 39-11 CNT3
11 68-28 CSYNC
15 95-11 ¬GRAPHIC
8 68-32 ¬CHOLD
0V
36-8 CP50
180
R19
0V
RCLK 8
CCLK 8
CSYND 12
¬LD CNT 11
CNTEN 11

AGA
83.10.28

Signal	Description
PM 0-15	Pixel memory databus.


5,9 PIX RC 0-7
TMS4416
48
AO A1 A2 A3 A4 A5 A6 A7
RAS CAS W OE
PM 0 PM 1 PM 2 PM 3
74LS245
16
MD0-7 3,4,9,30
MD0 MD7
DIR OE
7 25-9 PIX RAS
7 26-7 PIX CAS
7 27-17 PIX WE L0
7 27-19 PIX OE
2 23-16 S1
7 27-15 GPIX
38
PM 4 PM 5 PM 6 PM 7
18
PM 8 PM 9 PM 10 PM 11
17
MD8-15 3,8,9,30
MD8 MD15
7 27-18 PIX WE H1
28
PM 12 PM 13 PM 14 PM 15 11,12
AGA 89.10.28

Signal	Description

CNT 0-3

Dot counter output used to generate CCLK and to control Pix memory cycles.
When not in graphic mode, the dot counter is loaded with 16-char width. Char width is derived from the dotpattern read in the pixel memory by means of ROA914:

PM 7	6	5	4	3	2	1	0	16-char width	char width
X	X	X	X	X	X	X	0	1	15
X	X	X	X	X	X	0	1	2	14
X	X	X	X	X	0	1	1	3	13
X	X	X	X	0	1	1	1	4	12
X	X	X	0	1	1	1	1	5	11
X	X	0	1	1	1	1	1	6	10
X	0	1	1	1	1	1	1	7	9
0	1	1	1	1	1	1	1	8	8
1	1	1	1	1	1	1	1	9	7

LOAD

Loads next dotpattern into the shiftregisters

PHASE

True every second clock period allowing the shifters to advance only every 100 nSec.

EVEN DOT

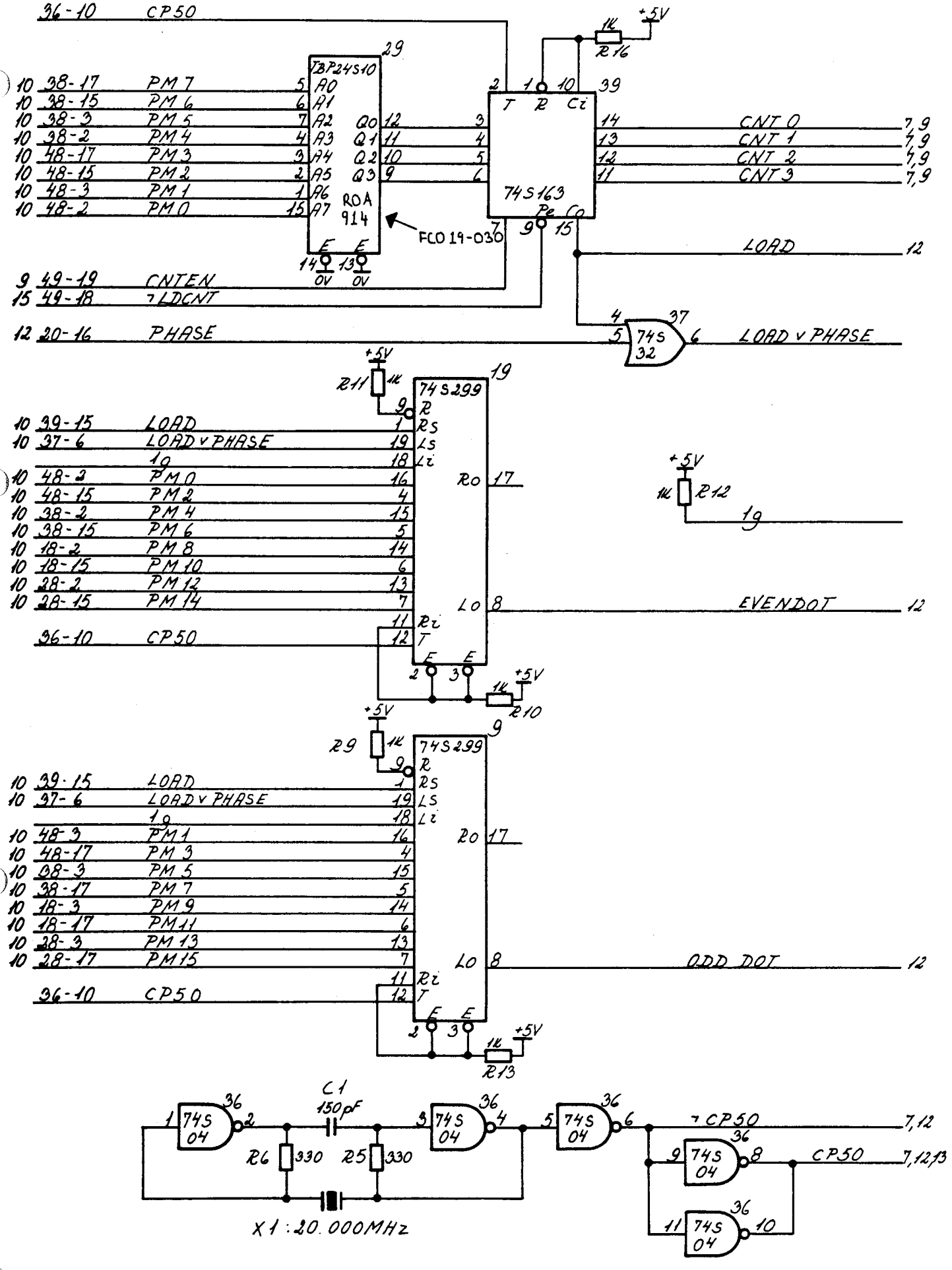
Reading the pairs of even and odd numbered.

ODD DOT

Dot bits out in parallel. This feature is used in low resolution graphics. When serial mono dot stream is used (alpha and high resolution) EVENDOT and ODD DOT are multiplexed in PAT 024 p.12

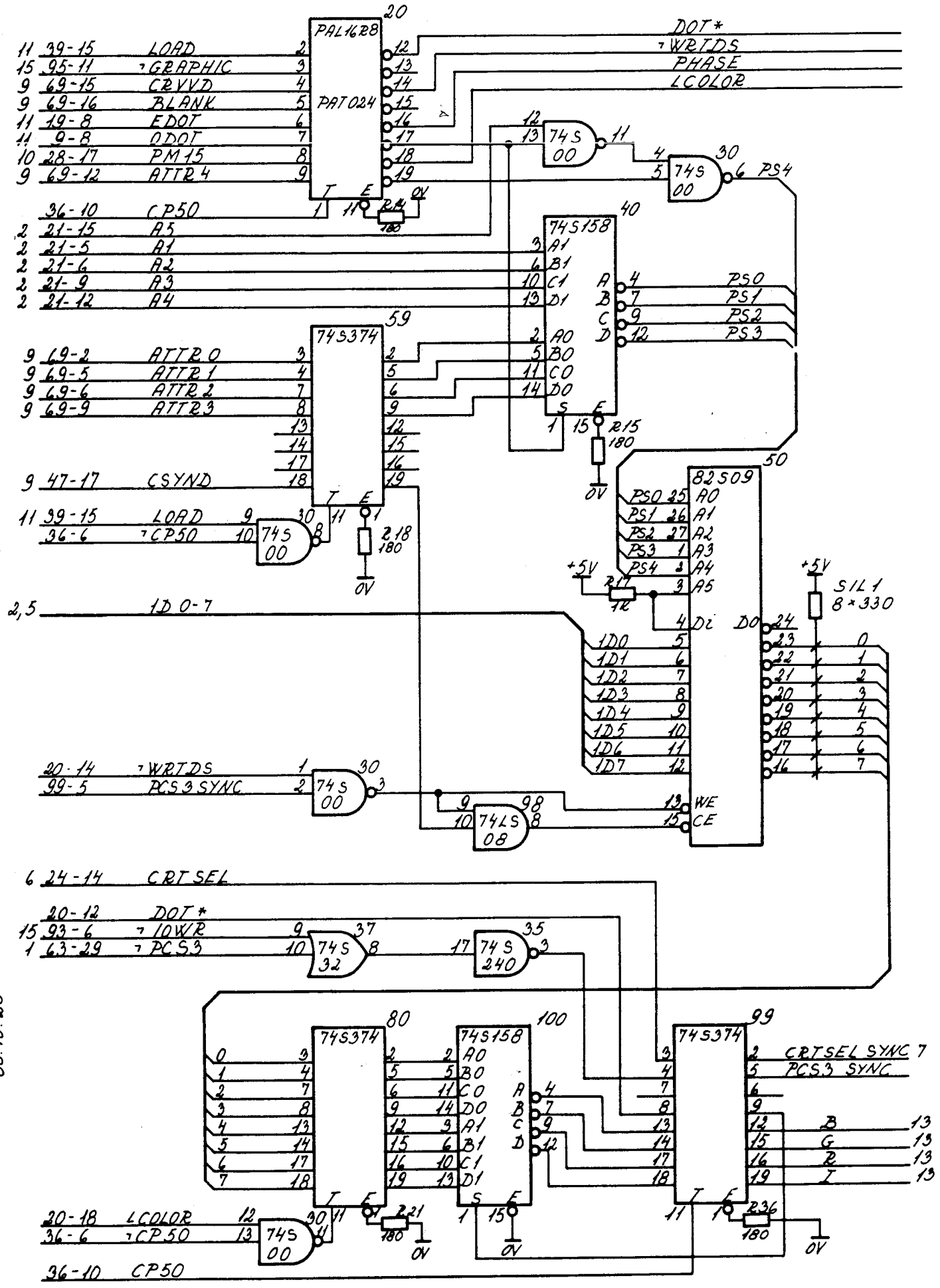
CP 50

20 MHz (50 nsec) dot clock.


36-10 CP50
29
TBP24S10
10 38-17 PM7
10 38-15 PM6
10 38-3 PM5
10 38-2 PM4
10 48-17 PM3
10 48-15 PM2
10 48-3 PM1
10 48-2 PM0
A0 A1 A2 A3 A4 A5 A6 A7
Q0 Q1 Q2 Q3
ROA 914
FCO 19-030
74S163
T R Ci Pe Co
CNT 0 7,9
CNT 1 7,9
CNT 2 7,9
CNT 3 7,9
LOAD 12
+5V
1K R16
9 49-19 CNTEN
15 49-18 ⁊LDCNT
12 20-16 PHASE
74S 32
LOAD v PHASE
74S299
R11 1K
10 39-15 LOAD
10 37-6 LOAD v PHASE
19
10 48-3 PM0
10 48-15 PM2
10 38-2 PM4
10 38-15 PM6
10 18-2 PM8
10 18-15 PM10
10 28-2 PM12
10 28-15 PM14
R Rs Ls Li Ro Lo Ri T E
EVENDOT 12
R12 1K
36-10 CP50
R10 1K
R9 1K
10 48-3 PM1
10 48-17 PM3
10 38-3 PM5
10 38-17 PM7
10 18-3 PM9
10 18-17 PM11
10 28-3 PM13
10 28-17 PM15
ODD DOT 12
R13 1K
AGA 83.10.18
C1 150pF
74S 04
R6 330
R5 330
X1 : 20.000MHz
⁊CP50 7,12
CP50 7,12,13

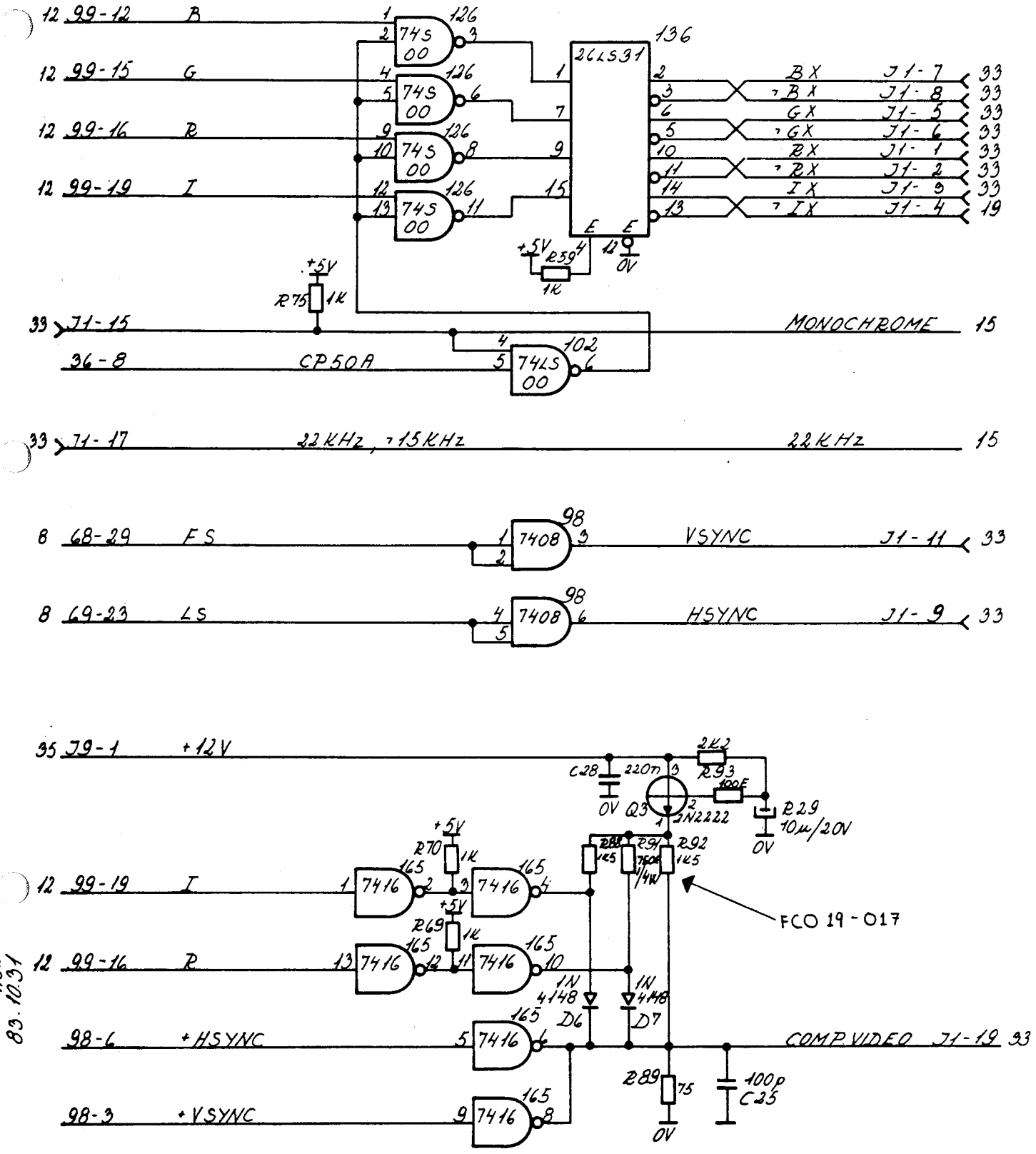
Signal	Description
DOT *	In low resolution graphics equal to ODD DOT else multiplex between ODD DOT and EVEN DOT on basis of PHASE. In alpha mode DOT* is off in case of BLANK and inverted in case of CRVVD.
-WRTDS	When the PALETTE is read and the contents are loaded into the Register pos. 80, programmed write pulses are gated off. When low Resolution Graphics are displayed, programmed writes to the Pallette are dummy, in other cases the write pulses are long enough to write the Pallette even if interrupted in the middle by a read.
PAT 024	
PIN 17	PallRD controls the address multiplexer for the Pallette (PS 0-4)
DOT*	is delayed one clock period before controlling the dot selector in pos. 100. This dot selector selects the high or low order four bits from the pallette register and presents them (via a syncronizing register) to the monitor as
B	Blue
G	Green
R	Read and
I	Intensity signals

```
PAL16R8A                PAL DESIGN SPECIFIKATION
PAT024                       PKA 830728
          CRT DOT GENERATOR

CP50 LOAD /GRAPH CRVVD BLANK EDOT ODOT PM15 ATTR4 GND
/OE DOT NC /WRTDS /ATTB4 PHASE /PALLRD LDCOL /COLSEL4 VCC

/PHASE  := /LOAD*PHASE +
           LOAD*/GRAPH +
           LOAD*/ATTR4

/DOT    :=    BLANK*/GRAPH*/CRVVD
          + /BLANK*PHASE*GRAPH*/EDOT
          + /BLANK*PHASE*/GRAPH*/CRVVD*/EDOT
          + /BLANK*PHASE*/GRAPH*CRVVD*EDOT
          + /BLANK*/PHASE*GRAPH*/ATTB4*/ODOT
          + /BLANK*/PHASE*GRAPH*ATTB4*/DOT
          + /BLANK*/PHASE*/GRAPH*/CRVVD*/ODOT
          + /BLANK*/PHASE*/GRAPH*CRVVD*ODOT

ATTB4   := /LOAD*ATTB4 +
           LOAD*ATTR4

PALLRD  :=  GRAPH*ATTB4 +
            LOAD +
            PALLRD*/LDCOL

/LDCOL  :=  LDCOL +
           /LDCOL*/GRAPH*/PALLRD +
           /LDCOL*/ATTB4*/PALLRD +
            GRAPH*ATTB4*/PHASE

COLSEL4 :=  GRAPH*ATTR4* LOAD*PM15 +
            PALLRD*GRAPH*ATTB4*/LOAD*ODOT +
            /GRAPH*ATTR4* LOAD +
            PALLRD*/GRAPH*ATTB4*/LOAD

WRTDS   :=  LOAD + PALLRD

DESCRIPTION:
```

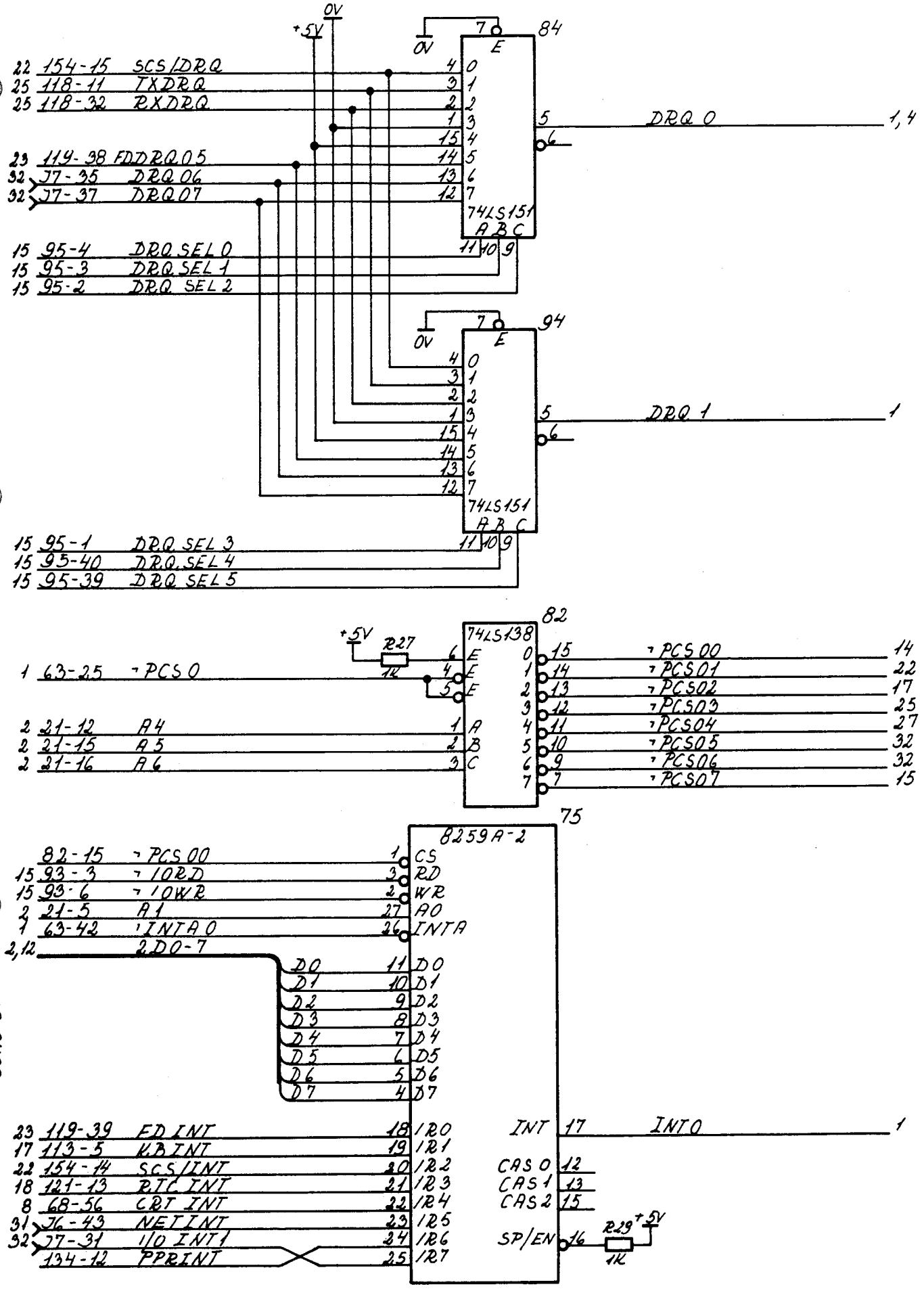

20
PAL16R8
PAT024
LOAD
GRAPHIC
CRVVD
BLANK
EDOT
ODOT
PM15
ATTR4
CP50
A5
A1
A2
A3
A4
DOT*
WRTDS
PHASE
LCOLOR
74S 00
30
PS4
40
74S158
PS0
PS1
PS2
PS3
59
74S374
ATTR0
ATTR1
ATTR2
ATTR3
CSYND
R15 180
50
82S09
R17 1K
+5V
SIL 1
8 × 330
1D0-7
WRTDS
PCS3 SYNC
74LS 08
WE
CE
CRTSEL
DOT*
IOWR
PCS3
74S 32
74S 240
80
100
99
CRTSEL SYNC
PCS3 SYNC
R21 180
R36 180
LCOLOR
CP50
0V

AGA
83.10.28

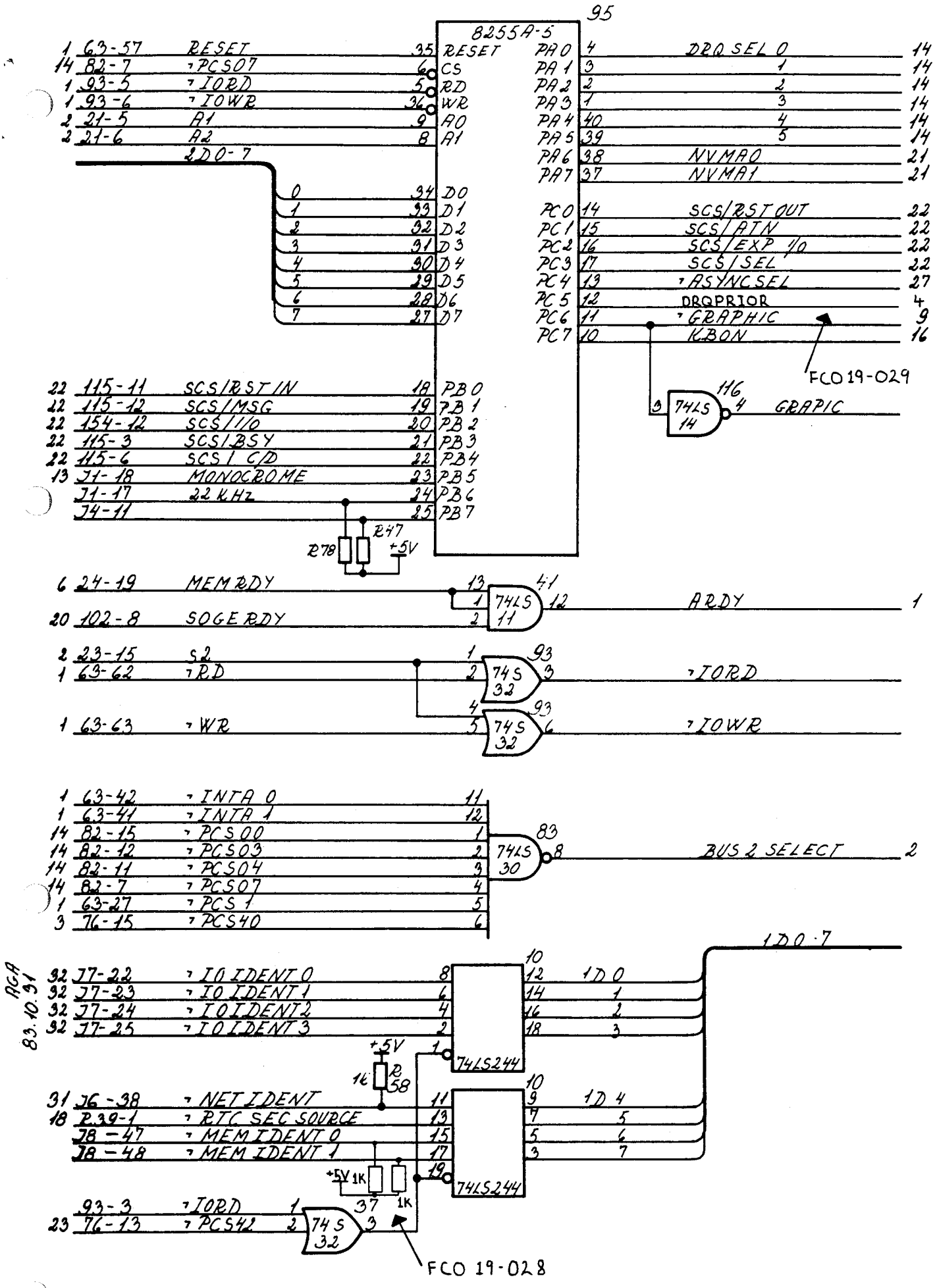
Signal	Description
Bx through Ix	These signals are balanced video signals for Blue, Green, Red and intensity. In the case no colour monitor is connected, the video signals are chopped to create a uniform horizontal and veritical characteristic on the screen.
22 KHz	This signal is grounded in the plug, in the case a television monitor is connected, and is read by the software on the input port p.15.
FS	Framesync to monitor.
LS	Line sync to monitor (also used to start refresh cycles in memory).
COMP VIDEO	Composite video signal.


12 99-12 B
12 99-15 G
12 99-16 R
12 99-19 I
74S 00
126
136
26LS31
BX J1-7 33
-BX J1-8 33
GX J1-5 33
-GX J1-6 33
RX J1-1 33
-RX J1-2 33
IX J1-3 33
-IX J1-4 19
+5V
R39 1K
R75 1K
33 J1-15
MONOCHROME 15
36-8 CP50A
74LS 00
102
33 J1-17 22KHz, -15KHz 22KHz 15
8 68-29 FS
8 69-23 LS
7408
98
VSYNC J1-11 33
HSYNC J1-9 33
35 J9-1 +12V
C28 220n
R93 2K2
100E
Q3 2N2222
R29 10µ/20V
R70 1K
R69 1K
7416
165
R91 1K5
R92 1K5
FCO 19-017
1N 4148
D6
D7
98-6 +HSYNC
98-3 +VSYNC
COMPVIDEO J1-19 33
R89 75
C25 100p
RGA 83.10.31

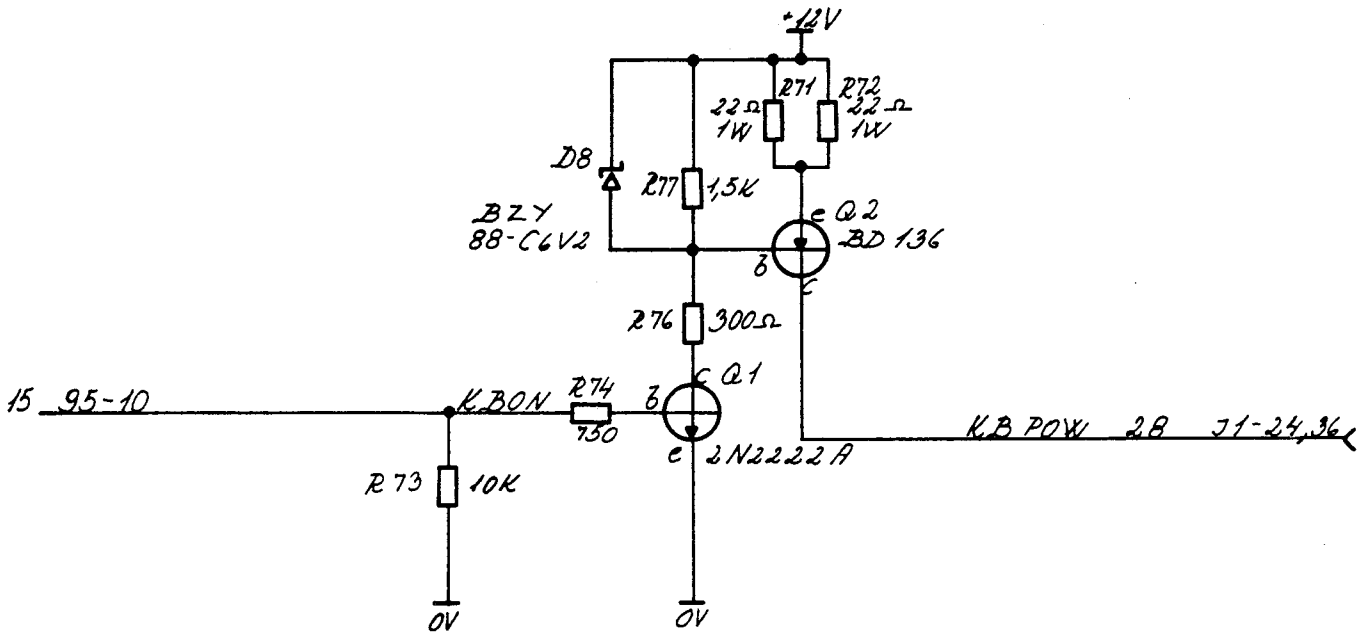
Signal	Description
DRQ 0	Data channel Request 0. Arranged to have higher priority than the coprocessors.
DRQ 1	Has lower priority than the coprocessors. This priority is established partly in the CPU and partly in PAT 059 on page 4.
PCS00 to PCS07	Are further decoding of the Peripheral Chip Select output no. 0 from the CPU. They are addressed as IO ports in the address ranges: Peripheral: PCS00: 0 to E 8259 PCS01: 10 to 1E SCSI bus PCS02: 20 to 2E Keyboard PCS03: 30 to 3E 8274 PCS04: 40 to 4E PCS05: 50 to 5E Sound generator PCS06: 60 to 6E I/O Xpansion PCS07: 70 to 7E 8255
INTO	Interrupt input to CPU.


0V
+5V
84
74LS151
A B C
22 154-15 SCS/DRQ
25 118-11 TXDRQ
25 118-32 RXDRQ
29 114-38 FDDRQ05
32 J7-35 DRQ06
32 J7-37 DRQ07
15 95-4 DRQ SEL 0
15 95-3 DRQ SEL 1
15 95-2 DRQ SEL 2
DRQ 0
1,4
94
74LS151
A B C
15 95-1 DRQ SEL 3
15 95-40 DRQ SEL 4
15 95-39 DRQ SEL 5
DRQ 1
1
82
74LS138
+5V
R27
1K
1 63-25 ¬PCS 0
2 21-12 A4
2 21-15 A5
2 21-16 A6
¬PCS 00
¬PCS 01
¬PCS 02
¬PCS 03
¬PCS 04
¬PCS 05
¬PCS 06
¬PCS 07
14
22
17
25
27
32
32
15
75
8259A-2
82-15 ¬PCS 00
15 93-3 ¬IORD
15 93-6 ¬IOWR
2 21-5 A1
1 63-42 ¬INTA 0
2,12 2D0-7
CS
RD
WR
A0
INTA
D0
D1
D2
D3
D4
D5
D6
D7
23 119-39 ED INT
17 113-5 KB INT
22 154-14 SCS/INT
18 121-13 RTC INT
8 68-56 CRT INT
31 J6-43 NET INT
32 J7-31 I/O INT1
134-12 PPRINT
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
INT
INT 0
1
CAS 0
CAS 1
CAS 2
SP/EN
R29
1K
+5V
AGA
83.10.31

Signal	Description
DRQ SEL 0-5	Selector bits for selecting DMA channel users. DRQ SEL 0-2 select the user device for DMA channel 0 DRQ SEL 3-5 select the user device for DMA channel 1
SCSIRSTOUT SCSIATN SCSISEL	These are control signals to be transmitted on the SCSI bus
SCSI EXP I/O	Indicates expected direction of SCSI-datatransfer
-ASYNC SEL	Selector for clock input to 8274 channel A.
-GRAPHIC	CRT mode selector.
KBON	Power on control for the keyboard.
ARDY	Is the request signal to the processor for insertion of wait state.
-IOWR -IORD	Write and Read signal generated by I/O instructions.
BUS 2 SELCT	When active, 2D 0-7 are used for I/O transfer (A MOS device is addressed).
1D 0-7	Connection of the configuration sense port to the 1D Bus.

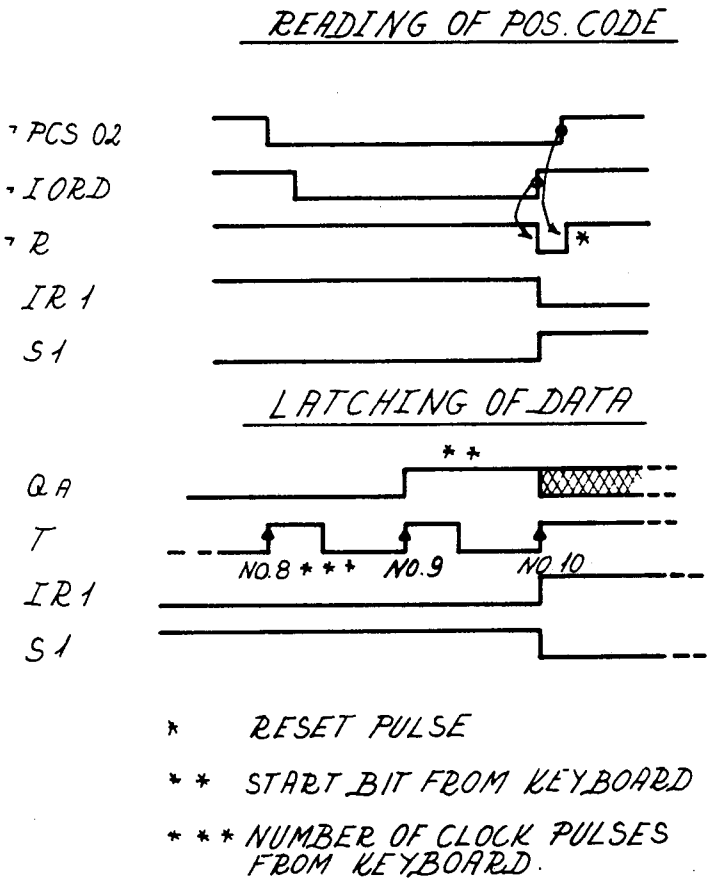

95
8255A-5
1 63-57 RESET
14 82-7 ↑PCS07
1 93-5 ↑IORD
1 93-6 ↑IOWR
2 21-5 A1
2 21-6 A2
2DO-7
RESET
CS
RD
WR
A0
A1
D0
D1
D2
D3
D4
D5
D6
D7
PA0 DRQ SEL 0 14
PA1 1 14
PA2 2 14
PA3 3 14
PA4 4 14
PA5 5 14
PA6 NVMA0 21
PA7 NVMA1 21
PC0 SCS/RST OUT 22
PC1 SCS/ATN 22
PC2 SCS/EXP I/O 22
PC3 SCS/SEL 22
PC4 ↑ASYNC SEL 27
PC5 DRQPRIOR 4
PC6 ↑GRAPHIC 9
PC7 KBON 16
FCO 19-029
22 115-11 SCS/RST IN
22 115-12 SCS/MSG
22 154-12 SCS/I/O
22 115-3 SCS/BSY
22 115-6 SCS/C/D
13 J1-18 MONOCROME
J1-17 22 KHz
J4-11
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
R47
R78
+5V
116
74LS 14
GRAPIC
6 24-19 MEMRDY
20 102-8 SOGERDY
74LS 11
41
ARDY 1
2 23-15 S2
1 63-62 ↑RD
74S 32
93
↑IORD
1 63-63 ↑WR
↑IOWR
1 63-42 ↑INTA 0
1 63-41 ↑INTA 1
14 82-15 ↑PCS00
14 82-12 ↑PCS03
14 82-11 ↑PCS04
14 82-7 ↑PCS07
1 63-27 ↑PCS1
3 76-15 ↑PCS40
74LS 30
83
BUS 2 SELECT 2
1DO-7
AGA 83.10.31
32 J7-22 ↑IO IDENT 0
32 J7-23 ↑IO IDENT 1
32 J7-24 ↑IO IDENT 2
32 J7-25 ↑IO IDENT 3
74LS244
10
1D0
1D4
+5V
R 58
31 J6-38 ↑NET IDENT
18 P39-1 ↑RTC SEC SOURCE
J8-47 ↑MEM IDENT 0
J8-48 ↑MEM IDENT 1
1K
93-3 ↑IORD
23 76-13 ↑PCS42
74S 32
FCO 19-028

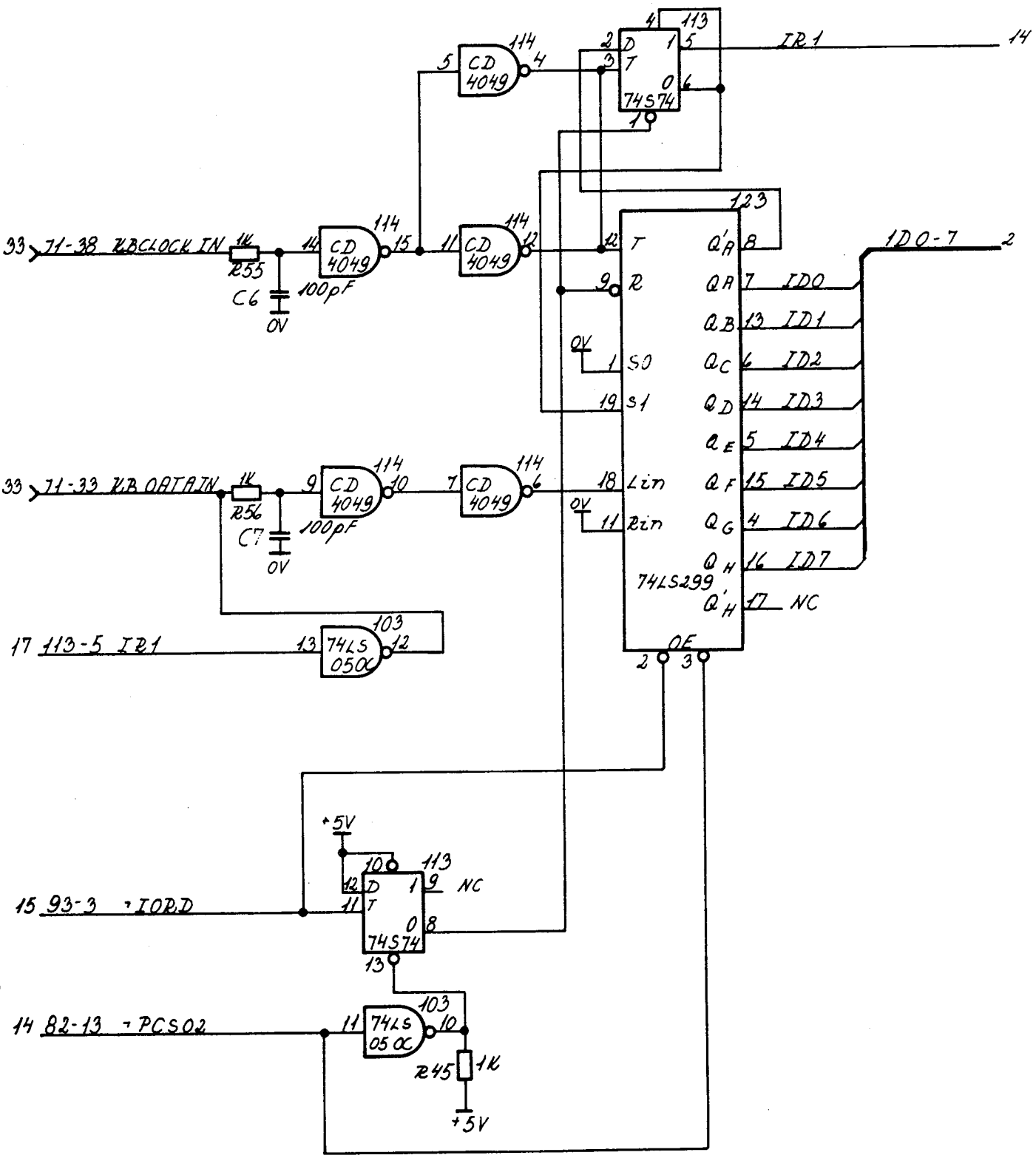
Signal	Description
KB POW	Power supply to keyboard. When the keyboard is connected the voltage on this line is 8-10 V.
KB ON	Turnes on the keyboard.


+12V
R71
22Ω
1W
R72
22Ω
1W
D8
BZY
88-C6V2
R77
1,5K
Q2
BD 136
R76
300Ω
Q1
15 95-10
K.BON
R74
730
2N2222A
K.B POW 28 J1-24,36
R73
10K
0V
0V

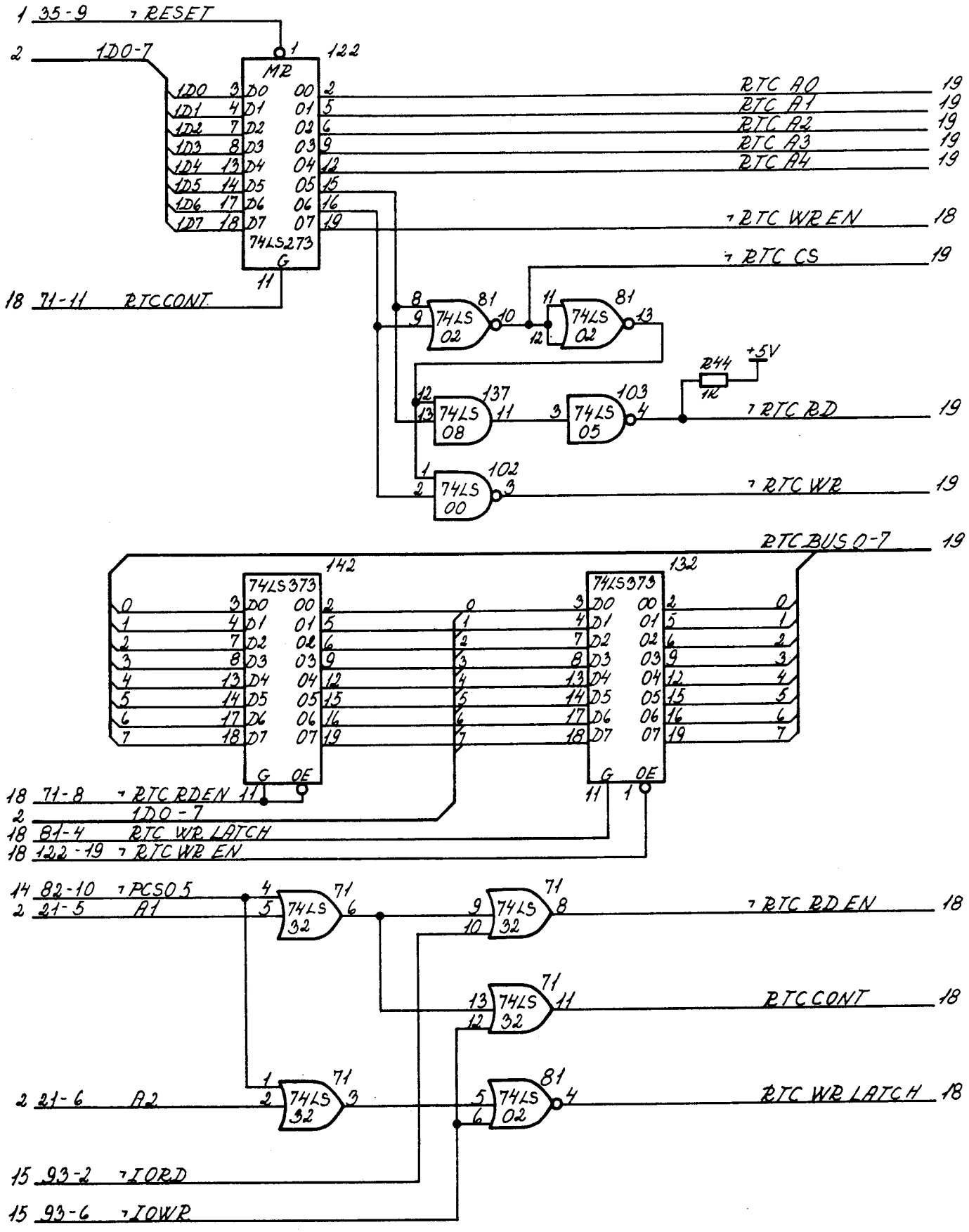
AGA
83.11.01

Signal	Description
KB CLOCK IN	This signal is the clock information supplied by the keyboard.
KB DATA IN	This signal is the data information supplied by the keyboard.
IR1	This interrupt request is asserted when a character is received. It is deasserted when the character is read.




33 71-38 KBCLOCK IN
R55 1K
C6 100pF
0V
CD 4049
114
113
74S74
IR1
14
123
74LS299
IDO-7
2
IDO
ID1
ID2
ID3
ID4
ID5
ID6
ID7
NC
33 71-33 KB DATAIN
R56 1K
C7 100pF
17 113-5 IR1
74LS 05OC
103
+5V
15 93-3 -IORD
14 82-13 -PCS02
R45 1K
AGA 83.11.01

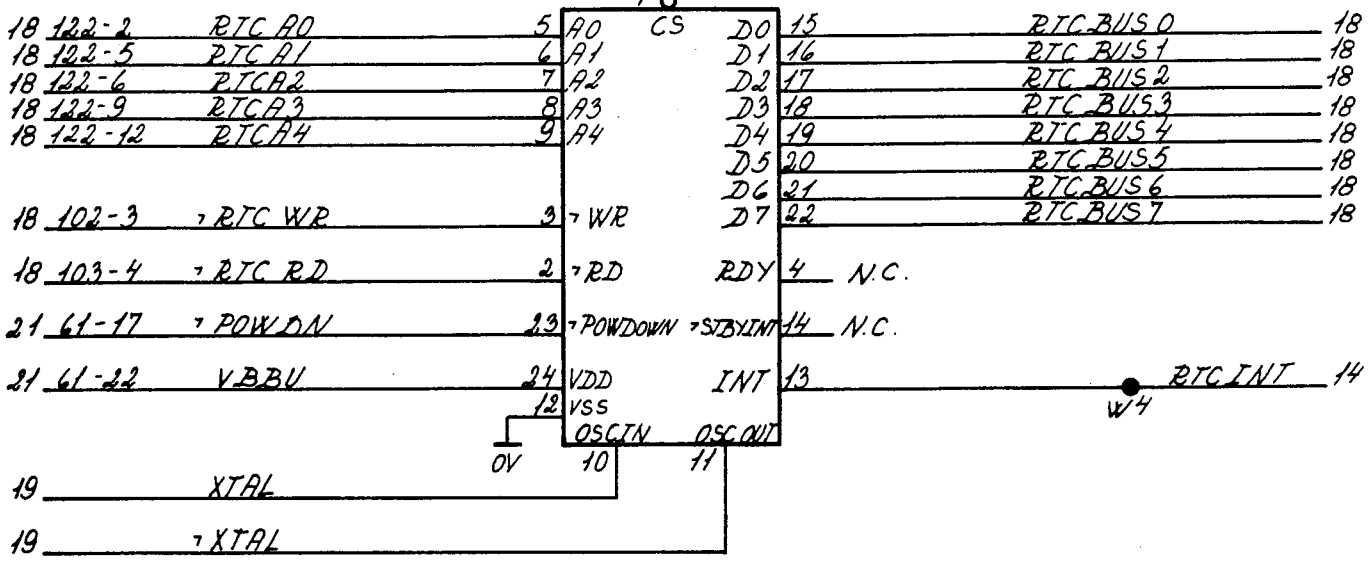
Signal	Description
RTC CONT	Latches the control information passed to the Real Time Clock (RTC).
-RTC RD EN	Enables data output from RTC.
-RTC WR EN	Enables data input to RTC.
RTC WR LATCH	Latches data input to RTC.
RCT A0-4	Address information transferred to the CRT.
-RTC RD	Read signal used to control the RTC.
-RTC WR	Write signal used to control the RTC.
-RTC CS	Chip select signal used to control the RTC.
RTC BUS 0-7	Local data bus used by the RTC and the sound generator.


1 35-9 ~RESET
2 1DO-7
MR
74LS273
RTC A0
RTC A1
RTC A2
RTC A3
RTC A4
~RTC WR EN
~RTC CS
18 71-11 RTCCONT
74LS 02
74LS 08
74LS 05
74LS 00
R44
1K
+5V
~RTC RD
~RTC WR
RTC BUS 0-7
74LS373
18 71-8 ~RTC RDEN
2 1DO-7
18 81-4 RTC WR LATCH
18 122-19 ~RTC WR EN
14 82-10 ~PCSO 5
2 21-5 A1
74LS 32
~RTC RD EN
RTCCONT
2 21-6 A2
RTC WR LATCH
15 93-2 ~IORD
15 93-6 ~IOWR

Signal	Description
VBBU	Battery supported power supply.
-POWDN	Indicates the power down condition.

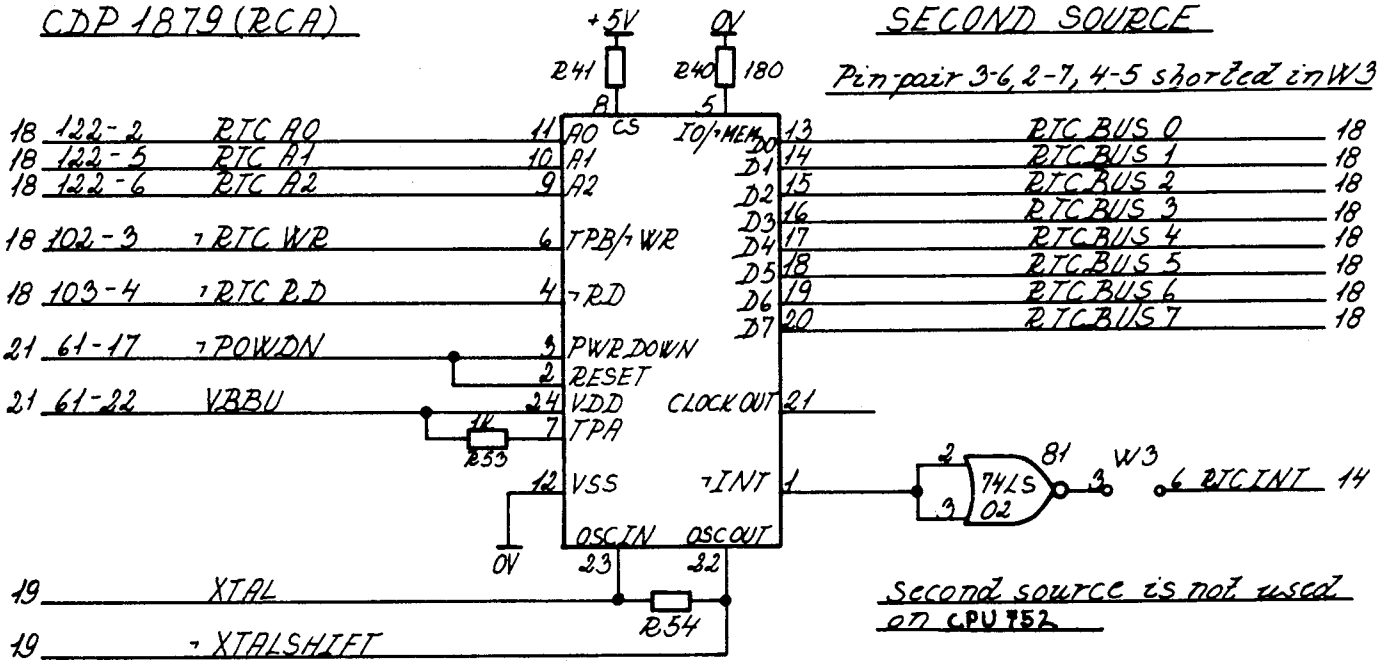
MM58167 (NSC) — FIRST SOURCE

No pin-pairs shorted in W3

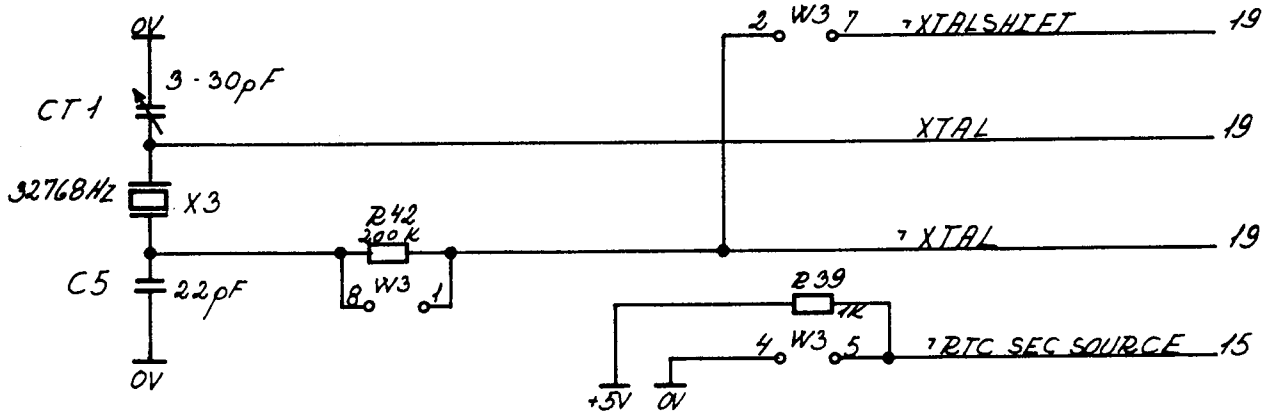


CDP 1879 (RCA) — SECOND SOURCE

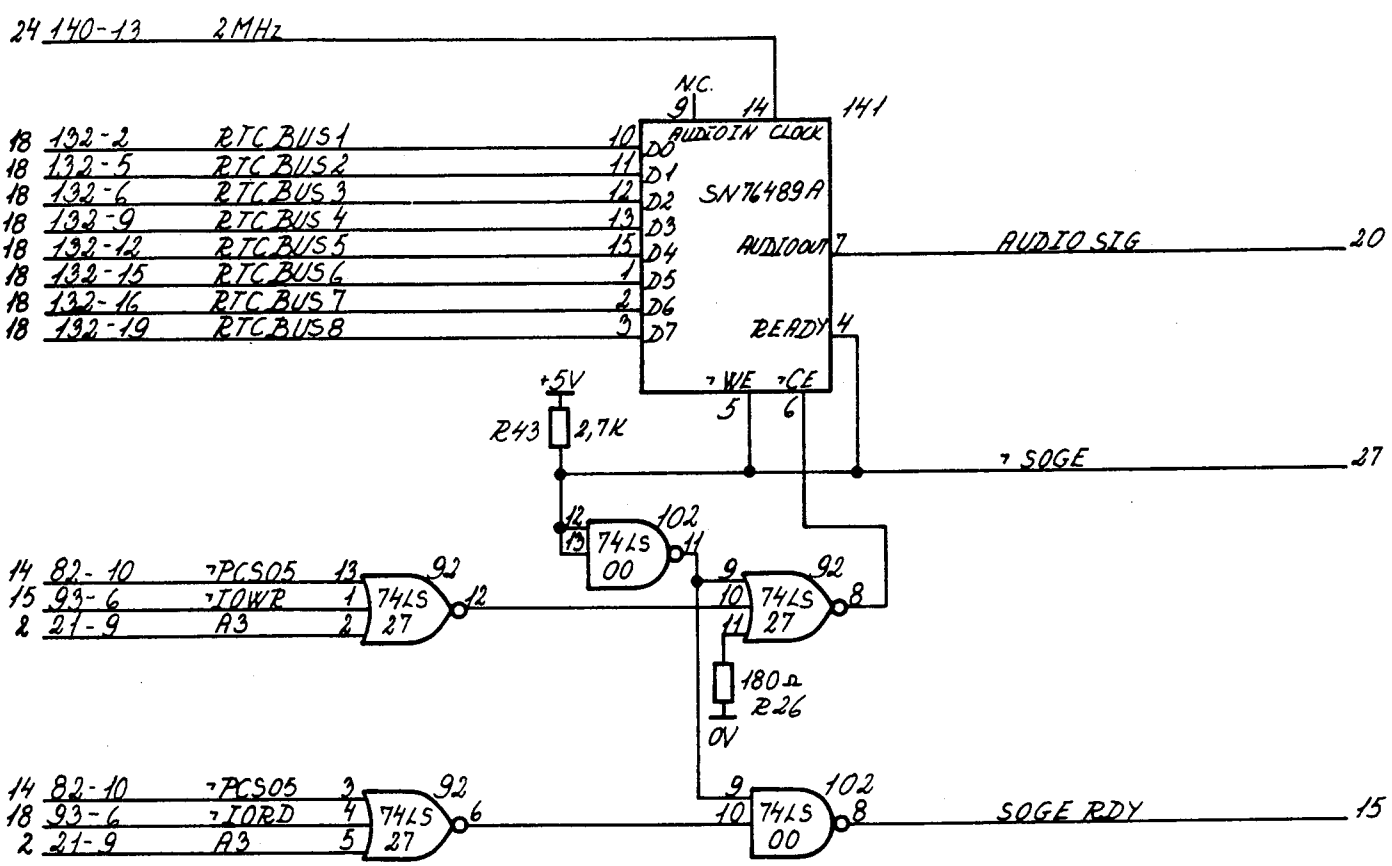
Pin pair 3-6, 2-7, 4-5 shorted in W3

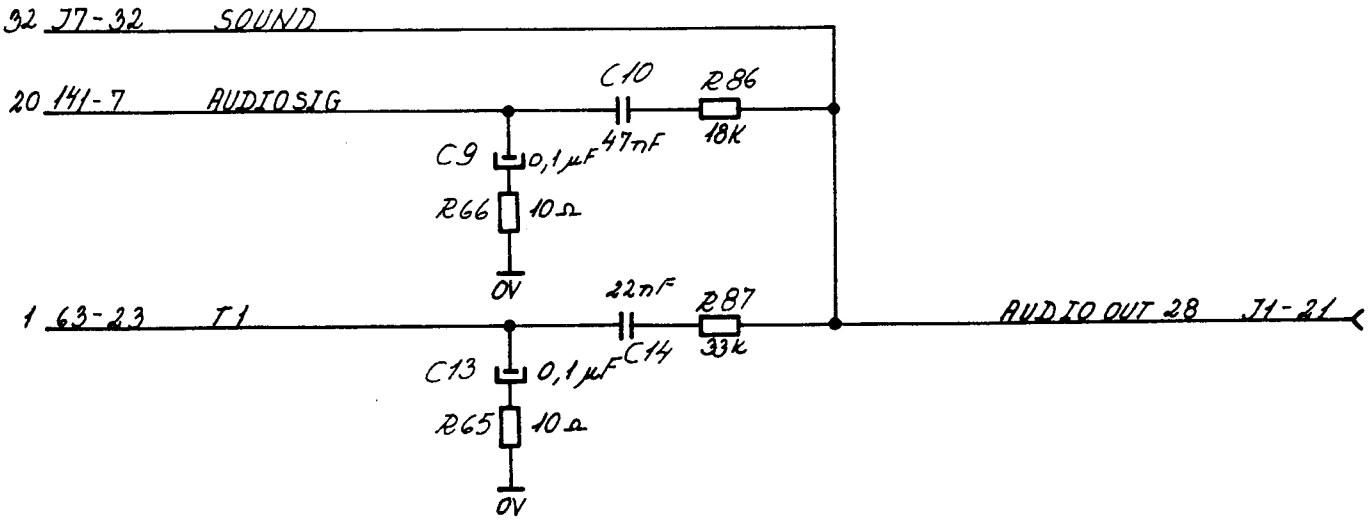


Second source is not used on CPU 752



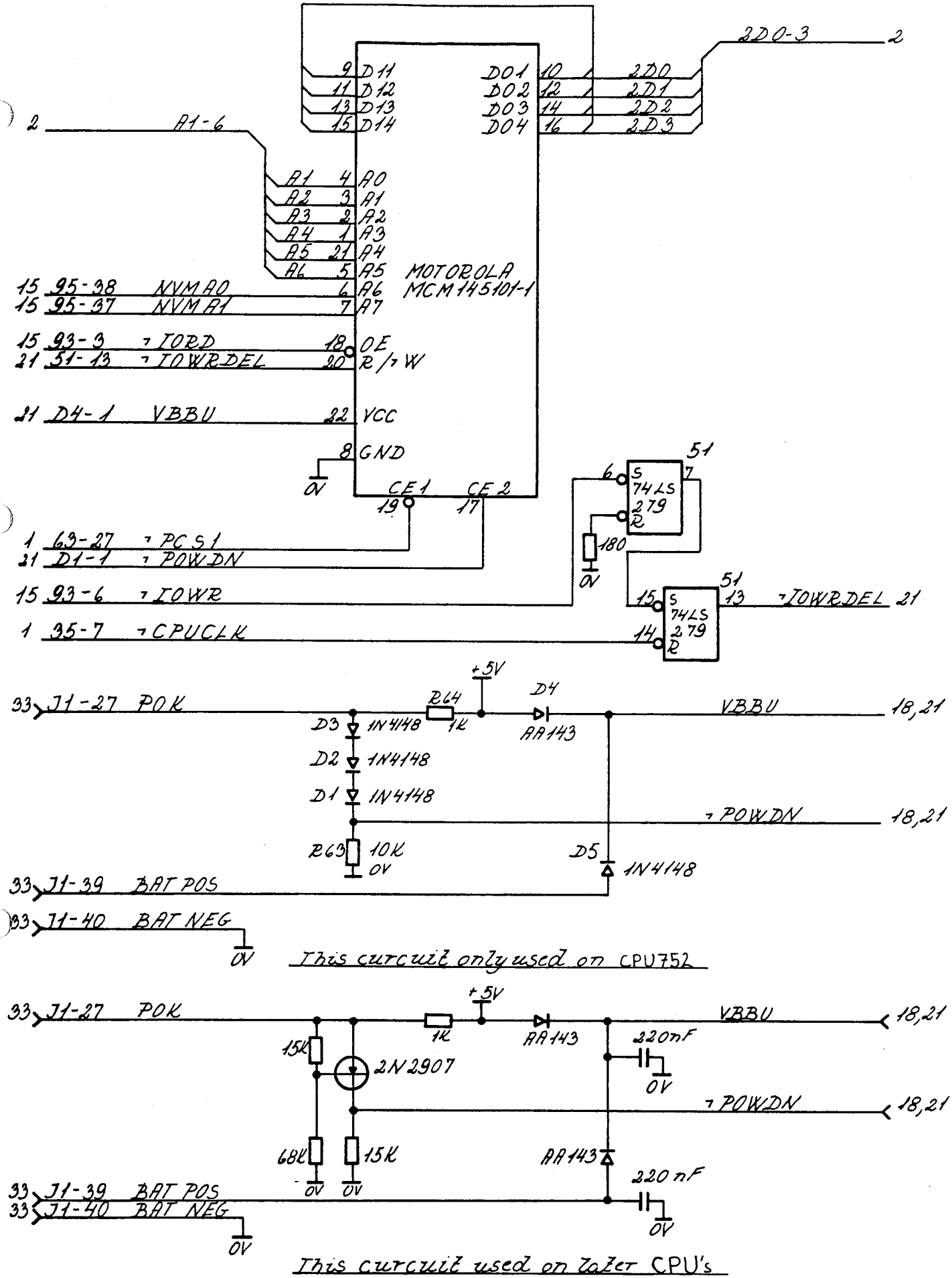
Signal	Description
RTC BUS 0-7	Local databus used by the RTC and the sound generator.
-SOGE	Indicates the presence of the sound generator.
AUDIO SIG	Analog audio output.
SOGE RDY	Indicates the READY-condition of the sound generator.
AUDIO OUT	The analog mixed signal of T1 and AUDIO SIG.


24 140-13 2MHz
N.C.
9
14
141
AUDIOIN CLOCK
SN76489A
18 132-2 RTC BUS1
18 132-5 RTC BUS2
18 132-6 RTC BUS3
18 132-9 RTC BUS4
18 132-12 RTC BUS5
18 132-15 RTC BUS6
18 132-16 RTC BUS7
18 132-19 RTC BUS8
10 D0
11 D1
12 D2
13 D3
15 D4
1 D5
2 D6
3 D7
AUDIOOUT 7
AUDIO SIG 20
READY 4
¬WE 5
¬CE 6
+5V
R43 2,7K
¬SOGE 27
102
74LS 00
92
74LS 27
14 82-10 ¬PCS05
15 93-6 ¬IOWR
2 21-9 A3
180Ω R26
0V
18 93-6 ¬IORD
SOGE RDY 15


92 J7-32 SOUND
20 141-7 AUDIOSIG
C10 47nF
R86 18K
C9 0,1µF
R66 10Ω
0V
1 63-23 T1
22nF
R87 33K
C14
C13 0,1µF
R65 10Ω
0V
AUDIO OUT 28 J1-21

RGA 89.11.01

Signal	Description
POK	Power OK-signal generated by the power supply.
VBBU	Battery supported power supply.
-POWDN	Indicates the power down condition.
-IOWRDEL	Delayed version of the -IOWR signal.
BAT POS	Back-up battery connection.
BAT NEG	OV.

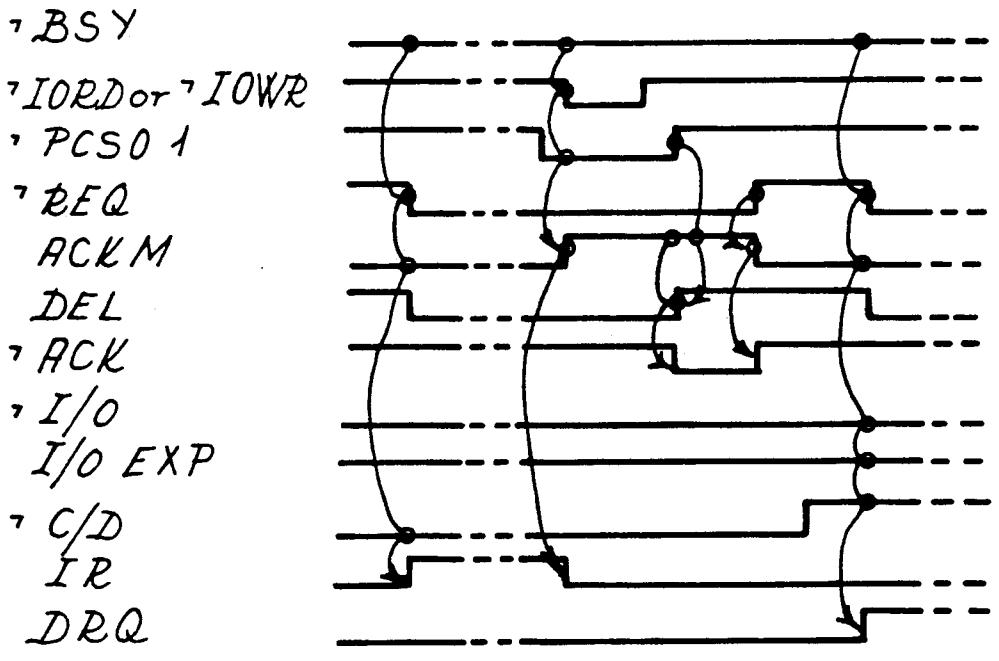


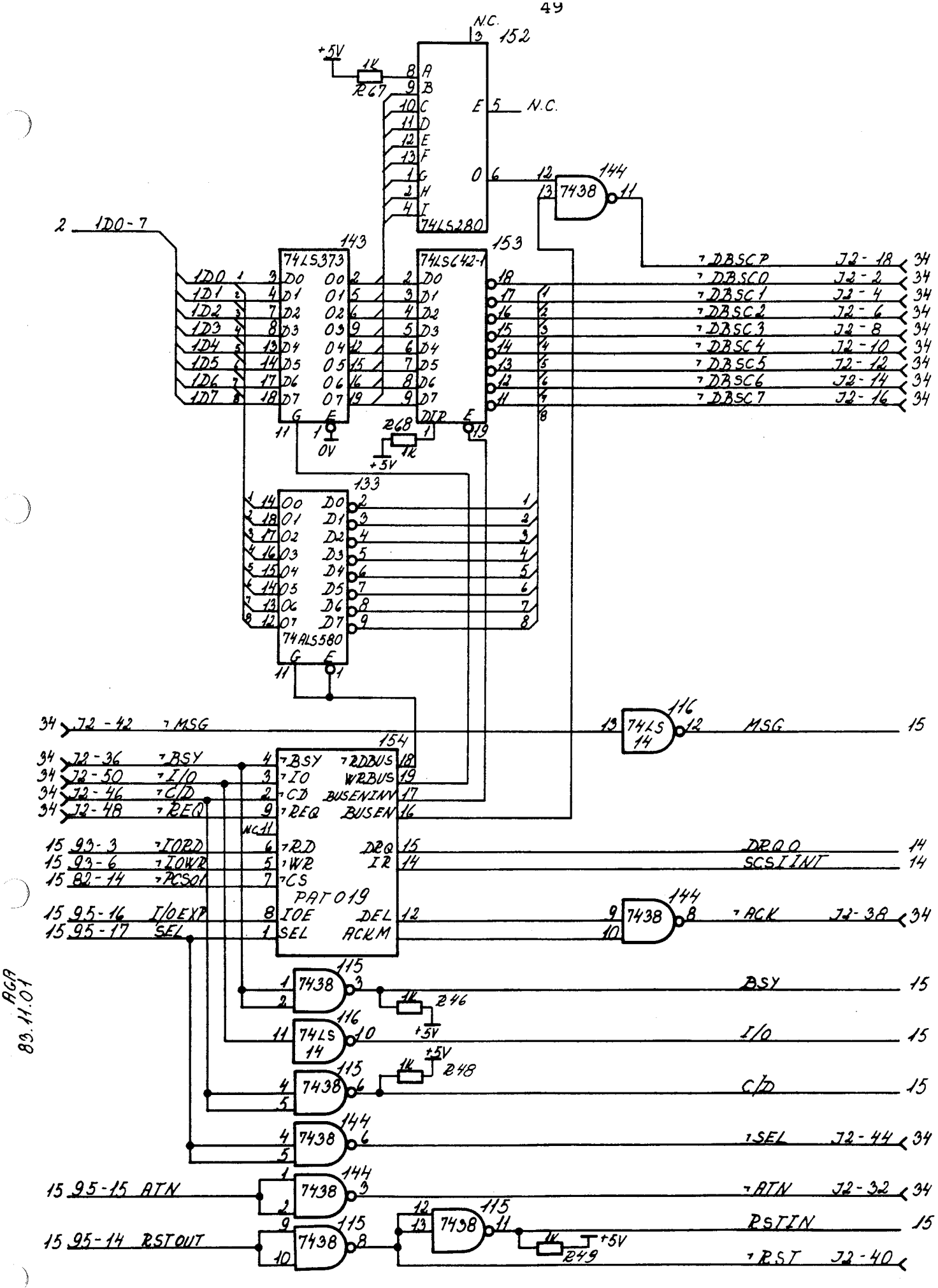
This curcuit only used on CPU752

This curcuit used on later CPU's

Signal	Description
-MSG	
-BSY	
-I/O	Input from the SCSI-device.
-C/D	
-REQ	
-ACK	
-ATN	Output to the SCSI-device.
-SEL	
DBSC 0-7	Bidirectional SCSI data bus.
DBSCP	Parity output to SCSI-device.
-RST	Bidirectional Reset Signal.

```
PAL16L8                          PAL DESIGN SPECIFIKATION
PAT0019                             THJ 830719
          SCSI SUPPORT CIRCUIT

SEL /CD /IO /BSY /WR /RD /CS IOE /REQ GND
NC DEL ACKM IR DRQ BUSEN BUSENINV /RDBUS WRBUS VCC

IF(VCC) /WRBUS   = /WR + /CS
IF(VCC)  RDBUS   =  RD*CS
IF(VCC) /BUSENINV = /IO
IF(VCC) /BUSEN   =  IO
IF(VCC) /DRQ     = /IO*IOE + /IOE*IO + /BSY + /REQ + CD + ACKM
IF(VCC) /IR      = /BSY + /REQ + IO*IOE*/CD + /IO*/IOE*/CD + ACKM
IF(VCC) /ACKM    = /WR*/RD*/ACKM + /BSY + /REQ + /CS*/ACKM
IF(VCC) /DEL     = REQ*/ACKM + REQ*CS

DESCRIPTION:
```




N.C.
152
+5V
1K
R67
74LS280
N.C.
144
7438
2 1D0-7
143
74LS373
153
74LSC42-1
DBSCP J2-18 34
DBSC0 J2-2 34
DBSC1 J2-4 34
DBSC2 J2-6 34
DBSC3 J2-8 34
DBSC4 J2-10 34
DBSC5 J2-12 34
DBSC6 J2-14 34
DBSC7 J2-16 34
R68
1K
0V
+5V
133
74ALS580
116
74LS 14
34 J2-42 MSG
MSG 15
154
34 J2-36 BSY
34 J2-50 I/O
34 J2-46 C/D
34 J2-48 REQ
15 93-3 IORD
15 93-6 IOWR
15 82-14 PCS01
15 95-16 I/OEXP
15 95-17 SEL
PAT019
2DBUS
WRBUS
BUSENINV
BUSEN
DRQ
IR
DEL
ACKM
DRQ0 14
SCSIINT 14
ACK J2-38 34
115
7438
R46
BSY 15
I/O 15
R48
C/D 15
SEL J2-44 34
15 95-15 ATN
ATN J2-32 34
15 95-14 RSTOUT
RSTIN 15
R49
RST J2-40
83.11.01 AGA
CPU752 SCSI/SASI INTERFACE 22

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