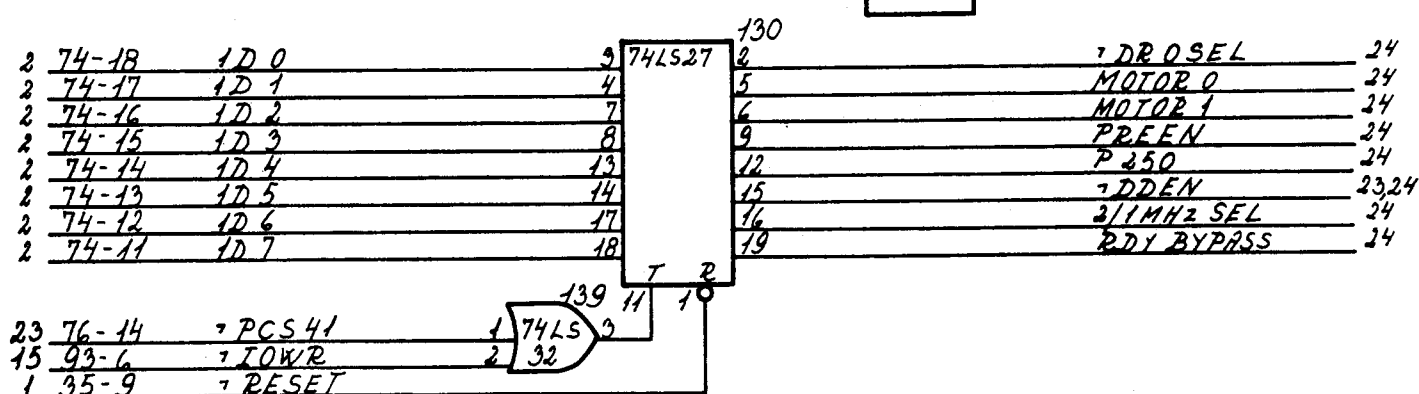
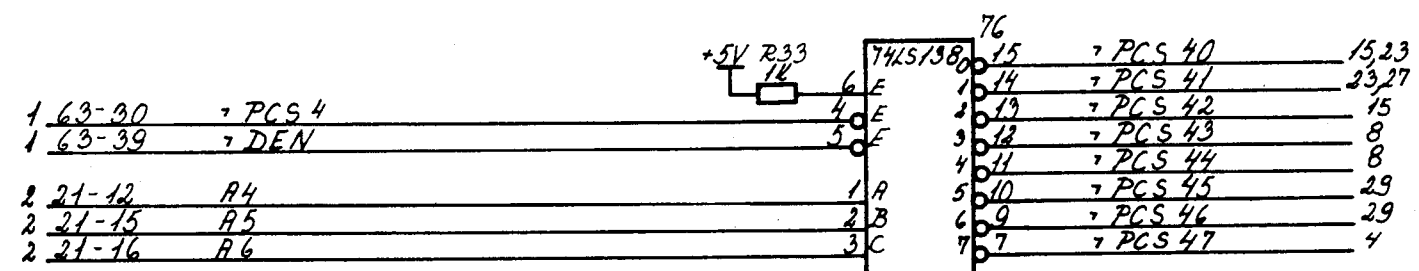
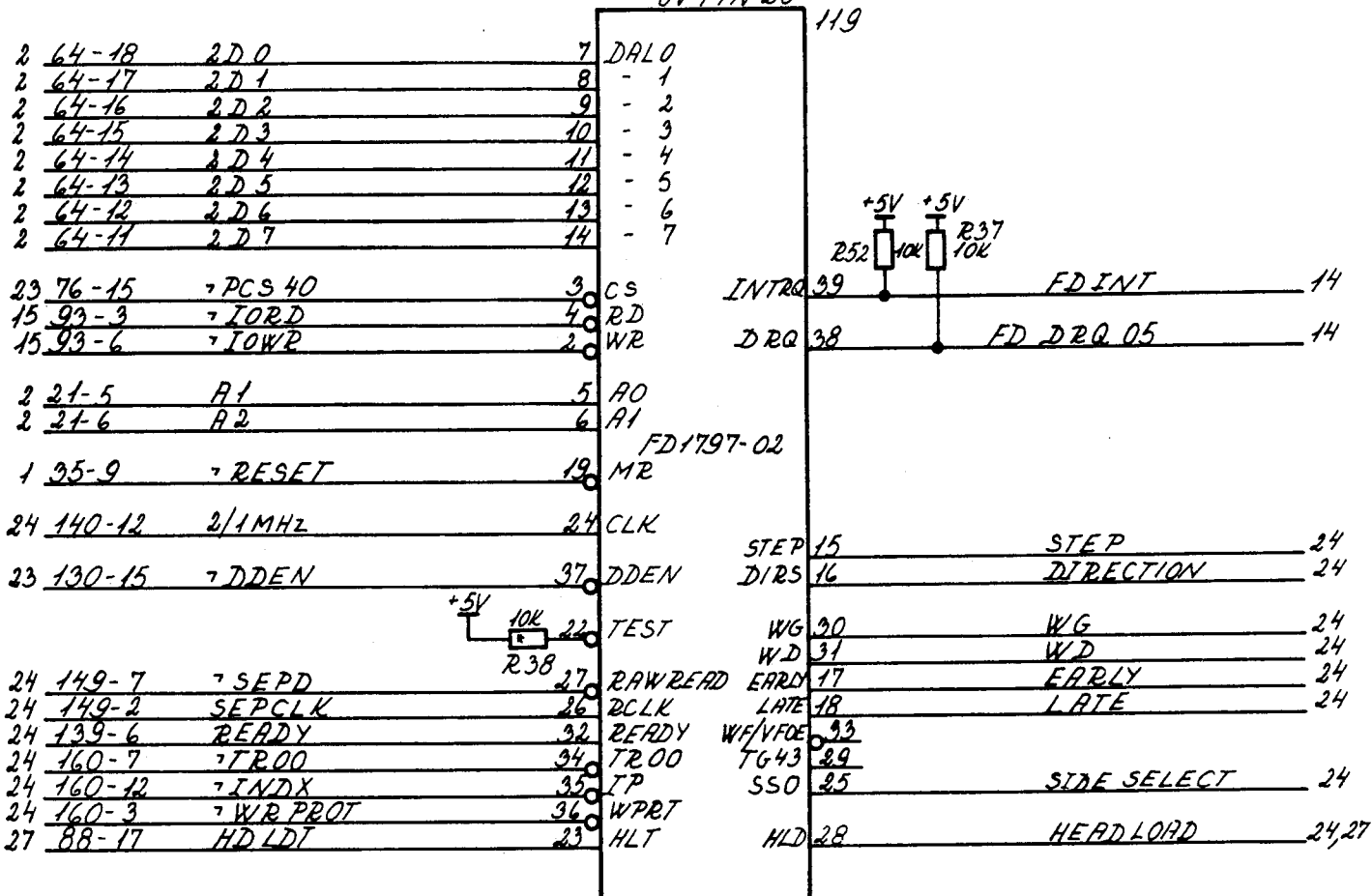


WD: FD 1797-02
SMC: FDC 1797-02

PCS 4: I/O BASE +200-27F

+5V PIN 21 ± 0.25V
+12V PIN 40 ± 0.6V
0V PIN 20



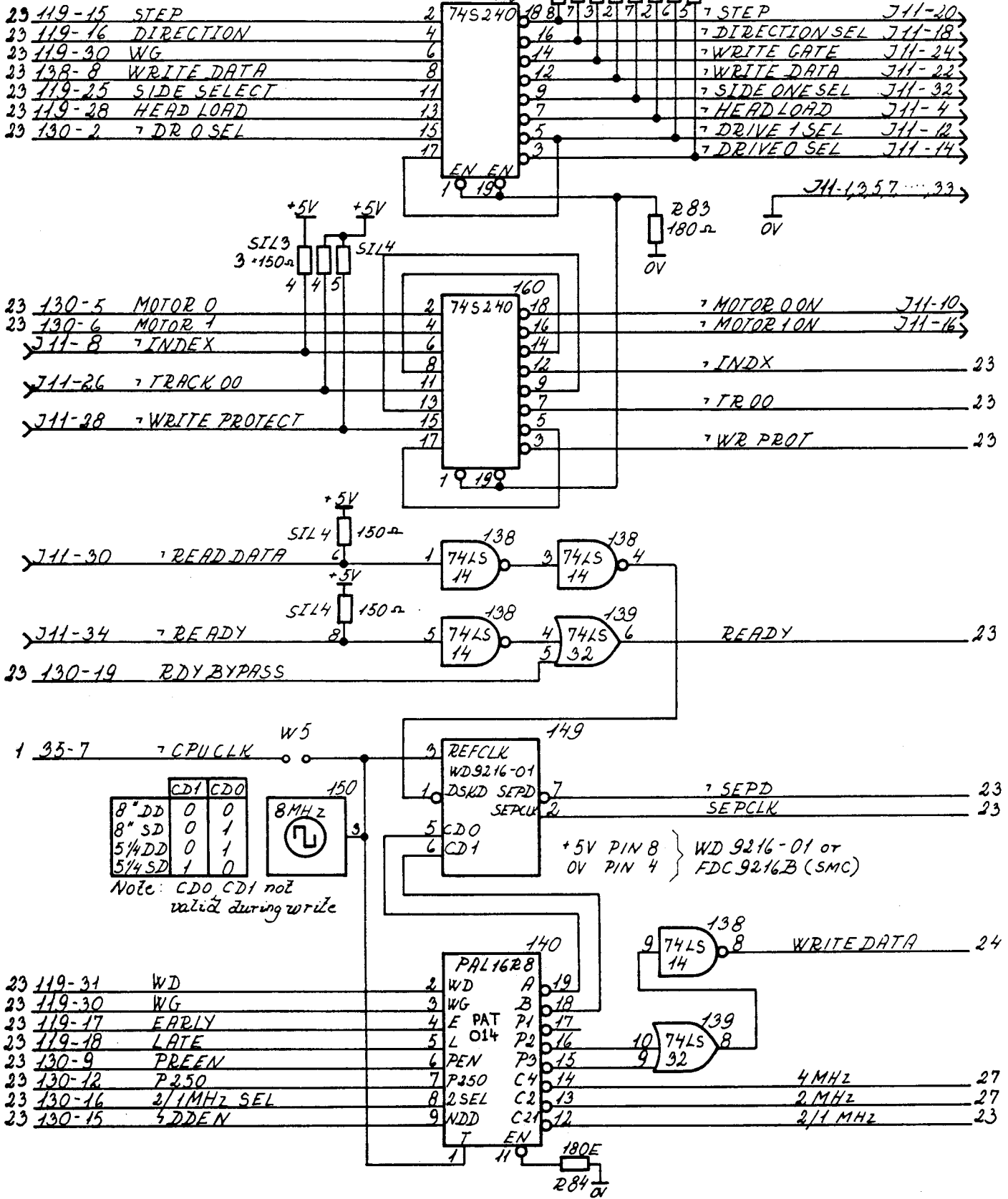
83.11.01

PAL16R8 PAL DESIGN SPECIFICATION
 PAT0014 83.08.03 JPJ
 FDD PRECOMP, CLOCK LOGIC, RC750

CK WD WG E L PEN P250 2SEL NDD GND
 /E /C21 /C2 /C4 /P3 /P2 /P1 /B /A VCC

A := 2SEL*/NDD*/WG + /2SEL*NDD*/WG + WG*WD
 B := 2SEL*/WG + /2SEL*/NDD*/WG + WG*A
 P1 := L*A*/B*PEN*WG*/P1*/P2*/P3 +
 WG*P1*/P2*P3 + WG*P2*/P3 +
 E*A*/B*PEN*WG*/P1*/P2*/P3
 P2 := WG*P1*/P2*/P3 +
 A*/B*/P1*/P2*/P3*WG*/PEN +
 A*/B*/P1*/P2*/P3*WG*/E*/L*PEN +
 WG*/P1*P2*/P3 +
 E*A*/B*PEN*WG*/P1*/P2*/P3 + WG*P1*P2
 P3 := /WG + L*P250*A*/B*PEN*WG*/P1*/P2*/P3 +
 WG*P1*P2*/P3 +
 E*P250*A*/B*PEN*WG*/P1*/P2*/P3 +
 WG*P1*P2*P3
 C4 := /C4
 C2 := C4*/C2 + /C4*C2
 C21 := 2SEL*C2 + /2SEL*/C21*C2*C4 +
 /2SEL*C21*C2*/C4 + /2SEL*C21*/C2

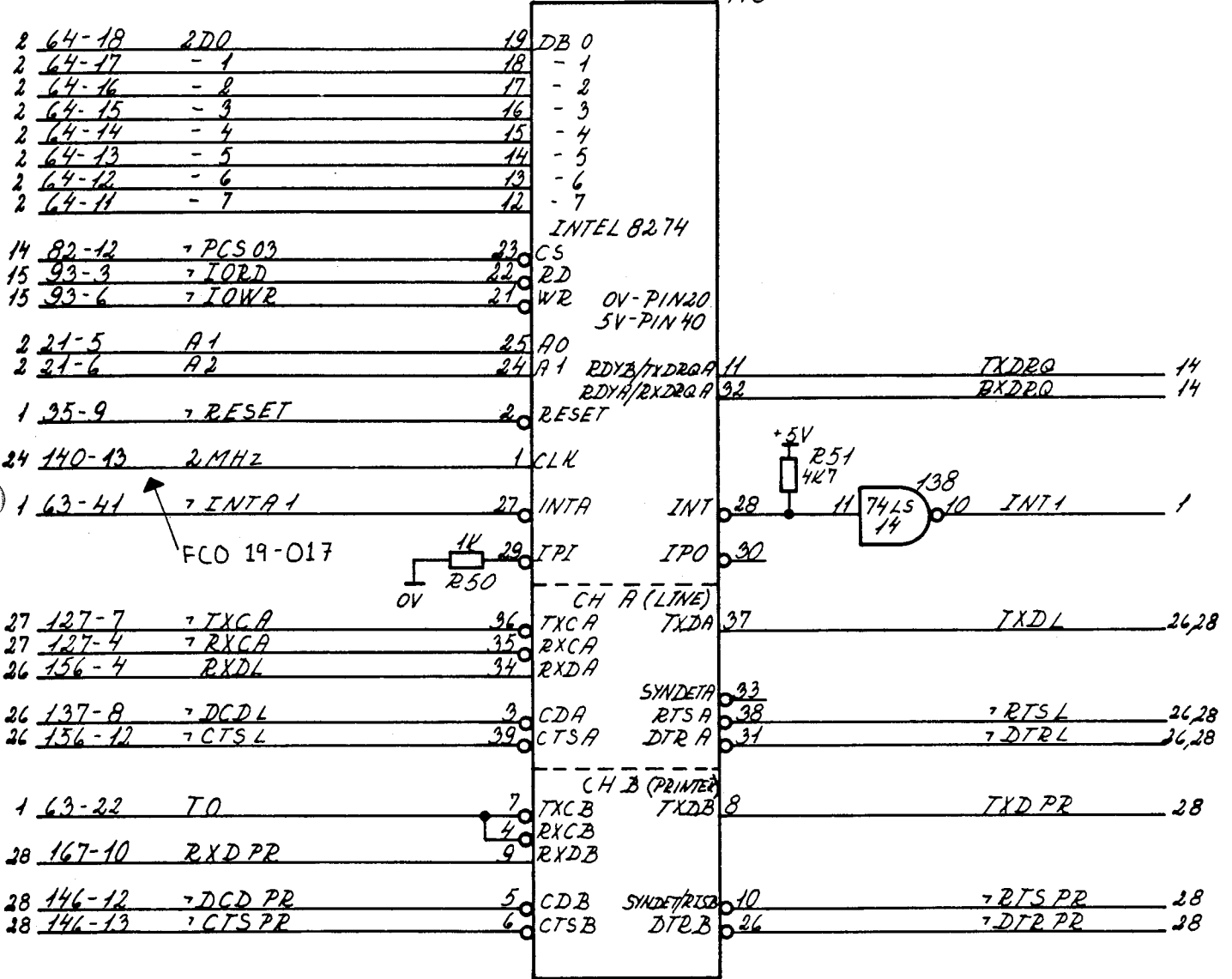
DESCRIPTION:



83.11.01

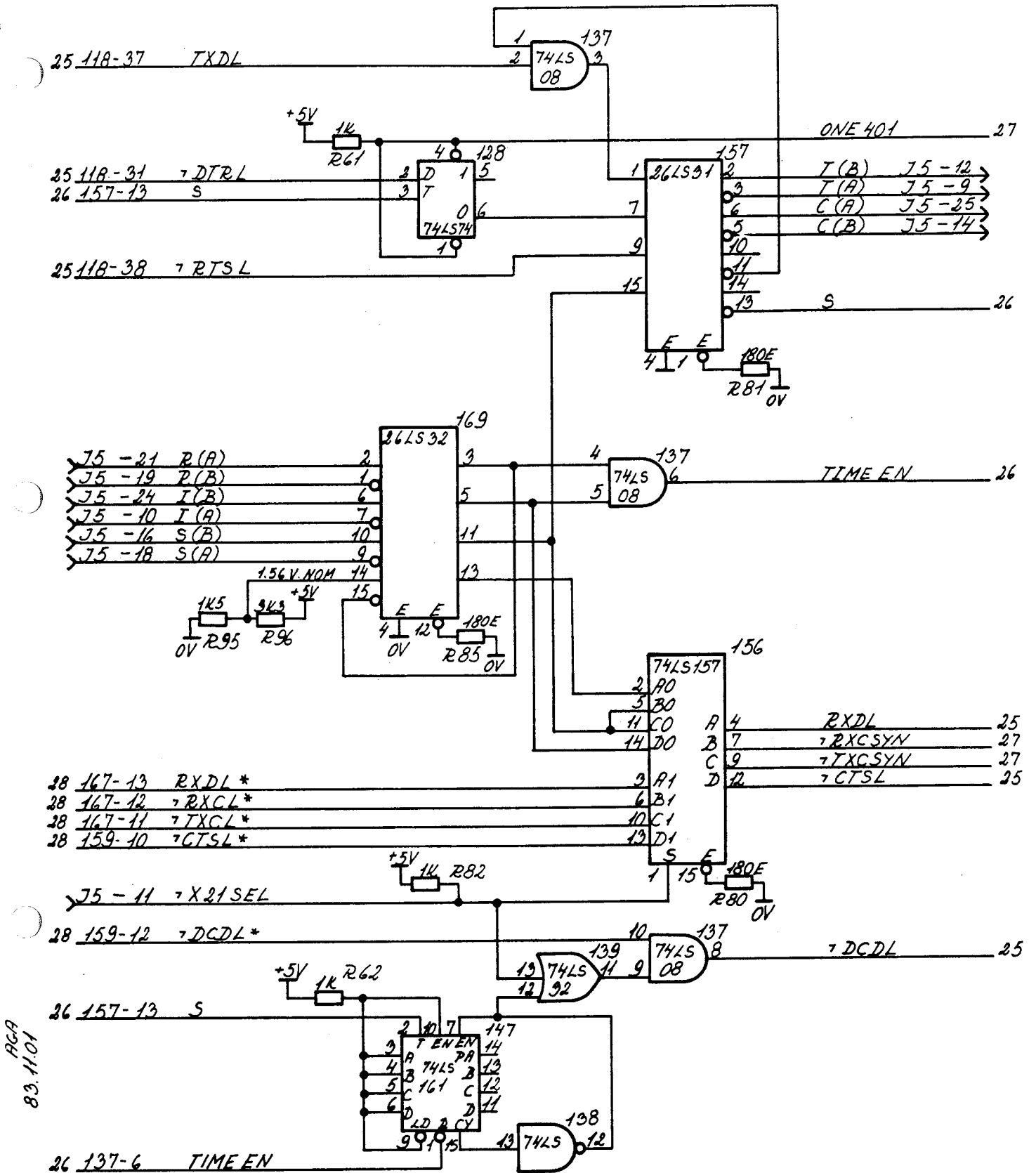
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118



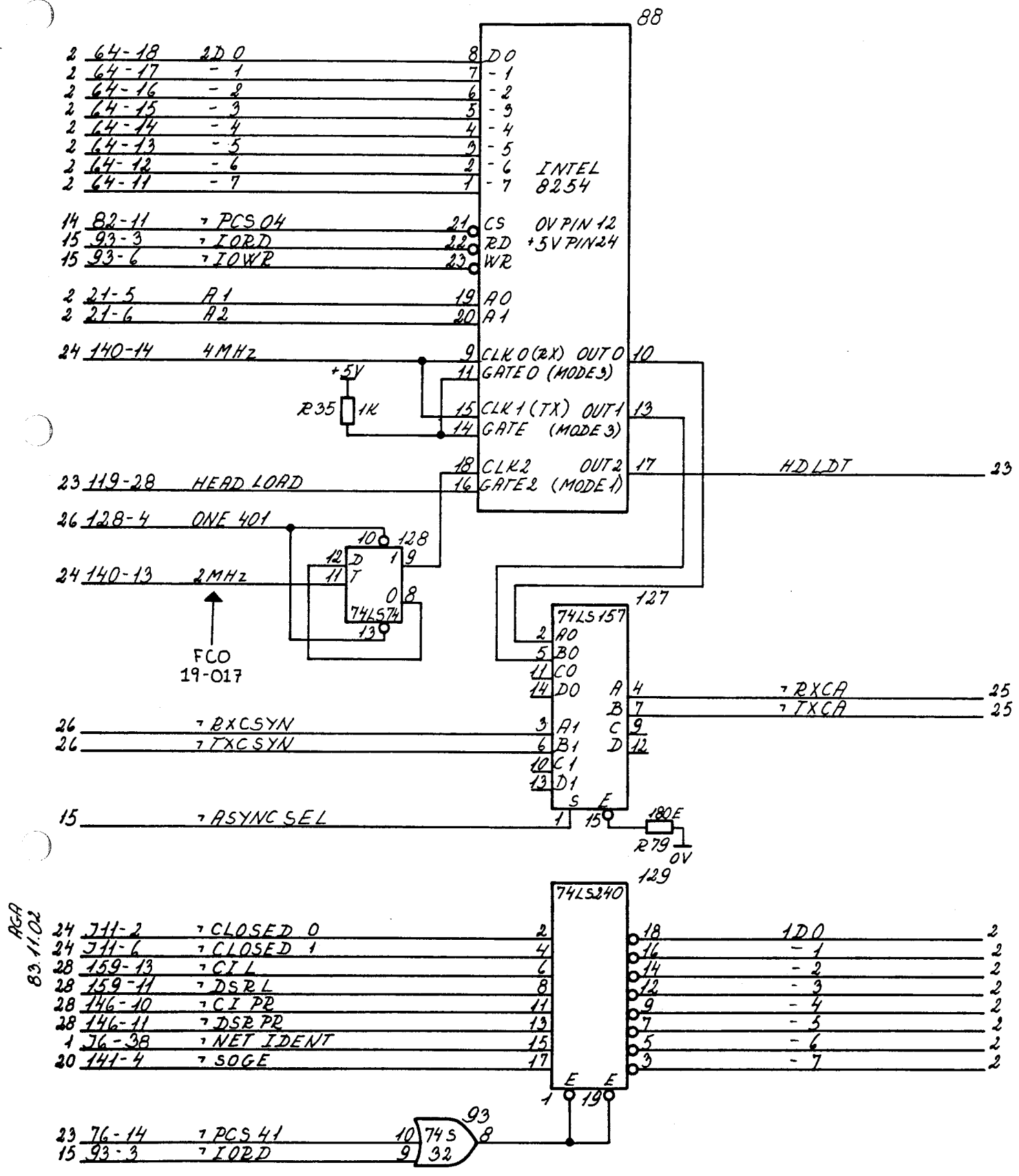
AGA
83.11.02

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AGA
83.1101

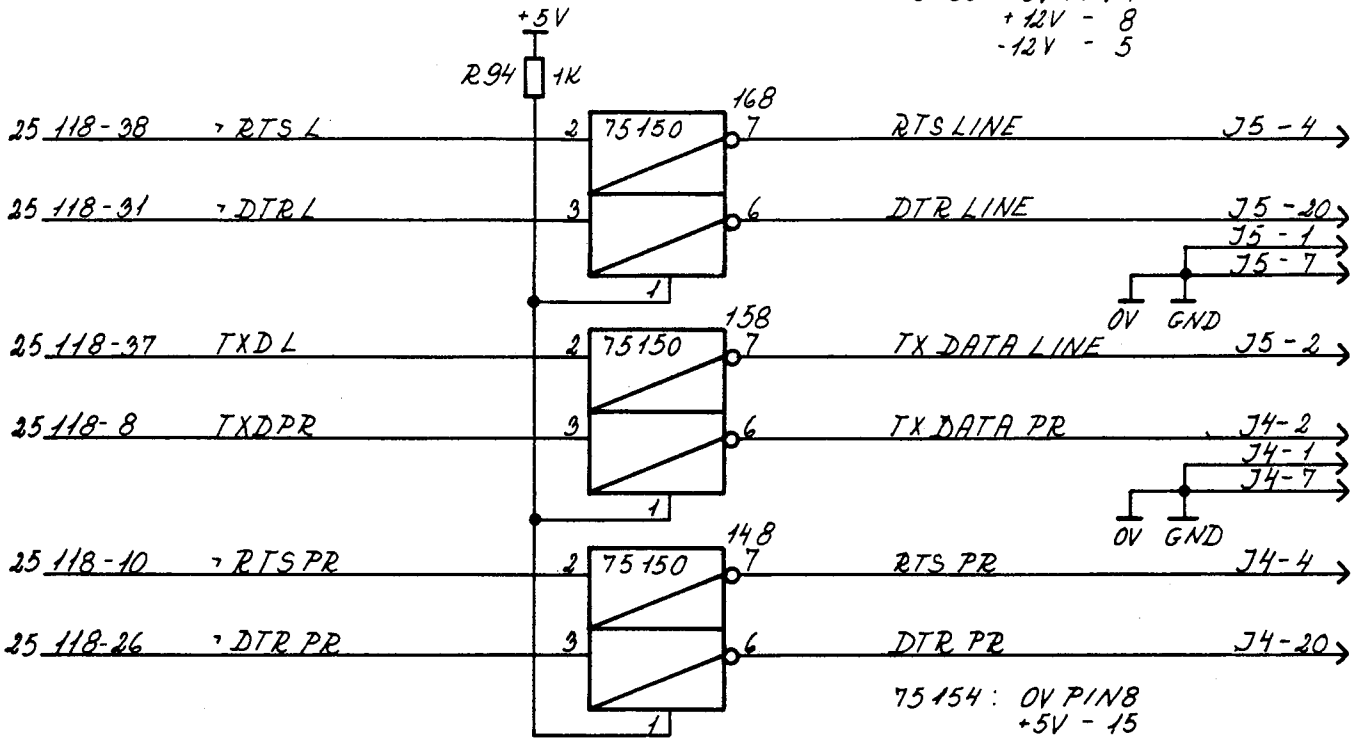
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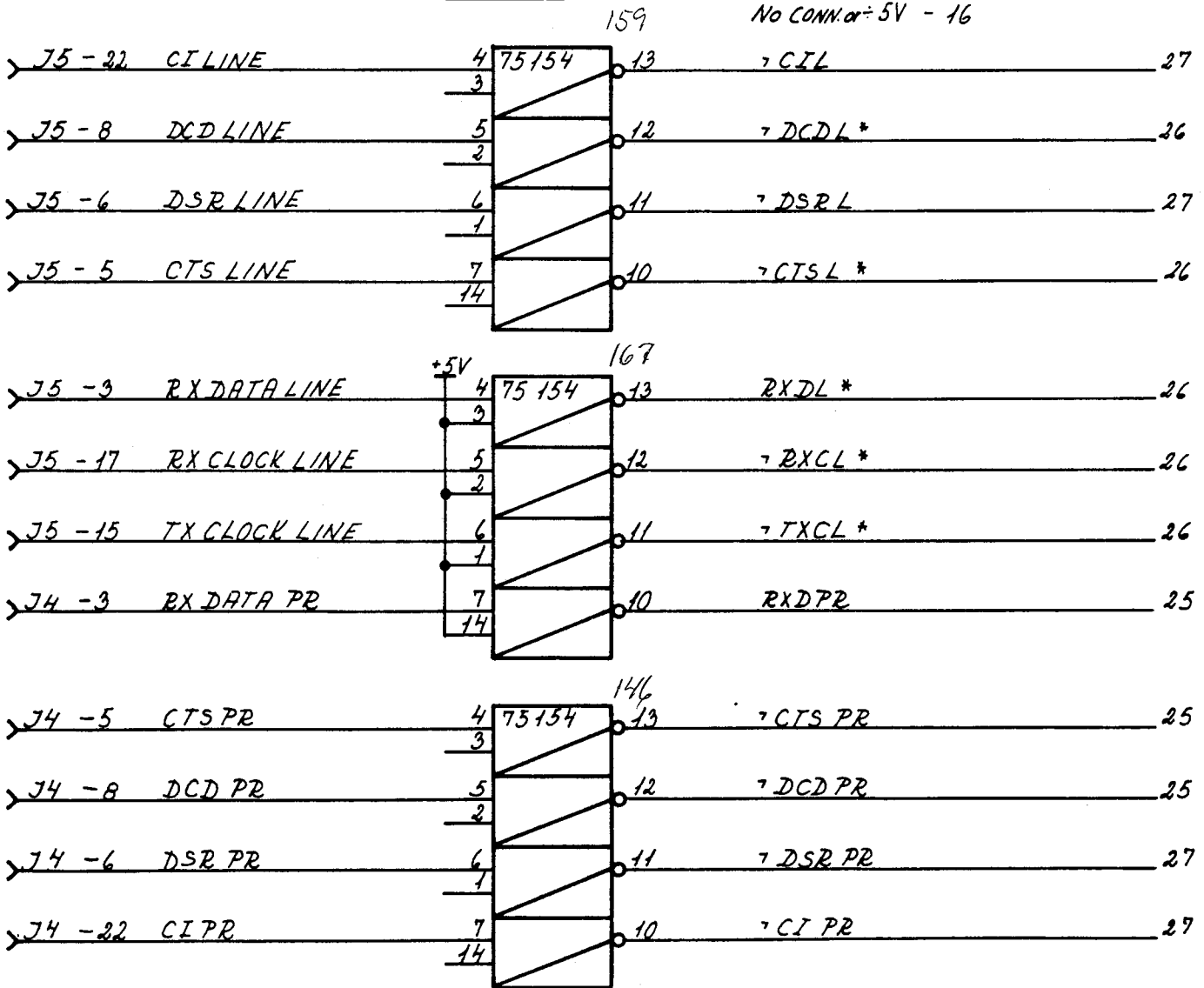
AGA
83.11.02

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75150: 0V PIN 4
+12V - 8
-12V - 5

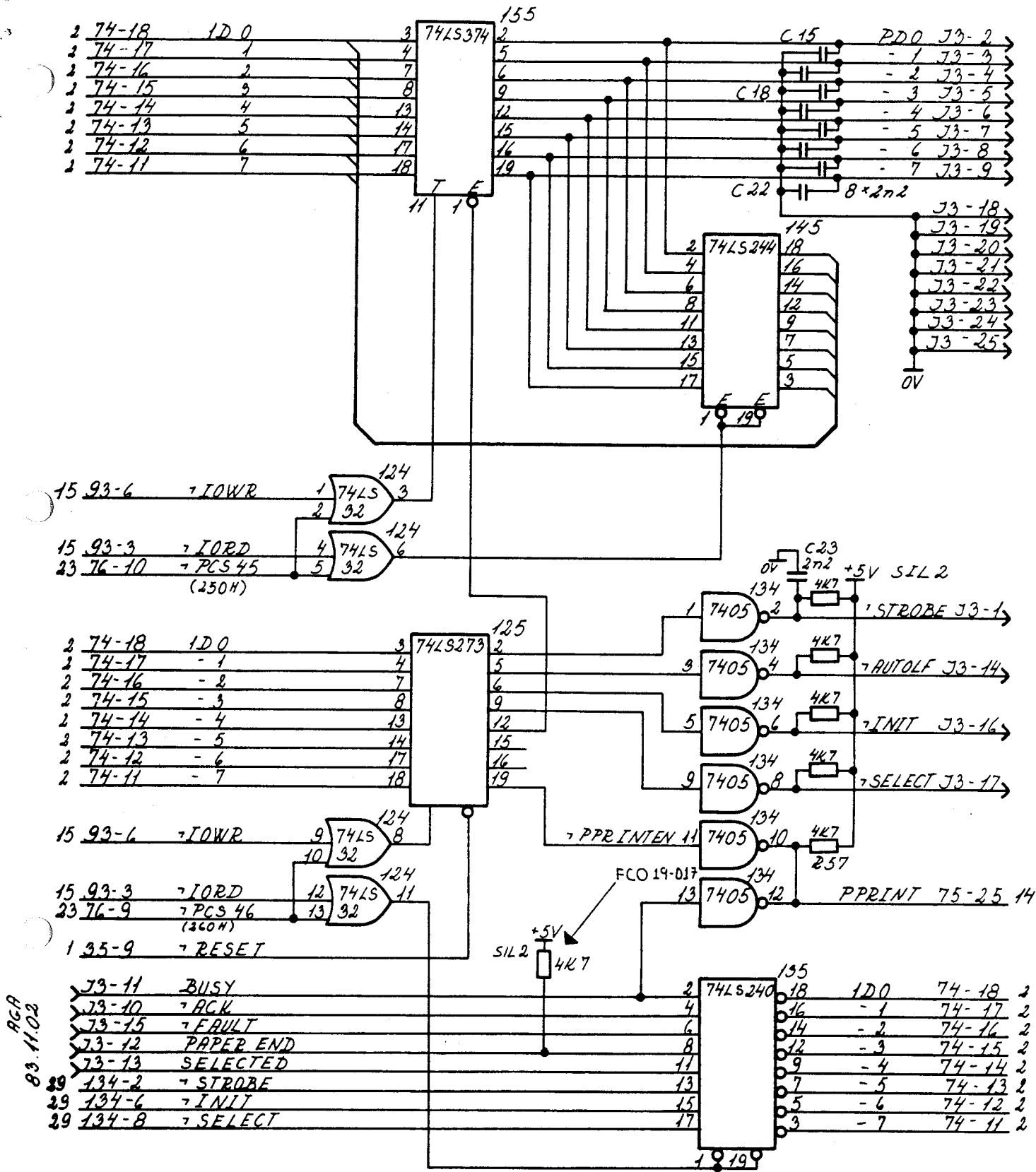


75154: 0V PIN 8
+5V - 15
No CONN. or -5V - 16



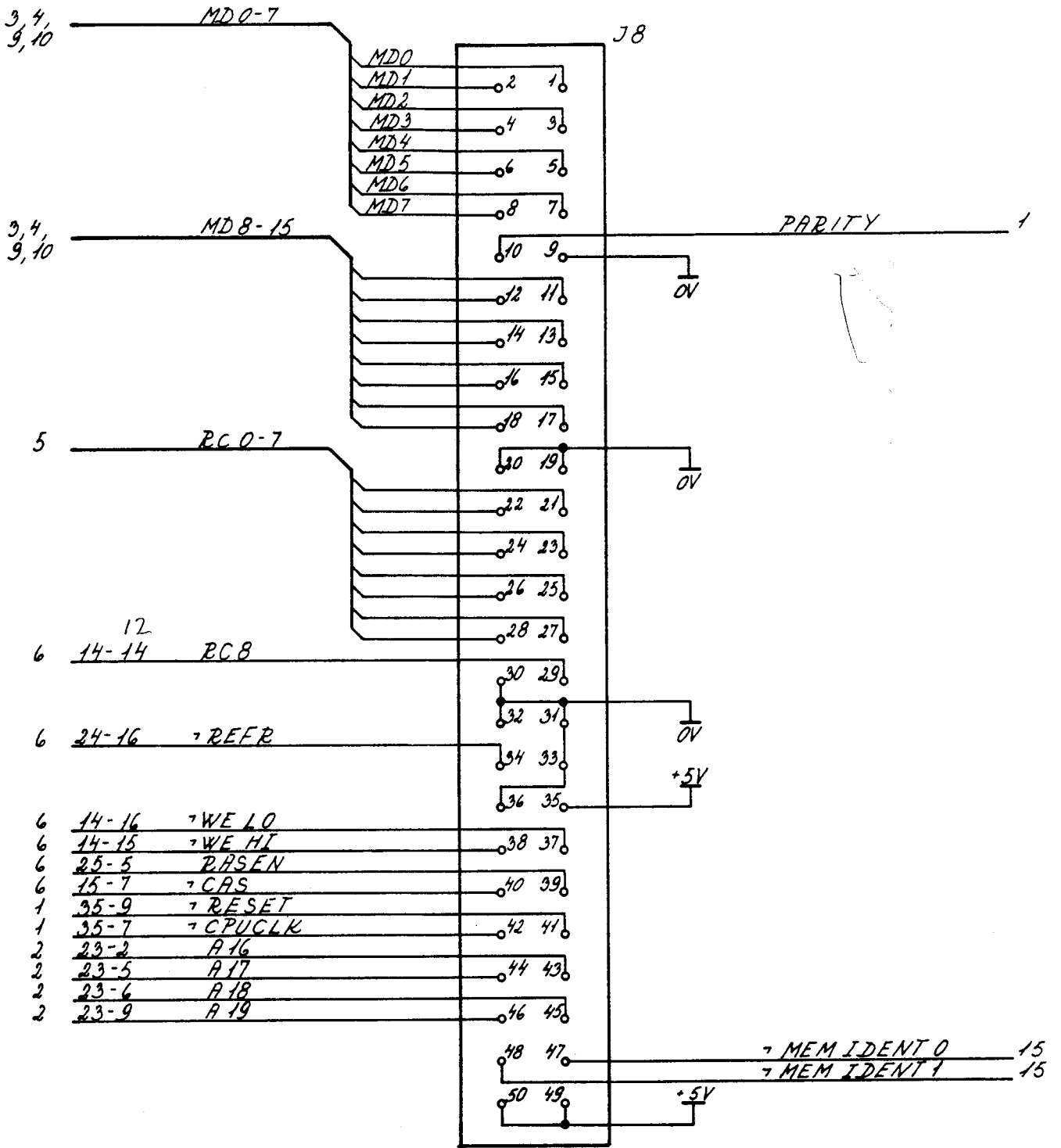
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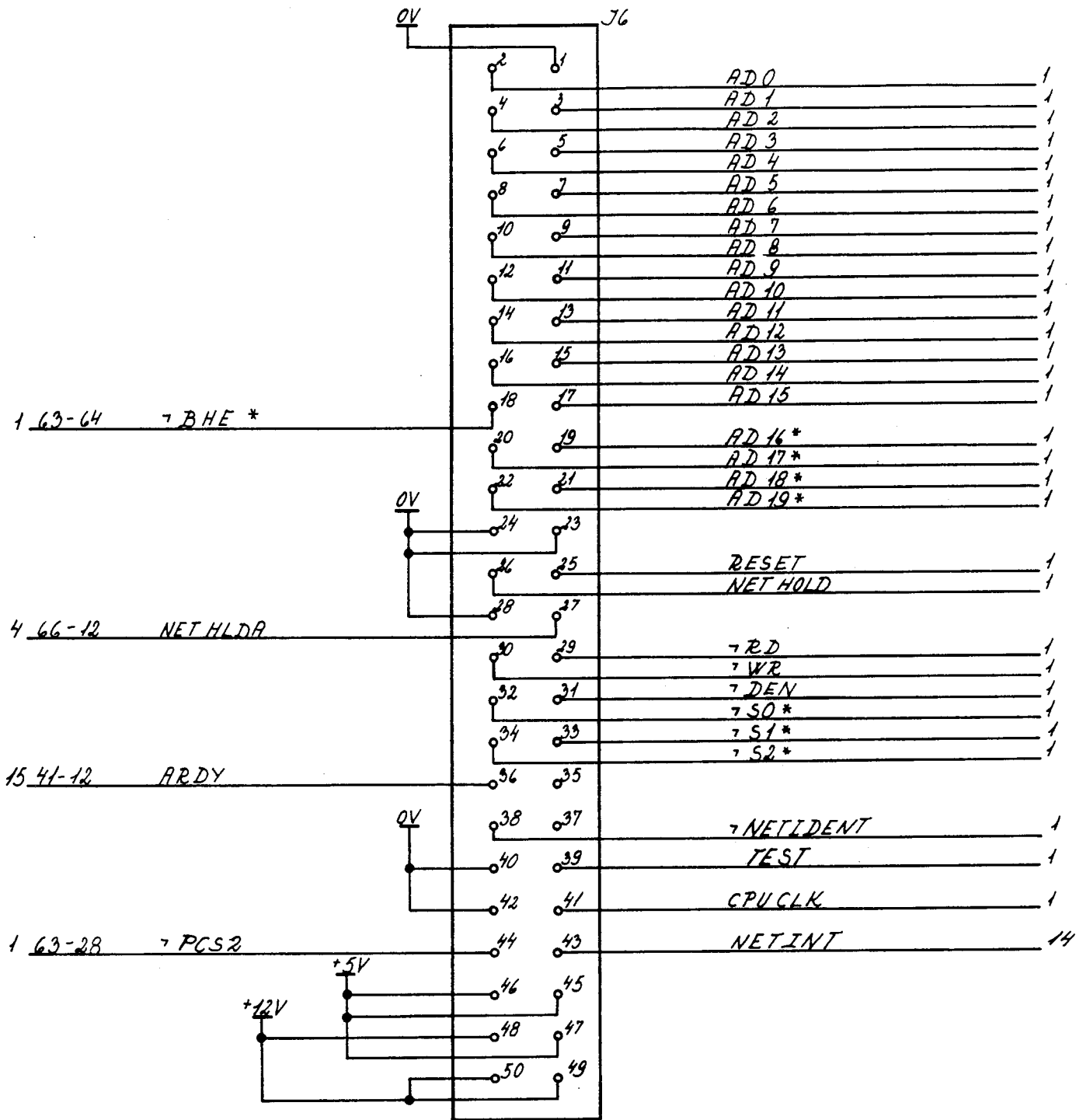
83.11.02

<u>Signal</u>	<u>Description</u>	
PARITY	Memory parity error detected.	
-MEMIDENT 0-1	Indication of attached memory size	
-MIO	-M11	Size
1	1	256 Kbytes
1	0	512 Kbytes
0	1	768 Kbytes
0	0	960 Kbytes



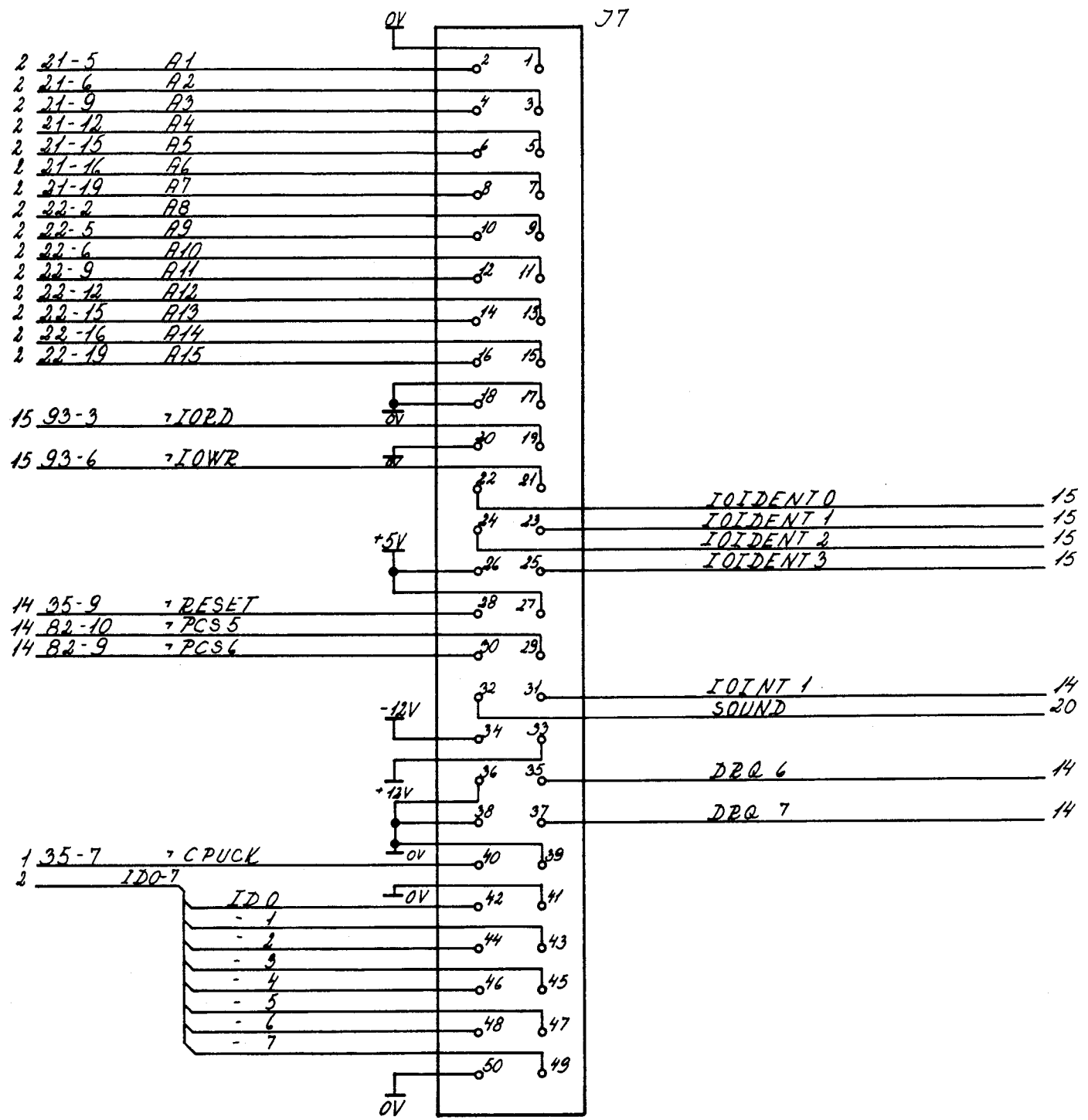
AGA
83.11.01

<u>Signal</u>	<u>Description</u>
AD 0-15	
A 16-19	Processor address/databus, driven or sensed by the processor currently holding the bus.
RESET	Generated by the CPU during hard reset.
HOLD	Bushold request to the CPU.
-RD, -WR, -DEN, DT/-R -NETIDENT	Bus control signals Low when an Ethernet processor is attached.
NET ALE	The coprocessor is presenting an address on the AD bus.
NET INT	Interrupt request from the net processor (IR5).



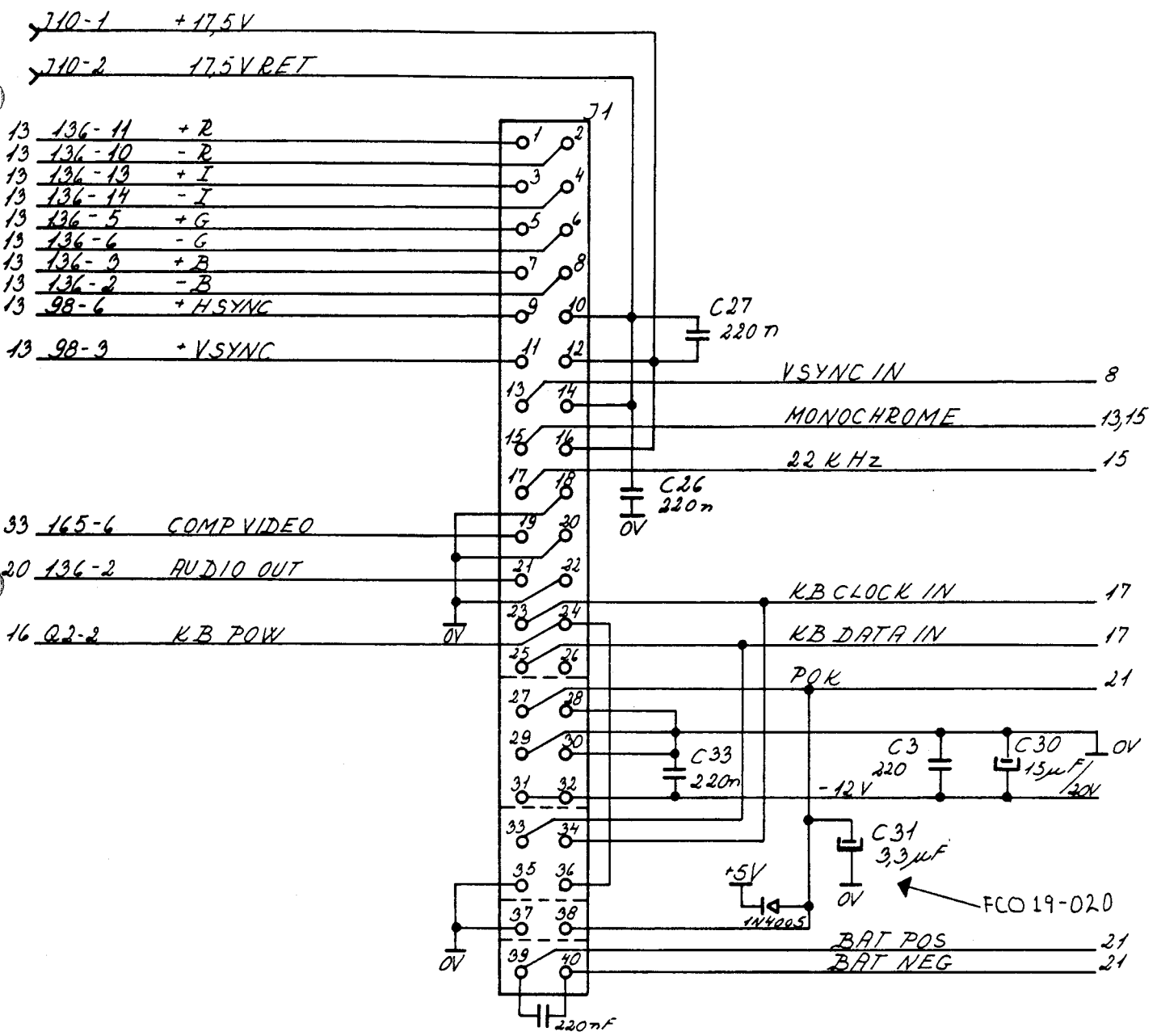
PC-A
83.11.02

<u>Signal</u>	<u>Description</u>
A1-15	Addressbus capable to address 32768 I/O ports
-IORD	When active the addressed device should place the relevant data on the databus 1D 0-7
-IOWR	When active, relevant data is present on the databus 1D 0-7 and may be strobed into the addressed port.
IOIDENT 0-3	Strap options for identifying attached I/O controllers.
-RESET	Low when a hard reset is issued.
-PCS 5	
-PCS 6	Decoded chip select outputs active on addresses 280 to 2FE and 300 to 37E
I/O INT	Interrupt request from I/O devices (IR7)
DRQ 6-7	DMA request inputs from I/O devices
-CPU CLK	Clockpulse from CPU 6 or 8 MHz
1 D 0-7	Databus.



AGA
83.11.02

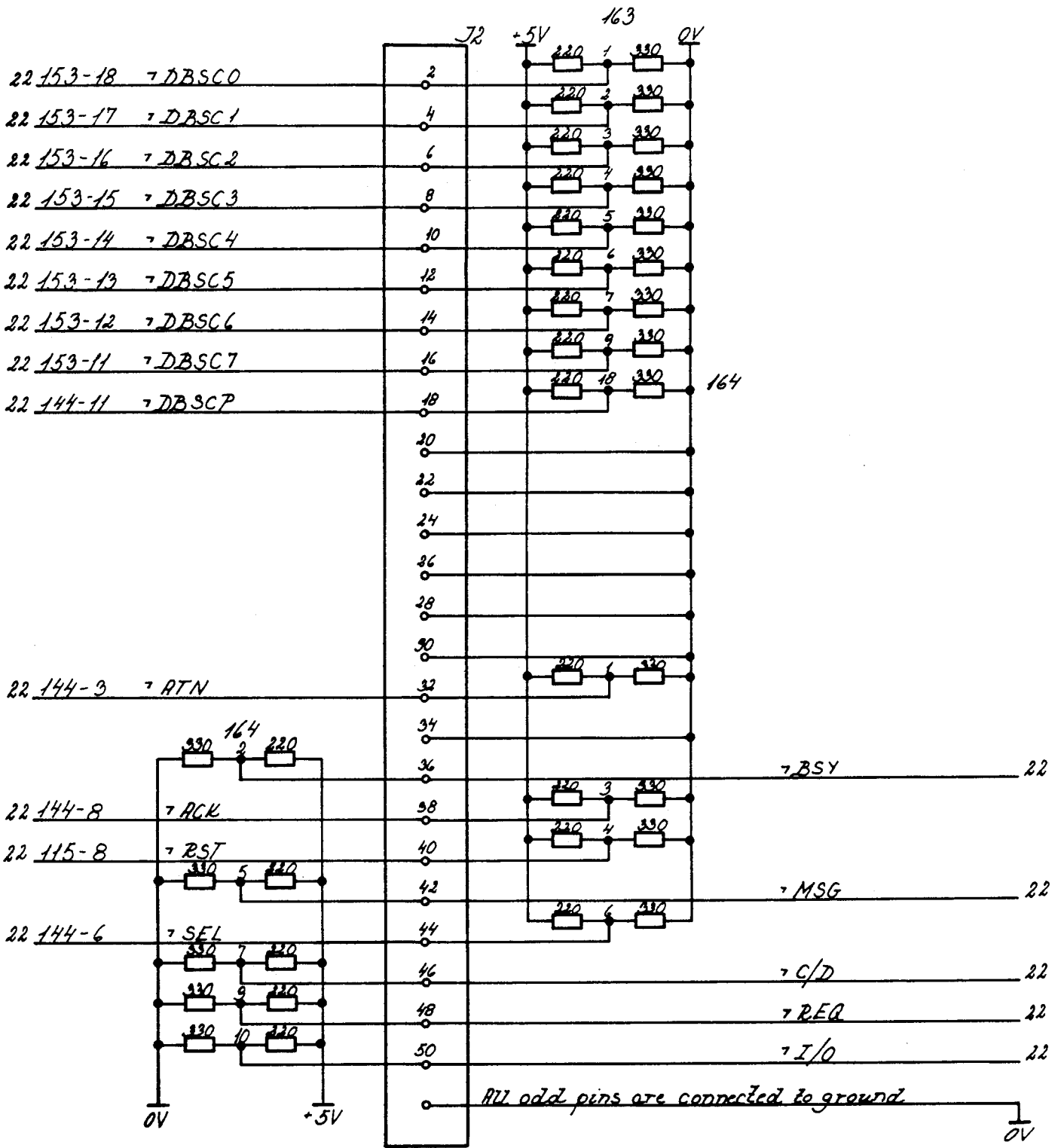
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Seen from Mounting side

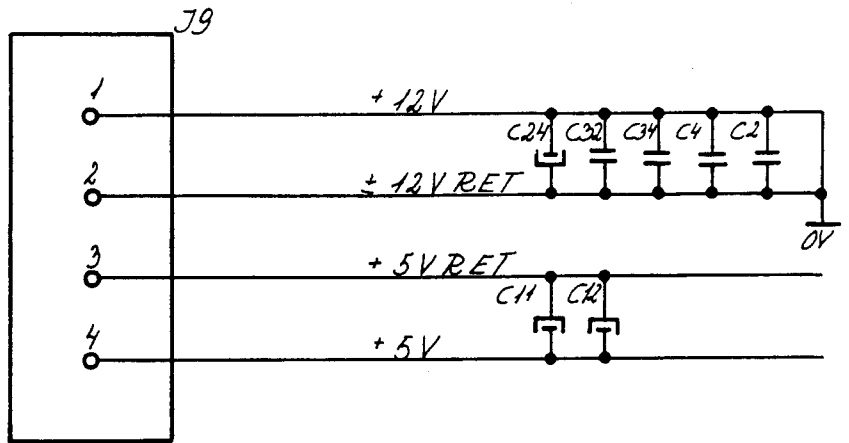
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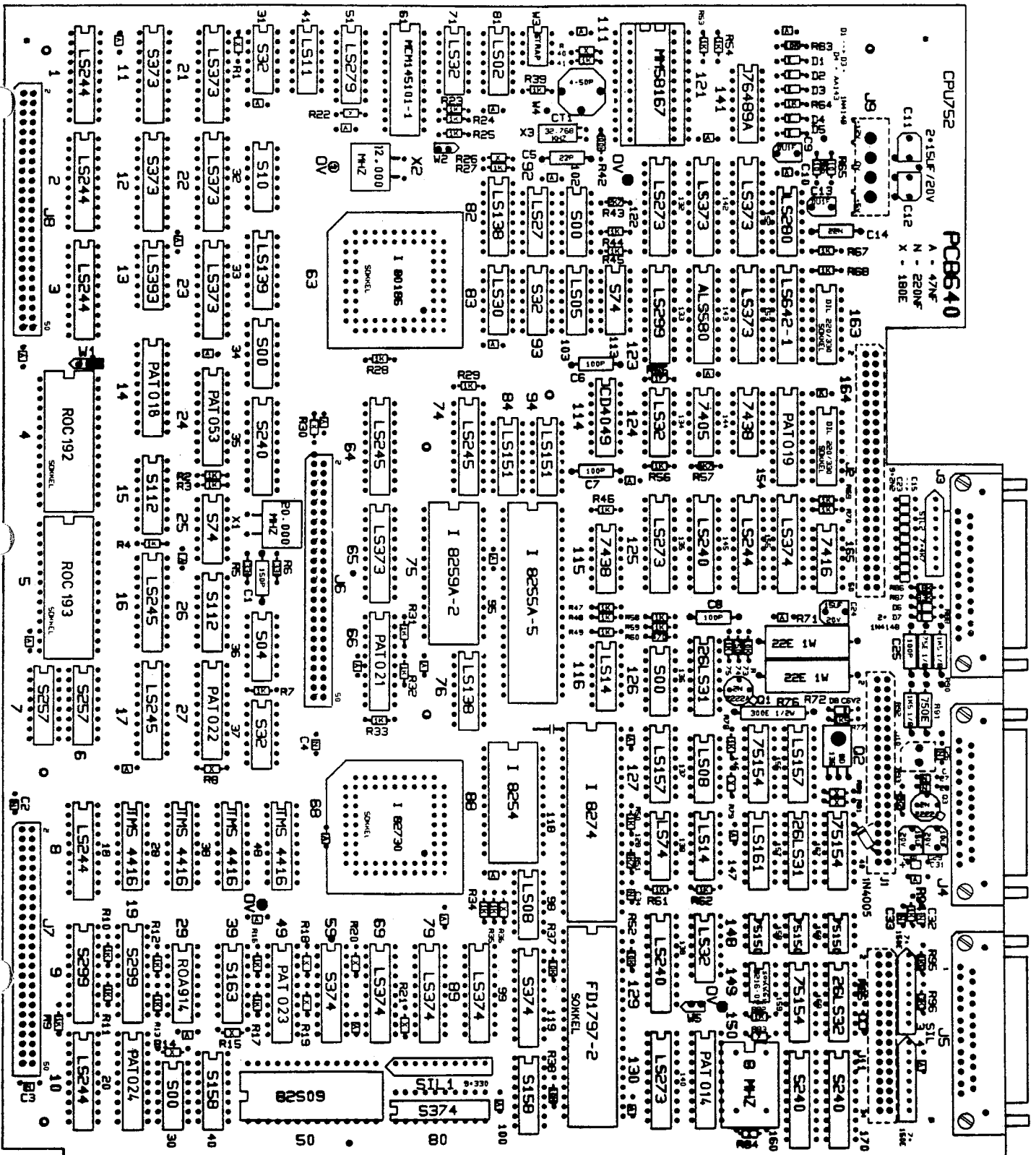
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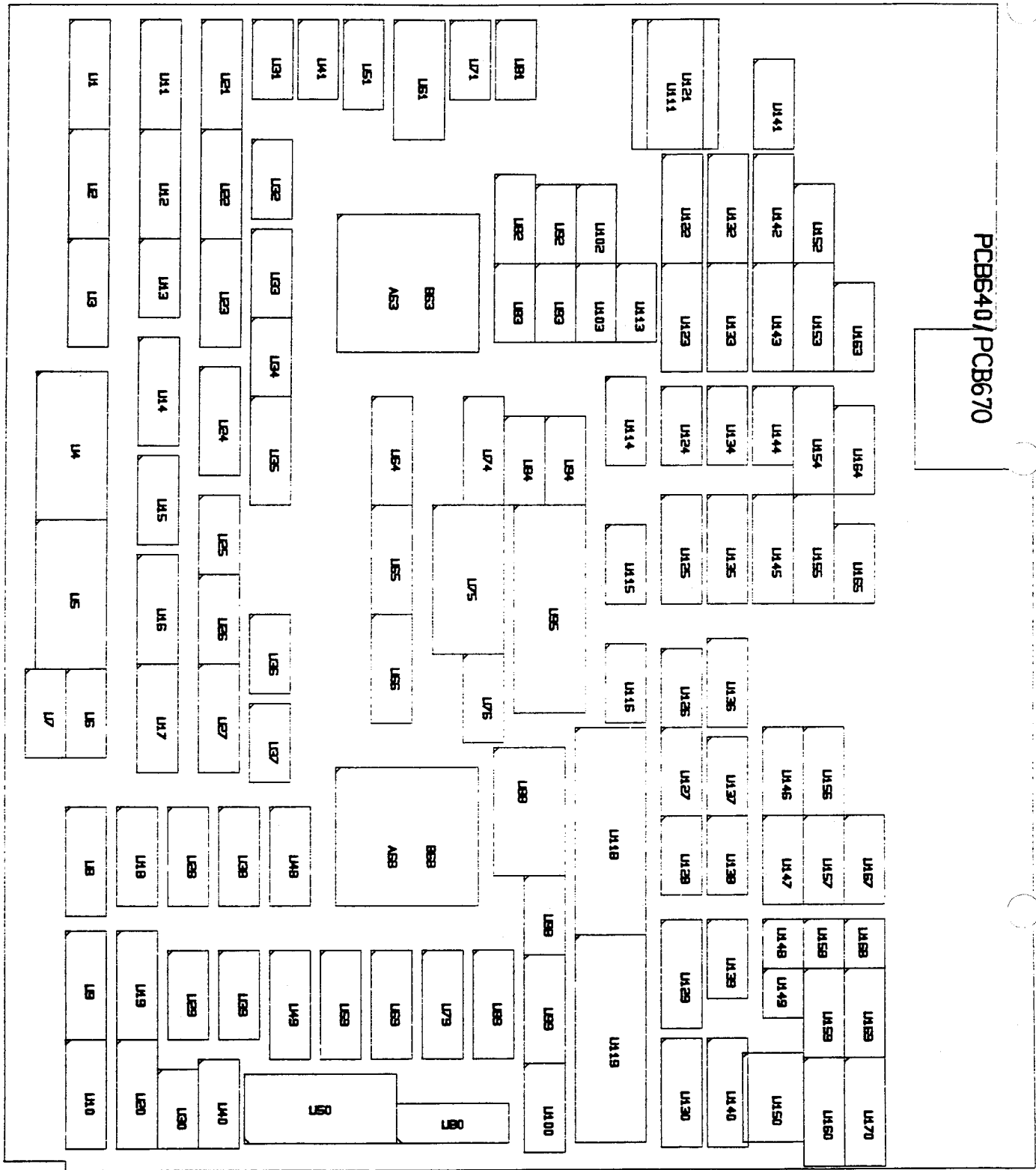
AGA
83.11.01

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BETEGNELSE CPU 752		UDGAVE	
01	831219 HC	07	840127 HC
02	831220 CP	08	840130 HC
03	840104 HC	09	840202 HC
04	840109 HC	10	840223 HC
05	840124 HC	11	840612 HC
PA PART NR	PA TEGN. PART NR	TEGN NR	
DESIGN HC	MONTAGE	760 53 100	
01 UDGAVE 831118			

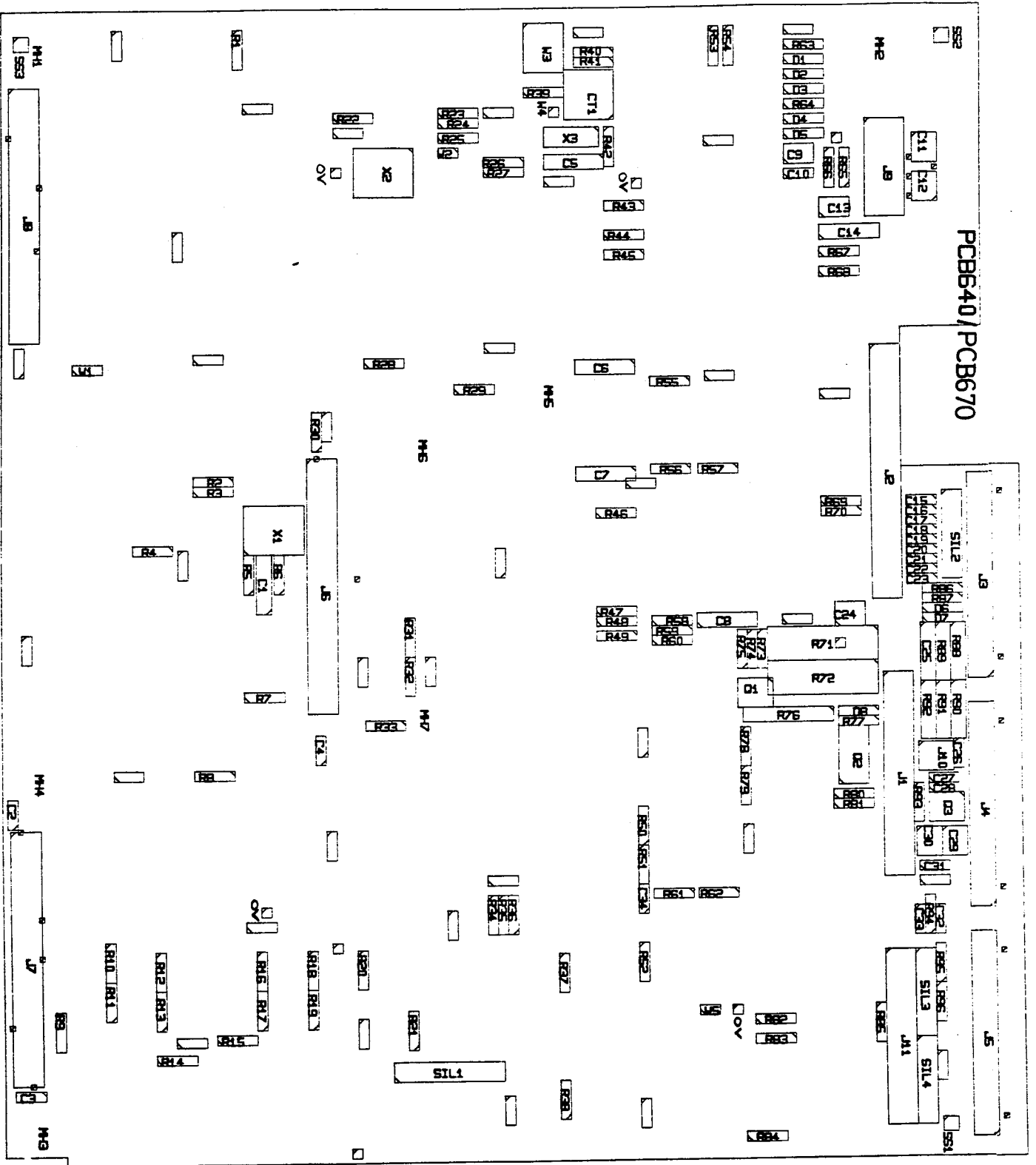
PCB640/PCB670





LAYER 1 COMPONENT SIDE

BETEGNELSE		UDGAVE	
SUPPLEMENT TIL MONTAGETEGNING.		02	07
MONTERING AF IC.		03	08
PA PART NR.	PA TEGN PART NR.	04	09
DESIGN CP		05	10
01 UDGAVE 840116	MONTAGE	06	11
		TEGN NR 760 53 930	

LAYER 1 COMPONENT SIDE



SYMBOL  UDEN POS.NR. => AFKOBLING 47nF.

BETEGNFISE SUPPLEMENT TIL MONTAGETEGNING. MONTERING DIV. DISKRETE		UDGAVE	
PA PART NR	PA TEGN. PART NR	02	07
DESIGN CP	MONTAGE	03	08
01 UDGAVE 840116		04	09
		05	10
		06	11
		TEGN NR  760 53920	

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RETURN LETTER

Title: CPU752 Technical Manual
RC750 CPU-Board.

RCSL No.: 991 09819

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Do you find errors in this manual? If so, specify by page.

How can this manual be improved?

Other comments?

Name: _____ Title: _____

Company: _____

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Date: _____

Thank you

RCSL Nr. 46-F 0093

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