

Internal use only

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Title:

CPU755, CPU756 Technical Manual
RC750 CPU-Board

Keywords:

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Abstract:

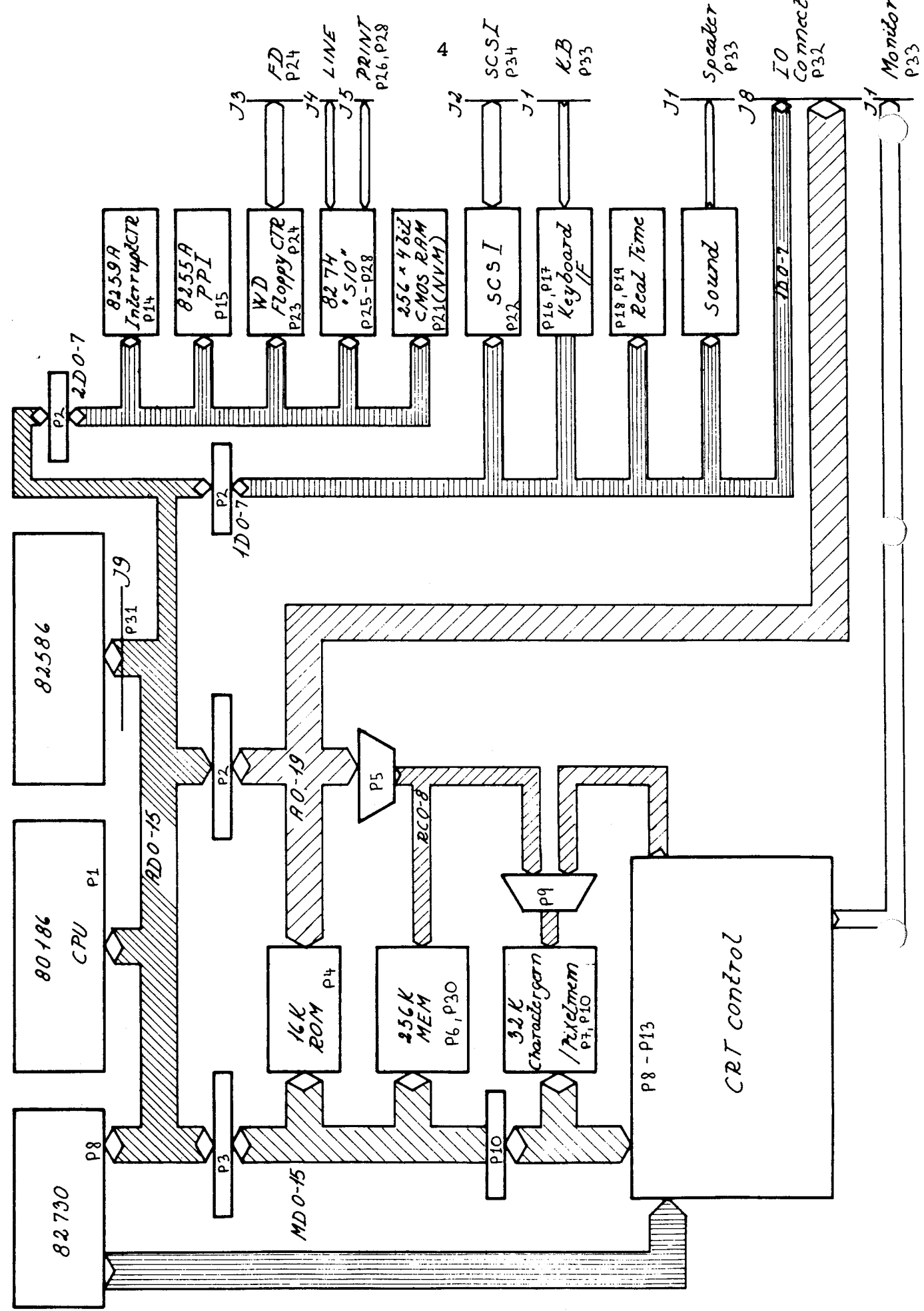
This manual contains the technical description of CPU755 and CPU756. Both CPUs are used in RC750.

The block diagram, shown on page 4, intends to give a general overview of the CPU.

The individual functional blocks are marked with references to relevant pagenumbers in the logic diagram.

The lefthand pages are thought as comments and explanation of the logic diagrams presented on the righthand pages.

PKA ACA
830520 830616

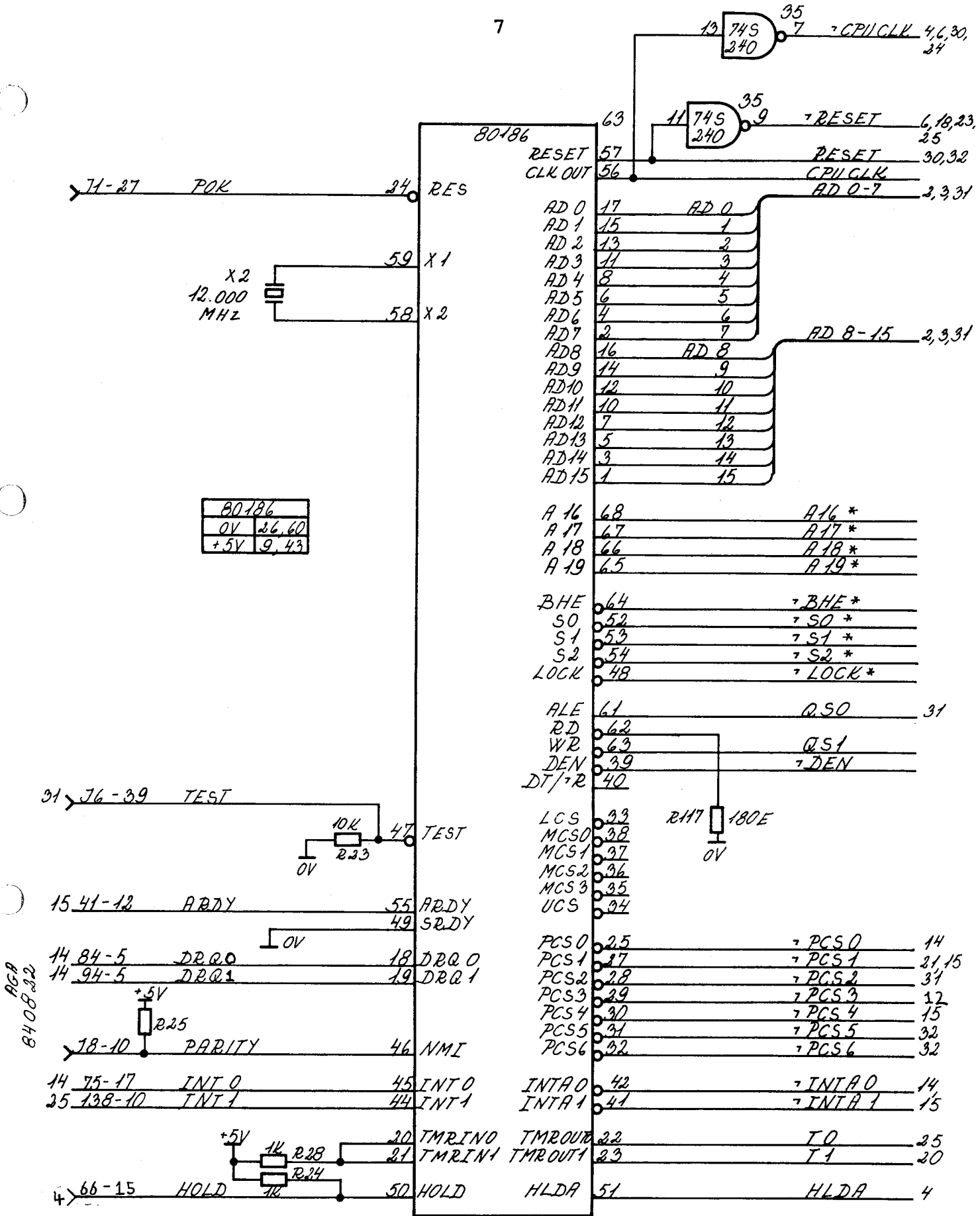


CPU 750

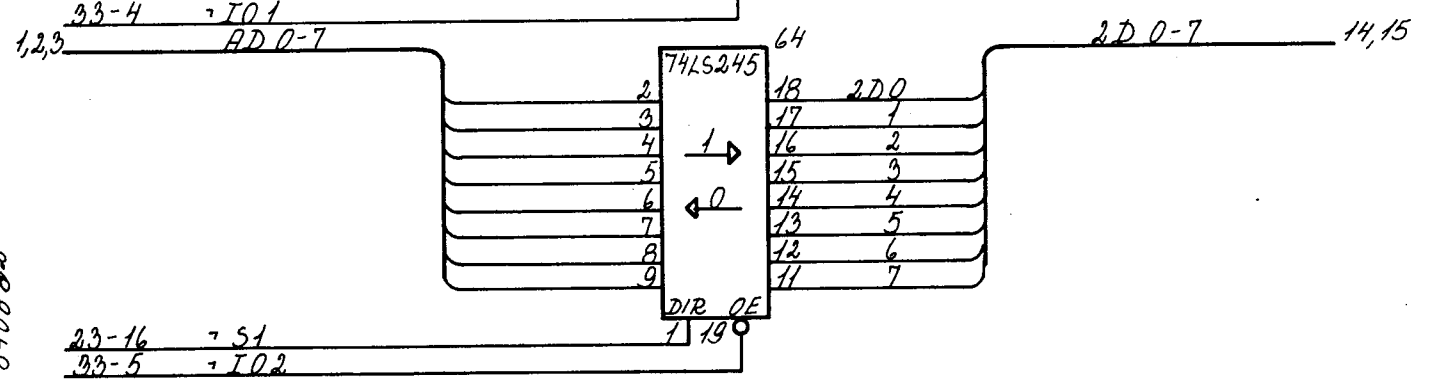
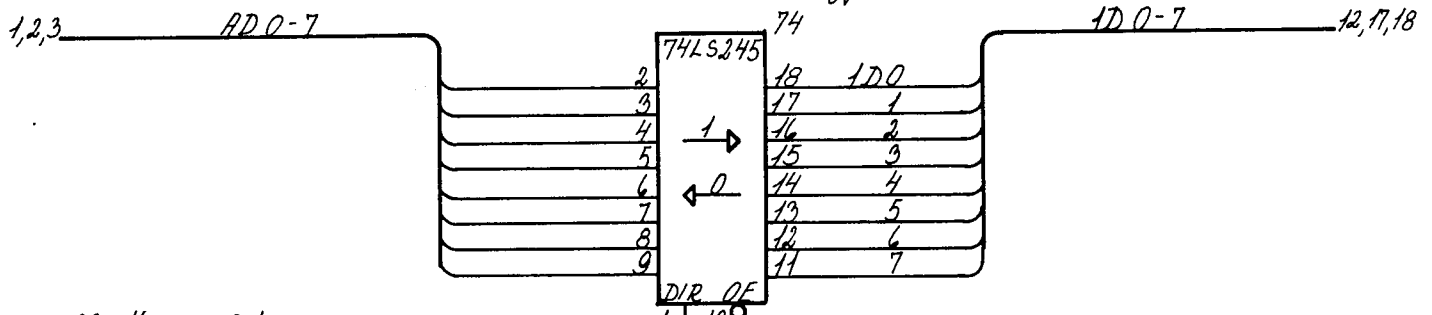
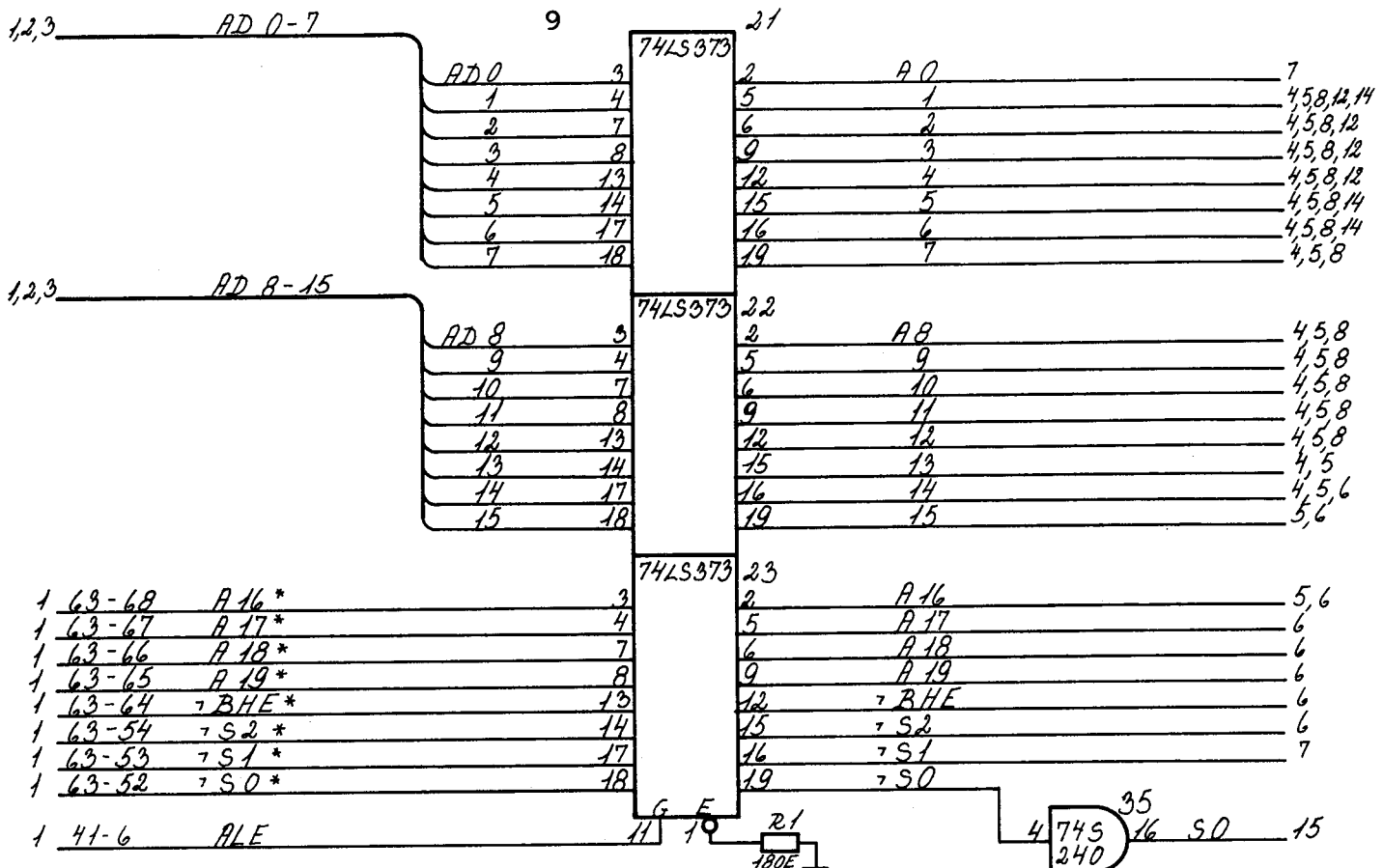
Block Diagram

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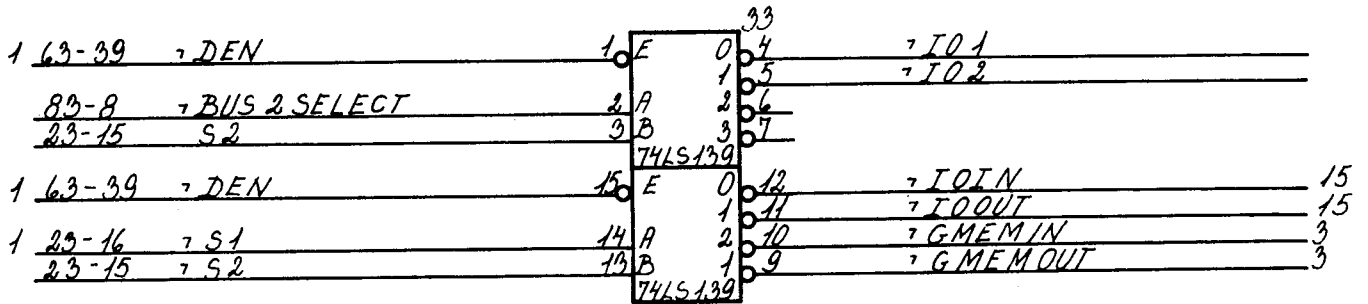
<u>Signal</u>	<u>Description</u>																																				
AD 0-15	Multiplexed Address/Databus common for the coprocessors. AD0 is least and AD15 most significant.																																				
ALE	Address Latch Enable Signifies a valid address on the AD bus.																																				
CPU CLK	Timing signal for parts running synchronously with the CPU.																																				
RESET	True when the CPU is being reset.																																				
A 16-19	The four most significant addressbits.																																				
-BHE	Byte High Enable low when data is transferred on D 8-15.																																				
-S0-2	Bus status signals indicating the kind of bus cycle being performed:																																				
	<table border="1"> <thead> <tr> <th>-S2</th> <th>-S1</th> <th>-S0</th> <th>Bus cycle</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Interrupt Acknowledge</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Read I/O</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Write I/O</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Halt</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Instruction Fetch</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Read Memory</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Write Memory</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Passive</td> </tr> </tbody> </table>	-S2	-S1	-S0	Bus cycle	0	0	0	Interrupt Acknowledge	0	0	1	Read I/O	0	1	0	Write I/O	0	1	1	Halt	1	0	0	Instruction Fetch	1	0	1	Read Memory	1	1	0	Write Memory	1	1	1	Passive
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1	0	1	Read Memory																																		
1	1	0	Write Memory																																		
1	1	1	Passive																																		
-RD, -WR	Read and Writestrobes.																																				
-DEN, DT/-R	Data enable, Direction Transmit/not Receive. Used to control Databuffers.																																				
-PCS 0-6	Peripheral Chip Select outputs.																																				
-INTA 0-1	Interrupt acknowledge.																																				
T 0-1	Timer outputs.																																				
HLDA	Hold acknowledge.																																				



<u>Signal</u>	<u>Description</u>
AD 0-19	Memory or I/O address for the current buscycle.
-BHE	Byte High Enable: latched version of the signal on the CPU.
-S 0-2	Bus status: latched versions of the signals on the CPU.
1 D 0-7	Databus used for transfer to or from peripherals having TTL bus interface.
2 D 0-7	Databus used for transfer to or from peripherals having MOS bus interface.
-GMEM IN/OUT	Gate memory data in/out: Controls for memory bus buffers.



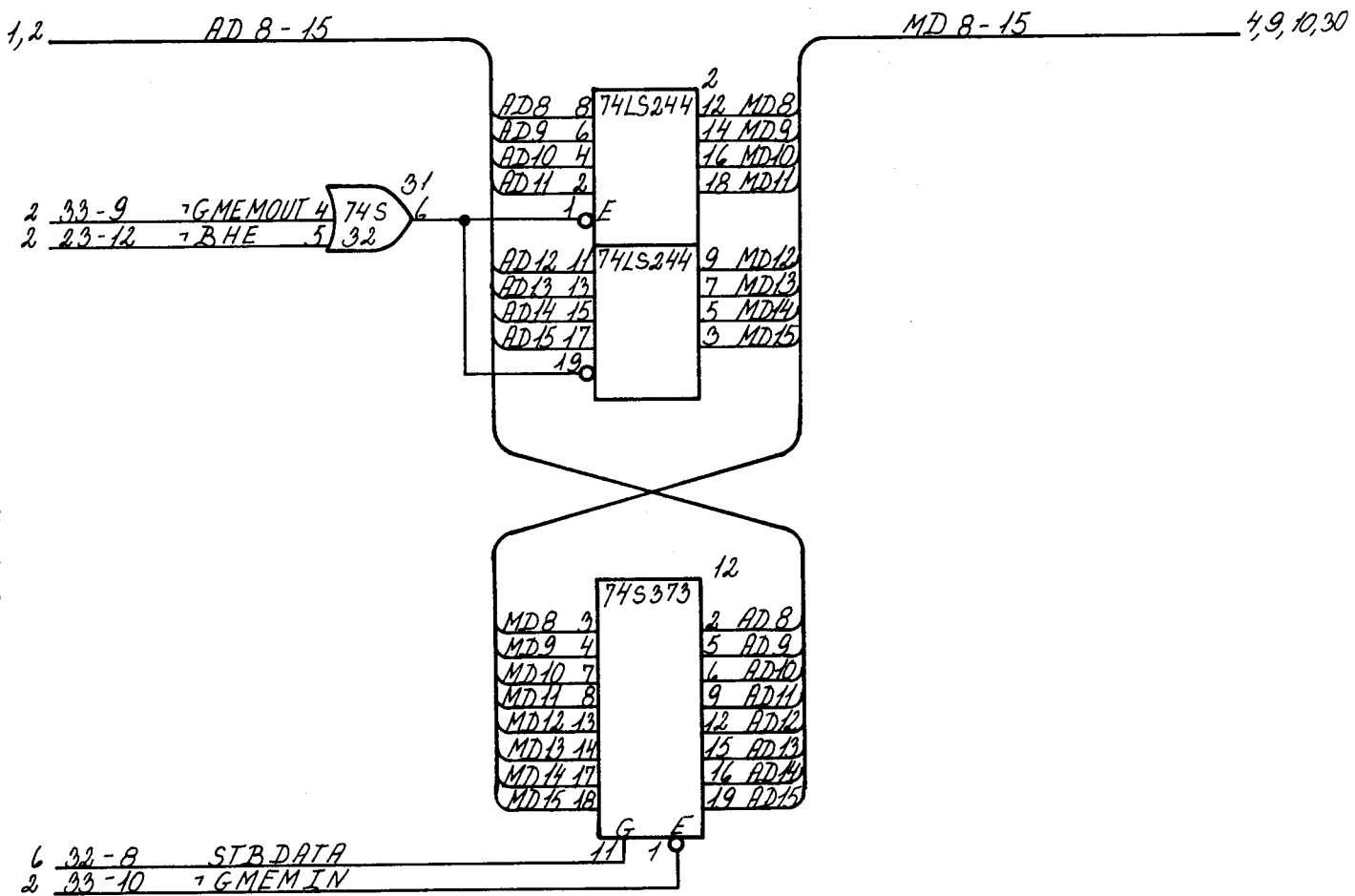
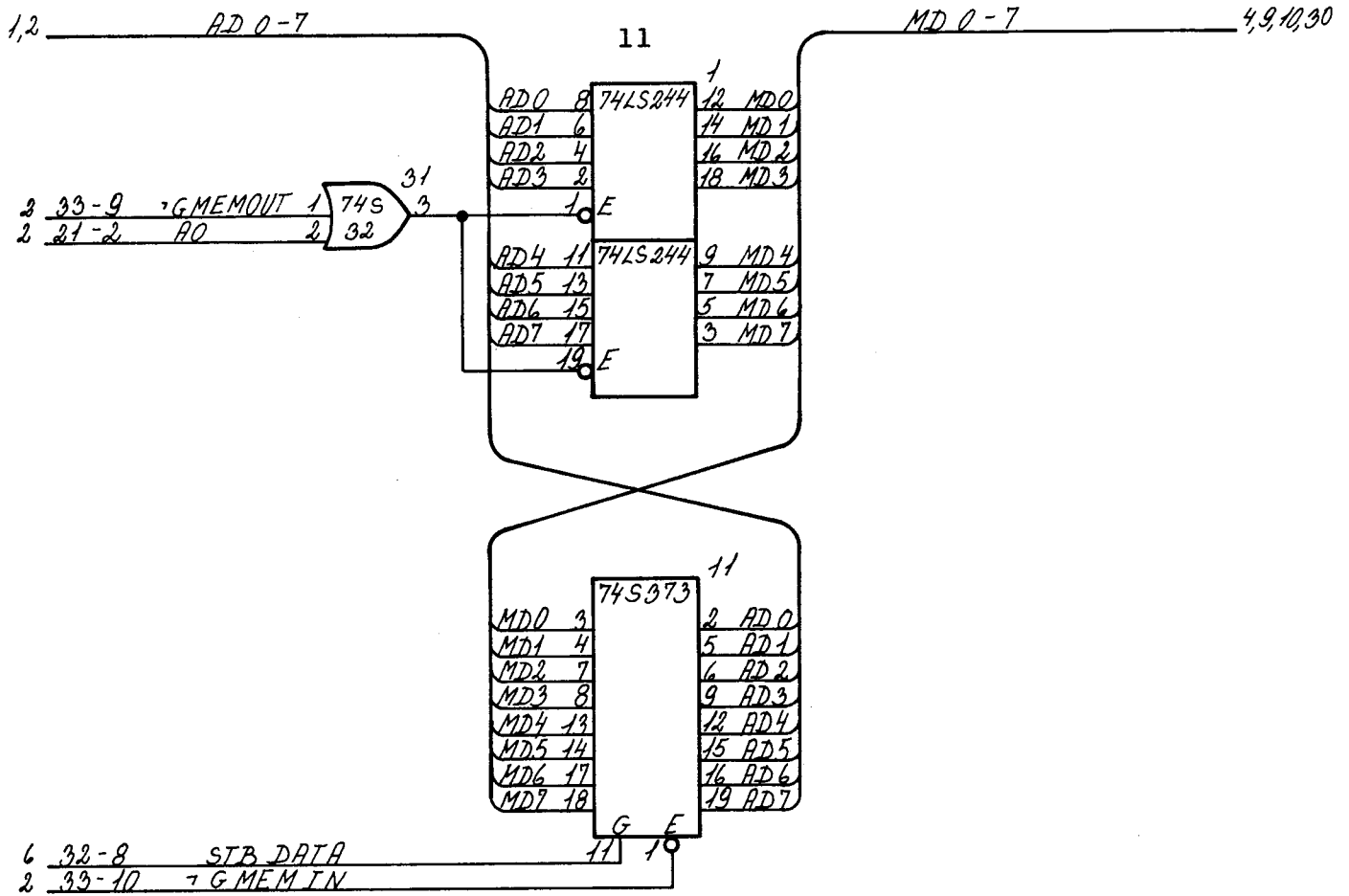
PCB
840882



CPU755 CPU756 ADDRESS LATCHES & DATA BUFFERS

<u>Signal</u>	<u>Description</u>
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MD 0-15	Memory databus connected to Main memory, Pixel memory and Read Only memory.
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840822

<u>Signal</u>	<u>Description</u>
MD 0-15	Memory databus.
NET HOLDA	Coprocessor hold acknowledge.
CRT HOLDA	CRT controller hold acknowledge.
HOLD	Hold request to CPU.
DRQPRIOR	Changes the DMA-priority with respect to CRT and LAN.

PAL16R8
PAT091
BUS ARBITOR

PAL DESIGN SPECIFIKATION
PKA 850624

CPUCK /NETH CRTH /DRQPRIOR HLDA LS /CLREF /MACC DRQ GND
/E NETA CRTA /DRQD HOLD /CRTAD REFRQ /MACCD /MACCDD VCC

/NETA := /NETH + /HLDA + CRTA + CRTAD + DRQD + /HOLD
/CRTA := /CRTH + /HLDA + NETH + NETA + DRQD + /HOLD
/HOLD := /NETH*/CRTH + /HOLD*DRQ*DRQPRIOR + /HOLD*DRQD +
CRTAD*DRQD*/CRTH + /CRTAD*DRQD*/NETH

/REFRQ := /LS

MACCDD := MACC*/MACCD*/MACCDD

MACCD := MACCDD

DRQD := NETA*DRQ*DRQPRIOR + CRTA*DRQ*DRQPRIOR +
DRQD*DRQ*DRQPRIOR + /HOLD*HLDA + DRQD*HLDA +
/NETH*/CRTH*HLDA

CRTAD := CRTA + CRTAD*CRTH

DESCRIPTION:

PRIORITY: IF DRQPRIOR THEN

0: DRQ

1: NET

2: CRT

ELSE

0: NET

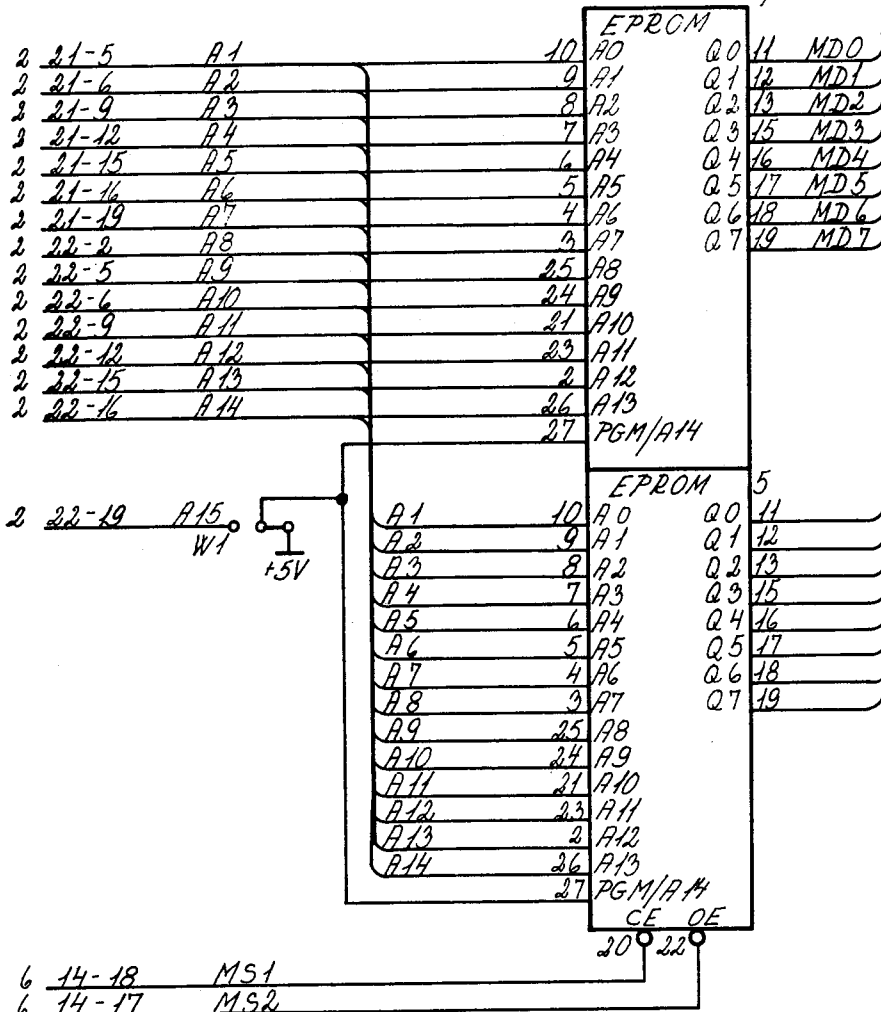
1: CRT

2: DRQ

NET WILL ALWAYS INTERRUPT CRT.

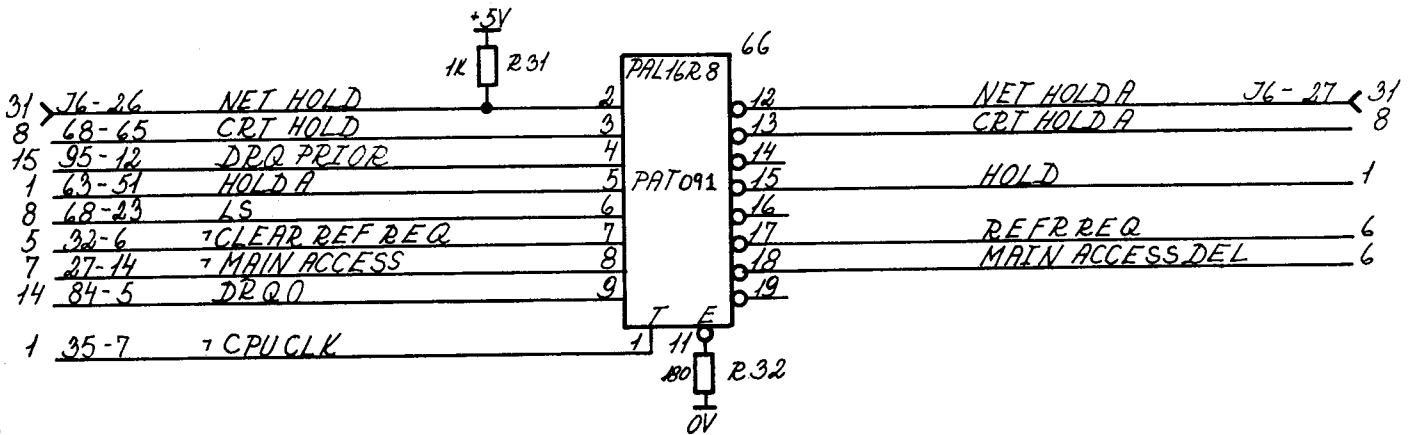
IF DRQPRIOR THEN DRQ INTERRUPTS BOTH NET AND CRT.

13 SOCKETS 4



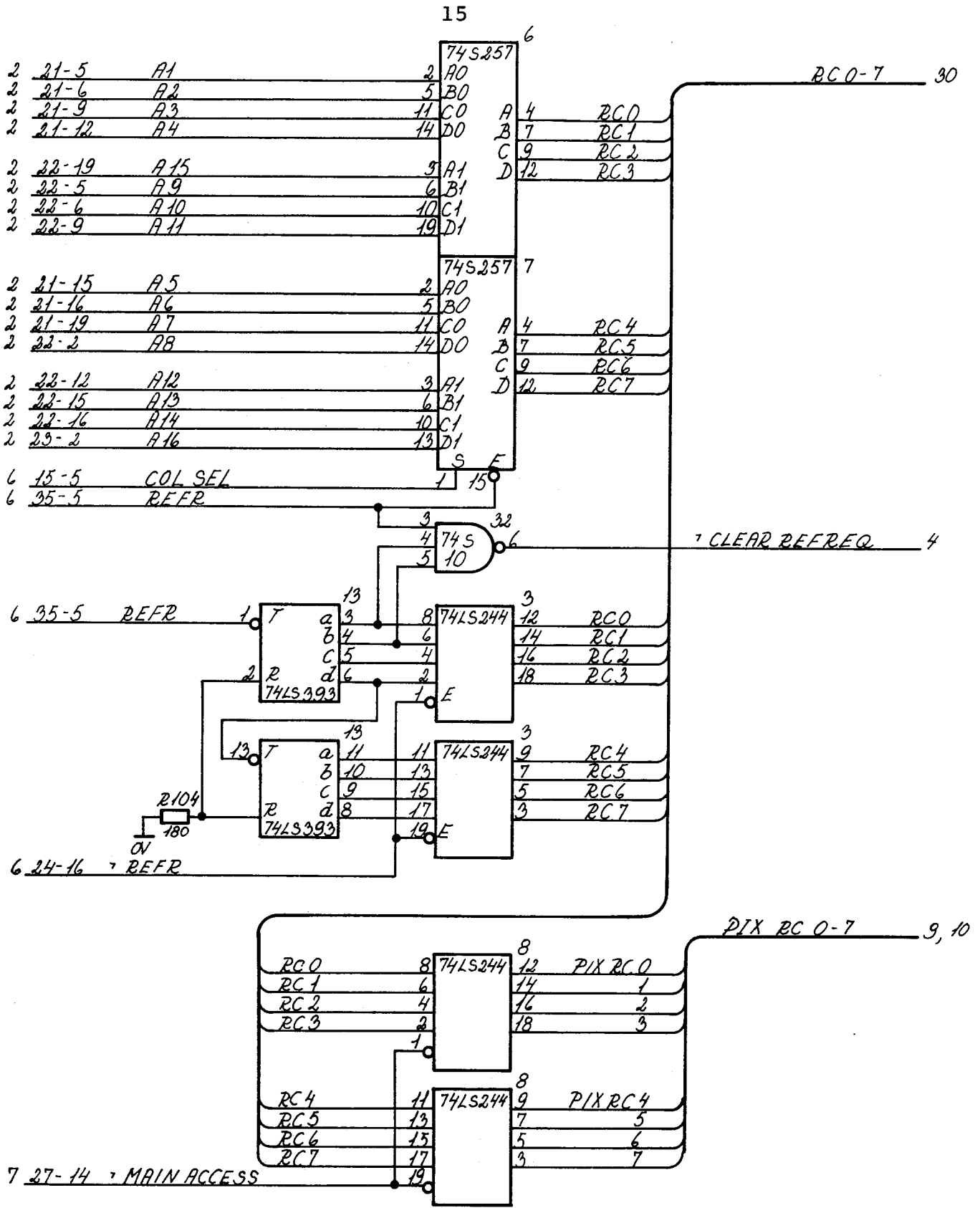
EPROM TYPES:

- 2764
- 27128
- 27256



840822 RGA

<u>Signal</u>	<u>Description</u>
RC 0-75	Row and Column address multiplexed for addressing of the main memory consisting of DRAM's.
CLEAR REFREQ	This signal is active when the fourth refresh cycle in each refresh burst is being executed, indicating the end of the burst.
PIX RC 0-7	Row and Column address multiplexed for addressing of the pixel memory.



PGA
8408 23

CPU755 CPU756

ADDRESS MULTIPLEXERS FOR
ROW/COLUMN SELECTION & REFRESH ADDRESS COUNTER

Signal	Description
MS 0-2	Memory selection code
WE LO/HI	Write enable for low and high byte
/RC8	A18 and A19 multiplexed

PAL16L8 PAL DESIGN SPECIFIKATION
 PAT0092 PKA 850613
 MEMADDR. DECODER RC750

/S2 A14 A15 A16 A17 A18 A19 A0 /BHE GND
 RASEN RC8 /S1 COLSEL /WEHI /WELO
 MS2 MS1 MS0 VCC

IF(VCC) /MS0 = /A19+/A18+/A17+/A16+A15+S2
 IF(VCC) /MS1 = A19+/A19+S1+/S1+/MS1
 IF(VCC) /MS2 = A19*A18*A17*A16*A15+S2
 IF(VCC) WELO = /S2*/S1*/A0
 IF(VCC) WEHI = /S2*/S1*BHE
 IF(VCC) /RC8 = /COLSEL*/A17+COLSEL*/A18

DESCRIPTION:

PAL16R8A PAL DESIGN SPECIFIKATION
 PAT053 (PAT020 REPLACEMENT) PKA 840201
 MAIN MEMORY CONTROLLER

CPCLK ALE MS0 MS1 MS2 REFREQ NC /MAINACC /RESET GND
 /OE /ALED MAINM CRTSEL RASEN /REFR /CAS COLSEL MRDY VCC

ALED := ALE

/MAINM := CAS + MAINACC
 + /MAINM*MRDY*/ALE*/REFREQ + /MAINM*MRDY*ALED*/REFREQ
 + /MAINM*MS0*/REFREQ + /MAINM*/MS1*/MS2*/REFREQ
 + /MAINM*RASEN

/CRTSEL := MAINACC + RESET
 + /CRTSEL*MRDY*/ALE*/REFREQ + /CRTSEL*MRDY*ALED*/REFREQ
 + /CRTSEL*/MS0*/REFREQ + /CRTSEL*RASEN
 + /CRTSEL*REFREQ*/REFR

/RASEN := CAS + MAINACC
 + /RASEN*MRDY*/ALE*/REFREQ + /RASEN*MRDY*ALED*/REFREQ
 + /RASEN*/MS0*/MS1*/MS2*/REFREQ + /RASEN*REFREQ*/REFR

REFR := REFR*/MAINACC*/RESET
 + REFREQ*/RASEN*/MAINM*/CRTSEL*/MAINACC

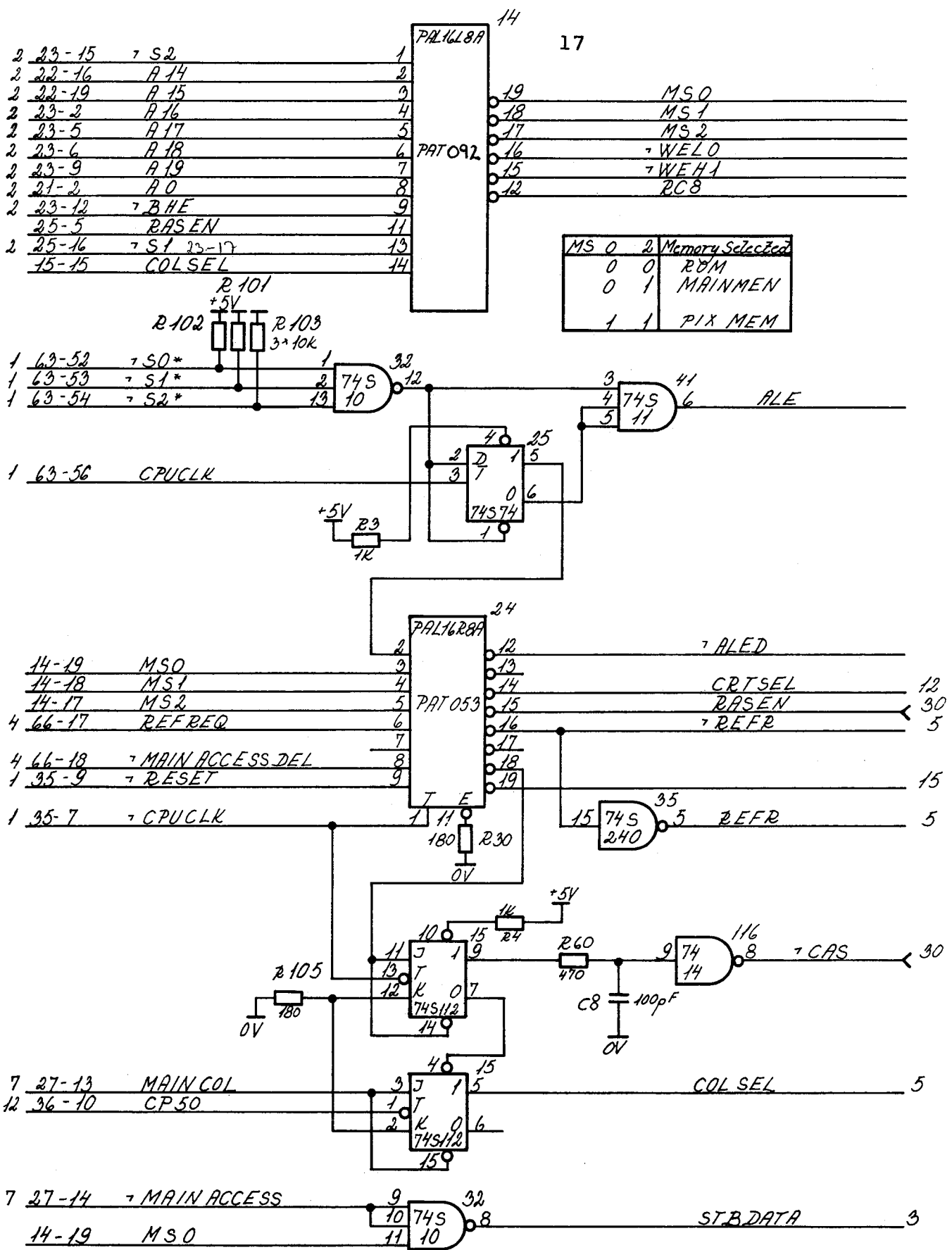
/COLSEL := CAS + /COLSEL*MRDY*/ALE + /COLSEL*MRDY*ALED
 + /COLSEL*/MS0*/MS1*/MS2 + /COLSEL*MS0
 + /COLSEL*RASEN + /COLSEL*REFREQ
 + /COLSEL*REFR

CAS := /CAS*RASEN*/REFR*/CRTSEL*MS2
 + /CAS*RASEN*/REFR*/CRTSEL*MS1
 + RESET

/MRDY := ALE*/ALED*REFR*MS1 + ALE*/ALED*REFREQ*MS1
 + ALE*/ALED*REFR*MS2 + ALE*/ALED*REFREQ*MS2
 + ALE*/ALED*MS0
 + /MRDY*REFR + /MRDY*REFREQ + /MRDY*MS0*/MAINACC

DESCRIPTION:

CRTSEL	Access to pixel memory
RASEN	Enable Row Address Selection
REFR	Refresh cycle in progress
COLSEL	Control signal to address mux
STBDATA	Load datalatches with MB0-15



AGA
84.08.24

CPU755 CPU756 MAIN MEMORY CONTROL

<u>Signal</u>	<u>Description</u>
PIXRAS	RAS signal to Pixel memory
/PIXROWSEL	Selection signals to address multiplexer
/PIXCOLSEL	for addresses generated by 82730. Both inactive when a mainaccess is in progress, as main memory controller supplies multiplexed address.
PIXCAS	CAS signal to Pixel memory
PIX S1	Pixel memory cycle in progress
MAINCOL	Address multiplex control signal during main access.
MAINACCESS	Main system (CPU or coprocessor) is accessing the Pixel memory.
GPIX	Connects the PIX memory data bus to the Main memory data bus.
PIXWELO/HI	Write enable LO and HI for the pix memory
PIXOE	Output enable to pix memory chips.

PAL16R8A PAL DESIGN SPECIFIKATION
PAT022 PKA 830721
PIXEL MEMORY CONTROLLER

CP50 CRTSEL /REFR /WELO /WEHI CNT0 CNT1
CNT2 CNT3 GND /E /PIXS1 MAINCOL /MAINACC
/GPIX PIXCASEN /PIXWELO /PIXWEHI
/PIXOE VCC

PIXS1 := CNT0*/CNT1*/CNT2*/CNT3*CRTSEL +
CNT0*/CNT1*/CNT2*CNT3 +
PIXS1*/CNT0 +
PIXS1*/CNT2

MAINACC := CNT0*/CNT1*/CNT2*/CNT3*CRTSEL +
MAINACC*/CNT1 +
MAINACC*/CNT2

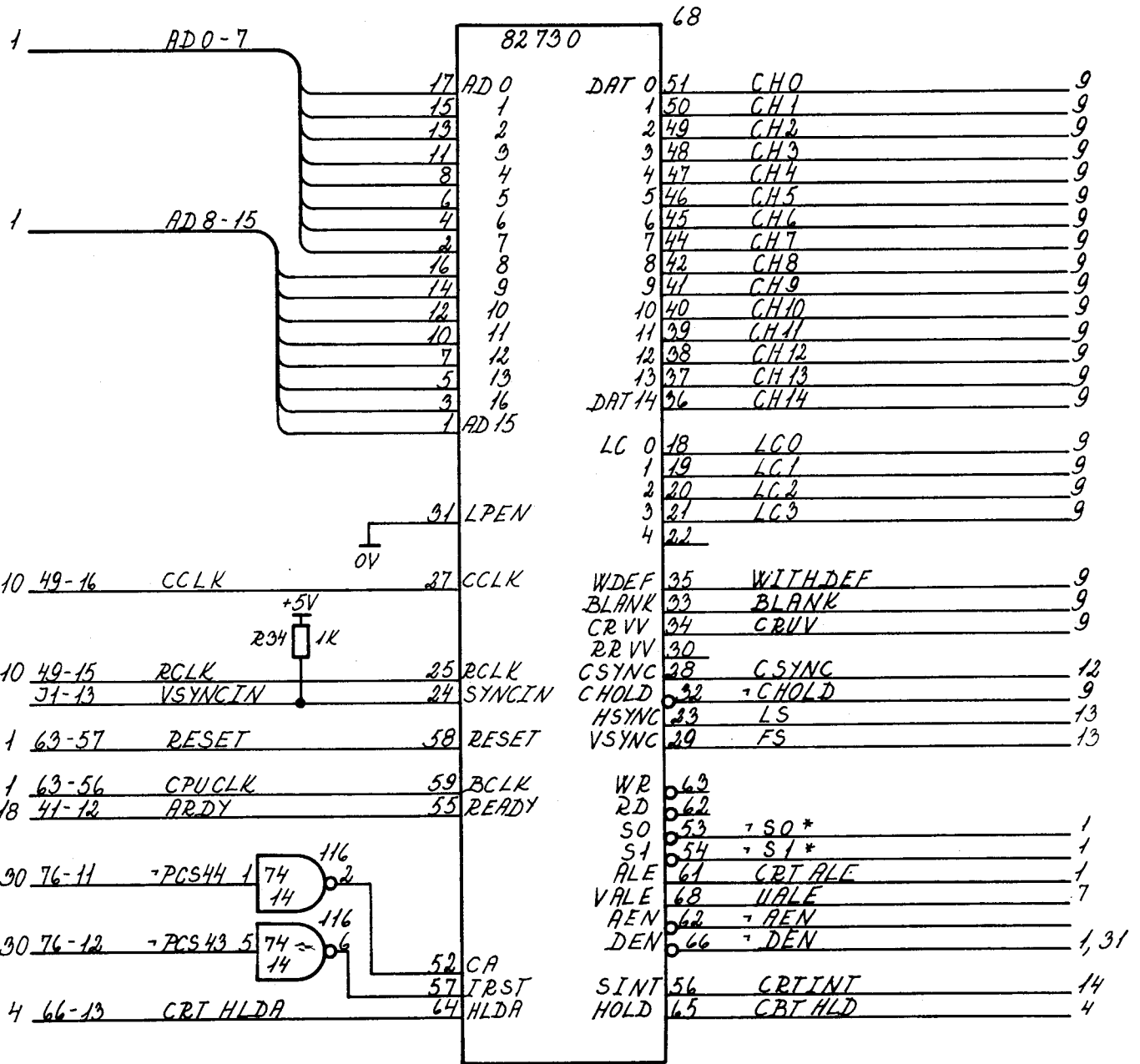
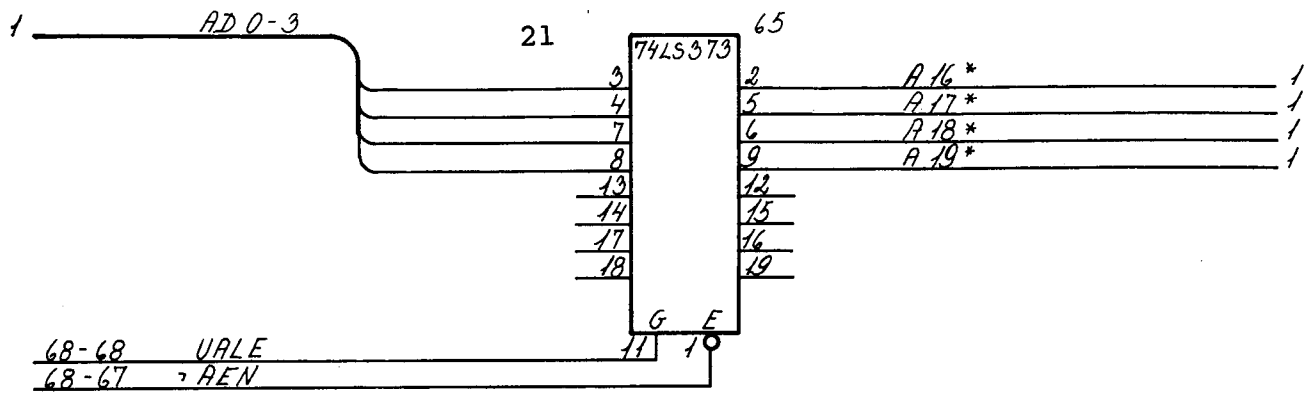
GPIX := CNT0*/CNT1*/CNT2*/CNT3*CRTSEL*/REFR +
GPIX*/CNT0 +
GPIX*/CNT1 +
GPIX*/CNT2

/PIXCASEN:= /GPIX*/CNT3 +
/CNT2*/CNT1 +
/CNT2*/CNT0 +
CNT0*CNT1*CNT2

PIXWELO := WELO*MAINACC*/REFR
PIXWEHI := WEHI*MAINACC*/REFR
PIXOE := CNT3 + MAINACC*/PIXWELO*/PIXWEHI*/WELO*/WEHI
/MAINCOL:= /MAINACC + CNT0*CNT1*CNT2

DESCRIPTION:

<u>Signal</u>	<u>Description</u>
A16-19*	Most Significant addressbits generated by 74LS373 which is loaded from the Processor bus on UALE (Upper Address Latch Enable) time.
CH 0-14	Value of next displayed character clocked out of 82730 on CCLK.
LC 0-3	Video Line Count bits indication video line no within one row.
BLANK	Next character shall not be displayed
CRVV	Next character shall be displayed in reverse video.
CSYNC	True during retrace for synchronizing CCLK to RCLK.
CHOLD	When active the CCLK is stopped.
LS	Line sync
FS	Frame sync
-WR	
-RD	Bus controls
-S0*	For the coprocessor bus
-S1*	
CRTALE	
UALE	Upper Address Latch Enable
CRT INT	Interrupt signal (IR3)
CRT HLD	Coprocessor bushold request.



82730	
+5V	9, 43
0V	26, 60

Signal Description

PIXRC 0-7 Pipelined and multiplexed characterbits
and videoline count bits for read into
the pixel memory.

ATTR 0-4 Pipelined version of character bits 10-14

CRVVD,
BLANKD Pipelined versions of CRUV and BLANK

PAL16R8A PAL DESIGN SPECIFICATION
PAT063 erstatter PAT023 PKA 840809
CRT CLOCK CONTROL

CP50 CNT0 CNT1 CNT2 CNT3 CSYNC /GRAPH /CHOLD NC GND
/OE /A /B /C RCLK CCLK CSYND /LDCNT CNTEN VCC

A := /B*/C*/RCLK
 + B* C*/RCLK
 + /B* C* RCLK
 + B*/C* RCLK

B := A*/C*/RCLK
 + A* C* RCLK
 + /A* B

C := /A* B*/RCLK
 + C*/RCLK
 + C*/B
 + C* A

/RCLK := /A*/B*/C
 + /RCLK* A
 + /RCLK* B
 + /RCLK*/C

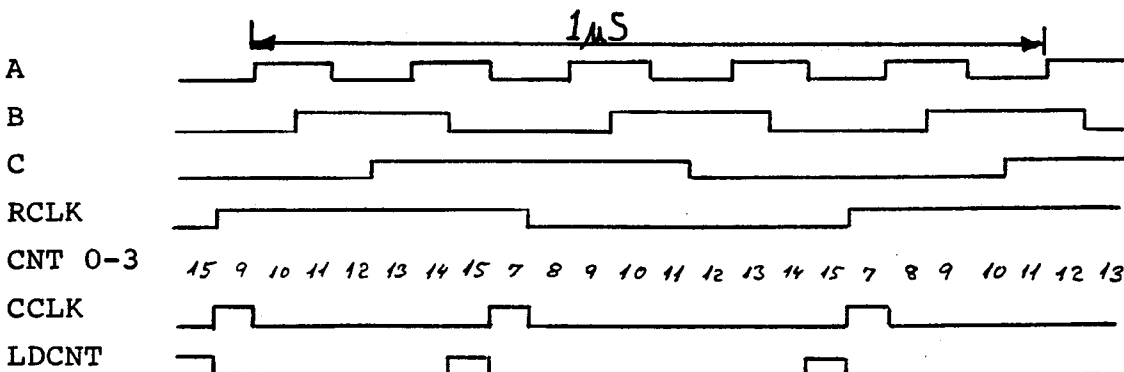
/CCLK := CCLK +/CNT3 +/CNT2 +/CNT1 +/CNT0 + CHOLD

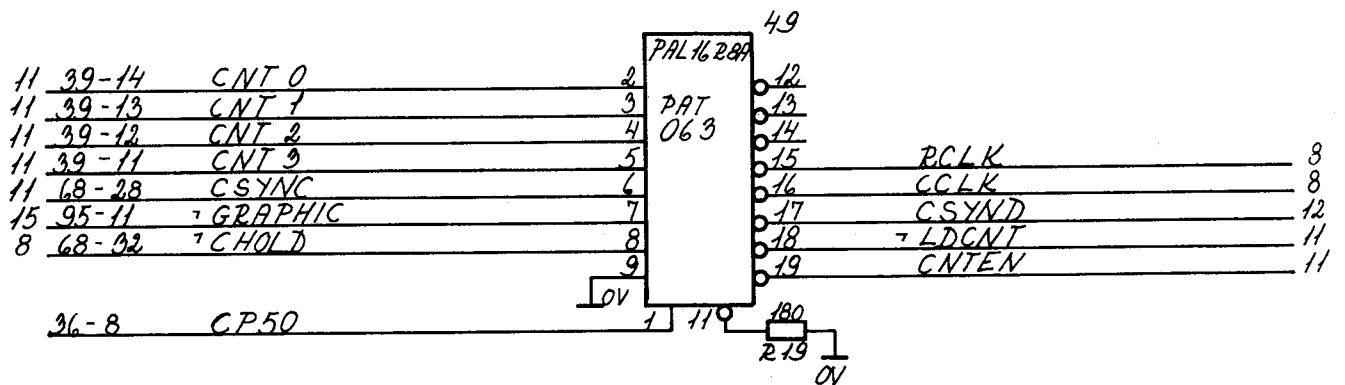
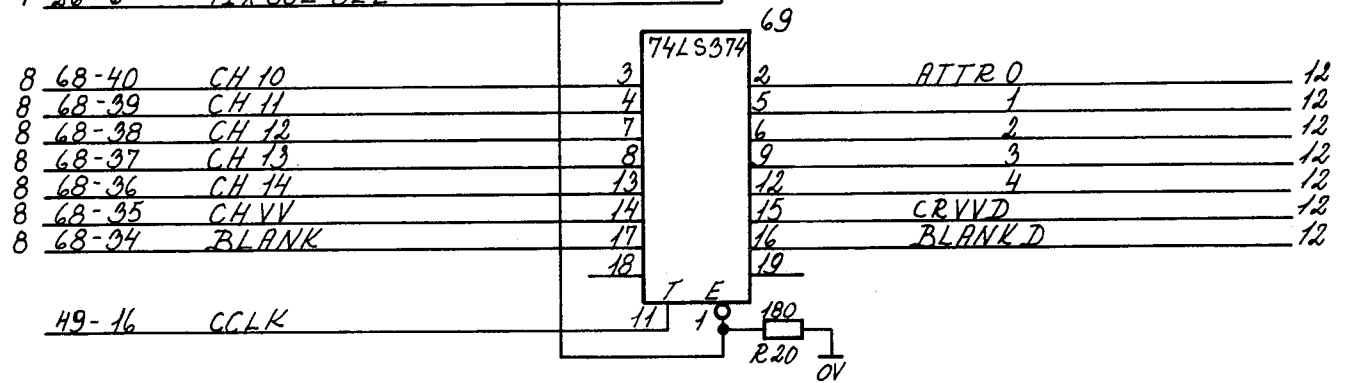
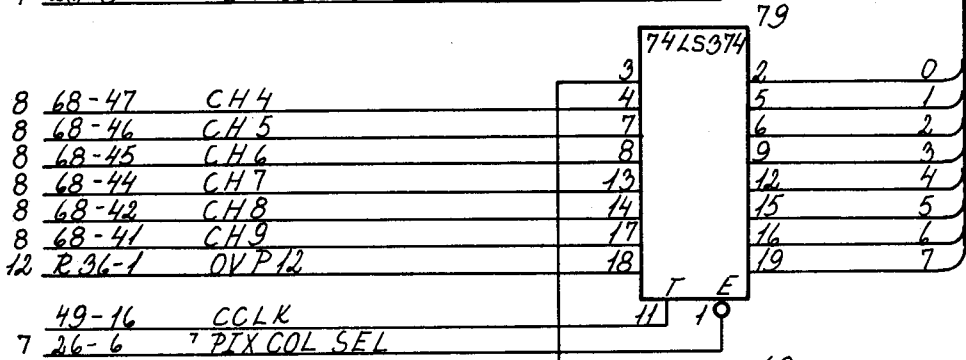
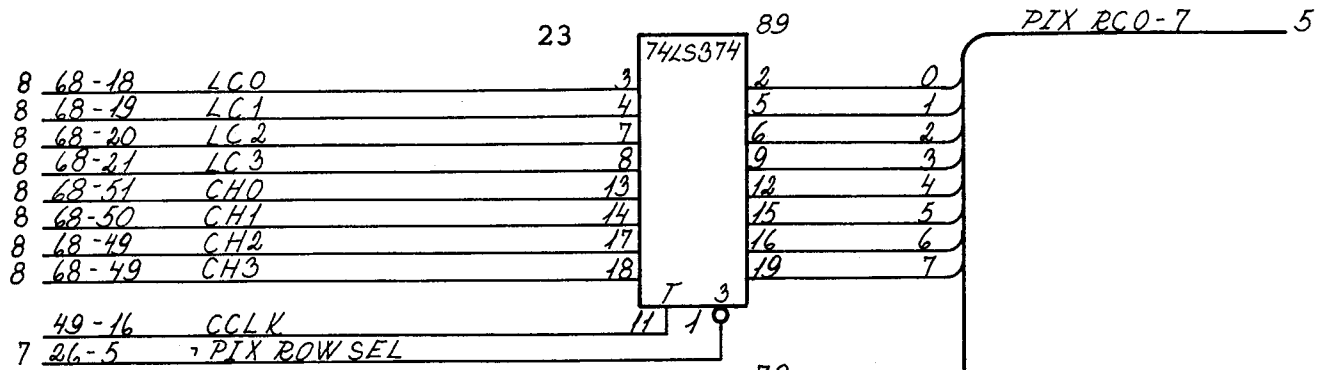
/CSYND := /CSYNC
 + /CSYND* RCLK
 + /CSYND*/C
 + /CSYND* B

/CNTEN := CSYND* CNT1* CNT2* CNT3* B
 + CSYND* CNT1* CNT2* CNT3*/C
 + CSYND* CNT1* CNT2* CNT3* RCLK
 + CHOLD* CNT1* CNT2* CNT3* B
 +/CNTEN* CNT1* CNT2* CNT3* B
 + CHOLD* CNT1* CNT2* CNT3*/C
 +/CNTEN* CNT1* CNT2* CNT3*/C
 + CHOLD* CNT1* CNT2* CNT3* RCLK

LDCNT := /LDCNT* CNT1* CNT2* CNT3*/CSYND*/GRAPH*/CHOLD

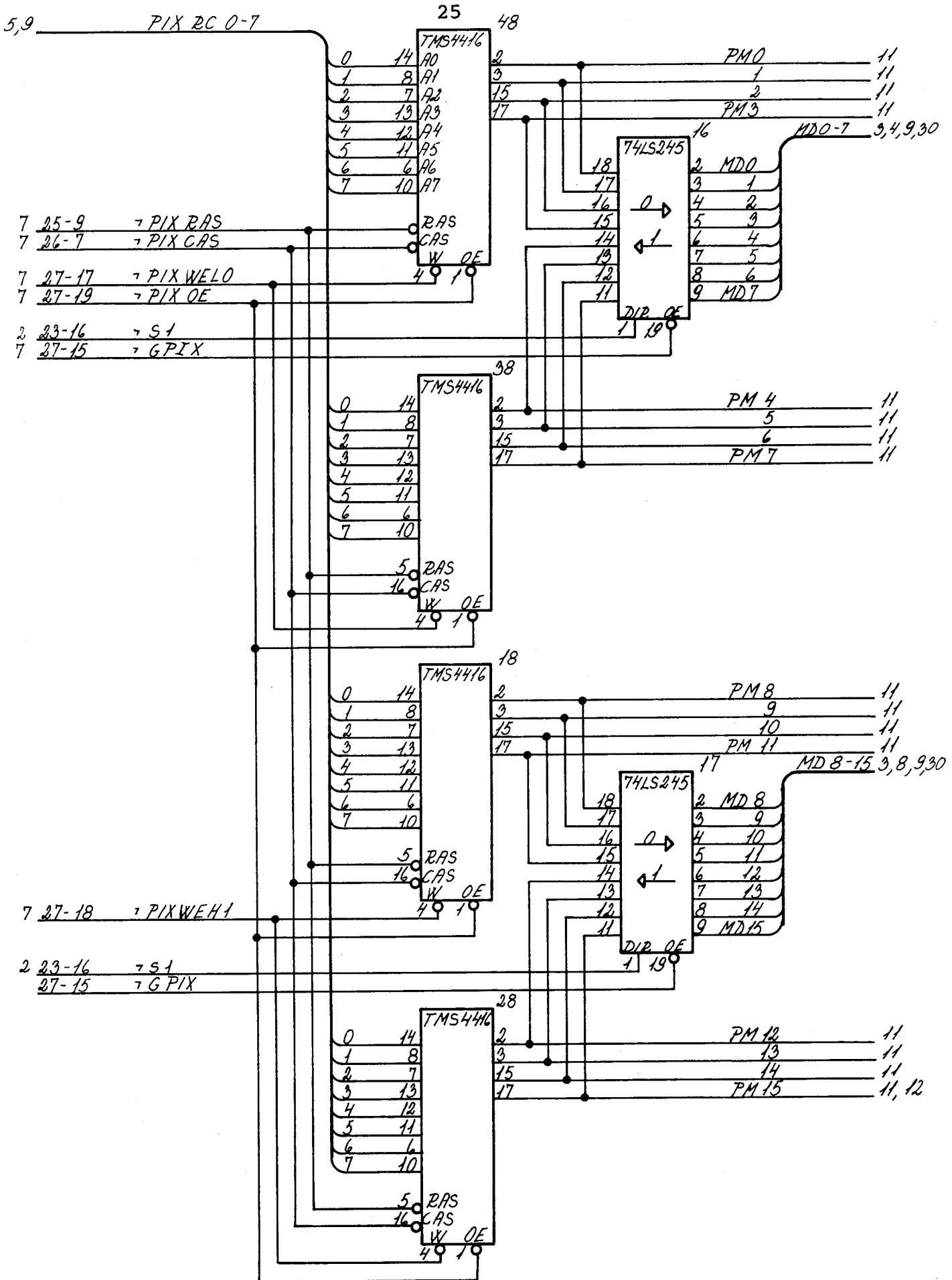
DESCRIPTION:





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<u>Signal</u>	<u>Description</u>
PM 0-15	Pixel memory databus.

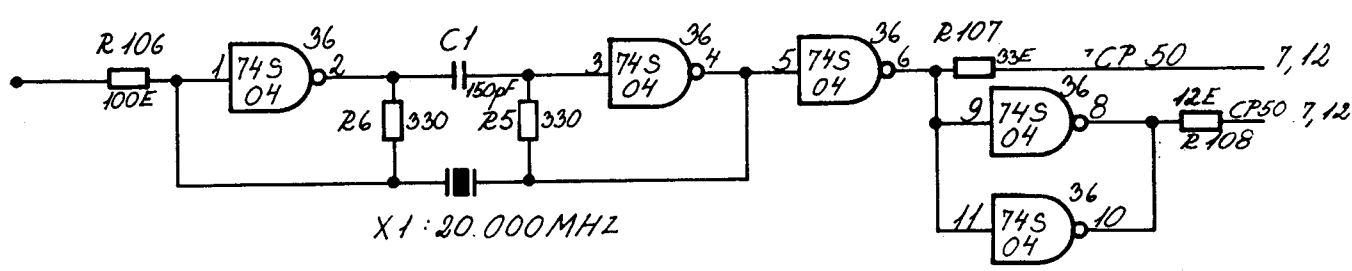
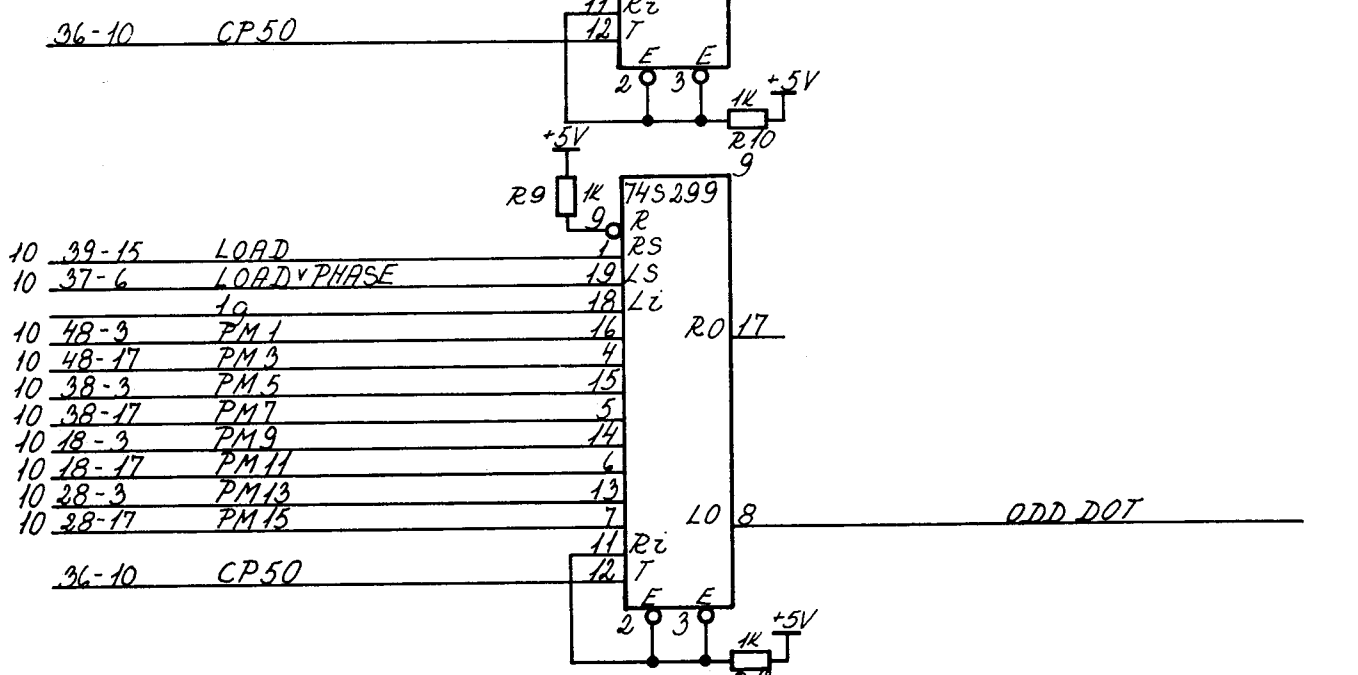
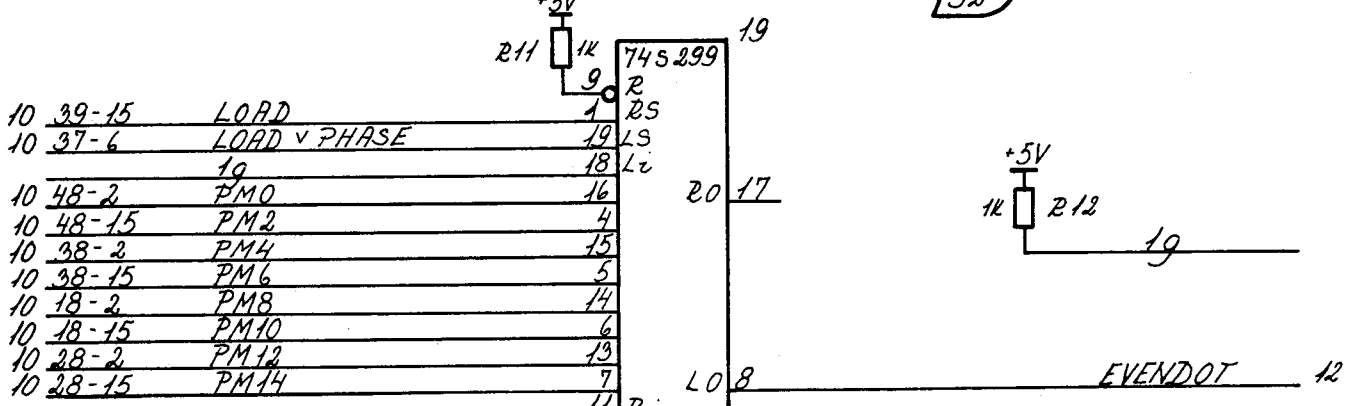
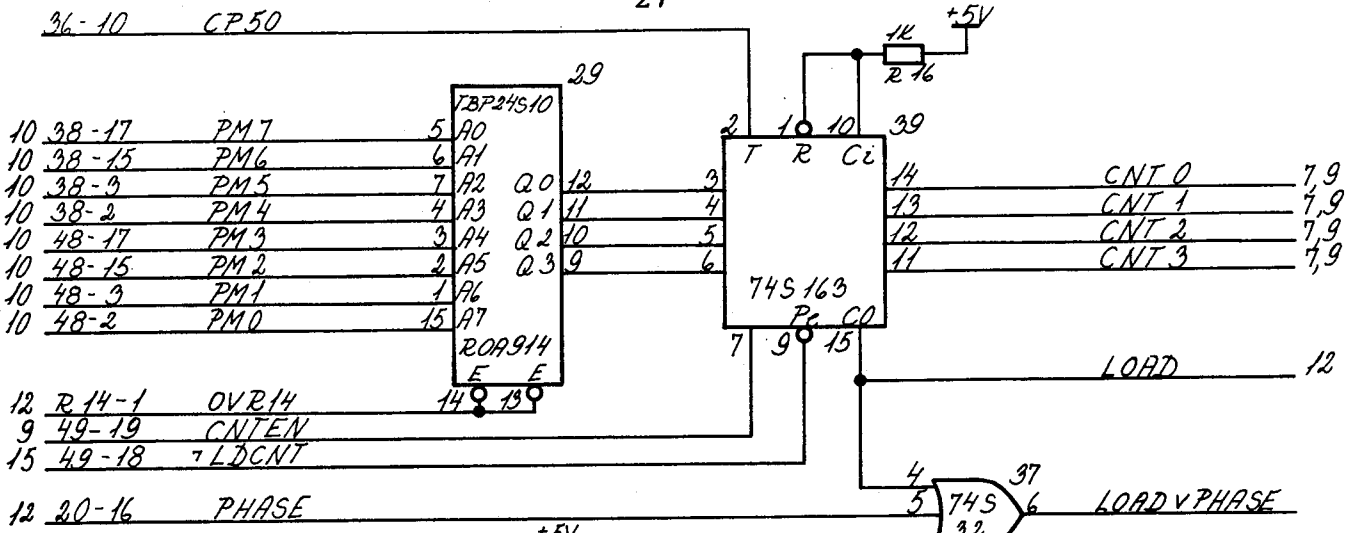


Signal	Description
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CNT 0-3	Dot counter output used to generate CCLK and to control Pix memory cycles. When not in graphic mode, the dot counter is loaded with 16-char width. Char width is derived from the dotpattern read in the pixel memory by means of ROA914:
---------	--

PM 7 6 5 4 3 2 1 0	16-char width	char width
X X X X X X X 0	1	15
X X X X X X 0 1	2	14
X X X X X 0 1 1	3	13
X X X X 0 1 1 1	4	12
X X X 0 1 1 1 1	5	11
X X 0 1 1 1 1 1	6	10
X 0 1 1 1 1 1 1	7	9
0 1 1 1 1 1 1 1	8	8
1 1 1 1 1 1 1 1	9	7

LOAD	Loads next dotpattern into the shiftregisters
PHASE	True every second clock period allowing the shifters to advance only every 100 nSec.
EVEN DOT	Reading the pairs of even and odd numbered.
ODD DOT	Dot bits out in parallel. This feature is used in low resolution graphics. When serial mono dot stream is used (alpha and high resolution) EVENDOT and ODD DOT are multiplexed in PAT 024 p.12
CP 50	20 MHz (50 nsec) dot clock.



DOT SHIFTER & COUNTER & DOT CLOCK

CPU755 CPU756

84 12 06 RGA

<u>Signal</u>	<u>Description</u>
DOT *	In low resolution graphics equal to ODD DOT else multiplex between ODD DOT and EVEN DOT on basis of PHASE. In alpha mode DOT* is off in case of BLANK and inverted in case of CRVVD.
-WRTDS	When the PALETTE is read and the contents are loaded into the Register pos. 80, programmed write pulses are gated off. When low Resolution Graphics are displayed, programmed writes to the Palette are dummy, in other cases the write pulses are long enough to write the Palette even if interrupted in the middle by a read.
PAT 024	
PIN 17	PallRD controls the address multiplexer for the Palette (PS 0-4)
DOT*	is delayed one clock period before controlling the dot selector in pos. 100. This dot selector selects the high or low order four bits from the palette register and presents them (via a synchronizing register) to the monitor as
B	Blue
G	Green
R	Read and
I	Intensity signals

PAL16RA
PAT024

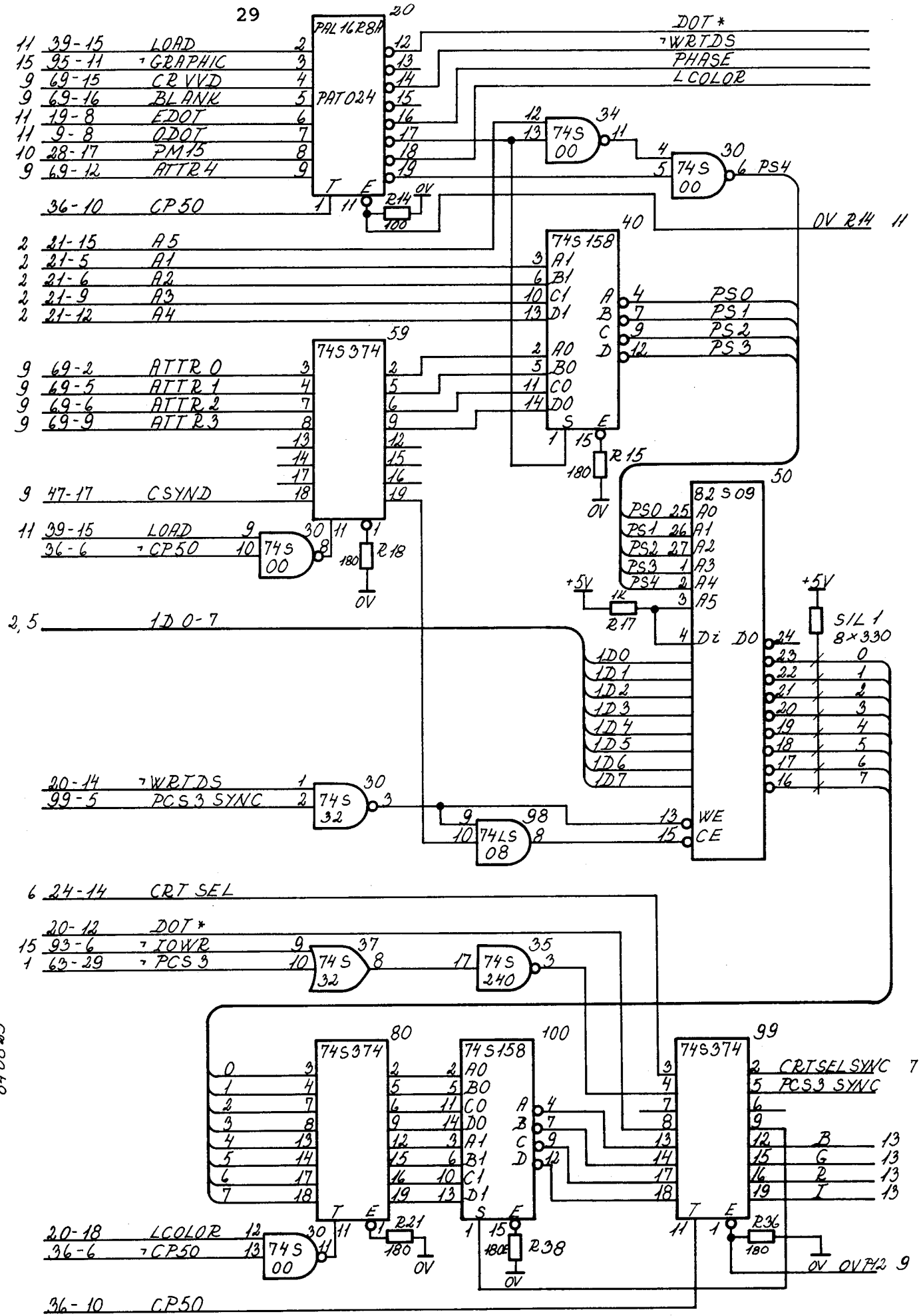
PAL DESIGN SPECIFIKATION
PKA 830728

CRT DOT GENERATOR

CP50 LOAD /GRAPH CRVVD BLANK EDOT ODOT PM15 ATTR4 GND
/OE DOT NC /WRTDS /ATTB4 PHASE /PALLRD LDCOL /COLSEL4 VCC

/PHASE := /LOAD*PHASE + LOAD*/GRAPH + LOAD*/ATTR4	PALLRD := GRAPH*ATTB4 + LOAD + PALLRD*/LDCOL
/DOT := BLANK*/GRAPH*/CRVVD + /BLANK*PHASE*/GRAPH*/EDOT + /BLANK*PHASE*/GRAPH*/CRVVD*/EDOT + /BLANK*PHASE*/GRAPH*/CRVVD*EDOT + /BLANK*/PHASE*/GRAPH*/ATTB4*/ODOT + /BLANK*/PHASE*/GRAPH*/ATTB4*/DOT + /BLANK*/PHASE*/GRAPH*/CRVVD*/ODOT + /BLANK*/PHASE*/GRAPH*/CRVVD*ODOT	/LDCOL := LDCOL + /LDCOL*/GRAPH*/PALLRD + /LDCOL*/ATTB4*/PALLRD + GRAPH*ATTB4*/PHASE
ATTB4 := /LOAD*ATTB4 + LOAD*ATTR4	COLSEL4 := GRAPH*ATTR4* LOAD*PM15 + PALLRD*GRAPH*ATTB4*/LOAD*ODOT + /GRAPH*ATTR4* LOAD + PALLRD*/GRAPH*ATTB4*/LOAD
	WRTDS := LOAD + PALLRD

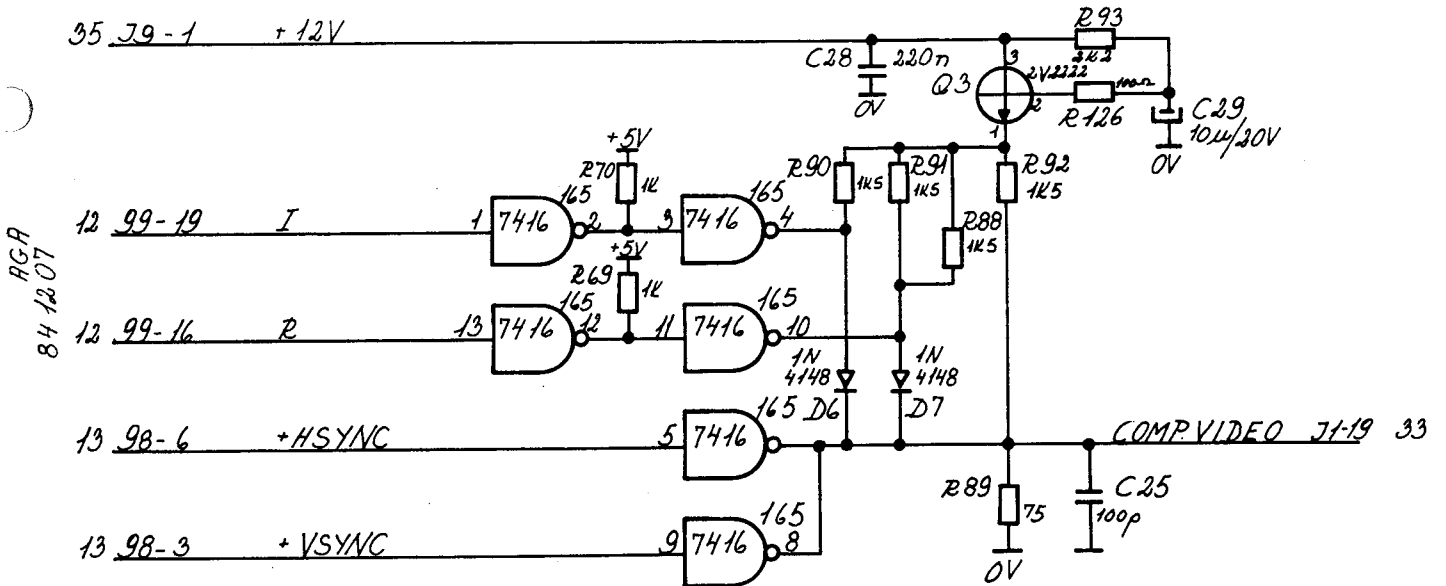
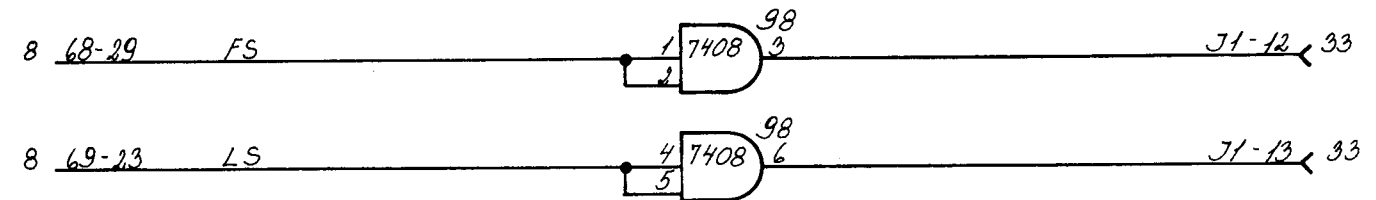
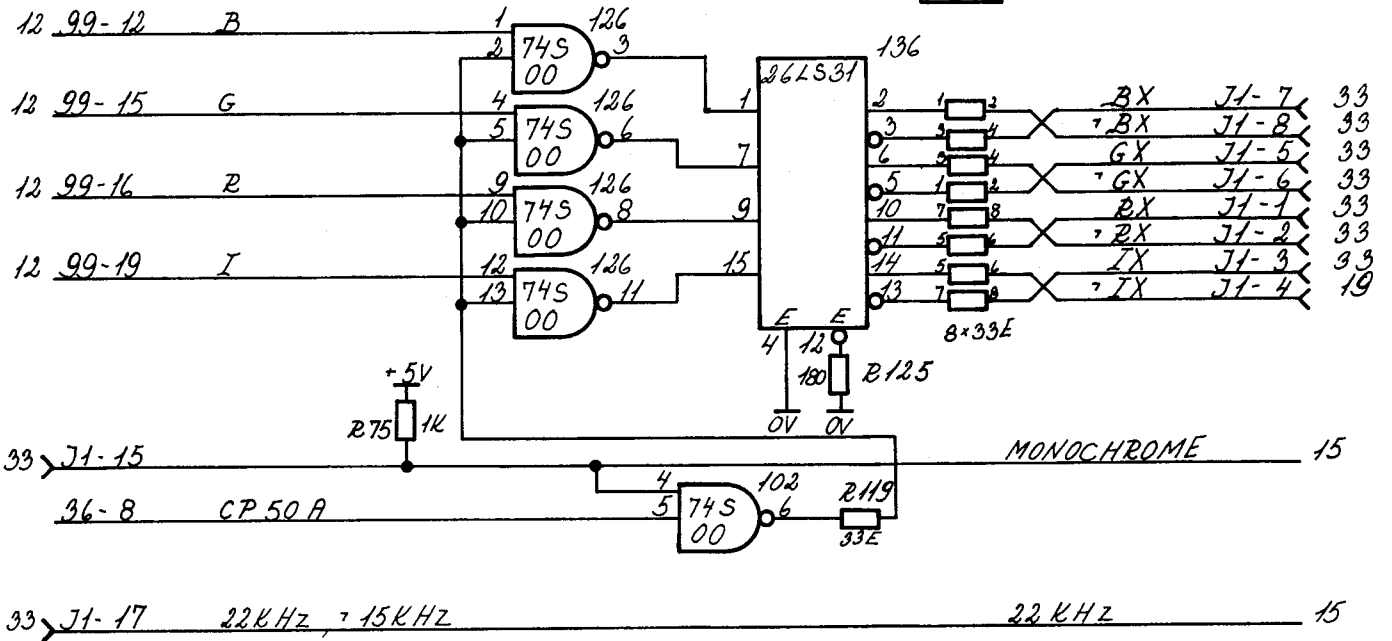
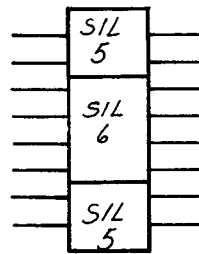
DESCRIPTION:



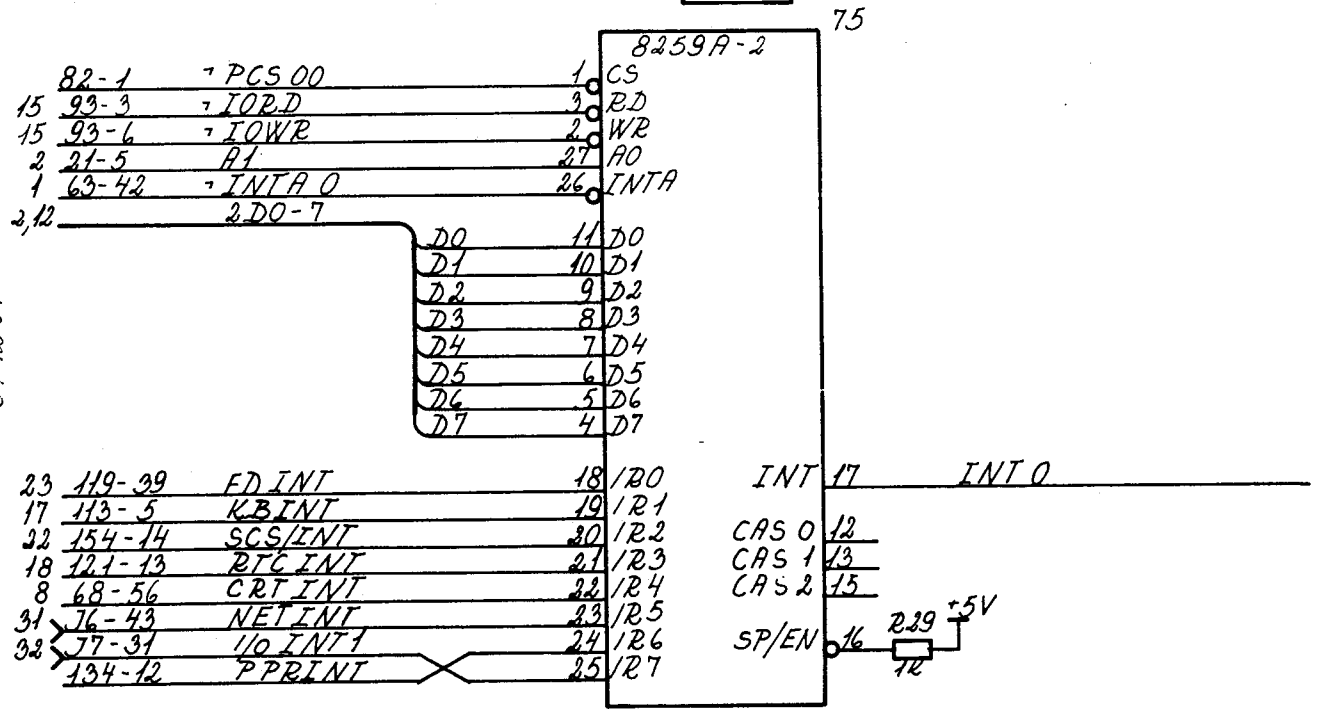
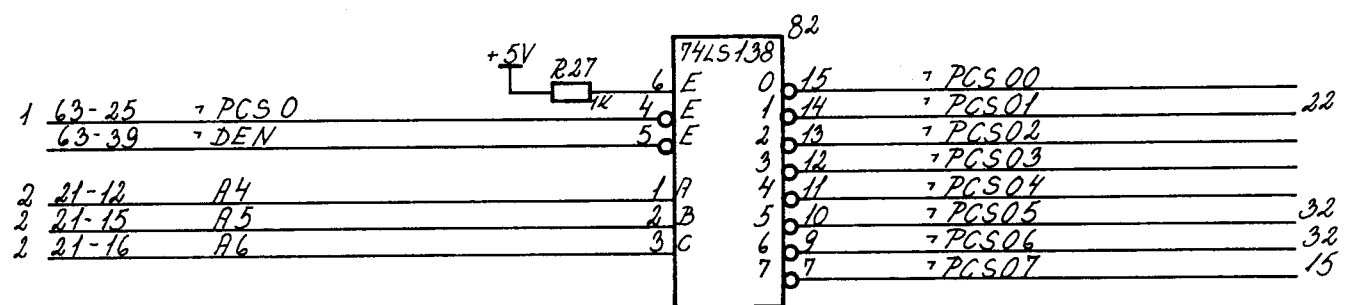
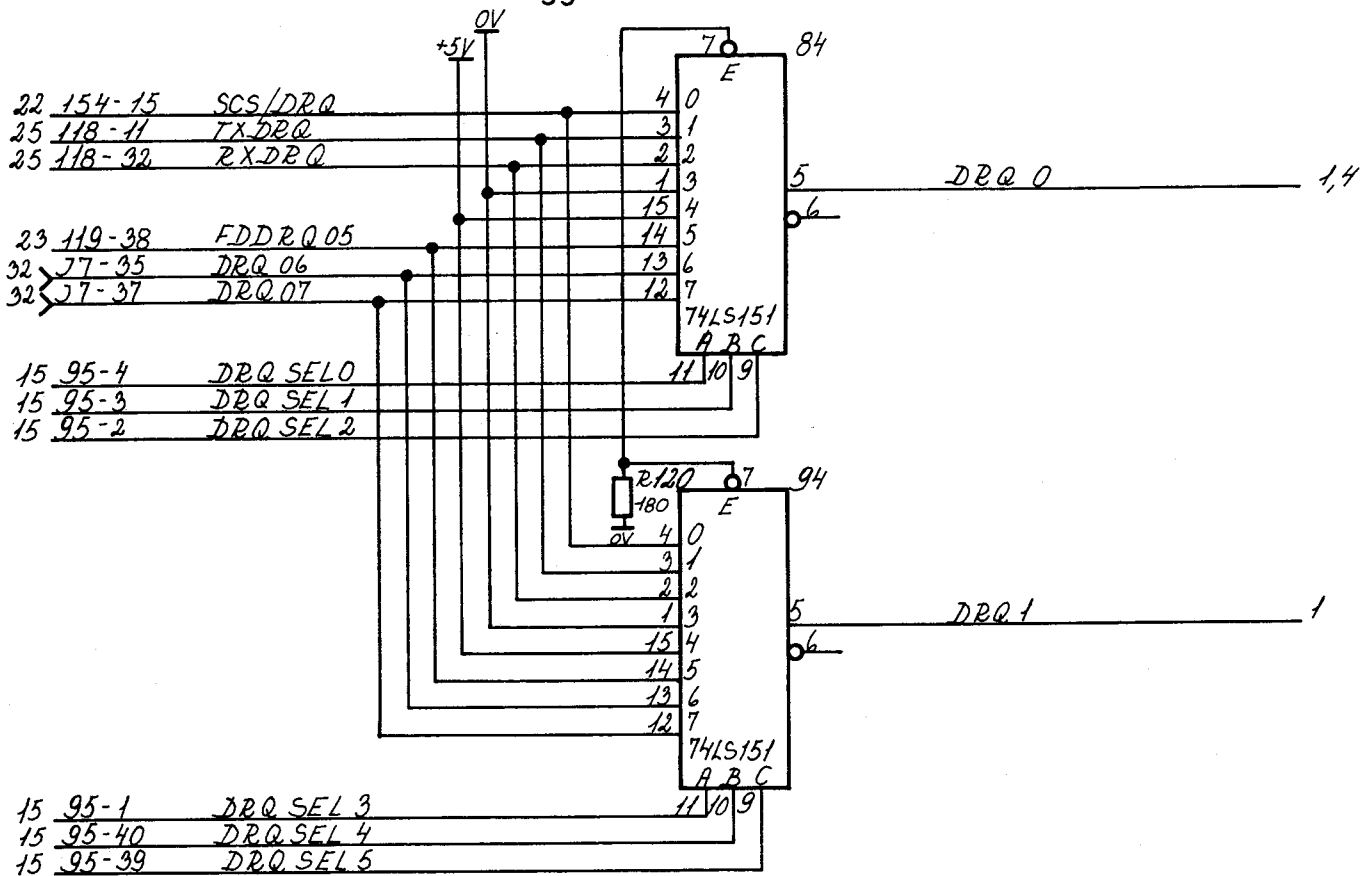
AGA
840829

CPU755 CPU756 COLOUR & ATTRIBUTE CONTROL

<u>Signal</u>	<u>Description</u>
Bx throughq	These signals are balanced video signals for Blue, Green, Red and intensity.
Ix	In the case no colour monitor is connected, the video signals are chopped to create a uniform horizontal and vertical characteristic on the screen.
22 KHz	This signal is grounded in the plug, in the case a television monitor is connected, and is read by the software on the input port p.15.
FS	Framesync to monitor.
LS	Line sync to monitor (also used to start refresh cycles in memory).
COMP VIDEO	Composite video signal.



<u>Signal</u>	<u>Description</u>
DRQ 0	Data channel Request 0. Arranged to have higher priority than the coprocessors.
DRQ 1	Has lower priority than the coprocessors. This priority is established partly in the CPU and partly in PAT 059 on page 4.
PCS00 to PCS07	Are further decoding of the Peripheral Chip Select output no. 0 from the CPU. They are addressed as IO ports in the address ranges: Peripheral:
	PCS00: 0 to E 8259
	PCS01: 10 to 1E SCSI bus
	PCS02: 20 to 2E Keyboard
	PCS03: 30 to 3E 8274
	PCS04: 40 to 4E
	PCS05: 50 to 5E Sound generator
	PCS06: 60 to 6E I/O Xpansion
	PCS07: 70 to 7E 8255
INT0	Interrupt input to CPU.

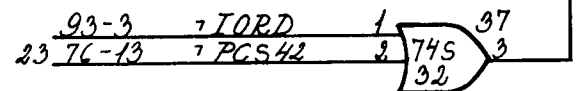
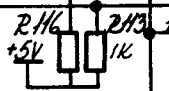
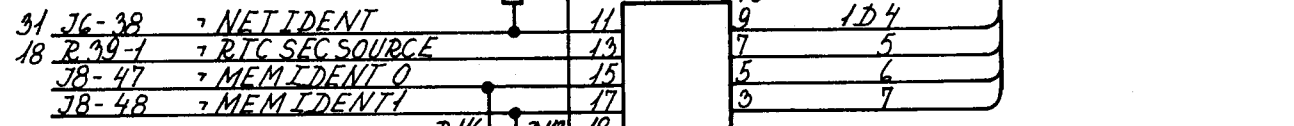
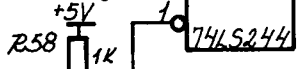
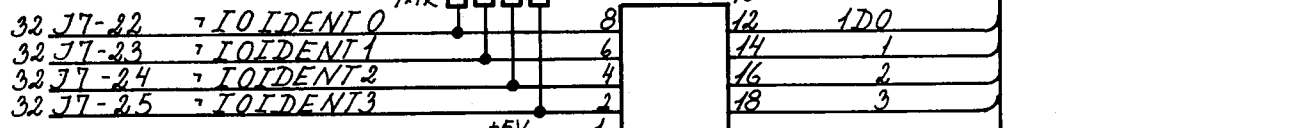
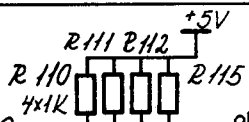
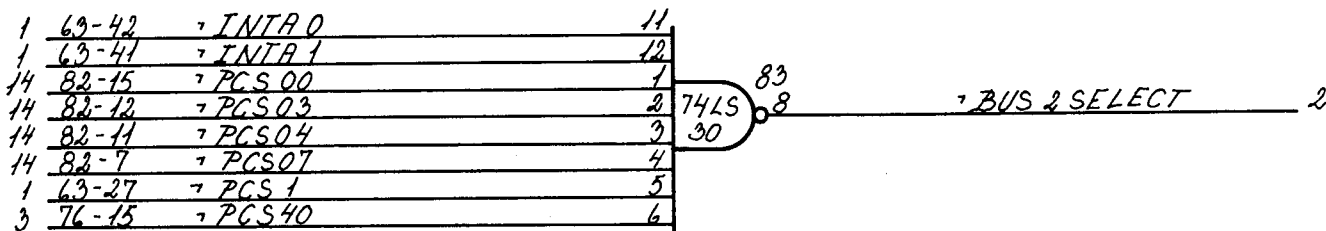
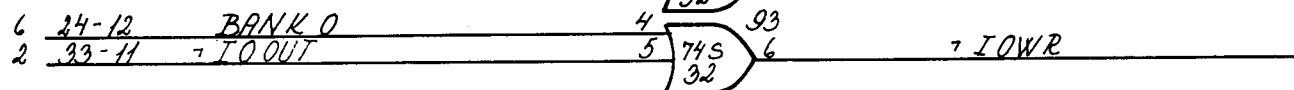
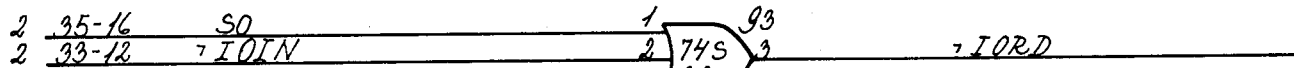
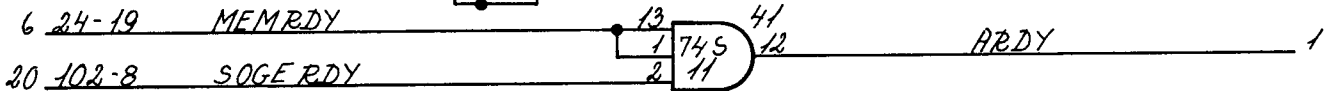
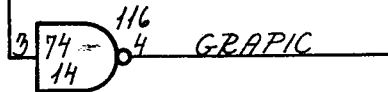
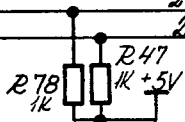
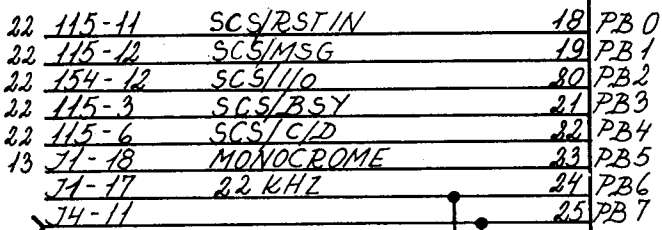
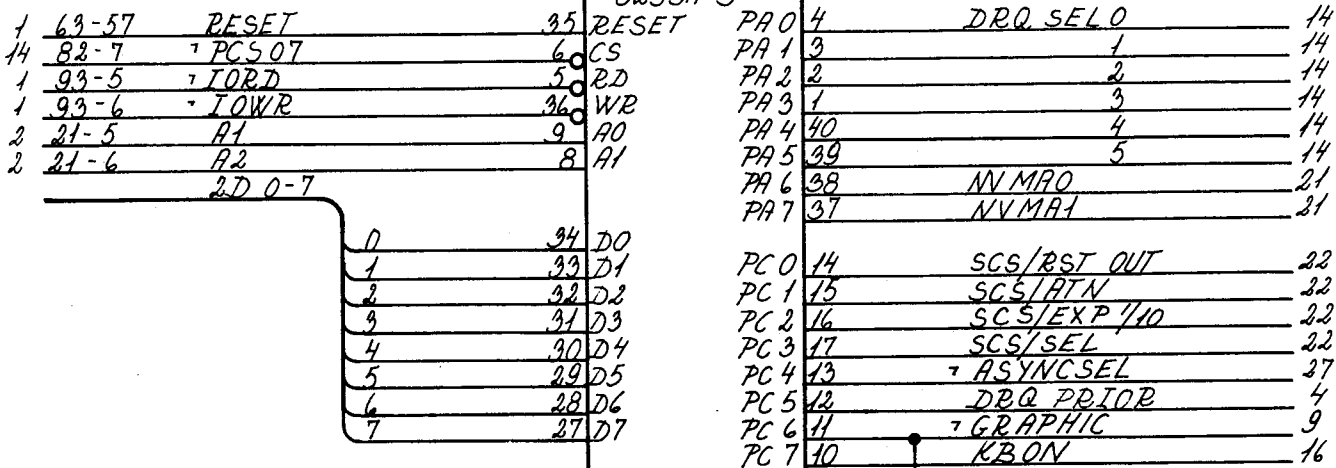


AGA
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DMA SELECTORS, PCS DECODER, INTERRUPT CONTROLLER

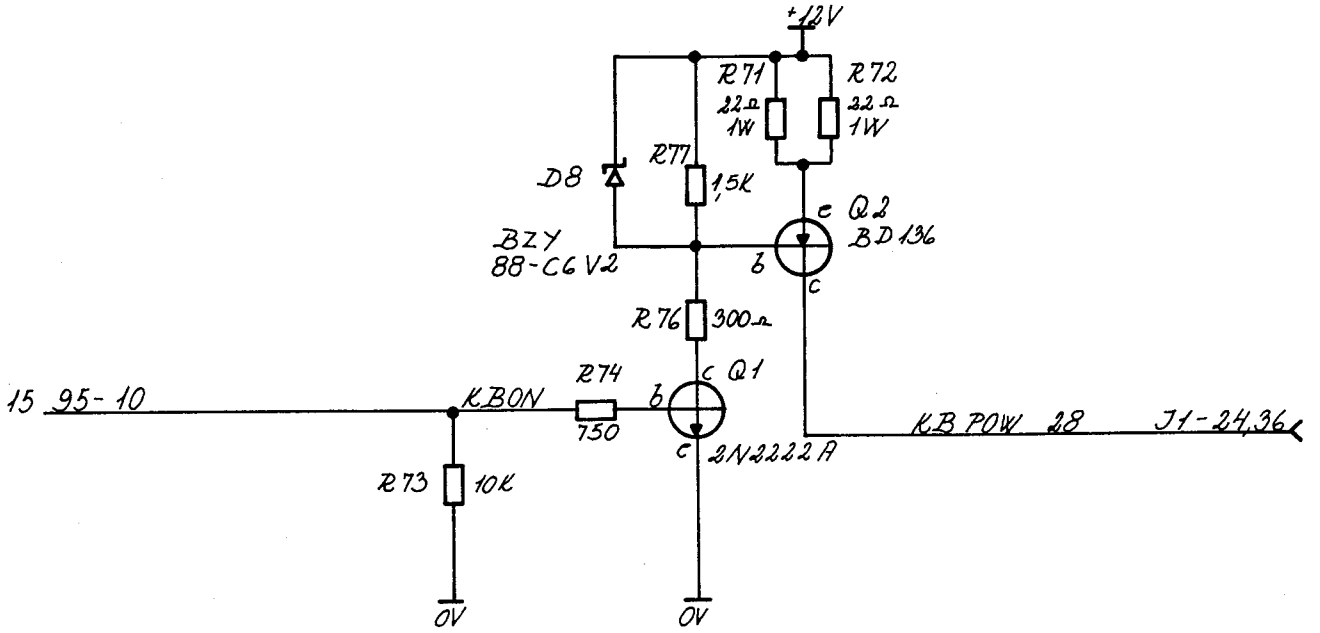
<u>Signal</u>	<u>Description</u>
DRQ SEL 0-5	Selector bits for selecting DMA channel users. DRQ SEL 0-2 select the user device for DMA channel 0 DRQ SEL 3-5 select the user device for DMA channel 1
SCSIRSTOUT	These are control signals to be transmitted on the SCSI bus
SCSIATN	
SCSISEL	
SCSI EXP I/O	Indicates expected direction of SCSI-datatransfer
-ASYNC SEL	Selector for clock input to 8274 channel A.
-GRAPHIC	CRT mode selector.
KBON	Power on control for the keyboard.
ARDY	Is the request signal to the processor for insertion of wait state.
-IOWR -IORD	Write and Read signal generated by I/O instructions.
BUS 2 SELCT	When active, 2D 0-7 are used for I/O transfer (A MOS device is addressed).
1D 0-7	Connection of the configuration sense port to the 1D Bus.

8255A-5



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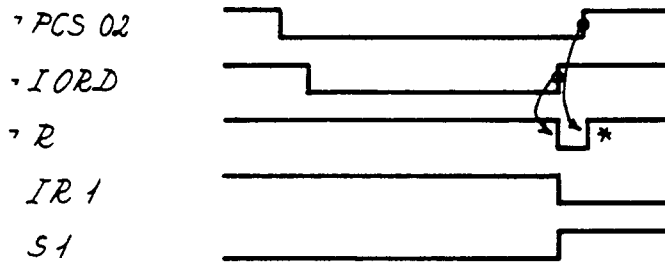
<u>Signal</u>	<u>Description</u>
KB POW	Power supply to keyboard. When the keyboard is connected the voltage on this line is 8-10 V.
KB ON	Turnes on the keyboard.



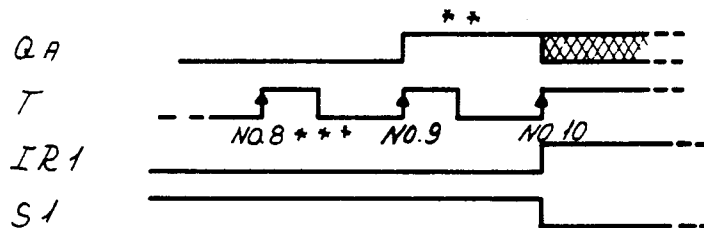
RGA
840831

<u>Signal</u>	<u>Description</u>
KB CLOCK IN	This signal is the clock information supplied by the keyboard.
KB DATA IN	This signal is the data information supplied by the keyboard.
IR1	This interrupt request is asserted when a character is received. It is deasserted when the character is read.

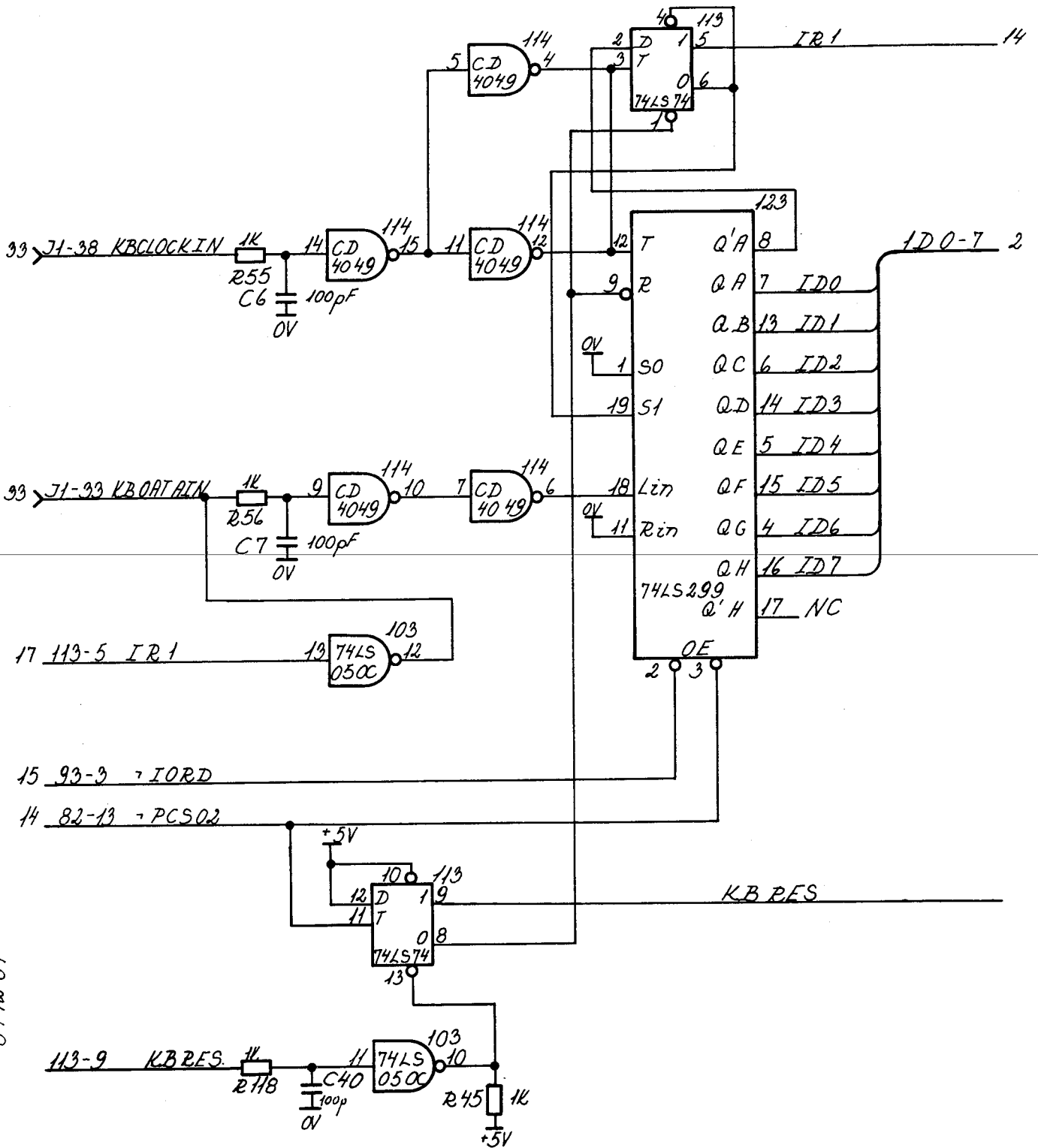
READING OF POS. CODE



LATCHING OF DATA

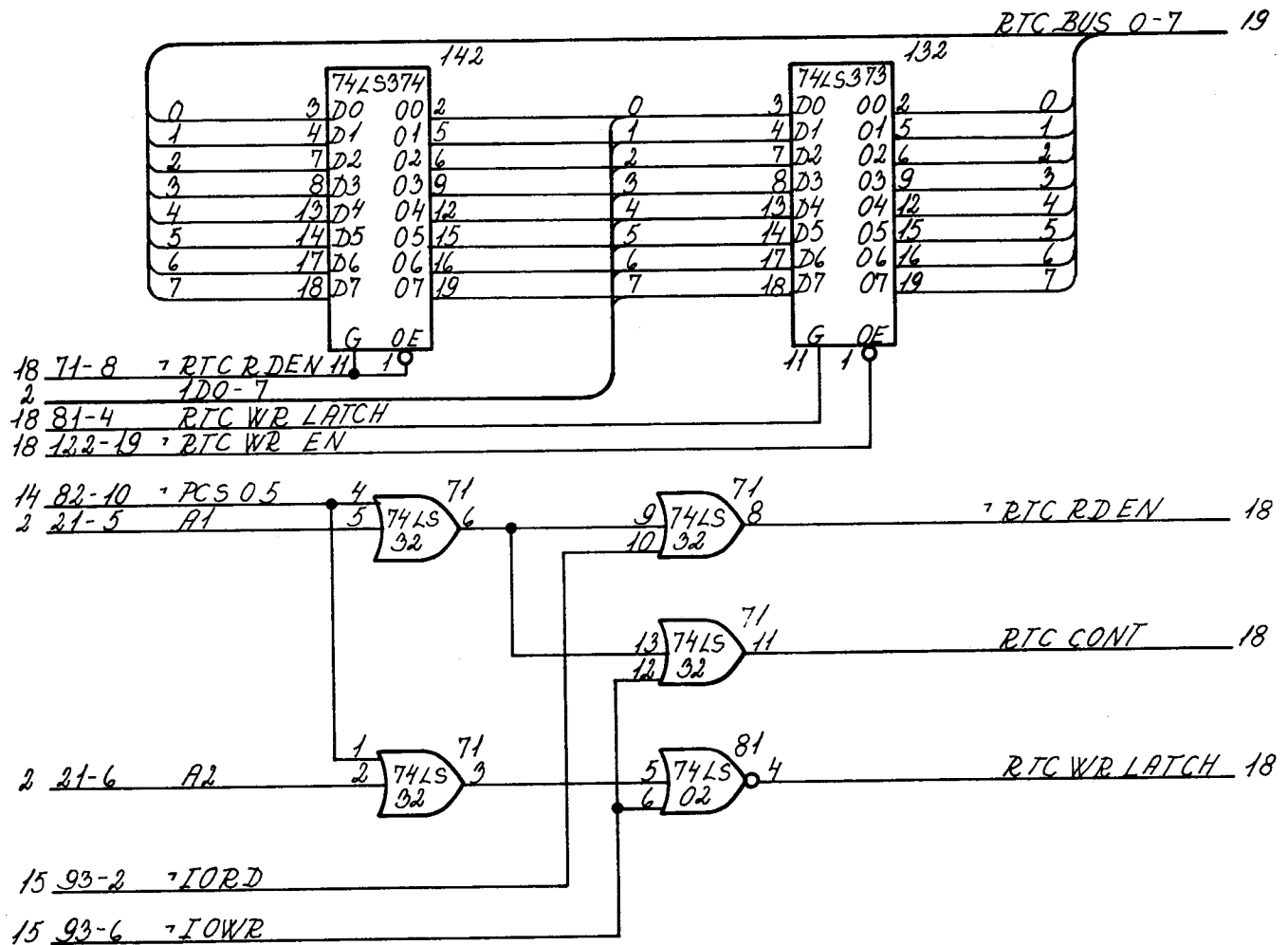
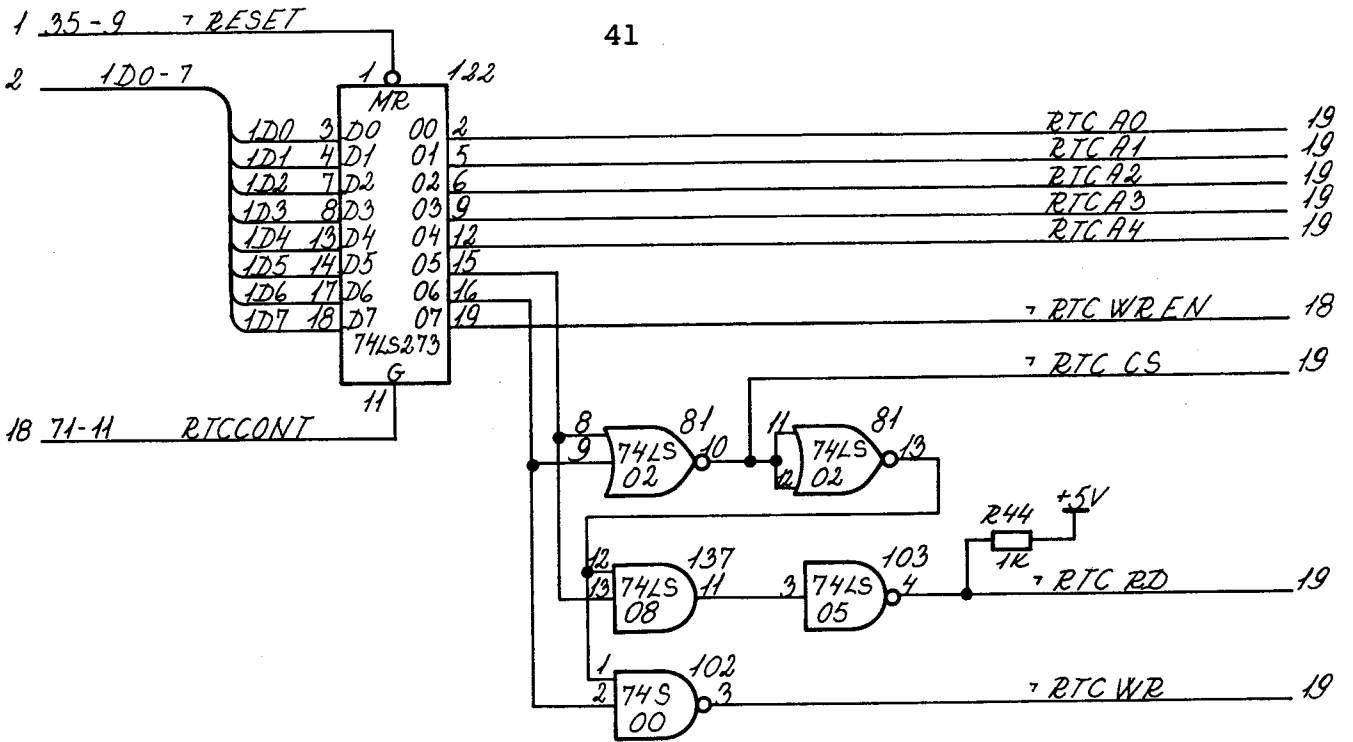


- * RESET PULSE
- ** START BIT FROM KEYBOARD
- *** NUMBER OF CLOCK PULSES FROM KEYBOARD.



841207

<u>Signal</u>	<u>Description</u>
RTC CONT	Latches the control information passed to the Real Time Clock (RTC).
-RTC RD EN	Enables data output from RTC.
-RTC WR EN	Enables data input to RTC.
RTC WR LATCH	Latches data input to RTC.
RCT A0-4	Address information transferred to the CRT.
-RTC RD	Read signal used to control the RTC.
-RTC WR	Write signal used to control the RTC.
-RTC CS	Chip select signal used to control the RTC.
RTC BUS 0-7	Local data bus used by the RTC and the sound generator.



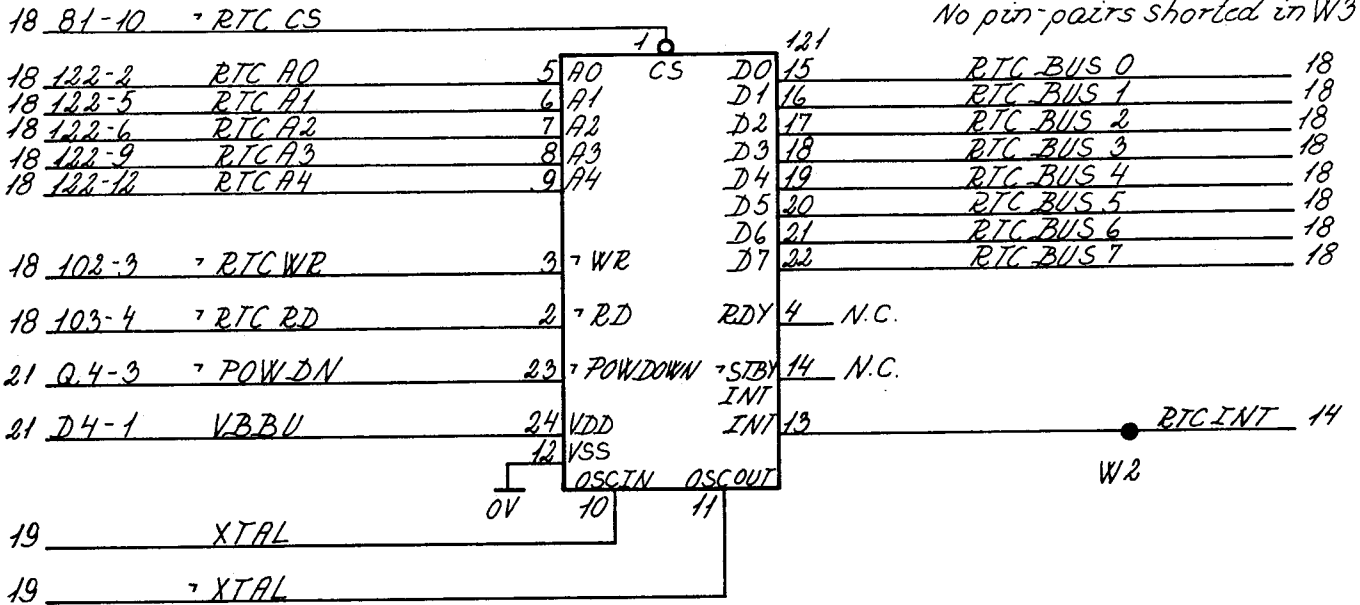
<u>Signal</u>	<u>Description</u>
VBBU	Battery supported power supply.
-POWDN	Indicates the power down condition.

MM58167(NSC)

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FIRST SOURCE

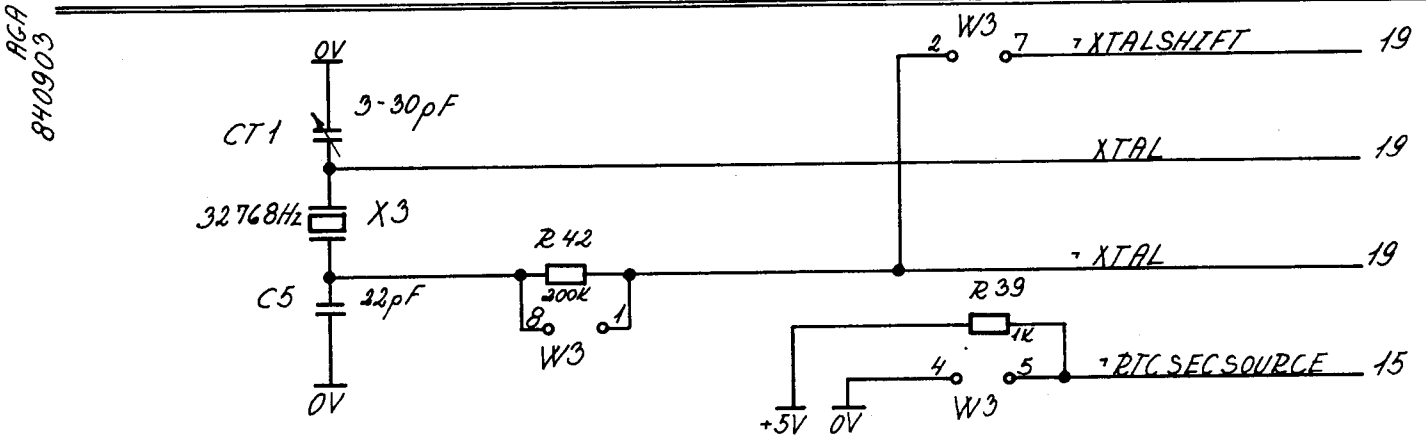
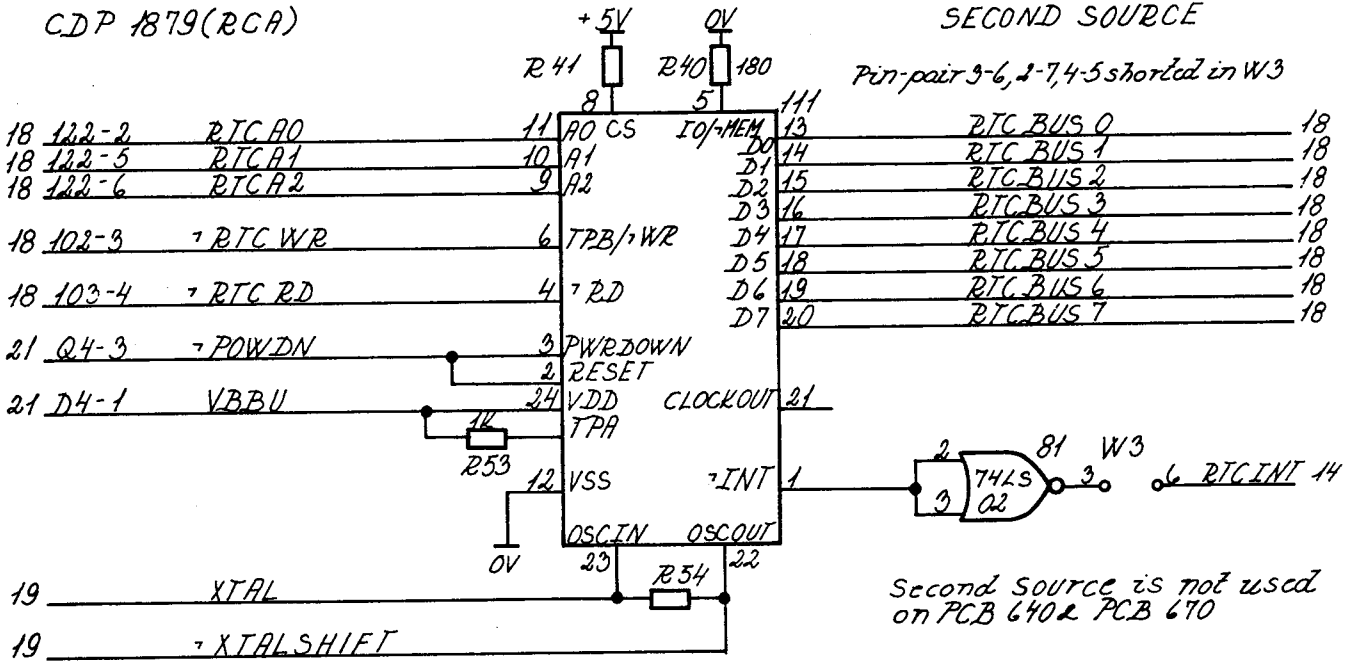
No pin-pairs shorted in W3



CDP 1879(RCA)

SECOND SOURCE

Pin-pair 3-6, 2-7, 4-5 shorted in W3

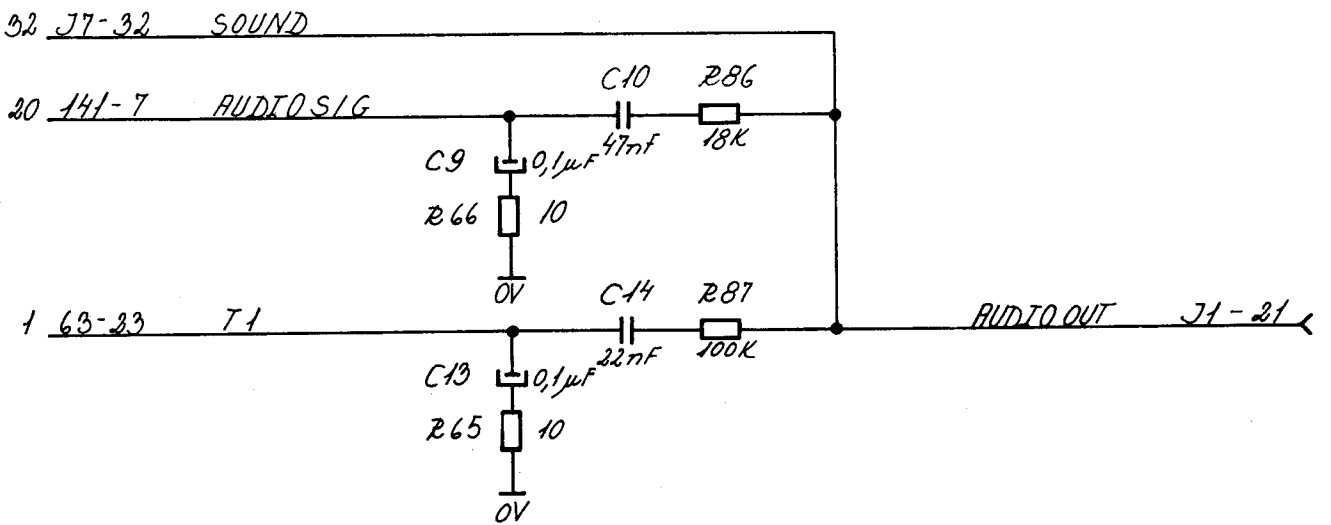
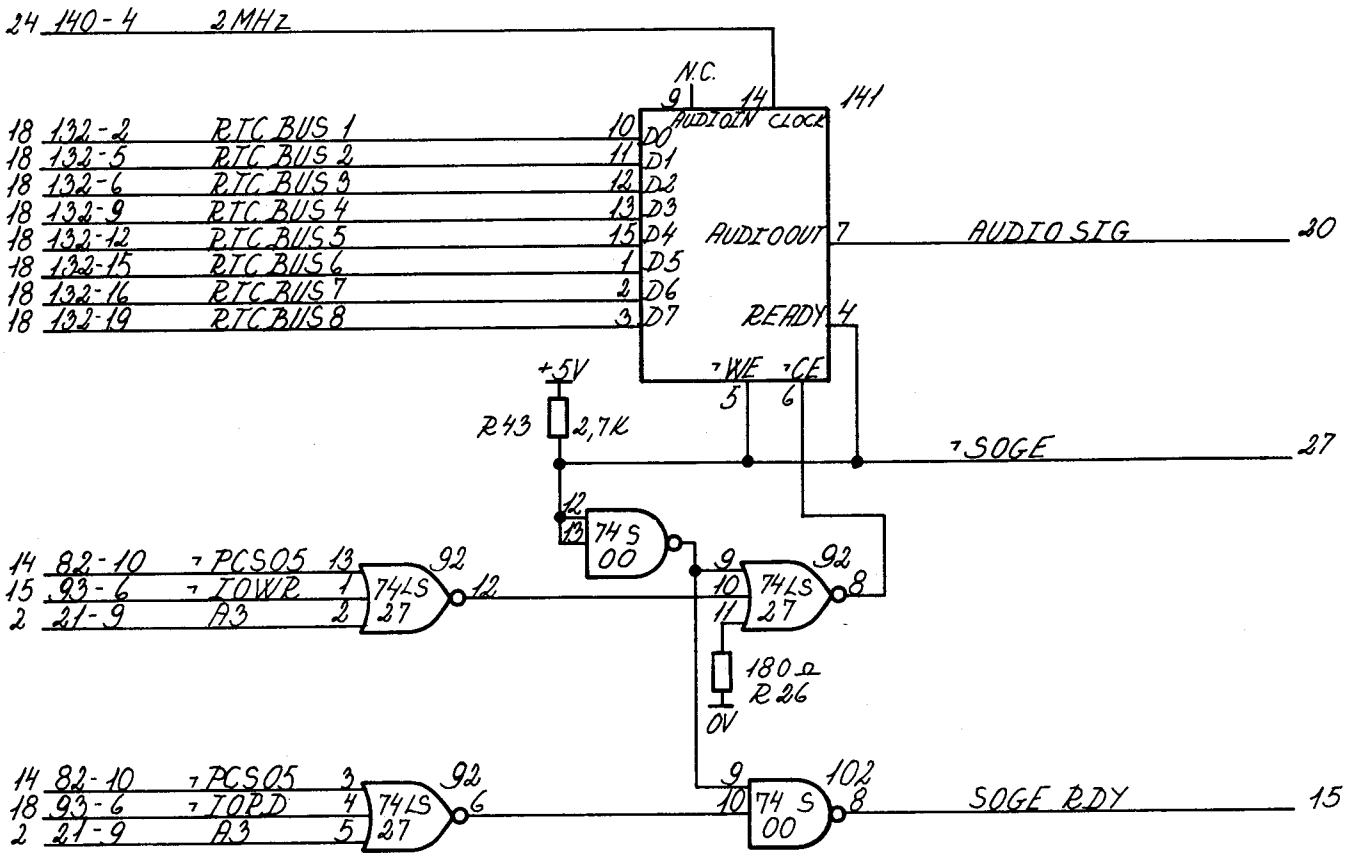


REAL TIME CLOCK (RTC) FIRST & SECOND SOURCE

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CPU755 CI

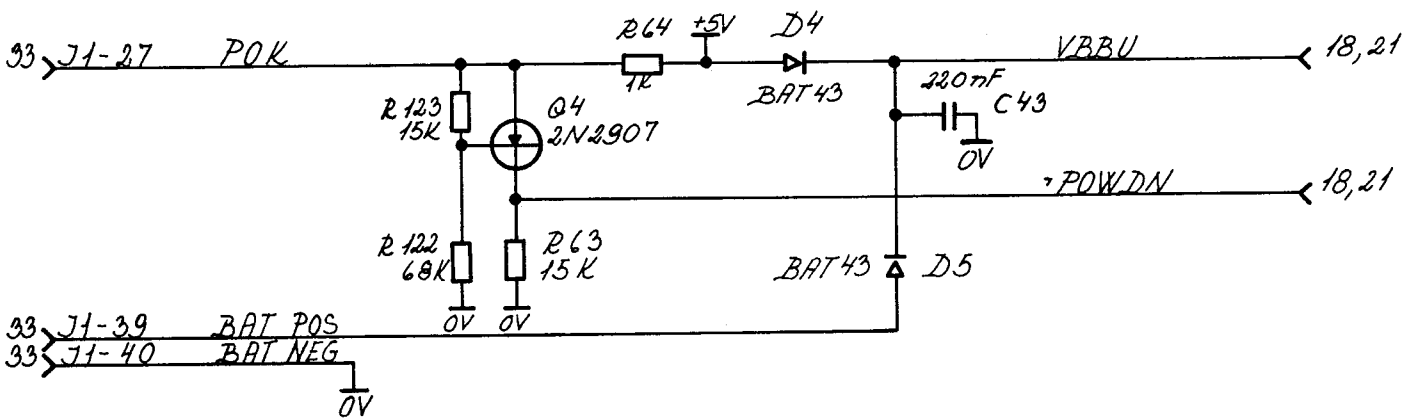
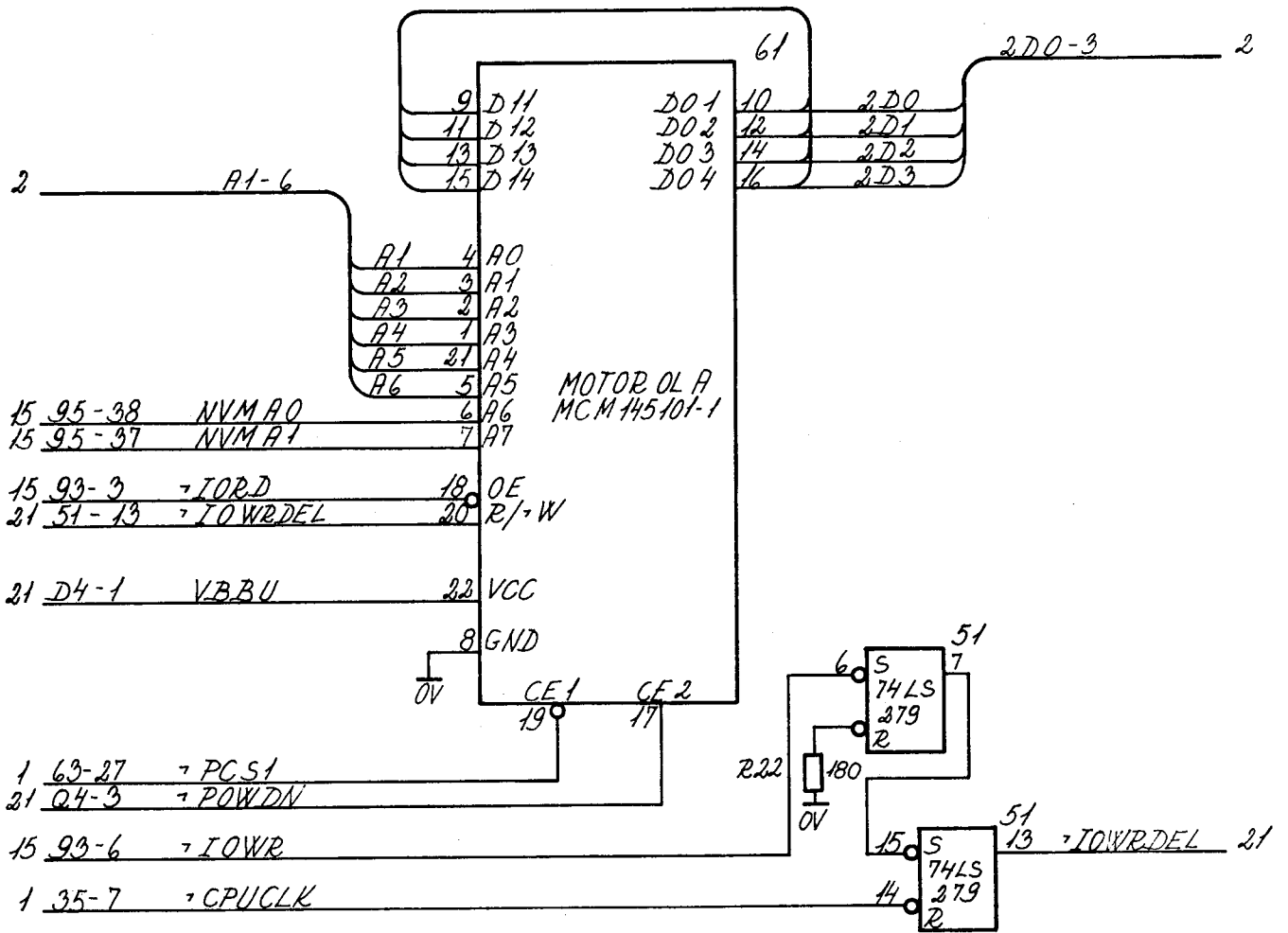
<u>Signal</u>	<u>Description</u>
RTC BUS 0-7	Local databus used by the RTC and the sound generator.
-SOGE	Indicates the presence of the sound generator.
AUDIO SIG	Analog audio output.
SOGE RDY	Indicates the READY-condition of the sound generator.
AUDIO OUT	The analog mixed signal of T1 and AUDIO SIG.



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CPU755 CPU756 SOUND GENERATOR

<u>Signal</u>	<u>Description</u>
POK	Power OK-signal generated by the power supply.
VBBU	Battery supported power supply.
-POWDN	Indicates the power down condition.
-IOWRDEL	Delayed version of the -IOWR signal.
BAT POS	Back-up battery connection.
BAT NEG	OV.



This circuit used on later PCB's.

<u>Signal</u>	<u>Description</u>
-MSG	
-BSY	
-I/O	Input from the SCSI-device.
-C/D	
-REQ	
-ACK	
-ATN	Output to the SCSI-device.
-SEL	
DBSC 0-7	Bidirectional SCSI data bus.
DBSCP	Parity output to SCSI-device.
-RST	Bidirectional Reset Signal.

PAL16L8
PAT0019

PAL DESIGN SPECIFIKATION
THJ 830719

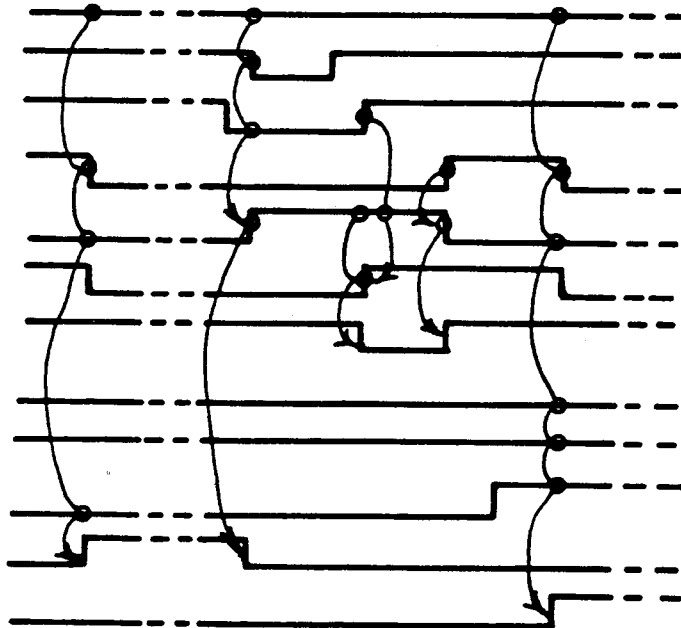
SCSI SUPPORT CIRCUIT

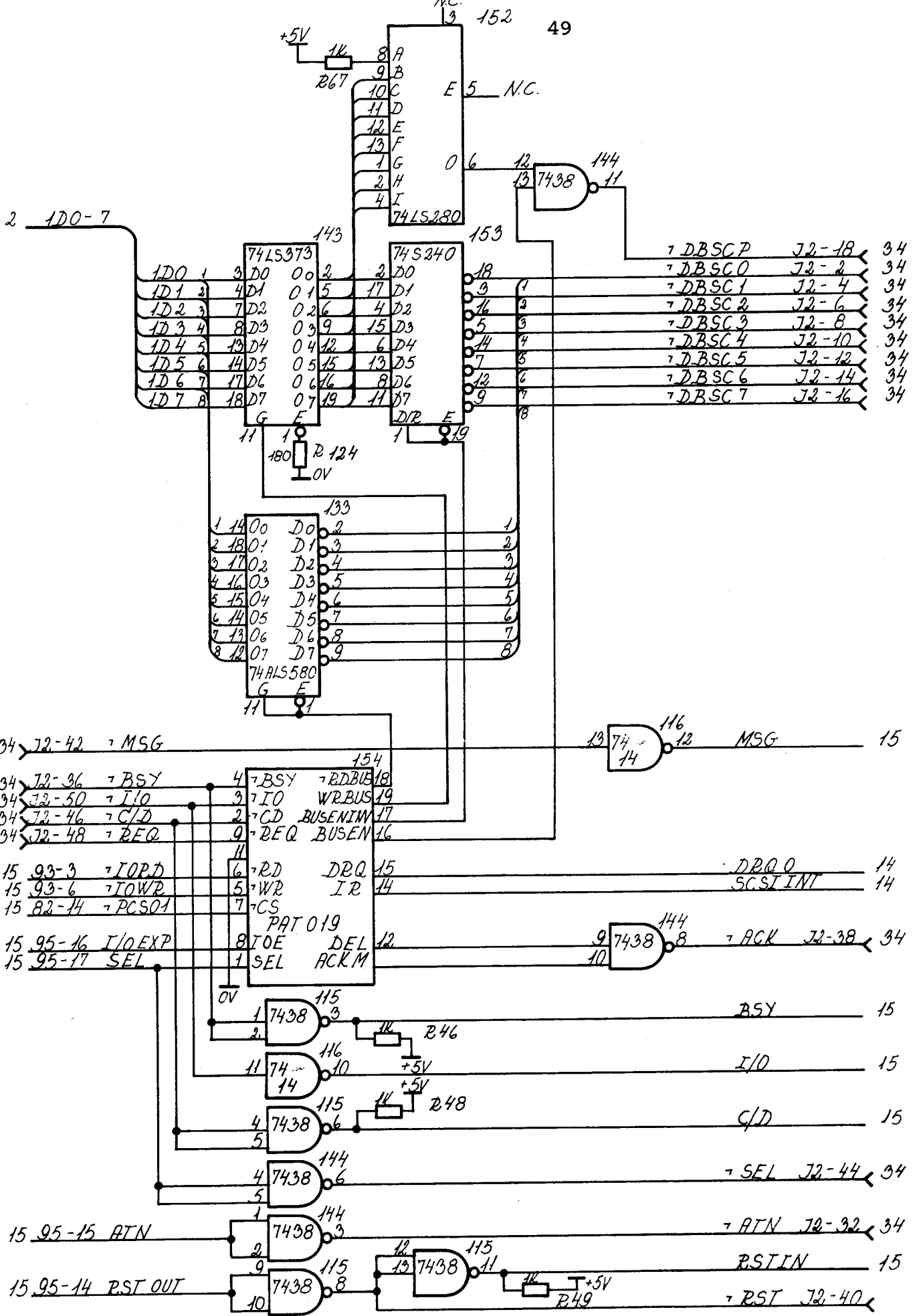
SEL /CD /IO /BSY /WR /RD /CS IOE /REQ GND
NC DEL ACKM IR DRQ BUSEN BUSENINV /RDBUS WRBUS VCC

IF(VCC) /WRBUS = /WR + /CS
IF(VCC) RDBUS = RD*CS
IF(VCC) /BUSENINV = /IO
IF(VCC) /BUSEN = IO
IF(VCC) /DRQ = /IO*IOE + /IOE*IO + /BSY + /REQ + CD + ACKM
IF(VCC) /IR = /BSY + /REQ + IO*IOE*/CD + /IO*/IOE*/CD + ACKM
IF(VCC) /ACKM = /WR*/RD*/ACKM + /BSY + /REQ + /CS*/ACKM
IF(VCC) /DEL = REQ*/ACKM + REQ*CS

DESCRIPTION:

7 BSY
7 IORD or *7* IOWR
7 PCS0 1
7 REQ
ACKM
DEL
7 ACK
7 I/O
I/O EXP
7 C/D
IR
DRQ





CPU755 CPU756 SCSI/SASI INTERFACE

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