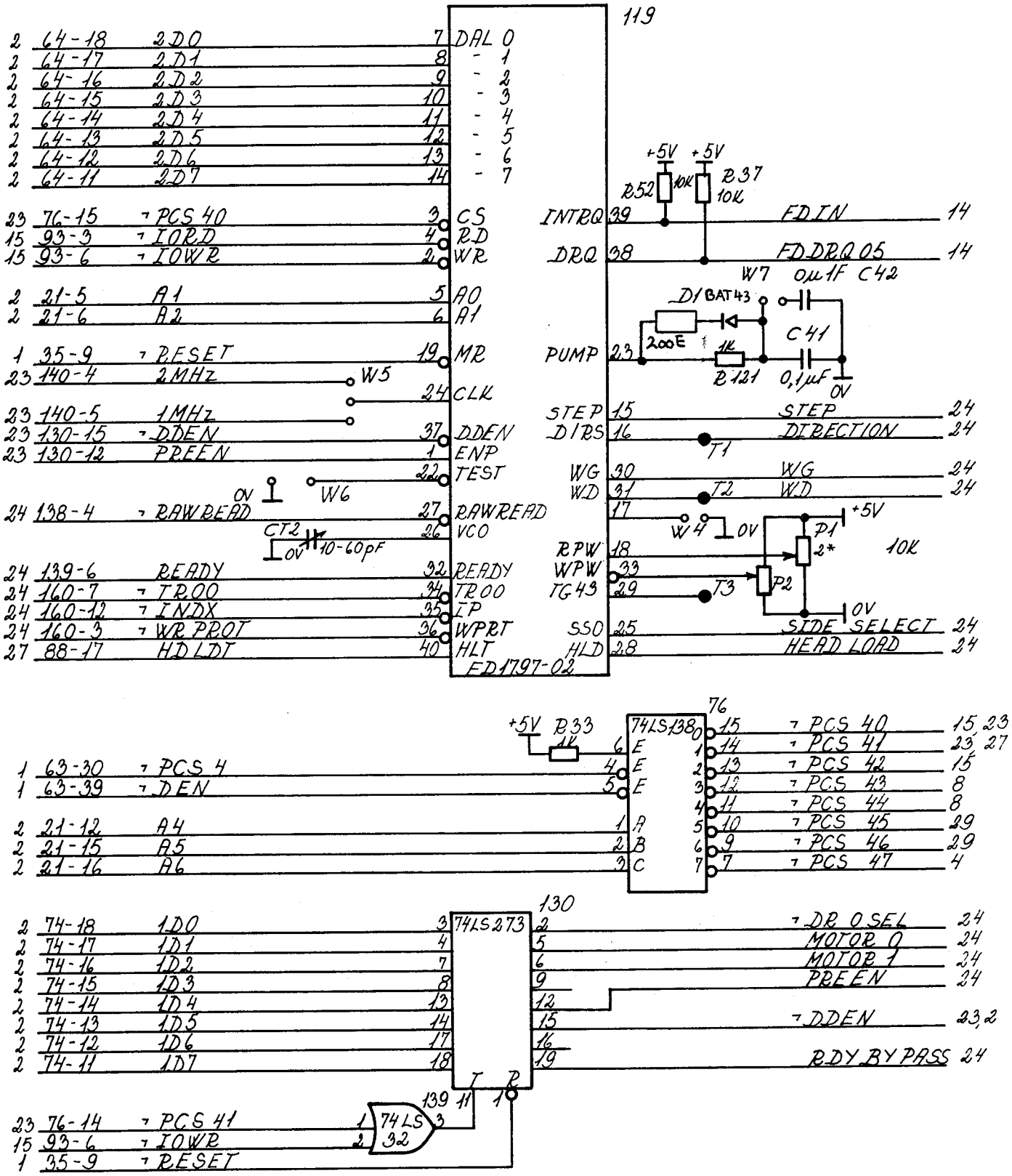
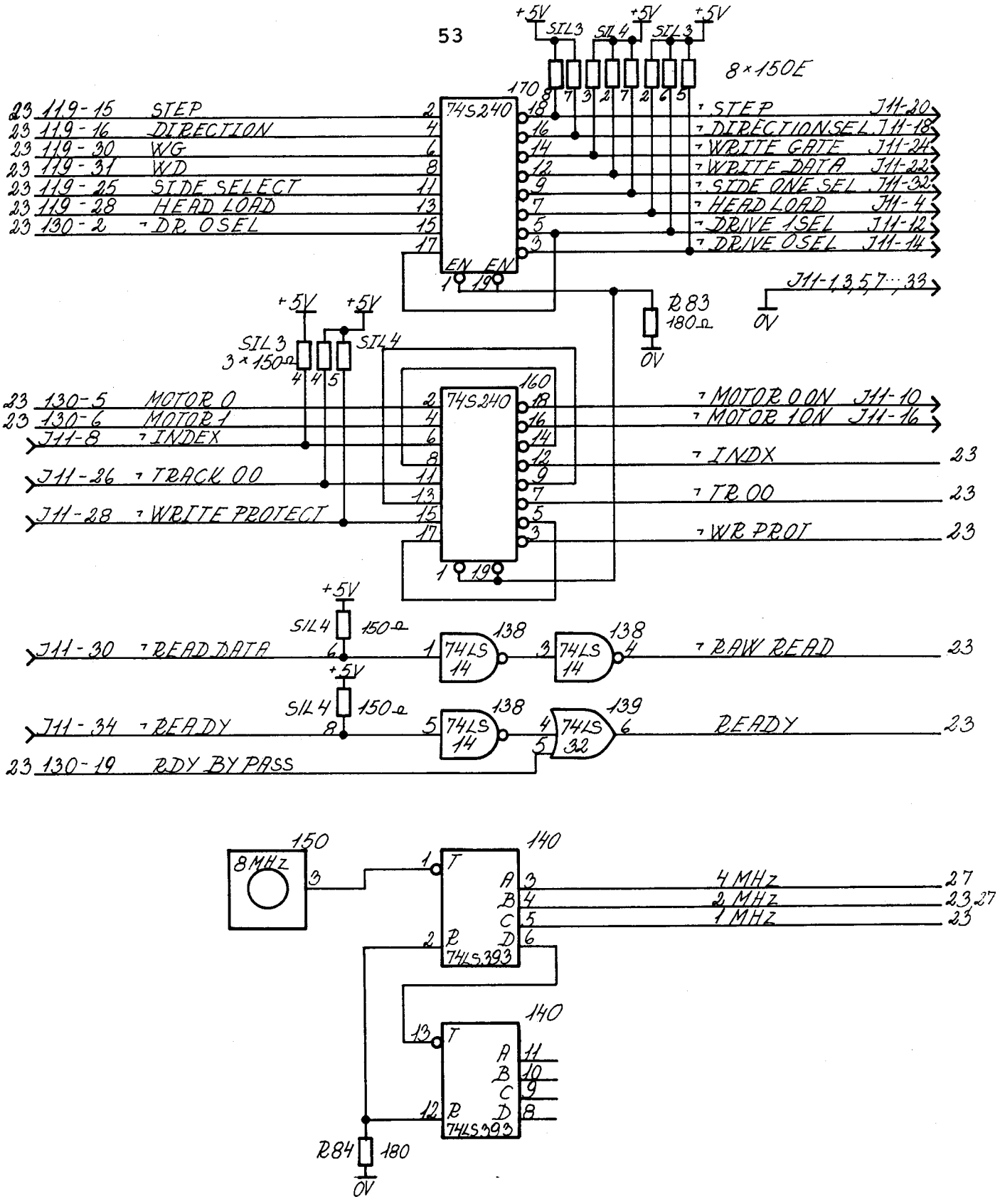
WD : 2797-2

SIEMENS : SAB 2797

+5V PIN 21 : 0,25V

PCS 4 : I/O BASE +200 - 27F





AGA 84 10 34

CPU755 CPU756

FLOPPY DISC CONTROLLER BUFFERS
DATA SEPARATOR & WRITE PRECOMPENSATION

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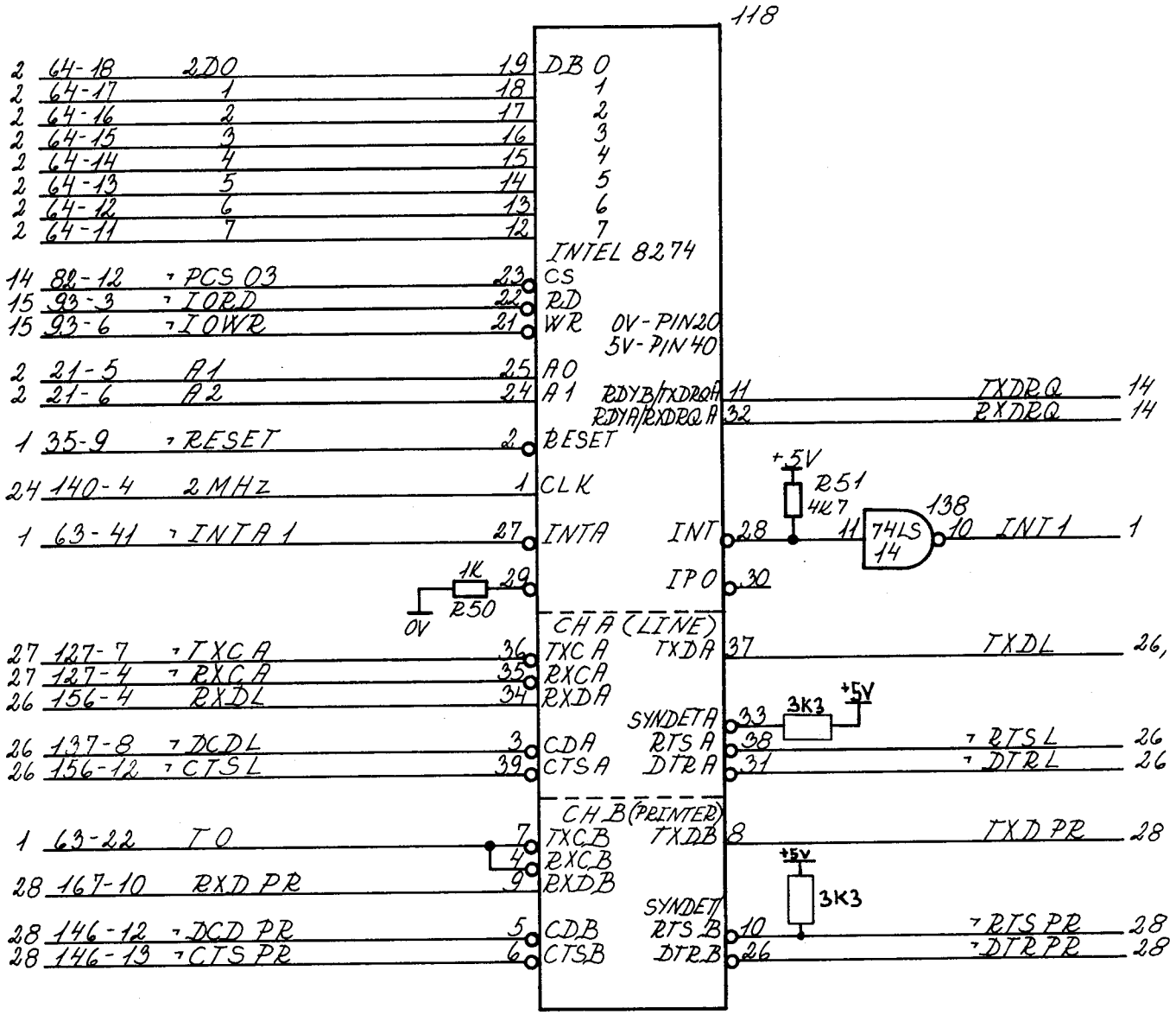
118
INTEL 8274
DB 0
1
2
3
4
5
6
7
CS
RD
WR
0V - PIN 20
5V - PIN 40
A0
A1
RESET
CLK
INTA
INT
IP 0
RDYB/TXDRQA
RDYA/RXDRQA
CH A (LINE)
TXC A
RXCA
RXDA
CDA
CTSA
TXDA
SYNDETA
RTS A
DTR A
CH B (PRINTER)
TXCB
RXCB
RXDB
CDB
CTSB
TXDB
SYNDETB
RTS B
DTR B
2 64-18 2D0
2 64-17 1
2 64-16 2
2 64-15 3
2 64-14 4
2 64-13 5
2 64-12 6
2 64-11 7
14 82-12 ▿PCS 03
15 93-3 ▿IORD
15 93-6 ▿IOWR
2 21-5 A1
2 21-6 A2
1 35-9 ▿RESET
24 140-4 2MHz
1 63-41 ▿INTA 1
1K
R50
0V
+5V
R51
4K7
138
74LS
14
INT 1
TXDRQ
RXDRQ
27 127-7 ▿TXC A
27 127-4 ▿RXC A
26 156-4 RXDL
26 137-8 ▿DCDL
26 156-12 ▿CTSL
TXDL
3K3
▿RTSL
▿DTRL
1 63-22 TO
28 167-10 RXD PR
TXD PR
28 146-12 ▿DCD PR
28 146-13 ▿CTS PR
▿RTS PR
▿DTR PR

AGA 841024

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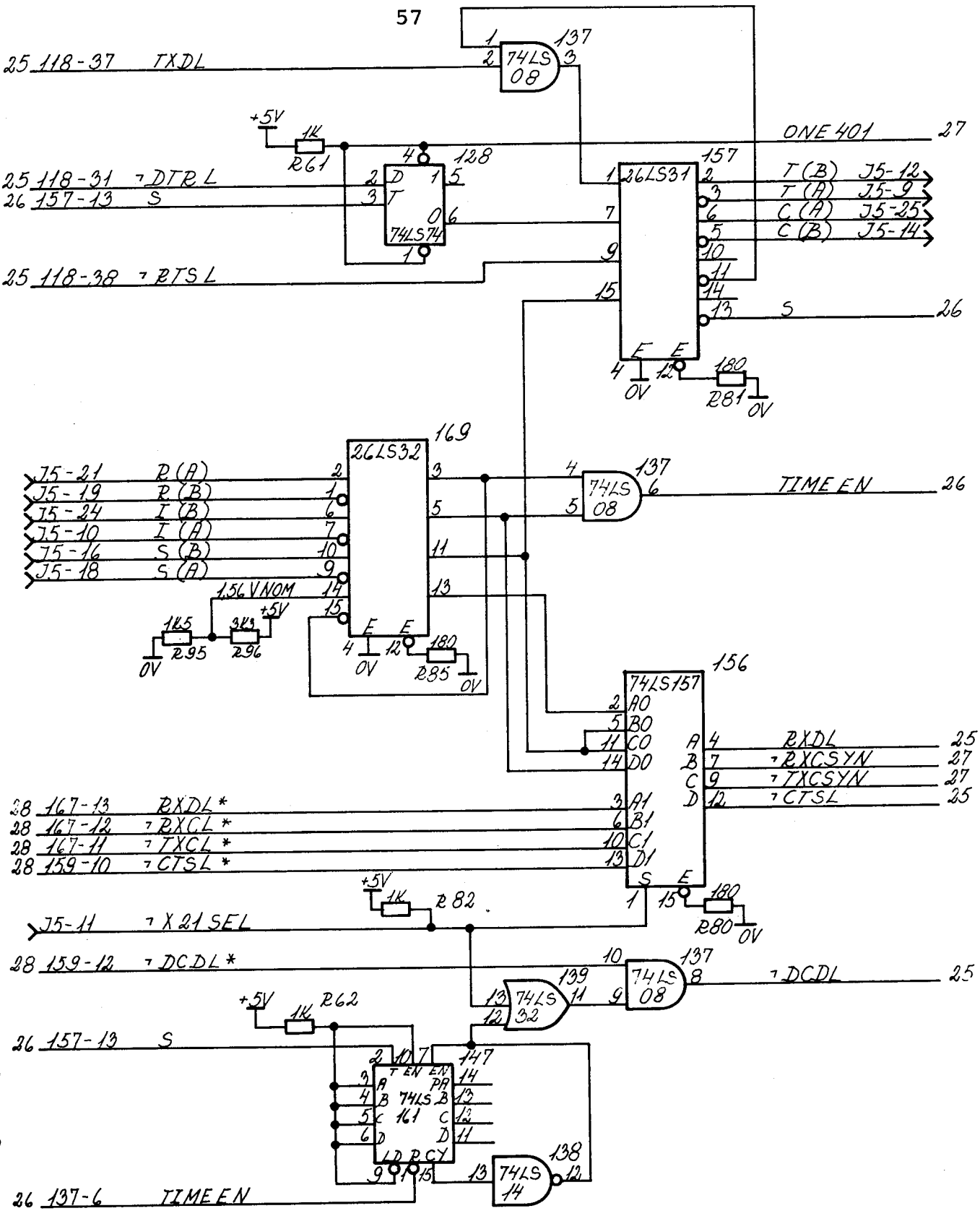
25 118-37 TXDL
137
74LS 08
+5V
1K
R61
ONE 401
27
128
74LS74
25 118-31 ¬DTR L
26 157-13 S
25 118-38 ¬RTS L
157
26LS31
T(B) J5-12
T(A) J5-9
C(A) J5-25
C(B) J5-14
S
26
180
R81
0V
169
26LS32
J5-21 R(A)
J5-19 R(B)
J5-24 I(B)
J5-10 I(A)
J5-16 S(B)
J5-18 S(A)
1.56 VNOM
1K5
R95
3K3
R96
R85
TIME EN
156
74LS157
AO
BO
CO
DO
A1
B1
C1
D1
RXDL
¬RXCSYN
¬TXCSYN
¬CTSL
28 167-13 RXDL*
28 167-12 ¬RXCL*
28 167-11 ¬TXCL*
28 159-10 ¬CTSL*
R82
J5-11 ¬X21 SEL
28 159-12 ¬DCDL*
¬DCDL
139
74LS 32
R62
26 157-13 S
147
74LS 161
138
74LS 14
26 137-6 TIME EN
RGA 84 11 29

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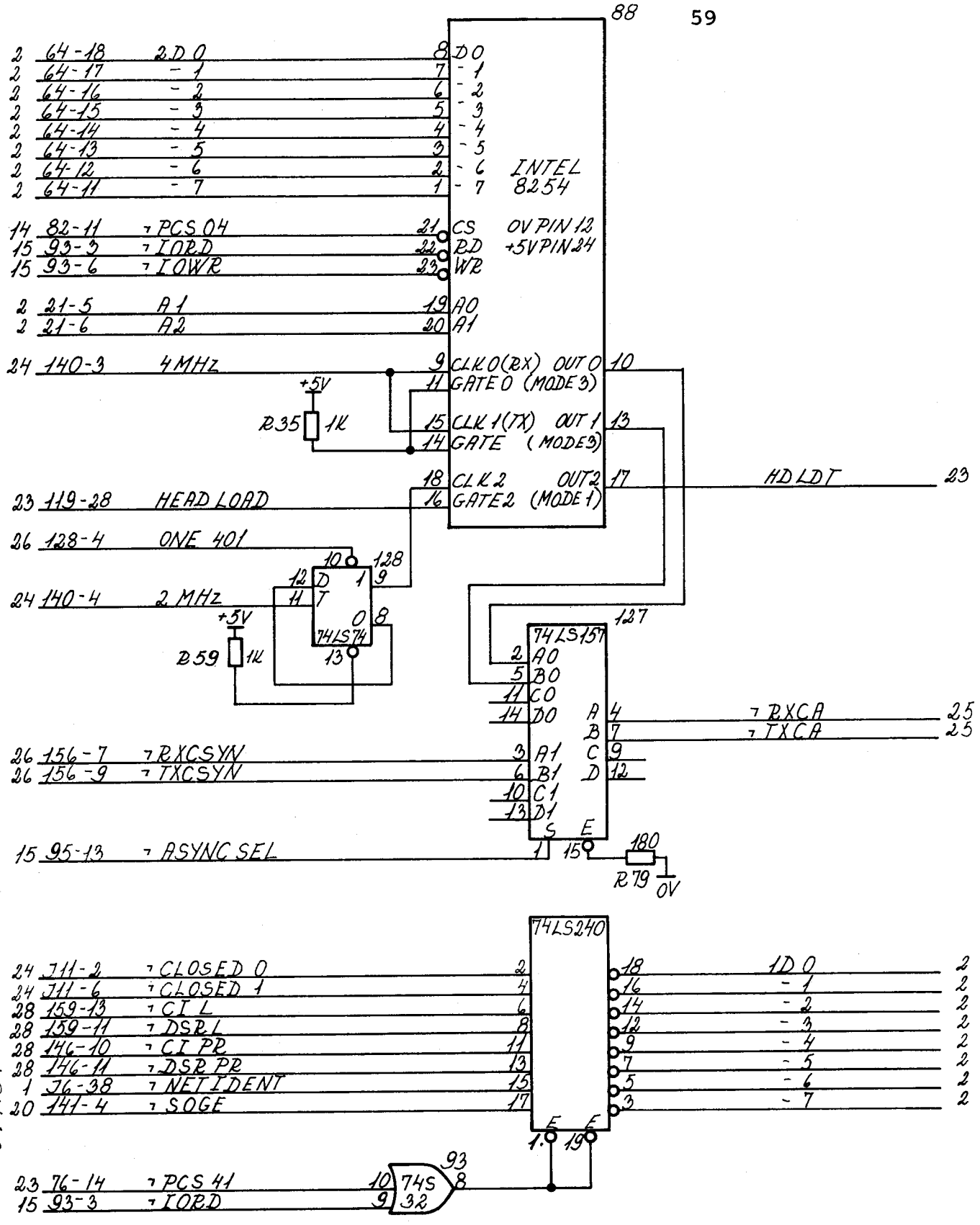
88
INTEL 8254
74LS74
74LS157
74LS240
74S 32
+5V
R35 1K
R59 1K
R79 180
0V
HEAD LOAD
ONE 401
4MHz
2 MHz
ASYNC SEL
RXCSYN
TXCSYN
PCS 04
IORD
IOWR
HDLDT
RXCA
TXCA
CLOSED 0
CLOSED 1
CI L
DSR L
CI PR
DSR PR
NET IDENT
SOGE
PCS 41
AGA 84 1191

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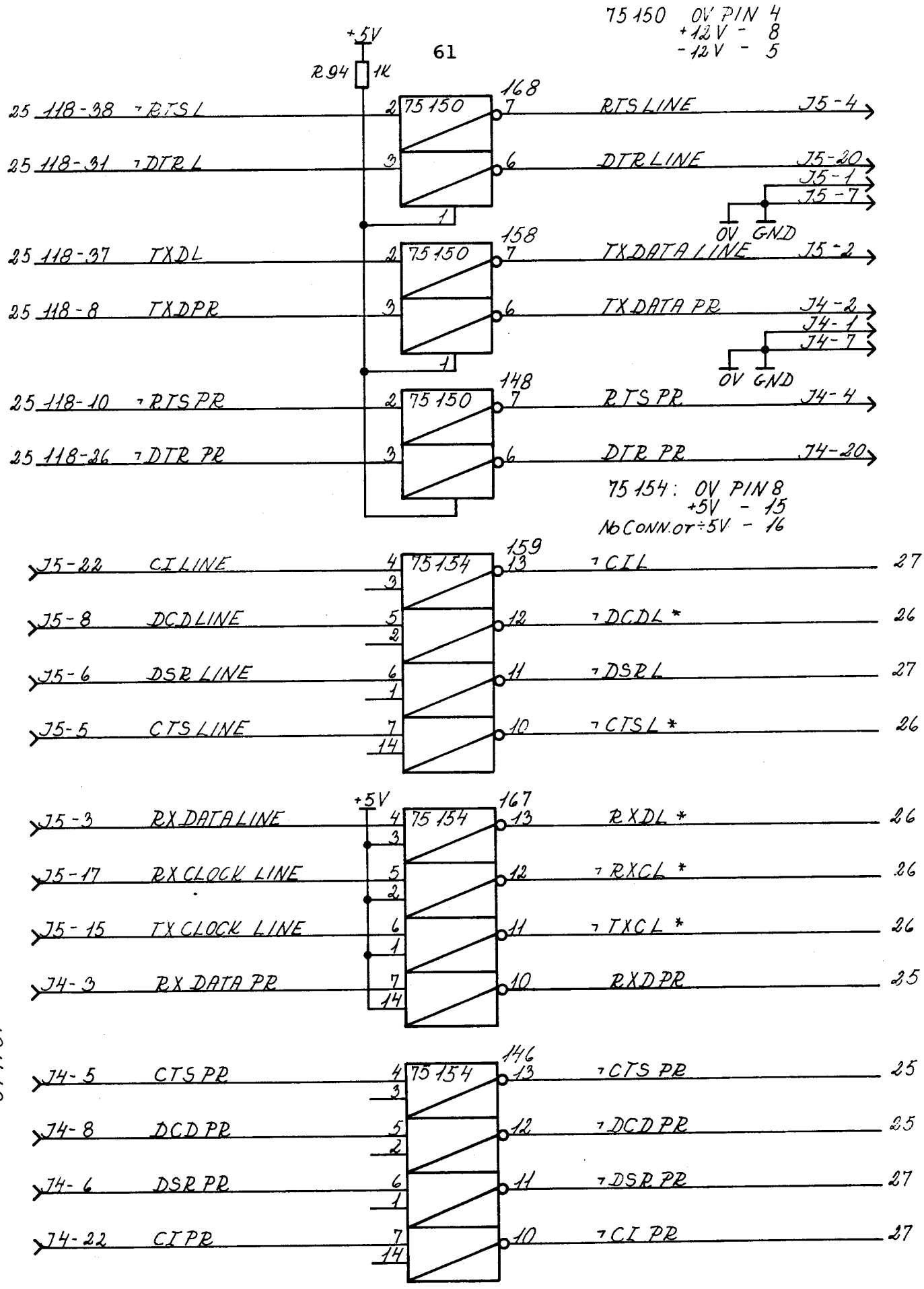
75150 0V PIN 4
+12V - 8
-12V - 5
+5V
R94 1K
168
158
148
159
167
146
25 118-38 RTSL
25 118-31 DTRL
25 118-37 TXDL
25 118-8 TXDPR
25 118-10 RTSPR
25 118-26 DTR PR
75150
RTS LINE
DTR LINE
TX DATA LINE
TX DATA PR
RTS PR
DTR PR
J5-4
J5-20
J5-1
J5-7
J5-2
J4-2
J4-1
J4-7
J4-4
J4-20
0V GND
75154: 0V PIN 8
+5V - 15
No CONN.or +5V - 16
J5-22 CI LINE
J5-8 DCD LINE
J5-6 DSR LINE
J5-5 CTS LINE
CIL
DCDL *
DSRL
CTSL *
J5-3 RX DATA LINE
J5-17 RX CLOCK LINE
J5-15 TX CLOCK LINE
J4-3 RX DATA PR
RXDL *
RXCL *
TXCL *
RXDPR
J4-5 CTS PR
J4-8 DCD PR
J4-6 DSR PR
J4-22 CI PR
CTS PR
DCD PR
DSR PR
CI PR
27
26
25

84 11 AGA 31

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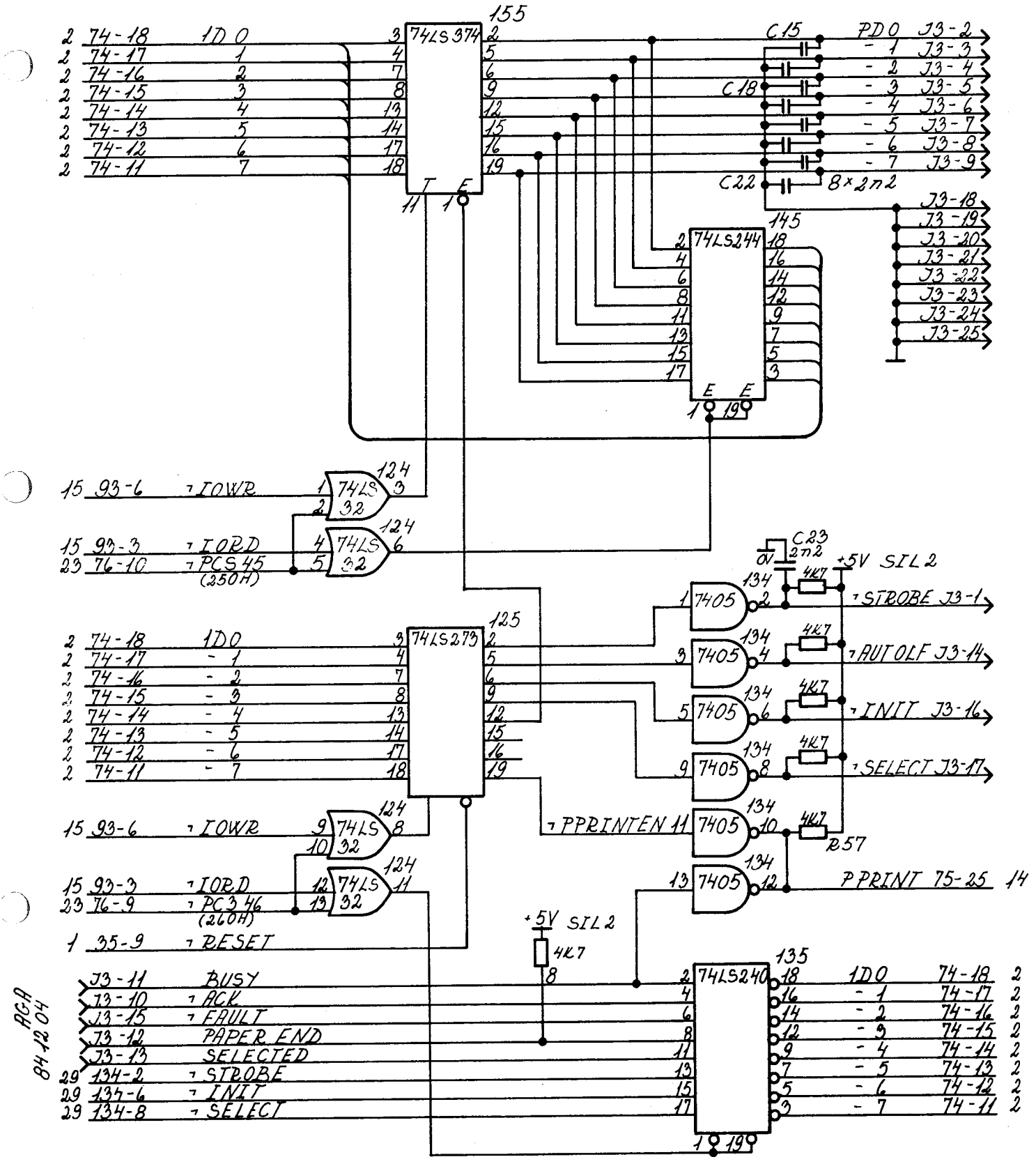
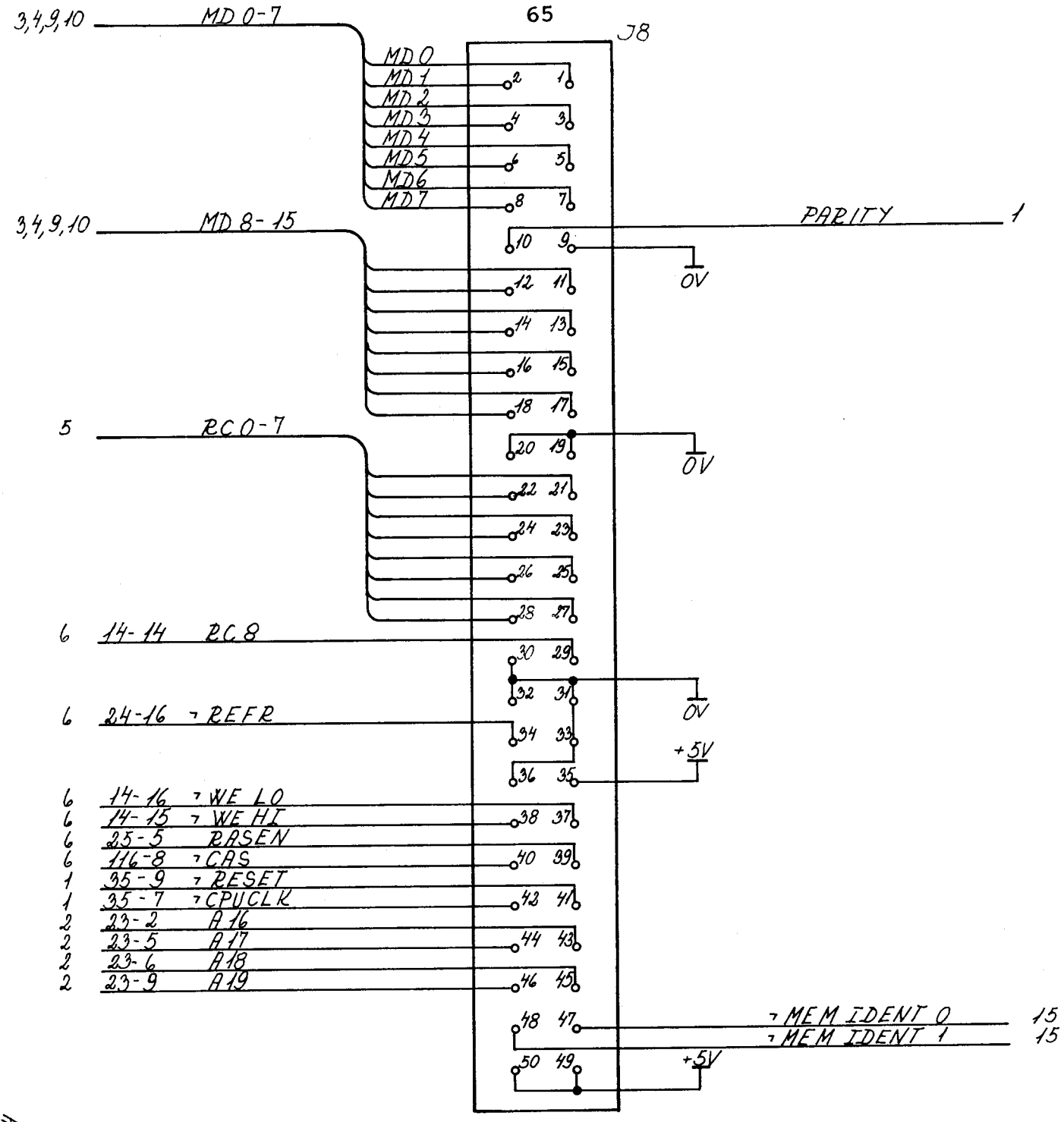
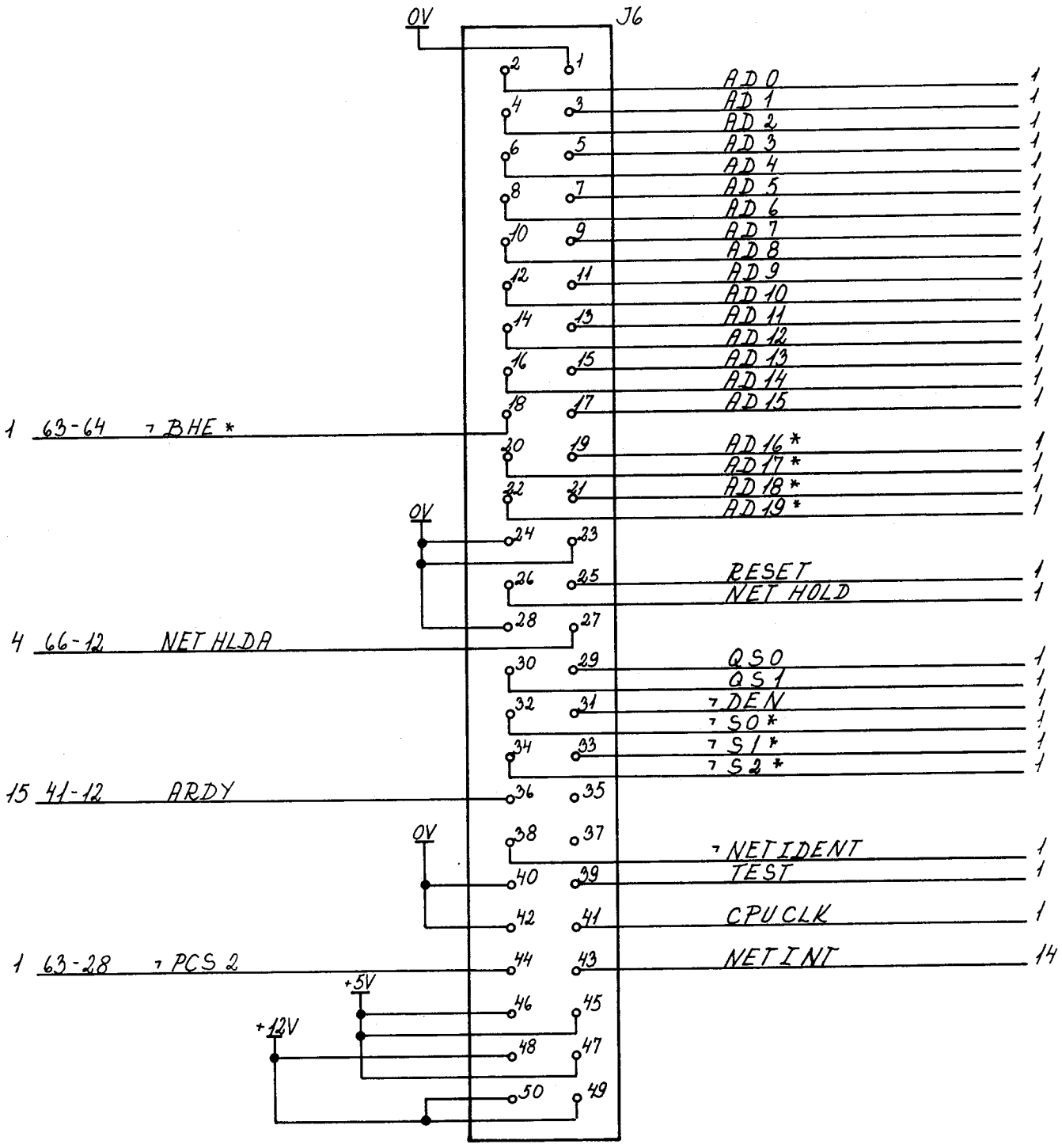

155
74LS374
145
74LS244
C15
C18
C22
8×2n2
PD0 J3-2
- 1 J3-3
- 2 J3-4
- 3 J3-5
- 4 J3-6
- 5 J3-7
- 6 J3-8
- 7 J3-9
J3-18
J3-19
J3-20
J3-21
J3-22
J3-23
J3-24
J3-25
2 74-18 1D0
2 74-17 1
2 74-16 2
2 74-15 3
2 74-14 4
2 74-13 5
2 74-12 6
2 74-11 7
15 93-6 ¬IOWR
15 93-3 ¬IORD
23 76-10 ¬PCS45 (250H)
124
74LS 32
125
74LS273
C23 2n2
+5V SIL2
4K7
134
7405
¬STROBE J3-1
¬AUTOLF J3-14
¬INIT J3-16
¬SELECT J3-17
¬PPRINTEN 11
R57
PPRINT 75-25 14
23 76-9 ¬PC346 (260H)
1 35-9 ¬RESET
135
74LS240
J3-11 BUSY
J3-10 ¬ACK
J3-15 ¬FAULT
J3-12 PAPER END
J3-13 SELECTED
29 134-2 ¬STROBE
29 134-6 ¬INIT
29 134-8 ¬SELECT
RGA 84 12 04

Signal	Description		
PARITY	Memory parity error detected.		
-MEMIDENT 0-1	Indication of attched memory size		
	-MI0	-MI1	Size
	1	1	256 Kbytes
	1	0	512 Kbytes
	0	1	768 Kbytes
	0	0	960 Kbytes


65
J8
3,4,9,10
MD 0-7
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
3,4,9,10
MD 8-15
PARITY
1
0V
5
RC 0-7
6
14-14
RC 8
6
24-16
¬REFR
+5V
6
14-16
¬WE LO
6
14-15
¬WE HI
6
25-5
RASEN
6
116-8
¬CAS
1
35-9
¬RESET
1
35-7
¬CPUCLK
2
23-2
A16
2
23-5
A17
2
23-6
A18
2
23-9
A19
¬MEM IDENT 0
15
¬MEM IDENT 1
15

AGA
84 12 04

Signal	Description
AD 0-15	
A 16-19	Processor address/databus, driven or sensed by the processor currently holding the bus.
RESET	Generated by the CPU during hard reset.
HOLD	Bushold request to the CPU.
-RD, -WR,	
-DEN, DT/-R	Bus control signals
-NETIDENT	Low when an Ethernet processor is attached.
NET ALE	The coprocessor is presenting an address on the AD bus.
NET INT	Interrupt request from the net processor (IR5).


0V
J6
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
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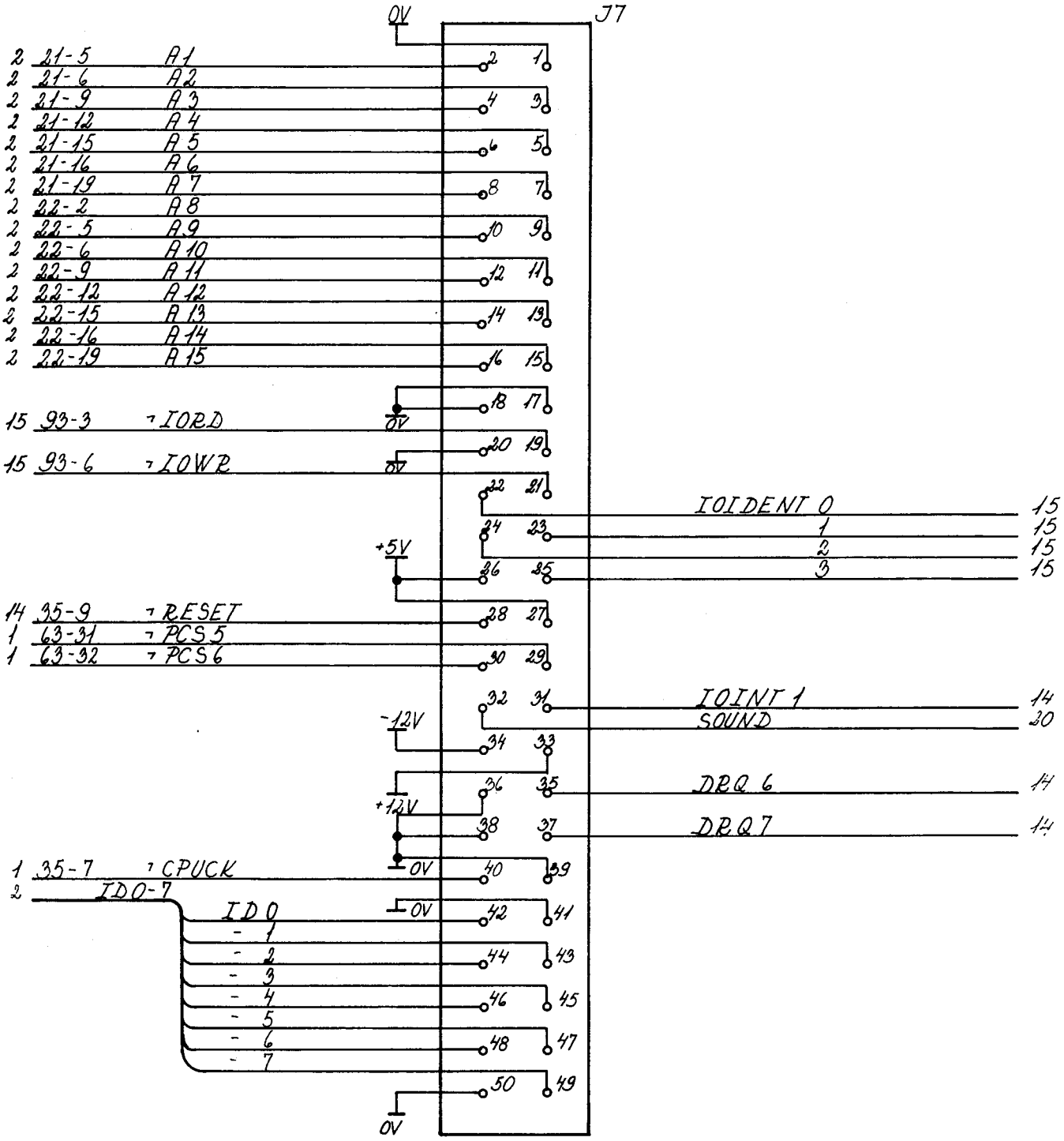
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
AD 0
AD 1
AD 2
AD 3
AD 4
AD 5
AD 6
AD 7
AD 8
AD 9
AD 10
AD 11
AD 12
AD 13
AD 14
AD 15
AD 16 *
AD 17 *
AD 18 *
AD 19 *
RESET
NET HOLD
QS 0
QS 1
¬ DEN
¬ S0 *
¬ S1 *
¬ S2 *
¬ NET IDENT
TEST
CPUCLK
NET INT
1 63-64 ¬ BHE *
4 66-12 NET HLDA
15 41-12 ARDY
1 63-28 ¬ PCS 2
+5V
+12V
0V
0V
0V

AGA 84 12 04

Signal	Description
A1-15	Addressbus capable to address 32768 I/O ports
-IORD	When active the addressed device should place the relevant data on the databus 1D 0-7
-IOWR	When active, relevant data is present on the databus 1D 0-7 and may be strobed into the addressed port.
IOIDENT 0-3	Strap options for identifying attached I/O controllers.
-RESET	Low when a hard reset is issued.
-PCS 5	
-PCS 6	Decoded chip select outputs active on addresses 280 to 2FE and 300 to 37E
I/O INT	Interrupt request from I/O devices (IR7)
DRQ 6-7	DMA request inputs from I/O devices
-CPU CLK	Clockpulse from CPU 6 or 8 MHz
1 D 0-7	Databus.


0V
J7
2 21-5 A1
2 21-6 A2
2 21-9 A3
2 21-12 A4
2 21-15 A5
2 21-16 A6
2 21-19 A7
2 22-2 A8
2 22-5 A9
2 22-6 A10
2 22-9 A11
2 22-12 A12
2 22-15 A13
2 22-16 A14
2 22-19 A15
15 93-3 ¬IORD
15 93-6 ¬IOWR
+5V
14 35-9 ¬RESET
1 63-31 ¬PCS5
1 63-32 ¬PCS6
-12V
+12V
1 35-7 ¬CPUCK
2 IDO-7
IDO
- 1
- 2
- 3
- 4
- 5
- 6
- 7
IOIDENT 0 15
1 15
2 15
3 15
IOINT 1 14
SOUND 30
DRQ 6 14
DRQ7 14

AGA 84 12 06

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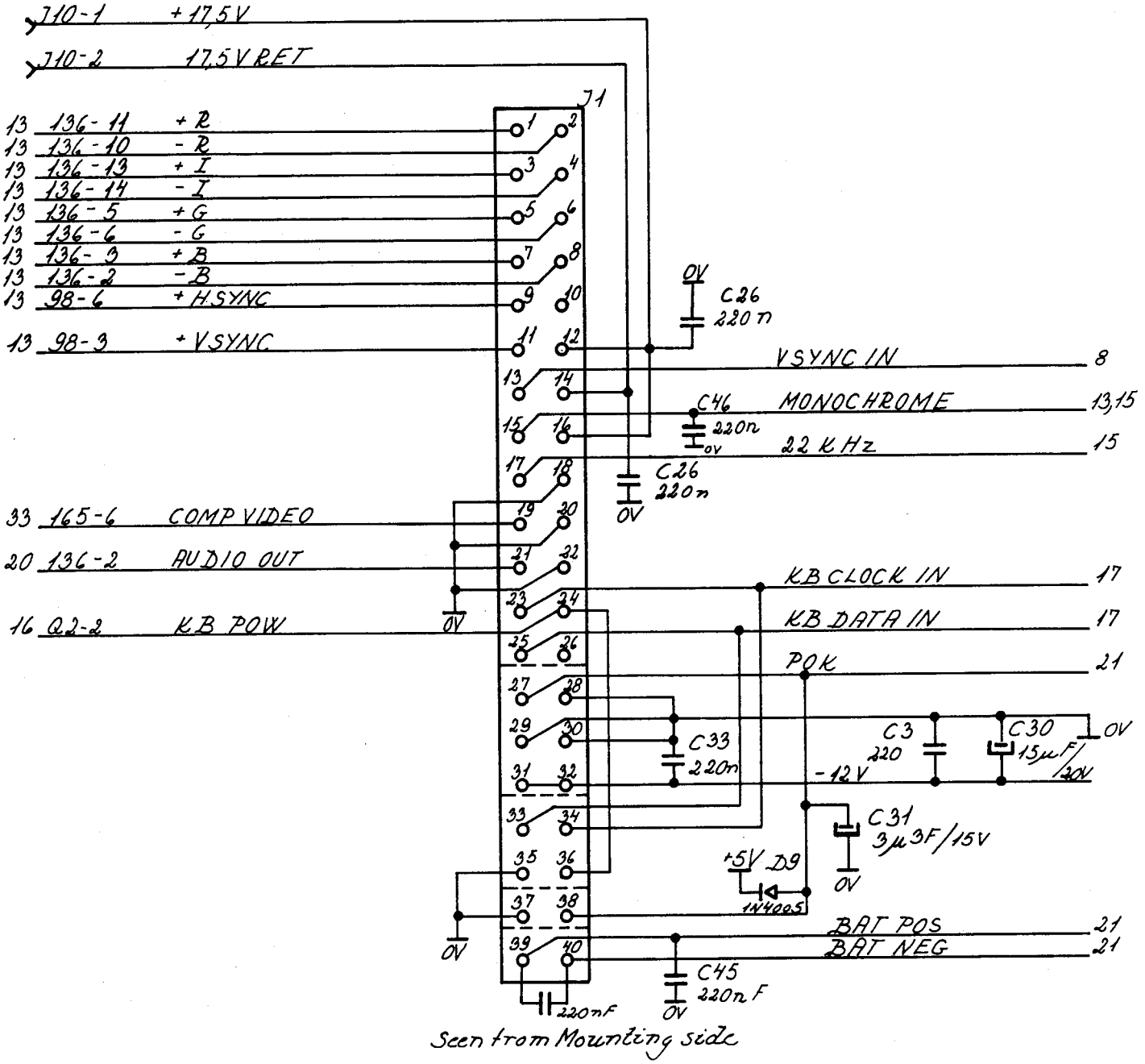
J10-1 +17,5V
J10-2 17,5V RET
J1
13 136-11 +R
13 136-10 -R
13 136-13 +I
13 136-14 -I
13 136-5 +G
13 136-6 -G
13 136-3 +B
13 136-2 -B
13 98-6 +H.SYNC
13 98-3 +VSYNC
33 165-6 COMP VIDEO
20 136-2 AUDIO OUT
16 Q2-2 KB POW
0V
C26 220 n
VSYNC IN 8
C46 220n
MONOCHROME 13,15
22 KHz 15
C26 220n
KB CLOCK IN 17
KB DATA IN 17
POK 21
C33 220n
C3 220
C30 15µF/30V
-12V
C31 3µ3F/15V
+5V D9
1N4005
BAT POS 21
BAT NEG 21
C45 220n F
220nF
Seen from Mounting side

AGA 83.11.01

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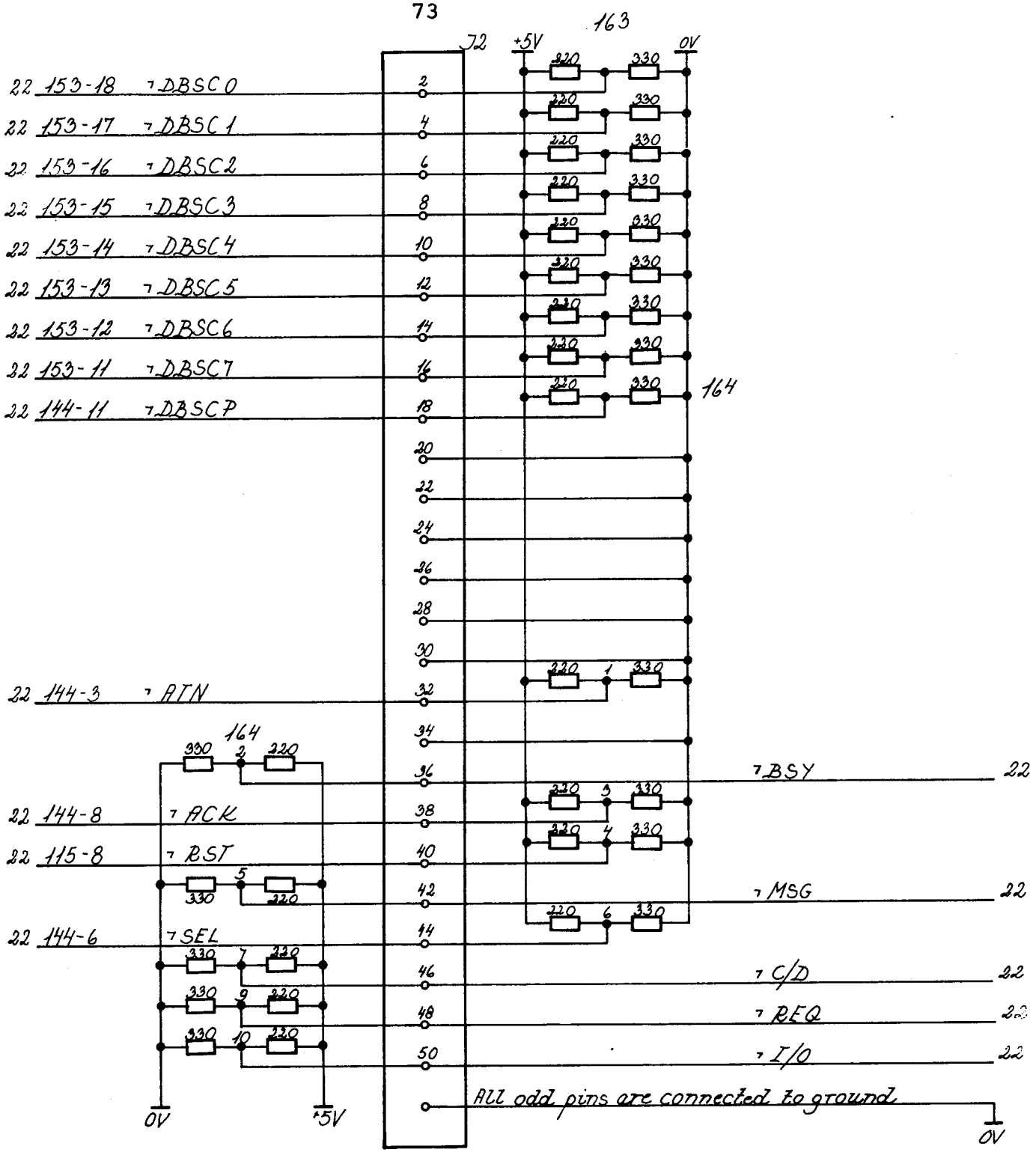
J2
+5V
0V
163
164
22 153-18 ⅂DBSC0
22 153-17 ⅂DBSC1
22 153-16 ⅂DBSC2
22 153-15 ⅂DBSC3
22 153-14 ⅂DBSC4
22 153-13 ⅂DBSC5
22 153-12 ⅂DBSC6
22 153-11 ⅂DBSC7
22 144-11 ⅂DBSCP
22 144-3 ⅂ATN
22 144-8 ⅂ACK
22 115-8 ⅂RST
22 144-6 ⅂SEL
⅂BSY 22
⅂MSG 22
⅂C/D 22
⅂REQ 22
⅂I/O 22
All odd pins are connected to ground
0V
+5V
220
330

AGA
84 12 06

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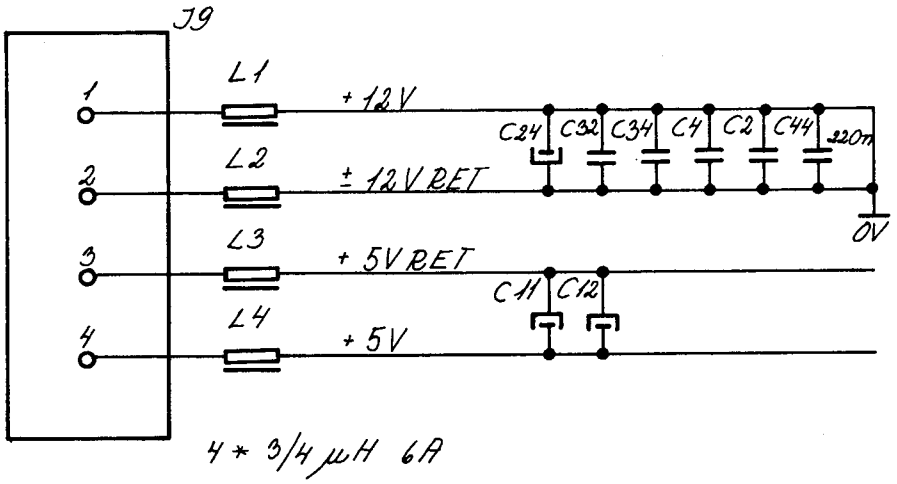

4 * 3/4 µH 6A

4stk Drosselspoler

RGA
84 12 06

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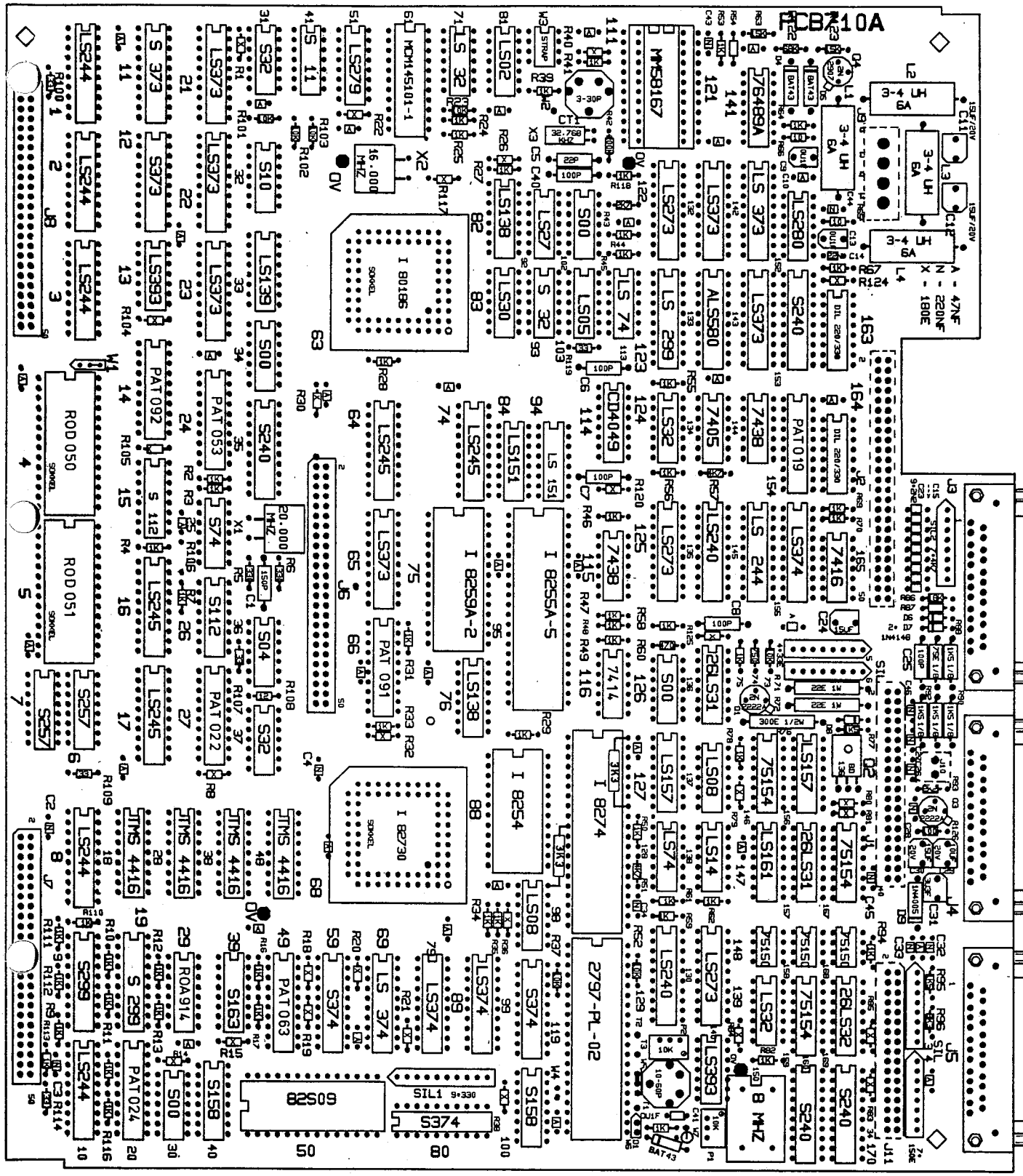


STIK: J1, J2, J9, J10, J11.
MONTERES FRA LODSIDEN.

W4, MONTERES IKKE.

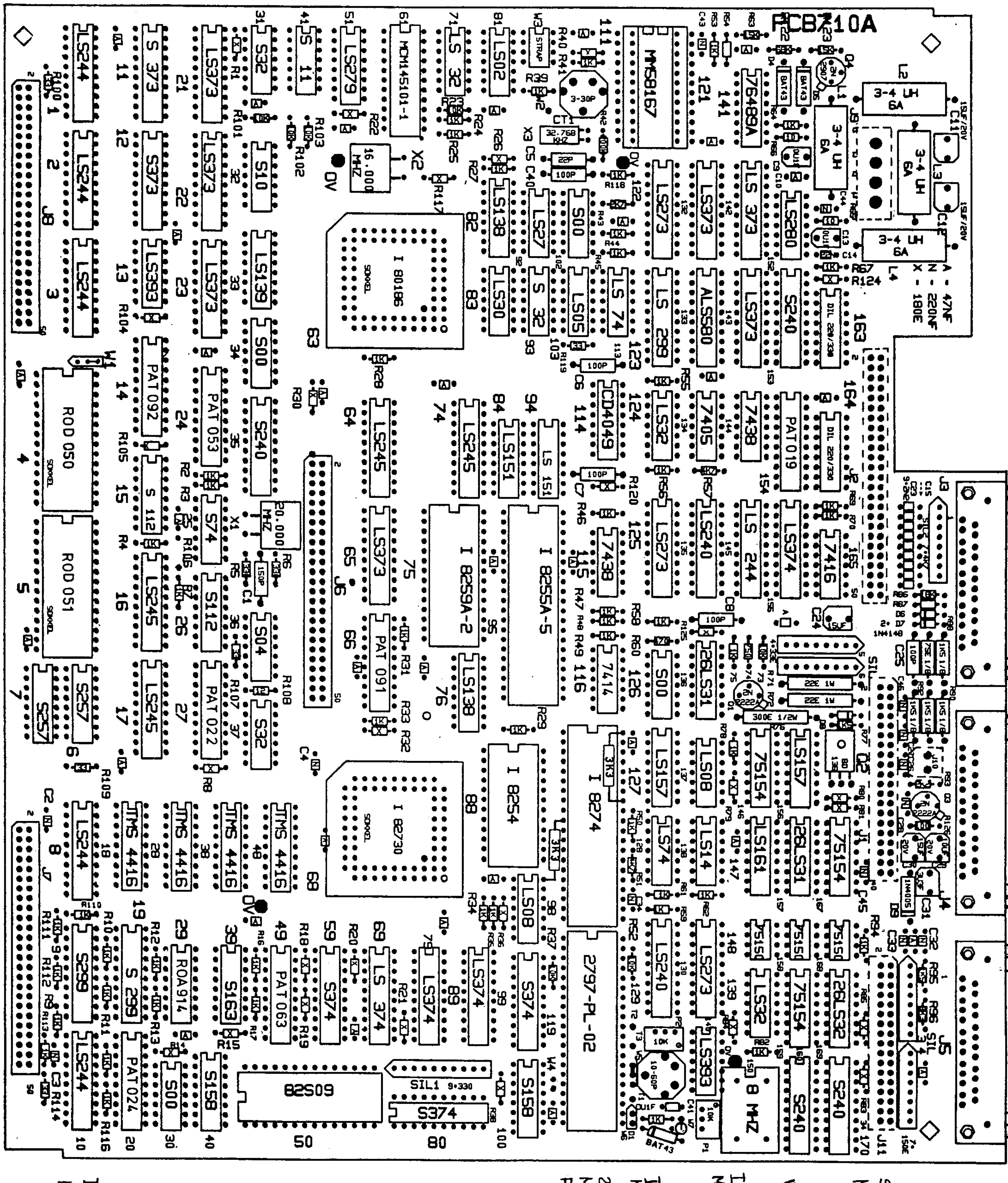
I POS. W7
MONTERES 200E.

I POS. W5
MONTERES LUS.

2 STK. 3K3 ¼W
MONTERES VED
POS. 118.

I POS. W1
MONTERES LUS.

ENHED / BETEGNELSE			
CPU 755			6
MONTAGETEGNING PCB 710A	850704 HC	760 85 085	5
	850617 HC	760 85 084	4
	850523 HC	760 85083	3
	850515 HC	760 85082	2
	850506 HC	760 85081	1
	DATO / SIGN 850301 HC	TEGN NR 760 85080	0



STIK: J1, J2, J9, J10, J11.
MONTERES FRA LODDESIDEN.

W4, MONTERES IKKE.

I Pos W7
MONTERES 200E.

I POS. W5
MONTERES LUS.
2 STK. 3K3 1/20W
MONTERES VED
POS. 118.

I Pos. W1
MONTERES LUS.

ENHED / BETEGNELSE			
			6
CPU 756			5
MONTAGETEGNING PCB 710A	850704HC	760 85094	4
	850617HC	760 85093	3
	850523HC	760 85092	2
	850515HC	760 85091	1
	DATO / SIGN 850509HC	TEGN NR 760 85090	0

RETURN LETTER

Title: CPU755, CPU756 Technical Manual
RC750 CPU-Board

RCSL No.: 991 10250

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Do you find errors in this manual? If so, specify by page.

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How can this manual be improved?

_____

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_____

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