

Internal use only

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Title:

DRAWINGS for MEM752

Keywords:

MEM752, Memory board, RC750

Abstract:

This manual contains drawings for MEM752 which is used in the RC750 system as main memory

(18 printed pages)

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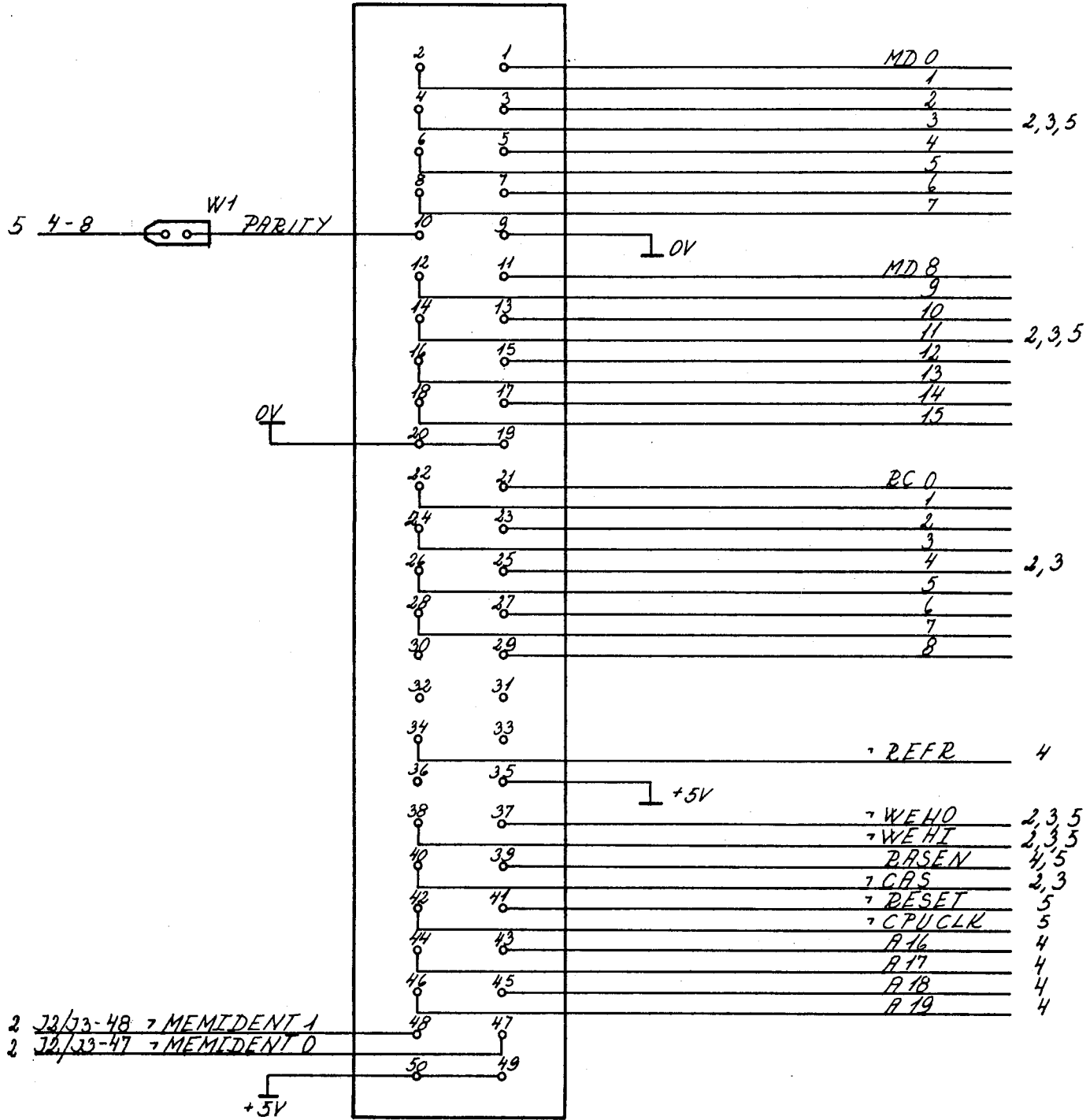
1. GENEREL 1

1. GENEREL

This manual contains the drawings for MEM752, which is used as the main memory (256k byte) in the RC750 system.

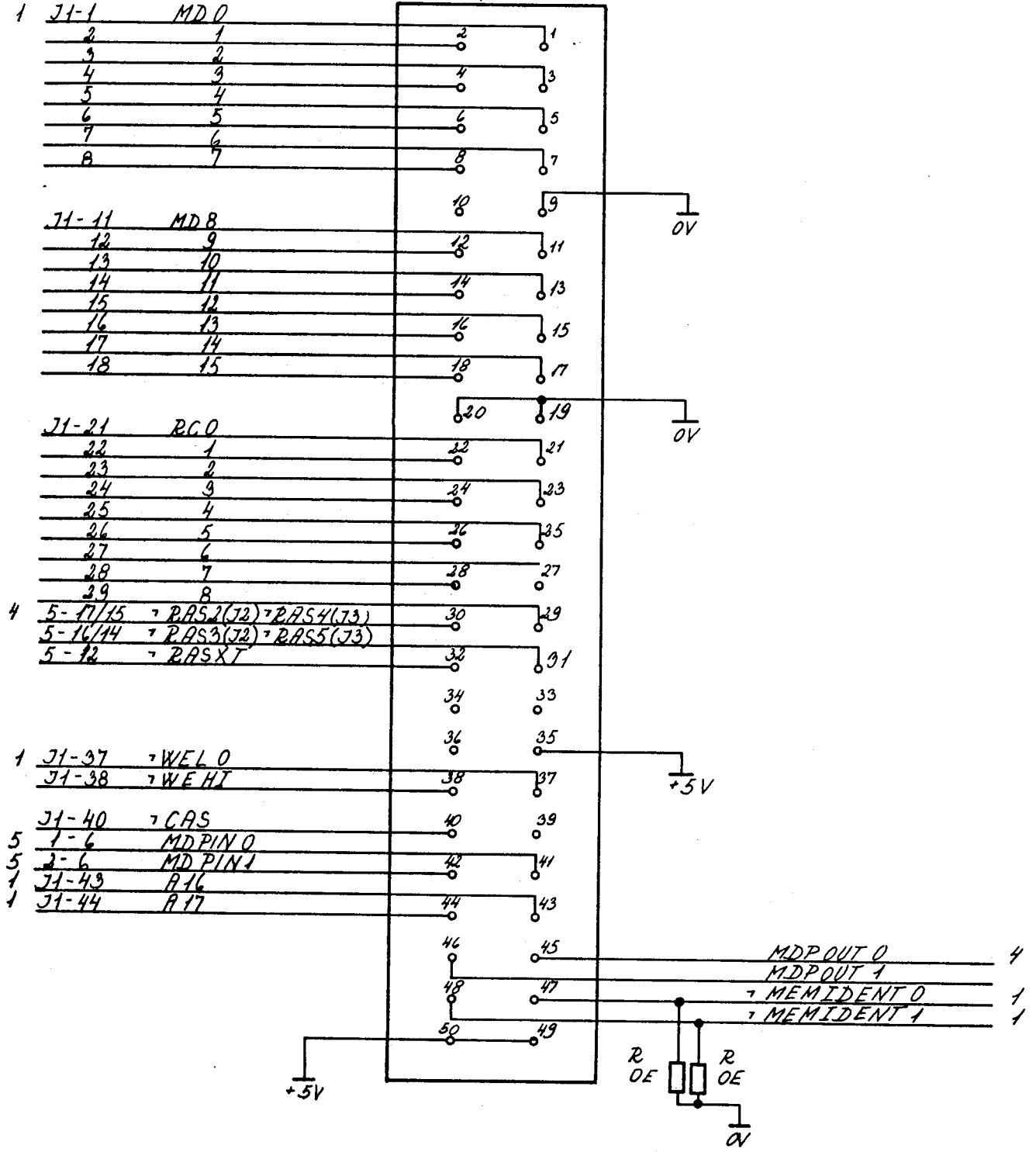
| <u>Signal name</u> | <u>Description</u> |
|--------------------|--|
| MD0-15 | Memory data bus. |
| RC0-8 | Time multiplexed row and column addresses. |
| -, REFR | Referesh request. |
| -, WELO | Write enable, low byte. |
| -, WEHI | Write enable, high byte. |
| RASEN | Row address strobe. |
| -, CAS | Colomn address strobe. |
| -, RESET | Reset signal from CPU. |
| A16-19 | memory address signals. |

J1



| <u>Signal name</u> | <u>Description</u> |
|--------------------|-------------------------------------|
| MDPOUTO | Stored parity bit 0 |
| MDPOUT1 | Stored parity bit 1 |
| -,MEMIDENTO-1 | Memory size identification signals. |

J2/J3



AGA
840222

| <u>Signal name</u> | <u>Description</u> |
|--------------------|---------------------|
| MDPOUTO-1 | Memory parity bits. |

AGA
840222

MEM 752

256 K BYTE DRAM

4,5 MDPINO 1-6

1,2,5 MD0-7

4,5 MDPINI 2-6

1,2,5 MD8-15

1,2 BC0-7

1,2 PC8

4 PRBS0

1,2 CAS

31-40

4 PRAS1

1,2 WEH1

31-38

1,2 WELO

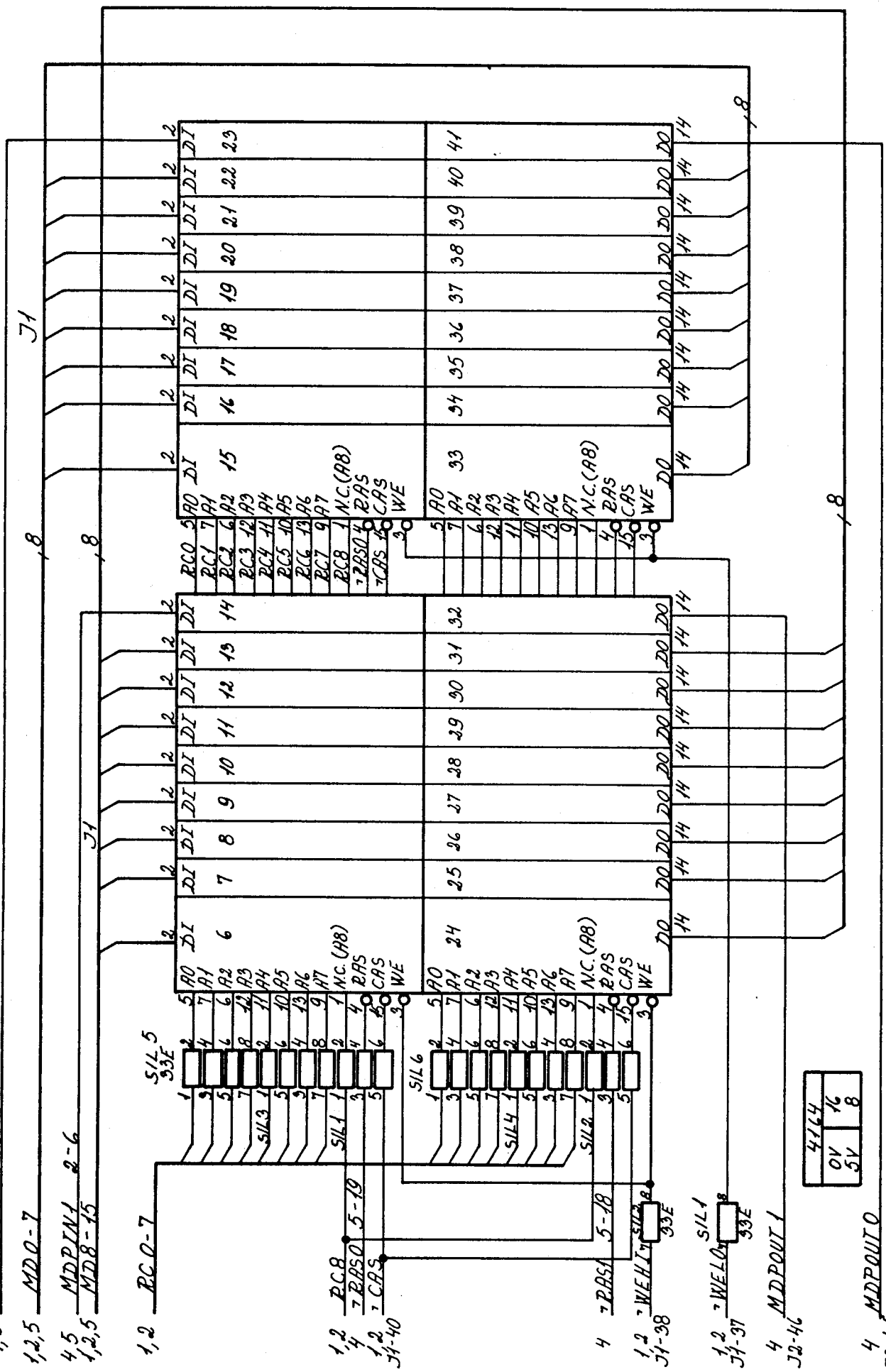
31-37

4 MDPQOUT1

J2-46

4 MDPQOUT0

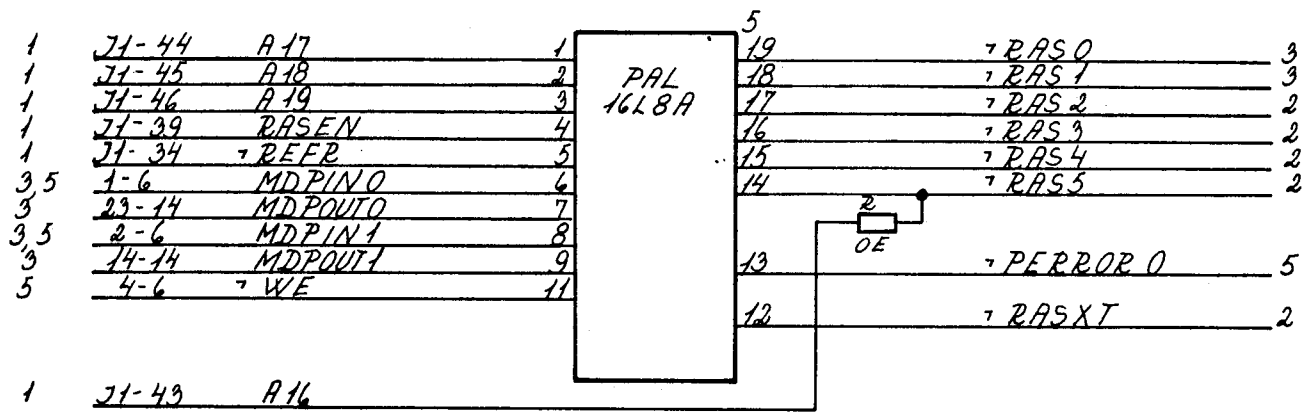
J2-45



High Byte

Low Byte

| <u>Signal name</u> | <u>Description</u> |
|--------------------|---|
| -,RAS0 | Row address strobe in the address space: 00000H - 1FFFFH. |
| -,RAS1 | Row address strobe in the address space: 20000H - 3FFFFH. |
| -,RAS2 | Row address strobe in the address space: 40000H - 5FFFFH. |
| -,RAS3 | Row address strobe in the address space: 60000H - 7FFFFH. |
| -,RAS4 | Row address strobe in the address space: 80000H - 9FFFFH. |
| -,RAS5 | Row address strobe in the address space: A0000H - BFFFFH. |
| -,RASXT | Row address strobe in the address space: C0000H - FFFFFH. |
| -,PERROR0 | Parity error signal. |



| A19 | A18 | A17 | ~RAS |
|-----|-----|-----|------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | X | not |

$$RAS0 = \neg A17 * \neg A18 * \neg A19 * RASEN$$

$$* \neg REFR + RASEN * REFR$$

$$RAS1 = A17 * \neg A18 * \neg A19 * RASEN$$

$$* \neg REFR + RASEN * REFR$$

$$RAS2 = \neg A17 * A18 * \neg A19 * RASEN$$

$$* \neg REFR + RASEN * REFR$$

$$RAS3 = A17 * A18 * \neg A19 * RASEN$$

$$* \neg REFR + RASEN * REFR$$

$$RAS4 = \neg A17 * \neg A18 * A19 * RASEN$$

$$* \neg REFR + RASEN * REFR$$

$$RAS5 = A17 * \neg A18 * A19 * RASEN$$

$$* \neg REFR + RASEN * REFR$$

$$PERRO0 = \neg MDPIN0 * MDPOUTO * \neg REFR * \neg WE$$

$$+ MDPIN0 * \neg MDPOUTO * \neg REFR * \neg WE$$

$$+ \neg MDPIN1 * MDPOUT1 * \neg REFR * \neg WE$$

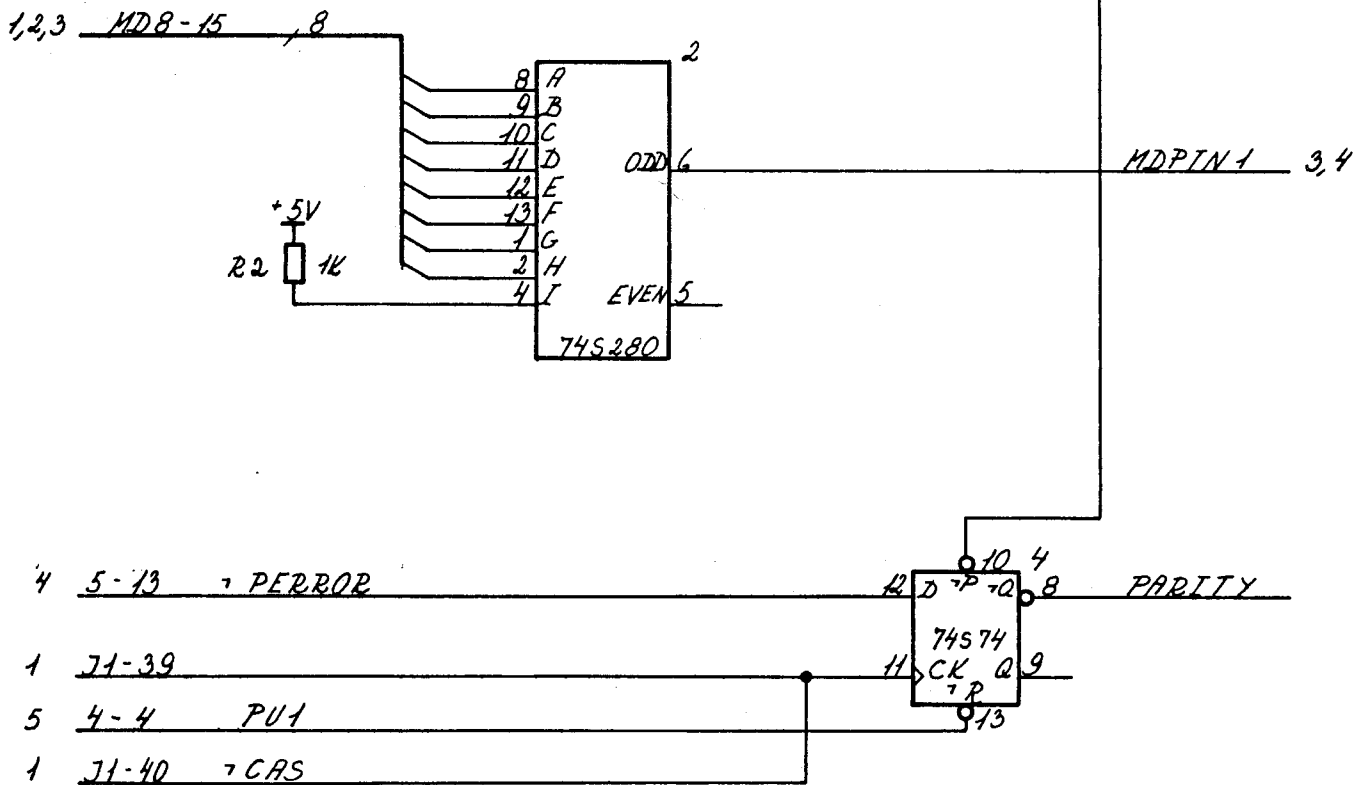
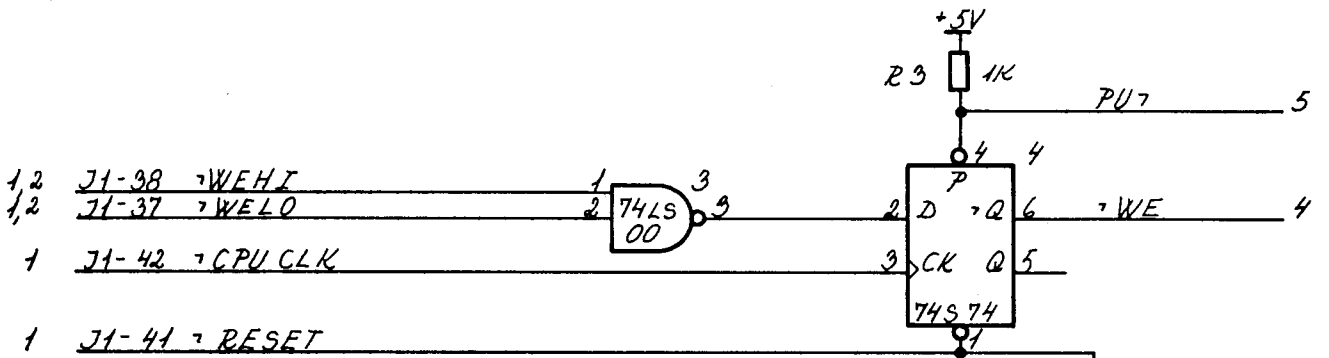
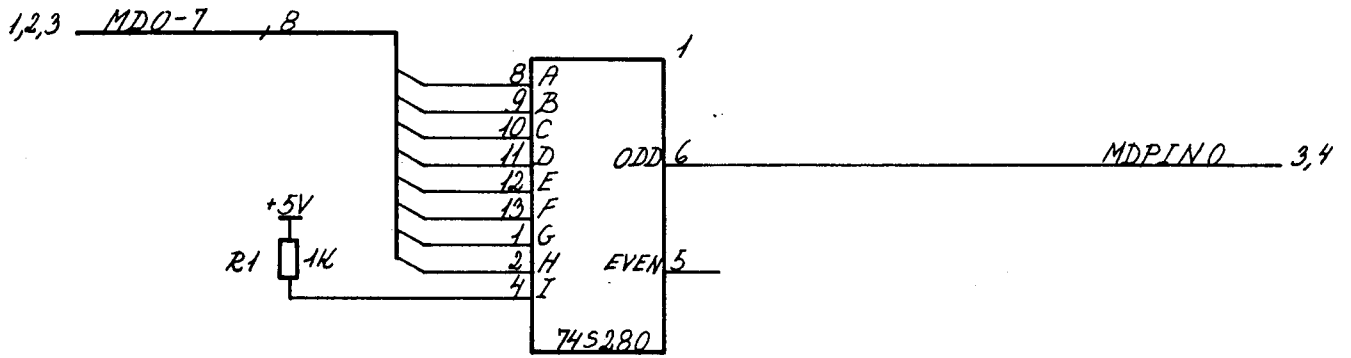
$$+ MDPIN1 * \neg MDPOUT1 * \neg REFR * \neg WE$$

$$RASXT = A18 * A19 * RASEN * \neg REFR$$

$$+ RASEN * REFR$$

RCA
840222

| <u>Signal name</u> | <u>Description</u> |
|--------------------|---|
| MDPINO | Memory parity signal generated from MD0-7. |
| MDPIN1 | MEMORY PARITY SIGNAL GENERATED FROM MD8-15. |
| PUL | Pull-up level. |
| -,WE | Write enable signal used by the parity error detect circuit. |
| Parity | Parity error signal to the CPU. Generates NMI-interrupt signals. |



RETURN LETTER

Title: Drawings for MEM752

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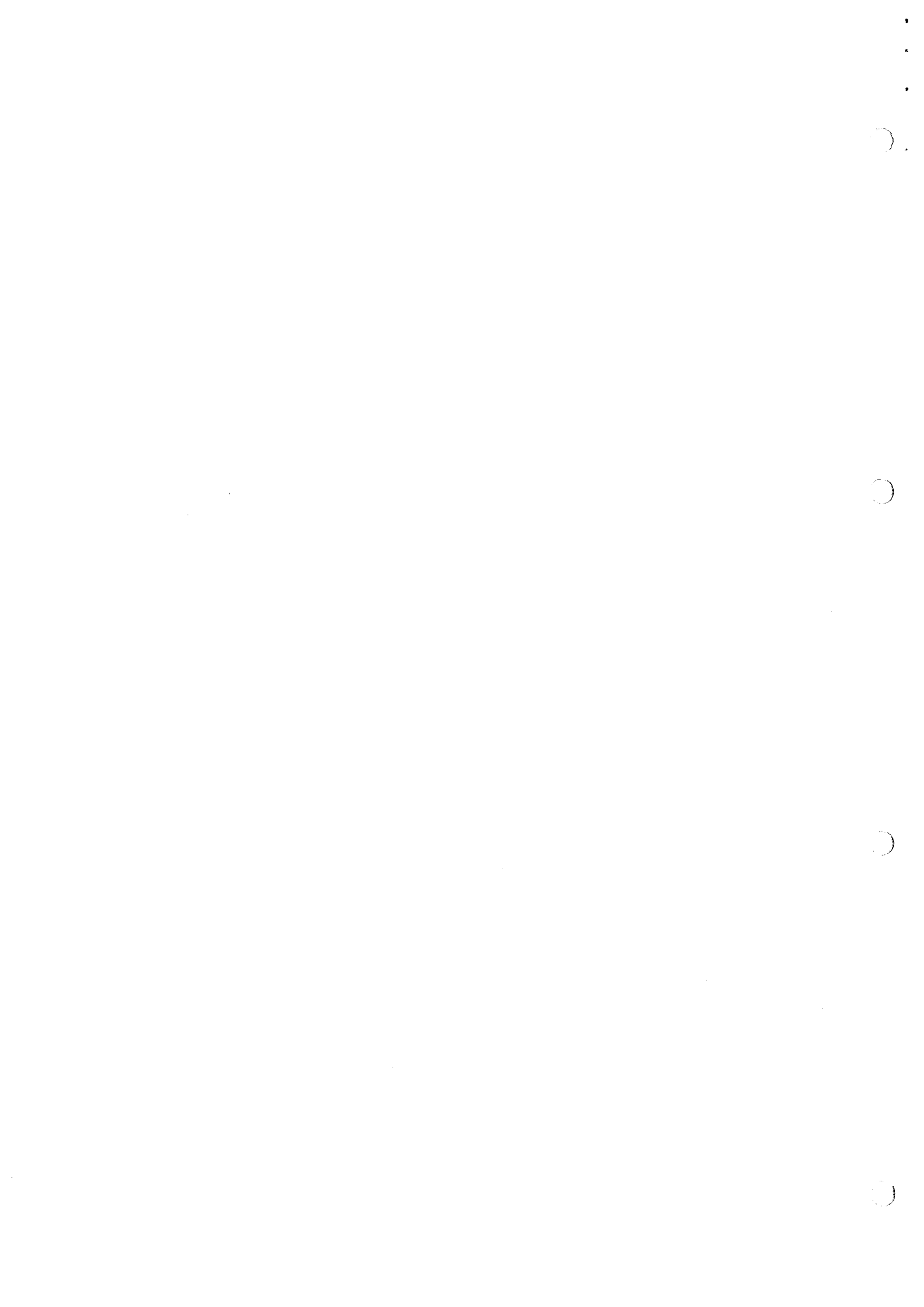
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