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Title:

# RC750
# CPU board
# Reference Manual

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**Keywords:**

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**Abstract:**

This paper contains the information necessary to program the RC750.

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## 1. CPU



The system is based on an Intel 80186 single chip CPU. This CPU is described in detail in the Intel Reference Manual.

This section describes how the pheriperals and memory are connected to the CPU.

80186 can handle up to 1M bytes of memory. The RC750 CPU board is equipped with 256 Kbytes of general memory, 32K bytes of memory dedicated to the CRT controller, but accessed by the CPU as normal memory, and finally 32 Kbytes of ROM (Read only memory) for autoload and standard programs.

The following peripherals are standard:

CRT control
Floppy interface
SASI interface
V24/X21
V24 (printer)
Keyboard input
Non Volatile Memory
Real Time Clock
Sound device
I/O Bus connection.

The interconnections of these are shown on the blockdiagram fig. 1.

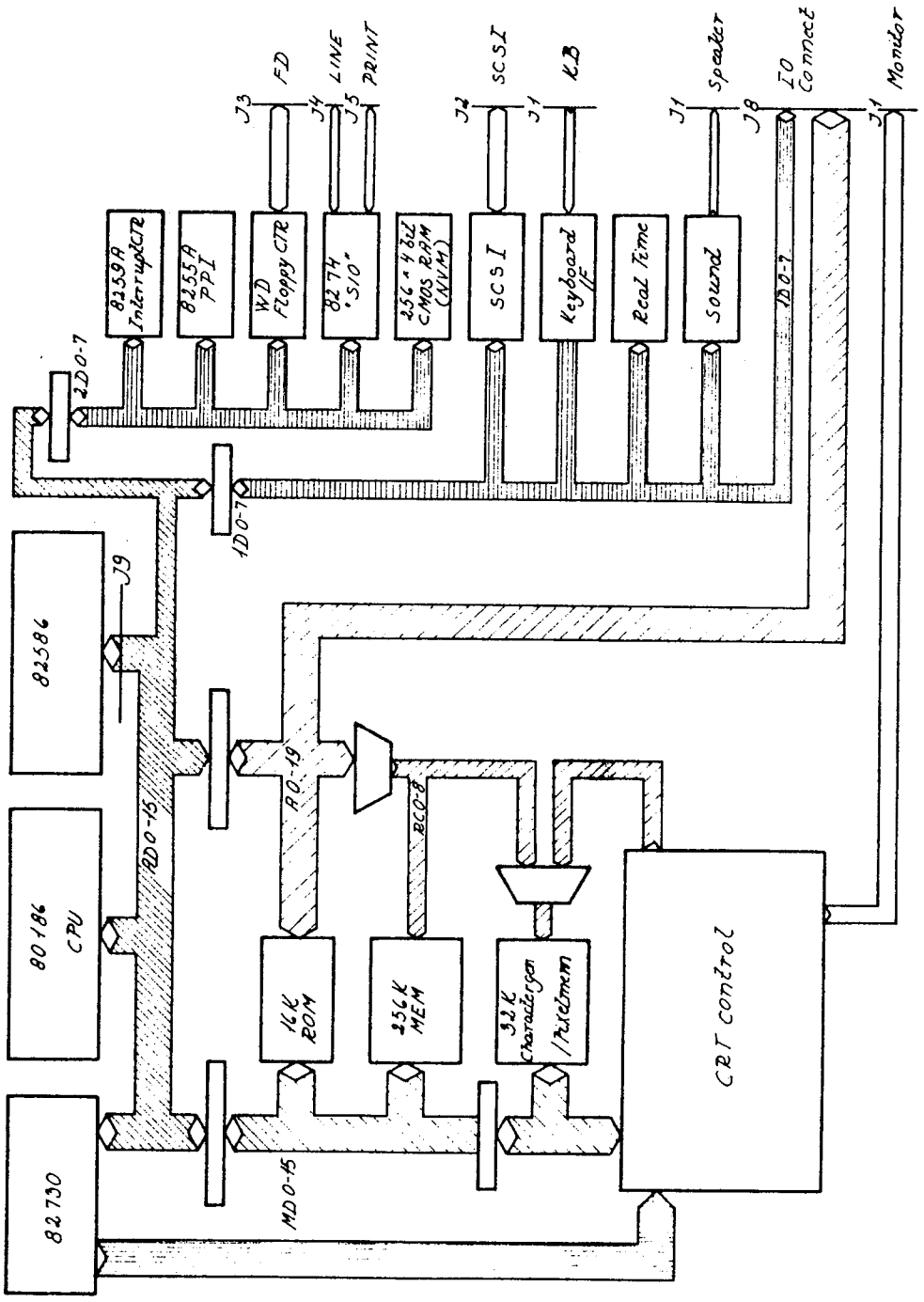



Figure 1: Block Diagram.

## 1.1 Memory

1.1

The memory consists of at least the following parts:

1. 256 K bytes of general memory
2. 32 K bytes of Pixel memory used by the CRT
3. 32 K bytes of Read Only Memory.

512 K of address space is left for memory extension. The address space is divided into the areas shown on fig. 2.

The CPU runs at 8MHz, which gives rise to a maximum of 2 memory accesses every microsecond. The memory chips used are fast enough to avoid the insertion of wait states. Only access to the CRT-memory may delay the CPU slightly, because of the heavy load the CRT imposes on this memory.

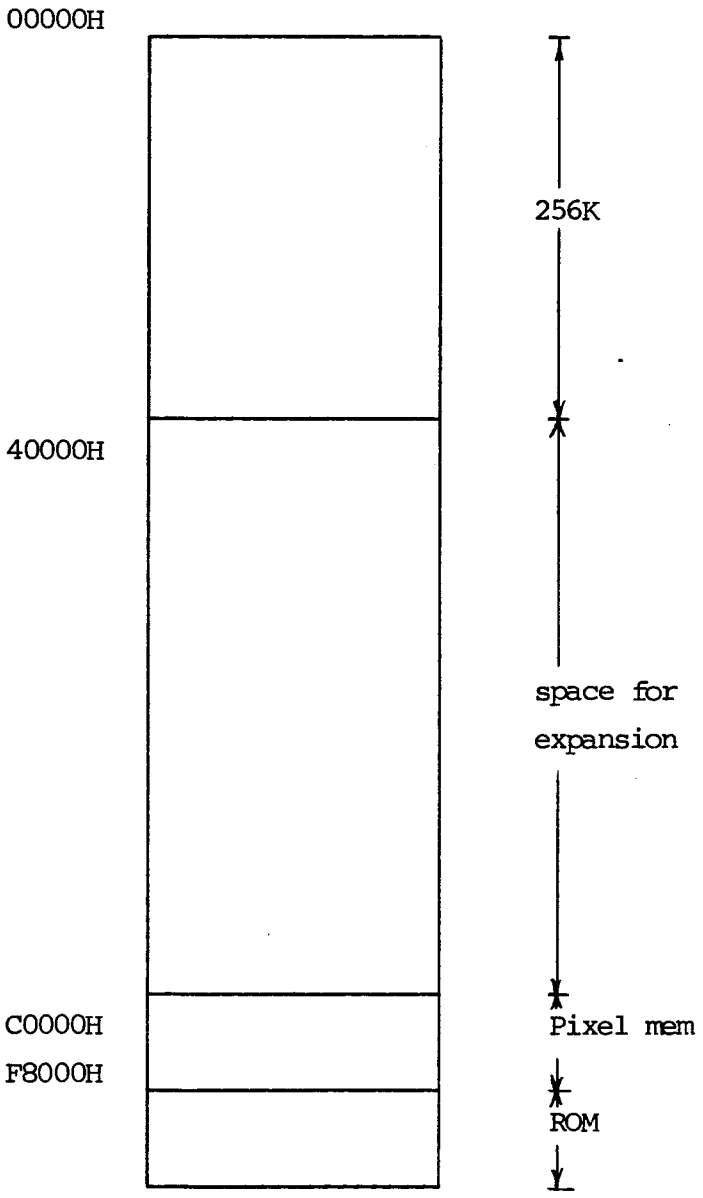



Figure 2:

The memory is of dynamic RAM type, and needs periodical refresh cycles. When the CRT controller is initialized, the line sync pulses are used to generate refresh requests. But while the CRT controller is uninitialized, the CPU must maintain refresh of the memory. This can be done by letting one of the DMA channels repeatingly move a block of 256 words (512 bytes) to the same locations.

## 1.2 Direct Memory Access 1.2

The 80186 has two integrated DMA channels which are shared between several peripherals.

The signals to the two DMA Request inputs are selected from up to eight lines by means of two selectors.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NVM addr | | DRQA sel | | | DRQB sel | | |

The two selectors are controlled by means of the outputport A on the 8255 PPI. Port A has the address I/O base + 70 Hex.

## 1.3 I/O 1.3

The peripherals are addressed via the seven PCS signals generated by the CPU. PCS0 controls eight chipselect signals on the CPU-board: PCS00 to PCS07 selected by means of the address bits A4 to A6.

As the pheripherals are connected to the least significant eight bits of the databus, the devices can only be accessed with even addresses. This gives each PCSx 64 addresses, and each PCS0x 8 addresses.

The PCS signals are allocated either I/O space or memory address space by programming a word in the controlblock (see the iAPX186 manual).

## 1.4 Interrupt 1.4

The peripherals able to interrupt he CPU except the 8274 are connected to this via a 8259A PIC. (Programmable Interrupt Controller). This is programmable via the port controlled by PCS0,0.

The IR inputs are connected as follows:

IR0 : Floppy
IR1 : Keyboard
IR2 : SCSI
IR3 : Real Time Clock
IR4 : CRT
IR5 : NET
IR6 : Parallel (Printer) Port
IR7 : I/O slot

8259 is connected to the INT0 and INTA0 terminals of the CPU in cascade mode.

Programming of the 8259 A takes place via the following addresses:

Initialization command word: I/O base + 0
Operation command word: I/O base + 2

The 8274 comm. controller is connected to the INT1 and INTA1 terminals also in cascade mode.

For programming the internal CPU interupt controller, see the iAPX186 referecne manual: Bit 5 (c) in the INT0 and INT1 control registers should be set to 1.

## 2. CRT CONTROL 2.

### 2.1 Generel 2.1

The CRT controller is build around an Intel 72730 coprocessor, which fetches characters in memory for display controlled by a channel program.

The characters are stored in a rowbuffer to avoid 13 redundant refetches of the characters in mainmemory. Then the character codes combined with a scanlinenumber generated by the 730 is used to address the character generator/Pixel memory.

The CRT controller should maintain a frame-frequency of about 60 Hz, each frame containing 350 videolines with 720 pixels each.

The controller will perform equally well as a memory mapped pixel graphic display, and a conventional alphanumeric display.

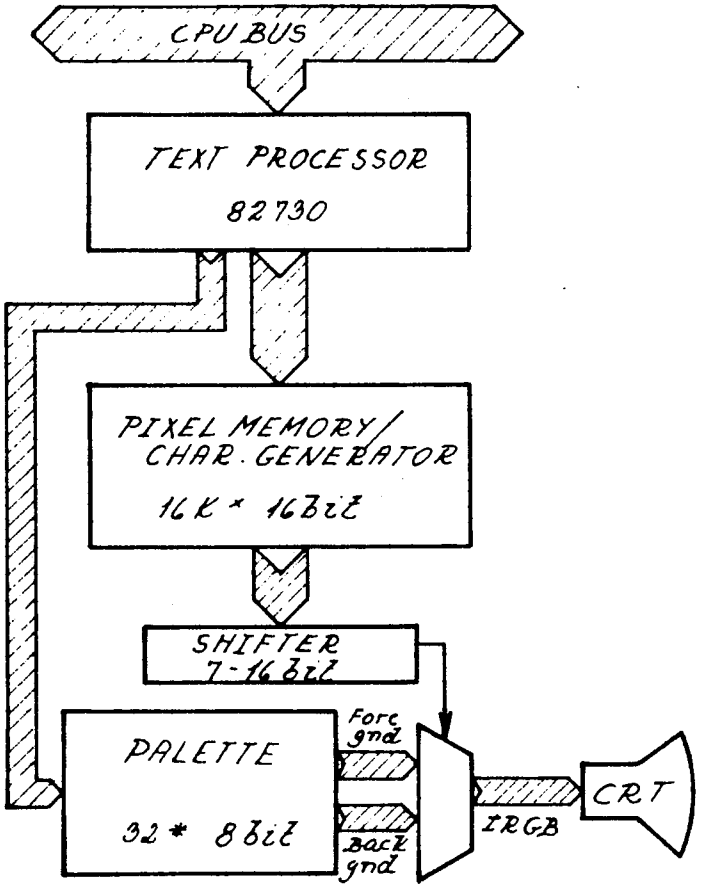



Figure 3: Blockdiagram of the CRT system.

The least significant 10 bits of the character code combined with the scanline address directly address the pixel memory to output a 16 bit 'word' of which at least 7 bit and at most all 16 bit are used as a dot pattern, shifted out of the shifter to be used as dot colour selector. In alpha mode, the bits select one of two colours, and in graphics either one out of two or four colours from a palet of 16 colours. If four colours are choosen in graphics mode, the dot frequency (horizontal resolusion) is only 10 MHz (360 dots).

## 2.2 Functional Description

### 2.2.1 82730 Coprocessor

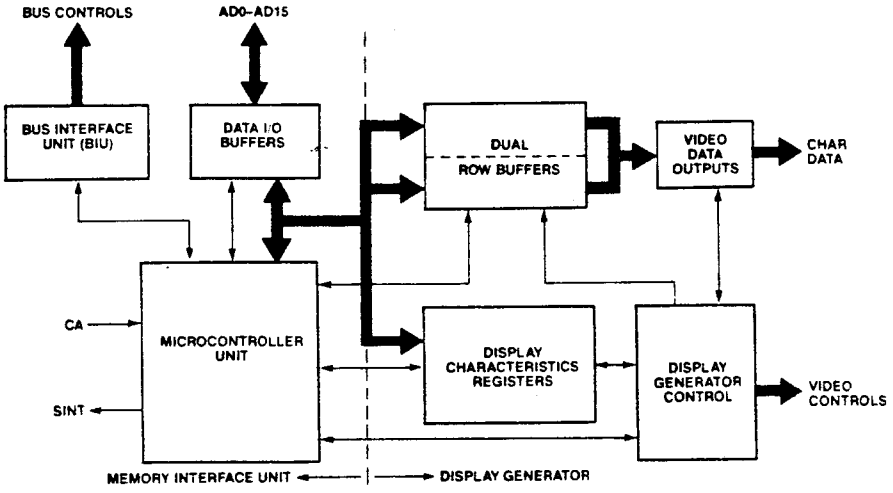



Figure 4: 82730 Block diagram.

Figure 4 shows a block diagram of the 82730. The chip is divided into two main sections. The Memory Interface Unit (MIU) and the Display Generator (DG). The MIU provides the communication between the 82730 and system processor and memory, while the DG acts on the display data and carries out the display operation.

Communication between the 82730 and the CPU takes place through messages placed in communication blocks in shared memory. The processor issues channel commands by preparing these message blocks and directing the 82730's attention to them by activating

a hardware channel attention signal (CA). The MIU fetches and executes these commands. When the display process is activated, the 82730 repeatedly fetches display data and embedded datastram commands from memory utilizing its built-in DMA capability, executes any datastream commands as encountered on the fly, and loads the row buffers with the display data. After executing these commands, the 82730 clears a busy flag in memory, to inform the host CPU that it is ready for the next command.

The MIU is divided into two sections. The Bus Interface Unit (BIU) and the Micro Controller Unit (MCU). The BIU proces the electrical interface to the system bus, and the timing signals required for the MCU operations, making these operations transparent to the MCU. The 82730 can be programmed during initialization to provide 8 or 16 bit data, and 16 or 32 bit addressing.

The MCU contains the microinstruction store and the associated circuitry required for the execution of all channel and datastream commands. It uses the BIU in carrying out its memory access tasks such as loading the row buffers with display data.

The interaction between the MCU and the DG takes place through shared internal storage. The MCU fetches data from memory and writes it in the internal storage, while the DG reads from the internal storage and carries out the display operation. The MCU and DG operate asynchronously with respect to each other. Syncrhonization is accomplished through communication via internal falgs and display timing signals generated by the DG. The internal shared storage consists of Row Buffers which store the display data and internal registers which store display parameters. There are two row buffers each capable of storing up to 200 characters. The data in one row buffer is used by the DG to display one complete character row on the screen, while the MCU is loading the second row buffer with display data fetched from memory. At the end of the row being displayed, the buffers are swapped and the MCU and DG resume their respective tasks.

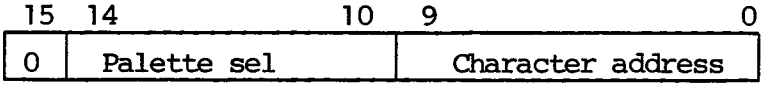
The Display Characteristics Registers contain all the information used to control every aspect of display characteristics from screen size to blink rates. A major portion of this registrer sets is the three Content Addressable Memory (CAM) arrays that allow very flexible timing control for row and screen characteristics. The user has the power to set the parameter for the entire screen by invoking a single high level command.

By separating the Video Interface clocks from the Bus Interface clock, the 82730 provides the designer the ability to independently maximize the performance of the CPU and Video sections of the system.

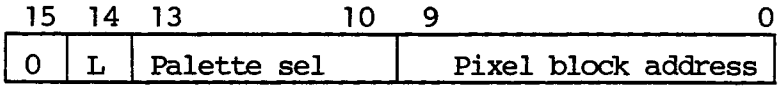
The Video interface constists of two independent clocks: the Reference Clock (RCLK) and the Character Clock (CCLK). While the RCLK controls the raster timing and defines the screen layout, the CCLK independently shifts character and attribute informationout of the 82730, which allows proportional spacing to be achieved.

It is this combination of hardware features and high level command interface that makes the 82730 the first VLSI Text Coprocessor which simplifies hardware design and software development.

The characters output from the DG have the following formats in alphanumeric mode:




or in graphic mode:




If bit 15 is 1, the character is a command to the 82730 and it is not output by the DG. The remaining 15 bits are used in the illustrated way, depending on the graphic/nongraphic mode. In

both cases, bits 0 to 9 are concatened to the video linenumber output by the DG and used as an address into the Character generator/Pixel memory.

In nongraphic mode, bits 10 to 14 are used to select a foreground/background - colourpair from the palette.

In graphic mode, bits 10 to 13 are used to select a colour quartet from the palette . In graphich mode bit 14 selects low resolution if 1.

In low resolution two dots are combined to one four state pixel being capable to have any of the four colours selected with bits 10 to 13. In high resolution, each dot being a two state pixel can have one of the two first colours in the quartet.

## 2.2.2 Pixel Memory

2.2.2

The Pixel memory has the task to supply the dot shifter with information. The address into the Pixel memory consists of 10 bits output from the refresh memory plus 4 bits scan linenumber from the 82730.

Pixel memory address:

| 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| character | | | | | | | | | | | scan line | | | |

bit 0 is not used, as 16 bit words are addressed.

Pixel memory address = 2* (video line number + 16* character).

The output word contains 16 bit and is used in three different ways controlled by the attribut.

A. character line:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| d | d | d | d | d | d | d | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

first displayed

One line of a 7 dots wide character is shown. The bits d are the dots of the character in the same order as on the screen (left to right). The zero in bit 8 succeeded by all ones are length designators. The character cannot be narrower than 7 and not wider than 15 dots.

B. High resolution graphic line:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| d | d | d | d | d | d | d | d | d | d | d | d | d | d | d | d |

first displayed

The bits d are all displayed in the indicated sequence. As in the nongraphic mode each d select one of two colours.

C. Low resolution graphic line:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $C_1$ | $C_0$ | $C_1$ | $C_0$ | $C_1$ | $C_0$ | $C_1$ | $C_0$ | $C_1$ | $C_0$ | $C_1$ | $C_0$ | $C_1$ | $C_0$ | $C_1$ | $C_0$ |

first displayed

The nipples ($C_1$, $C_0$) are displayed in the indicated sequence.

Each pixel occupies the space of two dots on the screen but can select one out of four colours (intensities) from the palette.

The Pixel memory has a size of 16K x 16bit or 32 K bytes and is accessible from the cpu as normal memory in the area F0000 to F7FFF Hex.

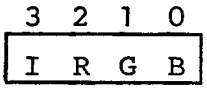
In graphic mode accesses to the Pixel memory may cause the CPU to go through a number of wait states before the memory becomes idle, because of the heavy load, the CRT imposes on it.

When nongraphic mode is selected, and narrower characters than 15 dots are displayed, the pixel memory will be busy serving the CRT all other time but during the retraces. This would give very long latencytimes and hence waiting times for the CPU with normal programmed accesses to the pixel memory, so in this mode it is recommended to access the pixel memory via DMA or with the 82730 stopped.

## 2.2.3 Palet

2.2.3

The output of the dot shifter is used to select one of two or four colours or intensities from a Palet. The Palet has room for 32 4 bit nibbles. The nibbles has the following meaning:




if I is set the Intensity is increased.
if R is set the Red beam is turned on.
if G is set the Green beam is turned on.
if B is set the Blue beam is turned on.

this gives the following effects:

| value of the colour nipple | IRGB | colour | intensity (B&W) |
|---|---|---|---|
| 0 | 0000 | Black | zero |
| 1 | 0001 | Blue | |
| 2 | 0010 | Green | |
| 3 | 0011 | Cyan | not defined |
| 4 | 0100 | Red | |
| 5 | 0101 | Magenta | |
| 6 | 0110 | Brown | |
| 7 | 0111 | Ligh gray | normal |
| 8 | 1000 | Dark gray | low |
| 9 | 1001 | Light blue | |
| 10 | 1010 | Light green | |
| 11 | 1011 | Light cyan | not defined |
| 12 | 1100 | Light red | |
| 13 | 1101 | Light magenta | |
| 14 | 1110 | Yellow | |
| 15 | 1111 | White | high |

The palet is written with a write instruction to the area 10 base + 180 to 1BF Hex.

The illustration shows which colour pairs are accessed on which addresses.

The number inside the boxes refer to the identity of the palette cells.

| Address | | bit | 7 6 5 4 | 3 2 1 0 |
|---|---|---|---|---|
| I/O base + | 180 | | 1 | 0 |
| | 182 | | 3 | 2 |
| | 184 | | 5 | 4 |
| | 186 | | 7 | 6 |
| | 188 | | 9 | 8 |
| | 18A | | 11 | 10 |
| | 18C | | 13 | 12 |
| | 18E | | 15 | 14 |
| | 190 | | 17 | 16 |
| | | | | |
| | | | | |
| | 1B4 | | 53 | 52 |
| | 1B6 | | 55 | 54 |
| | 1B8 | | 57 | 56 |
| | 1BA | | 29 | 58 |
| | 1BC | | 61 | 60 |
| | 1BE | | 63 | 62 |
| | | | I R G B | I R G B |

When accessed by the crt controller, the palet is organized in the following ways:

alphanumeric attribute

| | | |
|---|---|---|
| 0 | 1 | 0 |
| 1 | 3 | 2 |
| 2 | 5 | 4 |
| 3 | 7 | 6 |
| 4 | 9 | 8 |
| 5 | 11 | 10 |
| 6 | 13 | 12 |
| 7 | 15 | 14 |
| | | |
| | | |
| 25 | 51 | 50 |
| 26 | 53 | 52 |
| 27 | 55 | 54 |
| 28 | 57 | 56 |
| 29 | 59 | 58 |
| 30 | 61 | 60 |
| 31 | 63 | 62 |
| | I R G B | I R G B |
| | d=1 | d=0 |

High resolution graphics:

attribute =

| | | |
|---|---|---|
| 0 | 1 | 0 |
| 1 | 3 | 2 |
| 2 | 5 | 4 |
| 3 | 7 | 6 |
| | | |
| | | |
| 13 | 27 | 26 |
| 14 | 29 | 28 |
| 15 | 31 | 30 |
| | I R G B | I R G B |
| | d=1 | d=0 |

Low resolution graphics:

| attribute | | | | | |
|---|---|---|---|---|---|
| | 16 | 33 | 32 | 1 | 0 |
| | 17 | 35 | 34 | 3 | 2 |
| | 18 | 37 | 36 | 5 | 4 |
| | 19 | 39 | 38 | 7 | 6 |
| | | | | | |
| | | | | | |
| | 27 | 59 | 58 | 27 | 26 |
| | 29 | 61 | 60 | 29 | 28 |
| | 31 | 63 | 62 | 31 | 30 |
| | | I R G B | I R G B | I R G B | I R G B |
| | $(C_1, C_0)$ = | 11 | 10 | 01 | 00 |

Classical attributes as blinking, non displayed, inverse or intensified may be implemented by loading proper colour values into the different palet cells.

E.g. nondisplayed is obtained by having an palette selector selecting a set of palet cells containing some colour in foreground and background (for d=1 and d=0), and a blinking attribute is maintained by changing the foreground five or six times per second.

## 2.2.4 CRT Timing

2.2.4

The 82730 takes care of the CRT timing i.e. the Vertical and Horizontal sync pulses and the visible picture field. These timing pulses are generated from a 1,25 MHz clock called RCLK (see Intel 82730 manual). Various constant must be programmed into the 82730 at initialization time. These constants indicate duration of a videoline, position and with a sync pulse, start and stop at visible field in terms of RCLK counts.

For a 720 dot per videoline-screen, the visible part of the video line should have a duration of 45 RCLK's.

### 2.2.5 Graphic Mode 2.2.5

If bit 6 in the output register C of the 8255 PPI is set to 1 graphic mode is selected. For access of 8255 PPI see chapter 10.

### 2.2.6 Display Kind Indication 2.2.6

Bit 6 and 5 in port B of the PPI (see chapter 10) are used to indicate which kind of Display is connected to the system.

Bit 5 = 0 indicates a colour display is attached.
Bit 5 = 1 indicates a monochrome display.
Bit 6 = 0 indicates a linefrequency of 15,625 KHz
Bit 6 = 1 indicates a linefrequency of 22 KHz

### 2.2.7 CRT Interrupt 2.2.7

The 82730 may be programmed to generate interrupt on several conditions. Interrupts from 82730 are connected to the Int 4 input of the 8259.

## 3. KEYBOARD 3.

The keyboard is connected to the system via a special serial port on address 10 base + 20 Hex. When a character is received, an interrupt is generated (IR1 activated), and no further characters will arrive before the character is read.

The powersupply to the keyboard is controlled by means of bit 7 in the C register of the PPI (see chapter 10).

If bit 7 is set to 1, the KB power is on.
If bit 7 is set to 0, the KB power is off.

Within 0,5 - 1,0 sec. after power-up, the keyboard must be read in order to initalize the keyboard-receiver circuit.
Approximately 2 sec. after power-up, the keyboard will transmit a self-test-complete code, or 1 to 3 errorcodes. The next transmitted character, will be the character, identifying the version of the keyboard (Nationality code).

## 4. NON VOLATILE MEMORY 4.

The "NVM" is made up by a 256 by 4 bit CMOS RAM with battery backup.

The NVM is divided into 4 blocks of 64 words by 4 bits each. One of the four blocks is selected by means of bit 6 and 7 in port A or the PPI (see chapter 10).

Inside the selected block, the 64 words are accessible on the even addresses from I/O base + 80 to I/O base + FE.

The four bits is connected to bits 0 to 3 of the I/O bus.

When accessing the NVM, 3 wait-states must be used, i.e. 3 wait-states must be programmed into the CPU.

## 5. REAL TIME CLOCK 5.

The Real Time Clock is a CMOS LSI chip with battery backup, which allows the clock to continue the counting when the system is powered down.

The Real Time Clock (RTC) is a very "slow" device, so a special read and write procedure is to be performed.

In the following description of the procedures, A is indicating the internal addresses on the registers and latches containing the time information.

### Read the RTC

| ADD. | OPERATION | | DATA BUS | |
|---|---|---|---|---|
| I/O BASE + | WRITE | READ | BIT NO. 76543210 | COMMENTS |
| 5C H | X | | 100A 4A 3A 2A 1A 0 | Put on the address of the desired register or latch |
| 5C H | X | | 101A 4A 3A 2A 1A 0 | Create an internal read-pulse |
| | WAIT FOR 1µS (2 internal CPU Cycles) | | | |
| 5C H | | X | RTC DATA | Read data from RTC |
| 5C H | X | | 100A 4A 3A 2A 1A 0 | Remove the internal read-pulse |

Write to the RTC

| ADD. I/O BASE + | OPERATION WRITE READ | DATA BUS BIT NO. 76543210 | COMMENTS |
|---|---|---|---|
| 5C H | X | 000A 4A 3A 2A 1A 0 | Put on the address of the desired register or latch |
| 5A H | X | RTC DATA | Write data to RTC |
| 5C H | X | 010A 4A 3A 2A 1A 0 | Create an internal write-pulse |
| WAIT FOR 1µS (2 internal CPU Cycles) | | | |
| 5C H | X | 000A 4A 3A 2A 1A 0 | Remove the internal write-pulse |

Two (2) types of RTC's can be used in RC750. The programmer must therefore make a destination between the two types.

Which type there is actually used can be seen from bit no. 5 in the input point located in I/O base + 220H.

When bit no. 5 in I/O base + 220H is "1" the following description of the internal registers and batches will be valid.

| Internal Addr. Bit no. A4 | A3 | A2 | A1 | A0 | (HEX) | Function | READ WRITE |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | (00) | C Seconds * 0.0001 | |
| 0 | 1 | 0 | 0 | 0 | (08) | L | |
| 0 | 0 | 0 | 0 | 1 | (01) | C Seconds * 0.01 | |
| 0 | 1 | 0 | 0 | 1 | (09) | L | |
| 0 | 0 | 0 | 1 | 0 | (02) | C Seconds | |
| 0 | 1 | 0 | 1 | 0 | (0A) | L | |
| 0 | 0 | 0 | 1 | 1 | (03) | C Minutes | |
| 0 | 1 | 0 | 1 | 1 | (0B | L | R/W |
| 0 | 0 | 1 | 0 | 0 | (04) | C Hours | |
| 0 | 1 | 1 | 0 | 0 | (0C) | L | |
| 0 | 0 | 1 | 0 | 1 | (05) | C Day of week | |
| 0 | 1 | 1 | 0 | 1 | (0D) | L | |
| 0 | 0 | 1 | 1 | 0 | (06) | C Day of month | |
| 0 | 1 | 1 | 1 | 0 | (0E) | L | |
| 0 | 0 | 1 | 1 | 1 | (07) | C Months | |
| 0 | 1 | 1 | 1 | 1 | (0F) | L | |
| 1 | 0 | 0 | 0 | 0 | (10) | Interrupt Status | R |
| 1 | 0 | 0 | 0 | 1 | (11) | Interrupt Control | W |
| 1 | 0 | 0 | 1 | 0 | (12) | C reset | W |
| 1 | 0 | 0 | 1 | 1 | (13) | L reset | W |
| 1 | 0 | 1 | 0 | 0 | (14) | Status bit | R |
| 1 | 0 | 1 | 0 | 1 | (15) | "GO" command | W |
| 1 | 0 | 1 | 1 | 0 | (16) | Standby Interrupt | W |
| 1 | 1 | 1 | 1 | 1 | (1F) | Test mode | |

L = latch C = counter.

The clock contains a counter chain counting from the crystal frequency of 32768 Hz down to one/year.

Moreover the clock contains a latch of same length and format as the counter.

Both the latch and the counter may be read and loaded at any time.

The counter and latch are constantly compared giving an interrupt (it enabled) when they are equal. This means that you may receive an interrupt on a certain millisecond this year.

Both counter and latch are divided into sections corresponding to normal decimal notation:

| 1 9 | 3 9 | 0 7 | 2 9 | 5 9 | 5 9 | 9 9 | 9 0 |
|---|---|---|---|---|---|---|---|
| Month | Day of M. | Day of W | Hour | Minute | Second | S*0.01 | S*0.0001 |

This illustration shows the maximum value of the single BCD digits (four bit groups), not the maximum value of the byte. These are different for

Month : 11
Day of M. : 31, 30, 29 or 28
Hour : 23

Three reset commands exist:

Latch reset
Counter reset and
"Go" command.

The latch reset and counter reset clear the byte specified by the data in the write command:

Only one bit may be set, and the byte to be cleared is pointed out as follows:

D0 : Sec. * 0.0001
D1 : Sec. * 0.01
D2 : Seconds
D3 : Minutes
D4 : Hours
D5 : Day of week
D6 : Day of month
D7 : Month

The same is done by writing a zero into the corresponding register.

By means of the "Go" command the second counter, and the "fraction of a second" counters are reset, to enable an exact starting time.

By setting one or more bits in the interrupt control register, interrupt will occur on IR3 on one or more of the following events:

D0 : Counter: = latch
D1 : sec. * 0.1: = 0
D2 : Seconds: = 0
D3 : Minutes: = 0
D4 : Hours: = 0
D5 : Day of week: = 0
D6 : Day of month: = 0
D7 : Month: = 0

(: =) means that the counter rolls over.

By reading of the status register, it can be deduced which of the above mentioned reasons had caused the interrupt.

After the time is read the statusbit in address 14 H should be read also. This bit is gated to D0 and indicates if the counters have changed during the read operation, making the reading unsafe.

When bit no. 5 in I/O base + 220H is "0" the following description of the internal registers and latches will be valid.

| Internal Addr. Bit no. A4 A3 A2 A1 A0 | Bit no. 3 in control-register | Function | READ WRITE |
|---|---|---|---|
| X X 0 1 0 | 0 | Seconds counter | R/W |
| X X 0 1 1 | 0 | Minutes counter | R/W |
| X X 1 0 0 | 0 | Hours counter | R/W |
| X X 1 0 1 | 0 | Date counter | R/W |
| X X 1 1 0 | 0 | Month counter | R/W |
| X X 0 1 0 | 1 | Seconds alarm latch | W |
| X X 0 1 1 | 1 | Minutes alarm latch | W |
| X X 1 0 0 | 1 | Hours alarm latch | W |
| X X 1 1 1 | | Control register | W |
| X X 1 1 1 | | Int. Status Register | R |

X = don't cares

Control register

This register controls the following:

Frequency select (B0, B1)
Start/stop (B2)
Counter/Latch Control (B3)
Clock select (B4, B5, B6, B7)

Control register:

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|

The frequency select bits (B0, B1) must always be 00 (zero). This indicates that the reference frequency used by the RTC will be 32768Hz.

The start/stop bit (B2) starts and stops the RTC. B2 = 1 starts the RTC. B2 = 0 stops the RTC.

The counter/latch control selects the counter or the latch function of a certain register.

B3 = "0" = "Write to counter and disable alarm"
B3 = "1" = "Write to latch and enable alarm".

If first B3 is set to "0" and then date is written to i.e. the address XX011 then the minutes counter is located. At the same time the alarm is disabled. I.e. that no RTC-interrupt will occur. When the contents of the counters matches the contents of the alarm latches. If the alarm is to be enabled the control register must be accessed and B3 set to "1". When data is written to address XX011 while B3="1" then the minutes alarm latch will be accessed.

The clock select bits (B7, B6, B5, B4) controls the rate of which interrupts occur.

An RTC-interrupt can be generated in two different ways: As described above an interrupt will occur when B3 in the control register is set to "1" and the content of the counters matches the content of the latches.

The second way to generate an RTC-interrupt is to choose a clock-signal (50% duty cycle) as the interrupt source. The following table shows the possible clock-signals.

| B7 | B6 | B5 | B4 | | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | disable | |
| 0 | 0 | 0 | 1 | 488,2 | µS |
| 0 | 0 | 1 | 0 | 976,5 | µS |
| 0 | 0 | 1 | 1 | 1953,1 | µS |
| 0 | 1 | 0 | 0 | 3906,2 | µS |
| 0 | 1 | 0 | 1 | 7812,5 | µS |
| 0 | 1 | 1 | 0 | 15,625 | µS |
| 0 | 1 | 1 | 1 | 31,25 | µS |
| 1 | 0 | 0 | 0 | 62,5 | µS |
| 1 | 0 | 0 | 1 | 125 | µS |
| 1 | 0 | 1 | 0 | 250 | µS |
| 1 | 0 | 1 | 1 | 500 | µS |
| 1 | 1 | 0 | 0 | Sel. | |
| 1 | 1 | 0 | 1 | Min. | |
| 1 | 1 | 1 | 0 | Hour | |
| 1 | 1 | 1 | 1 | Day | |

When an RTC-interrupt is detected the Interrupt status register can be read in order to determine the source of the interrupt.

When bit no. 7 (MSB) is set to "1" the interrupt source is the alarm. When bit no. 6 is set to "1" the interrupt source is the clock. Bit no. 0-5 in the Int. Status register will always be zero.

The counters and latches from seconds through months holds the time and alarm information in BCD.

The bit no. 7 (MSB) of the hours counter/latch irelicates AM and PM. The bit is set to "0" when AM and set to "1" when PM.

Bit no. 6 at the hours counter/latch determines 12 hours or 24 hours operation. When set to "1" the 12 hours operation is selected. When set to "0" the 24 hours operationis selected.

The bit no. 7 (MSB) of the month counter should be set to "1" when the year is a loop year.

## 6. SOUND DEVICE 6.

The sound generator creates sound to the loudspeaker located in the CRT monitor enclosure.

The Sound Generator (SOGE) is a write-only register. A special write-procedure must be performed to ensure that the SOGE accepts the written data.

Write Procedure

| ADD. | OPERATION | | DATA BUS | |
|---|---|---|---|---|
| I/O BASE + | WRITE | READ | BIT NO. 76543210 | COMMENTS |
| 56 H | | X | | Ignore the read data! |
| 5 CH | X | | 000XXXXX | Prepare the SOGE to receive data |
| 5 AH | X | | DATA TO SOGE | Write data to sound Generator |
| 56 H | X | | XXXXXXXX | Create a write-pulse to SOGE |

X = dont care

Four of the dividers are ten bit wide, and may be programmed individually to divide a frequency of 62,5 KHz with any integer in the range 1 to 1024. The outputs are square waves with 50% dutycycle, and fed into each their attennator.

The forth divider divides the 62,5 KHz with 16, 32 or 64 or just takes the output of the third of the above named dividers, and outputs the result into a pseudo random generator creating pink noise. The noise is fed into the fourth attenator. Each attennator can damp the input from 0 dB down to -28 dB in steps of 2 dB or turn the input entirely off.

The generator has registers for the control of the above mentioned functions:

| register | |
|---|---|
| 0 | tone 1 |
| 1 | tone 2 |
| 2 | tone 3 |
| 3 | noise |

The frequencies require two bytes for update:

| | bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| First byte | | 1 | tone | | 0 | f3 | f2 | f1 | f0 |

| | bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| Second byte | | 0 | X | f9 | f8 | f7 | f6 | f5 | f4 |

Where (f0-f9)+1 is the modulus for the selected divider.

The noise generator is programmed with one byte:

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 1 | 1 | 1 | 0 | X | FB | NF1 | NF0 |

Where FB selects noise type:

FB = 0: periodic noise
1: white noise and
NF selects "noise frequency":
NF 1,0 =
00: 3,90 KHz
01: 1,95 KHz
10: 0,98 KHz
11: output from tone 3.

The attennators are programmed with one byte each:

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 1 | generator | | 1 | A3 | A2 | A1 | A0 |

A0 to A3 control four stages at attennation:
A0 damps 2 dB when 1
A1 damps 4 dB when 1
A2 damps 8 dB when 1
A3 damps 16 dB when 1
if A0-A3 = 1111 the output is off.

The Sound Generator is a single-source, i.e. that one cannot always be sure on the presence of the Sound Generator. To detect wether the SOGE is present or not, the following procedure can be performed.

Present Detection

| ADD. I/O BASE + | OPERATION WRITE | OPERATION READ | DATA BUS BIT NO. 76543210 | COMMENTS |
|---|---|---|---|---|
| 5 CH | X | | 000XXXXX | Prepare the SOGE to receive data |
| 5 AH | X | | 11111111 | Write data to SOGE |
| 56 H | X | | XXXXXXXX | Create a write-pulse to the SOGE |

X = dont care

Within 10 µS after the above described procedure, a read-operation should be performed to I/O base + 210 H. If bit no. 7 in the read data is zero (0), then the Sound Generator is present. If the Sound Generator is not present, sound can be made by using the CPU timer no. 1.

## 7. SERIAL COMMUNICATION 7.

An Intel 8274 chip makes up two full duplex seriel communication pathes, A and B. Path A has both V24 and X21 interface on it while patch B has only V24, and is intended mainly as a port for printer attachment. The programming of 8274 is described in the intel reference manual.

Channel A is accessed via the addresses I/O base + 30 and I/O base + 34, and channel B is accessed via the addresses I/O base + 32 and I/O base + 36:

I/O base + 30 data register channel A
I/O base + 32 data register channel B
I/O base + 34 control register channel A
I/O base + 36 control register channel B.

Two DMA Request inputs are assigned to the 8274:

DRQ 1 : Transmitter channel A
DRQ 2 : Receiver channel A

The interrupt is connected to the INT1 input on the CPU, and INTA1 out of the CPU is connected to 8274.

The serial clock inputs to the A channel may be slected either from the 8254 timer outputs (0 for RX, 1 for TX) CR from the Xmt clock and Rec clock pins on the port terminals. The selection is made by loading bit 4 in PPI port C (see chapter 10):

Bit 4 = 0 selects 8254 timer outputs for transmit- and receive-clock.

The T0 output is the clock for the B channel.

Channel A and B each has two extra modem signals, Data Set Ready and Calling Indicator Which may be read from a parallel input on address I/O base + 210 hex as follows:

bit 2: calling Indicator Ch. A
bit 3: Data Set Ready Ch. A
bit 4: Calling Indicator Ch. B
bit 5: Data Set Ready Ch. B

The 8254 timer

Contains three programmable counter timers.

Timer 0 and 1 are used for channel A Receive and transmit baud rate generators respectively.

Timer 2 is used as a 50 mS one shot (mode 1) counting from a 1 Mhz clock.

Timer 0 and 1 are used as programmable rate generators (mode 3) counting from a 4 Mhz clock.

The timer registers have the following I/O addresses:

| | |
|---|---|
| Counter 0 | I/O base + 40 |
| Counter 1 | I/O base + 42 |
| Counter 2 | I/O base + 44 |
| Control word | I/O base + 46 |

For further information on programming the 8254 timer, see Intel Component data Catalog.

## 8. FLOPPY DISC CONTROLLER 8.

The floppy disc controller is based on the WD 1797 controller chip and supports the following.

- Up to two 5 1/4 inch drives connected in daisy chain
- Data transfer by DMA
- 8" compatible 5 1/4 inch drives
- Dual Side/Single Density 125 kbps, FM
  Dual Side/Dual Density 250 kbps, MFM
  Dual Side/Quadriple Density 250 kbps, MFM
  Dual/Side/Dual Density 500 kbps, MFM
- Multisector transfer capability
- Programmable Write Precompensation

## 8.1 FDC/CPU I/O Interface 8.1

The floppy disc controller (FDC) and an external control register (FCR) (for clock selection, precompensation, motor on/off and drive select) are accessed by I/O commands as follows:

| I/O Base addr. offset (HEX) | I/O | FUNCTION |
|---|---|---|
| 200 | I | Read FDC Status Register |
| | O | Write Control Command. |
| 202 | I | Read FDC TRACK Register |
| | O | Write FDC TRACK Register |
| 204 | I | Read Sector Register |
| | O | Write Sector Register |
| 206 | I | Read Data Register |
| | O | Write Data Register |
| 210 | O | Write FCR Register |
| | I | Not defined |

For further information on programming the registers on addr 200-206 refer to Western Digital data sheet on WD1797.

The FCR register has the following layout:

| Bit-No (0 = LSB) | Name | Description |
|---|---|---|
| 0 | Drive sel. | Selects between drives, a o selects drive O. A drive is only selected if its motor is on. |
| 1 | Motor 0. | |
| 2 | Motor 1. | 0: Motor OFF, 1: Motor ON. |
| 3 | Precomp Enable | Write precompensation 0: Disabled 1: Enabled |
| 4 | Precomp ensation. | 0: 125 nsec<br>1: 250 nsec. |
| 5 | -,DD | 0: Dual density<br>1: Single density |
| 6 | 2 MHz | WD 1797 Clock select<br>0: 1 MHz (5 1/4")<br>1: 2 MHz ( 8") |
| 7 | READY CONTROL | 0: Ready from drive<br>1: Ready always set |

Precompensation is only used in MFM-mode and is normally applied in the following way.

| CYLINDER NO | PRECOMPENSATION |
|---|---|
| 0-43 | 125 nsec. |
| 44-77 | 250 nsec. |

This control sceme may be refined as required by the actual drives.

the floppy disc controller is normally initialized to transfer data in DMA-mode and then requires a DMA channel to be allocated (to DMA request 5).

## 9. SCSI (SASI) 9.

Small Computer System Interface (ref. ANSI X3T9.2/82-2 Rev. 3.

The SCSI interface is used for attachment of a winchester disc, and other intelligent peripherals.

The optional busarbitration is not implemented.

The controller contains a data port accessible via I/O address 10 + I/O base.

The input port on address I/O base + 72 contains the following bits, which when read reflect the momentary state of the corresponding bus signals.

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | undefined | | | C/D | BSY | I/O | MSG | RST |

State of the corresponding bus signal.

The outputport C on the 8255 address I/O base + 74 or 10 base + 76 (see chapter 10) contains the following flip flops

| 3 | 2 | 1 | 0 |
|---|---|---|---|
| SEL | EXP I/O | ANT | RST |

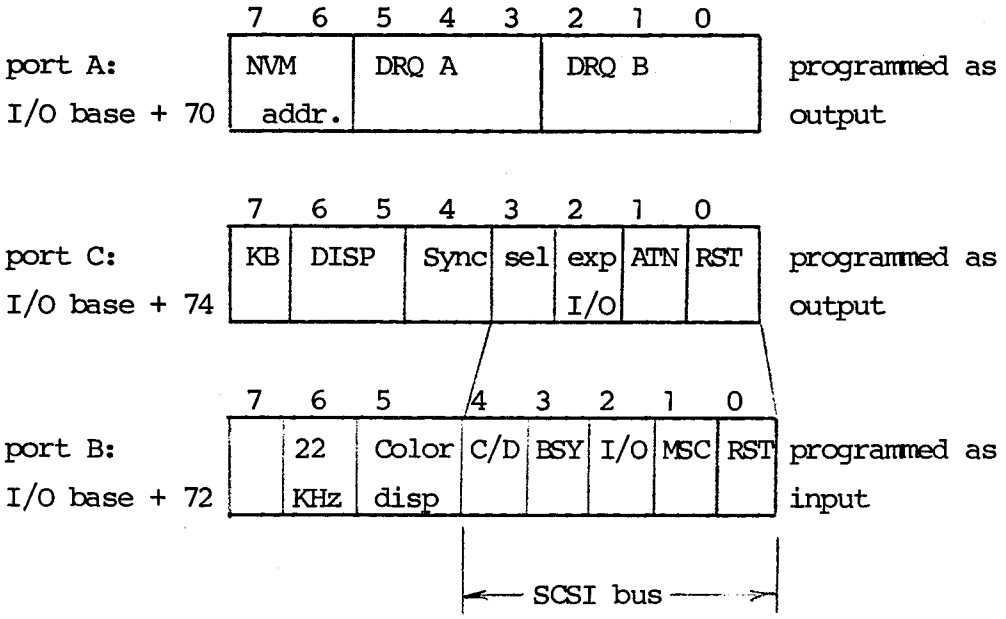
The three signals SEL, ATN and RST are directly output on the bus. The flip flop "exp I/O" is used to control the DMA as follows:

A datatransfer request from the SCSI bus (C/D=0) gives rise to a DMA request if the state of the I/O line matches with the state of the exp I/O flip flop, else an interrupt is generated.

A transfer request with C/D = 1 generates an interrupt. A read or Write to address I/O base + 10 generates an ACK on the SCSI bus.

## 10. PPI 8255 10.

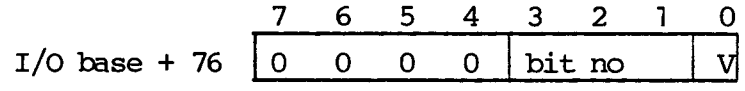
The parallel ports in the 8255 connected to the addresses I/O base + 70 to 10 base + 76 are used in the following way:




The controlregister in address I/O base + 76 should initially be loaded with the following contents

I/O base + 76: 10000010

The bits in port C may be set/reset individually in the following way:




The value of V is loaded into port C (bit no).

## 11. PARALLEL (PRINTER) INTERFACE 11.

The parallel interface is primarily intended for connecting a printer, but may also be used as a general input/output port.

The interface consists of 4 registers.

- Data output register, directly controlling the data pins if enabled.
- Data input port reflecting the state of the data pins at the time of reading.
- Control output register directly controlling four control output pins and enables data output register and interrupt.
- Status read register reflecting the state of 8 control/status pins at the time of reading.

Register I/O addresses relative to I/O-base:

data output : 250 (hex)
Data input : 250 (hex)
Control output: 260 (hex)
Status input : 260 (hex)

The registers have the following layouts:

Data output register (OUT 250H)

| BIT | CONNECTOR PIN NO | DESCRIPTION |
|---|---|---|
| 0 | 2 | If the output register is enabled (control reg. |
| 1 | 3 | bit 4 = 0) then a bit in the register directly |
| 2 | 4 | controls the corresponding connector pin as |
| 3 | 5 | follows: |
| 4 | 6 | |
| 5 | 7 | Bit state TTL output |
| 6 | 8 | 0 LOW |
| 7 | 9 | 1 HIGH |

Data input port (IN 250H)

| BIT | CONNECTOR PIN NO | DESCRIPTION |
|---|---|---|
| 0 | 2 | Read back of data output register, or if this is |
| 1 | 3 | disabled the state of the connector pins. |
| 2 | 4 | |
| 3 | 5 | |
| 4 | 6 | |
| 5 | 7 | |
| 6 | 8 | |
| 7 | 9 | |

| PIN-TTL LEVEL | BIT STATE READ |
|---|---|
| LOW | 0 |
| HIGH | 1 |

Control register (OUT 260 H)

The four LSB (bit 0-3) of this register are connected through open collector inverters to corresponding connector pins (all four having 4.7 K ohm pull up resistors to +5V).

| BIT NO. | SIGNAL (PIN NO) | DESCRIPTION |
|---|---|---|
| 0 | -,STROBE (1) | See above |
| 1 | -,AUTOLF (14) | See above |
| 2 | -,INIT (16) | See above |
| 3 | -,SELECT (17) | See above |
| 4 | OUT DISABLE | Output register disable<br>if 0: enables output register line drivers<br>if 1: three-states the output register and allows pins 2-9 to be used for inputs. |
| 5 | | NOT USED |
| 6 | | NOT USED |
| 7 | INT. DISABLE | Parallel interrupt disable<br>if 0: enables interrupts (INT. CONTROLLER INPUT 6) when BUSY input pin (11) is LOW.<br>if 1: disables interrupts. |

Status input port (IN 260H)

Each bit in this port represents the inverse state of a pin in the connector. The 5 LSB are inputs only while the 3 MSB inputs the state of 3 open collector.

| BIT NO. | CONNECTOR PIN NO. | SIGNAL DESCRIPTION | |
|---|---|---|---|
| 0 | 11 | NOT BUSY | : 0 when input signal, BUSY is high |
| 1 | 10 | ACK | : 0 when input signal is high |
| 2 | 15 | FAULT | : 0 when input signal is high |
| 3 | 12 | NOT PAPER END | : 0 when input signal is high |
| 4 | 13 | NOT SELECTED | : 0 when input signal is high |
| 5 | 1 | STROBE | : 0 when input signal is high |
| 6 | 16 | INIT | : 0 when input signal is high |
| 7 | 17 | SELECT | : 0 when input signal is high |

## 12. ADDRESSES 12.

| IO area | Peripheral | Direction | Interrupt | DMA request |
|---|---|---|---|---|
| IO base + 0 | 8259 Interrupt ctr | | | |
| IO base + 10 | SCSI data reg | I/O | 2 | 0 |
| IO base + 20 | Keyboard | I | 1 | |
| IO base + 30 | Comm. | I/O | | 1 |
| IO base + 32 | ch. A | I/O | INT1 on the CPU | |
| IO base + 34 | Comm. | | | 2 |
| IO base + 36 | ch. B | | | |
| IO base + 40 | 8254 timer | I/O | | |
| IO base + 50 | Sound + real time clock | O | 3 | |
| IO base + 60 | CRT control | O | 4 | 3 |
| IO base + 70 | NVM + DMA sel | O | | |
| IO base + 72 | SCSI + Comm | I | | |
| IO base + 74 | SCSI + control | O | | |
| IO base + 76 | Control for 70-74 | O | | |
| IO base + 80 to FE | NVM | I/O | | |
| IO base + 100 | Ch. AH to NET | | | |
| IO base + 180 to 19F | Palet | O | | |
| IO base + 200 | Floppy control | I/O | 0 | 5 |
| IO base + 202 | track | | | |
| IO base + 204 | sector | | | |
| IO base + 206 | data | | | |
| IO base + 210 | Floppy control | O | | |
| IO base + 210 | Amx inputs | I | | |
| IO base + 220 | Utility key | I | | |
| IO base + 230 | Reset Int CRT | | | |
| IO base + 240 | Ch. Att. | | | |

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