RCSL No: 99 0 00785

Edition: 1984.09.18

Author: Knud Erik Hansen

Title:

ACC601
Technical Manual

RCSL Nr. 46-F 0087

A/S REGNECENTRALEN
af 1979

Keywords: RC759, PICCOLINE, ACC601, Technical Manual

Abstract: This paper contains all documents necessary to service the ACC601, Asynchronous Communication Controller, to the RC759 Piccoline microcomputer.

iSBX is trademark of Intel Corporation.

(28 printed pages)

RCSL Nr. 46-F 0087

Printed by A/S Regnecentralen af 1979, Copenhagen

TABLE OF CONTENTS PAGE

1. INTRODUCTION 1.

This paper provides a functional description and circuit analysis of the ACC601 Serial Multimodule Board. The functional description includes details on the RS232C and RS422/449 communications interface signals, the interface signals between the Multimodule board and the host microcomputer, and the clock generation hardware on the Multimodule board. Figure 1 shows a Block Diagram of the Multimodule board.

Figure 2 shows the installation of ACC601 in the RC759 microcomputer.

2. SERIAL COMMUNICATION CHANNEL INTERFACE 2.

The communications interface on the Multimodule board may be configured for either RS232C or RS422/449 operation via jumper modifications. Default wiring of the Multimodule board is for RS232C operation. To convert to RS422 /449 operation, move the 2 x 8-circuit shorting plugs from sockets U6 and U7 to U4 and U5.

CAUTION

Remove power from the Multimodule board before moving the shorting plugs. When installing the plugs, ensure that they are in the correct sockets for the desired mode. Failure to observe these precautions may damage the circuits.

The serial interface provides RS232C or RS422 buffers for eight lines; Data In, Data Out, Request to Send, Clear to Send, Data Set Ready, Data Terminal Ready, Receive Clock, and DTE Transmit Clock. All necessary driver and receiver chips are supplied with the board.

NOTE

The requirement to supply both RS232C and RS449 interfaces precludes the use of standard pin connection for the RS449 Terminal Timing (TT) clock signal. The TT signal is routed through two spare pins and the standard pins are unconnected. Special user-wiring is required to move the TT signal from the spare pins to the standard pins.

3. CPU Interface

3.

The interface between the host microcomputer and the Multimodule board consists of several signals that are defined in the following paragraphs. Each signal may be found in the schematic diagram included as figure 1 in this manual.

RESET (Reset). This active high input signal to the 8251A USART places the USART chip into the IDLE mode until a new set of control words is written to the chip.

MA0 (Address bit 0). This active high input to the 8251A USART and to the 8253 is used in conjunction with IORD/ and IOWRT/ signals to define which register on the 8251A or the 8253 is addressed.

MA1 (Address bit 1). This active high input signal to the 8253 is used in conjunction with MA0 to select one of the counters to be operated on in the 8253 and to address the control word register for mode selection.

IORD/ (Read). This active low input to the Multimodule board performs one of two functions depending on the chip selected. When low, IORD/ informs the 8251A that the host microcomputer is reading data or status from the 8251A, and it informs the 8253 that the host iSBX microcomputer is reading the values of the counter.

IOWRT/ (Write). This active low input to the Multimodule board may perform one of two funtions dependent on chip select. When low, IOWRT/ informs 8251A that the host microcomputer is writing data or control words to the 8251A. IOWRT/ also informs the 8253 that the host iSBC microcomputer is outputting mode information or loading counters.

MCS0/ (Chip Select). This active low input to the 8251A USART enables it to perform read and write operations. When MCS0/ is high, the USART data bus is held in a float state and the IORD/ and IOWRT/ signals do not effect the USART.

MCS1/ (Chip Select). This active low input to the 8253 PIT enables it to perform read and write operations. However, MCS1/ has no effect on the operation of the internal counters in the 8253.

MD0-MD7 (Bidirectional Data Bus). These active high I/O lines are Multimodule boards' tie-in to the host microcomputer data bus. MD0 through MD7 transfer data, commands, and status between the Multimodule board and the host microcomputer. MINTR0, MINTR1 (interrupt request lines). These active high output lines may be jumpered to Out0, or Out1 on the 8253, or to TxRDY on the 8251A.

OPT0, OPT1 (Option lines). These active high I/O lines are included to give the Multimodule board greater functional flexibility. These lines may be user-defined for special functions.

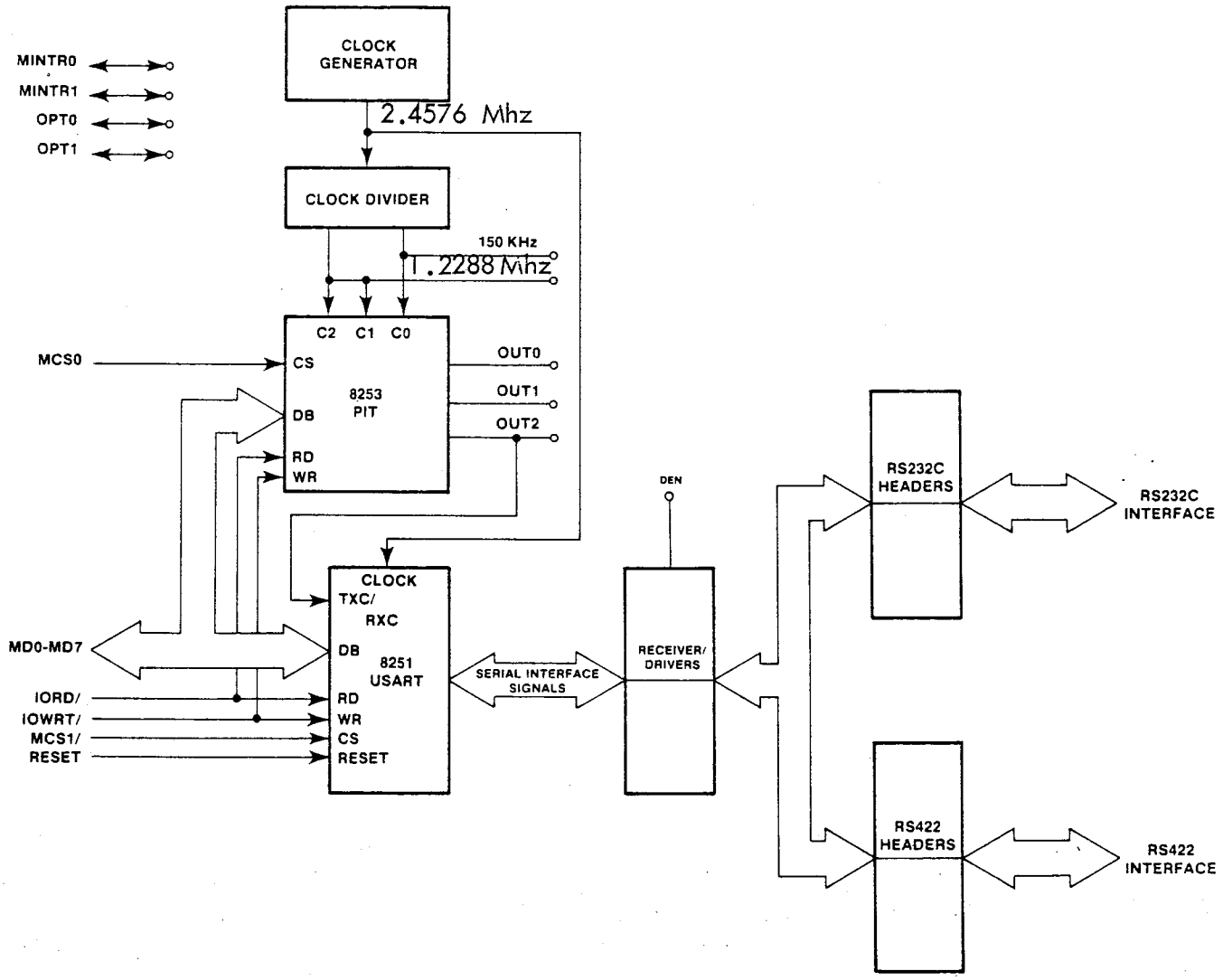


Fig. 1. ACC601 Block Diagram

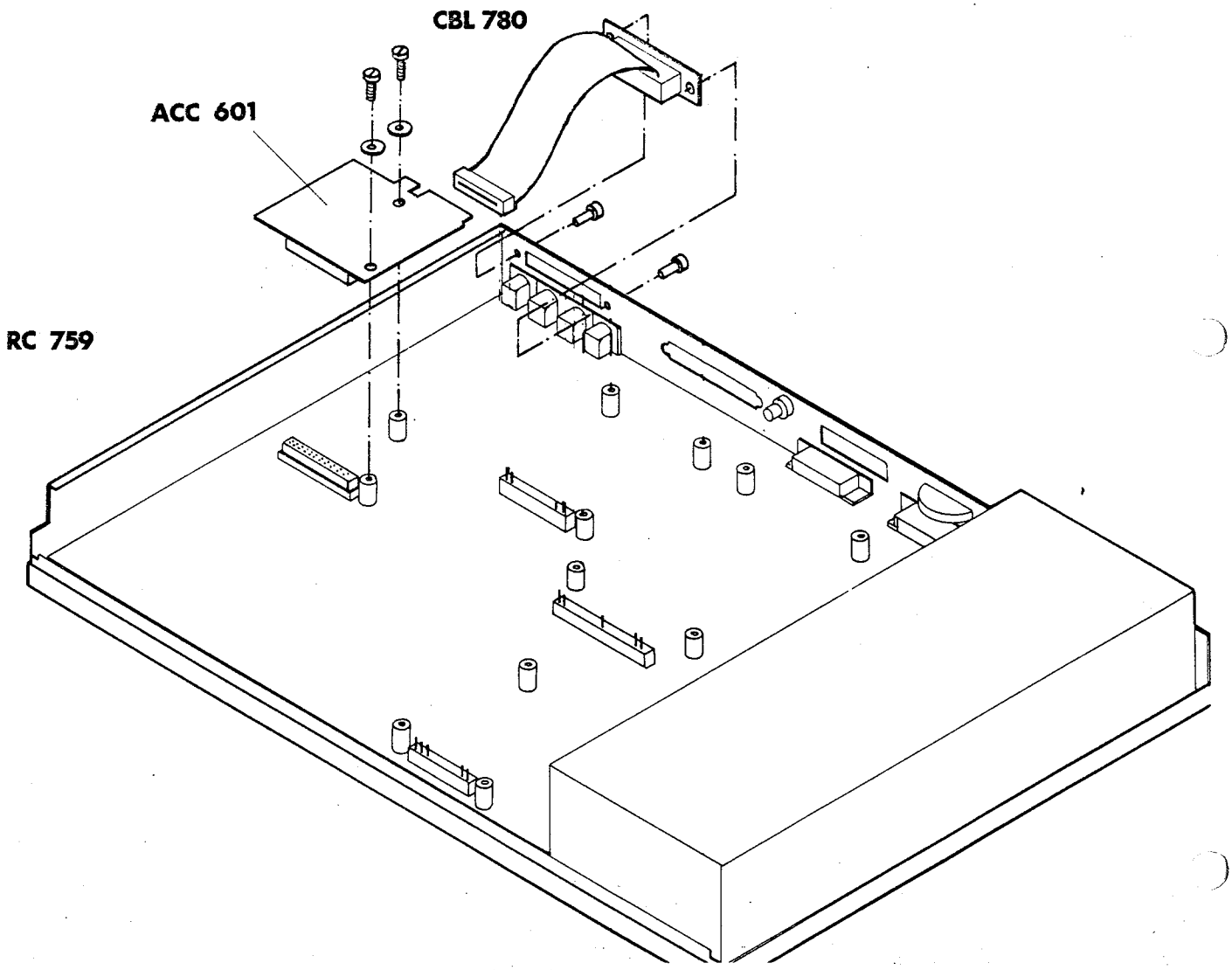


Fig. 2. ACC601 Installation

4. INTERFACE BUFFERING 4.

Interface buffering is provided by logic elements U1, U2 and U3. U1 is an input buffer that may be used with either RS232C or RS422 configuration, depending on the position of the mode selection header blocks. U2 provides RS422 output buffering, and U3 provides RS232C output buffering.

5. CLOCK GENERATION CIRCUITRY 5.

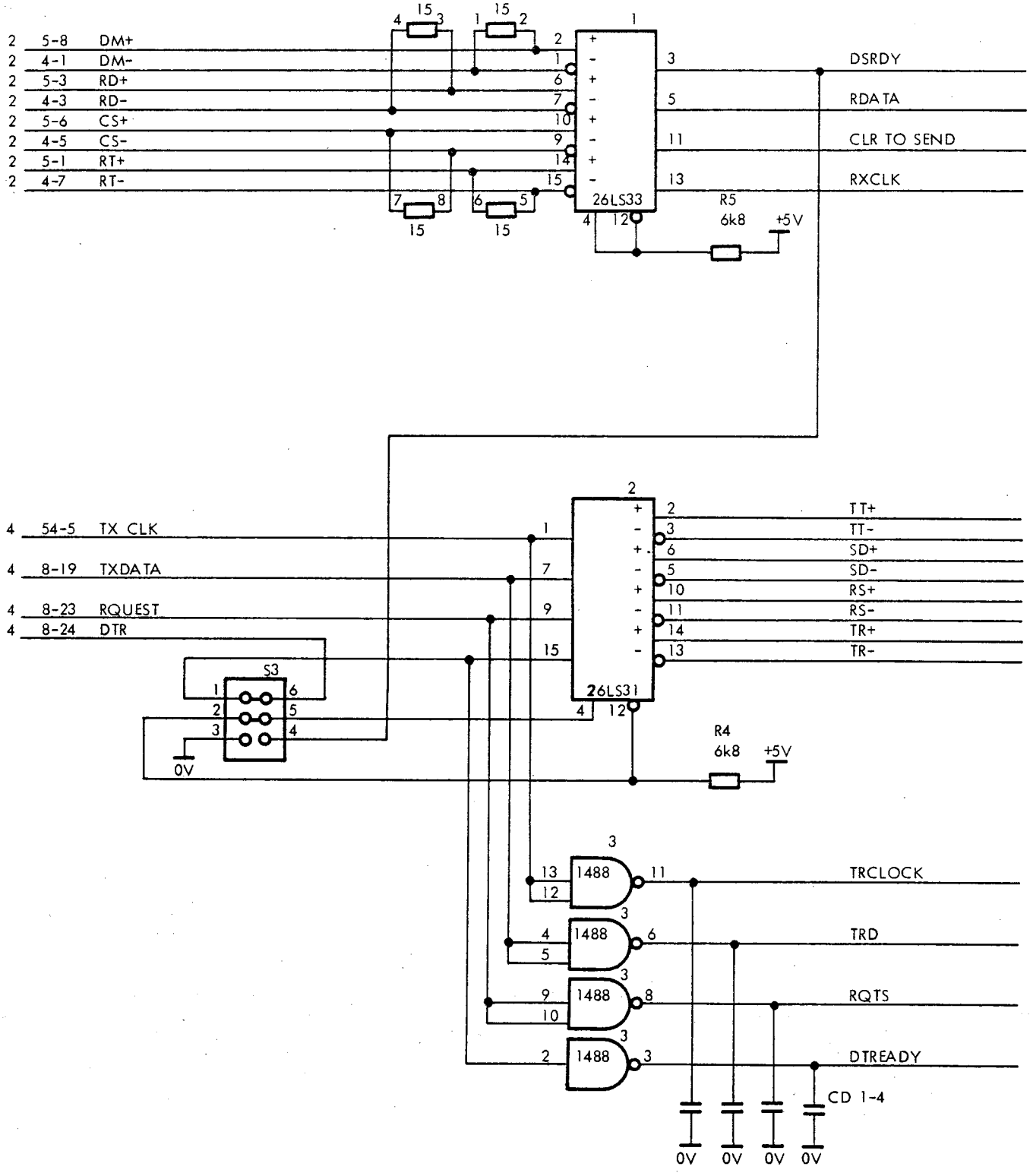
The Multimodule board includes an 8224 Clock Generator chip that creates a 2.46 MHz output from a 22.1148 MHz crystal input. The output is then passed through a 74LS161 Synchronous Four-Bit Counter which generates a 1.23 MHz clock and a 153.6 KHz clock to drive the 8253 PIT. The clock output frequency labeled OUT2, which is produced by the 8253 PIT, will vary according to the configuration and programming of the PIT.

The two remaining clock frequencies output from the 8253 PIT are jumper selectable to generate interrupts for the Multimodule board.

6. LOGIC DIAGRAMS

6.

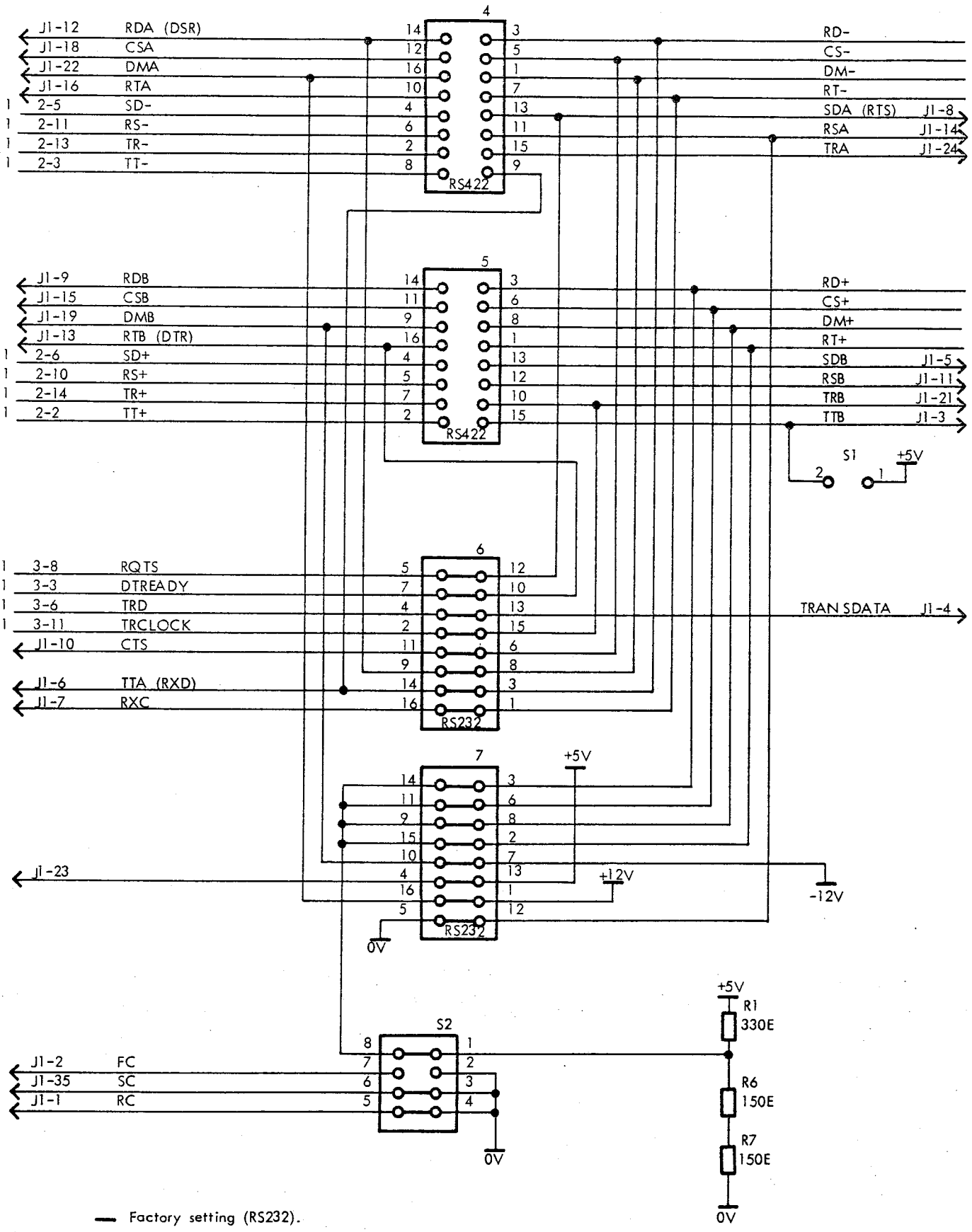
Signal name	Destination	Description
CLR TO SEND	p.4	CLeaR TO SEND. Input from the modem indicating that the transmitter can start.
DSRDY	p.4	Data Set ReaDY
DTREADY	p.2	Data Terminal READY. RS232 output.
RDATA	p.4	Received serial DATA.
RXCLK	p.4	Receiver timing input.
RS +/-	p.2	Request to Send. RS422 output.
RQTS	p.2	ReQuest To Send. RS232 output.
SD +/-	p.2	Send Data. RS422 output.
TT+/-	p.2	Terminal Timing. RS422 output.
TR +/-	p.2	Terminal Ready. RS422 output.
TRD	p.2	TRansmit Data. RS232 output.



840924 KNEH 840924 OKJ

15 and CD 1-4 are customer supplied and installed.

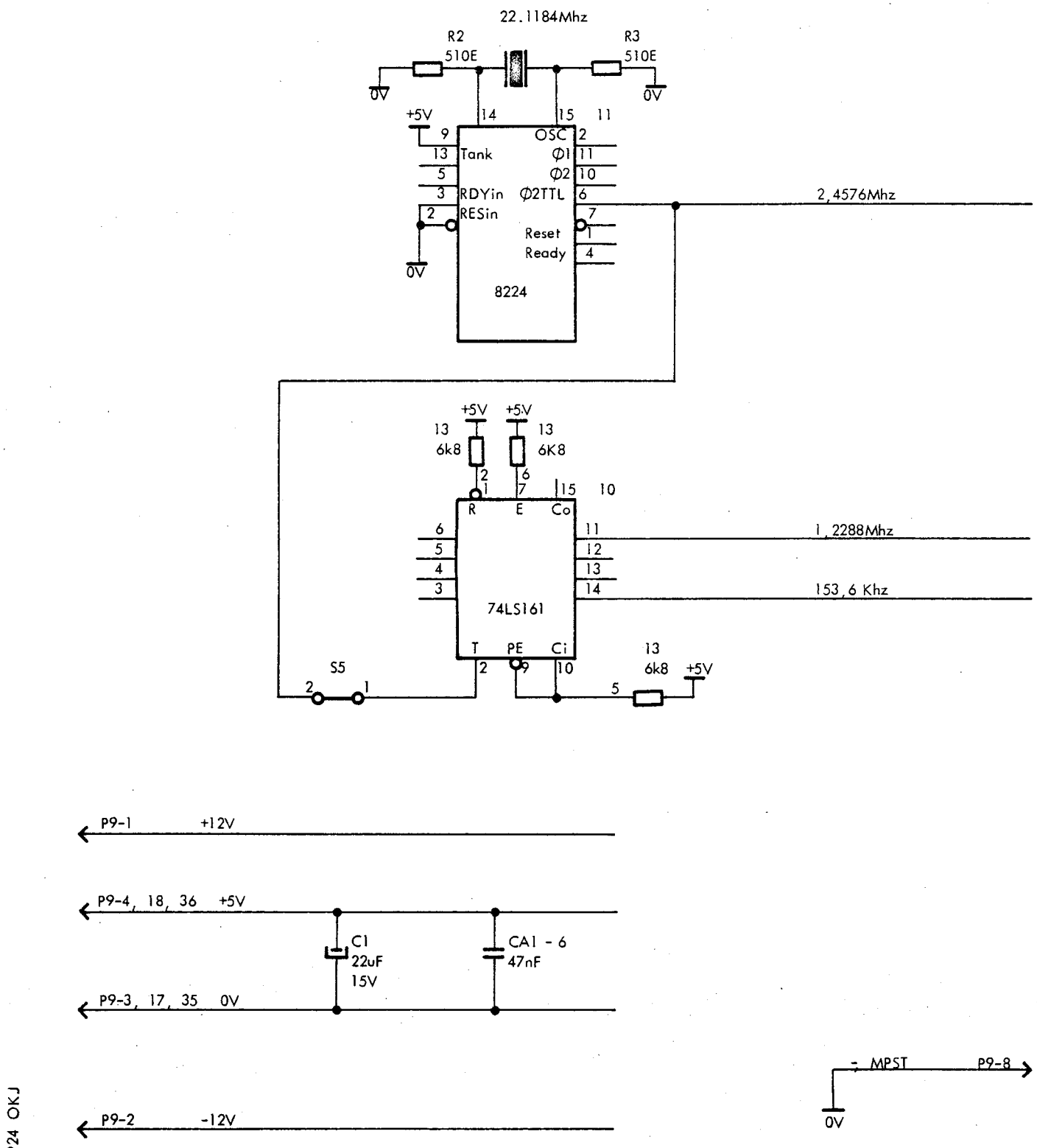
Signal Name	Destination	Description
CS +/-	p.1	Clear to Send. RS422 input.
DM +/-	p.1	Data Mode. RS422 input.
RD +/-	p.1	Receive Data. RS422 input.
RT +/-	p.1	Receive Timing. RS422 input.
RSA, RSB	J1	Request to Send.
SDA, SDB	J1	Send Data.
TRA, TRB	J1	Terminal Ready.
TTB	J1	Transmit Timing.
TRANS DATA	J1	TRANSmit DATA.



— Factory setting (RS232).

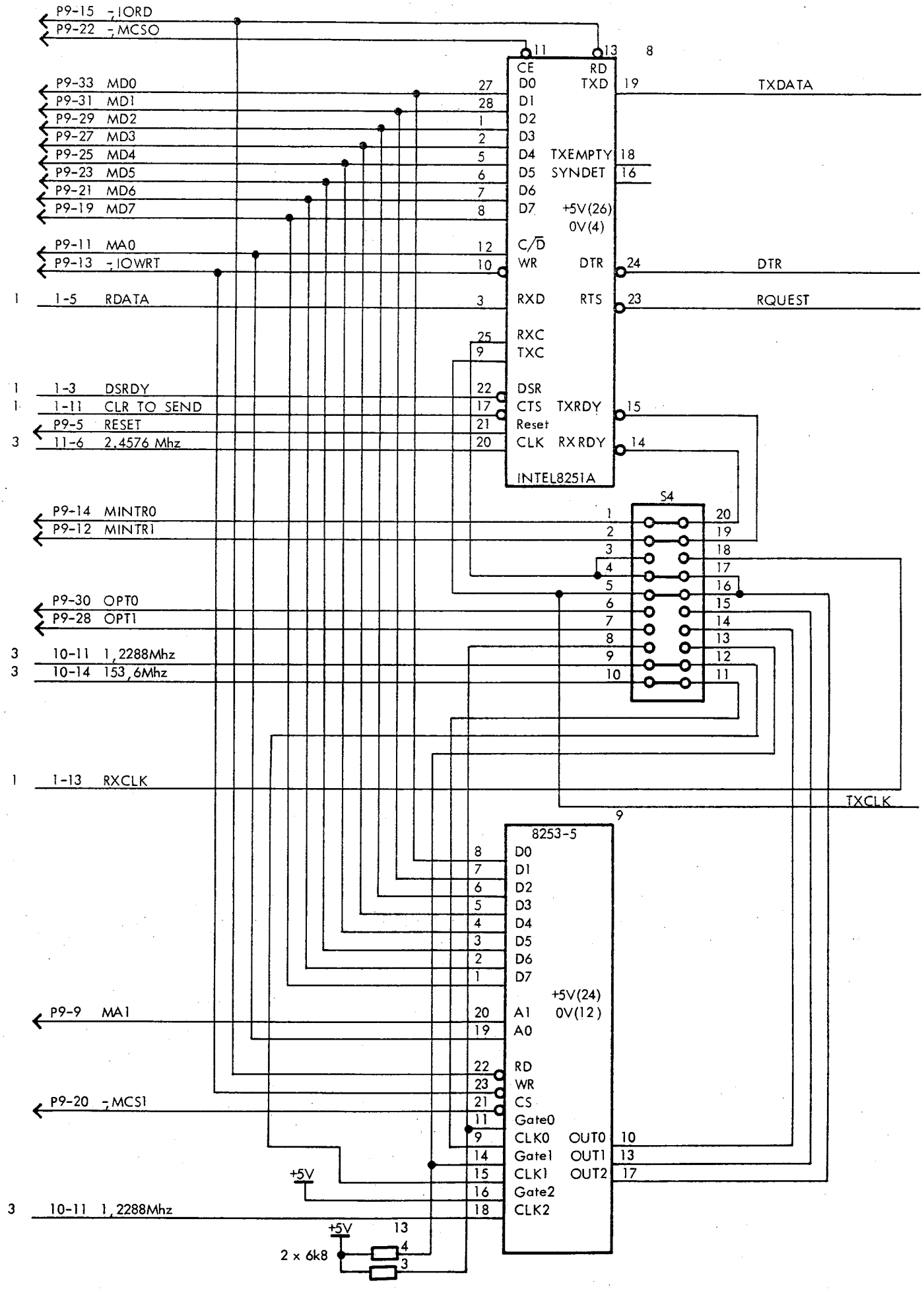
840924 KNEH 840924 OKJ

Signal Name	Destination	Description
2.4576MHZ	p.4	
1.2288MHz	p.4	
153.6KHZ	p.4	
/MPST	p.9	Module PreSenT



840924 KNEH 840924 OKJ

Signal Name	Destination	Description
DTR	p.1	Data Terminal Ready
RQUEST	p.1	ReQUEST to send.
TXDATA	p.1	Transmit DATA.
TXCLK	p.1	Transmit CLocK.



840924 KNEH 840924 OKJ

ACC601 USART Circuit and baud rate timer circuit p. 4.

A14689 Circuit Diagram

7. JACK/PLUG LIST 7.

Figure 3 shows the signals in the iSBX plug P9.

Figure 4 shows the interface connector J1.

Pin	Mnemonic	Description	Pin	Mnemonic	Description
35	GND	SIGNAL GROUND	36	+5V	+5 Volts
33	MD0	MDATA BIT 0	34	—	Reserved
31	MD1	MDATA BIT 1	32	—	Reserved
29	MD2	MDATA BIT 2	30	OPT0	OPTION 0
27	MD3	MDATA BIT 3	28	OPT1	OPTION 1
25	MD4	MDATA BIT 4	26	—	Reserved
23	MD5	MDATA BIT 5	24	—	Reserved
21	MD6	MDATA BIT 6	22	MCS0/	M CHIP SELECT 0
19	MD7	MDATA BIT 7	20	MCS1/	M CHIP SELECT 1
17	GND	SIGNAL GROUND	18	+5V	+5 Volts
15	IORD/	IO READ COMMAND	16	MWAIT/	M WAIT
13	IOWRT/	IO WRITE COMMAND	14	MINTR0	M INTERRUPT 0
11	MA0	M ADDRESS 0	12	MINTR1	M INTERRUPT 1
9	MA1	M ADDRESS 1	10	—	Reserved
7	—	Reserved	8	MPST/	M PRESENT
5	RESET	RESET	6	MCLK/	M CLOCK
3	GND	SIGNAL GROUND	4	+5V	+5 Volts
1	+12V	+12 Volts	2	-12V	-12 Volts

Fig. 3. iSBX Bus Connector (P9) Pin Assignment

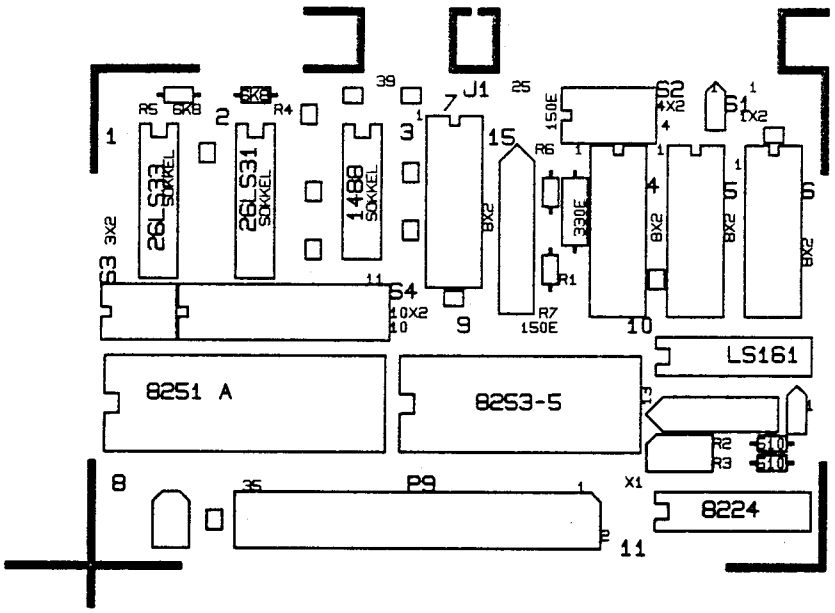
J1 Pin	RS232C Pin	ACC601 Support	RS232 Name	RS232 Function	RS422 Pin	ISBX 351 Support	RS449 Name	RS449 Function
1	14		(S) TXD	Secondary Transmit Data	20	YES	RC	Receive Common
2	1	YES	FG	Frame Ground	1	YES	Shield	Shield
3	15		DTE TXC	Transmit Clock	21	**	Spare	Terminal Timing (TT)
4	2	YES	TXD	Transmit Data	2		SI (I)	Signaling Rate Indicator
5	16		(S) RXD	Secondary Receive Data	22	YES	SD (N)	Send Data
6	3	YES	RXD	Receive Data	3	*	Spare (N)	Terminal Timing (TT)
7	17	YES	RXC	Receive Clock	23		ST (N)	Send Timing
8	4	YES	RTS	Request to Send	4	YES	SD (I)	Send Data
9	18		—	—	24	YES	RD (N)	Receive Data
10	5	YES	CTS	Clear to Send	5		ST (I)	Send Timing
11	19		(S) RTS	Secondary Request to Send	25	YES	RS (N)	Request to Send
12	6	YES	DSR	Data Set Ready	6	YES	RD (I)	Receive Data
13	20	YES	DTR	Data Terminal Ready	26	YES	RT (N)	Receive Timing
14	7	YES	SG	Signal Ground	7	YES	RS (I)	Request to Send
15	21		SQ	Signal Quality	27	YES	CS (N)	Clear to Send
16	8		DCD	Data Carrier Detect	8	YES	RT (I)	Receive Timing
17	22		RI	Ring Indicator	28		IS (I)	In Service
18	9		—	—	9	YES	CS (I)	Clear to Send
19	23	*	—	-12V Power	29	YES	DM (N)	Data Mode
20	10		—	—	10		LL (I)	Local Loopback
21	24	YES *	(TXC)	Ext Transmit Clock	30	YES	TR (N)	Terminal Ready
22	11	—	—	+12V Power	11	YES	DM (I)	Data Mode
23	25	*	—	+5V Power	31		RR (N)	Receiver Ready
24	12		(S) DCD	Secondary Data Carrier Detect	12	YES	TR (I)	Terminal Ready
25	N/C		—	—	32		SS (I)	Select Standby
26	13		(S) CTS	Secondary Clear to Send	13		RR (I)	Receiver Ready
35	N/C				37	YES	SC	Send Common
36	N/C				18		TM (I)	Test Mode
37	N/C				N/C		—	—
38	N/C				19	YES	SG	Signal Ground
39	N/C				N/C		—	—
40	N/C				N/C		—	—

NOTES:
* Non-standard usage of this line; used with TTX.
** Refer to paragraph 6.17.
(N) = Non-inverting signal.
(I) = Inverting signal.

Fig. 4. Connector J1 Pin Assignment

8. ASSEMBLY DRAWING

8.



PCB133 COMPONENT NOTATION

Fig. 5. Assembly Drawing

A. INDICES

A.1 Survey of Figures

RETURN LETTER

Title: ACC601 Technical Manual RCSL No.: 99 0 00785

A/S Regnecentralen af 1979/RC Computer A/S maintains a continual effort to improve the quality and usefulness of its publications. To do this effectively we need user feedback, your critical evaluation of this manual.

Please comment on this manual's completeness, accuracy, organization, usability, and readability:

Do you find errors in this manual? If so, specify by page.

How can this manual be improved?

Other comments?

Name:_____ Title:_____

Company:_____

Address:_____

Date:_____

Thank you

42-i 1288

..... Fold here .....

..... Do not tear - Fold here and staple .....

Affix
postage
here

REGNECENTRALEN
af 1979

Information Department
Lautrupbjerg 1
DK-2750 Ballerup
Denmark