
RCSL No: 99 0 00762

Edition: 1984.06.06

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Title:

TECHNICAL MANUAL
for
DPA701

Keywords:

RC759, Piccoline, DPA701, Technical Manual

Abstract:

This paper contains all technical information about DPA701, Disk/Printer Adapter to RC759.

(22 printed pages)

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1. INTRODUCTION

The DPA701 (Disk Printer Adapter) interfaces the Disk/Printer Unit (RC779) to the I/O bus of the RC759 central unit.

This adapter is placed as "baby-print" on the printed circuit board in the central unit in connector J8. The adapter is power supplied from this connector.

Figure 1 shows the Installation of DPA701.

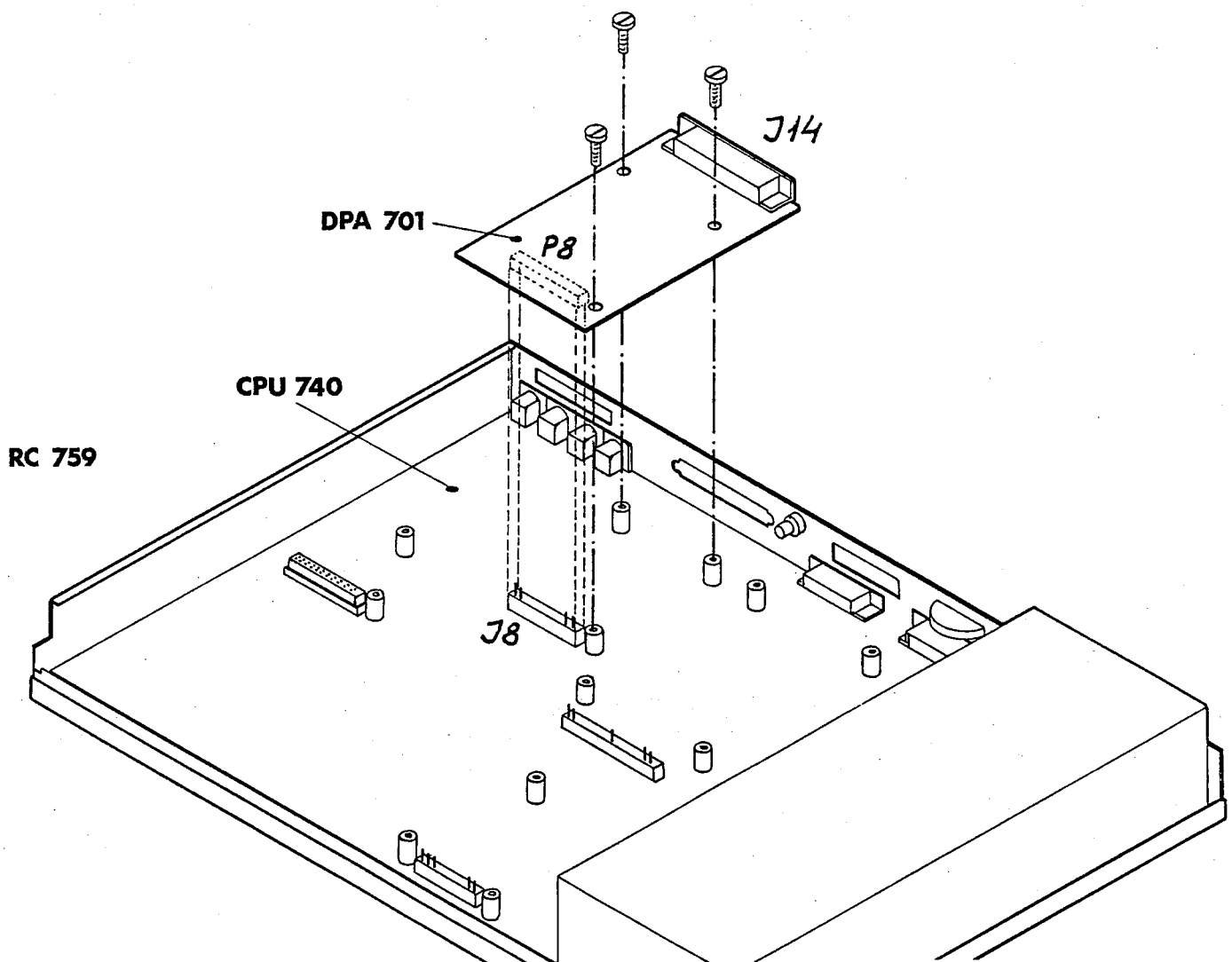


Fig. 1. Installation of DPA701

2. TECHNICAL DESCRIPTION

2.

Logical this adapter acts as a set of balanced drivers/receivers between the internal CPU I/O bus and the external bus to the Disk/Printer Unit.

26LS31 is used as driver circuit and 26LS32 as receiver unit.

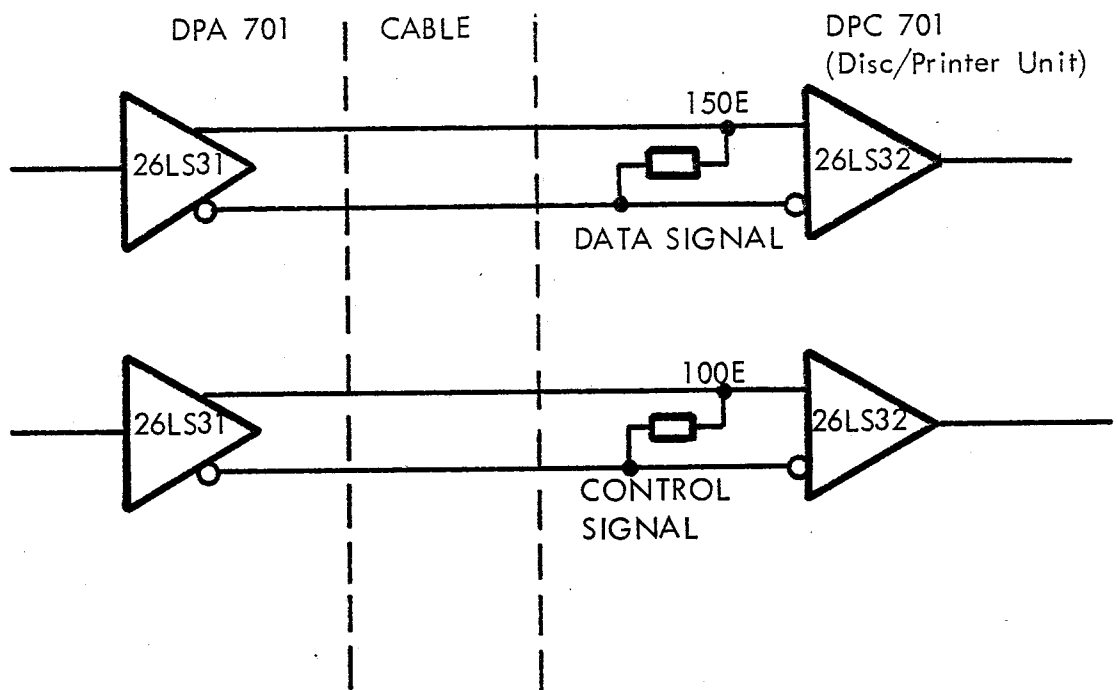


Fig. 2. Transmitter-receiver Connection

On figure 2 is shown the Transmitter-receiver Connection together with the used termination. The termination is always placed at the receiver side. The signals from DPC701 to DPA701 are equal to those shown on figure 2.

Enable of the drivers and receivers together with the direction of the data bus is controlled by the PAL-circuit, PAT577.

Figure 3 gives the logical description of this circuit. This circuit accepts all I/O commands where /PCS5 (Peripheral Chip Select from the CPU) = 0, i.e. I/O addresses 280H-2FFH.

PAL16L8
 PAT577
 BUS CONTROLLER TO DPA701

PAL DESIGN SPECIFICATION
 1984.05.01, KNEH

/PCSS DT /DEN /IORD /IOWR RESET ALE 8 9 GND
 11 12 13 14 15 /EDIN EADD EDOUT 19 VCC

IF (VCC) /17 = /ALE
 IF (VCC) /EADD = EDIN+EDOUT+RESET
 IF (VCC) /EDOUT = RESET+/PCSS+/DEN*/IOWR+/DT
 IF (VCC) EDIN = /RESET*PCSS*DEN*/DT

DESCRIPTION:

Fig. 3. Pal Design Specification PAT577

3. CHECK OUT PROCEDURE

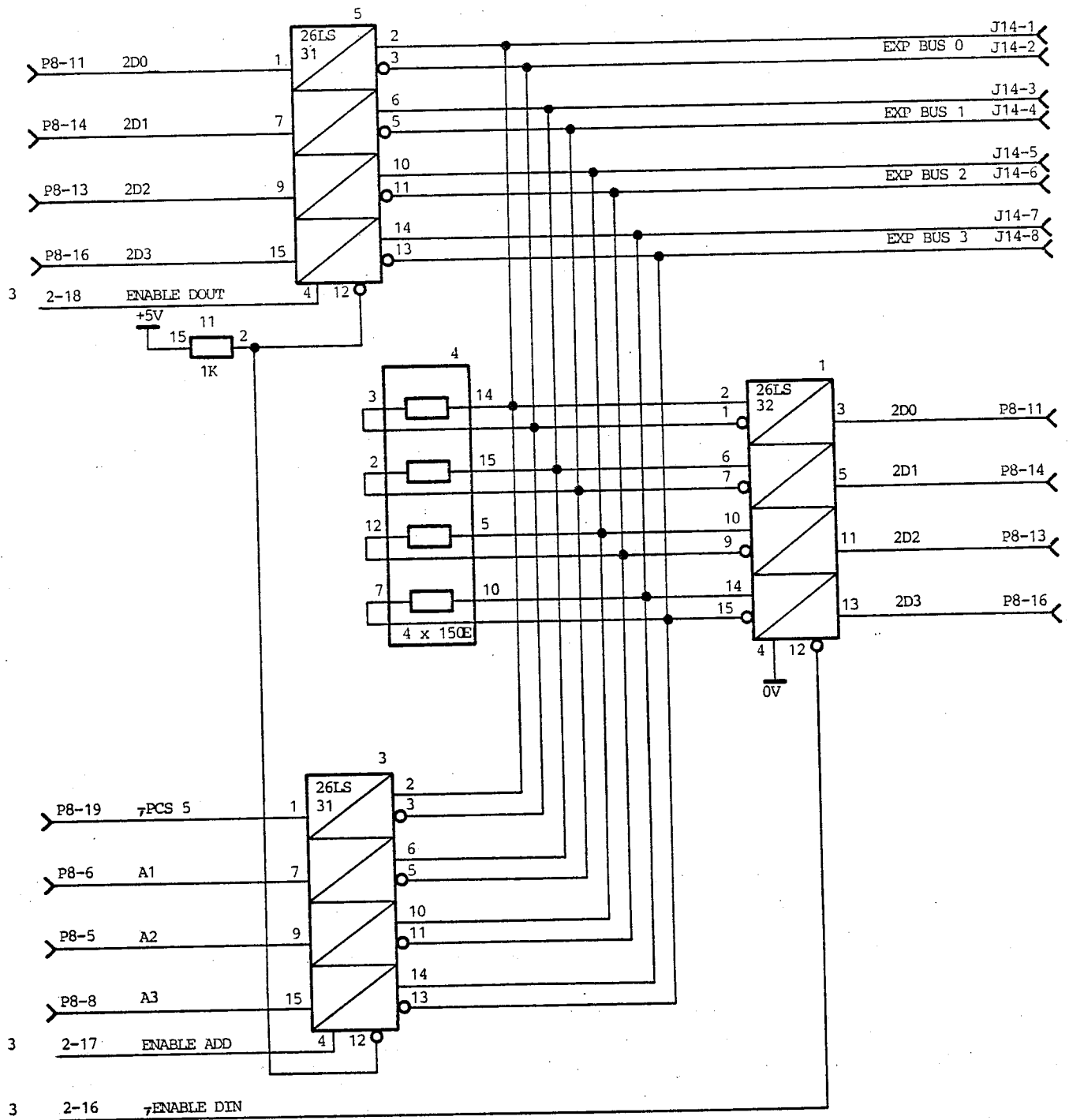
3.

The DPA701 is checked by using the built in Floppy test and printer test described in the RC759, iAPX186, PC, Selftest (RCSL 19 0 00760) Refer to this document for details about running these tests.

4. Logic Diagrams

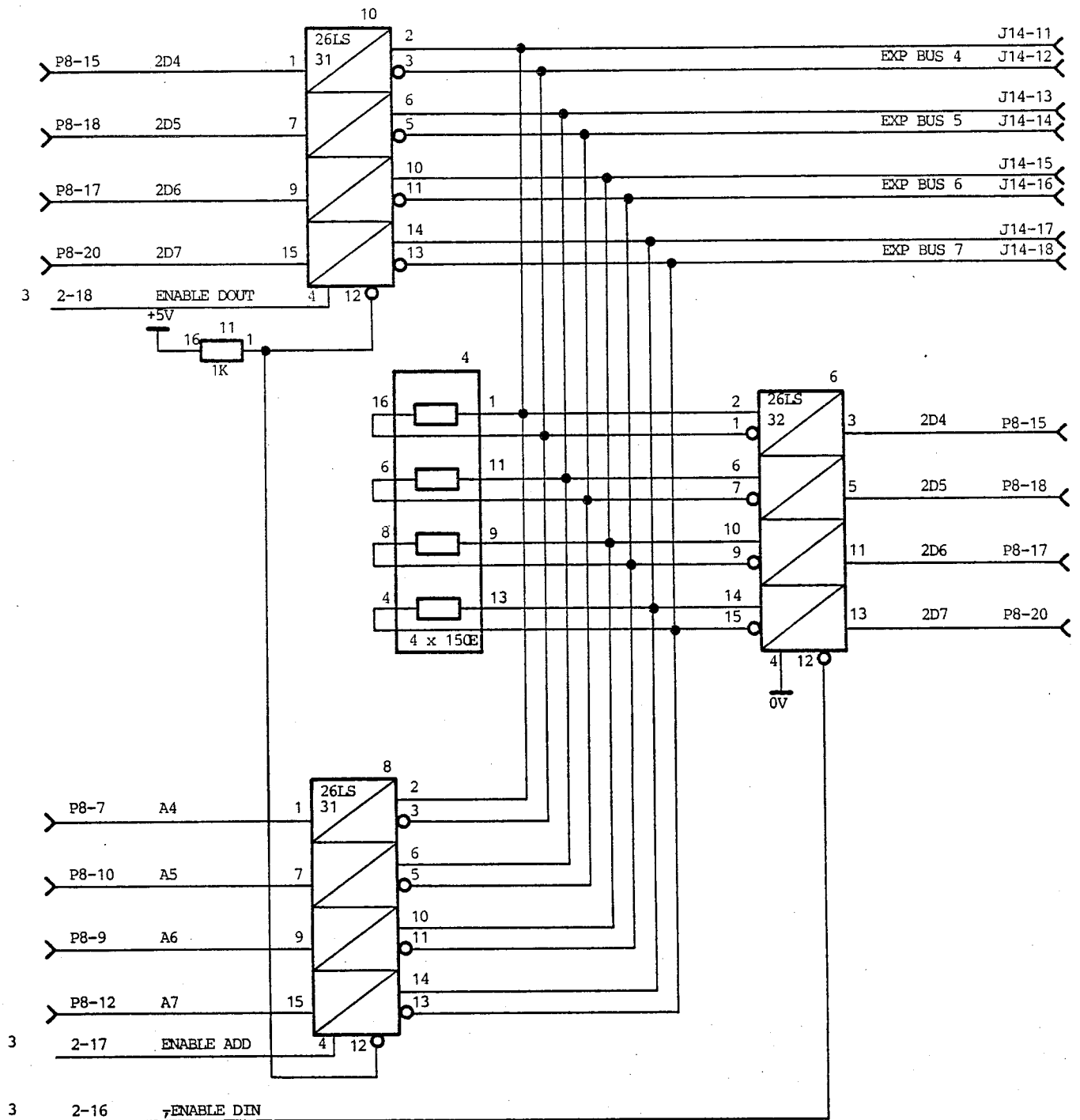
4.

Signal Name	Destination	Description
EXP BUS 0-3	J14	EXPander BUS bit 0-3. This bus is a multiplexed Address/ Data bus; controlled by /DEN and DT//R. When /DEN = 1 this bus contains address bits A1 - A7. When /DEN = 0 this bus acts as a bidirectional data; the direction is controlled by DT//R.
2DO-D3	P8	Bidirectional data bus interfacing to CPU740.



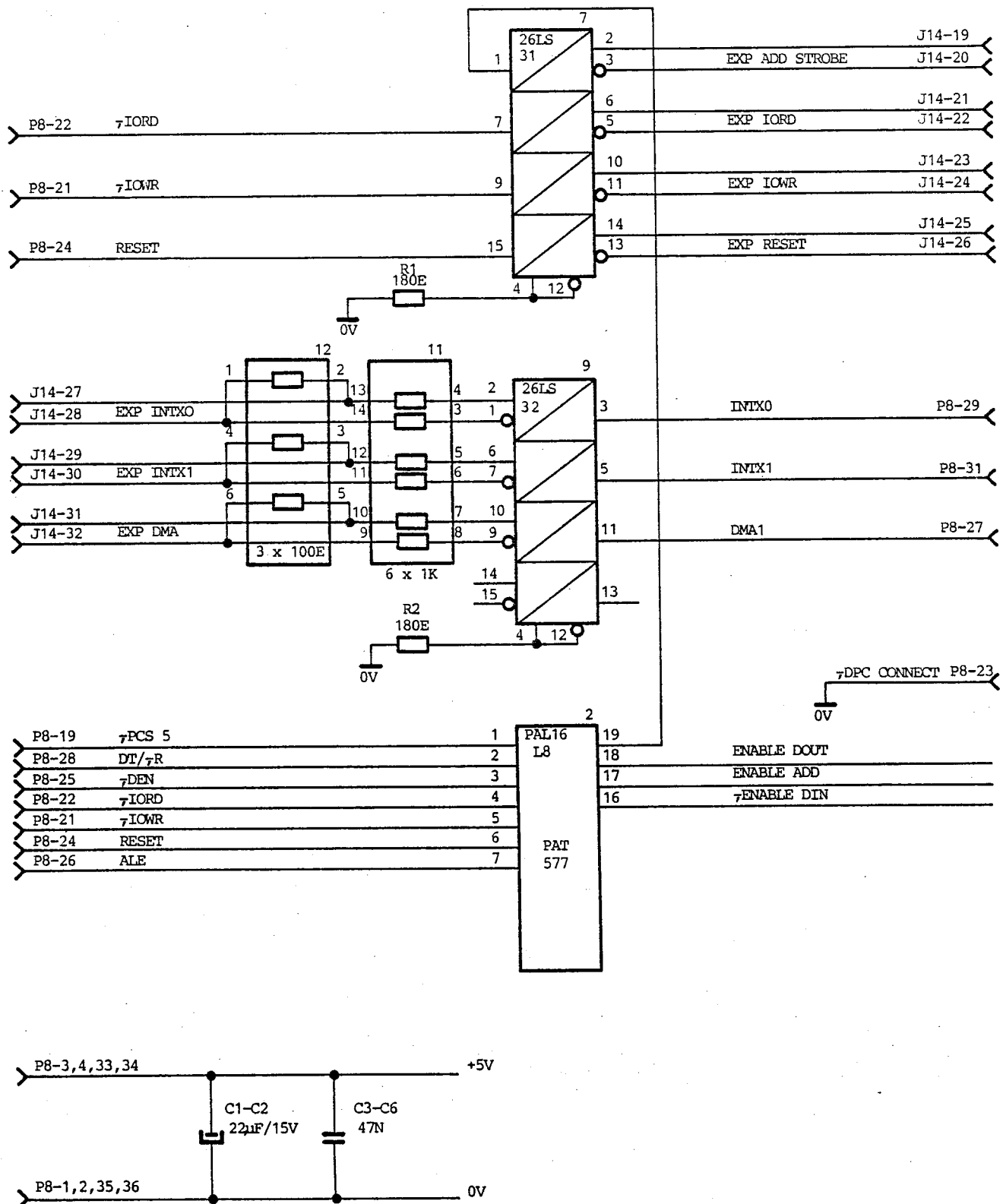
840124/KNIEH 840516/AMS 840516/LLM

Signal Name	Destination	Description
EXPBUS 4-7	J14	EXPander bus bit 4-7. This bus is a multiplexed Address/ data bus; controlled by /DEN. /DEN = 1 Address phase. /DEN = 0 Data phase. In data phase DT//R controls the transfer direction.
2D4-7	P8	Bidirectional data bus interfa- cing to CPU740.

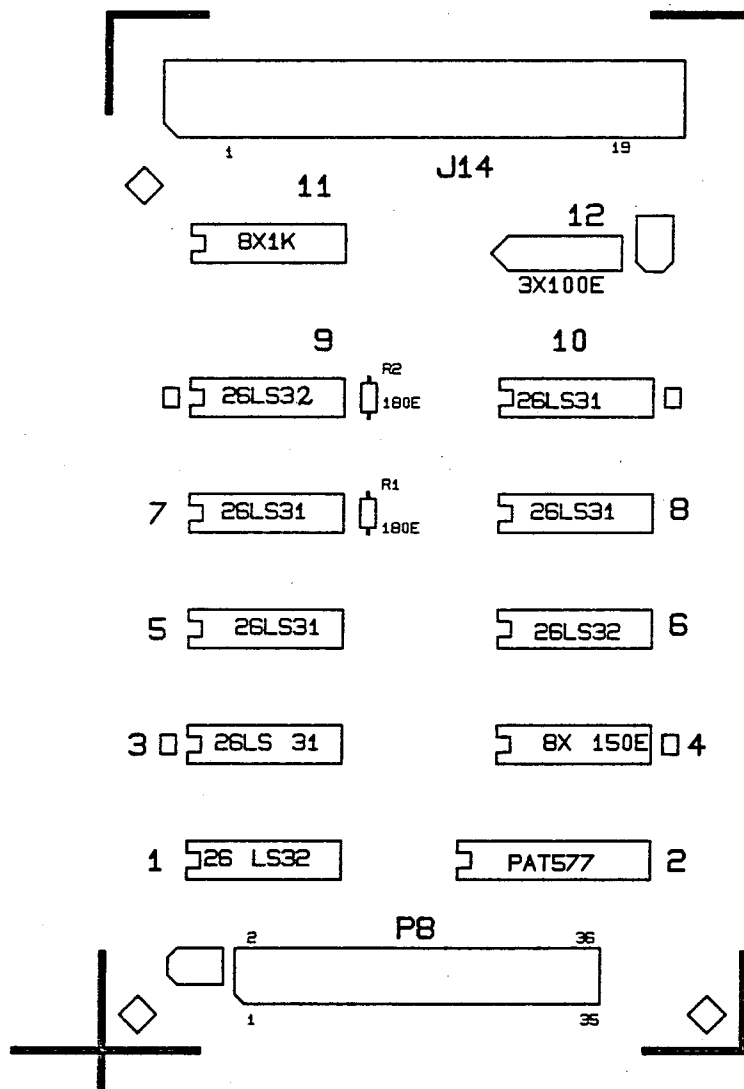


840124/KNEH 240516/AMS 840516/LLM

Signal Name	Destination	Description
EXP ADD STROBE	J14	EXPander ADDRESS STROBE. Used to latch the address supplied on EXPBUS 0-7.
EXP IORD	J14	EXPander I/O Read pulse.
EXP IOWR	J14	EXPander I/O Write pulse.
ENABLE ADD	p.1 p.2	ENABLE the ADDRESS bus drivers.
ENABLE DOUT	p.1 p.2	ENABLE expander bus Data OUT drivers.
/ENABLE DIN	p.1 p.2	ENABLE expander bus Data IN receivers.
/DPC CONNECT	P8	Indicates to the hardware configuration program in CPU740 that a DPA module is connected.
INTX0	P8	Interrupt from the Expander bus (Floppy).
INTX1	P8	Interrupt from the Expander bus (Printer).
DMA1	P8	Expander bus DMA request.



840124/KNEH 840516/AMS 840516/LLM



PCB125 COMPONENT NOTATION

Fig. 4. Assembly Drawing

Pin number	Signal name
1	+EXP BUS 0
2	-EXP BUS 0
3	+EXP BUS 1
4	-EXP BUS 1
5	+EXP BUS 2
6	-EXP BUS 2
7	+EXP BUS 3
8	-EXP BUS 3
9	
10	
11	+EXP BUS 4
12	-EXP BUS 4
13	+EXP BUS 5
14	-EXP BUS 5
15	+EXP BUS 6
16	-EXP BUS 6
17	+EXP BUS 7
18	-EXP BUS 7
19	+EXP ADD STROBE
20	-EXP ADD STROBE
21	+EXP IORD
22	-EXP IORD
23	+EXP IOWR
24	-EXP IOWR
25	+EXP RESET
26	-EXP RESET
27	+EXP INTX 0
28	-EXP INTX 0
29	+EXP INTX 1
30	-EXP INTX 1
31	+EXP DMA
32	-EXP DMA

Fig. 5. Jack List J14

Pin number	Signal Name
1	Ov
2	Ov
3	+5V
4	+5V
5	A2
6	A1
7	A4
8	A3
9	A6
10	A5
11	2D0
12	A7
13	2D2
14	2D1
15	2D4
16	2D3
17	2D6
18	2D5
19	/PCS 5
20	2D7
21	/IOWR
22	/IORD
23	/DPC CONNECT
24	RESET
25	/DEN
26	ALE
27	DMA 1
28	DT//R
29	INTX0
30	
31	INTX1
32	
33	+5V
34	+5V
35	Ov
35	Ov

Fig. 6. Plug List P8

A. INDICES

A.

A.1 Survey of Figures

A.1

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RETURN LETTER

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